NOTES (UNLESS OTHERWISE SPECIFIED)

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).

2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
   Er - MUST BE FROM 4.2 TO 4.4

4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'

5. CHARACTERISTIC IMPEDANCE - SEE DETAIL "B"

6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .0045"/.005"

7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
   .05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
   2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - GREEN COLOR BOTH SIDES.
   MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP

10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.

14. TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.

15. 2 SOLDER SAMPLES TO BE PROVIDED.

16. BASIC GRID INCREMENT AT 1:1 IS .0001.

17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN,
   - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (94)

19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
   ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM.

21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER.PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

22. INTENTIONAL SHORTS AT:

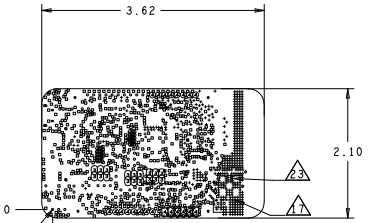
| Location | RefDes | Net 1 | | Net 2 |
|---|---|---|---|---|
| (466.00 1466.00) | SH501 | P3V3_SDA | & | SDA_VOUT33 |
| (484.00 1637.00) | J25 | SDA_RST_TGTMCU_J_B | & | SDA_RST_TGTMCU_B |
| (808.00 259.00) | SH503 | P_LED_PWR | & | N21175258 |
| (804.00 1691.00) | SH3 | VREFH/VREF_OUT | & | VREFH |
| (972.00 257.00) | J22 | VDD_BRD | & | VDD_MCU |
| (984.00 838.00) | SH500 | V_TGTMCU | & | P1V8_3V3_BRD |
| (1029.00 1645.00) | J29 | PTA17 | & | D12 |
| (920.00 1691.00) | SH4 | PTA18 | & | D13 |
| (1331.00 716.00) | J14 | SWD_CLK_TGTMCU_BUF | & | SWD_CLK_TGTMCU |
| (1331.00 916.00) | J13 | SWD_DIO_TGTMCU_BUF | & | PTA0_SWD_DIO |
| (1331.00 816.00) | J12 | PTA1_SWD_CLK | & | SWD_CLK_TGTMCU |
| (1163.00 1545.00) | J28 | PTA16 | & | D11 |
| (1266.00 1691.00) | SH7 | PTA19 | & | D10 |
| (1368.00 1692.00) | SH8 | PTC1 | & | D9 |
| (1468.00 1691.00) | SH9 | PTC5 | & | D8 |
| (1829.00 140.00) | SH25 | ADC0_DP0/CMP0_IN0 | & | A0 |
| (1622.00 1691.00) | SH10 | PTB0 | & | D7 |
| (1722.00 1691.00) | SH11 | PTC18 | & | D6 |
| (2027.00 140.00) | SH29 | PTB2 | & | A2 |
| (1929.00 140.00) | SH28 | PTB18 | & | A1 |
| (1874.00 1691.00) | SH12 | PTC17 | & | D5 |
| (1974.00 1691.00) | SH13 | PTC4 | & | D4 |
| (2097.00 139.00) | SH30 | PTB3 | & | A3 |
| (2208.00 1545.00) | J31 | UART0_TX_TGTMCU | & | D1 |
| (2078.00 1691.00) | SH14 | PTC16 | & | D3 |
| (2121.00 1691.00) | SH15 | PTC19 | & | D2 |
| (2342.00 1645.00) | J30 | UART0_RX_TGTMCU | & | D0 |
| (2581.00 824.00) | J37 | VDD_RFF | & | VDD_RF |

J16 PIN3 & PIN4
J17 PIN3 & PIN4
RF_ANT & GND

23. INTENTIONAL SHORT ON TOP LAYER BETWEEN RF_ANT AND GND

24. OVERALL PCB DIELECTRIC THICKNESS ARE TARGETED (A & C) 4.5 MILS+/-10% AND (B) 48 MILS +/-10%
AS SHOWN IN DETAIL 'A'. ADJUSTEMENT IN SUBSTRATE "C" IS ALLOWED TO MEET OVERALL HEIGHT REQUIREMENT.

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPROVED |
| | X2 | ORIGINAL RELEASE | 12-04-15 | A.Q |
| | X3 | LAYOUT UPDATE | 12-10-15 | A.Q |
| | A | BOM UPDATE, RF OPTIMIZATION | 03-10-16 | A.Q |
| | A1 | UPDATE SYMBOL WITH LIBRARY | 06-11-16 | |
| | A2 | LAYOUT UPDATE | 08-03-16 | |
| | B | SCHEMATIC AND LAYOUT UPDATES | 12-22-16 | |
| | B1 | SWAPPED QSPI SI AND SO SIGNALS | 01-13-17 | |
| | C | STACKUP, AND LAYOUT UPDATES | 03-24-17 | A.Q |
| | C1 | ADD CAP FOR PTC1-5 AND UPDATE J9 | 08-24-17 | |

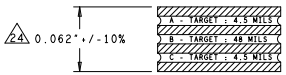



PRIMARY DATUM
GRID ORIGIN

DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%

| Layers | Single Ended | | Differential | | | Differential | | |
|---|---|---|---|---|---|---|---|---|
| | Trace Width (Mils) | Impedance (Ohms) | Trace Width (Mils) | Trace Spacing "to Target" (Mils) | Impedance (Ohms) | Trace Width (Mils) | Trace Spacing "to Target" (Mils) | Impedance (Ohms) |
| L1_PS | 8.00 | 50 | | | | | | |
| | | | | | | | | |

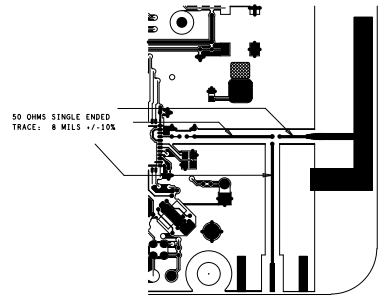
| DRILL CHART: TOP to BOTTOM<br>ALL UNITS ARE IN MILS | | | | |
|---|---|---|---|---|
| FIGURE | SIZE | TOLERANCE | PLATED | QTY |
| + | 8.0 | +0.0/-8.0 | PLATED | 512 |
| | 8.0 | +3.0/-3.0 | PLATED | 19 |
| ▫ | 10.0 | +0.0/-10.0 | PLATED | 702 |
| ◦ | 12.0 | +0.0/-12.0 | PLATED | 2 |
| ⌖ | 12.0 | +2.0/-2.0 | PLATED | 2 |
| ⊕ | 26.0 | +2.0/-2.0 | PLATED | 20 |
| ⊖ | 39.0 | +3.0/-3.0 | PLATED | 18 |
| ⌖ | 40.0 | +3.0/-3.0 | PLATED | 57 |
| ⊕ | 40.0 | +3.0/-3.0 | PLATED | 16 |
| ◪ | 41.0 | +3.0/-3.0 | PLATED | 6 |
| ▪ | 63.0 | +3.0/-3.0 | PLATED | 1 |
| ▪ | 73.0 | +3.0/-3.0 | PLATED | 2 |
| ▪ | 125.0 | +3.0/-3.0 | NON-PLATED | 4 |
| ▪ | 34.0x26.0 | +2.0/-2.0 | PLATED | 2 |
| ▬ | 60.0x33.0 | +2.0/-2.0 | PLATED | 2 |




| FINISHED Cu WEIGHT | | |
|---|---|---|
| LAYER 1 | TOP SIDE | 1 oz. |
| LAYER 2 | GROUND PLANE | 1 oz. |
| LAYER 3 | INTERNAL 1 | 1 oz. |
| LAYER 4 | BOTTOM SIDE | 1 oz. |

DETAIL A
LAYER STACKUP
SCALE: NONE

DETAIL B




___ PUBI (PUBLIC INFORMATION)
X NIUO (NXP INTERNAL USE ONLY)
___ NCP (NXP CONFIDENTIAL PROPRIETARY)



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
XX .01 ±5-30'
XXX .005
✓ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS. REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

| APPROVALS | DATE |
|---|---|
| DRAWN A. QUIROZ | 08/24/17 |
| CHECKED K. TILLEY | 08/24/17 |
| DESIGN ENGINEER A. QUIROZ | 08/24/17 |

PART NO. 170-29102

NXP SEMICONDUCTORS

6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
FRDM-KW41Z

| SIZE | CAD FILE NAME | DWG. NO. | REV |
|---|---|---|---|
| D | LAY-29102 | FAB-29102 | C1 |

SCALE 1/1 DO NOT SCALE DRAWING SHEET 1 OF 1