Freescale Semiconductor

MPC5566RM
Rev. 2.1, 05/2012

MPC5566 Microcontroller Reference Manual

This MPC5566 Reference Manual set consists of the following files:

- MPC5566 Reference Manual Addendum, Rev 2
- MPC5566 Microcontroller Reference Manual, Rev 2

freescale™ semiconductor

Freescale Semiconductor
Reference Manual Addendum

MPC5566RMAD
Rev. 2, 05/2012

MPC5566 Reference Manual Addendum

This errata document describes corrections to the *MPC5566 Microcontroller Reference Manual*, order number MPC5566RM. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com/powerarchitecture for the latest updates.

The current version available of the *MPC5566 Microcontroller Reference Manual* is Revision 2.0.

Table of Contents

freescale™ semiconductor

1 Addendum for Revision 2.0

Table 1. MPC5566RM Rev 2.0 addendum

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Section 12.4.2.7/Page 12-50</td><td>Change sentence “The bytes indicated as ‘—’ are not driven during that write cycle” to read “The bytes indicated as ‘—’ are indeterminate and may be driven during that write cycle.”</td></tr>
<tr><td>Table 12-21, “Data Bus Contents for Write Cycles”/Page 12-50</td><td>Replace table with the one below to correct information about data bus contents for write cycles. Note that only two columns have changed: under “32-Bit Port Size,” columns “D0:D7” and “D8:D15.”
<table>
<tr><th rowspan="2">Transfer Size</th><th rowspan="2">TSIZ [0:1]</th><th colspan="2">Address</th><th colspan="4">32-Bit Port Size</th><th colspan="2">16-Bit Port Size[1]</th></tr>
<tr><th>A30</th><th>A31</th><th>D0:D7</th><th>D8:D15</th><th>D16:D23</th><th>D24:D31</th><th>D0:D7</th><th>D8:D15</th></tr>
<tr><td rowspan="4">Byte</td><td>01</td><td>0</td><td>0</td><td>OP0</td><td>—</td><td>—</td><td>—</td><td>OP0</td><td>—</td></tr>
<tr><td>01</td><td>0</td><td>1</td><td>—</td><td>OP1</td><td>—</td><td>—</td><td>—</td><td>OP1</td></tr>
<tr><td>01</td><td>1</td><td>0</td><td>—</td><td>—</td><td>OP2</td><td>—</td><td>OP2</td><td>—</td></tr>
<tr><td>01</td><td>1</td><td>1</td><td>—</td><td>—</td><td>—</td><td>OP3</td><td>—</td><td>OP3</td></tr>
<tr><td rowspan="2">16-bit</td><td>10</td><td>0</td><td>0</td><td>OP0</td><td>OP1</td><td>—</td><td>—</td><td>OP0</td><td>OP1</td></tr>
<tr><td>10</td><td>1</td><td>0</td><td>—</td><td>—</td><td>OP2</td><td>OP3</td><td>OP2</td><td>OP3</td></tr>
<tr><td>32-bit</td><td>00</td><td>0</td><td>0</td><td>OP0</td><td>OP1</td><td>OP2</td><td>OP3</td><td>OP0/ OP2[2]</td><td>OP1/OP3</td></tr>
</table>
NOTES:
1 Also applies when DBM=1 for 16-bit data bus mode.
2 This case consists of two 16-bit external transactions, the first writing OP0 and OP1, the second writing OP2 and OP3.</td></tr>
<tr><td>Table 9-23, “DMA Request Summary for eDMA”/Page 9-43</td><td>Change two rows in the table to correct information about eSCI COMBTX DMA request. Only the Transmit Data Register Empty and LIN Transmit Data Ready flags drive the DMA request. The Transmit Complete flag is not used.
<table>
<tr><th>DMA Request</th><th>Channel</th><th>Source</th><th>Description</th></tr>
<tr><td>eSCIA_COMBTX</td><td>18</td><td>ESCIA.SR[TDRE] || ESCIA.SR[TC] || ESCIA.SR[TXRDY]</td><td>eSCIA combined DMA request of the Transmit Data Register Empty and LIN Transmit Data Ready DMA requests</td></tr>
<tr><td>eSCIB_COMBTX</td><td>34</td><td>ESCIB.SR[TDRE] || ESCIB.SR[TC] || ESCIB.SR[TXRDY]</td><td>eSCIB combined DMA request of the Transmit Data Register Empty and LIN Transmit Data Ready DMA requests</td></tr>
</table></td></tr>
</table>

Table 1. MPC5566RM Rev 2.0 addendum

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Figure 5-2, “Master Privilege Control Registers”/Page 5-5</td><td>Change read status for bits 20–31 from zero to reserved.
 
</td></tr>
<tr><td>Table A-1, “Module Base Addresses”/Page A-1</td><td>Correct names of peripheral bridge modules by adding underscore (PBRIDGEA becomes PBRIDGE_A, PBRIDGEB becomes PBRIDGE_B). Only two rows of the table are changed.
<table>
<tr><th>Module</th><th>Base Address</th><th>Page</th></tr>
<tr><td>Peripheral Bridge A (PBRIDGE_A)</td><td>0xC3F0_0000</td><td>Page A-2</td></tr>
<tr><td>Peripheral Bridge B (PBRIDGE_B)</td><td>0xFFF0_0000</td><td>Page A-35</td></tr>
</table></td></tr>
<tr><td>Table A-2, “MPC5566 Detailed Register Map”/Page A-2</td><td>Correct names of peripheral bridge A control registers by adding underscore (PBRIDGEA_x becomes PBRIDGE_A_x).
<table>
<tr><th>Register Description</th><th>Register Name</th><th>Used Size</th><th>Address</th></tr>
<tr><td>Peripheral bridge A master privilege control register</td><td>PBRIDGE_A_MPCR</td><td>32-bit</td><td>Base + 0x0000</td></tr>
<tr><td>Reserved</td><td>—</td><td>—</td><td>Base + (0x0004-0x001F)</td></tr>
<tr><td>Peripheral bridge A peripheral access control register 0</td><td>PBRIDGE_A_PACR0</td><td>32-bit</td><td>Base + 0x0020</td></tr>
<tr><td>Reserved</td><td>—</td><td>—</td><td>Base + (0x0024-0x003F)</td></tr>
<tr><td>Peripheral bridge A off-platform peripheral access control register 0</td><td>PBRIDGE_A_OPACR0</td><td>32-bit</td><td>Base + 0x0040</td></tr>
<tr><td>Peripheral bridge A off-platform peripheral access control register 1</td><td>PBRIDGE_A_OPACR1</td><td>32-bit</td><td>Base + 0x0044</td></tr>
<tr><td>Peripheral bridge A off-platform peripheral access control register 2</td><td>PBRIDGE_A_OPACR2</td><td>32-bit</td><td>Base + 0x0048</td></tr>
<tr><td>Reserved</td><td>—</td><td>—</td><td>Base + (0x004C-0xC3F7_FFFF)</td></tr>
</table></td></tr>
</table>

Table 1. MPC5566RM Rev 2.0 addendum

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table A-2, “MPC5566 Detailed Register Map”/Pages A-36–A-37</td><td>Correct names of peripheral bridge B control registers by adding underscore (PBRIDGEB_x becomes PBRIDGE_B_x).
<table>
<tr><th>Register Description</th><th>Register Name</th><th>Used Size</th><th>Address</th></tr>
<tr><td>Peripheral bridge B master privilege control register</td><td>PBRIDGE_B_MPCR</td><td>32-bit</td><td>Base + 0x0000</td></tr>
<tr><td>Reserved</td><td>—</td><td>—</td><td>Base + (0x0004-0x001F)</td></tr>
<tr><td>Peripheral bridge B peripheral access control register 0</td><td>PBRIDGE_B_PACR0</td><td>32-bit</td><td>Base + 0x0020</td></tr>
<tr><td>Reserved</td><td>—</td><td>—</td><td>Base + (0x0024-0x0027)</td></tr>
<tr><td>Peripheral bridge B peripheral access control register 2</td><td>PBRIDGE_B_PACR2</td><td>32-bit</td><td>Base + 0x0028</td></tr>
<tr><td>Reserved</td><td>—</td><td>—</td><td>Base + (0x002C-0x003F)</td></tr>
<tr><td>Peripheral bridge B off-platform peripheral access control register 0</td><td>PBRIDGE_B_OPACR0</td><td>32-bit</td><td>Base + 0x0040</td></tr>
<tr><td>Peripheral bridge B off-platform peripheral access control register 1</td><td>PBRIDGE_B_OPACR1</td><td>32-bit</td><td>Base + 0x0044</td></tr>
<tr><td>Peripheral bridge B off-platform peripheral access control register 2</td><td>PBRIDGE_B_OPACR2</td><td>32-bit</td><td>Base + 0x0048</td></tr>
<tr><td>Peripheral bridge B off-platform peripheral access control register 3</td><td>PBRIDGE_B_OPACR3</td><td>32-bit</td><td>Base + 0x004C</td></tr>
<tr><td>Reserved</td><td>—</td><td>—</td><td>(Base + 0x0050)-0xFFF0_3FFF)</td></tr>
</table></td></tr>
</table>

Table 1. MPC5566RM Rev 2.0 addendum

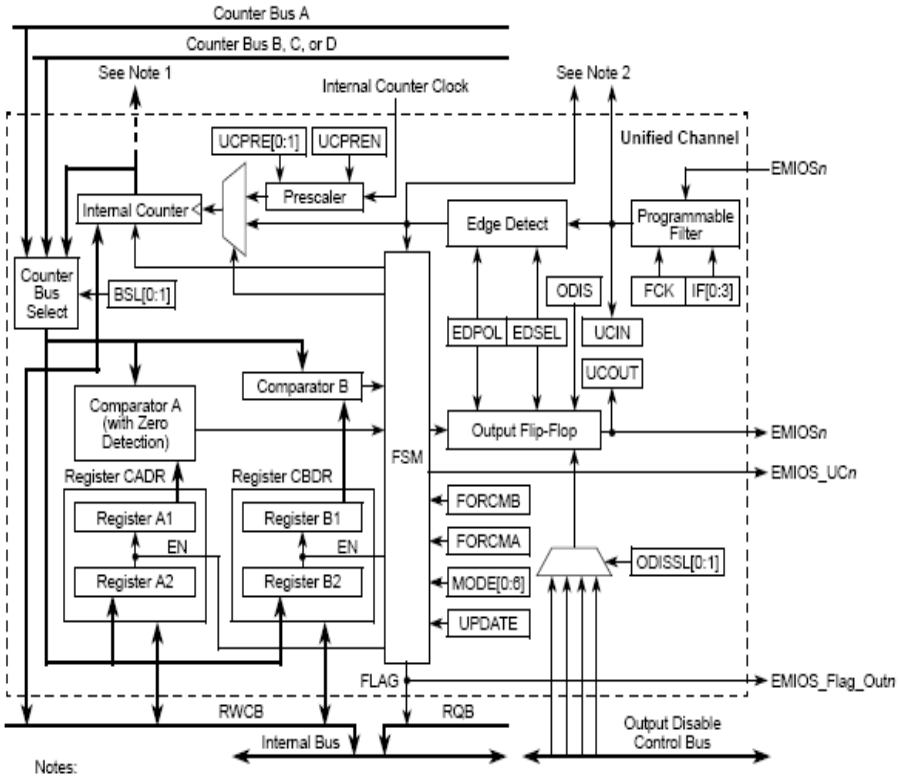
Location	Description
Figure 17-13, “Unified Channel Block Diagram”/Page 17-26	Reverse the arrow between the "Programmable Filter" and "Edge Detect".  **Figure 17-13. Unified Channel Block Diagram**
Section 9.3.1 eDMA Microarchitecture/ Page 9-33	In the Memory controller sub-bullet, delete the line "The hooks to a BIST controller for the local TCD memory are included in this module".
Section 9.2.2.13, “eDMA Interrupt Request Registers (EDMA_IRQRH, EDMA_IRQRL)”/ Page 9-19	In the third paragraph, remove the last line "without the need to perform a read-modify-write sequence to the EDMA_IRQRH and EDMA_IRQRL".
Section 8.3: Initialization and Application Information/Page 8-15	Change the sentence, “There are eight ECC check bits for each 64-bit data doubleword” to the following: • SRAM—Eight ECC check bits for each 64-bit SRAM data doubleword. • Flash—Eight ECC check bits for each 64-bit flash data doubleword.
Table 6-152, “SIU_DISR Field Descriptions”/ Page 6-113	• Bit 14-15–TRIGSELB: Correct the input select description as follows: 00: Replace the term “Invalid value” with “No Trigger” • Bit 22-23–TRIGSELC: Correct the input select description as follows: 00: Replace the term “Invalid value” with “No Trigger” • Bit 30-31–TRIGSELD: Correct the input select description as follows: 00: Replace the term “Invalid value” with “No Trigger”

Table 1. MPC5566RM Rev 2.0 addendum

Location	Description
Figure 11-9, “Synthesizer Status Register (FMPLL_SYNSR)”/Page 11-16	Correct the figure to reflect bits 23:28 and bits 30:31 as read-only. Address: Base + 0x0004 Access: User R/W **Synthesizer Status Register (FMPLL_SYNSR)** [1] Reset state determined during reset configuration. [2] Reset state determined during reset. **Note:** “w1c” signifies that this bit is cleared by writing a 1 to it.
Section 10.3.1.3, “INTC Interrupt Acknowledge Register (INTC_IACKR)”/Page 10-12	Remove the first paragraph from the “Note”: “The INTC_IACKR must not be read speculatively while in software vector mode. Therefore, for future compatibility, the TLB entry covering the INTC_IACKR must be configured to be guarded.”
Table 10-3. INTC Memory Map/Page 10-9	Add the following note at the end of this table: **Note:** To ensure compatibility with all PowerPC processors, the TLB entry covering the INTC memory map must be configured as guarded, both in software and hardware vector modes. • In software vector mode, the INTC_IACKR must not be read speculatively. • In hardware vector mode, guarded writes to the INTC_CPR or INTC_EOIR complete before the interrupt acknowledge signal from the processor asserts.
Table 10-9. MPC5566 Interrupt Request Sources/ Page 10-28	Update the note at the end of this table as follows: **Note:** The INTC has no spurious vector support. Therefore, if an asserted peripheral or software settable interrupt request (whose PRI value in INTC_PSRn is higher than the PRI value in INTC_CPR) negates before the interrupt request to the processor for that peripheral or software settable interrupt request is acknowledged, the interrupt request to the processor still can assert or remain asserted for that peripheral or software settable interrupt request. If the interrupt request to the processor does assert or does remain asserted: • The interrupt vector will correspond to that peripheral or software settable interrupt request. • The PRI value in the INTC_CPR will be updated with the corresponding PRI value in INTC_PSRn. Furthermore, clearing the peripheral interrupt request's enable bit in the peripheral or, alternatively, setting its mask bit has the same consequences as clearing its flag bit.Setting its enable bit or clearing its mask bit while its flag bit is asserted has the same effect on the INTC as an interrupt event setting the flag bit.

Table 1. MPC5566RM Rev 2.0 addendum

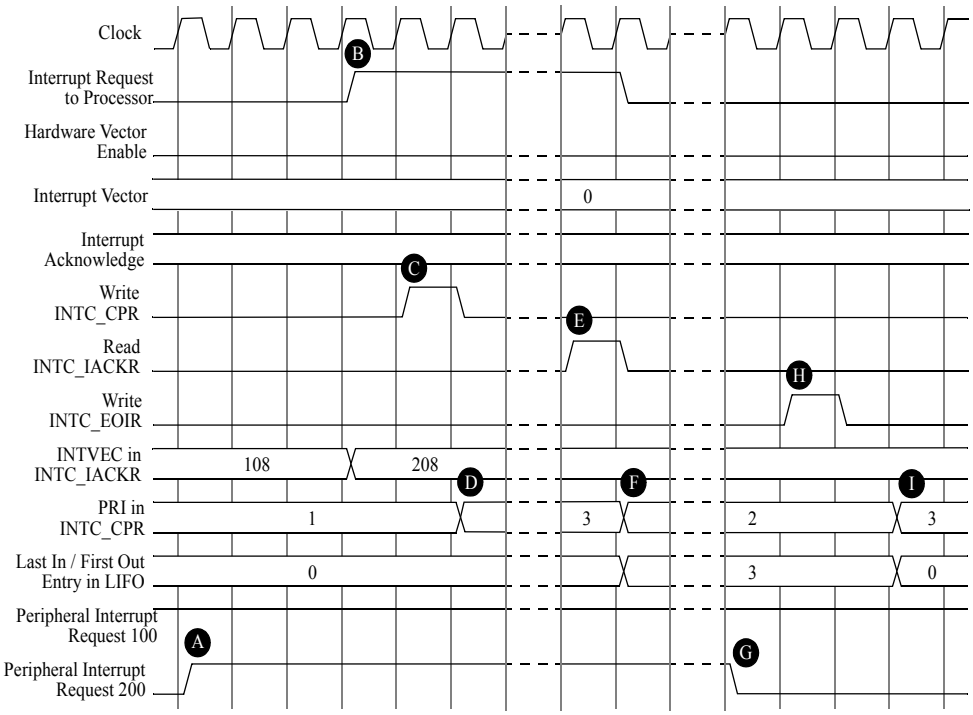
Location	Description
Section 10.4.2.1.4, “Priority Comparator Submodule”/ Page 10-30	Add the following paragraph to this section: One consequence of the priority comparator design is that once a higher priority interrupt is captured, it must be acknowledged by the CPU before a subsequent interrupt request of even higher priority can be captured. For example, if the CPU is executing a priority level 1 interrupt, and a priority level 2 interrupt request is captured by the INTC, followed shortly by a priority level 3 interrupt request to the INTC, the level 2 interrupt must be acknowledged by the CPU before a new level 3 interrupt will be generated.
Section 10.5.5.2, “Ensuring Coherency”/ Page 10-37	Move the content of this section under a new heading Section 10.5.5.2.1, “Interrupt with Blocked Priority”. Add the following paragraph to this section: **Section 10.5.5.2.2: Raised Priority Preserved** Before the instruction after the GetResource system service executes, all pending transactions have completed. These pending transactions can include an ISR for a peripheral or software settable interrupt request whose priority was equal to or lower than the raised priority. Also, during the epilog of the interrupt exception handler for this preempting ISR, the raised priority has been restored from the LIFO to PRI in INTC_CPR. The shared coherent data block now can be accessed coherently. Following figure shows the timing diagram for this scenario, and the table explains the events. The example is for software vector mode, but except for the method of retrieving the vector and acknowledging the interrupt request to the processor, hardware vector mode is identical.  **Raised Priority Preserved Timing Diagram**

Table 1. MPC5566RM Rev 2.0 addendum

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td></td><td>
Raised Priority Preserved Events
<table>
<tr><th>Event</th><th>Description</th></tr>
<tr><td>A</td><td>Peripheral interrupt request 200 asserts during execution of ISR108 running at priority 1.</td></tr>
<tr><td>B</td><td>Interrupt request to processor asserts. INTVEC in INTC_IACKR updates with vector for that peripheral interrupt request.</td></tr>
<tr><td>C</td><td>ISR108 writes to INTC_CPR to raise priority to 3 before accessing shared coherent data block.</td></tr>
<tr><td>D</td><td>PRI in INTC_CPR now at 3, reflecting the write. This write, just before accessing data block, is the last instruction the processor executes before being interrupted.</td></tr>
<tr><td>E</td><td>Interrupt exception handler prolog acknowledges interrupt by reading INTC_IACKR.</td></tr>
<tr><td>F</td><td>PRI of 3 pushed onto LIFO. PRI in INTC_CPR updates to 2, the priority of ISR208.</td></tr>
<tr><td>G</td><td>ISR208 clears its flag bit, deasserting its peripheral interrupt request.</td></tr>
<tr><td>H</td><td>Interrupt exception handler epilog writes to INTC_EOIR.</td></tr>
<tr><td>I</td><td>LIFO pops 3, restoring the raised priority onto PRI in INTC_CPR. Next value to pop from LIFO is the priority from before peripheral interrupt request 100 interrupted. ISR108 now can access data block coherently after interrupt exception handler executes rfi instruction.</td></tr>
</table>
</td></tr>
<tr><td>Section 6.3.1.125 “Pad Configuration Register 218 (SIU_PCR218)”</td><td>• Changed PA field from two bits to one bit
• Figure 6-126: Change note 2 to “... set the PA field to 0b0”.
• Table 6-122. PCR218 “PA Field Definition” change as shown below:
0b0 FCK
0b1 AN[15]</td></tr>
<tr><td>Section 19.4.5.4.1 “Calibration Overview”</td><td>Remove the braces from the equation “CAL_RES = GCC x (RAW_RES + OCC + 2)”.</td></tr>
<tr><td>Section 11.3.1.1 “Synthesizer Control Register (FMPLL_SYNCR)”</td><td>Deleted the last note in PREDIV field description that states:
“To use the 8–20 MHz OSC, the PLL predivider must be configured for divide-by-two operation by tying PLLCFG[2] low (set PREDIV to 0b000).”</td></tr>
</table>

2 Revision history

Table 2 provides a revision history for this document.

Table 2. Revision history

Revision	Substantive changes	Date of release
1.0	• Initial release. Corrected errors in chapter 12, “External Bus Interface (EBI).”	10/2009
2.0	• Corrected errors in chapter 9, “Enhanced Direct Memory Access (eDMA).” • Corrected errors in chapter 5, “Peripheral Bridge (PBRIDGE A and PBRIDGE B).” • Corrected peripheral bridge name errors in appendix A, “MPC5566 Register Map.” • Corrected unified channel block diagram in chapter 16, “Enhanced Modular Input/Output Subsystem (eMIOS). • Clarified the description in Section 9.4.1, “eDMA Microarchitecture”. • Clarified the description in Section 9.3.1.13, “eDMA Interrupt Request Registers (EDMA_IRQRL). • Clarified note in the INTC Interrupt Acknowledge Register • Added a note in the INTC Memory Map table • Clarified note at the end of the MPC5566 Interrupt Request Sources table • Added a paragraph to the Section 10.4.2.1.4, “Priority Comparator Submodule” • Updated Section 10.5.5.2, “Ensuring Coherency” • Corrected table “PCR218 PA Field Definition” and figure “AN[15]_FCK Pad Configuration Register (SIU_PCR218)” and note 2 under figure. • Deleted the last note in PREDIV field description of Synthesizer Control Register (FMPLL_SYNCR) that states	05/2012

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

MPC5566RMAD
Rev. 2
05/2012

MPC5566 Microcontroller Reference Manual

Devices Supported:

MPC5566

MPC5566 RM
Rev. 2.0
23 Apr 2008

freescale™
semiconductor

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 26668334
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

MPC5566 RM
Rev. 2.0
23 Apr 2008

Chapter 1
Introduction

Chapter 2
Signal Description

Chapter 3
e200z6 Core Complex

Chapter 4
Reset

Chapter 5
Peripheral Bridge (PBRIDGE A and PBRIDGE B)

Chapter 6
System Integration Unit (SIU)

Chapter 7
Crossbar Switch (XBAR)

Chapter 8
Error Correction Status Module (ECSM)

Chapter 9
Enhanced Direct Memory Access (eDMA)

Chapter 10
Interrupt Controller (INTC)

Chapter 11
Frequency Modulated Phase Locked Loop and System Clocks (FMPLL)

Chapter 12
External Bus Interface (EBI)

Chapter 13
Flash Memory

Chapter 14
Internal Static RAM (SRAM)

Chapter 15
Fast Ethernet Controller (FEC)

Chapter 16
Boot Assist Module (BAM)

Chapter 17
Enhanced Modular Input/Output Subsystem (eMIOS)

Chapter 18
Enhanced Time Processing Unit (eTPU)

Chapter 19
Enhanced Queued Analog-to-Digital Converter (eQADC)

Chapter 20
Deserial Serial Peripheral Interface (DSPI)

Chapter 21
Enhanced Serial Communication Interface (eSCI)

Chapter 22
FlexCAN2 Controller Area Network

Chapter 23
Voltage Regulator Controller (VRC) and POR Module

Chapter 24
IEEE 1149.1 Test Access Port Controller (JTAGC)

Chapter 25
Nexus Development Interface

Appendix A
MPC5566 Register Map

Appendix B
Calibration

Appendix C
MPC5566 Reference Manual Revision History

Chapter 1
Introduction

1.1 Overview

The MPC5566 microcontroller (MCU) is a member of the MPC5500 family of next generation powertrain microcontrollers built on Power Architecture™ technology. The MPC5500 family contains a host processor core that complies with the Power Architecture embedded category, which is 100 percent user mode compatible with the original Power PC™ user instruction set architecture (UISA). This family of parts contains many new features coupled with high-performance CMOS technology to provide significant performance improvement over the MPC565.

The e200z6 CPU of the MPC5500 family is part of the family of CPU cores that implement versions built on the Power Architecture embedded category. This core also has additional instructions, including digital signal processing (DSP) instructions, beyond the classic PowerPC instruction set.

The MPC5566 has the following memory hierarchy:

Unified cache	32 KB unified cache
SRAM	128 KB of internal SRAM
Flash	3 MB flash memory

The fastest accesses are to the unified cache.Both the internal SRAM and the flash memory hold instructions and data. The external bus interface is designed to support most of the standard memories used with the MPC5xx family.

The complex I/O timer functions of the MPC5500 family are performed by two enhanced time processor unit engines (eTPUs). Each eTPU engine controls 32 hardware channels. The eTPU has been enhanced over the TPU by providing 24-bit timers, double-action hardware channels, a variable number of parameters per channel, angle clock hardware, and additional control and arithmetic instructions. Each eTPU is programmed using a high-level programming language.

The timer functions of the MPC5500 family are performed by the enhanced modular input/output system (eMIOS). The eMIOS' 24 hardware channels are capable of single action, double action, pulse-width modulation (PWM), and modulus counter operation. Motor control capabilities include edge-aligned and center-aligned PWM.

Off-chip communication is performed by a suite of serial protocols including:

- 4 controller area networks (FlexCANs);
- 4 enhanced deserial/serial peripheral interface (DSPIs); and
- 2 enhanced serial communications interfaces (eSCIs).

The DSPIs support pin reduction through hardware serialization and deserialization of timer channels and general-purpose input/output (GPIO) signals.

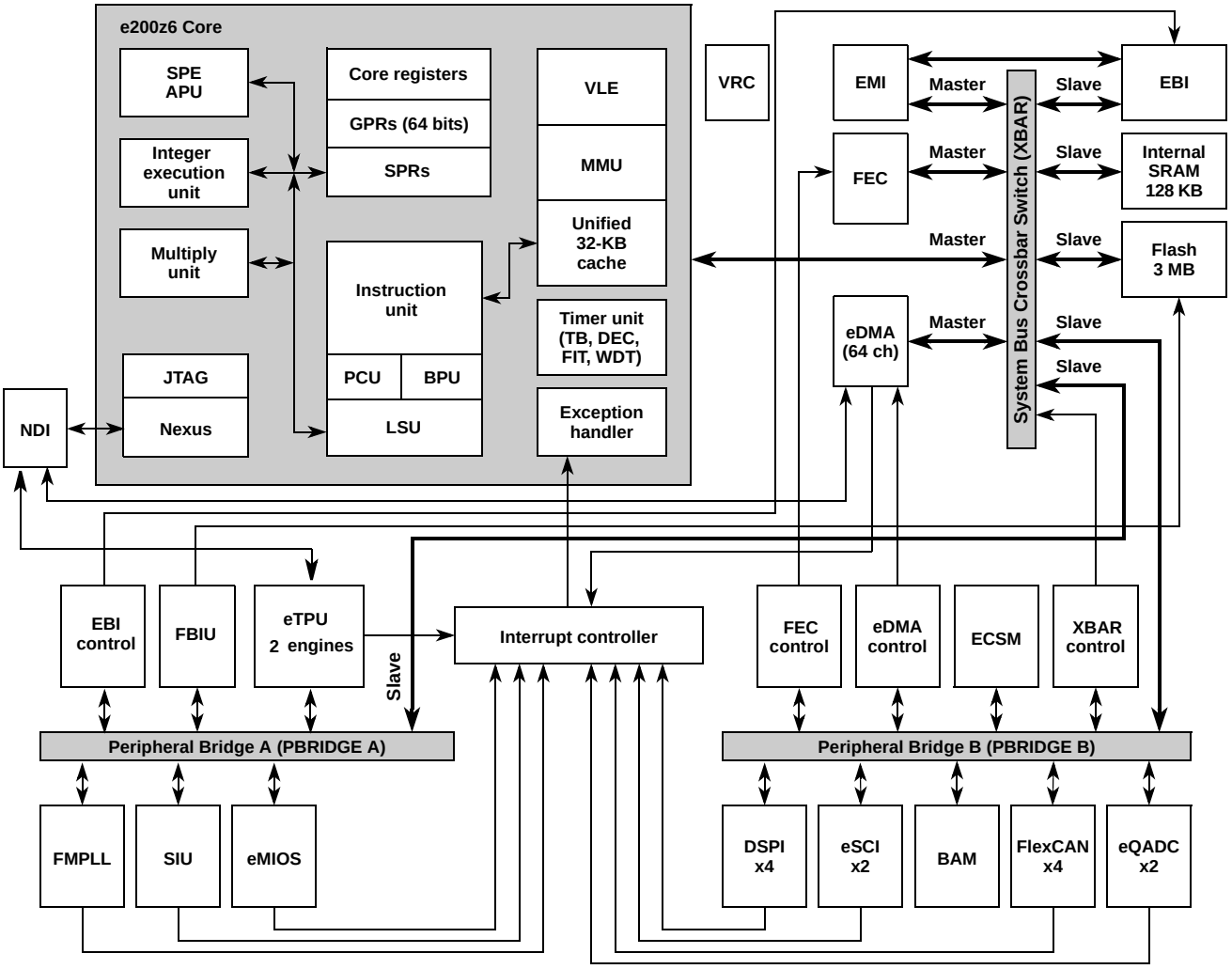
The MCU has two on-chip 40-channel enhanced queued dual analog to digital converters (eQADC).

The system integration unit (SIU) performs several chip-wide configuration functions. Pad configuration and general-purpose input and output (GPIO) are controlled from the SIU. External interrupts and reset control are also found in the SIU. The internal multiplexer submodule (SIU_DISR) provides multiplexing of eQADC trigger sources, daisy chaining the DSPIs, and external interrupt signal multiplexing.

The Fast Ethernet (FEC) module is a RISC-based controller that supports both 10 and 100 Mbps Ethernet/IEEE® 802.3 networks and is compatible with three different standard MAC (media access controller) PHY (physical) interfaces to connect to an external Ethernet bus. The FEC supports the 10 or 100 Mbps MII (media independent interface), and the 10 Mbps-only with a seven-wire interface, which uses a subset of the MII signals. The upper 16-bits of the 32-bit external bus interface (EBI) are used to connect to an external Ethernet device. The FEC contains built-in transmit and receive message FIFOs and DMA support.

1.2 Block Diagram

Figure 1-1 is a block diagram of the MPC5566.



MPC5566 device modules

BAM – Boot assist module
CAN – Controller area network (FlexCAN)
DSPI – Deserial/serial peripheral interface
EBI – External bus interface
ECSM – Error correction status module
EMI – External master interface
eDMA – Enhanced direct memory access
eMIOS – Enhanced modular I/O system
eQADC – Enhanced queued analog/digital converter
eSCI – Enhanced serial communications interface
eTPU – Enhanced time processing units
FBIU – Flash bus interface unit
FEC – Fast Ethernet controller
FMPLL – Frequency modulated phase-locked loop
NDI – Nexus developmental interface
SIU – System integration unit
SRAM – Internal static RAM
VRC – Voltage regulator controller
XBAR – System bus crossbar switch

Legend

e200z6 core components

APU – Auxiliary processing unit
BIU – Bus interface unit
BPU – Branch processing unit
DEC – Decrementer
FIT – Fixed interval timer
GPR – General-purpose register
JTAG – JTAG controller
LSU – Load/store unit
MMU – Memory management unit
PCU – Program counter unit
SPE – Signal processing engine
SPR – Special purpose register
TB – Time base
VLE – Variable length encoding
WDT – Watchdog timer
↔ – System bus

Figure 1-1. MPC5566 Block Diagram

1.3 Features

This section provides a high-level description of the features found in the MPC5566.

- Operating parameters
  - Fully static operation, up to 144 MHz
  - –40 to 150 °C junction temperature
  - Low-power design
    - Less than 1.2 Watts power dissipation
    - Designed for dynamic power management of core and peripherals
    - Software-controlled clock gating of peripherals
    - Separate power supply for stand-by operation for portion of internal SRAM
  - Fabricated in 0.13 μm process
  - 1.5 V internal logic
  - Input and output pins with 3.0–5.25 V range
    - 35% or 65% V_{DDEH} CMOS switch levels (with hysteresis)
    - Selectable hysteresis
    - Selectable slew rate control
  - External bus support 1.62–3.6 V operation and Nexus pins support 2.5–3.6 V operation
    - Selectable drive strength control
    - Unused pins configurable as GPIO
  - Designed with EMI reduction techniques
    - Frequency modulated phase-locked loop
    - On-chip bypass capacitance
    - Selectable slew rate and drive strength
- High-performance e200z6 core processor
  - 32-bit CPU built on Power Architecture™ technology
  - Freescale Variable Length Encoding (VLE) enhancements for code size footprint reduction
  - Thirty-two 64-bit general-purpose registers (GPRs)
  - Memory management unit (MMU) with 32-entry associative translation look-aside buffer (TLB)
  - Branch processing unit
  - Fully pipelined load/store unit
  - 32 KB unified cache with line locking
    - 4 or 8-way set associative
    - Two 32-bit fetches per clock
    - 8-entry store buffer
    - Way locking

  - Supports assigning cache as instruction or data only on a per-way basis
  - Supports tag and data parity
- Vectored interrupt support
- Interrupt latency is less than 70 ns @132 MHz (measured from interrupt request to execution of first instruction of interrupt exception handler)
- Reservation instructions for implementing read-modify-write constructs (internal SRAM and flash)
- Signal processing engine (SPE) auxiliary processing unit (APU) operating on 64-bit GPRs
- Floating point
  - IEEE® 754 compatible with software wrapper
  - Single precision in hardware, double precision with software library
  - Conversion instructions between single precision floating point and fixed point
- Long cycle time instructions, except for guarded loads. Do not increase interrupt latency in the MPC5566 to reduce latency; long cycle time instructions are aborted upon interrupt requests.
- Extensive system development support through Nexus debug module

• System bus crossbar switch (XBAR)
- Four master ports, five slave ports
- 32-bit address bus, 64-bit data bus
- Simultaneous accesses from different masters to different slaves (there is no clock penalty when a parked master accesses a slave)

• Enhanced direct memory access (eDMA) controller
- 64 channels support independent 8-, 16-, 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer

• Interrupt controller (INTC)
- 329 interrupt request registers [1]
  - 298 peripheral interrupt requests
  - 8 software settable sources
  - 26 reserved
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resources

1. Although this device has a maximum of 329 interrupts, the logic requires that the total number of interrupts be divisible by four. Therefore, the total number of interrupts specified for this device is 332.

- Frequency modulated phase-locked loop (FMPLL)
  - Input clock frequency: 8–20 MHz
  - Current controlled oscillator (ICO) range from 48 MHz to maximum device frequency
  - Reduced frequency divider (RFD) for reduced frequency operation without re-lock
  - Four selectable modes of operation
  - Programmable frequency modulation
  - Lock-detect circuitry continuously monitors lock status
  - Loss-of-clock (LOC) detection for reference and feedback clocks
  - Self-clocked mode (SCM) operation
  - On-chip loop filter (reduces number of external components required)
    - Engineering clock output configurable: Divide-by-2 to 126 of the system clock frequency
- External bus interface (EBI)
  - 1.8–3.3 V nominal I/O voltage
  - (the 496-pin VertiCal assembly has the calibration functionality).416 BGA: 32-bit data bus, 24-bit address bus (the 496-pin VertiCal assembly has the calibration functionality).
  - Memory controller with support for various memory types
    - Non-burst SDR flash and SRAM
    - Asynchronous and legacy flash and SRAM
    - Most standard memories used with the MPC5xx family
  - Configurable bus speed modes
    - 50% of system frequency
    - 25% of system frequency
  - Support for external master accesses to internal addresses
  - Burst support
  - Bus monitor
    - User selectable
    - Programmable timeout period (with eight external bus clock resolution)
  - Four chip selects: $\overline{\text{CS}}$[0:3] multiplexed with ADDR[8:11]
  - Four write/byte enable ($\overline{\text{WE}}$/$\overline{\text{BE}}$[0:3]) signals in the 416-pin package and the 496 pin assembly
  - Configurable wait states (via chip selects)
  - Optional automatic CLKOUT gating to save power and reduce EMI
  - Compatible with MPC5xx external bus (with some limitations)
    Selectable drive strengths; 10 pF, 20 pF, 30 pF, 50 pF
  - Chip selects: up to four chip selects (CAL_$\overline{\text{CS}}$[0:3])
- System integration unit (SIU)
    - Centralized GPIO control of bus pins: 416 BGA package: 178 pins
    - 416 CSP BGA package: 225 pins
  - Centralized pad control on a per-pin basis

  - System reset monitoring and generation
  - External interrupt inputs, filtering and control
- Error correction status module (ECSM)
  Configurable error-correcting codes (ECC) reporting for internal SRAM and flash memories
- On-chip flash
  - 3 MB burst flash memory
  - 386 KB × 64-bit configuration
  - Censorship protection scheme to prevent flash content visibility
  - Hardware read-while-write feature that can erase/program blocks while other blocks are read (used for EEPROM emulation and data calibration)
  - 28 blocks with sizes ranging from 16–128 KB to support features such as boot block, operating system block, and EEPROM emulation. Blocks are structured as follows:
    - 2 x 16 KB
    - 2 x 48 KB
    - 2 x 64 KB
    - 22 x 128 KB
  - Read while write with multiple partitions
  - Page programming mode to support rapid end of line programming
  - Hardware programming state machine
- Configurable cache memory, 0–32 KB
  - 4- and 8-way set-associative unified (instruction and data) cache
  - Decouples processor performance from system memory performance
- On-chip internal static RAM (SRAM)
  - 128 KB general-purpose SRAM of which 32 KB are on standby power
  - ECC performs single-bit correction, double-bit error detection
- Boot assist module (BAM): Enables and manages the transition of MCU from reset to user code execution in the following configurations:
  - Application can boot from internal or external flash memory
  - Download and execution of code via FlexCAN or eSCI
  - Application can boot with classic Power Architecture code or VLE code
- Enhanced modular I/O system (eMIOS)
  - 24 orthogonal channels with double action, PWM, and modulus counter functionality
  - Supports all DASM and PWM modes of MIOS14 (MPC5xx)
  - Four selectable time bases plus a shared time or angle counter bus
  - DMA and interrupt request support
  - Motor control capability
- Enhanced time processor units (eTPUs)
  - Two 32-channel engines

  - 24-bit timer resolution
  - 20 KB shared code memory, 4 KB shared data memory
  - Event-triggered timer subsystem
  - High-level assembler and compiler
  - Variable number of parameters to allocate per channel
  - Double match and capture channels
  - Angle clock hardware support
  - Shared time or angle counter bus for all eTPU and eMIOS modules
  - DMA and interrupt request support
  - Nexus class 3 debug support (with some class 4 support)
- Enhanced queued analog/digital converter (eQADC)
  - Two independent ADCs with 12-bit A/D resolution
  - Common mode conversion range of 0–5 V
  - 40 single-ended input channels, expandable to 65 channels with external multiplexers on the 416 BGA package
  - Eight channels can be used as four pairs of differential analog input channels
  - 10-bit accuracy at 400 ksamples/sec., 8-bit accuracy at 800 ksamples/sec.
  - Supports six FIFO queues with fixed priority
  - Queue modes with priority-based preemption; initiated by software command, internal (eTPU and eMIOS), or external triggers
  - DMA and interrupt request support
  - Supports all functional modes from QADC (MPC5xx family)
- Four deserial serial peripheral interface modules (DSPI)
  - Serial peripheral interface (SPI)
    - Full duplex communication ports with interrupt and eDMA request support
    - Supports all functional modes from QSPI submodule of QSMCM (MPC5xx family)
    - Support for queues in RAM
    - Six chip selects, expandable to 64 with external demultiplexers
    - Programmable frame size, baud rate, clock delay, and clock phase on a per-frame basis
    - Modified SPI mode for interfacing to peripherals with longer setup time requirements
  - Deserial serial interface (DSI)
    - Pin reduction by hardware serialization and deserialization of eTPU and eMIOS channels
    - Chaining of DSI submodules
    - Triggered transfer control and change in data transfer control (for reduced EMI)
- Two enhanced serial communication interface (eSCI) modules
  - UART mode provides NRZ format and half or full duplex interface
  - eSCI bit rate up to 1 Mb/sec.
  - Advanced error detection, and optional parity generation and detection

  - Word length programmable as 8 or 9 bits
  - Separately enabled transmitter and receiver
  - LIN support
  - DMA support
  - Interrupt request support
- Four FlexCANs
  - 64 message buffers each
  - Full implementation of the CAN protocol specification, Version 2.0B
  - Based on and including all existing features of the Freescale TouCAN module
  - Programmable acceptance filters
  - Individual receive filtering per message buffer
  - Short latency time for high-priority transmit messages
  - Arbitration scheme according to message ID or message buffer number
  - Listen-only mode capabilities
  - Programmable clock source: system clock or oscillator clock
  - Reception queue possible by setting more than one receive message buffer with the same ID
  - Backwards compatibility with previous FlexCAN modules
- Nexus development interface (NDI)
  - Per IEEE®-ISTO 5001-2003
  - Real-time development support for Power Architecture core and the eTPU engines through Nexus class 3 (some class 4 support)
  - Data trace of eDMA accesses
  - Read and write access
  - Configured via the IEEE® 1149.1 (JTAG) port
  - High-bandwidth mode for fast message transmission
  - Reduced bandwidth mode for reduced pin usage
- IEEE® 1149.1 JTAG controller (JTAGC)
  - IEEE® 1149.1-2001 test access port (TAP) interface
  - JCOMP input that provides the ability to share the TAP; selectable modes of operation include JTAGC/debug or normal system operation
  - 5-bit instruction register that supports IEEE® 1149.1-2001 defined instructions
  - 5-bit instruction register that supports additional public instructions
  - Three test data registers: a bypass register, a boundary scan register, and a device identification register
  - TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

- Voltage regulator controller (VRC)
  Provides a low-cost solution to power the core logic; it reduces the number of power supplies required from the customer power supply chip
- POR block
  Provides initial reset condition up to the voltage at which pins ($\overline{\text{RESET}}$) can be read safely; it does not guarantee the safe operation of the chip at specified minimum operating voltages
- Fast Ethernet controller (FEC)

  Only the 416 BGA package has a fast Ethernet controller (FEC) module that supports the following features:
  - IEEE® 802.3 MAC (compliant with IEEE® 802.3 1998 edition)
  - Built-in FIFO and DMA controller
  - Fully software compatible to the FEC module of Freescale's industry standard PowerQUICC communications controller
  - Full compliance with the IEEE 802.3 standard for 10/100 base-T
  - Support for different Ethernet physical interfaces:
    - IEEE® 802.3 MII
    - 10Mbps 7-wire interface (industry standard)
  - MII management interface for control and status
  - Large on-chip transmit and receive FIFOs to support a variety of bus latencies
  - Retransmission from the transmit FIFO after a collision
  - Automatic internal flushing of the receive FIFO for runts and collisions
  - External BD tables of user-definable size allow nearly unlimited flexibility in management of transmit and receive buffer memory
  - Address recognition for broadcast, single-station address, promiscuous mode, and multicast hashing
  - Ethernet channel uses DMA burst transactions to transfer data to and from external/system memory

1.4 MPC5500 Family Comparison

The following table compares the product features of the MPC5554 versus the MPC5566:

Table 1-1. MPC5554 and MPC5566 Comparison

Module		MPC5554	MPC5566
PowerPC core		e200z6	e200z6
Variable Length Encoding (VLE)		—	Y
Unified cache (KB)		32 [1]	32 [2]
Memory management unit (MMU)		32 entries	32 entries
Crossbar		3 x 5	4 x 5
Core Nexus		Class 3 + (NZ6C3)	Class 3 + (NZ6C3)
SRAM (KB)		64	128
Flash memory	Main array (MB)	2	3 [3]
	Shadow block (KB)	1	1
External bus interface (EBI)	Data	32 bit	32 bit [4]
	Address	24 bit	24 bit [5]
Calibration bus interface (CBI)		—	Y
Enhanced direct memory access (eDMA)		64 channels	64 channels
eDMA Nexus		Class 3	Class 3
Enhanced serial computer interface (eSCI)		2	2
	eSCI A	Y	Y
	eSCI B	Y	Y
	eSCI C	—	—
	eSCI D	—	—
Controller area network (FlexCAN)		3	4 [6]
	CAN A	64 buffers	64 buffers
	CAN B	64 buffers	64 buffers
	CAN C	64 buffers	64 buffers
	CAN D	—	64 buffers
	CAN E	—	—
Deserial to Serial Peripheral Interface (DSPI)		4	4
	DSPI A	Y	Y
	DSPI B	Y	Y
	DSPI C	Y	Y
	DSPI D	Y	Y
Enhanced Management I/O System (eMIOS)		24 channels	24 channels

Table 1-1. MPC5554 and MPC5566 Comparison (continued)

Module	MPC5554	MPC5566
Enhanced Time Processing Unit (eTPU)	64 channels	64 channels
eTPU A	Y	Y
eTPU B	Y	Y
Code memory (KB)	16	20
Parameter RAM (KB)	3	4
Nexus	Class 3	Class 3
Interrupt controller (INT)	308	329 [7]
Enhanced queued analog-to-digital converter (eQADC)	40 channel	40 channel
ADC 0	Y	Y
ADC 1	Y	Y
Fast Ethernet controller (FEC)	—	Y [8]
FlexRay	—	—
FlexRay Nexus	—	—
Frequency modulated phase lock loop (FMPLL)	Y	Y
Maximum system frequency[9]	132 MHz	147 MHz
Crystal range	8–20 MHz	8–20 MHz
Voltage regulator controller (VRC)	Y	Y

1 8-way associative
2 4-way and 8-way associative
3 32-byte flash page size for programming
4 Not externally available in all package configurations
5 Either ADDR[8:31] or ADDR[6:29] can be selected to have a 24-bit bus.
6 Updated FlexCAN module with optional individual receive filters
7 Although this device has a maximum of 329 interrupts, the logic requires that the total number of interrupts be divisible by four. Therefore, the total number of interrupts specified for this device is 332.
8 The FEC signals are muxed with data bus pins DATA[16:31].
9 Initial automotive temperature range qualification.

1.5 Detailed Features

The following sections provide detailed information about each of the on-chip modules.

1.5.1 e200z6 Core Overview

The device uses the e200z6 core explained in detail in the *e200z6 PowerPC™ Core Reference Manual*. The e200z6 CPU uses a seven-stage pipeline for instruction execution:

- Instruction fetch 1
- Instruction fetch 2
- Instruction decode and register file read

- Execute 1
- Execute 2 and memory access 1
- Execute 3 and memory access 2
- Register writeback

The operation of the pipeline stages overlap so that most instructions execute in a single-clock.

The integer execution unit consists of a 32-bit arithmetic unit (AU), a logic unit (LU), a 32-bit barrel shifter, a mask-insertion unit (MIU), a condition register manipulation unit (CRU), a count-leading-zeros unit (CLZ), a 32 x 32 hardware multiplier array, result feed-forward hardware, and support hardware for division.

Most arithmetic and logical operations are executed in a single cycle with the exception of multiply and divide instructions, which are implemented with a pipelined hardware array. The CLZ unit operates in a single clock cycle.

The instruction unit contains an incremental program counter (PC) and a dedicated branch address adder to minimize delays during change of flow operations. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding six sequential instructions and two branch target instructions.

Branch target addresses are calculated in parallel with branch instruction decode, resulting in execution time of three clocks. Conditional branches which are not taken execute in a single clock. Branches with successful look-ahead and target prefetching have an effective execution time of one clock.

Memory load and store operations are provided for byte, halfword, word (32-bits), and doubleword (64-bits) data, with automatic zero or sign extension of byte and halfword load data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized.

The condition register unit supports the condition register (CR) and condition register operations defined by the Power Architecture technology. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching.

Vectored and auto-vectored interrupts are supported by the CPU. Vectored interrupt supports unique interrupt handlers invoked with no software overhead for multiple interrupt sources.

The signal processing extension (SPE) APU supports vector instructions (SIMD) operating on 16- and 32-bit fixed-point data types, as well as 32-bit IEEE®-754 single-precision floating-point formats, and supports single-precision floating-point operations in a pipelined fashion. The 64-bit general-purpose register file is used for source and destination operands, and there is a unified storage model for single-precision floating-point data types of 32-bits and the normal integer type. Low latency fixed-point and floating-point add, subtract, multiply, divide, compare, and conversion operations are provided, and most operations can be pipelined.

The CPU includes support for Variable Length Encoding (VLE) instruction enhancements that have modified instruction set that uses a combination of 16- and 32-bit instructions from the classic Power Architecture instruction. This reduces the code size without noticeably affecting performance. The classic Power Architecture instruction set and VLE instruction set are available concurrently. Regions of the memory map are designated as PPC or VLE using an additional configuration bit in each table look-aside buffer (TLB) entry in the MMU.

1.5.2 System Bus Crossbar Switch (XBAR)

The system bus' multi-port crossbar (XBAR) switch supports simultaneous connections between four master ports and five slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width on all master and slave ports.

The crossbar allows concurrent transactions from any master port to any slave port. It is possible to use all master ports and slave ports at the same time as a result of independent master requests. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the highest priority master and grants it ownership of the slave port. All other masters requesting that slave port must wait until the higher priority master completes its transactions. By default, masters requests' have equal priority and are granted access to a slave port in round-robin fashion based on the last master ID granted access.

1.5.3 Enhanced Direct Memory Access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 64 programmable channels, with minimal intervention from the CPU. The hardware microarchitecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is used to minimize the overall module size.

1.5.4 Interrupt Controller (INTC)

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled real-time systems. The INTC allows interrupt request servicing from 329 [1] total interrupt vectors.

For high-priority interrupt requests, the time from when the peripheral interrupt request asserts to when the processor executes the interrupt service routine (ISR) is minimized. A unique vector for each interrupt request source is used to quickly determine which ISR to execute. The INTC module provides a number of priorities to ensure that lower priority ISRs do not delay the execution of higher priority ISRs. Software is used to configure the interrupt priorities for each interrupt source.

When multiple tasks share a resource, coherent accesses to that resource must be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the

1. Although this device has a maximum of 329 interrupts, the logic requires that the total number of interrupts be divisible by four. Therefore, the total number of interrupts specified for this device is 332.

priority level can be raised temporarily so that no task can preempt another task that shares the same resource.

Multiple processors can assert interrupt requests to each other through software settable interrupt requests (by using application software to assert requests). These maskable interrupt requests can divide the software into a high-priority portion and a low-priority portion for servicing the interrupt requests. The high-priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software settable interrupt request to finish the servicing in a lower priority ISR.

1.5.5 Frequency Modulated Phase-Locking Loop (FMPLL)

The frequency modulated phase-locking loop (FMPLL) generates high-speed system clocks from an 8–20 MHz crystal oscillator or an external clock generator. Furthermore, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio, modulation depth, and modulation rate are all software configurable.

1.5.6 External Bus Interface (EBI)

The external bus interface (EBI) controls data transfer across the crossbar switch to/from memories or peripherals in the external address space. The EBI is available on the 416 BGA package only. The EBI also enables an external master to access internal address space. The EBI includes a memory controller that generates interface signals to support a variety of external memories. The memory controller supports single data rate (SDR) burst mode flash, external SRAM, and asynchronous memories. In addition, the EBI supports up to four regions (via chip selects), along with programmed region-specific attributes.

1.5.7 System Integration Unit (SIU)

The device's system integration unit (SIU) controls MCU reset configuration, pad configuration, external interrupt, general-purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration module contains the external pin boot configuration logic. The pad configuration module controls the static electrical characteristics of I/O pins. The GPIO module provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the $\overline{\text{RSTOUT}}$ pin. The SIU is accessed by the e200z6 core through the crossbar switch.

1.5.8 Error Correction Status Module (ECSM)

The error correction status module (ECSM) provides status information regarding platform memory errors reported by error-correcting codes.

1.5.9 Flash Memory

The MPC5566 provides 3 MB of programmable, non-volatile, flash memory storage. Non-volatile memory (NVM) can be used for instruction and/or data storage.

The flash memory has a flash bus interface unit (FBIU) that connects the system bus to a dedicated flash memory array controller. The FBIU supports a 64-bit data bus width at the system bus port, and a 256-bit read data interface to flash memory. The FBIU contains two 256-bit prefetch buffers, and a prefetch controller that prefetches sequential lines of data from the flash array into the buffer. Prefetch buffer hits allow no-wait responses. Normal flash array accesses are registered in the FBIU and are forwarded to the system bus on the following cycle, incurring three wait-states. Prefetch operations can be automatically controlled, as well as restricted to servicing a single bus master. Prefetches can also require a trigger for instruction or data accesses.

1.5.10 Cache

The e200z6 core uses the following unified (instruction and data) cache with a 32-byte line size:32-KB, four- or eight-way set-associative

The cache improves system performance by providing low-latency data to the e200z6 instruction and data pipelines, which decouples processor performance from system memory performance. The cache is virtually indexed and physically tagged. The e200z6 does not provide hardware support for cache coherency in a multi-master environment. Software must be designed to maintain cache coherency with other possible bus masters.

Both instruction and data accesses are performed using a single bus connected to the cache. The processor uses virtual addresses to index the cache array. The memory management unit (MMU) provides the virtual-to-physical address conversion to perform the cache tag compare. The MMU can pass the virtual addresses to the cache as the physical address without the conversion. If the physical address matches a valid cache tag entry, the access hits in the cache. For a read operation, the cache supplies the data to the processor, and for a write operation, the data from the processor is written to cache. If the access does not match a valid cache tag entry (misses in the cache), or a write access is required to memory, the cache performs a bus cycle on the system bus.

1.5.11 Static RAM (SRAM)

The MPC5500 family internal SRAM module provides a general-purpose memory block that supports mapped read/write accesses from any master. The SRAM size is 128 KB. Included within the SRAM block is a 32-KB block powered by a separate supply for standby operation and ECC error correction and detection.

1.5.12 Boot Assist Module (BAM)

The boot assist module (BAM) is read-only memory programmed by Freescale and is identical for all MCUs with an e200z6 core. The BAM program executes every time the MCU is powered on, or when reset in normal mode. The BAM supports these boot modes:

- Booting from internal flash memory
- Single master booting from external memory
- Serial boot loading (program is downloaded to SRAM over an eSCI or FlexCAN peripheral and then executed)

The BAM reads the reset configuration halfword (RCHW) from flash memory (either internal or external) to configure the device hardware. The MMU is then configured for all resources and maps all physical addresses to logical addresses with the minimum address translation, to allow application boot code to execute as either Classic Power Architecture Book E code (default) or as Freescale VLE code.

1.5.13 Enhanced Management Input/Output System (eMIOS)

The enhanced modular I/O system (eMIOS) module generates or measures time events. A unified channel (UC) module provides a consistent interface to a superset of all the MIOS channel functionality. This allows more flexibility to program each unified channel for different functions in different applications. To identify up to two timed events, each UC uses two comparators, a time base selector, and registers. This structure can produce match events to measure or generate a waveform. Alternatively, input events can capture the time base, allowing measurement of an input signal.

1.5.14 Enhanced Time Processing Unit (eTPU)

The enhanced time processing unit (eTPU) is an enhanced coprocessor designed for timing control. Operating in parallel with the host CPU, the eTPU processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the CPU setup and service times are minimized or eliminated. In the MCU, the TPU engine is combined with shared instruction and data RAM to form a powerful time processing subsystem.

The MPC5566 has two eTPU engines. You can use the high-level assembler and compiler, along with the eTPU documentation set, to develop customized eTPU functions. The eTPU supports several features of older TPU versions, making it easy to port earlier application versions.

1.5.15 Enhanced Queued A/D Converter (eQADC)

The enhanced queued analog to digital converter (eQADC) module provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog to digital converters (ADCs), and a single master-to-single slave serial interface to an off-chip external device. The two on-chip ADCs are designed to access all the analog channels.

The eQADC transfers commands from multiple command FIFOs (CFIFOs) to the on-chip ADCs or to the external device. The module can also receive data from the on-chip ADCs or from an off-chip external device into multiple result FIFOs (RFIFOs) in parallel, independently of the CFIFOs. The eQADC supports software and external hardware triggers from other modules to initiate transfers of commands from the CFIFOs to the on-chip ADCs or to the external device. It also monitors the fullness of CFIFOs and RFIFOs, and accordingly generates eDMA or interrupt requests to control data movement between the FIFOs and the system memory, which is external to the eQADC.

1.5.16 Deserial/Serial Peripheral Interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the MCU and external devices. The DSPI supports pin-count reduction through

serialization and deserialization of eTPU channels, eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol.

The MPC5566 has four DSPI modules (A, B, C, and D). The DSPIs have three configurations:

- Serial peripheral interface (SPI) configuration where the DSPIs operate as serial ports only with support for queues.
- Deserial serial interface (DSI) configuration where the DSPIs serialize eTPU and eMIOS output channels, and deserialize the input data by passing it to the eTPU and eMIOS input channels.
- Combined serial interface (CSI) configuration where the DSPIs operate in both SPI and DSI configurations, interleaving DSI frames with SPI frames, and giving priority to SPI frames.

For queued operations, the SPI queues reside in system memory external to the DSPI. Data transfers between the memory and the DSPI FIFOs use the eDMA controller or the host software.

1.5.17 Enhanced Serial Communications Interface (eSCI)

The enhanced serial communications interface (eSCI) allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to interface to local interconnect network (LIN) slave devices. The MPC5566 has two eSCI modules (A and B).

1.5.18 Flexible Controller Area Network (FlexCAN)

The MCU contains four controller area network (FlexCAN) modules. Each FlexCAN module is a communication controller implementing the CAN protocol according to CAN Specification version 2.0B. The CAN protocol is designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth. Each FlexCAN module contains 64 message buffers.

1.5.19 Nexus Development Interface (NDI)

The Nexus development interface (NDI) module provides real-time development support capabilities for the MPC5500 family's MCU built on the Power Architecture in compliance with the IEEE®-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI module integrates several Nexus modules to provide the development support interface for the MPC5500 family. The NDI module interfaces to the host processor, single or dual eTPU processors, and internal buses to provide development support as per the IEEE®-ISTO 5001-2003 standard. The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCU internal memory map, Nexus trace of eDMA transfers, and access to the Power Architecture and eTPU internal registers during a halt, using the auxiliary port. The Nexus interface also supports a JTAG only mode using only the JTAG pins.

1.5.20 JTAG Controller (JTAGC)

The JTAG controller (JTAGC) module provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE® 1149.1-2001 standard. All data input to and output from the JTAGC

module is communicated in serial format. The JTAGC module is compliant with the IEEE® 1149.1-2001 standard.

1.5.21 Fast Ethernet Controller (FEC)

The MPC5566 fast Ethernet controller includes these distinctive features:

- IEEE 802.3 MAC (compliant with IEEE 802.3 1998 edition)
- Fully software compatible to the FEC module of Freescale's industry standard PowerQUICC communications controller
- MII management interface for control and status
- Built-in FIFO and DMA controller
- Support for different Ethernet physical interfaces:
  - IEEE 802.3 MII
  - 10 Mbps 7-wire interface (industry standard)
- Support for full-duplex operation (200 Mbps throughput) with a system clock of 100 MHz.
- Support for half-duplex operation (100 Mbps throughput) with a system clock of 50 MHz.
- IEEE 802.3 full duplex flow control
- Programmable max frame length supports IEEE 802.1 VLAN tags and priority
- Retransmission from transmit FIFO following a collision (no system bus utilization)
- Automatic internal flushing of the receive FIFO for runts (collision fragments) and address recognition rejects (no system bus utilization)
- Address recognition
  - Frames with broadcast address may be always accepted or always rejected
  - Exact match for single 48-bit individual (unicast) address
  - Hash (64-bit hash) check of individual (unicast) addresses
  - Hash (64-bit hash) check of group (multicast) addresses
  - Promiscuous mode
- RMON and IEEE statistics
- Interrupts for network activity and error conditions

1.6 MPC5500 Family Memory Map

This section describes the MPC5500 family memory map. All addresses in the device, including those that are reserved, are identified in the tables. The addresses represent the physical addresses assigned to each module. Logical addresses are translated by the MMU into physical addresses.

Reserved register bits are allocated for future products and have a default value of zero. When writing to a register, the reserved bits default values must be written as well. Most device features are activated by writing a non-zero value to them.

Reserved memory is allocated for future products, therefore do not write to memory segments that are designated as reserved.

Under software control of the MMU, the logical addresses allocated to modules can be changed on a minimum of a 4 KB boundary. Peripheral modules may be redundantly mapped. You must use the MMU to prevent corruption.

Table 1-2 shows a detailed list of the device memory map.

Table 1-2. MPC5566 Detailed Memory Map

Address Range[1]	Allocated Size[1] (bytes)	Used Size (bytes)	Use
0x0000_0000–0x002F_FFFF	3 MB	3 MB	Flash memory array
0x0030_0000–0x00FF_FBFF	13 MB–1 KB (total flash shadow row)	N/A	Reserved
0x00FF_FC00–0x00FF_FFFF	1 KB	1 KB	Flash shadow row
0x0100_0000–0x1FFF_FFFF	496 MB	2 MB	Emulation mapping of flash array
0x2000_0000–0x3FFF_FFFF	512 MB	N/A	External memory [2]
0x4000_0000–0x4000_7FFF	32 KB	32 KB	Internal SRAM array, standby powered
0x4000_8000–0x4001_FFFF	96 KB	96 KB	Internal SRAM array
0x4002_0000–0xBFFF_FFFF	2048 MB–128 KB (total SRAM)	N/A	Reserved
Bridge A Peripherals			
0xC000_0000–0xC3EF_FFFF	63 MB	N/A	Reserved
0xC3F0_0000–0xC3F0_3FFF	16 KB	—	Bridge A registers
0xC3F0_4000–0xC3F7_FFFF	496 KB	N/A	Reserved
0xC3F8_0000–0xC3F8_3FFF	16 KB	—	FMPLL registers
0xC3F8_4000–0xC3F8_7FFF	16 KB	48	External bus interface (EBI) configuration registers
0xC3F8_8000–0xC3F8_BFFF	16 KB	28	Flash configuration registers
0xC3F8_C000–0xC3F8_FFFF	16 KB	N/A	Reserved
0xC3F9_0000–0xC3F9_3FFF	16 KB	2.5 KB	System integration unit (SIU)
0xC3F9_4000–0xC3F9_FFFF	48 KB	N/A	Reserved

Table 1-2. MPC5566 Detailed Memory Map (continued)

Address Range[1]	Allocated Size[1] (bytes)	Used Size (bytes)	Use
0xC3FA_0000–0xC3FA_3FFF	16 KB	1056	Modular timer system (eMIOS)
0xC3FA_4000–0xC3FB_FFFF	112 KB	N/A	Reserved
0xC3FC_0000–0xC3FC_3FFF	16 KB	3 KB	Enhanced time processing unit (eTPU) registers
0xC3FC_4000–0xC3FC_7FFF	16 KB	N/A	Reserved
0xC3FC_8000–0xC3FC_8FFF	16 KB	4 KB	eTPU shared data memory (parameter RAM)
0xC3FC_C000–0xC3FC_FFFF	16 KB	3 KB	eTPU shared data memory (parameter RAM) mirror
0xC3FD_0000–0xC3FD_4FFF	20 KB	20 KB	eTPU shared code RAM
0xC3FD_5000–0xC3FF_FFFF	176 KB	N/A	Reserved
0xC400_0000–0xDFFF_FFFF	448 MB	N/A	Reserved
Bridge B Peripherals			
0xE000_0000–0xFBFF_FFFF	448 MB	N/A	Reserved
0xFC00_0000–0xFFEF_FFFF	63 MB	N/A	Reserved
0xFFF0_0000–0xFFF0_3FFF	16 KB	N/A	Bridge B registers
0xFFF0_4000–0xFFF0_7FFF	16 KB	N/A	System bus crossbar switch (XBAR)
0xFFF0__8000–0xFFF0_FFFF	32 KB	N/A	Reserved
0xFFF1_0000–0xFFF3_FFFF	192 KB	N/A	Reserved
0xFFF4_0000–0xFFF4_3FFF	16 KB	N/A	ECSM
0xFFF4_4000–0xFFF4_7FFF	16 KB	N/A	DMA controllers 2 (eDMA)
0xFFF4_8000–0xFFF4_BFFF	16 KB	N/A	Interrupt controller (INTC)
0xFFF4_C000–0xFFF4_C3FF	1 KB	N/A	Fast Ethernet controller (FEC) [3]
0xFFF4_C400–0xFFF4_FFFF	15 KB	N/A	Reserved
0xFFF5_0000–0xFFF7_FFFF	192 KB	N/A	Reserved
0xFFF8_0000–0xFFF8_3FFF	16 KB	164	Enhanced queued analog-to-digital converter (eQADC)
0xFFF8_4000–0xFFF8_FFFF	48 KB	N/A	Reserved
0xFFF9_0000–0xFFF9_3FFF	16 KB	200	Deserial serial peripheral interface (DSPI A)
0xFFF9_4000–0xFFF9_7FFF	16 KB	200	Deserial serial peripheral interface (DSPI B)
0xFFF9_8000–0xFFF9_BFFF	16 KB	200	Deserial serial peripheral interface (DSPI C)
0xFFF9_C000–0xFFF9_FFFF	16 KB	200	Deserial serial peripheral interface (DSPI D)
0xFFFA_0000–0xFFFA_FFFF	64 KB	N/A	Reserved
0xFFFB_0000–0xFFFB_3FFF	16 KB	44	Serial communications interface (eSCI A)
0xFFFB_4000–0xFFFB_7FFF	16 KB	44	Serial communications interface (eSCI B)
0xFFFB_8000–0xFFFB_FFFF	32 KB	N/A	Reserved

Table 1-2. MPC5566 Detailed Memory Map (continued)

Address Range[1]	Allocated Size[1] (bytes)	Used Size (bytes)	Use
0xFFFC_0000–0xFFFC_3FFF	16 KB	1152	Controller area network (FlexCAN A)
0xFFFC_4000–0xFFFC_7FFF	16 KB	1152	Controller area network (FlexCAN B)
0xFFFC_8000–0xFFFC_BFFF	16 KB	1152	Controller area network (FlexCAN C)
0xFFFC_C000–0xFFFC_FFFF	16 KB	1152	Controller area network (FlexCAN D)
0xFFFD_0000–0xFFFF_BFFF	176 KB	N/A	Reserved
0xFFFF_C000–0xFFFF_FFFF[4]	16 KB	16 KB	Boot assist module (BAM) [4]

1 If the allocated size is more than the used size, the base address for the module is the lowest address of the listed address range, unless noted otherwise.

2 A common configuration is: EBI memory ranges from 0x2000_0000 to 0x2FFF_FFFF; and Calibration memory ranges from 0x3000_0000 to 0x3FFF_FFFF. Hardware does not force any restrictions on allocating memory to the EBI versus calibration bus.

3 The FEC pins are muxed with DATA[16:31].

4 The BAM address range is configured so that the 4 KB BAM occupies 0xFFFF_F000–0xFFFF_FFFF.

1.7 Multi-Master Operation Memory Map

When the MCU acts as a slave in a multi-master system, the external bus interface (EBI) translates the 24-bit external address to a 32-bit internal address. Table 1-3 lists the translation parameters.

Table 1-3. External to Internal Memory Map Translation Table for Slave Mode

External Address[8:11] [1]	Internal Address[0:11]	MB	Internal Slave	Internal Address Range
0b0xxx	N/A	8	N/A	N/A. Off-chip flash access
0b10xx	0b0000_0000_00xx	4	Internal flash array	0x0000_0000–0x003F_FFFF
0b1100	0b0100_0000_0000	1	Internal SRAM	0x4000_0000–0x4000_FFFF
0b1101	0b0110_0000_0000	1	Reserved [2]	0x6000_0000–0x600F_FFFF
0b1110	0b1100_0011_1111	1	Bridge A peripherals	0xC3F0_0000–0xC3FF_FFFF
0b1111	0b1111_1111_1111	1	Bridge B peripherals	0xFFF0_0000–0xFFFF_FFFF

1 Only the lower 24 address signals (ADDR[8:31]) are available off-chip for external master accesses.

2 Reserved for a future module that requires its own crossbar slave port.

Table 1-4 shows the memory map for the MCU acting as a slave in a multi-master system from the point of view of the external master.

Table 1-4. MPC5566 Family Slave Memory Map as Seen from an External Master

External Address Range [1]	Size	Use
0x0000_0000[2]–0x007F_FFFF	8 MB	N/A. Used for off-chip memory accesses
0x0080_0000–0x00AF_FFFF	3 MB	Slave flash [3]
0xB0_0000 – 0xBF_FFFF	1 MB	Reserved
0x00C0_0000–0x00C1_FFFF	128 KB	Slave internal SRAM
0x00C2_0000–0x00CF_FFFF	1 MB–128 KB (less total SRAM)	Reserved
0x00D0_0000–0x00DF_FFFF	1 MB	Reserved
0x00E0_0000–0x00EF_FFFF	1 MB	Slave bridge A peripherals
0x00F0_0000–0x00FF_FFFF	1 MB	Slave bridge B peripherals

1 Only the lower 24 address signals (ADDR[8:31]) are available off-chip for external master accesses.

2 This address range is not part of the MPC5500 family slave memory map, rather it is shown to illustrate the addressing scheme for off-chip accesses in multi-master mode.

3 The shadow row of the slave flash is not accessible by an external master.

Chapter 2
Signal Description

This chapter describes the external device signals, including a table of signal properties, detailed descriptions of the available signals, and the I/O pin power/ground segmentation.

2.1 Block Diagram

To provide an extensive feature set and compatibility between the MPC5500 devices, most of the balls have multiplexed signal functions. Primary signal functions that are not available on the device, but are used as pin labels in the Ball Grid Array (BGA) map are listed in Table 2-1.

Figure 2-1 shows only the signals that are available on the device. Read the last two columns in Table 2-1 for a list of BGA package connections provided by the VertiCal assembly.

NOTE

The Vertical assembly has ball connections for all the *available* signals on the device.

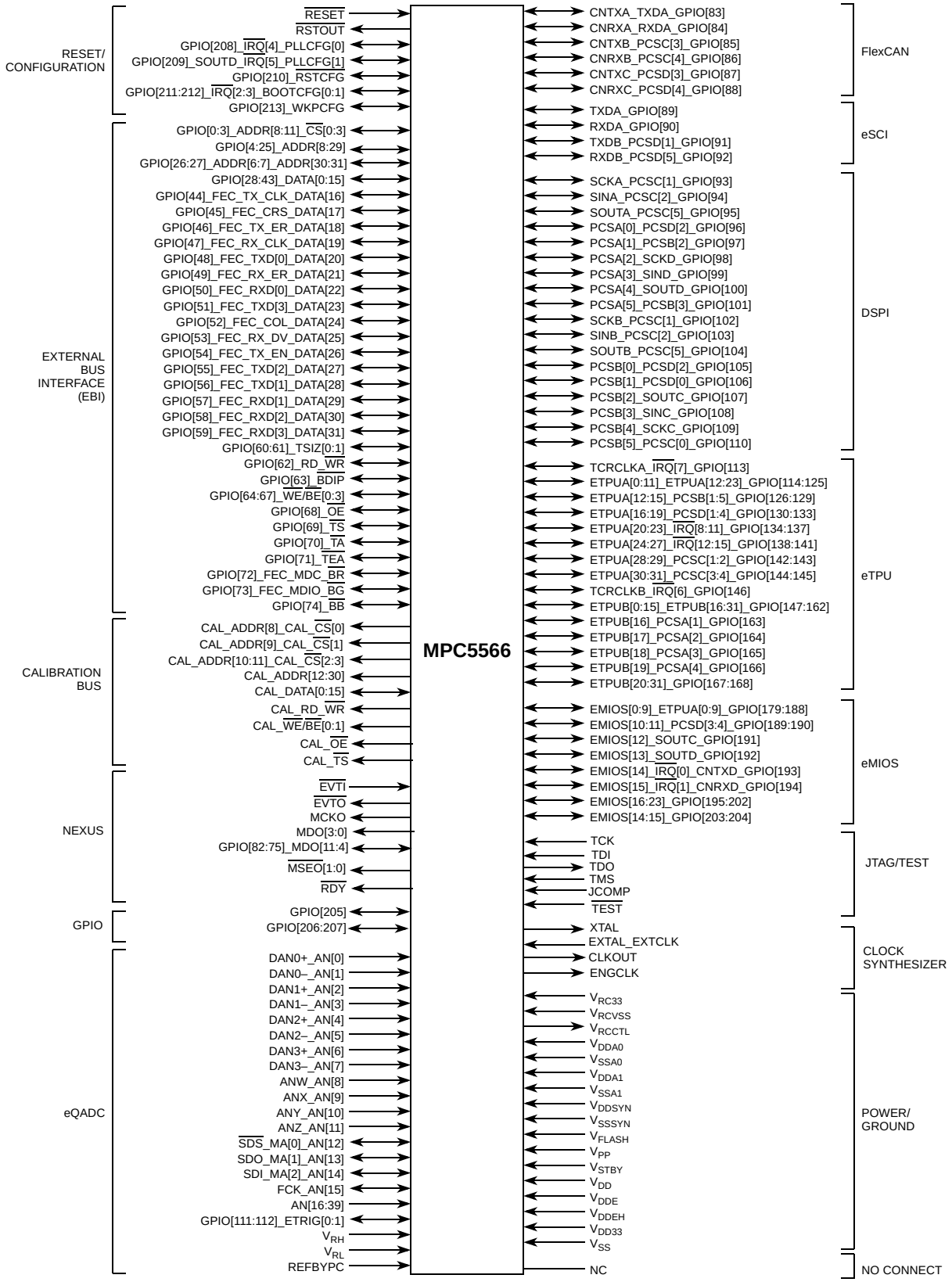


Figure 2-1. MPC5566 Signals

2.2 External Signal Descriptions

This section summarizes the external signal functions, the electrical characteristics, and pad configuration settings for this device. The signal properties and electrical characteristics are set in the System Integration Unit (SIU) Pad Configuration (PCR) registers.

2.2.1 Multiplexed Signals

Signal functions are multiplexed to each ball on the BGA in a function hierarchy: Primary, Main Primary, Alternate, Second Alternate, and General Purpose Input/Output (I/O). For example, in the signal PCSA[3]_SIND_GPIO[99], the primary signal function is PCSA[3], the first alternate signal function is SIND, and the GPIO function is a generic General Purpose I/O signal. Multiplexing signal functions allows for more flexibility when configuring the device, as well as providing compatibility with other devices in the MPC5500 product family.

The primary signal function name is used in the Ball Grid Array (BGA) map to identify the location of the ball, however, the primary signal function is not always valid for all devices. As shown in Figure 2-2, when the primary signal function is not available on the device, a dash appears in the following Signal table columns: Signal Functions, P/A/G, and I/O Type.

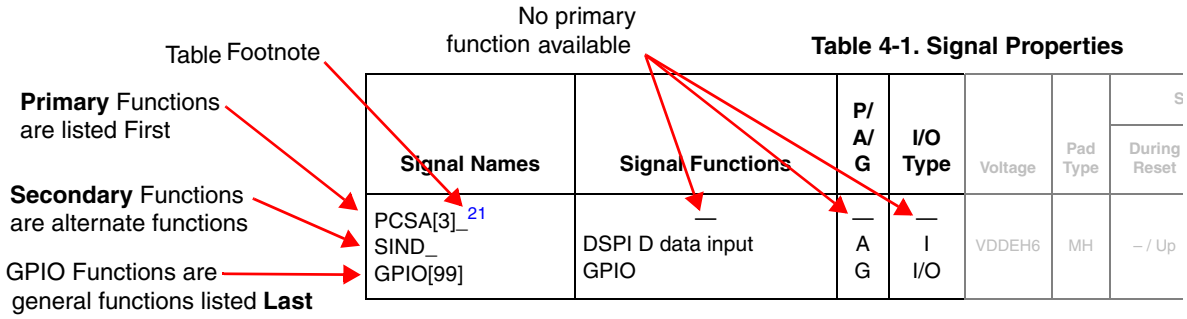
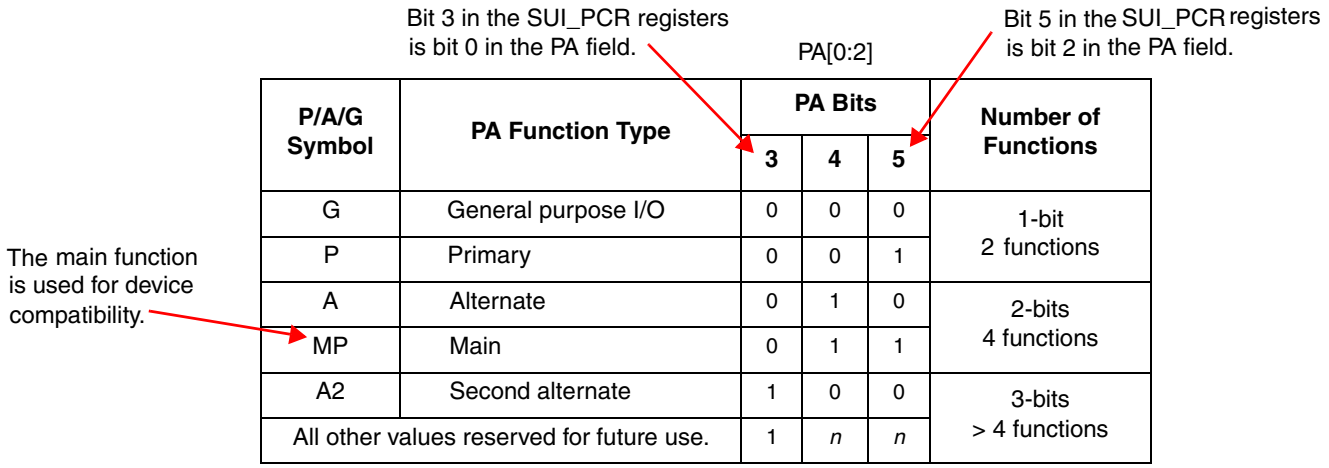


Figure 2-2. Primary Function Not Available on Device

The entries in the P/A/G column designate the position in the signal function hierarchy for multiplexed functions. These symbols correspond to binary values for the Pin Assignment (PA) field in the SIU_PCR registers that determine the active signal function. The PA field is from 1- to 3-bits wide, depending on the PCR register. Figure 2-3 explains the symbol definitions used in the P/A/G column for Table 2-1.



P/A/G Symbol	PA Function Type	PA Bits 3	4	5	Number of Functions
G	General purpose I/O	0	0	0	1-bit 2 functions
P	Primary	0	0	1	
A	Alternate	0	1	0	2-bits 4 functions
MP	Main	0	1	1	
A2	Second alternate	1	0	0	3-bits > 4 functions
All other values reserved for future use.		1	*n*	*n*	

Figure 2-3. Understanding the P/A/G Column Entries

2.2.2 Device Signals Summary

Table 2-1 gives a summary of the device's external signals and properties. Read Section 2.3, "Detailed Signal Description," for more information and descriptions of each signal.

The following table lists the signal functions and their properties for this device:

Table 2-1. MPC5566 Signal Properties

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status During Reset [5]	Status After Reset [6]	416 Package	496 Vertical Assembly [4]
Reset / Configuration									
$\overline{\text{RESET}}$	External reset input	P	I	V_{DDEH6}	SH	$\overline{\text{RESET}}$ / Up	$\overline{\text{RESET}}$ / Up	W26	AA27
$\overline{\text{RSTOUT}}$	External reset output	P	O	V_{DDEH6}	SH	$\overline{\text{RSTOUT}}$ / Low	$\overline{\text{RSTOUT}}$ / High	V25	W26
PLLCFG[0]_ $\overline{\text{IRQ}}$[4]_ GPIO[208]	PLLMRFM mode selection External interrupt request GPIO	P A G	I I I/O	V_{DDEH6}	MH	PLLCFG / Up	– / Up	AB25	AB27
PLLCFG[1]_ $\overline{\text{IRQ}}$[5]_ SOUTD_ GPIO[209]	PLLMRFM reference selection External interrupt request DSPI D data output GPIO	P A A2 G	I I O I/O	V_{DDEH6}	MH	PLLCFG / Up	– / Up	AA24	AA26
PLLCFG[2] [7]	PLLMRFM configuration input 2 [7]	P	I	V_{DDEH6}	MH	PLLCFG / –	– / –	–	–
$\overline{\text{RSTCFG}}$_ GPIO[210]	Reset configuration input GPIO	P G	I I/O	V_{DDEH6}	SH	$\overline{\text{RSTCFG}}$ / Up	– / Up	V26	Y28
BOOTCFG[0]_ $\overline{\text{IRQ}}$[2]_ GPIO[211]	Boot configuration input External interrupt request GPIO	P A G	I I I/O	V_{DDEH6}	SH	BOOTCFG / Down	– / Down	AA25	AB26

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
BOOTCFG[1]_ $\overline{IRQ}$[3]_ GPIO[212]	Boot configuration input External interrupt request GPIO	P A G	I I I/O	V_{DDEH6}	SH	BOOTCFG / Down	– / Down	Y24	AB24
WKPCFG_ GPIO[213]	Weak pull configuration input GPIO	P G	I I/O	V_{DDEH6}	SH	WKPCFG / Up	– / Up	Y23	AA24
External Bus Interface (EBI) [8]									
$\overline{CS}$[0]_ ADDR[8]_ [9, 10] GPIO[0]	External chip selects External address bus GPIO	P A G	O I/O I/O	V_{DDE2}	F	– / Up	– / Up [11]	P4	T7
$\overline{CS}$[1:3]_ ADDR[9:11]_ [9, 10] GPIO[1:3]	External chip selects External address bus GPIO	P A G	O I/O I/O	V_{DDE2}	F	– / Up	– / Up [11]	P3, P2, P1	R5, P5, R7
ADDR[8:11]_ [9, 10] GPIO[4:7]	External address bus GPIO	P G	I/O I/O	V_{DDE2}	F	– / Up	– / Up [11]	V4, W3, W4, Y3	Y5, Y3, AA3, AB3
ADDR[12:26]_ [10] GPIO[8:22]	External address bus GPIO	P G	I/O I/O	V_{DDE2}	F	– / Up	– / Up [11]	AA4, AA3, AB4, AB3, U1, V2, V1, W2, W1, Y2, Y1, AA2, AA1, AB2, AC1	Y7, AC3, AC5, AB5, T3, T2, T1, V2, W1, W2, Y1, Y2, AA2, AB2, AC2
ADDR[27:29]_ [10] GPIO[23:25]	External address bus GPIO	P G	I/O I/O	V_{DDE2}	F	– / Up	– / Up [11]	AC2, AD1, AE1	AD2:3, AD1
ADDR[30:31]_ [10] ADDR[6:7]_ [12] GPIO[26:27]	External address bus External address bus GPIO	P A G	I/O I/O I/O	V_{DDE2}	F	– / Up	– / Up [11]	AD2, AC3	AF2, AE2
DATA[0:15]_ [10] GPIO[28:43]	External address bus GPIO	P G	I/O I/O	V_{DDE3}	F	– / Up	– / Up [11]	AE8, AF9, AE9, AF10, AE10, AF12, AE11, AF13, AC11, AD11, AC12, AD12, AC14, AD13, AC15, AD14	AG11, AF12, AG13, AH13, AG14, AH15, AG15, AH16, AB12, AF10, AD13, AF11, AB15, AD12, AD15, AF13
DATA[16]_ [10] FEC_TX_CLK_ GPIO[44]	External data bus Ethernet transmit clock GPIO	P A G	I/O I I/O	V_{DDE3}	F	– / Up	– / Up [11]	AF3	AF5
DATA[17]_ [10] FEC_CRS_ GPIO[45]	External data bus Ethernet carrier sense GPIO	P A G	I/O I I/O	V_{DDE3}	F	– / Up	– / Up [11]	AE4	AG5

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
DATA[18]_ [10] FEC_TX_ER_ GPIO[46]	External data bus Ethernet transmit error GPIO	P A G	I/O O I/O	V_{DDE3}	F	– / Up	– / Up [11]	AF4	AH5
DATA[19]_ [10] FEC_RX_CLK_ GPIO[47]	External data bus Ethernet receive clock GPIO	P A G	I/O I I/O	V_{DDE3}	F	– / Up	– / Up [11]	AE5	AG6
DATA[20]_ [10] FEC_TXD[0]_ GPIO[48]	External data bus Ethernet transmit data GPIO	P A G	I/O O I/O	V_{DDE3}	F	– / Up	– / Up [11]	AF6	AG7
DATA[21]_ [10] FEC_RX_ER_ GPIO[49]	External data bus Ethernet receive error GPIO	P A G	I/O I I/O	V_{DDE3}	F	– / Up	– / Up [11]	AE6	AG8
DATA[22]_ [10] FEC_RXD[0]_ GPIO[50]	External data bus Ethernet receive data GPIO	P A G	I/O I I/O	V_{DDE3}	F	– / Up	– / Up [11]	AF7	AG9
DATA[23]_ [10] FEC_TXD[3]_ GPIO[51]	External data bus Ethernet transmit data GPIO	P A G	I/O O I/O	V_{DDE3}	F	– / Up	– / Up [11]	AE7	AH9
DATA[24]_ [10] FEC_COL_ GPIO[52]	External data bus Ethernet collision data GPIO	P A G	I/O I I/O	V_{DDE3}	F	– / Up	– / Up [11]	AD5	AD7
DATA[25]_ [10] FEC_RX_DV_ GPIO[53]	External data bus Ethernet receive data valid GPIO	P A G	I/O I I/O	V_{DDE3}	F	– / Up	– / Up [11]	AD6	AF6
DATA[26]_ [10] FEC_TX_EN_ GPIO[54]	External data bus Ethernet transmit enable GPIO	P A G	I/O O I/O	V_{DDE3}	F	– / Up	– / Up [11]	AC6	AB9
DATA[27]_ [10] FEC_TXD[2]_ GPIO[55]	External data bus Ethernet transmit data GPIO	P A G	I/O O I/O	V_{DDE3}	F	– / Up	– / Up [11]	AD7	AF7
DATA[28]_ [10] FEC_TXD[1]_ GPIO[56]	External data bus Ethernet transmit data GPIO	P A G	I/O O I/O	V_{DDE3}	F	– / Up	– / Up [11]	AC7	AD8
DATA[29]_ [10] FEC_RXD[1]_ GPIO[57]	External data bus Ethernet receive data GPIO	P A G	I/O I I/O	V_{DDE3}	F	– / Up	– / Up [11]	AD8	AF8
DATA[30]_ [10] FEC_RXD[2]_ GPIO[58]	External data bus Ethernet receive data GPIO	P A G	I/O I I/O	V_{DDE3}	F	– / Up	– / Up [11]	AC9	AD10
DATA[31]_ [10] FEC_RXD[3]_ GPIO[59]	External data bus Ethernet receive data GPIO	P A G	I/O I I/O	V_{DDE3}	F	– / Up	– / Up [11]	AC10	AD11
TSIZ[0:1]_ GPIO[60:61]	External transfer size GPIO	P G	I/O I/O	V_{DDE2}	F	– / Up	– / Up [11]	T2, U2	R2, P2
RD_$\overline{WR}$_ GPIO[62]	External read/write GPIO	P G	I/O I/O	V_{DDE2}	F	– / Up	– / Up [11]	T3	U3

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
$\overline{\text{BDIP}}$_ GPIO[63]	External burst data in progress GPIO	P G	O I/O	V_{DDE2}	F	– / Up	– / Up [11]	N1	N1
$\overline{\text{WE}}$/$\overline{\text{BE}}$[0:1]_ [13] GPIO[64:65]	External write/byte enable GPIO	P G	O I/O	V_{DDE2}	F	– / Up	– / Up [11]	R4, R3	U5, T5
$\overline{\text{WE}}$/$\overline{\text{BE}}$[2:3]_ [13] GPIO[66:67]	External write/byte enable GPIO	P G	O I/O	V_{DDE2}	F	– / Up	– / Up [11]	R2, R1	N3, P1
$\overline{\text{OE}}$_ GPIO[68]	External output enable GPIO	P G	O I/O	V_{DDE3}	F	– / Up	– / Up [11]	AE12	AF16
$\overline{\text{TS}}$_ GPIO[69]	External transfer start GPIO	P G	I/O I/O	V_{DDE2}	F	– / Up	– / Up [11]	V3	W3
$\overline{\text{TA}}$_ GPIO[70]	External transfer acknowledge GPIO	P G	I/O I/O	V_{DDE2}	F	– / Up	– / Up [11]	U3	V3
$\overline{\text{TEA}}$_ GPIO[71]	External transfer error acknowledge GPIO	P G	I/O I/O	V_{DDE2}	F	– / Up	– / Up [11]	N2	N2
$\overline{\text{BR}}$_ FEC_MDC_ GPIO[72]	External bus request Ethernet management clock GPIO	P A G	I/O O I/O	V_{DDE3}	F	– / Up	– / Up [11]	AE13	AF17
$\overline{\text{BG}}$_ FEC_MDIO_ GPIO[73]	External bus grant Ethernet management data I/O GPIO	P A G	I/O I/O I/O	V_{DDE3}	F	– / Up	– / Up [11]	AE14	AG16
$\overline{\text{BB}}$_ GPIO[74]	External bus busy GPIO	P G	I/O I/O	V_{DDE3}	F	– / Up	– / Up [11]	AF14	AG17
Calibration Bus									
CAL_$\overline{\text{CS}}$[0]	Calibration chip select	P	O	V_{DDE12}	F	– / Up	– / Up	—	AB11
CAL_$\overline{\text{CS}}$[1:3]_ CAL_ADDR[9:11]	Calibration chip select Calibration address bus	P A	O O	V_{DDE12}	F	– / Up	– / Up	—	AA12, AA10, AB10
CAL_ADDR[12:30]	Calibration address bus	P	O	V_{DDE12}	F	– / Up	– / Up	—	AA14, R8, AA15, W7, P7, P8, U7, N7, M8, M7, V7, L8, T8, K8, L7, U8, V8, AB13, AB14
CAL_DATA[0:15]	Calibration data bus	P	I/O	V_{DDE12}	F	– / Up	– / Up	—	W21, Y22, V21, W22, U21, U22, T21, T22, AA17, AB16, AA18, AB17, AA19, AB19, AA20, AB20
CAL_RD_$\overline{\text{WR}}$	Calibration read/write	P	O	V_{DDE12}	F	– / Up	– / Up	—	W8
CAL_$\overline{\text{WE}}$/$\overline{\text{BE}}$[0:1]	Calibration write/byte enable	P	O	V_{DDE12}	F	– / Up	–/ Up	—	Y8, AA7
CAL_$\overline{\text{OE}}$	Calibration output enable	P	O	V_{DDE12}	F	– / Up	– / Up	—	AD16

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
CAL_$\overline{TS}$	Calibration transfer start	P	O	V_{DDE12}	F	– / Up	– / Up	—	AA11
NEXUS									
$\overline{EVTI}$	Nexus event in	P	I	V_{DDE7}	F	I / Up	$\overline{EVTI}$ / Up	F25	G26
$\overline{EVTO}$	Nexus event out	P	O	V_{DDE7}	F	O / Low	$\overline{EVTO}$ / High	F26	G27
MCKO	Nexus message clock out	P	O	V_{DDE7}	F	O / Low	MCKO / Enabled [14]	G24	H26
MDO[0] [15]	Nexus message data out	P	O	V_{DDE7}	F	O / High	MDO / Low	B24	C25
MDO[3:1]	Nexus message data out	P	O	V_{DDE7}	F	O / Low	MDO / Low	C23, D21, C22	C24, B21, C23
MDO[11:4]_ [16] GPIO[82:75]	Nexus message data out GPIO	P G	O I/O	V_{DDE7}	F	O / Low	– / Down	B23, D20, C21, B22, A23, C20, B21, A22	B24, C20, B20, B23, A24, A20, C22, A23
$\overline{MSEO}$[1:0]	Nexus message start/end out	P	O	V_{DDE7}	F	O / High	$\overline{MSEO}$ / High	F23, G23	G24, H24
$\overline{RDY}$	Nexus ready output	P	O	V_{DDE7}	F	O / High	$\overline{RDY}$ / High	H23	J24
JTAG / TEST									
TCK	JTAG test clock input	P	I	V_{DDE7}	F	TCK / Down	TCK / Down	D25	E27
TDI	JTAG test data input	P	I	V_{DDE7}	F	TDI / Up	TDI / Up	D26	E28
TDO	JTAG test data output	P	O	V_{DDE7}	F	TDO / Up[17]	TDO / Up	E25	F27
TMS	JTAG test mode select input	P	I	V_{DDE7}	F	TMS / Up	TMS / Up	E24	E26
JCOMP	JTAG TAP controller enable	P	I	V_{DDE7}	F	JCOMP / Down	JCOMP / Down	F24	F26
$\overline{TEST}$	Test mode select	P	I	V_{DDE7}	F	$\overline{TEST}$ / Up	$\overline{TEST}$ / Up	E26	F28
FlexCAN									
CNTXA_ TXDA_ GPIO[83]	FlexCAN A transmit eSCI A transmit GPIO	P A G	O O I/O	V_{DDEH4}	SH	I / Up	– / Up [18]	AD21	AF22
CNRXA_ RXDA_ GPIO[84]	FlexCAN A receive eSCI A receive GPIO	P A G	I I I/O	V_{DDEH4}	SH	– / Up	– / Up [18]	AE22	AG22
CNTXB_ PCSC[3]_ GPIO[85]	FlexCAN B transmit DSPI C peripheral chip select GPIO	P A G	O O I/O	V_{DDEH4}	MH	– / Up	– / Up	AF22	AG23
CNRXB_ PCSC[4]_ GPIO[86]	FlexCAN B receive DSPI C peripheral chip select GPIO	P A G	I O I/O	V_{DDEH4}	MH	– / Up	– / Up	AF23	AH23

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
CNTXC_ PCSD[3]_ GPIO[87]	FlexCAN C transmit DSPI D peripheral chip select GPIO	P A G	O O I/O	V_{DDEH6}	MH	– / Up	– / Up	V23	W24
CNRXC_ PCSD[4]_ GPIO[88]	FlexCAN C receive DSPI D peripheral chip select GPIO	P A G	I O I/O	V_{DDEH6}	MH	– / Up	– / Up	W24	Y26
eSCI									
TXDA_ GPIO[89]	eSCI A transmit GPIO	P G	O I/O	V_{DDEH6}	SH	– / Up	– / Up [18]	U24	V24
RXDA_ GPIO[90]	eSCI A receive GPIO	P G	I I/O	V_{DDEH6}	SH	– / Up	– / Up [18]	V24	U26
TXDB_ PCSD[1]_ GPIO[91]	eSCI B transmit DSPI D peripheral chip select GPIO	P A G	O O I/O	V_{DDEH6}	MH	– / Up	– / Up	W25	Y27
RXDB_ PCSD[5]_ GPIO[92]	eSCI B receive DSPI D peripheral chip select GPIO	P A G	I O I/O	V_{DDEH6}	MH	– / Up	– / Up	W23	Y24
DSPI									
SCKA_ PCSC[1]_ GPIO[93]	DSPI A clock DSPI C peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH6}	MH	– / Up	– / Up	R26	U27
SINA_ PCSC[2]_ GPIO[94]	DSPI A data input DSPI C peripheral chip select GPIO	P A G	I O I/O	V_{DDEH6}	MH	– / Up	– / Up	R25	P27
SOUTA_ PCSC[5]_ GPIO[95]	DSPI A data output DSPI C peripheral chip select GPIO	P A G	O O I/O	V_{DDEH6}	MH	– / Up	– / Up	R24	P24
PCSA[0]_ PCSD[2]_ GPIO[96]	DSPI A peripheral chip select DSPI D peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH6}	MH	– / Up	– / Up	T24	R24
PCSA[1]_ PCSB[2]_ [19] GPIO[97]	DSPI A peripheral chip select DSPI B peripheral chip select GPIO	P A G	O O I/O	V_{DDEH6}	MH	– / Up	– / Up	T23	T24
PCSA[2]_ SCKD_ GPIO[98]	DSPI A peripheral chip select DSPI D clock GPIO	P A G	O I/O I/O	V_{DDEH6}	MH	– / Up	– / Up	T25	N26
PCSA[3]_ SIND_ GPIO[99]	DSPI A peripheral chip select DSPI D data input GPIO	P A G	O I I/O	V_{DDEH6}	MH	– / Up	– / Up	P23	N24
PCSA[4]_ SOUTD_ GPIO[100]	DSPI A peripheral chip select DSPI D data output GPIO	P A G	O O I/O	V_{DDEH6}	MH	– / Up	– / Up	U23	U24
PCSA[5]_ PCSB[3]_ [19] GPIO[101]	DSPI A peripheral chip select DSPI B peripheral chip select GPIO	P A G	O O I/O	V_{DDEH6}	MH	– / Up	– / Up	U25	T26

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
SCKB_ [19] PCSC[1]_ GPIO[102]	DSPI B clock DSPI C peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH10}	MH	– / Up	– / Up	P25	T27
SINB_ [19] PCSC[2]_ GPIO[103]	DSPI B data input DSPI C peripheral chip select GPIO	P A G	I O I/O	V_{DDEH10}	MH	– / Up	– / Up	M26	P28
SOUTB_ [19] PCSC[5]_ GPIO[104]	DSPI B data output DSPI C peripheral chip select GPIO	P A G	O O I/O	V_{DDEH10}	MH	– / Up	– / Up	N23	N28
PCSB[0]_ [19] PCSD[2]_ GPIO[105]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH10}	MH	– / Up	– / Up	N25	R27
PCSB[1]_ [19] PCSD[0]_ GPIO[106]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A G	O I/O I/O	V_{DDEH10}	MH	– / Up	– / Up	N26	R28
PCSB[2]_ [19] SOUTC_ GPIO[107]	DSPI B peripheral chip select DSPI C data output GPIO	P A G	O O I/O	V_{DDEH10}	MH	– / Up	– / Up	P26	T28
PCSB[3]_ [19] SINC_ GPIO[108]	DSPI B peripheral chip select DSPI C data input GPIO	P A G	O I I/O	V_{DDEH10}	MH	– / Up	– / Up	N24	M27
PCSB[4]_ [19] SCKC_ GPIO[109]	DSPI B peripheral chip select DSPI C clock GPIO	P A G	O I/O I/O	V_{DDEH6}	MH	– / Up	– / Up	P24	N27
PCSB[5]_ [19] PCSC[0]_ GPIO[110]	DSPI B peripheral chip select DSPI C peripheral chip select GPIO	P A G	O I/O I/O	V_{DDEH6}	MH	– / Up	– / Up	R23	M26
eQADC									
AN[0]_ DAN0+	Single-ended analog input Positive terminal differential input	P	I	V_{DDA1} [20]	A	I / –	AN[0] / –	B7	C9
AN[1]_ DAN0-	Single-ended analog input Negative terminal differential input	P	I	V_{DDA1} [20]	A	I / –	AN[1] / –	A7	B8
AN[2]_ DAN1+	Single-ended analog input Positive terminal differential input	P	I	V_{DDA1} [20]	A	I / –	AN[2] / –	D9	G12
AN[3]_ DAN1-	Single-ended analog input Negative terminal differential input	P	I	V_{DDA1} [20]	A	I / –	AN[3] / –	C8	E10
AN[4]_ DAN2+	Single-ended analog input Positive terminal differential input	P	I	V_{DDA1} [20]	A	I / –	AN[4] / –	B8	C10
AN[5]_ DAN2-	Single-ended analog input Negative terminal differential input	P	I	V_{DDA1} [20]	A	I / –	AN[5] / –	A8	B9
AN[6]_ DAN3+	Single-ended analog input Positive terminal differential input	P	I	V_{DDA1} [20]	A	I / –	AN[6] / -	D10	G13
AN[7]_ DAN3-	Single-ended analog input Negative terminal differential input	P	I	V_{DDA1} [20]	A	I / –	AN[7] / -	C9	E11

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
AN[8]_ ANW	Single-ended analog input External multiplexed analog input	P	I	V_{DDA1} [20]	A	I / –	AN[8] / –	C4	E7
AN[9]_ ANX_	Single-ended analog input External multiplexed analog input	P	I	V_{DDA1} [20]	A	I / –	AN[9] / –	D6	C4
AN[10]_ ANY	Single-ended analog input External multiplexed analog input	P	I	V_{DDA1} [20]	A	I / –	AN[10] / –	D7	E6
AN[11]_ ANZ	Single-ended analog input External multiplexed analog input	P	I	V_{DDA1} [20]	A	I / –	AN[11] / –	A4	B6
AN[12]_ MA[0]_ $\overline{SDS}$	Single-ended analog input Mux address eQADC serial data strobe	P [21] A G [22]	I O O	V_{DDEH9}	MH, A [23]	I / –	AN[12] / –	D15	H15
AN[13]_ MA[1]_ SDO	Single-ended analog input Mux address eQADC serial data out	P [21] A G [22]	I O O	V_{DDEH9}	MH, A [23]	I / –	AN[13] / –	C15	G15
AN[14]_ MA[2]_ SDI	Single-ended analog input Mux Address eQADC Serial Data In	P [21] A G [22]	I O I	V_{DDEH9}	MH, A [23]	I/ –	AN[14] / –	B15	E16
AN[15]_ FCK	Single-ended analog input eQADC Free Running Clock	P [21] G [22]	I O	V_{DDEH9}	MH, A [23]	I / –	AN[15] / –	A15	C16
AN[16:18]	Single-ended analog input	P	I	V_{DDA1} [20]	A	I / –	AN[16:18] / –	A6, C5, D8	B7, E8, H12
AN[19:20]	Single-ended analog input	P	I	V_{DDA1} [20]	A	I / –	AN[19:20] / –	B5, B6	C7, C8
AN[21:25]	Single-ended analog input	P	I	V_{DDA0} [20]	A	I / –	AN[21:25] / –	C7, B10, A10, D11, C11	E9, C11, B11, H13, E12
AN[26]	Single-ended analog input	P	I	V_{DDA0} [20]	A	I / –	AN[26] / –	B11	C12
AN[27:28]	Single-ended analog input	P	I	V_{DDA0} [20]	A	I / –	AN[27:28] / –	A11, A12	B12, A13
AN[29]	Single-ended analog input	P	I	V_{DDA0} [20]	A	I / –	AN[29] / –	D12	E13
AN[30:32]	Single-ended analog input	P	I	V_{DDA0} [20]	A	I / –	AN[30:32] / –	C12, B12, B13	C13, B13, B14
AN[33]	Single-ended analog input	P	I	V_{DDA0} [20]	A	I / –	AN[33] / –	C13	E14
AN[34:35]	Single-ended analog input	P	I	V_{DDA0} [20]	A	I / –	AN[34:35] / –	D13, A13	G14, A14
AN[36]	Single-ended analog input	P	I	V_{DDA1} [20]	A	I / –	AN[36] / –	B3	C5
AN[37:39]	Single-ended analog input	P	I	V_{DDA1} [20]	A	I / –	AN[37:39] / –	A3, D5, B4	B5, B4, C6
ETRIG[0]_ GPIO[111]	eQADC trigger input GPIO	P G	I I/O	V_{DDEH8}	SH	– / Up	– / Up	B16	A16
ETRIG[1]_ GPIO[112]	eQADC trigger input GPIO	P G	I I/O	V_{DDEH8}	SH	– / Up	– / Up	A16	B16
V_{RH}	Voltage reference high	P	I	– [20]	V_{DDINT}	– / –	VRH	A9	A9

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
V_{RL}	Voltage reference low	P	I	– [20]	V_{SSINT}	– / –	VRL	C10	A10
REFBYPC	Reference bypass capacitor input	P	I	– [20]	V_{DDINT}	– / –	REFBYPC	B9	B10
eTPU									
TCRCLKA_ $\overline{IRQ}$[7]_ GPIO[113]	eTPU A TCR clock External interrupt request GPIO	P A G	I I I/O	V_{DDEH1}	SH	– / Up	– / Up	N4	N5
ETPUA[0:3]_ ETPUA[12:15]_ GPIO[114:117]	eTPU A channel eTPU A channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH1}	SH	– / WKPCFG	– / WKPCFG	N3, M4, M3, M2	M5, G8, M3, L3
ETPUA[4:11]_ ETPUA[16:23]_ GPIO[118:125]	eTPU A channel eTPU A channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH1}	SH	– / WKPCFG	– / WKPCFG	M1, L4, L3, L2, L1, K4, K3, K2	L2, H9, M2, K3, K2, G9, L5, J3
ETPUA[12]_ PCSB[1]_ GPIO[126]	eTPU A channel DSPI B peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	K1	J2
ETPUA[13]_ PCSB[3]_ GPIO[127]	eTPU A channel DSPI B peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	J4	G10
ETPUA[14]_ PCSB[4]_ GPIO[128]	eTPU A channel DSPI B peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	J3	K5
ETPUA[15]_ PCSB[5]_ GPIO[129]	eTPU A channel DSPI B peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	J2	H3
ETPUA[16]_ PCSD[1]_ GPIO[130]	eTPU A channel DSPI D peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	J1	K1
ETPUA[17]_ PCSD[2]_ GPIO[131]	eTPU A channel DSPI D peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	H4	H10
ETPUA[18]_ PCSD[3]_ GPIO[132]	eTPU A channel DSPI D peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	H3	J5
ETPUA[19]_ PCSD[4]_ GPIO[133]	eTPU A channel DSPI D peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	H2	G3
ETPUA[20:23]_ $\overline{IRQ}$[8:11]_ GPIO[134:137]	eTPU A channel External interrupt request GPIO	P A G	I/O I I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	H1, G4, G2, G1	J1, H11, F3, H2
ETPUA[24:27]_ $\overline{IRQ}$[12:15]_ GPIO[138:141]	eTPU A channel (output only) External interrupt request GPIO	P A G	O I I/O	V_{DDEH1}	SH	– / WKPCFG	– / WKPCFG	F1, G3, F3, F2	G2, H5, G5, E3
ETPUA[28]_ PCSC[1]_ GPIO[142]	eTPU A channel (output only) DSPI C peripheral chip select GPIO	P A G	O O I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	E1	F1

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
ETPUA[29]_ PCSC[2]_ GPIO[143]	eTPU A channel (output only) DSPI C peripheral chip select GPIO	P A G	O O I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	E2	F2
ETPUA[30]_ PCSC[3]_ GPIO[144]	eTPU A channel DSPI C peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	D1	E1
ETPUA[31]_ PCSC[4]_ GPIO[145]	eTPU A Channel DSPI C peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH1}	MH	– / WKPCFG	– / WKPCFG	D2	E2
TCRCLKB_ $\overline{IRQ}$[6]_ GPIO[146]	eTPU B TCR clock External interrupt request GPIO	P A G	I I I/O	V_{DDEH6}	SH	– / Up	– / Up	M23	K21
ETPUB[0:15]_ ETPUB[16:31]_ GPIO[147:162]	eTPU B channel eTPU B channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH6}	SH	– / WKPCFG	– / WKPCFG	M25, M24, L26, L25, L24, K26, L23, K25, K24, J26, K23, J25, J24, H26, H25, G26	L22, K22, L26, M24, J22, K26, H20, L24, G21, L27, H19, K27, G20, K28, J27, J28
ETPUB[16]_ PCSA[1]_ GPIO[163]	eTPU B channel DSPI A peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH8}	MH	– / WKPCFG	– / WKPCFG	D16	E18
ETPUB[17]_ PCSA[2]_ GPIO[164]	eTPU B channel DSPI A peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH8}	MH	– / WKPCFG	– / WKPCFG	D17	E19
ETPUB[18]_ PCSA[3]_ GPIO[165]	eTPU B channel DSPI A peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH8}	MH	– / WKPCFG	– / WKPCFG	A17	G17
ETPUB[19]_ PCSA[4]_ GPIO[166]	eTPU B channel DSPI A peripheral chip select GPIO	P A G	I/O O I/O	V_{DDEH8}	MH	– / WKPCFG	– / WKPCFG	C16	G16
ETPUB[20:31]_ GPIO[167:178]	eTPU B channel GPIO	P G	I/O I/O	V_{DDEH8}	MH	– / WKPCFG	– / WKPCFG	A18, B17, C17, D18, A19, B18, C18, A20, B19, D19, C19, B20	B17, H16, C17, E20, B18, E17, E22, B19, C18, E21, E23, C19
eMIOS									
EMIOS[0:2]_ ETPUA[0:2]_ GPIO[179:181]	eMIOS channel eTPU A channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AF15, AE15, AC16	AD17, AD21, P21
EMIOS[3:5]_ ETPUA[3:5]_ GPIO[182:184]	eMIOS channel eTPU A channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AD15, AF16, AE16	R22, AD18, AD22
EMIOS[6:7]_ ETPUA[6:7]_ GPIO[185:186]	eMIOS channel eTPU A channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AD16, AF17	P22, AD19

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
EMIOS[8:9]_ ETPUA[8:9]_ GPIO[187:188]	eMIOS channel eTPU A channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AC17, AE17	N21, AD23
EMIOS[10:11]_ PCSD[3:4]_ GPIO[189:190]	eMIOS channel DSPI D peripheral chip selects GPIO	P A G	I/O I/O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AD17, AF18	N22, AG18
EMIOS[12]_ SOUTC_ GPIO[191]	eMIOS channel (output only) DSPI C data output GPIO	P A G	O O I/O	V_{DDEH4}	MH	– / WKPCFG	– / WKPCFG	AC18	M21
EMIOS[13]_ SOUTD_ GPIO[192]	eMIOS channel (output only) DSPI D data output GPIO	P A G	O O I/O	V_{DDEH4}	MH	– / WKPCFG	– / WKPCFG	AE18	AF18
EMIOS[14]_ $\overline{\text{IRQ}}$[0]_ CNTXD_ GPIO[193]	eMIOS channel (input/output) External interrupt request FlexCAN D transmit GPIO	P A A2 G	O I O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AF19	AH19
EMIOS[15]_ $\overline{\text{IRQ}}$[1]_ CNRXD_ GPIO[194]	eMIOS channel (input/output) External interrupt request FlexCAN D receive GPIO	P A A2 G	O I I I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AD18	M22
EMIOS[16]_ ETPUB[0]_ GPIO[195]	eMIOS channel eTPU B channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AE19	AG19
EMIOS[17]_ ETPUB[1]_ GPIO[196]	eMIOS channel eTPU B channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AD19	AF19
EMIOS[18]__ ETPUB[2]_ GPIO[197]	eMIOS channel eTPU B channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AF20	AH20
EMIOS[19]__ ETPUB[3]_ GPIO[198]	eMIOS channel eTPU B channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH4}	SH	–/ WKPCFG	– / WKPCFG	AE20	AG20
EMIOS[20]_ ETPUB[4]_ GPIO[199]	eMIOS channel eTPU B channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AF21	AG21
EMIOS[21]__ ETPUB[5]_ GPIO[200]	eMIOS channel eTPU B channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AC19	L21
EMIOS[22]__ ETPUB[6]_ GPIO[201]	eMIOS channel eTPU B channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AD20	AF20
EMIOS[23]__ ETPUB[7]_ GPIO[202]	eMIOS channel eTPU B channel (output only) GPIO	P A G	I/O O I/O	V_{DDEH4}	SH	– / WKPCFG	– / WKPCFG	AE21	AF21

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
GPIO									
EMIOS[14:15]_ GPIO[203:204] [24]	eMIOS channel (output only) GPIO	P G	O I/O	V_{DDEH6}	SH	– / Up	– / Up	H24, G25	J26, H27
GPIO[205] [25]	GPIO	G	I/O	V_{DDEH8}	MH	– / Up	– / Up	A21	B22
GPIO[206:207] [26, 27]	GPIO	G	I/O	V_{DDE3}	F	– / Up	– / Up	AF8, AD10	AH10, AG10
Clock Synthesizer									
XTAL	Crystal oscillator output	P	O	V_{DDSYN}	A	O / –	XTAL [28] / –	AB26	AD28
EXTAL_ EXTCLK [29]	Crystal oscillator input External clock input	P A	I I	V_{DDSYN}	A	I / –	EXTAL [30] / –	AA26	AC28
CLKOUT	System clock output	P	O	V_{DDE5}	F	CLKOUT / Enabled	CLKOUT / Enabled	AE24	AF25
ENGCLK	Engineering clock output	P	O	V_{DDE5}	F	ENGCLK/ Enabled	ENGCLK / Enabled	AF25	AG26
Power / Ground									
V_{RC33} [31]	Voltage regulator control supply	P	I	3.3 V	V_{DDINT}	N/A	V_{RC33}	AC25	AD26
V_{RCVSS}	Voltage regulator control ground	P	I	0.0 V	V_{SSINT}	N/A	V_{RCVSS}	Y25	V27
V_{RCCTL}	Voltage regulator control output	P	O	3.3 V	V_{DDINT}	N/A	V_{RCCTL}	AB24	AC26
V_{DDA0} [32]	Analog power input ADC0	P	I	5.0 V	V_{DDINT}	N/A	V_{DDA0}	C14	E15
V_{SSA0} [32]	Analog ground input ADC0	P	I	—	V_{SSINT}	N/A	V_{SSA0}	A14, B14	A15, B15
V_{DDA1} [32]	Analog power input ADC1	P	I	5.0 V	V_{DDINT}	N/A	V_{DDA1}	A5	A5
V_{SSA1} [32]	Analog ground input ADC1	P	I	—	V_{SSINT}	N/A	V_{SSA1}	C6	A6
V_{DDSYN}	Clock synthesizer power input	P	I	3.3 V	V_{DDE}	N/A	V_{DDSYN}	AC26	AD27
V_{SSSYN}	Clock synthesizer ground input	P	I	—	V_{SSE}	N/A	V_{SSSYN}	Y26	AC27
V_{FLASH}	Flash read supply input	P	I	3.3 V	V_{DDINT}	N/A	V_{FLASH}	U26	W27
V_{PP} [33]	Flash program/erase supply input	P	I	5.0 V	V_{DDINT}	N/A	V_{PP}	T26	W28
V_{STBY} [34]	SRAM standby power input	P	I	0.8–1.2 V	V_{STBY}	N/A	V_{STBY}	A2	B3
V_{DD}	Internal logic supply input	P	I	1.5 V	V_{DD}	N/A	V_{DD}	A24,B1, C2, C26, D3, E4, AB23, AC5, AC24, AD4, AD25, AE3, AE26, AF2	B25, C2, D3, D27, F5, H7, J8, Y21, AA9, AA22, AB8, AC24, AD6, AE27, AF4, AF27, AG3

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
V_{DDE2} [35]	External I/O supply input	P	I	1.8–3.3 V	V_{DDE}	N/A	V_{DDE}	M10, M11, N10, N11, P10, P11, R10, R11, T1, T4, T10, T12, T13, T14, T15, U11, U12, U13, U14, U15, Y4, AB1, AC8, AC13, AF5, AF11	M11, N11, N12, N13, P11, P12, P13, R1, V5, AA5, AC1
V_{DDE3} [35]	External I/O supply input	P	I	1.8–3.3 V	V_{DDE}	N/A	V_{DDE}	—	T14, U13, U14, V12, V13, V14, AD9, AD14, AH6, AH14
V_{DDE5}	External I/O supply input	P	I	1.8–3.3 V	V_{DDE}	N/A	V_{DDE}	AC21, AD22, AE23, AF24	AF23, AG24, AH24
V_{DDE7}	External I/O supply input	P	I	1.8–3.3 V	V_{DDE}	N/A	V_{DDE}	B26, C25, D24, E23, K14, K15, K16, K17, L17, M17, N17	C27, D26, F24, H22, J21, L15, L16, L17, L18, M18, N18, P18
V_{DDE12}	External I/O supply input	P	I	1.8–3.3 V	V_{DDE}	N/A	V_{DDE}	—	K7, N8, R11, R12, R13, R17, R18, R21, T11, T12, T15, T18, U2, U11, U15, U16, V15, V16, V17, V22, AA13, AA16, AB18, AB21, AE2, AG4, AG12
V_{DDEH1}	External I/O supply input	P	I	3.3–5.0 V	V_{DDE}	N/A	V_{DDEH}	E3, F4	G11, J7
V_{DDEH4}	External I/O supply input	P	I	3.3–5.0 V	V_{DDE}	N/A	V_{DDEH}	AC20	AD20
V_{DDEH6}	External I/O supply input	P	I	3.3–5.0 V	V_{DDE}	N/A	V_{DDEH}	AA23	V26
V_{DDEH8}	External I/O supply input	P	I	3.3–5.0 V	V_{DDE}	N/A	V_{DDEH}	D22	C21
V_{DDEH9} [36]	External I/O supply input	P	I	3.3–5.0 V	V_{DDE}	N/A	V_{DDEH}	D14	H14
V_{DDEH10}	External I/O supply input	P	I	3.3–5.0 V	V_{DDE}	N/A	V_{DDEH}	J23	K24

Table 2-1. MPC5566 Signal Properties (continued)

Signal Names	Signal Functions [1]	P/A/G	I/O Type	Voltage [2]	Pad Type [3]	Status		416 Package	496 Vertical Assembly [4]
						During Reset [5]	After Reset [6]		
V_{DD33} [37]	I/O pad pre-driver and level shifter reference voltage input	P	I	3.3 V	V_{DD33}	N/A	3.3 V	A25, C1, U4, AD9, AD26	B26, D2, W5, AE27, AF9
V_{SS}	Ground	P	—	—	V_{SSINT}	N/A	V_{SS}	A1, A26, B2, B25, C3, C24, D4, D23, K10, K11, K12, K13, L10, L11, L12, L13, L14, L15, L16, M12, M13, M14, M15, M16, N12, N13, N14, N15, N16, P12, P13, P14, P15, P16, P17, R12, R13, R14, R15, R16, R17, T11, T16, T17, U10, U16, U17, AC4, AC23, AD3, AD24, AE2, AE25, AF1, AF26	A1, A2, A27, A28, B1, B2, B27, B28, C3, C26, E5, E24, G7, G22, H8, H21, L11, L12, L13, L14, M12, M13, M14, M15, M16, M17, N14, N15, N16, N17, P14, P15, P16, P17, R14, R15, R16, T13, T16, T17, U12, U17, U18, V11, V18, AA8, AA21, AB7, AB22, AD5, AF3, AF26, AG1, AG2, AG27, AG28, AH1, AH2, AH27, AH28, AD24
No Connect									
NC [38]	No connect	N/A	N/A	N/A	N/A	N/A	N/A	AC22, AD23	G18, G19, H17, H18, AF24, AG25

1 For each pin in the table, each line in a Function row is a separate function of the pin. For all MPC5566 I/O pins the selection of primary pin function or secondary function or GPIO is done in the MPC5566 SIU except where explicitly noted.

2 V_{DDE} (fast I/O) and V_{DDEH} (slow I/O) power supply inputs are grouped into segments. Each segment of V_{DDEH} pins can connect to a separate 3.3–5.0 V (+5% to –10%) power supply input. Each segment of V_{DDE} pins can connect to a separate 1.8–3.3 V (±10%) power supply, with the exception of the V_{DDE2} and V_{DDE3} segments that are shorted together and must use the same power supply input. This segment is labeled V_{DDE2} in the BGA map.

3 The pad type is indicated by one of the abbreviations; F for fast, MH for medium (high voltage), MHA for medium (high voltage) and analog, SH for slow (high voltage), A for analog. Some pads may have two types, depending on which pad function is selected.

4 The 496 assembly contains the VertiCal base and includes the 416 pins.

5 The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. Terminology is O = output, I = input, Up = weak pull up enabled, Down = weak pull down enabled, Low = output driven low, High = output driven high. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

6 Function after reset of GPI is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

[7] PLLCFG[2] is tied to ground in this device.
[8] The EBI is specified and tested at 1.8–3.3 V.
[9] Do not configure both the primary function in ADDR[8:11]_GPIO[4:7] and the secondary function in $\overline{CS}$[0:3]_ADDR[8:11]_GPIO[0:3] pins to be the address input. Only configure one set of pins for the address input.
[10] When using the EBI functions, select the function in the SIU_PCR register, and then enable the EBI functions in the EBI registers for these pins. Both the SIU and EBI configurations must match to operation correctly.
[11] The function and state of this pin(s) after execution of the BAM program is determined by the BOOTCFG[0:1] pins. Read Table 16-8 for details on the External Bus Interface (EBI) configuration after execution of the BAM program.
[12] ADDR[6:7] are for master accesses to increase the memory space and are not used for slave accesses to the chip.
[13] GPIO is selected in the SIU_PCR register. When configured for EBI operation, the pin function of write enable ($\overline{WE}$) or byte enable ($\overline{BE}$) is specified in the EBI_BR*n* and EBI_CAL_BR*n* registers for each chip select region.
[14] MCKO is only enabled if debug mode is enabled. Debug mode can be enabled before or after exiting system reset ($\overline{RSTOUT}$ negated).
[15] MDO[0] is driven high following a power-on reset until the system clock achieves lock, at which time it is then negated. There is an internal pull up on MDO[0].
[16] The function of the MDO[11:4]_GPIO[82:75] pins is selected during a debug port reset by the $\overline{EVTI}$ pin or by selecting FPM in the NPC_PCR. When functioning as MDO[4:11] the pad configuration specified by the SIU does not apply. Read Section 2.3.3.6, "Nexus Message Data Out / GPIO MDO[11:4]_GPIO[82:75]" for more detail on MDO[4:11] pin operation.
[17] The pull-up on TDO is only functional when not in JTAG mode, that is with JCOMP negated.
[18] The function and state of the FlexCAN A and eSCI A pins after execution of the BAM program is determined by the BOOTCFG[0:1] pins. Read Table 16-9 for details on the FlexCAN and eSCI pin configuration after execution of the BAM program.
[19] For compatibility to the MPC5554, always power V_{DDEH6} and V_{DDEH10} from the same power supply (3–5.25 V). To allow one DSPI to operate at a different operating voltage, connect V_{DDEH6} and V_{DDEH10} to separate power supplies, but this configuration is not compatible with the MPC5554.
[20] All analog input channels are connected to both ADC blocks. The supply designation for this pin(s) specifies only the ESD rail used.
[21] To use this analog function, the PA field of the corresponding SIU_PCR register should be set to 0b11.
[22] To select this function the PA field of the corresponding SIU_PCR register should be set for GPIO.
[23] If analog features are used, tie V_{DDEH9} to V_{DDA1}.
[24] Because other balls already are named EMIOS[14:15], the balls for these signals are named GPIO[203:204].
[25] The GPIO[205] pin is a protect for pin for configuring an external boot for a double data rate memory.
[26] The GPIO[206:207] pins are protect for pins for double data rate memory data strobes.
[27] GPIO[206:207] can be selected as the source for the eQADC trigger in the eQADC trigger input select register (SIU_ETISR).
[28] The function after reset of the XTAL pin is determined by the value of the signal on the PLLCFG[1] pin. When bypass mode is chosen XTAL has no function and must be grounded.
[29] When the FMPLL is configured for external reference mode, the V_{DDE5} supply affects the acceptable signal levels for the external reference. Refer to Section 11.1.4.2, "External Reference Mode."
[30] The function after reset of the EXTAL_EXTCLK pin is determined by the value of the signal on the PLLCFG[1] pin. If the EXTCLK function is chosen, the valid operating voltage for the pin is 1.62–3.60 V. If the EXTAL function is chosen, the valid operating voltage is 3.3 V.
[31] V_{RC33} is the 3.3 V input for the voltage regulator control.
[32] The $V_{DDA}n$ and $V_{SSA}n$ power supply inputs are split into separate traces in the package substrate. Each trace is bonded to a separate pad location, which provides isolation between the analog and digital sections within each ADC.
[33] Can be tied to 5.0 V for both read operation and program/erase.
[34] Tie the V_{STBY} pin to V_{SS} if the battery backed SRAM is not used.
[35] Both V_{DDE2} and V_{DDE3} pins are labeled as V_{DDE2} pins on the BGA maps. V_{DDE3} can be connected internally to V_{DDE2}.
[36] The V_{DDEH9} segment can be powered from 3.0–5.0 V for mux address or SSI functions, but must meet the V_{DDA} specifications of 4.5–5.25 V for analog input function.
[37] All pins with pad type F are driven to a high state if their V_{DDE} segment is powered before V_{DD33}.
[38] The pins are reserved for the clock and inverted clock outputs for DDR memory interface.

2.3 Detailed Signal Description

This section gives detailed descriptions of the device signals. Read Section 2.2.2, "Device Signals Summary," for the signal properties.

2.3.1 Reset and Configuration Signals

2.3.1.1 External Reset Input RESET

The RESET input is asserted by an external device to reset the all modules of the device MCU. The RESET pin must be asserted during a power-on reset.

Read Section 4.2.1, “Reset Input (RESET).”

2.3.1.2 External Reset Output RSTOUT

The RSTOUT output is a push/pull output that is asserted during an internal device reset. The pin can also be asserted by software without causing an internal reset of the device MCU.

Read Section 4.2.2, “Reset Output (RSTOUT).”

NOTE

During a power-on-reset (POR), RSTOUT is tri-stated.

2.3.1.3 Phase Locked-Loop Configuration / External Interrupt Request / GPIO PLLCFG[0]_IRQ[4]_GPIO[208]

PLLCFG[0]_IRQ[4]_GPIO[208] are sampled on the negation of the RESET input pin, if the RSTCFG pin is asserted at that time. The values are used to configure the FMPLL mode of operation. The alternate function is an external interrupt request input.

2.3.1.4 Phase Locked-Loop Configuration / External Interrupt Request / DSPI / GPIO PLLCFG[1]_IRQ[5]_SOUTD_GPIO[209]

PLLCFG[1]_IRQ[5]_SOUTD_GPIO[209] — If the RSTCFG signal is asserted, these functions are sampled at that time when the RESET input pin negates. The values are used to configure the FMPLL operation mode. The alternate function is an external interrupt request input, and the second alternate function is the data output for the DSPI module D.

2.3.1.5 Phase Locked-Loop Configuration PLLCFG[2]

The MPC5566 does not use PLLCFG[2], therefore PLLCFG[2] is tied low.

Read Section 11.3.1.1, “Synthesizer Control Register (FMPLL_SYNCR).”

2.3.1.6 Reset Configuration Input / GPIO RSTCFG_GPIO[210]

The RSTCFG input is used to enable the BOOTCFG[0:1] and PLLCFG[0:1] pins during reset. If RSTCFG is negated during reset, the BOOTCFG and PLLCFG pins are not sampled at the negation of RSTOUT. In that case, the default values for BOOTCFG and PLLCFG are used. If RSTCFG is asserted during reset, the values on the BOOTCFG and PLLCFG pins are sampled and configure the boot and FMPLL modes.

2.3.1.7 Reset Configuration / External Interrupt Request / GPIO BOOTCFG[0:1]_IRQ[2:3]_GPIO[211:212]

BOOTCFG[0:1]_IRQ[2:3]_GPIO[211:212] signals are sampled on the negation of the RSTOUT pin, only if RSTCFG is asserted at that time. The values are used by the Boot Assist Module (BAM) program to determine the boot configuration of the device. The alternate functions are the external interrupt request inputs (IRQs).

2.3.1.8 Weak Pull Configuration / GPIO WKPCFG_GPIO[213]

WKPCFG_GPIO[213] determines whether specified eTPU and eMIOS pins are connected to a weak pullup or weak pulldown during and immediately after reset.

2.3.2 External Bus Interface (EBI) Signals

2.3.2.1 External Chip Select / External Address / GPIO CS[0]_ADDR[8]_GPIO[0]

CS[0]_ADDR[8]_GPIO[0] is an external bus interface (EBI) chip select output signals. ADDR[8] is the alternate signal function and is an external bus address function.

2.3.2.2 External Chip Select / External Address / GPIO CS[1:3]_ADDR[9:11]_GPIO[1:3]

CS[1:3]_ADDR[9:11]_GPIO[1:3] are the external bus interface (EBI) chip select output signals. The alternate functions are the ADDR[9:11] and is an external bus address function.

2.3.2.3 External Address / GPIO ADDR[8:11]_GPIO[4:7]

ADDR[8:11]_GPIO[4:7] are the External Bus Interface (EBI) address signals.

2.3.2.4 External Address / GPIO ADDR[12:29]_GPIO[8:25]

ADDR[12:29]_GPIO[8:25] are External Bus Interface (EBI) address signals.

2.3.2.5 External Address / Master Address Expansion / GPIO ADDR[30:31]_ADDR[6:7]_GPIO[26:27]

ADDR[30:31]_ADDR[6:7]_GPIO[26:27] are the EBI address signals. Use the ADDR[6:7] alternate signal functions to increase memory for master accesses; these signal cannot be used for slave accesses to the chip.

2.3.2.6 External Data / GPIO DATA[0:15]_GPIO[28:43]

DATA[0:15]_GPIO[28:43] are the EBI data signals for the first 16-bits.

2.3.2.7 External Data / Ethernet Transmit Clock / GPIO DATA[16]_FEC_TX_CLK_GPIO[44]

DATA[16]_FEC_TX_CLK_GPIO[44] is an EBI data signal. The alternate signal is FEC transmit clock.

2.3.2.8 External Data / Ethernet Carrier Sense Data / GPIO DATA[17]_FEC_CRS_GPIO[45]

DATA[17]_FEC_CRS_GPIO[45] is an EBI data signal. The alternate signal is FEC carrier sense data function.

2.3.2.9 External Data / Ethernet Transmit Error / GPIO DATA[18]_FEC_TX_ER_GPIO[46]

DATA[18]_FEC_TX_ER_GPIO[46] is an EBI data signal. The alternate signal is FEC transmit error.

2.3.2.10 External Data / Ethernet Receive Clock / GPIO DATA[19]_FEC_RX_CLK_GPIO[47]

DATA[19]_FEC_RX_CLK_GPIO[47] is an EBI data signal. The alternate signal is FEC receive clock.

2.3.2.11 External Data / Ethernet Transmit Data / GPIO DATA[20]_FEC_TXD[0]_GPIO[48]

DATA[20]_FEC_TXD[0]_GPIO[48] is an EBI data signal. The alternate signal is FEC transmit data [0] function.

2.3.2.12 External Data / Ethernet Receive Error / GPIO DATA[21]_FEC_RX_ER_GPIO[49]

DATA[21]_FEC_RX_ER_GPIO[49] is an EBI data signal. The alternate function is FEC receive error function.

2.3.2.13 External Data / Ethernet Receive Data / GPIO DATA[22]_FEC_RXD[0]_GPIO[50]

DATA[22]_FEC_RXD[0]_GPIO[50] is an EBI data signal. The alternate function is the FEC receive data [0] function.

2.3.2.14 External Data / Ethernet Transmit Data / GPIO DATA[23]_FEC_TXD[3]_GPIO[51]

DATA[23]_FEC_TXD[3]_GPIO[51] is an EBI data signal. The alternate function is FEC transmit data [3] function.

2.3.2.15 External Data / Ethernet Collision Detect / GPIO DATA[24]_FEC_COL_GPIO[52]

DATA[24]_FEC_COL_GPIO[52] is an EBI data signal.The alternate function is an FEC collision detect signal function.

2.3.2.16 External Data / Ethernet Receive Data Valid / GPIO DATA[25]_FEC_RX_DV_GPIO[53]

DATA[25]_FEC_RX_DV_GPIO[53] is an EBI data signal. The alternate function is an FEC receive data valid function.

2.3.2.17 External Data / Ethernet Transmit Enable / GPIO DATA[26]_FEC_TX_EN_GPIO[54]

DATA[26]_FEC_TX_EN_GPIO[54] is an EBI data signal. The alternate function is the FEC transmit enable.

2.3.2.18 External Data / Ethernet Transmit Data / GPIO DATA[27]_FEC_TXD[2]_GPIO[55]

DATA[27]_FEC_TXD[2]_GPIO[55] is an EBI data signal. The alternate function is the FEC transmit data [2].

2.3.2.19 External Data / Ethernet Transmit Data / GPIO DATA[28]_FEC_TXD[1]_GPIO[56]

DATA[28]_FEC_TXD[1]_GPIO[56] is an EBI data signal. The alternate function is FEC transmit data [1].

2.3.2.20 External Data / Ethernet Receive Data / GPIO DATA[29]_FEC_RXD[1]_GPIO[57]

DATA[29]_FEC_RXD[1]_GPIO[57] is an EBI data signal.The alternate function is FEC receive data [1].

2.3.2.21 External Data / Ethernet Receive Data / GPIO DATA[30]_FEC_RXD[2]_GPIO[58]

DATA[30]_FEC_RXD[2]_GPIO[58] is an EBI data signal.The alternate function is FEC receive data [2].

2.3.2.22 External Data / Ethernet Receive Data / GPIO DATA[31]_FEC_RXD[3]_GPIO[59]

DATA[31]_FEC_RXD[3]_GPIO[59] is an EBI data signal.The alternate function is FEC receive data [3].

2.3.2.23 External Master Bus / GPIO TSIZ[0:1]_GPIO[60:61]

TSIZ[0:1]_GPIO[60:61] indicate the size of an external bus transfer when in external master or slave mode operation. The TSIZ[0:1] signals are not driven by the EBI in single master operation.

2.3.2.24 External Read/Write / GPIO RD_$\overline{\text{WR}}$_GPIO[62]

RD_$\overline{\text{WR}}$_GPIO[62] indicates whether an external bus transfer is a read or write operation.

2.3.2.25 External Burst Data In Progress / GPIO $\overline{\text{BDIP}}$_GPIO[63]

$\overline{\text{BDIP}}$_GPIO[63] indicates that an EBI burst transfer is in progress.

2.3.2.26 External Write/Byte Enable / GPIO $\overline{\text{WE}}$/$\overline{\text{BE}}$[0:3]_GPIO[64:67]

$\overline{\text{WE}}$/$\overline{\text{BE}}$[0:3]_GPIO[64:67] specify which data pins contain valid data for an external bus transfer.

2.3.2.27 External Output Enable / GPIO $\overline{\text{OE}}$_GPIO[68]

$\overline{\text{OE}}$_GPIO[68] indicates that the EBI is ready to accept read data.

2.3.2.28 External Transfer Start / GPIO $\overline{\text{TS}}$_GPIO[69]

$\overline{\text{TS}}$_GPIO[69] is asserted by the EBI owner to indicate the start of a transfer.

2.3.2.29 External Transfer Acknowledge / GPIO $\overline{\text{TA}}$_GPIO[70]

$\overline{\text{TA}}$_GPIO[70] is asserted by the EBI owner to acknowledge that the slave has completed the current transfer.

2.3.2.30 External Transfer Error Acknowledge / Ethernet Receive Data / GPIO TEA_FEC_RXD[3]_GPIO[71]

TEA_FEC_RXD[3]_GPIO[71] indicates that an error occurred in the current external bus transfer. The alternate function is FEC receive data [3].

2.3.2.31 External Bus Request / Ethernet Management Clock / GPIO BR_FEC_MDC_GPIO[72]

BR_FEC_MDC_GPIO[72] is the bus request. The alternate function is the Ethernet management clock output, FEC_MDC.

2.3.2.32 External Bus Grant / Ethernet Management Data I/O / GPIO BG_FEC_MDIO_GPIO[73]

BG_FEC_MDIO_GPIO[73] is the bus grant. The secondary function is the Ethernet management data I/O, FEC_MDIO.

2.3.2.33 External Bus Busy / GPIO BB_GPIO[74]

BB_GPIO[74] is the external bus busy.

2.3.3 Nexus Signals

2.3.3.1 Nexus Event In EVTI

EVTI is an input that is read during a debug port reset to enable or disable the Nexus Auxiliary port for data trace. After reset, the EVTI pin is used to initiate program and data trace synchronization messages or generate a breakpoint.

2.3.3.2 Nexus Event Out EVTO

EVTO is an output that provides timing to a development tool for a single watchpoint or breakpoint occurrence.

2.3.3.3 Nexus Message Clock Out MCKO

MCKO is a free running clock output to the development tools which is used for timing of the MDO and MSEO signals.

2.3.3.4 Nexus Message Data Out MDO[0]

MDO[0] is a trace message output to the development tools. In addition, MDO[0] indicates the lock status of the system clock following a power-on reset. MDO[0] is driven high following a power-on-reset until the system clock achieves lock, at which time it is then negated. There is an internal pullup on MDO[0].

2.3.3.5 Nexus Message Data Out MDO[3:1]

MDO[3:1] are the trace message outputs to the development tools.

2.3.3.6 Nexus Message Data Out / GPIO MDO[11:4]_GPIO[82:75]

MDO[11:4]_GPIO[82:75] are the trace message outputs to the development tools for full port mode. These pins function as GPIO when the Nexus port controller (NPC) operates in reduced port mode.

2.3.3.7 Nexus Message Start / End Out $\overline{\text{MSEO}}$[1:0]

$\overline{\text{MSEO}}$[1:0] are output signals that indicate when messages start and end on the MDO pins.

2.3.3.8 Nexus Ready Output $\overline{\text{RDY}}$

$\overline{\text{RDY}}$ is an output signal that indicates to the development tools the data is ready to be read from or written to the Nexus read/write access registers.

2.3.4 JTAG Signals

2.3.4.1 JTAG Test Clock Input TCK

TCK provides the clock input for the on-chip test logic.

2.3.4.2 JTAG Test Data Input TDI

TDI provides the serial test instruction and data input for the on-chip test logic.

2.3.4.3 JTAG Test Data Output TDO

TDO provides the serial test data output for the on-chip test logic.

2.3.4.4 JTAG Test Mode Select Input TMS

TMS controls test mode operations for the on-chip test logic.

2.3.4.5 JTAG Compliance Input JCOMP

The JCOMP pin is used to enable the JTAG TAP controller.

2.3.4.6 Test Mode Enable Input $\overline{\text{TEST}}$

The $\overline{\text{TEST}}$ pin is used to place the chip in test mode. Negate $\overline{\text{TEST}}$ for normal operation.

2.3.5 Controller Area Network (FlexCAN) Signals

2.3.5.1 FlexCAN A Transmit / eSCI A Transmit / GPIO CNTXA_TXDA_GPIO[83]

CNTXA_TXDA_GPIO[83] is the transmit pin for the FlexCAN A module. The alternate function is the transmit pin for the eSCI A module.

2.3.5.2 FlexCAN A Receive / eSCI A Receive / GPIO CNRXA_RXDA_GPIO[84]

CNRXA_RXDA_GPIO[84] is the receive pin for the FlexCAN A module. The alternate function is the receive pin for the eSCI A module.

2.3.5.3 FlexCAN B Transmit / DSPI C / GPIO CNTXB_PCSC[3]_GPIO[85]

CNTXB_PCSC[3]_GPIO[85] is the transmit pin for the FlexCan B module. The alternate function is a peripheral chip select output for the DSPI C module.

2.3.5.4 FlexCAN B Receive / DSPI C / GPIO CNRXB_PCSC[4]_GPIO[86]

CNRXB_PCSC[4]_GPIO[86] is the receive pin for the FlexCan B module. The alternate function is a peripheral chip select output for the DSPI C module.

2.3.5.5 FlexCAN C Transmit / DSPI D / GPIO CNTXC_PCSD[3]_GPIO[87]

CNTXC_PCSD[3]_GPIO[87] is the transmit pin for the FlexCAN C module. The alternate function is PCSD[3], a peripheral chip select for the DSPI D module.

2.3.5.6 FlexCAN A Receive / DSPI D / GPIO CNRXC_PCSD[4]_GPIO[88]

CNRXC_PCSD[4]_GPIO[88] is the receive pin for the FlexCAN C module. The alternate function is PCSD[4], a peripheral chip select for the DSPI D module.

2.3.6 Enhanced Serial Communications Interface (eSCI) Signals

2.3.6.1 eSCI A Transmit / GPIO TXDA_GPIO[89]

TXDA_GPIO[89] is the transmit data pin for the eSCI A module.

2.3.6.2 eSCI A Receive / GPIO RXDA_GPIO[90]

RXDA_GPIO[90] is the receive pin for the eSCI A module. The pin is an input only for the receive data function, but as GPIO the pin is input or output based on the SIU PCR configuration.

2.3.6.3 eSCI B Transmit / DSPI D / GPIO TXDB_PCSD[1]_GPIO[91]

TXDB_PCSD[1]_GPIO[91] is the transmit pin for the eSCI B module. The alternate function is a peripheral chip select output for the DSPI D module.

2.3.6.4 eSCI B Receive / DSPI D / GPIO RXDB_PCSD[5]_GPIO[92]

RXDB_PCSD[5]_GPIO[92] is the transmit pin for the eSCI B module. The secondary function is a peripheral chip select for the DSPI D module.

2.3.7 Deserial/Serial Peripheral Interface (DSPI) Signals

2.3.7.1 DSPI A Clock / DSPI C / GPIO SCKA_PCSC[1]_GPIO[93]

SCKA_PCSC[1]_GPIO[93] — SCKA is the primary function and is the SPI clock pin for the DSPI A module. The alternate signal function is the PCSC[1], a peripheral chip select for the DSPI C module.

2.3.7.2 DSPI A Data Input / DSPI C / GPIO SINA_PCSC[2]_GPIO[94]

SINA_PCSC[2]_GPIO[94] — SINA is the primary function and is the data input pin for the DSPI A module. The alternate signal function is PCSC[2], a peripheral chip select for the DSPI C module.

2.3.7.3 DSPI A Data Output / DSPI C / GPIO SOUTA_PCSC[5]_GPIO[95]

SOUTA_PCSC[5]_GPIO[95] — SOUTA is the primary function and is the data output pin for the DSPI A module. The alternate function is PCSC[5], a peripheral chip select for the DSPI C module and is available on this device.

2.3.7.4 DSPI A /DSPI D / GPIO PCSA[0]_PCSD[2]_GPIO[96]

PCSA[0]_PCSD[2]_GPIO[96] — The PCSA[0] primary function is a peripheral chip select output pin for the DSPI A module. In slave mode, PCSA[0] also serves as the slave select input (SS) of the DSPI A module. The alternate function is PCSD[2], a peripheral chip select for the DSPI D module.

2.3.7.5 DSPI A / DSPI B / GPIO PCSA[1]_PCSB[2]_GPIO[97]

PCSA[1]_PCSB[2]_GPIO[97] — The PCSA[1] primary function is a peripheral chip select output pin for the DSPI A module. The alternate function is PCSB[2], a peripheral chip select for the DSPI B module.

2.3.7.6 DSPI A /DSPI D Clock / GPIO PCSA[2]_SCKD_GPIO[98]

PCSA[2]_SCKD_GPIO[98] — The PCSA[2] is the primary function and is a peripheral chip select output pin for the DSPI A module. The alternate function is SCKD, a DSPI clock pin for the DSPI D module.

2.3.7.7 DSPI A /DSPI D Data Input / GPIO PCSA[3]_SIND_GPIO[99]

PCSA[3]_SIND_GPIO[99] — The PCSA[3] is the primary function and is a peripheral chip select output pin for the DSPI A module. The alternate function is SIND, a data input pin for the DSPI D module.

2.3.7.8 DSPI A / DSPI D Data Output / GPIO PCSA[4]_SOUTD_GPIO[100]

PCSA[4]_SOUTD_GPIO[100] — The PCSA[4] is the primary function and is a peripheral chip select output pin for the DSPI A module. The alternate function is SOUTD, a data output pin for the DSPI D module.

2.3.7.9 DSPI A / DSPI B / GPIO PCSA[5]_PCSB[3]_GPIO[101]

PCSA[5]_PCSB[3]_GPIO[101] — The PCSA[5] is the primary function and is a peripheral chip select output pin for the DSPI A module. The alternate function is PCSB[3], a peripheral chip select output pin for the DSPI B module.

2.3.7.10 DSPI B Clock / DSPI C / GPIO SCKB_PCSC[1]_GPIO[102]

SCKB_PCSC[1]_GPIO[102] — SCKB is the primary function, and is the SPI clock pin for the DSPI B module. The alternate function is PCSC[1], a chip select output for the DSPI C module.

2.3.7.11 DSPI B Data Input / DSPI C / GPIO SINB_PCSC[2]_GPIO[103]

SINB_PCSC[2]_GPIO[103] — SINB is the primary function and is the data input pin for the DSPI B module. The alternate function is a chip select output for the DSPI C module.

2.3.7.12 DSPI B Data Output / DSPI C / GPIO SOUTB_PCSC[5]_GPIO[104]

SOUTB_PCSC[5]_GPIO[104] — SOUTB is the primary function and is the data output pin for the DSPI B module. The alternate function is a chip select output for the DSPI C module.

2.3.7.13 DSPI B / DSPI D / GPIO PCSB[0]_PCSD[2]_GPIO[105]

PCSB[0]_PCSD[2]_GPIO[105] — PCSB[0] is the primary function and is a DSPI B peripheral chip select output pin. It also is a Slave Select ($\overline{SS}$) input pin for the DSPI B module slave mode operation. The alternate function is PCSD[2] and is a chip select output for the DSPI D module.

2.3.7.14 DSPI B / DSPI D / GPIO PCSB[1]_PCSD[0]_GPIO[106]

PCSB[1]_PCSD[0]_GPIO[106] — PCSB[1] is the primary a peripheral chip select output pin for the DSPI B module. The alternate function is PCSD[0] and is a DSPI D peripheral chip select output, that also can be used as a Slave Select ($\overline{SS}$) input pin for DSPI D module slave mode operation.

2.3.7.15 DSPI B / DSPI C Data Output / GPIO PCSB[2]_SOUTC_GPIO[107]

PCSB[2]_SOUTC_GPIO[107] — PCSB[2] is the primary function and is a peripheral chip select output pin for the DSPI B module. SOUTC is the alternate function and is the data output for the DSPI C module.

2.3.7.16 DSPI B / DSPI C Data Input / GPIO PCSB[3]_SINC_GPIO[108]

PCSB[3]_SINC_GPIO[108] — PCSB[3] is the primary function and is a peripheral chip select output pin for the DSPI B module. SINC is the alternate function and is the data input for the DSPI C module.

2.3.7.17 DSPI B / DSPI C Clock / GPIO PCSB[4]_SCKC_GPIO[109]

PCSB[4]_SCKC_GPIO[109] — PCSB[4] is the primary function and is a peripheral chip select output pin for the DSPI B module. SCKC is the alternate function and is the SPI clock for the DSPI C module.

2.3.7.18 DSPI B / DSPI C / GPIO PCSB[5]_PCSC[0]_GPIO[110]

PCSB[5]_PCSC[0]_GPIO[110] — PCSB[5] is the primary function and is a peripheral chip select output pin for the DSPI B module. PCSC[0] is the alternate function and is a DSPI C peripheral chip select output, but can also be used as a Slave Select ($\overline{SS}$) input pin for DSPI C module slave mode operation.

2.3.8 Enhanced Queued A/D Controller (eQADC) Signals

2.3.8.1 Analog Input / Differential Analog Input AN[0]_DAN0+

AN[0] is a single-ended analog input to the two on-chip ADCs. DAN0+ is the positive terminal of the differential analog input DAN0 (DAN0+ to DAN0–).

2.3.8.2 Analog Input / Differential Analog Input AN[1]_DAN0–

AN[1] is a single-ended analog input to the two on-chip ADCs. DAN0– is the negative terminal of the differential analog input DAN0 (DAN0+ to DAN0–).

2.3.8.3 Analog Input / Differential Analog Input AN[2]_DAN1+

AN[2] is a single-ended analog input to the two on-chip ADCs. DAN1+ is the positive terminal of the differential analog input DAN1 (DAN1+ to DAN1–).

2.3.8.4 Analog Input / Differential Analog Input AN[3]_DAN1–

AN[3] is a single-ended analog input to the two on-chip ADCs. DAN1– is the negative terminal of the differential analog input DAN1 (DAN1+ to DAN1–).

2.3.8.5 Analog Input / Differential Analog Input AN[4]_DAN2+

AN[4] is a single-ended analog input to the two on-chip ADCs. DAN2+ is the positive terminal of the differential analog input DAN2 (DAN2+ to DAN2–).

2.3.8.6 Analog Input / Differential Analog Input AN[5]_DAN2–

AN[5] is a single-ended analog input to the two on-chip ADCs. DAN2– is the negative terminal of the differential analog input DAN2 (DAN2+ to DAN2–).

2.3.8.7 Analog Input / Differential Analog Input AN[6]_DAN3+

AN[6] is a single-ended analog input to the two on-chip ADCs. DAN3+ is the positive terminal of the differential analog input DAN3 (DAN3+ to DAN3–).

2.3.8.8 Analog Input / Differential Analog Input AN[7]_DAN3–

AN[7] is a single-ended analog input to the two on-chip ADCs. DAN3– is the negative terminal of the differential analog input DAN3 (DAN3+ to DAN3–).

2.3.8.9 Analog Input / Multiplexed Analog Input AN[8]_ANW

AN[8] is an analog input pin. ANW is an analog input in external multiplexed mode.

2.3.8.10 Analog Input / Multiplexed Analog Input AN[9]_ANX

AN[9] is an analog input pin. ANX is an analog input in external multiplexed mode.

2.3.8.11 Analog Input / Multiplexed Analog Input AN[10]_ANY

AN[10] is an analog input pin. ANY is an analog input in external multiplexed mode.

2.3.8.12 Analog Input / Multiplexed Analog Input AN[11]_ANZ

AN[11] is an analog input pin. ANZ is an analog input in external multiplexed mode.

NOTE

Attempts to convert the input voltage applied to AN[12], AN[13], AN[14], and AN[15] while a non-eQADC function is selected causes an undefined conversion result.

2.3.8.13 Analog Input / Mux Address 0 / eQADC Serial Data Strobe AN[12]_MA[0]_SDS

AN[12]_MA[0]_SDS is an analog input pin. The alternate function, MA[0], is a MUX address pin. SDS is the serial data strobe for the eQADC SSI; this function is selected by setting the PA field of SIU_PCR215 to GPIO. This pin has reduced analog to digital conversion accuracy as compared to the AN[0:7] and AN[16:39] analog input pins because they are powered by V_{DDEH9} and can be used as digital pins for the synchronous serial interface (SSI) to external ADCs or used as the multiplexor digital outputs (MA[0]).

SDS is the serial data select output that is muxed with AN[12] and MA[0]. It indicates to the external (slave) device when it can latch incoming serial data, when it can output its own serial data, and when it must abort a data transmission. SDS corresponds to the chip select signal in a conventional SPI interface.

This pin is configured by setting the pad configuration register, SIU_PCR215.

2.3.8.14 Analog Input / Mux Address 1 / eQADC Serial Data Out AN[13]_MA[1]_SDO

AN[13]_MA[1]_SDO is an analog input pin. The alternate function, MA[1], is a MUX address pin. SDO is the serial data output for the eQADC SSI; this function is selected by setting the PA field of SIU_PCR216 to GPIO. This pin has reduced analog to digital conversion accuracy as compared to the AN[0:7] and AN[16:39] analog input pins because they are powered by V_{DDEH9} and can be used as digital pins for the synchronous serial interface (SSI) to external ADCs or used as the multiplexor digital outputs (MA[1]).

This pin is configured by setting the pad configuration register, SIU_PCR216.

2.3.8.15 Analog Input / Mux Address 2 / eQADC Serial Data In AN[14]_MA[2]_SDI

AN[14]_MA[2]_SDI is an analog input pin. The alternate function, MA[2], is a MUX address pin. SDI is the serial data input for the eQADC SSI; this function is selected by setting the PA field of SIU_PCR217 to GPIO. This pin has reduced analog to digital conversion accuracy as compared to the AN[0:7] and AN[16:39] analog input pins because they are powered by V_{DDEH9} and can be used as digital pins for the synchronous serial interface (SSI) to external ADCs or used as the multiplexor digital outputs (MA[2]).

This pin is configured by setting the pad configuration register, SIU_PCR217.

2.3.8.16 Analog Input / eQADC Free Running Clock AN[15]_FCK

AN[15]_FCK is an analog input pin. The alternate function is the free running clock for the eQADC SSI. This pin has reduced analog to digital conversion accuracy as compared to the AN[0:7] and AN[16:39] analog input pins.

This pin is configured by setting the pad configuration register, SIU_PCR218.

2.3.8.17 Analog Input AN[16:39]

AN[16:39] are analog input pins.

2.3.8.18 External Trigger / GPIO ETRIG[0:1]_GPIO[111:112]

External trigger signals trigger a software or hardware event. The eQADC can detect rising edge, falling edge, high level, and low level on each of the external trigger signals. The eQADC also supports configurable digital filters for these external trigger signals. The eQADC external trigger input pins can be connected to the eTPU, the eMIOS, or an external signal. The source is selected by configuring the eQADC trigger source in the SIU_ETISR register.

ETRIG[0] is the external trigger for CFIFO0, CFIFO2, and CFIFO4; ETRIG[1] serves as the external trigger for CFIFO1, CFIFO3, and CFIFO5.

GPIO[111:112] are general purpose input/output functions.

2.3.8.19 Voltage Reference High V_{RH}

V_{RH} is the voltage reference high input pin for the eQADC.

2.3.8.20 Voltage Reference Low V_{RL}

V_{RL} is the voltage reference low input pin for the eQADC.

2.3.8.21 Reference Bypass Capacitor REFBYPC

REFBYPC is a bypass capacitor input for the eQADC. The REFBYPC pin is used to connect an external bias capacitor between the REFBYPC pin and V_{RL}. The value of this capacitor must be 100nF. This bypass capacitor is used to provide a stable reference voltage for the ADC.

2.3.9 Enhanced Time Processing Unit (eTPU) Signals

2.3.9.1 eTPU A TCR Clock / External Interrupt Request / GPIO TCRCLKA_$\overline{\text{IRQ}}$[7]_GPIO[113]

TCRCLKA_$\overline{\text{IRQ}}$[7]_GPIO[113] is the TCR clock input for the eTPU A module. The alternate function is an external interrupt request input for the SIU module.

2.3.9.2 eTPU A Channel / eTPU A Output Channel / GPIO ETPUA[0]_ETPUA[12]_GPIO[114]

ETPUA[0]_ETPUA[12]_GPIO[114] is an input/output channel pin for the eTPU A module. ETPUA[0] is the primary function and is an input/output channel for the eTPU A module. The alternate function, ETPUA[12], is an output channel for the eTPU A module. When configured as ETPUA[12], the pin functions as output only. ETPUA[12] is an alternate function and is only for eTPU A module output channels.

2.3.9.3 eTPU A Channel / eTPU A Output Channel / GPIO ETPUA[1]_ETPUA[13]_GPIO[115]

ETPUA[1]_ETPUA[13]_GPIO[115] is an input/output channel pin for the eTPU A module. ETPUA[1] is the primary function and is an input/output channel for the eTPU A module. The alternate function, ETPUA[13], is an output channel for the eTPU A module. When configured as ETPUA[13], the pin functions as output only.

2.3.9.4 eTPU A Channel / eTPU A Output Channel / GPIO ETPUA[2]_ETPUA[14]_GPIO[116]

ETPUA[2]_ETPUA[14]_GPIO[116] is an input/output channel pin for the eTPU A module. ETPUA[2] is the primary function and is an input/output channel for the eTPU A module. The alternate function is an output channel for the eTPU A module. When configured as ETPUA[14], the pin functions as output only.

2.3.9.5 eTPU A Channel / eTPU A Output Channel / GPIO ETPUA[3]_ETPUA[15]_GPIO[117]

ETPUA[3]_ETPUA[15]_GPIO[117] is an input/output channel pin for the eTPU A module. ETPUA[3] is the primary function and is an input/output channel for the eTPU A module. The alternate function is an output channel for the eTPU A module. When configured as ETPUA[15], the pin functions as output only.

2.3.9.6 eTPU A Channel / eTPU A Output Channel / GPIO ETPUA[4]_ETPUA[16]_GPIO[118]

ETPUA[4]_ETPUA[16]_GPIO[118] is an input/output channel pin for the eTPU A module. The alternate function, ETPUA[16], is an output channel for the eTPU A module. When configured as ETPUA[16], the pin functions as output only.

2.3.9.7 eTPU A Channel / eTPU A Output Channel / GPIO ETPUA[5]_ETPUA[17]_GPIO[119]

ETPUA[5]_ETPUA[17]_GPIO[119] is an input/output channel pin for the eTPU A module. The alternate function, ETPUA[17], is an output channel for the eTPU A module. When configured as ETPUA[17], the pin functions as output only.

2.3.9.8 eTPU A Channel / eTPU A Output Channel / GPIO ETPUA[6]_ETPUA[18]_GPIO[120]

ETPUA[6]_ETPUA[18]_GPIO[120] is an input/output channel pin for the eTPU A module. The alternate function, ETPUA[18], is an output channel for the eTPU A module. When configured as ETPUA[18], the pin functions as output only.

2.3.9.9 eTPU A Channel / eTPU A Output Channel / GPIO ETPUA[7]_ETPUA[19]_GPIO[121]

ETPUA[7]_ETPUA[19]_GPIO[121] is an input/output channel pin for the eTPU A module. The alternate function, ETPUA[19], is an output channel for the eTPU A module. When configured as ETPUA[19], the pin functions as output only.

2.3.9.10 eTPU A Channel / eTPU A Output Channel / GPIO ETPUA[8]_ETPUA[20]_GPIO[122]

ETPUA[8]_ETPUA[20]_GPIO[122] is an input/output channel pin for the eTPU A module. The alternate function, ETPUA[20], is an output channel for the eTPU A module. When configured as ETPUA[20], the pin functions as output only.

2.3.9.11 eTPU A Channel / eTPU A Output Channel / GPIO ETPUA[9]_ETPUA[21]_GPIO[123]

ETPUA[9]_ETPUA[21]_GPIO[123] is an input/output channel pin for the eTPU A module. The alternate function, ETPUA[21], is an output channel for the eTPU A module. When configured as ETPUA[21], the pin functions as output only.

2.3.9.12 eTPU A Channel / eTPU A Output Channel / GPIO ETPUA[10]_ETPUA[22]_GPIO[124]

ETPUA[10]_ETPUA[22]_GPIO[124] is an input/output channel pin for the eTPU A module. The alternate function, ETPUA[22], is an output channel for the eTPU A module. When configured as ETPUA[22], the pin functions as output only.

2.3.9.13 eTPU A Channel / eTPU A Output Channel / GPIO ETPUA[11]_ETPUA[23]_GPIO[125]

ETPUA[11]_ETPUA[23]_GPIO[125] is an input/output channel pin for the eTPU A module. The alternate function, ETPUA[23], is an output channel for the eTPU A module. When configured as ETPUA[23], the pin functions as output only.

2.3.9.14 eTPU A Channel / DSPI B / GPIO ETPUA[12]_PCSB[1]_GPIO[126]

ETPUA[12]_PCSB[1]_GPIO[126] is an input/output channel pin for the eTPU A module. The alternate function is a peripheral chip select for the DSPI B module.

2.3.9.15 eTPU A Channel / DSPI B / GPIO ETPUA[13]_PCSB[3]_GPIO[127]

ETPUA[13]_PCSB[3]_GPIO[127] is an input/output channel pin for the eTPU A module. The alternate function is a peripheral chip select for the DSPI B module.

2.3.9.16 eTPU A Channel / DSPI B / GPIO ETPUA[14]_PCSB[4]_GPIO[128]

ETPUA[14]_PCSB[4]_GPIO[128] is an input/output channel pin for the eTPU A module. The alternate function is a peripheral chip select for the DSPI B module.

2.3.9.17 eTPU A Channel / DSPI B / GPIO ETPUA[15]_PCSB[5]_GPIO[129]

ETPUA[15]_PCSB[5]_GPIO[129] is an input/output channel pin for the eTPU A module. The alternate function is a peripheral chip select for the DSPI B module.

2.3.9.18 eTPU A Channel / DSPI D / GPIO ETPUA[16]_PCSD[1]_GPIO[130]

ETPUA[16]_PCSD[1]_GPIO[130] is an input/output channel pin for the eTPU A module. The alternate function is a peripheral chip select for the DSPI D module.

2.3.9.19 eTPU A Channel / DSPI D / GPIO ETPUA[17]_PCSD[2]_GPIO[131]

ETPUA[17]_PCSD[2]_GPIO[131] is an input/output channel pin for the eTPU A module. The alternate function is a peripheral chip select for the DSPI D module.

2.3.9.20 eTPU A Channel / DSPI D / GPIO ETPUA[18]_PCSD[3]_GPIO[132]

ETPUA[18]_PCSD[3]_GPIO[132] is an input/output channel pin for the eTPU A module. The alternate function is a peripheral chip select for the DSPI D module.

2.3.9.21 eTPU A Channel / DSPI D / GPIO ETPUA[19]_PCSD[4]_GPIO[133]

ETPUA[19]_PCSD[4]_GPIO[133] is an input/output channel pin for the eTPU A module. The alternate function is a peripheral chip select for the DSPI D module.

2.3.9.22 eTPU A Channel / External Interrupt / GPIO ETPUA[20]_$\overline{\text{IRQ}}$[8]_GPIO[134]

ETPUA[20]_$\overline{\text{IRQ}}$[8]_GPIO[134] is an input/output channel pin for the eTPU A module. The alternate function is an external interrupt request input for the SIU module.

2.3.9.23 eTPU A Channel / External Interrupt / GPIO ETPUA[21]_IRQ[9]_GPIO[135]

ETPUA[21]_IRQ[9]_GPIO[135] is an input/output channel pin for the eTPU A module. The alternate function is an external interrupt request input for the SIU module.

2.3.9.24 eTPU A Channel / External Interrupt / GPIO ETPUA[22]_IRQ[10]_GPIO[136]

ETPUA[22]_IRQ[10]_GPIO[136] is an input/output channel pin for the eTPU A module. The alternate function is an external interrupt request input for the SIU module.

2.3.9.25 eTPU A Channel / External Interrupt / GPIO ETPUA[23]_IRQ[11]_GPIO[137]

ETPUA[23]_IRQ[11]_GPIO[137] is an input/output channel pin for the eTPU A module. The alternate function is an external interrupt request input for the SIU module.

2.3.9.26 eTPU A Output Channel / External Interrupt / GPIO ETPUA[24:27]_IRQ[12:15]_GPIO[138:141]

ETPUA[24:27]_IRQ[12:15]_GPIO[138:141] are output channel pins for the eTPU A module. The alternate functions are external interrupt request inputs for the SIU module.

2.3.9.27 eTPU A Output Channel / DSPI C / GPIO ETPUA[28]_PCSC[1]_GPIO[142]

ETPUA[28]_PCSC[1]_GPIO[142] is an output channel pin for the eTPU A module. The alternate function is a peripheral chip select for the DSPI C module.

2.3.9.28 eTPU A Output Channel / DSPI C / GPIO ETPUA[29]_PCSC[2]_GPIO[143]

ETPUA[29]_PCSC[2]_GPIO[143] is an output channel pin for the eTPU A module. The alternate function is a peripheral chip select for the DSPI C module.

2.3.9.29 eTPU A Channel / DSPI C / GPIO ETPUA[30]_PCSC[3]_GPIO[144]

ETPUA[30]_PCSC[3]_GPIO[144] is an input/output channel pin for the eTPU A module. The alternate function is a peripheral chip select for the DSPI C module.

2.3.9.30 eTPU A Channel / DSPI C / GPIO ETPUA[31]_PCSC[4]_GPIO[145]

ETPUA[31]_PCSC[4]_GPIO[145] is an input/output channel pin for the eTPU A module. The alternate function is a peripheral chip select for the DSPI C module.

2.3.9.31 eTPU B TCR Clock / External Interrupt Request / GPIO TCRCLKB_IRQ[6]_GPIO[146]

TCRCLKB_IRQ[6]_GPIO[146] is the TCR B clock input for the eTPU module. The alternate function is an external interrupt request input for the SIU module.

2.3.9.32 eTPU B Channel / eTPU B Output Channel / GPIO ETPUB[0:15]_ETPUB[16:31]_GPIO[147:162]

ETPUB[0:15]_ETPUB[16:31]_GPIO[147:162] are 16 input/output channel pins for the eTPU B module. The alternate functions are output channels for the eTPU B module; that is, when configured as ETPUB[16:31], the pins function as outputs only.

2.3.9.33 eTPU B Channel / DSPI A / GPIO ETPUB[16:19]_PCSA[1:4]_GPIO[163:166]

ETPUB[16:19]_PCSA[1:4]_GPIO[163:166] are input/output channel pins for the eTPU B module. The alternate functions are peripheral chip select signals for DSPI A.

2.3.9.34 eTPU B Channel / GPIO ETPUB[20:31]_GPIO[167:178]

ETPUB[20:31]_GPIO[167:178] are input/output channel pins for the eTPU B module.

2.3.10 Enhanced Management Input/Output System (eMIOS) Signals

2.3.10.1 eMIOS Channel / eTPU A Output Channel / GPIO EMIOS[0:9]_ETPUA[0:9]_GPIO[179:188]

EMIOS[0:9]_ETPUA[0:9]_GPIO[179:188] is an input/output channel pin for the eMIOS module. The alternate functions are output channels for the eTPU A module; that is, when configured as ETPUA[0:9], the pins function as outputs only.

2.3.10.2 eMIOS Channel / DSPI D / GPIO EMIOS[10:11]_PCSD[3:4]_GPIO[189:190]

EMIOS[10:11]_PCSD[3:4]_GPIO[189:190] is an input/output channel pin for the eMIOS module. The alternate functions are PCSD[3:4] and are peripheral chip selects for the DSPI D module.

2.3.10.3 eMIOS Output Channel / DSPI C / GPIO EMIOS[12]_SOUTC_GPIO[191]

EMIOS[12]_SOUTC_GPIO[191] is an output channel pin for the eMIOS module. The alternate function is the data output signal for the DSPI C module.

2.3.10.4 eMIOS Output Channel / DSPI D / GPIO EMIOS[13]_SOUTD_GPIO[192]

EMIOS[13]_SOUTD_GPIO[192] is an output channel pin for the eMIOS module. The alternate function is the data output signal for the DSPI D module.

2.3.10.5 eMIOS Output Channel / External Interrupt Request / FlexCAN Transmit Data / GPIO EMIOS[14]_$\overline{\text{IRQ}}$[0]_CNTXD_GPIO[193]

EMIOS[14]_$\overline{\text{IRQ}}$[0]_CNTXD_GPIO[193] is an output channel pin for the eMIOS module. The alternate function is an external interrupt request input and the second alternate function is the FlexCAN transmit data signal.

2.3.10.6 eMIOS Output Channel / External Interrupt Request / FlexCAN Receive Data / GPIO EMIOS[15]_$\overline{\text{IRQ}}$[1]_CNRXD_GPIO[194]

EMIOS[15]_$\overline{\text{IRQ}}$[1]_CNRXD_GPIO[194] is an output channel pin for the eMIOS module. The alternate function is an external interrupt request input and the secondary alternate function is the FlexCAN receive data.

2.3.10.7 eMIOS Channel / eTPU B Output Channel / GPIO EMIOS[16]_ETPUB[0]_GPIO[195]

EMIOS[16]_ETPUB[0]_GPIO[195] is an input/output channel pin for the eMIOS module. The alternate function is an ETPUB (output only).

2.3.10.8 eMIOS Channel / eTPU B Output Channel / GPIO EMIOS[17]_ETPUB[1]_GPIO[196]

EMIOS[17]_ETPUB[1]_GPIO[196] is an input/output channel pin for the eMIOS module. The alternate function is an ETPU B output channel.

2.3.10.9 eMIOS Channel / eTPU B Output Channel / GPIO EMIOS[18]_ETPUB[2]_GPIO[197]

EMIOS[18]_ETPUB[2]_GPIO[197] is an input/output channel pin for the eMIOS module. The alternate function is ETPU B (output only).

2.3.10.10 eMIOS Channel / eTPU B Output Channel / GPIO EMIOS[19]_ETPUB[3]_GPIO[198]

EMIOS[19]_ETPUB[3]_GPIO[198] is an input/output channel pin for the eMIOS module. The alternate function is an ETPU B output channel.

2.3.10.11 eMIOS Channel /eTPU B Output Channel / GPIO EMIOS[20:21]_ETPUB[4:5]_GPIO[199:200]

EMIOS[20:21]_ETPUB[4:5]_GPIO[199:200] is an input/output channel pin for the eMIOS module.

2.3.10.12 eMIOS Channel / eTPU B Output Channel / GPIO EMIOS[22]_ETPUB[6]_GPIO[201]

EMIOS[22]_ETPUB[6]_GPIO[201] is an input/output channel pin for the eMIOS module. The alternate function is ETPU B output channel.

2.3.10.13 eMIOS Channel / eTPU B Output Channel / GPIO EMIOS[23]_ETPUB[7]_GPIO[202]

EMIOS[23]_ETPUB[7]_GPIO[202] is an input/output channel pin for the eMIOS module.The alternate function is an ETPU B output channel.

2.3.11 General Purpose Input/Output (GPIO) Signals

2.3.11.1 eMIOS Output Channel / GPIO EMIOS[14:15]_GPIO[203:204]

The EMIOS[14:15]_GPIO[203:204] pins' primary function is EMIOS[14:15]. When configured as EMIOS[14:15], the pins function as output channels for the eMIOS module. Because other balls on the BGA map are already named EMIOS[14:15], the ball names on the BGA map for these signals are named GPIO[203:204]. The general purpose I/O function for these pins is GPIO.

2.3.11.2 General Purpose Input Output GPIO[205]

The GPIO[205] only has GPIO functionality. This pin is reserved for double data rate memory interface support. The pad type for GPIO[205] is MH (3.0–5.5 V).

2.3.11.3 General Purpose Input Output GPIO[206:207]

GPIO[206:207] have GPIO functionality. The GPIO pins are reserved for double data rate memory (DDRAM) interface support. The pad types for GPIO[206:207] is F (1.62–3.6 V).

Read Section 6.3.1.115, "Pad Configuration Registers 206–207 (SIU_PCR206–SIU_PCR207)."

The GPIO[206:207] pins can be selected as sources for the ADC trigger in the SIU_ETISR.

2.3.12 Calibration Bus Signals

Calibration signals function only when using the 496 pin assembly.

2.3.12.1 Calibration Chip Select 0 / GPIO CAL_$\overline{CS}$[0]

CAL_$\overline{CS}$[0] is the primary function and selects the primary chip for calibration.

2.3.12.2 Calibration Chip Select / Calibration Address CAL_$\overline{CS}$[1:3]_CAL_ADDR[9:11]

CAL_$\overline{CS}$[1:3] are the primary functions that select the primary chip for calibration. The alternate functions are calibration address signals. These signals are functional only when using the 496 pin assembly.

2.3.12.3 Calibration Address CAL_ADDR[12:30]

CAL_ADDR[12:30] are the calibration addresses. They are functional only when using the 496 pin assembly.

2.3.12.4 Calibration Data CAL_DATA[0:15]

CAL_DATA[0:15] is the primary function and is a calibration address. It is functional only when using the 496 pin assembly.

2.3.12.5 Calibration Read/Write CAL_RD_$\overline{WR}$

CAL_RD_$\overline{WR}$ is the primary function and is a calibration read/write signal function. It is functional only when using the 496 pin assembly.

2.3.12.6 Calibration Write/Byte Enable CAL_$\overline{WE}$/$\overline{BE}$[0:1]

CAL_$\overline{WE}$/$\overline{BE}$[0:1] is the primary function and is a calibration write enable and byte enable. It is functional only when using the 496 pin assembly.

2.3.12.7 Calibration Output Enable CAL_$\overline{OE}$

CAL_$\overline{OE}$ is the primary function and is a calibration output enable. It is functional only when using the 496 pin assembly.

2.3.12.8 Calibration Transfer Start CAL_$\overline{TS}$

CAL_$\overline{TS}$ is the primary function and is a calibration transfer start. It is functional only when using the 496 pin assembly.

2.3.13 Clock Synthesizer Signals

2.3.13.1 Crystal Oscillator Output XTAL

XTAL is the output pin for an external crystal oscillator.

2.3.13.2 Crystal Oscillator Input / External Clock Input EXTAL_EXTCLK

EXTAL is the input pin for an external crystal oscillator or an external clock source. The alternate function is the external clock input. The function of this pin is determined by the PLLCFG configuration pins.

2.3.13.3 System Clock Output CLKOUT

CLKOUT is the device system clock output.

2.3.13.4 Engineering Clock Output ENGCLK

ENGCLK is a 50% duty cycle output clock with a maximum frequency of the device system clock divided by two. ENGCLK is not synchronous to CLKOUT.

2.3.14 Power and Ground Signals

2.3.14.1 Voltage Regulator Control Supply Input V_{RC33}

V_{RC33} is the 3.3 V supply input pin for the on-chip 1.5 V regulator control circuit.

2.3.14.2 Voltage Regulator Control Ground Input V_{RCVSS}

V_{RCVSS} is the ground reference for the on-chip 1.5 V regulator control circuit.

2.3.14.3 Voltage Regulator Control Output V_{RCCTL}

V_{RCCTL} is the output pin for the on-chip 1.5 V regulator control circuit.

2.3.14.4 eQADC Analog Supply V_{DDAn}

V_{DDAn} is the analog supply input pin for the eQADC.

2.3.14.5 eQADC Analog Ground Reference V_{SSAn}

V_{SSAn} is the analog ground reference input pin for the eQADC.

2.3.14.6 Clock Synthesizer Power Input V_{DDSYN}

V_{DDSYN} is the power supply input for the FMPLL.

2.3.14.7 Clock Synthesizer Ground Input V_{SSSYN}

V_{SSSYN} is the ground reference input for the FMPLL.

2.3.14.8 Flash Read Supply Input V_{FLASH}

V_{FLASH} is the on-chip Flash read supply input.

2.3.14.9 Flash Program/Erase Supply Input V_{PP}

V_{PP} is the on-chip flash program and erase supply input.

2.3.14.10 SRAM Standby Power Input V_{STBY}

V_{STBY} is the power supply input that is used to maintain a portion of the contents of internal SRAM during power down. If not used, tie V_{STBY} to V_{SS}.

2.3.14.11 Internal Logic Supply Input V_{DD}

V_{DD} is the 1.5 V logic supply input.

2.3.14.12 External I/O Supply Input V_{DDEn}

V_{DDEn} is the 1.8–3.3 V, with a tolerance of ±10% external I/O supply input.

2.3.14.13 External I/O Supply Input V_{DDEHn}

V_{DDEHn} is the 3.3–5.0 V, with a tolerance of –10% to +5% external I/O supply input.

2.3.14.14 Fixed 3.3 V Internal Supply Input V_{DD33}

V_{DD33} is the 3.3 V internal supply input.

2.3.14.15 Ground V_{SS}

V_{SS} is the ground reference input.

2.3.15 I/O Power and Ground Segmentation

Table 2-3 gives the power/ground segmentation. Each segment provides the power and ground for the I/O pins and can be powered by any voltage within the allowed voltage range regardless of the power on the other segments. The power/ground segmentation applies regardless of whether a particular pin is configured for its primary function or GPIO.

Table 2-2. MPC5566 Device Power/Ground Segmentation

Power Segment	Voltage Range[1]	I/O Pins Powered by Segment
V_{DDA0}	5.0 V	AN[21:35], REFBYPC, V_{RH}
V_{DDA1}	5.0 V	AN[0:11], AN[16:20], AN[36:39]
V_{DDE2}	1.8–3.3 V	ADDR[8:31], $\overline{BDIP}$, $\overline{CS}$[0:3], RD_$\overline{WR}$, $\overline{TA}$, $\overline{TEA}$, $\overline{TS}$, $\overline{WE}$/$\overline{BE}$[0:3]
V_{DDE3}	—	$\overline{BB}$, $\overline{BG}$, $\overline{BR}$, DATA[0:31], GPIO[206:207], $\overline{OE}$
V_{DDE5}	1.8–3.3 V	CLKOUT, ENGCLK
V_{DDE7}	1.8–3.3 V	$\overline{EVTI}$, $\overline{EVTO}$, JCOMP, MCKO, MDO[0:11], $\overline{MSEO}$[0:1], $\overline{RDY}$, TCK, TDI, TDO, $\overline{TEST}$, TMS
V_{DDE12}	—	CAL_ADDR[12:30], CAL_$\overline{CS}$[0], CAL_$\overline{CS}$[1:3], CAL_DATA[0:15], CAL_$\overline{OE}$, CAL_RD_$\overline{WR}$, CAL_$\overline{TS}$, CAL_$\overline{WE}$[0:1]
V_{DDEH1}	3.3–5.0 V	ETPUA[0:31], TCRCLKA
V_{DDEH4}	3.3–5.0 V	CNRXA, CNRXB, CNTXA, CNTXB, EMIOS[0:23]
V_{DDEH6}	3.3–5.0 V	BOOTCFG[0:1], CNRXC, CNTXC, PCSA[0:5], PCSB[3:5], PLLCFG[0:1], $\overline{RESET}$, $\overline{RSTCFG}$, $\overline{RSTOUT}$, RXDA, RXDB, SINA, SCKA, SOUTA, TXDA, TXDB, WKPCFG
V_{DDEH8}	3.3–5.0 V	ETRIG[0:1], GPIO[205]
V_{DDEH9}	3.3–5.0 V	AN[12:15]
V_{DDEH10}	3.3–5.0 V	PCSB[0:2], SCKB, SINB, SOUTB
V_{DDSYN}	3.3 V	EXTAL, XTAL
V_{SSA0}	GND	VRL
V_{DD}	1.5 V	

Table 2-2. MPC5566 Device Power/Ground Segmentation (continued)

Power Segment	Voltage Range[1]	I/O Pins Powered by Segment
V_{DD33}	3.3 V	
V_{FLASH}	3.3 V	
V_{RC33}	3.3 V	
V_{RCCTL}	3.3 V	
V_{RCVSS}	3.3 V	
V_{PP}[2]	5.0 V	
V_{DDE}	1.8–3.3 V	
V_{DDEH}	3.3–5.0 V	
V_{STBY}	0.8–1.2 V	
V_{SSA1}	GND	
V_{SSSYN}	—	
V_{SS}	GND REF	V_{SS}
NC	—	

1 These are nominal voltages. V_{DDE} is 1.62–3.6 V; V_{DDEH} is 3.0–5.5 V. All V_{DDE} voltages are ± 10%; V_{DDEH} voltages are +5% to –10%. V_{RC33} is ± 10%; V_{DDSYN} is ± 10%; V_{DDA1} voltages are +5% to –10%.

2 During read operations, VPP can be as high as 5.3 V and as low as 3.0 V.

Table 2-3. MPC5566 Device Power/Ground Segmentation for the 496 Pin Assembly

Power Segment	Voltage Range [1]	I/O Pins Powered by Segment
V_{DDA0}	5.0 V	AN[22:35]
V_{DDA1}	5.0 V	AN[0]_DAN0+, AN[1]_DAN0-, AN[2]_DAN1+, AN[3]_DAN1-, AN[4]_DAN2+, AN[5]_DAN2-, AN[6]_DAN3+, AN[7]_DAN3-, AN[8]_ANW, AN[9]_ANX, AN[10]_ANY, AN[11]_ANZ, AN[16:21], AN[36:39]
V_{SSA0}	GND	V_{SSA0}
V_{SSA1}	GND	V_{SSA1}
V_{DDE2}	1.8–3.3 V	$\overline{CS}$[0], $\overline{CS}$[1:3]_ADDR[9:11]_GPIO[1:3], ADDR[8:29]_GPIO[4:25], ADDR[30:31]_ADDR[6:7]_GPIO[26:27], RD_$\overline{WR}$_GPIO[62], $\overline{BDIP}$_GPIO[63], $\overline{WE}$/$\overline{BE}$[0:1]_GPIO[64:65], $\overline{WE}$/$\overline{BE}$[2:3]_GPIO[66:67], $\overline{TS}$_GPIO[69], $\overline{TA}$_GPIO[70], $\overline{TEA}$_GPIO[71], TSIZ[0:1]_GPIO[60:61]
V_{DDE3} [2]	1.8–3.3 V	DATA[0:15]_GPIO[28:43], DATA[16]_FEC_TX_CLK_GPIO[44], DATA[17]_FEC_CRS_GPIO[45], DATA[18]_FEC_TX_ER_GPIO[46], DATA[19]_FEC_RX_CLK_GPIO[47], DATA[20]_FEC_TXD[0]_GPIO[48], DATA[21]_FEC_RX_ER_GPIO[49], DATA[22]_FEC_RXD[0]_GPIO[50], DATA[23]_FEC_TXD[3]_GPIO[51], DATA[24]_FEC_COL_GPIO[52], DATA[25]_FEC_RX_DV_GPIO[53], DATA[26]_FEC_TX_EN_GPIO[54], DATA[27]_FEC_TXD[2]_GPIO[55], DATA[28]_FEC_TXD[1]_GPIO[56], DATA[29]_FEC_RXD[1]_GPIO[57], DATA[30]_FEC_RXD[2]_GPIO[58], DATA[31]_FEC_RXD[3]_GPIO[59], $\overline{OE}$_GPIO[68], $\overline{BR}$_FEC_MDC_GPIO[72], $\overline{BG}$_FEC_MDIO_GPIO[73], $\overline{BB}$_GPIO[74], GPIO[206:207]

Table 2-3. MPC5566 Device Power/Ground Segmentation for the 496 Pin Assembly (continued)

Power Segment	Voltage Range [1]	I/O Pins Powered by Segment
V_{DDE5}	1.8–3.3 V	CLKOUT, ENGCLK
V_{DDE7}	1.8–3.3 V	$\overline{EVTI}$, $\overline{EVTO}$, MCKO, MDO[3:0], MDO[11:4]_GPIO[82:75], $\overline{MSEO}$[1:0], $\overline{RDY}$, TCK, TDI, TDO, TMS, JCOMP, $\overline{TEST}$
V_{DDE12}	1.8–3.3 V	CAL_$\overline{CS}$[0], CAL_$\overline{CS}$[1:3]_CAL_ADDR[9:11], CAL_ADDR[12:30], CAL_DATA[0:15], CAL_RD_$\overline{WR}$, CAL_$\overline{WE}$/$\overline{BE}$[0:1], CAL_$\overline{OE}$, CAL_$\overline{TS}$
V_{DDEH1}	3.3–5.0 V	TCRCLKA_$\overline{IRQ}$[7]_GPIO[113], ETPUA[0:3]_ETPUA[12:15]_GPIO[114:117], ETPUA[4:7]_ETPUA[16:19]_GPIO[118:121], ETPUA[8:11]_ETPUA[20:23]_GPIO[122:125], ETPUA[12]_PCSB[1]_GPIO[126], ETPUA[13]_PCSB[3]_GPIO[127], ETPUA[14]_PCSB[4]_GPIO[128], ETPUA[15]_PCSB[5]_GPIO[129], ETPUA[16]_PCSD[1]_GPIO[130], ETPUA[17]_PCSD[2]_GPIO[131], ETPUA[18]_PCSD[3]_GPIO[132], ETPUA[19]_PCSD[4]_GPIO[133], ETPUA[20:27]_$\overline{IRQ}$[8:15]_GPIO[134:141], ETPUA[28:31]_PCSC[1:4]_GPIO[142:145]
V_{DDEH4}	3.3–5.0 V	CNTXA_TXDA_GPIO[83], CNRXA_RXDA_GPIO[84], CNTXB_PCSC[3]_GPIO[85], CNRXB_PCSC[4]_ GPIO[86], EMIOS[0:9]_ETPUA[0:9]_GPIO[179:188], EMIOS[10:11]_PCSD[3:4]_GPIO[189:190], EMIOS[12]_SOUTC_GPIO[191], EMIOS[13]_SOUTD_GPIO[192], EMIOS[14]_$\overline{IRQ}$[0]_CNTXD_GPIO[193], EMIOS[15]_$\overline{IRQ}$[1]_CNRXD_GPIO[194], EMIOS[16:23]_ETPUB[0:7]_GPIO[195:202]
V_{DDEH6}	3.3–5.0 V	$\overline{RESET}$, $\overline{RSTOUT}$, PLLCFG[0]_$\overline{IRQ}$[4]_GPIO[208], PLLCFG[1]_$\overline{IRQ}$[5]_SOUTD_GPIO[209], $\overline{RSTCFG}$_GPIO[210], BOOTCFG[0]_$\overline{IRQ}$[2]_GPIO[211], BOOTCFG[1]_$\overline{IRQ}$[3]_GPIO[212], WKPCFG_GPIO[213], CNTXC_PCSD[3]_GPIO[87], CNRXC_PCSD[4]_GPIO[88], TXDA_GPIO[89], RXDA_GPIO[90], TXDB_PCSD[1]_GPIO[91], RXDB_PCSD[5]_GPIO[92], SCKA_PCSC[1]_GPIO[93], SINA_PCSC[2]_GPIO[94], SOUTA_PCSC[5]_GPIO[95], PCSA[0]_PCSD[2]_GPIO[96], PCSA[1]_PCSB[2]_GPIO[97], PCSA[2]_SCKD_GPIO[98], PCSA[3]_SIND_GPIO[99], PCSA[4]_SOUTD_GPIO[100], PCSA[5]_PCSB[3]_GPIO[101], PCSB[3]_SINC_GPIO[108], PCSB[4]_SCKC_GPIO[109], PCSB[5]_PCSC[0]_GPIO[110], TCRCLKB_$\overline{IRQ}$[6]_GPIO[146], ETPUB[0:15]_ETPUB[16:31]_GPIO[147:162], EMIOS[14:15]_GPIO[203:204]
V_{DDEH8}	3.3–5.0 V	ETRIG[0:1]_GPIO[111:112], ETPUB[16:19]_PCSA[1:4]_GPIO[163:166], ETPUB[20:31]_GPIO[167:178], GPIO[205]
V_{DDEH9}	3.3–5.0 V	AN[12]_MA[0]_$\overline{SDS}$, AN[13]_MA[1]_SDO, AN[14]_MA[2]_SDI, AN[15]_FCK
V_{DDEH10}	3.3–5.0 V	SCKB_PCSC[1]_GPIO[102], SINB_PCSC[2]_GPIO[103], SOUTB_PCSC[5]_GPIO[104], PCSB[0]_PCSD[2]_GPIO[105], PCSB[1]_PCSD[0]_GPIO[106], PCSB[2]_SOUTC_GPIO[107]
V_{DDSYN}	3.3 V	EXTAL, XTAL
V_{DD33}	3.0–3.6 V	—
V_{RC33}	3.3 V	V_{RCCTL}
V_{RCVSS}	0.0 V	—
V_{FLASH}	3.0–3.6 V	—
V_{PP} [3]	4.5–5.25 V	—
V_{STBY}	0.9–1.1 V	—
NC	—	No connect

[1] These are nominal voltages. V_{DDE} is 1.62–3.6 V; V_{DDEH} is 3.0–5.5 V. All V_{DDE} voltages are ±10%; V_{DDEH} voltages are –10% to +5%. V_{RC33} is ±10%; V_{DDSYN} is ±10%; V_{DDA1} is –10% to +5%.

[2] V_{DDE2} and V_{DDE3} are separate segments in the device pad ring. These segments are shorted together in the package substrate.
[3] During read operations, V_{PP} can be as high as 5.3 V or as low as 3.0 V.

2.4 eTPU Pin Connections and Serialization

2.4.1 ETPUA[0:15]

The ETPUA[0:15] module channels connect to external pins or can be serialized out through the DSPI C module. The full list of connections is given in Table 2-4. Although not shown in Figure 2-4, the output channels of ETPUA[12:15] are connected to the ETPUA[0:3]_ETPUA[12:15]_GPIO[114:117] pins.

The eTPU TCRA clock input is connected to an external pin only.

A diagram for the ETPUA[0:15] to SOUTC connection is given in Figure 2-4.

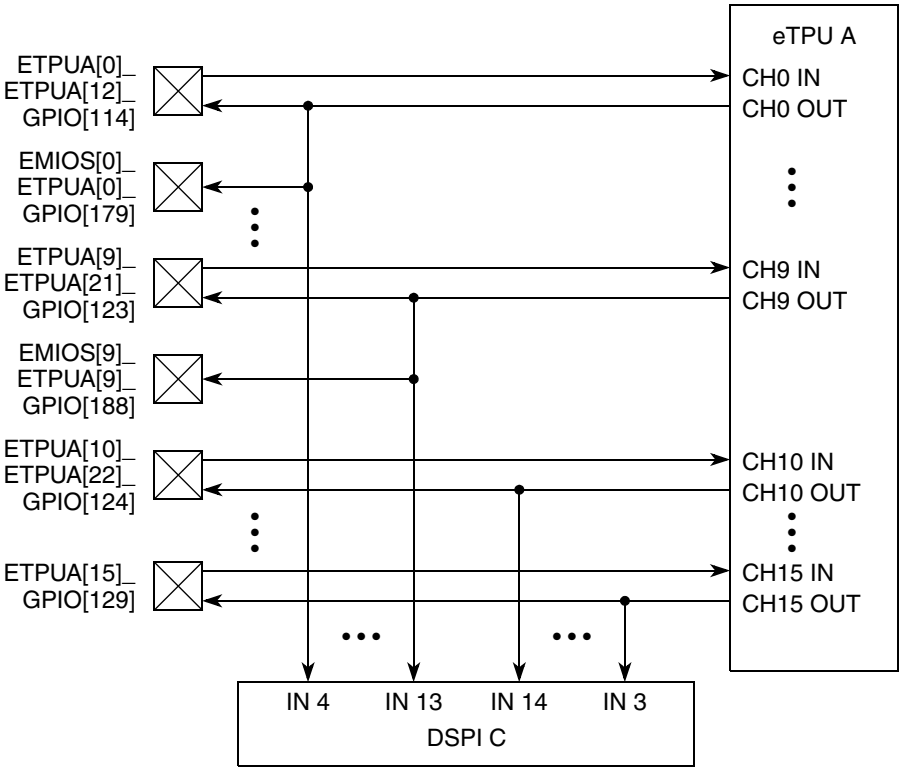


Figure 2-4. ETPUA[0:15]—DSPI C I/O Connections

Table 2-4. ETPUA[0:15]—DSPI C I/O Mapping

DSPI C Serialized Input	eTPU A Channel Output
15	11
14	10
13	9
12	8

Table 2-4. ETPUA[0:15]—DSPI C I/O Mapping (continued)

DSPI C Serialized Input	eTPU A Channel Output
11	7
10	6
9	5
8	4
7	3
6	2
5	1
4	0
3	15
2	14
1	13
0	12

2.4.2 ETPUA[16:31]

ETPUA[16:23,30:31] connect to external pins for both the input and output function. ETPUA[16:21,24:29] are serialized out on the DSPI B and DSPI D modules and ETPUA[22:23,30:31] are not serialized out. ETPUA[24:29] connect to external pins for only the output function. Figure 2-5 shows the connections for ETPUA16 and applies to ETPUA[16:21]. Figure 2-6 shows the connections for ETPUA24 and applies to TPUA[24:29]. The full ETPUA to DSPI B connections are given in Table 2-5, and ETPU A to DSPI D in Table 2-6. Although not shown in Figure 2-5, the output channels of ETPUA[16:23] are also connected to the ETPUA[4:11]_ETPUA[16:23]_GPIO[118:125] pins.

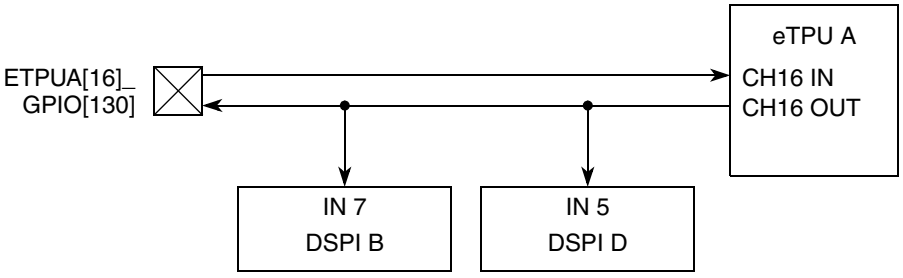


Figure 2-5. ETPUA[16:21]—DSPI B–DSPI D I/O Connections

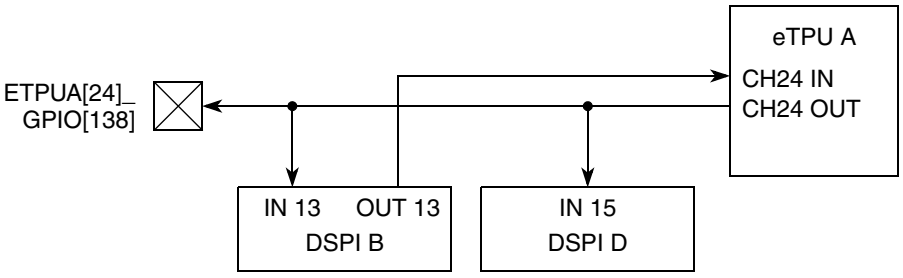


Figure 2-6. ETPUA[24:29]—DSPI B–DSPI D I/O Connections

Table 2-5. ETPUA[16:31]—DSPI B I/O Mapping

DSPI B Serialized Inputs / Outputs[1]	eTPU A Channel Output	eTPU A Channel Input
13	24	24
12	25	25
11	26	26
10	27	27
9	28	28
8	29	29
7	16	—
6	17	—
5	18	—
4	19	—
3	20	—
2	21	—

[1] DSPI B serialized input channels 0, 1, 14, and 15 are connected to eMIOS channels. DSPI B serialized output channels 14, 15 are connected to eMIOS channels. DSPI B serialized output channels 0 through 7 are not connected.

Table 2-6. ETPUA[16:31]—DSPI D I/O Mapping

DSPI D Serialized Inputs[1]	eTPU A Channel Output
15	24
14	25
13	26
12	27
11	28
10	29
5	16
4	17

Table 2-6. ETPUA[16:31]—DSPI D I/O Mapping (continued)

DSPI D Serialized Inputs[1]	eTPU A Channel Output
3	18
2	19
1	20
0	21

1 DSPI D serialized input channels 6 through 9 are connected to eMIOS channels.

2.4.3 ETPUB[0:31]

The I/O connections for ETPUB[0:31] channels are given in Figure 2-7. The outputs of ETPUB[16:31] are connected to two pins. This allows the input and output of those channels to be connected to different pins. The outputs of ETPUB[16:31] are multiplexed on the ETPUB[0:15] pins. The outputs of ETPUB[0:7] are multiplexed on the eMIOS[16:23] pins so that the output channels of ETPUB[0:7] can be used when the normal pins for these channels are used by ETPUB[16:23] channels. The output channels of ETPUB[0:15] are serialized on DSPI A. The full ETPUB to DSPI A connections are given in Table 2-7.

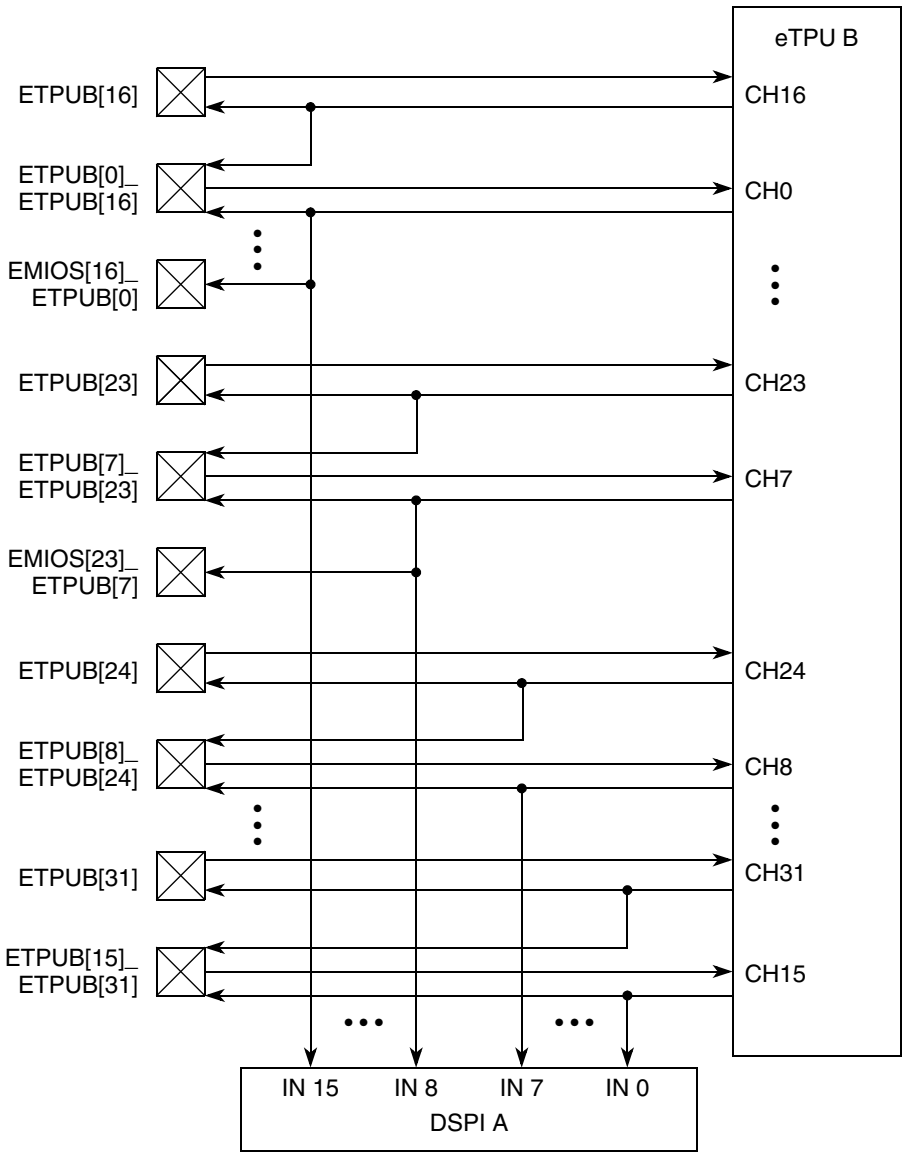


Figure 2-7. ETPUB[31:0]—DSPI A I/O Connections

Table 2-7. ETPUB[0:15]—DSPI A I/O Mapping

DSPI A Serialized Inputs	eTPU B Channel Output
15	0
14	1
13	2
12	3
11	4
10	5
9	6

Table 2-7. ETPUB[0:15]—DSPI A I/O Mapping (continued)

DSPI A Serialized Inputs	eTPU B Channel Output
8	7
7	8
6	9
5	10
4	11
3	12
2	13
1	14
0	15

2.5 eMIOS Pin Connections and Serialization

The eMIOS channels connect to external pins or can be serialized in and out of the device. The EMIOS[0:11, 16:23] signals connect to bidirectional pins that allow both input and output; however, EMIOS[12:15] signals connect to pins that are unidirectional as output only. The output channels of EMIOS[10:13] can be serialized OUT, and the inputs of EMIOS[12:15] can be serialized IN. The DSPI connections for EMIOS[10:11] are given in Figure 2-8, Figure 2-9 for EMIOS[12:13], and Figure 2-10 for EMIOS[14:15].

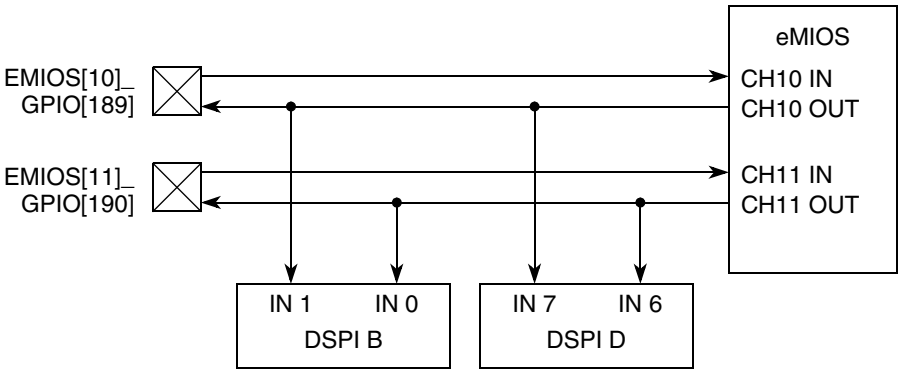


Figure 2-8. EMIOS[10:11]—DSPI B–DSPI D I/O Connections

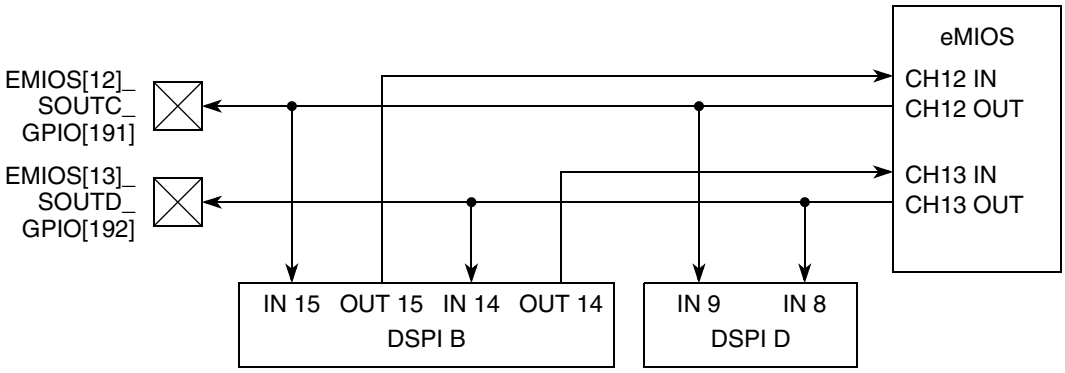


Figure 2-9. EMIOS[12:13]—DSPI B–DSPI D I/O Connections

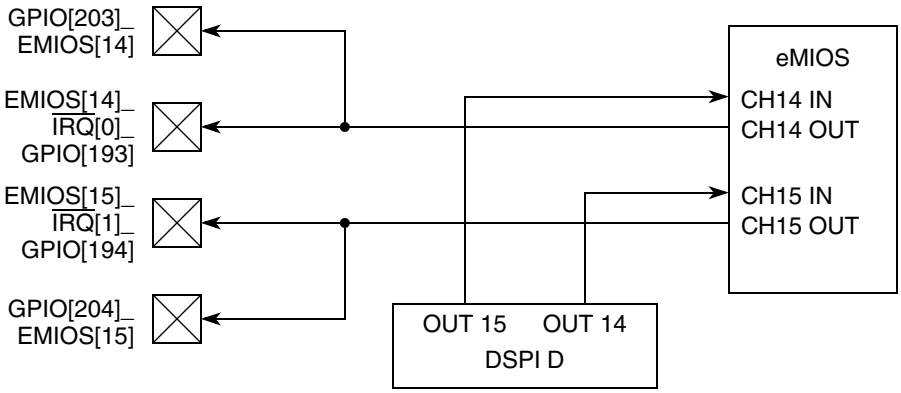


Figure 2-10. EMIOS[14:15]—DSPI D I/O Connections

Chapter 3
e200z6 Core Complex

3.1 Introduction

The core complex of the device consists of the e200z6 core, a 32 KB unified cache memory, a 32-entry memory management unit (MMU), a Nexus class 3 block, and a bus interface unit (BIU). The e200z6 core is the central processing unit (CPU) in the device. The e200z6 core is part of the family of CPU cores that implement versions built on the Power Architecture™ embedded category.

The host processor core of the device complies with the Power Architecture embedded category, which is 100 percent user mode compatible with the original Power PC™ user instruction set architecture (UISA). However, in the Power Architecture definition, the original floating-point resources (used by a SIMD design supporting single-precision vector and single-precision scalar operations) are provided that share the GPRs defined for integer instructions.

Refer to the *e200z6 PowerPC™ Core Reference Manual* for more information on the e200z6 core.

3.1.1 Block Diagram

Figure 3-1 shows a block diagram of the e200z6 core complex.

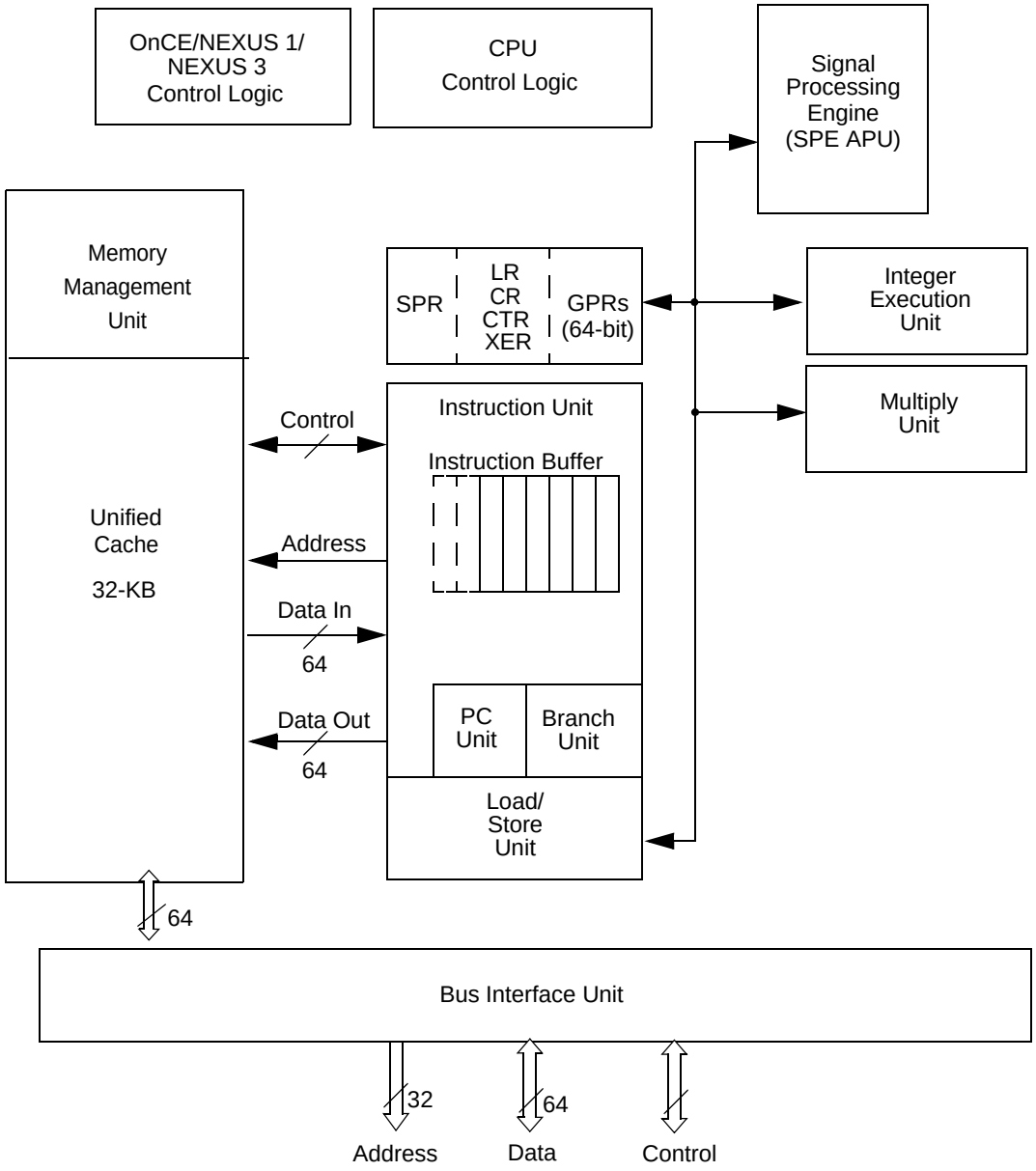


Figure 3-1. e200z6 Block Diagram

3.1.2 Overview

The e200z6 core integrates an integer execution unit, branch control unit, instruction fetch and load/store units, and a multi-ported register file capable of sustaining three read and two write operations per clock. Most integer instructions execute in a single-clock cycle. Branch target prefetching is performed by the branch target address cache to allow single-cycle branches in many cases.

The e200z6 core complex is built on a single-issue, 32-bit Power Architecture design with 64-bit general-purpose registers (GPRs). Power Architecture floating-point instructions are not supported in hardware, but are trapped and may be emulated by software. A signal processing extension (SPE) auxiliary processing unit (APU) is provided to support real-time fixed point and single-precision floating point operations using the general-purpose registers. All arithmetic instructions that execute in the core operate on data in the GPRs. The registers have been extended to 64-bits to support vector instructions defined by the SPE APU. These instructions operate on 16-bit or 32-bit data types, and produce vector or scalar results.

In addition to the base Power Architecture instruction set, the e200z6 core also implements the VLE (Variable Length Encoding) APU, providing improved code density.

3.1.3 Features

The following is a list of some key features of the e200z6:

- Single issue, 32-bit CPU built on the Power Architecture embedded category
- Implements the VLE APU for reduced code footprint. Refer to *EREF: A Programmer's Reference Manual for Freescale Book E Processors* and to *VLEPIM: Variable Length Encoding (VLE) Extension Programming Interface Manual*.
- In-order execution and retirement
- Precise exception handling
- Branch target address cache
  - — Dedicated branch address calculation adder
  - — Branch target prefetching
  - — Branch lookahead buffers of depth 2
- Load/store unit: Pipelined operation supports throughput of one load or store operation per cycle
- 64-bit general-purpose register file
- Memory management unit (MMU) with 32-entry fully-associative TLB and multiple page size support
- 32 KB, 4- or 8-way set associative unified cache
  - — Cache is configurable by software
  - — Minimize power use by the cache by selecting CORG = 1 or by setting WAM = 1. Refer to Table 3-9.
- Periodic timer and watchdog functions
- Periodic system integrity can be monitored through parallel signature checks

- Signal processing extension APU supporting fixed-point and single-precision floating-point operations, using the 64-bit general-purpose register file
- Nexus class 3 real-time development unit
- Power management
  - — Low-power design
  - — Dynamic power management of execution units, caches, and MMUs

3.1.3.1 Instruction Unit Features

The features of the instruction unit are the following:

- 64-bit path to cache supports fetching of two 32-bit instructions per clock, or up to four 16-bit VLE APU instructions per clock
- Instruction buffer holds up to six sequential instructions
- Dedicated PC incrementer supporting instruction prefetches
- Branch target address cache with dedicated branch address adder, and branch lookahead logic supporting single cycle execution of successful lookahead branches

3.1.3.2 Integer Unit Features

The integer unit supports single-cycle execution of most integer instructions:

- 32-bit AU for arithmetic and comparison operations
- 32-bit LU for logical operations
- 32-bit priority encoder for count leading zeros function
- 32-bit single cycle barrel shifter for static shifts and rotates
- 32-bit mask unit for data masking and insertion
- Divider logic for signed and unsigned divides in 6–16 clocks with minimized execution timing
- Pipelined 32x32 hardware multiplier array supports 32x32->32 multiply with three clock latency, one clock throughput

3.1.3.3 Load/Store Unit Features

The load/store unit supports load, store, and the load multiple/store multiple instructions:

- 32-bit effective address adder for data memory address calculations
- Pipelined operation supports throughput of one load or store operation per cycle
- Dedicated 64-bit interface to memory supports saving and restoring of up to two registers per cycle for load multiple and store multiple word instructions

3.1.3.4 MMU Features

The features of the MMU are as follows:

- Virtual memory support
- 32-bit virtual and physical addresses
- Eight-bit process identifier
- 32-entry fully associative TLB
- Support for nine page sizes (4, 16, 64, and 256 KB; 1, 4, 16, 64, and 256 MB)
- Entry flush protection

3.1.3.5 L1 Cache Features

The features of the cache are as follows:

- 32 KB, 4- or 8-way set associative unified cache
- Copyback and writethrough support
- Eight-entry store buffer
- Push buffer
- Linefill buffer
- 32-bit address bus plus attributes and control
- Separate unidirectional 64-bit read data bus and 64-bit write data bus
- Supports cache line locking
- Supports way allocation
- Cache power usage can be minimized

3.1.3.6 BIU Features

The features of the e200z6 BIU are as follows:

- 32-bit address bus plus attributes and control
- Separate unidirectional 64-bit read data bus and 64-bit write data bus
- Overlapped, in-order accesses

3.1.4 Microarchitecture Summary

The e200z6 processor utilizes a seven stage pipeline for instruction execution. The instruction fetch 1, instruction fetch 2, instruction decode/register file read, execute1, execute2/memory access1, execute3/memory access2, and register writeback stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The integer execution unit consists of a 32-bit arithmetic unit (AU), a logic unit (LU), a 32-bit barrel shifter (shifter), a mask-insertion unit (MIU), a condition register manipulation unit (CRU), a count-leading-zeros unit (CLZ), a 32 x 32 hardware multiplier array, result feed-forward hardware, and support hardware for division.

Most arithmetic and logical operations are executed in a single cycle with the exception of multiply, which is implemented with a pipelined hardware array, and the divide instructions. A count-leading-zeros unit operates in a single clock cycle.

The instruction unit contains a PC incrementer and a dedicated branch address adder to minimize delays during change of flow operations. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding six sequential instructions.

Branch target addresses are calculated in parallel with branch instruction decode, resulting in execution time of three clocks. Conditional branches which are not taken execute in a single clock. Branches with successful lookahead and target prefetching have an effective execution time of one clock.

Memory load and store operations are provided for byte, halfword, word (32-bit), and doubleword data with automatic zero or sign extension of byte and halfword load data as well as optional byte reversal of data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized.

The condition register unit supports the condition register (CR) and condition register operations defined by the Power Architecture embedded category. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching.

Vectored and auto-vectored interrupts are supported by the CPU. Vectored interrupt support is provided to allow multiple interrupt sources to have unique interrupt handlers invoked with no software overhead.

The SPE APU supports vector instructions operating on 16- and 32-bit fixed-point data types, as well as 32-bit IEEE-754 single-precision floating-point formats, and supports single-precision floating-point operations in a pipelined fashion. The 64-bit general-purpose register file is used for source and destination operands, and there is a unified storage model for single-precision floating-point data types of 32-bits and the normal integer type. Low latency fixed-point and floating-point add, subtract, multiply, divide, compare, and conversion operations are provided, and most operations can be pipelined.

3.2 Core Registers and Programmer's Model

This section describes the registers implemented in the e200z6 core. It includes an overview of registers defined by the Power Architecture embedded category, highlighting differences in how these registers are implemented in the e200z6 core, and provides a detailed description of core-specific registers. Full descriptions of the architecture-defined register set are provided in the Power Architecture embedded category.

The Power Architecture embedded category defines register-to-register operations for all computational instructions. Source data for these instructions are accessed from the on-chip registers or are provided as immediate values embedded in the opcode. The three-register instruction format allows specification of a target register distinct from the two source registers, thus preserving the original data for use by other instructions. Data is transferred between memory and registers with explicit load and store instructions only.

e200z6 extends the general-purpose registers to 64-bits for supporting SPE APU operations. Power Architecture instructions operate on the lower 32 bits of the GPRs only, and the upper 32 bits are unaffected by these instructions. SPE vector instructions operate on the entire 64-bit register. The SPE APU defines load and store instructions for transferring 64-bit values to/from memory.

Figure 3-2 and Figure 3-3 show the complete e200z6 register set. Figure 3-2 shows the registers that are accessible while in supervisor mode, and Figure 3-3 shows the set of registers that are accessible while in user mode. The number to the right of the special-purpose registers (SPRs) is the decimal number used in the instruction syntax to access the register (for example, the integer exception register (XER) is SPR 1).

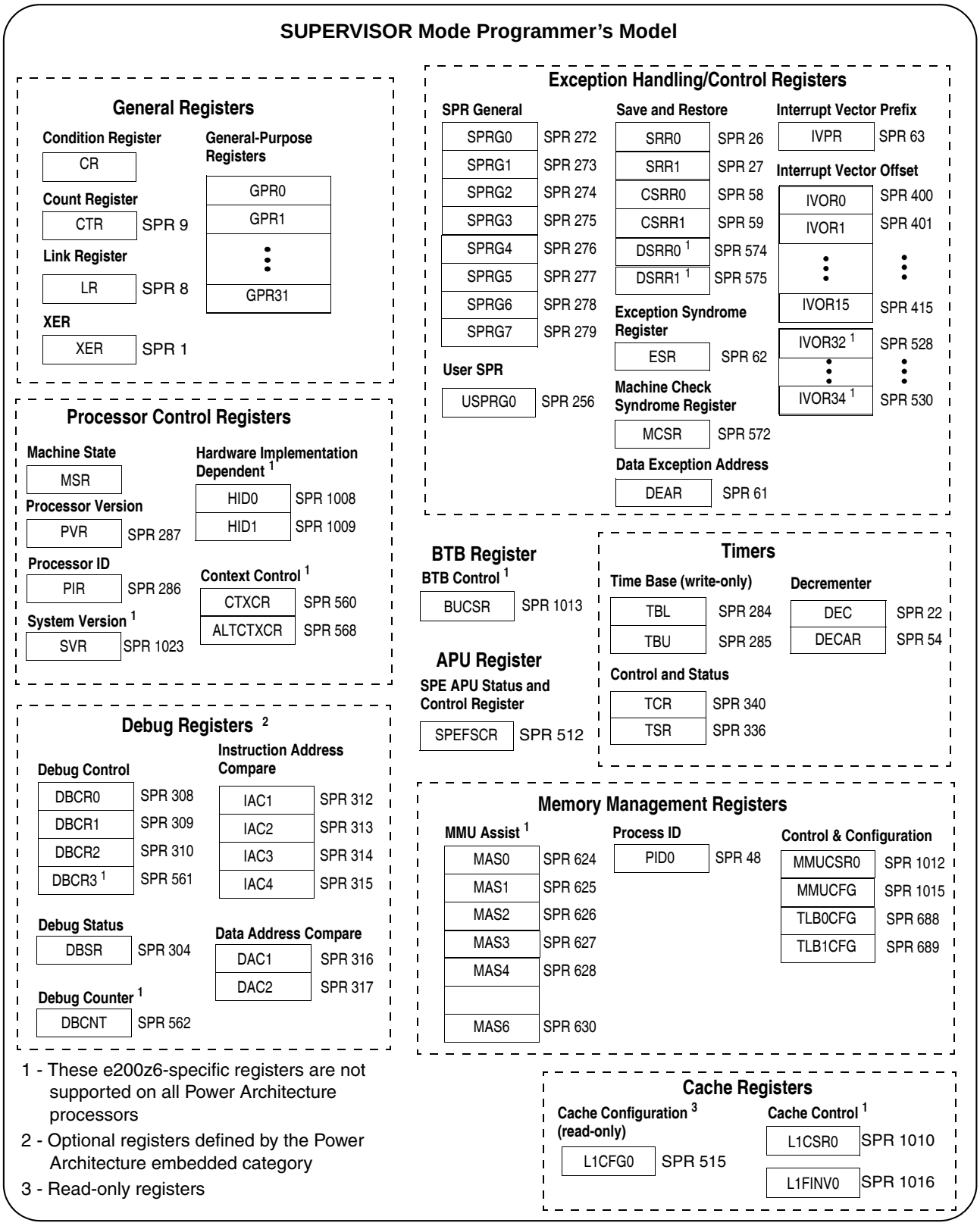


Figure 3-2. Supervisor Mode Programmer's Model

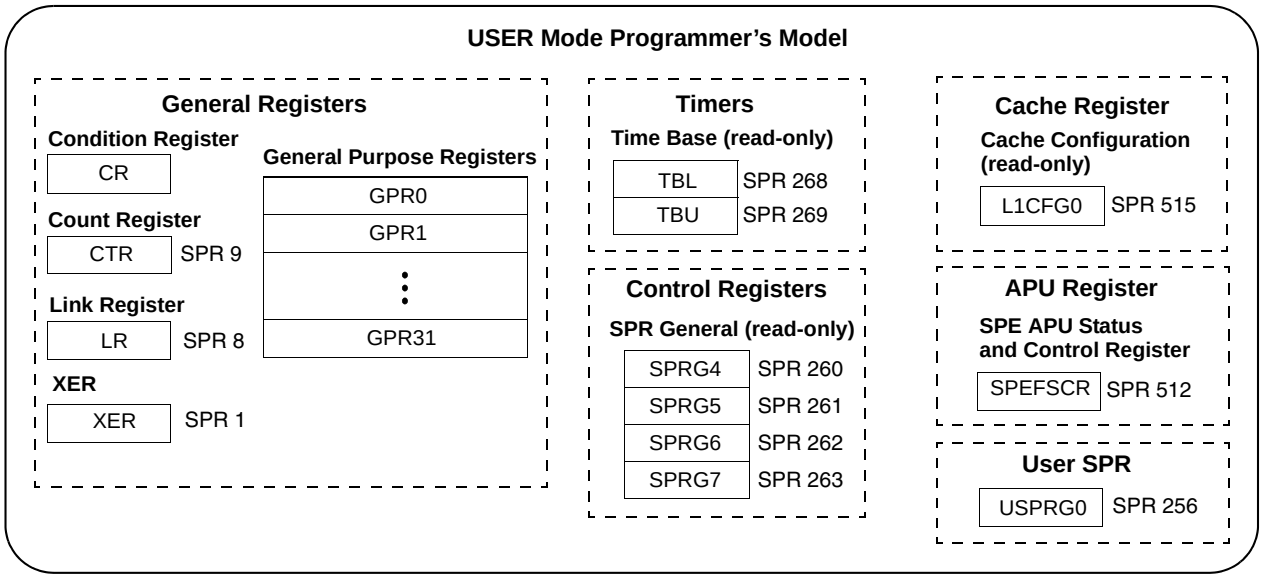


Figure 3-3. User Mode Programmer's Model

3.2.1 Power Architecture Registers

The e200z6 core supports most of the registers defined by the Power Architecture embedded category. Notable exceptions are the floating point registers FPR0–FPR31 and FPSCR. The e200z6 does not support the Power Architecture floating point architecture in hardware. The supported Power Architecture embedded category registers are described as follows:

3.2.1.1 User-Level Registers

The user-level registers can be accessed by all software with user or supervisor privileges. They include the following:

- General-purpose registers (GPRs). The thirty-two 64-bit GPRs (GPR0–GPR31) serve as data source or destination registers for integer and SPE APU instructions and provide data for generating addresses. PowerPC Book E instructions affect only the lower 32 bits of the GPRs. SPE APU instructions are provided which operate on the entire 64-bit register.
- Condition register (CR). The 32-bit CR consists of eight 4-bit fields, CR0–CR7, that reflect results of certain arithmetic operations and provide a mechanism for testing and branching.

  The remaining user-level registers are SPRs. Note that the PowerPC architecture provides the **mtspr** and **mfspr** instructions for accessing SPRs.
- Integer exception register (XER). The XER indicates overflow and carries for integer operations.
- Link register (LR). The LR provides the branch target address for the branch conditional to link register (**bclr**, **bclrl**) instructions, and is used to hold the address of the instruction that follows a branch and link instruction, typically used for linking to subroutines.

- Count register (CTR). The CTR holds a loop count that can be decremented during execution of appropriately coded branch instructions. The CTR also provides the branch target address for the branch conditional to count register (**bcctr**, **bcctrl**) instructions.
- The time-base facility (TB) consists of two 32-bit registers: time-base upper (TBU) and time-base lower (TBL). These two registers are accessible in a read-only fashion to user-level software.
- SPRG–SPRG7. The PowerPC Book E architecture defines software-use special purpose registers (SPRGs). SPRG4–SPRG7 are accessible as read-only by user-level software. The e200z6 does not allow user mode access to the SPRG3 register (defined as implementation dependent by Book E).
- USPRG0. The PowerPC Book E architecture defines user software-use special purpose register USPRG0 which is accessible in a read-write fashion by user-level software.

3.2.1.2 Supervisor-Level Only Registers

In addition to the registers accessible in user mode, supervisor-level software has access to additional control and status registers an operating system used for configuration, exception handling, and other operating system functions. The Power Architecture embedded category defines the following supervisor-level registers:

- Processor control registers
  - — Machine state register (MSR). The MSR defines the state of the processor. The MSR can be modified by the move to machine state register (**mtmsr**), system call (**sc)**, and return from exception (**rfi, rfci, rfdi)** instructions. It can be read by the move from machine state register (**mfmsr)** instruction. When an interrupt occurs, the contents of the MSR are saved to one of the machine state save/restore registers (SRR1, CSRR1, DSRR1).
  - — Processor version register (PVR). This register is a read-only register that identifies the version (model) and revision level of the processor built on the Power Architecture.
  - — Processor identification register (PIR). This read-only register is provided to distinguish the processor from other processors in the system.
- Storage control register

  Process ID register (PID, also referred to as PID0). This register is provided to indicate the current process or task identifier. It is used by the MMU as an extension to the effective address, and by external Nexus 2/3/4 modules for ownership trace message generation. The Power Architecture embedded category allows for multiple PIDs; e200z6 implements only one.
- Interrupt registers
  - — Data exception address register (DEAR). After a data storage interrupt (DSI), alignment interrupt, or data TLB miss interrupt, the DEAR is set to the effective address (EA) generated by the faulting instruction.
  - — Software-use special purpose registers (SPRGs). The SPRG0–SPRG7 registers are provided for operating system use.
  - — Exception syndrome register (ESR). The ESR register provides a syndrome to differentiate between the different kinds of exceptions which can generate the same interrupt.

  - Interrupt vector prefix register (IVPR) and the interrupt vector offset registers (IVOR1–IVOR15). These registers together provide the address of the interrupt handler for different classes of interrupts.
  - Save/restore registers (SRR0, SRR1). SRR0 holds the effective address for the instruction at which execution resumes when an **rfi** instruction is executed at the end of a non-critical class interrupt handler routine. SRR1 is used to save machine state on a non-critical interrupt, and stores the MSR register contents. The MSR value is restored when an **rfi** instruction is executed at the end of a non-critical class interrupt handler routine.
  - Critical save/restore registers (CSRR0, CSRR1). CSRR0 holds the effective address for the instruction at which execution resumes when an **rfci** instruction is executed at the end of a critical class interrupt handler routine. CSRR1 is used to save machine state on a critical interrupt, and stores the MSR register contents. The MSR value is restored when an **rfci** instruction is executed at the end of a critical class interrupt routine.
- Debug facility registers
  - Debug control registers (DBCR0–DBCR2). These registers provide control for enabling and configuring debug events.
  - Debug status register (DBSR). This register contains debug event status.
  - Instruction address compare registers (IAC1–IAC4). These registers contain addresses and/or masks which are used to specify instruction address compare debug events.
  - Data address compare registers (DAC1, DAC2). These registers contain addresses and/or masks which are used to specify data address compare debug events.
  - e200z6 does not implement the data value compare registers (DVC1, DVC2).
- Timer registers
  - The clock inputs for the timers are connected to the internal system clock.
  - Time base (TB). The TB is a 64-bit structure provided for maintaining the time of day and operating interval timers. The TB consists of two 32-bit registers, time-base upper (TBU) and time-base lower (TBL). The time-base registers can be written to by supervisor-level software only, but can be read by both user and supervisor-level software.
  - Decrementer register (DEC). This register is a 32-bit decrementing counter that provides a mechanism for causing a decrementer exception after a programmable delay.
  - Decrementer auto-reload (DECAR). This register is provided to support the auto-reload feature of the decrementer.
  - Timer control register (TCR). This register controls decrementer, fixed-interval timer, and watchdog timer options.
  - Timer status register (TSR). This register contains status on timer events and the most recent watchdog timer-initiated processor reset.

For more details about these registers, refer to the Power Architecture embedded category specifications.

3.2.2 Core-Specific Registers

The Power Architecture embedded category allows implementation-specific registers. Implementation-specific registers incorporated in the e200z6 core are described in this section.

3.2.2.1 User-Level Registers

The user-level registers can be accessed by all software with either user or supervisor privileges. They include the following:

- Signal processing extension APU status and control register (SPEFSCR). The SPEFSCR contains all fixed-point and floating-point exception signal bits, exception summary bits, exception enable bits, and rounding control bits needed for compliance with the IEEE 754 standard.
- The L1 cache configuration register (L1CFG0). This read-only register allows software to query the configuration of the L1 unified cache.

3.2.2.2 Supervisor-Level Registers

The following supervisor-level registers are defined in the e200z6 core in addition to the Power Architecture embedded category registers described previously:

- Configuration registers
  - — Hardware implementation-dependent 0 (HID0) controls processor and system functions.
  - — Hardware implementation-dependent 1 (HID1) controls processor and system functions.
- Exception handling and control registers
  - — Debug save and restore registers (DSRR0, DSRR1). DSRR0 holds the effective address for the instruction at which execution resumes when an **rfdi** instruction is executed at the end of a debug interrupt handler routine. DSRR1 is used to save machine state on a debug interrupt, and stores the MSR register contents. The MSR value is restored when an **rfdi** instruction is executed at the end of a debug interrupt handler routine.
  - — When enabled, the DSRR0 register is used to save the address of the instruction at which execution continues when **rfdi** executes at the end of a debug interrupt handler routine.
  - — Interrupt vector offset registers (IVOR32–IVOR34). These registers provide the address of the interrupt handler for different classes of interrupts.
- Debug facility registers
  - — Debug control register 3 (DBCR3) controls for debug functions not described in the Power Architecture embedded category.
  - — Debug counter register (DBCNT) provides counter capability for debug functions.

- Cache registers
  - L1 cache configuration register (L1CFG0) is a read-only register that allows software to query the configuration of the L1 cache.
  - L1 cache control and status register (L1CSR0) controls the operation of the L1 unified cache such as cache enabling, cache invalidation, cache locking, enabling 4 or 8 data/instruction ways, and control over cache power utilization, etc.
  - L1 cache flush and invalidate register (L1FINV0) controls software flushing and invalidation of the L1 unified cache.
- Memory management unit registers
  - MMU configuration register (MMUCFG) is a read-only register that allows software to query the configuration of the MMU.
  - MMU assist (MAS0-MAS4, MAS6) registers provide the interface to the core from the memory management unit.
  - MMU control and status register (MMUCSR0) controls invalidation of the MMU.
  - TLB configuration registers (TLBCFG0, TLBCFG1) are read-only registers that allow software to query the configuration of the TLBs.
- System version register (SVR) is a read-only and identifies the version (model) and revision level of the system with an e200z6 processor built on the Power Architecture embedded category.

For more details about these registers, refer to the e200z6 core reference documentation.

3.2.3 e200z6 Core Complex Features Not Supported in the Device

The device implements a subset of the e200z6 core complex features. The e200z6 core complex features that are *not* supported in the device are described in Table 3-1.

Table 3-1. e200z6 Features Not Supported in the Device Core

Function / Category	Description
Disabled events	The external debug event (DEVT2) and unconditional debug event (UDE) are not supported.
Power management	e200z6 core halted state and stopped state are not supported.
Power management	The following low-power modes are not supported: Doze mode Nap mode Sleep mode Time-base interrupt wake-up from low-power mode is not supported.
Power management	Core wake up is not supported. MSR[WE] bit in the machine state register is not supported. The OCR[WKUP] bit in the e200z6 OnCE control register (OCR) has no effect.
Machine check	The machine check input pin is not supported. HID0 [EMCP] has no effect, and MCSR[MCP] always reads a negated value.

Table 3-1. e200z6 Features Not Supported in the Device Core (continued)

Function / Category	Description
PVR value	Least significant halfword of processor version register (PVR) is 0x0000, that contains the following bitfields: MBG Use = 0x00 MBG Rev = 0x0 MBG ID = 0x0 The PVR register has two bitfields in the device.
Reservation management	Reservation management logic external to the e200z6 is not implemented.
Verification	The system version register (SVR) of the e200z6 is 0x 0000_0000.
Time Base	The decrement counters are always enabled in the e200z6.
	The timer external clock is not connected to a clock; Do not select the timer external clock.
Context control	The CTXCR and ALTCXTCR registers are not supported.

3.3 Functional Description

The following sections describe the functions of the e200z6 core blocks.

3.3.1 Memory Management Unit (MMU)

The memory management unit (MMU) is an implementation built on the Power Architecture embedded category with a 32-entry fully associative translation lookaside buffer (TLB). The Power Architecture embedded category divides the effective and real address space into pages. The page represents the granularity of effective address translation, permission control, and memory/cache attributes. The e200z6 MMU supports the following nine page sizes: (4, 16, 64, and 256 KB, 1, 4, 16, 64, and 256 MB).

3.3.1.1 Translation Lookaside Buffer (TLB)

The TLB consists of a 32-entry, fully associative content addressable memory (CAM) array. To perform a lookup, the CAM is searched in parallel for a matching TLB entry. The contents of this TLB entry are then concatenated with the page offset of the original effective address. The result constitutes the physical address of the access. Table 3-2 shows the TLB entry bit definitions.

Table 3-2. TLB Entry Bit Definitions

Field	Comments
V	Valid bit for entry
TS	Translation address space (compared against AS bit)
TID[0:7]	Translation ID (compared against PID0 or ‘0’)
EPN[0:19]	Effective page number (compared against effective address)
RPN[0:19]	Real page number (translated address)
SIZE[0:3]	Page size = 4 KB,16 KB, 64 KB, 256 KB, 1 MB, 4 MB, 16 MB, 64 MB, 256 MB
SX, SW, SR	Supervisor execute, write, and read permission bits

Table 3-2. TLB Entry Bit Definitions (continued)

Field	Comments
UX, UW, UR	User execute, write, and read permission bits
WIMGE	Translation attributes (Write-through required, cache-inhibited, memory coherence required, guarded, endian)
U0–U3	User bits—used by software only
IPROT	Invalidation protect
VLE	VLE page indicator

The TLB is accessed indirectly through several MMU assist (MAS) registers. Software can read and write to the MMU assist registers with **mtspr** (move to SPR) and **mfspr** (move from SPR) instructions. The MMU registers contain information related to reading and writing an entry in the TLB. Data is read from the TLB into the MAS registers with a **tlbre** (TLB read entry) instruction. Data is written to the TLB from the MAS registers with a **tlbwe** (TLB write entry) instruction.

Refer to Section 3.3.1.5, "MMU Assist Registers (MAS[0:4], MAS[6])," and the *e200z6 PowerPC™ Core Reference Manual* for more details.

3.3.1.2 Translation Flow

The effective address, concatenated with the address space value of the MSR bit (MSR[IS] or MSR[DS]), is compared to the number of bits of the EPN field and the TS field of TLB entries. If the contents of the effective address plus the address space bit matches the EPN field and TS bit of the TLB entry, that TLB entry is a candidate for a possible translation match. In addition to a match in the EPN field and TS, a matching TLB entry must match with the current process ID of the access (in PID0), or have a TID value of 0, indicating the entry is globally shared among all processes.

Figure 3-4 shows the translation match logic for the effective address plus its attributes, collectively called the virtual address, and how it is compared with the corresponding fields in the TLB entries.

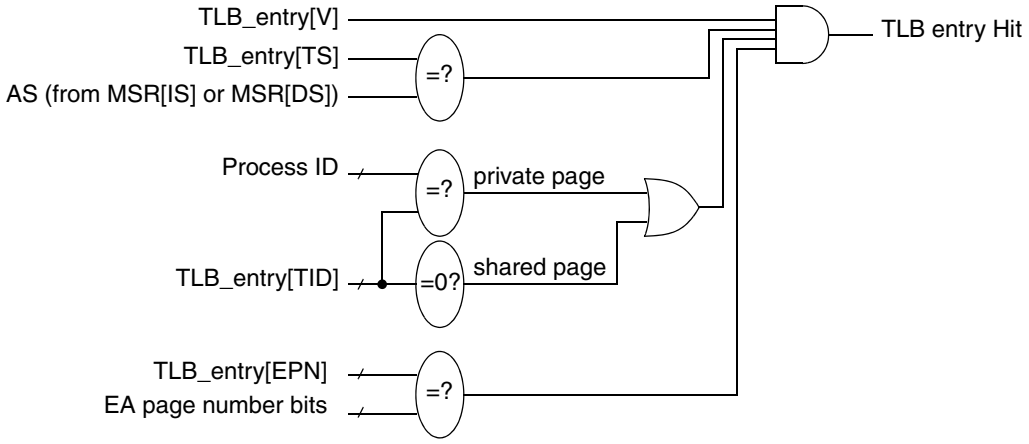


Figure 3-4. Virtual Address and TLB-Entry Compare Process

3.3.1.3 Effective to Real Address Translation

Instruction accesses are generated by sequential instruction fetches or due to a change in program flow (branches and interrupts). Data accesses are generated by load, store, and cache management instructions. The instruction fetch, branch, and load/store units generate 32-bit effective addresses. The MMU translates this effective address to a 32-bit real address which is then used for memory accesses. Figure 3-5 shows the effective to real address translation flow.

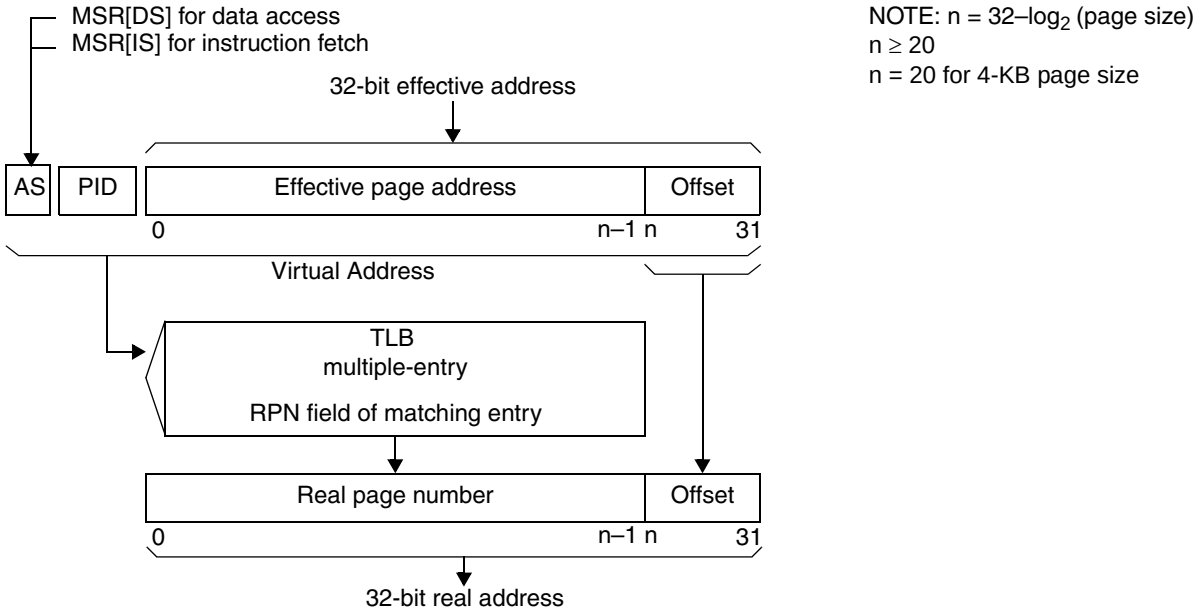


Figure 3-5. Effective to Real Address Translation Flow

3.3.1.4 Permissions

The application software can restrict access to virtual pages by selectively granting permissions for user mode read, write, and execute, and supervisor mode read, write, and execute on a per-page basis. For example, program code might be execute-only and data structures can be mapped as read/write/no-execute.

The following access control bits support selective permissions for access control:

- SR—Supervisor read permission. Allows loads and load-type cache management instructions to access the page while in supervisor mode.
- SW—Supervisor write permission. Allows stores and store-type cache management instructions to access the page while in supervisor mode.
- SX—Supervisor execute permission. Allows instruction fetches to access the page and instructions to be executed from the page while in supervisor mode.
- UR—User read permission. Allows loads and load-type cache management instructions to access the page while in user mode.
- UW—User write permission. Allows stores and store-type cache management instructions to access the page while in user mode.

- UX—User execute permission. Allows instruction fetches to access the page and instructions to be executed from the page while in user mode.

If the translation match was successful, the permission bits are checked as shown in Figure 3-6. If the access is not allowed by the access permission mechanism, the processor generates an instruction or data storage interrupt (ISI or DSI).

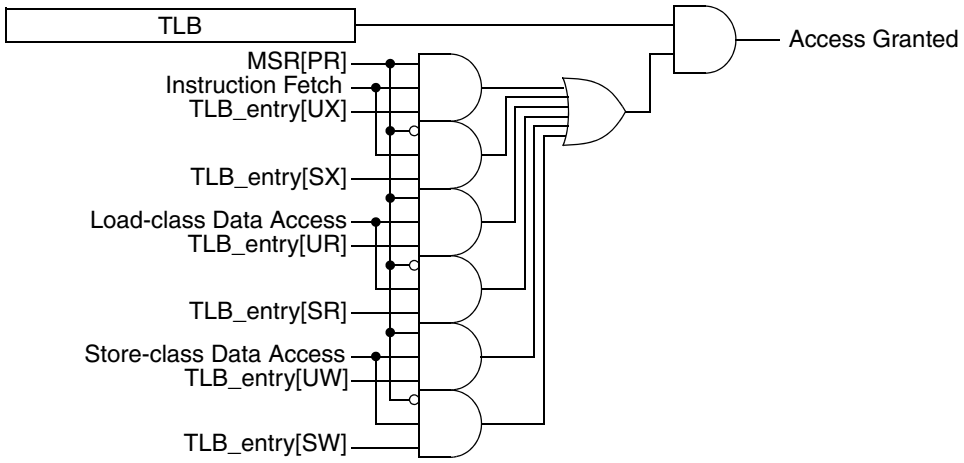


Figure 3-6. Granting of Access Permission

3.3.1.5 MMU Assist Registers (MAS[0:4], MAS[6])

The e200z6 uses six special purpose registers (MAS[0], MAS[1], MAS[2], MAS[3], MAS[4], and MAS[6]) to facilitate reading, writing, and searching the TLBs. The MAS registers can be read or written using the **mfspr** and **mtspr** instructions. The e200z6 does not implement the MAS5 register, present in other Freescale EIS designs, because the **tlbsx** instruction only searches based on a single SPID value.

For more information on the MAS*n* registers is available in the *e200z6 PowerPC*^{TM} *Core Reference Manual*.

3.3.1.5.1 MAS[0] Register

The MAS[0] register is shown in Figure 3-7.

SPR: 624 Access: R/W

	0 1	2 3	4 5 6 7	8 9 10 11	12 13 14 15	16 17 18 19	20 21 22 23	24 25 26 27	28 29 30 31
R W	—	TLBSEL	—		ESEL	—			NV
Reset	Undefined on Power Up — Unchanged on Reset								

Figure 3-7. MAS Register 0 Format — MAS[0]

MAS[0] fields are defined in Table 3-3.

Table 3-3. MAS[0] — MMU Read/Write and Replacement Control

Field	Description
0–1	Reserved, must be cleared.
2–3 TLBSEL	Selects TLB for access. 01 TLB1 (ignored by the e200z6, write to 01 for future compatibility)
4–10	Reserved, must be cleared.
11–15 ESEL	Entry select for TLB1.
16–26	Reserved, must be cleared.
27–31 NV	Next replacement victim for TLB1 (software managed). Software updates this field; it is copied to the ESEL field on a TLB error.

3.3.1.5.2 MAS[1] Register

The MAS[1] register is shown in Figure 3-8.

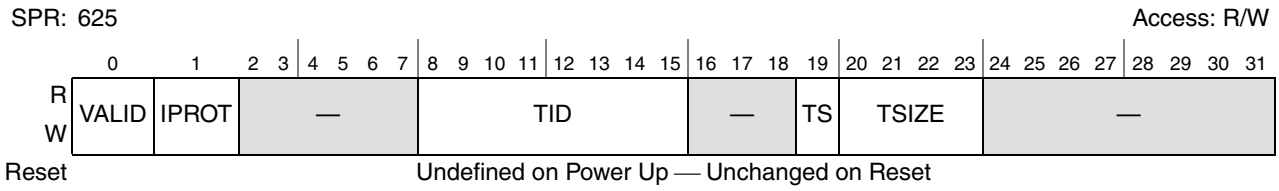


Figure 3-8. MMU Assist Register 1 — MAS[1]

MAS[1] fields are defined in Table 3-4.

Table 3-4. MAS[1] — Descriptor Context and Configuration Control

Field	Description
0 VALID	TLB entry valid. 0 This TLB entry is invalid. 1 This TLB entry is valid.
1 IPROT	Invalidation protect 0 Entry is not protected from invalidation. 1 Entry is protected from invalidation. Protects TLB entry from invalidation by **tlbivax** (TLB1 only), or flash invalidates through MMUCSR0[TLB1_FI].
2–7	Reserved, must be cleared.
8–15 TID	Translation ID bits. This field is compared with the current process IDs of the effective address to be translated. A TID value of 0 defines an entry as global and matches with all process IDs.
16–18	Reserved, must be cleared.
19 TS	Translation address space. This bit is compared with the IS or DS fields of the MSR (depending on the type of access) to determine if this TLB entry can be used for translation.

Table 3-4. MAS[1] — Descriptor Context and Configuration Control (continued)

Field	Description
20–23 TSIZE	Entry page size. Supported page sizes are: 0001 4 KB 0110 4 MB 0010 16 KB 0111 16 MB 0011 64 KB 1000 64 MB 0100 256 KB 1001 256 MB 0101 1 MB All other values are undefined.
24–31	Reserved, must be cleared.

3.3.1.5.3 MAS[2] Register

The MAS[2] register is shown in Figure 3-9.

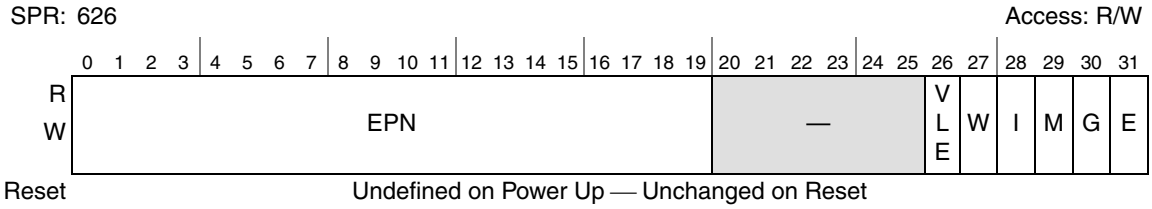


Figure 3-9. MMU Assist Register 2 — MAS[2]

MAS[2] fields are defined in Table 3-5.

Table 3-5. MAS[2] — EPN and Page Attributes

Field	Description
0–19 EPN	Effective page number [0:19].
20–25	Reserved, must be cleared.
26 VLE	Power Architecture VLE. 0 This page is a standard Book E page. 1 This page is a Power Architecture VLE page.
27 W	Write-through required. 0 This page is considered write-back with respect to the caches in the system. 1 All stores performed to this page are written through to main memory.
28 I	Cache inhibited. 0 This page is considered cacheable. 1 This page is considered cache-inhibited.
29 M	Memory coherence required.The e200z6 does not support the memory coherence required attribute, and thus it is ignored. 0 Memory coherence is not required. 1 Memory coherence is required.

Table 3-5. MAS[2] — EPN and Page Attributes (continued)

Field	Description
30 G	Guarded. The e200z6 ignores the guarded attribute because no speculative or out-of-order processing is performed. 0 Access to this page are not guarded, and can be performed before it is known if they are required by the sequential execution model. 1 All loads and stores to this page are performed without speculation (that is, they are known to be required).
31 E	Endianness. Determines endianness for the corresponding page. 0 The page is accessed in big-endian byte order. 1 The page is accessed in true little-endian byte order.

3.3.1.5.4 MAS[3] Register

The MAS[3] register is shown in Figure 3-10.

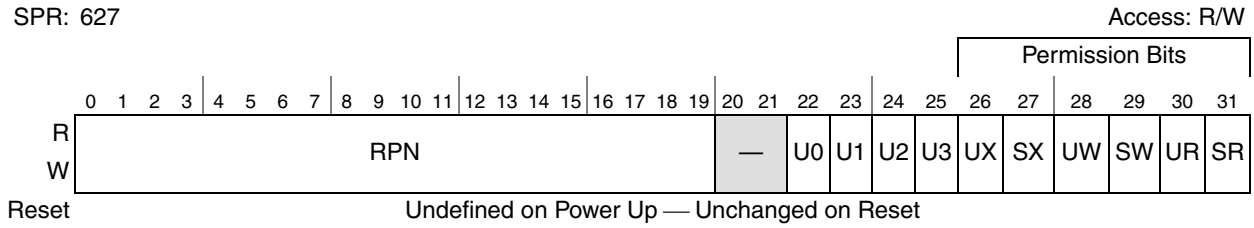


Figure 3-10. MMU Assist Register 3 — MAS[3]

MAS[3] fields are defined in Table 3-6.

Table 3-6. MAS[3] — RPN and Access Control

Field	Description
0–19 RPN	Real page number. Only bits that correspond to a page number are valid. Bits that represent offsets within a page are ignored and must be zero.
20–21	Reserved, must be cleared.
22–25 U0–U3	User bits.
26–31 PERMIS	Permission bits (UX, SX, UW, SW, UR, SR).

3.3.1.5.5 MAS[4] Register

The MAS[4] register is shown in Figure 3-11.

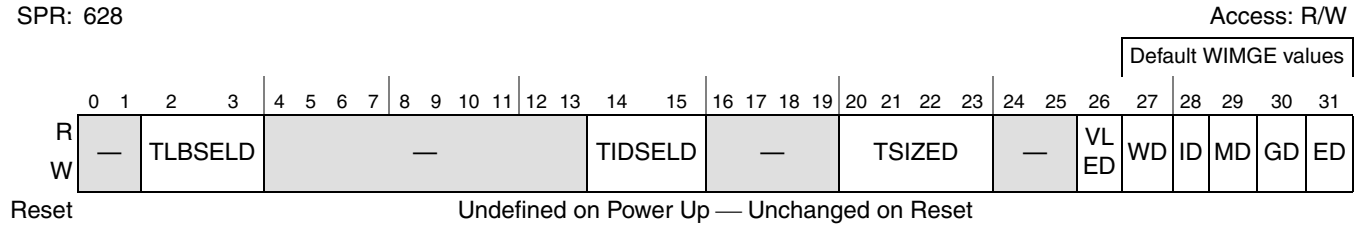


Figure 3-11. MMU Assist Register 4 MAS[4]

MAS[4] fields are defined in Table 3-7.

Table 3-7. MAS[4]—Hardware Replacement Assist Configuration Register

Field	Description
0–1	Reserved, must be cleared.
2–3 TLBSELD	Default TLB selected 01 TLB1 (ignored by the e200z6, write as 01 for future compatibility)
4–13	Reserved, must be cleared.
14–15 TIDSELD	Default PID# to load TID from 00 PID0 01 Reserved, do not use 10 Reserved, do not use 11 TIDZ (0x00)) (Use all zeros, the globally shared value)
16–19	Reserved, must be cleared.
20–23 TSIZED	Default TSIZE value
24–25	Reserved, must be cleared.
26 VLED	Default VLED value
27–31 DWIMGE	Default WIMGE values

3.3.1.5.6 MAS[6] Register

The MAS[6] register is shown in Figure 3-12.

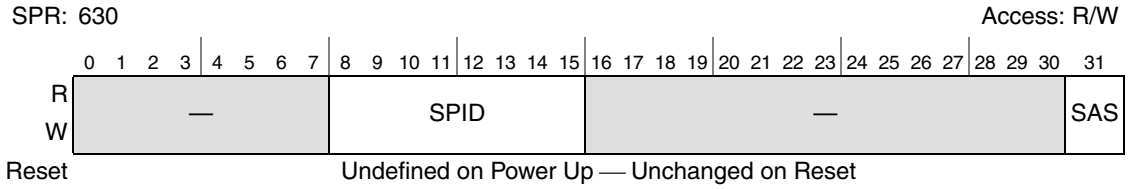


Figure 3-12. MMU Assist Register 6 — MAS[6]

MAS[6] fields are defined in Table 3-8.

Table 3-8. MAS[6] — TLB Search Context Register 0

Field	Description
0–7	Reserved, must be cleared.
8–15 SPID	PID value for searches
16–30	Reserved, must be cleared.
31 SAS	AS value for searches

3.3.2 L1 Cache

The e200z6 processor supports a 32-KB, 4- or 8-way set-associative, unified (instruction and data) cache with a 32-byte line size. The cache improves system performance by providing low-latency data to the e200z6 instruction and data pipelines, which decouples processor performance from system memory performance. The cache is virtually indexed and physically tagged. The e200z6 does not provide hardware support for cache coherency in a multi-master environment. Software must be used to maintain cache coherency with other possible bus masters.

Both instruction and data accesses are performed using a single bus connected to the cache. Addresses from the processor to the cache are virtual addresses used to index the cache array. The MMU provides the virtual to physical translation for use in performing the cache tag compare. If the physical address matches a valid cache tag entry, the access hits in the cache. For a read operation, the cache supplies the data to the processor, and for a write operation, the data from the processor updates the cache. If the access does not match a valid cache tag entry (misses in the cache) or a write access must be written through to memory, the cache performs a bus cycle on the system bus. Figure 3-13 shows a block diagram of the unified cache in the e200z6.

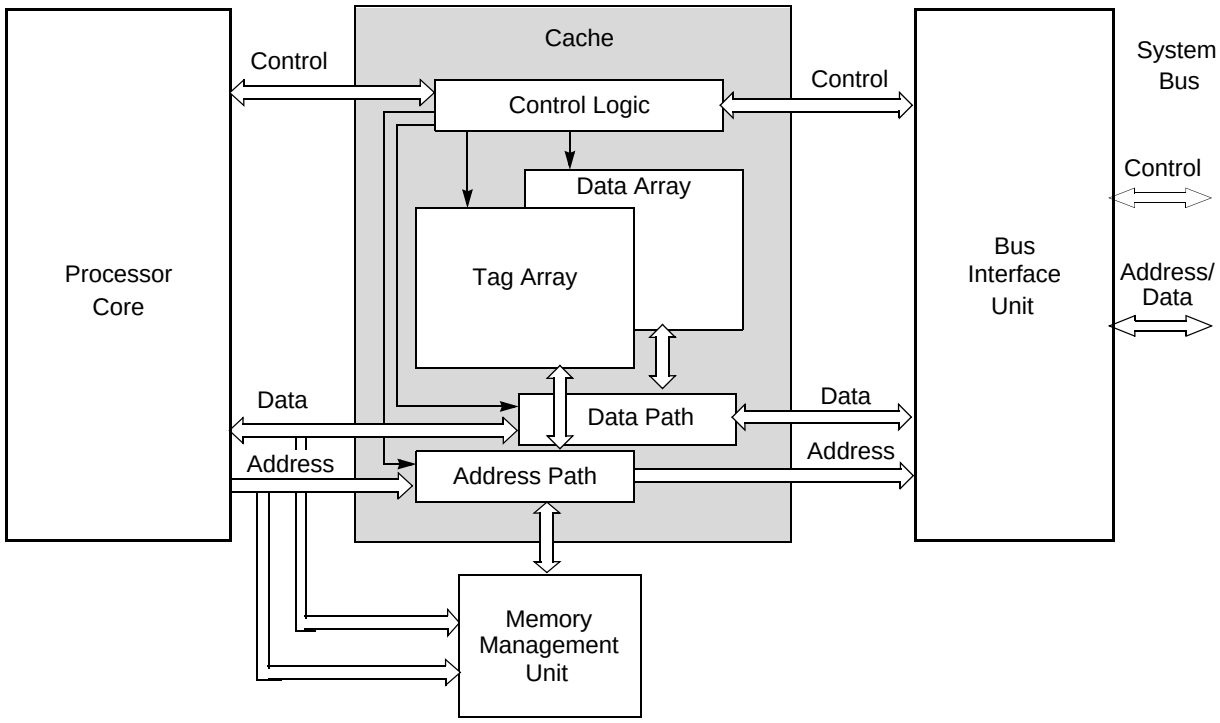


Figure 3-13. e200z6 Unified Cache Block Diagram

3.3.2.1 Cache Organization

The e200z6 cache is organized as 4 or 8 ways of 128 sets with each line containing 32 bytes (four doublewords) plus parity of storage. Figure 3-14 illustrates the cache organization, terminology used, the cache line format, and cache tag formats.

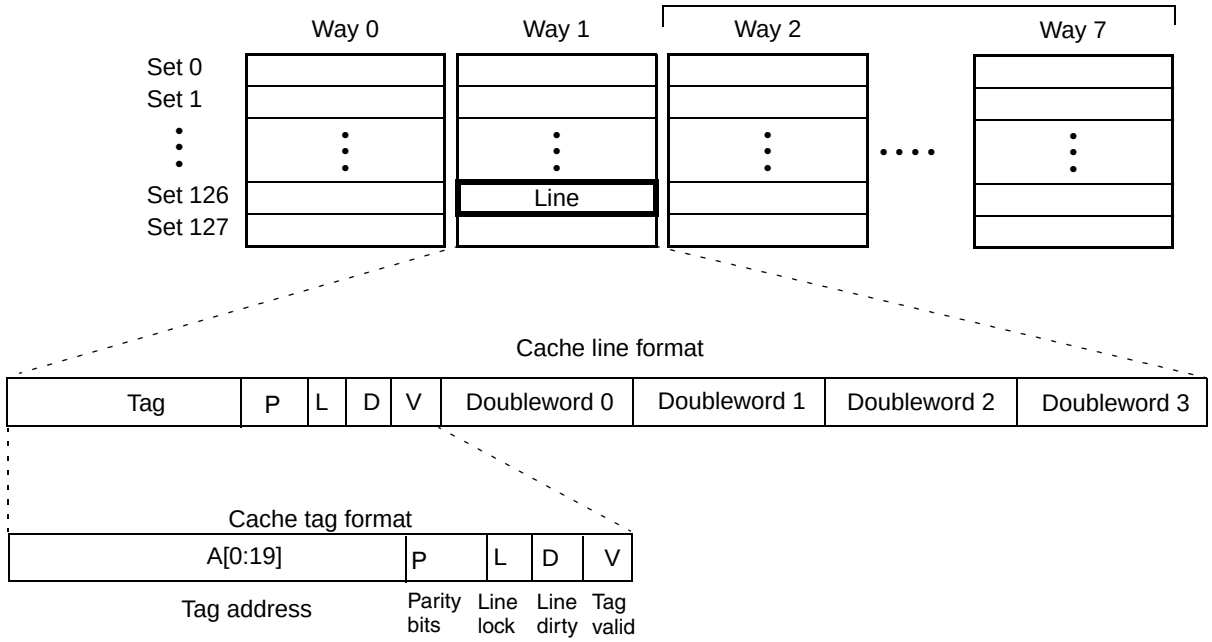


Figure 3-14. Cache Organization and Line Format

3.3.2.2 Cache Lookup

After it is enabled, the unified cache is searched for a tag match on all instruction fetches and data accesses from the CPU. If a match is found, the cached data is forwarded on a read access to the instruction fetch unit or the load/store unit (data access), or is updated on a write access, and can also be written-through to memory if required.

When a read miss occurs, if there is a TLB hit and the cache inhibit bit (WIMGE=0bx0xxx) of the hitting TLB entry is clear, the translated physical address is used to fetch a four doubleword cache line beginning with the requested doubleword (critical doubleword first). The line is fetched and placed into the appropriate cache block and the critical doubleword is forwarded to the CPU. Subsequent doublewords can be streamed to the CPU if they have been requested and streaming is enabled via the DSTRM bit in the L1CSR0 register.

During a cache line fill, doublewords received from the bus are placed into a cache linefill buffer, and can be forwarded (streamed) to the CPU if such a request is pending. Accesses from the CPU following delivery of the critical doubleword can be satisfied from the cache (hit under fill, non-blocking) or from the linefill buffer if the requested information has been already received.

The cache always fills an entire line, thereby providing validity on a line-by-line basis. A cache line is always in one of the following states: invalid, valid, or dirty (and valid). For invalid lines, the V bit is clear, causing the cache line to be ignored during lookups. Valid lines have their V bit set and D bit cleared,

indicating the line contains valid data consistent with memory. Dirty cache lines have the D and V bits set, indicating that the line has valid entries that have not been written to memory. In addition, a cache line can be locked (L bit set) indicating the line is not available for replacement.

The cache must be invalidated after a hardware reset; a hardware reset does not invalidate the cache lines. Following initial power-up, the cache contents are undefined. If the L, D, or V bits are set on any lines, the software must invalidate cache before the cache is enabled.

Figure 3-15 illustrates the general flow of cache operation.

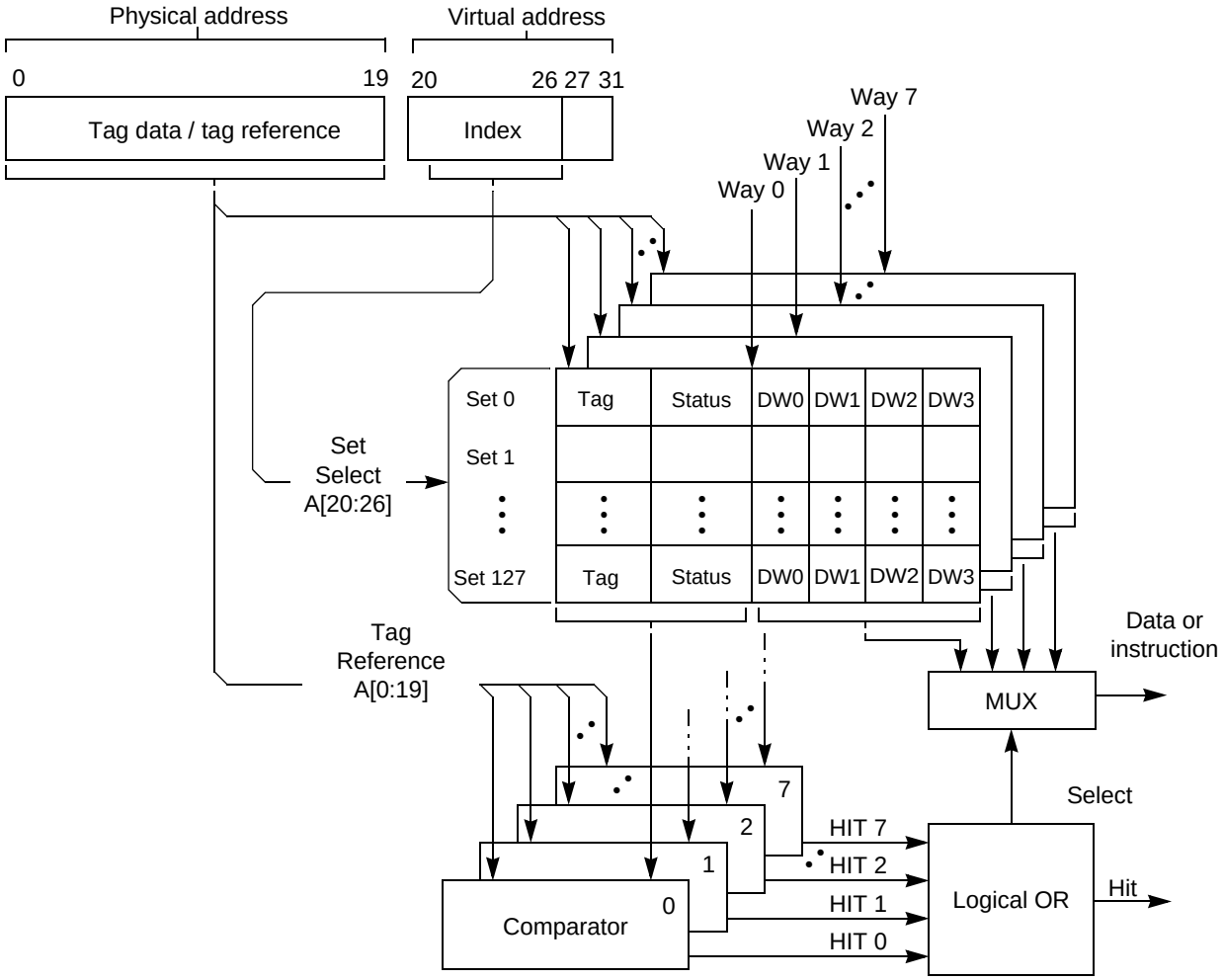


Figure 3-15. Cache Lookup Flow

To determine if the address is already allocated in the cache the following steps are taken:

1. The cache set index, virtual address bits A[20:26] are used to select one cache set. A set is defined as the grouping of four or eight lines (one from each way), corresponding to the same index into the cache array.
2. The higher order physical address bits A[0:19] are used as a tag reference or used to update the cache line tag field.
3. The four or eight tags from the selected cache set are compared with the tag reference. If any one of the tags matches the tag reference and the tag status is valid, a cache hit has occurred.
4. Virtual address bits A[27:28] are used to select one of the four doublewords in each line. A cache hit indicates that the selected doubleword in that cache line contains valid data (for a read access), or can be written with new data depending on the status of the W access control bit from the MMU (for a write access).

3.3.2.3 Cache Line Replacement Algorithm

On a cache read miss, the cache controller uses a pseudo-round-robin replacement algorithm to determine which cache line will be selected to be replaced. There is a single replacement counter for the entire cache. The replacement algorithm acts as follows: on a miss, if the replacement pointer is pointing to a way which is not enabled for replacement by the type of the miss access (the selected line or way is locked), it is incremented until an available way is selected (if any). After a cache line is successfully filled without error, the replacement pointer increments to point to the next cache way.

3.3.2.4 Cache Power Reduction

The device provides additional user control over cache power utilization via the L1CSR0[WID], [AWID], [WDD], and [AWDD] way disable bits and the L1CSR0[WAM] control bit. When WAM is set to 1, ways that are disabled for allocation on miss by a particular access type (instruction or data) via the L1CSR0[WID], [AWID], [WDD], and [AWDD] way disable bits are also disabled (not selected) during normal cache lookup operations, thus avoiding the power associated with reading tag and data information for a disabled way. This provides the capability of disabling some ways for instruction accesses and some ways for data accesses to reduce power. In doing so however, certain restrictions must be followed, and the ability to lock by way is no longer functional, since a locked way would never be accessed.

When setting WAM to 1, restrictions are required to avoid coherency issues between instruction and data accesses, and to avoid multiple ways hitting on a given access. The restriction on coherency is due to the fact that a given line could possibly be present twice in the cache; a copy in a way disabled for instruction access which can be read and written by data accesses, and a second copy in a way disabled for data access which can be executed via an instruction fetch. A data write to the line will result in the possibility of instruction fetches obtaining stale data, in the same manner as exists in a non-unified cache. Another restriction is that multiple hits to the same line must be avoided on any given instruction or data access. This must be avoided by controlling the ways via the L1CSR0[WID,] [WDD], [AWID], and [AWDD] bits such that no common way exists that can be accessed by both instructions and data, or by ensuring that MMU permissions are set so that no cacheable page has X (execute) permission which also has R (read) or W (write) permission, i.e. can be cacheable and accessed with both instruction and data accesses.

When WAM is set to 1, ways disabled for instruction access are not affected by the **icbt**, **icblc**, **icbtls**, and **icbi** instructions. Ways disabled for data accesses are not affected by the **dcba**, **dcbf**, **dcbi**, **dcblc**, **dcbst**, **dcbt**, **dcbtls**, **dcbtst**, **dcbtstls**, and **dcbz** instructions. Cache control operations using L1CSR0[CINV] and L1FINV0 operations are not affected by the WAM setting and proceed normally.

3.3.2.5 L1 Cache Control and Status Register 0 (L1CSR0)

The L1 cache control and status register 0 (L1CSR0) is a 32-bit register. The L1CSR0 register is accessed using a **mfspr** or **mtspr** instruction. The SPR number for L1CSR0 is 1010 in decimal. The L1CSR0 register is shown in Figure 3-16. The correct sequence necessary to change the value of LSCSR0 is:

1. **msync**
2. **isync**
3. **mtspr** L1CSR0

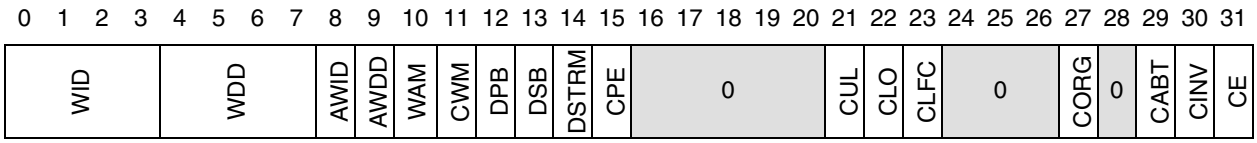


Figure 3-16. L1 Cache Control and Status Register 0 (L1CSR0)

The L1CSR0 bits are described in Table 3-9.

Table 3-9. L1CSR0 Field Descriptions

Bits	Name	Description
0:3	WID	Way instruction disable. 0 = The corresponding way is available for replacement by instruction miss line fills. 1 = The corresponding way is not available for replacement by instruction miss line fills. Bit 0 corresponds to way 0. Bit 1 corresponds to way 1. Bit 2 corresponds to way 2. Bit 3 corresponds to way 3. The WID and WDD bits can be used for locking ways of the cache, and also are used in determining the replacement policy of the cache.

Table 3-9. L1CSR0 Field Descriptions (continued)

Bits	Name	Description
4:7	WDD	Way data disable. 0 = The corresponding way is available for replacement by data miss line fills. 1 = The corresponding way is not available for replacement by data miss line fills. Bit 4 corresponds to way 0. Bit 5 corresponds to way 1. Bit 6 corresponds to way 2. Bit 7 corresponds to way 3. The WID and WDD bits can be used for locking ways of the cache, and also are used in determining the replacement policy of the cache.
8	AWID	Additional ways instruction disable. 0 = Additional ways beyond 0–3 are available for replacement by instruction miss line fills. 1 = Additional ways beyond 0–3 are not available for replacement by instruction miss line fills. For the 32KB 8-way cache, ways 4–7 are considered additional ways. When configured as a 4-way cache, this bit is ignored.
9	AWDD	Additional ways data disable. 0 = Additional ways beyond 0–3 are available for replacement by data miss line fills. 1 = Additional ways beyond 0–3 are not available for replacement by data miss line fills. For the 32KB 8-way cache, ways 4–7 are considered additional ways. When configured as a 4-way cache, this bit is ignored.
10	WAM	Way access mode 0 = Disable way access is checked not enabled for replacement on an access type are still checked for a cache hit for accesses of that type but are not replaced by an access miss of that type. 1 = Ways not enabled for replacement on a particular access type (instruction vs. data) via the AWID, WID, AWDD, and WDD fields are disabled and no lookup is performed for accesses of that type. Selecting WAM = 1 helps minimize power consumption. Software *must* ensure that the instruction to data coherency is maintained when using the power-saving feature of the WAM control. Cache must be invalidated prior to changing the value of this bit. Use of a dcbf followed by an icbi, msync, isync for modified lines which can be executed is required to maintain proper operation.
11	CWM	Cache write mode 0 = Cache operates in writethrough mode 1 = Cache operates in copyback mode When set to writethrough mode, the “W” page attribute from an optional MMU is ignored and all writes are treated as writethrough required. When set, write accesses are performed in copyback mode unless the “W” page attribute from an optional MMU is set.
12	DPB	Disable push buffer 0 = Push buffer enabled 1 = Push buffer disabled

Table 3-9. L1CSR0 Field Descriptions (continued)

Bits	Name	Description
13	DSB	Disable store buffer 0 = store buffer enabled 1 = store buffer disabled
14	DSTRM	Disable streaming 0 = streaming is enabled 1 = streaming is disabled
15	CPE	Cache parity enable 0 = parity checking is disabled 1 = parity checking is enabled
16–20	—	Reserved
21	CUL	Cache unable to lock Indicates a lock set instruction was not effective in locking a cache line. This bit is set by hardware on an “unable to lock” condition (other than lock overflows), and will remain set until cleared by software writing 0 to this bit location.
22	CLO	Cache lock overflow Indicates a lock overflow (overlocking) condition occurred. This bit is set by hardware on an “overlocking” condition, and will remain set until cleared by software writing 0 to this bit location.
23	CLFC	Cache lock bits flash clear When written to a 1, a cache lock bit flash clear operation is initiated by hardware. After this is complete, this bit is reset to 0. Writing a 1 during a flash clear operation results in an undefined operation. Writing a 0 during a flash clear operation is ignored. Cache lock bits flash clear operations require approximately 134 cycles to complete. Clearing occurs regardless of the enable (CE) value.
24–26	—	Reserved
27	CORG	Cache organization 0 = The cache is organized as 128 sets and 8 ways 1 = The cache is organized as 256 sets and 4 ways. Selecting CORG = 1 helps minimize power consumption.
28	—	Reserved
29	CABT	Cache operation aborted Indicates a cache invalidate or a cache lock bits flash clear operation was aborted prior to completion. This bit is set by hardware on an aborted condition, and will remain set until cleared by software writing 0 to this bit location.
30	CINV	Cache invalidate 0 = No cache invalidate 1 = Cache invalidation operation When written to a 1, a cache invalidation operation is initiated by hardware. After this is complete, this bit is reset to 0. Writing a 1 while an invalidation operation is in progress will result in an undefined operation. Writing a 0 to this bit while an invalidation operation is in progress will be ignored. Cache invalidation operations require approximately134 cycles to complete. Invalidation occurs regardless of the enable (CE) value.

Table 3-9. L1CSR0 Field Descriptions (continued)

Bits	Name	Description
31	CE	Cache Enable 0 = Cache is disabled 1 = Cache is enabled When disabled, cache lookups are not performed for normal load or store accesses. Other L1CSR0 cache control operations are still available. Also, operation of the store buffer is not affected by CE.

3.3.2.6 L1 Cache Configuration Register 0 (L1CFG0)

The L1 cache configuration register 0 (L1CFG0) is a 32-bit read-only register. L1CFG0 provides information about the configuration of the Z650n3 L1 cache design. The contents of the L1CFG0 register can be read using a **mfspr** instruction. The SPR number for L1CFG0 is 515 in decimal. The L1CFG0 register is shown in Figure 3-17.

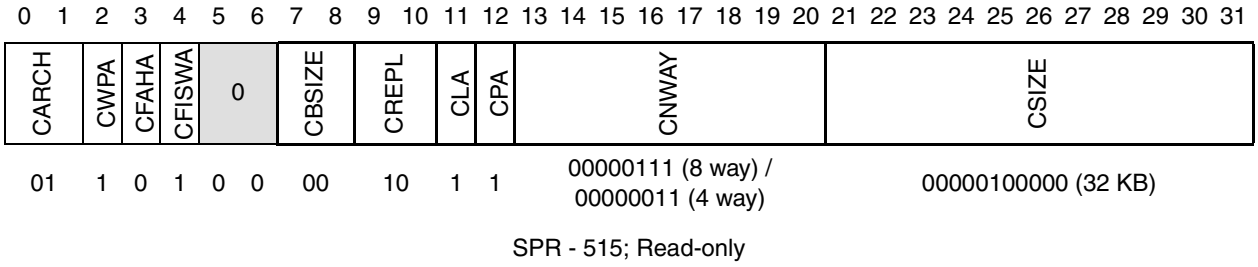


Figure 3-17. L1 Cache Configuration Register 0 (L1CFG0)

The L1CFG0 bits are described in Table 3-10.

Table 3-10. L1CFG0 Field Descriptions

Bits	Name	Description
0–1	CARCH	Cache architecture 01 - The cache architecture is unified
2	CWPA	Cache way partitioning available 1 - The cache supports partitioning of way availability for I/D accesses
3	CFAHA	Cache flush all by hardware available 0 - The cache does not support flush all in hardware
4	CFISWA	Cache flush/invalidate by set and way available 1 - The cache supports flushing/invalidation by set and way via the L1FINV0 spr
5–6	—	Reserved—read as zeros
7–8	CBSIZE	Cache block size 00 - The cache implements a block size of 32 bytes
9–10	CREPL	Cache replacement policy 10 - The cache implements a pseudo-round-robin replacement policy
11	CLA	Cache locking APU available 1 - The cache implements the line locking APU

Table 3-10. L1CFG0 Field Descriptions (continued)

Bits	Name	Description
12	CPA	Cache parity available 1 - The cache implements parity
13:20	CNWAY	Number of ways in the data cache 0x03 - The cache is 4-way set-associative 0x07 - The cache is 8-way set-associative **Note:** CNWAY shows the current cache organization as set by L1CSR0[CORG].
21:31	CSIZE	Cache size 0x020 - The size of the cache is 32 KB

3.3.3 Interrupt Types

The interrupts implemented in the device and the exception conditions that cause them are listed in Table 3-11.

Table 3-11. Interrupts and Conditions

Interrupt Type	Interrupt Vector Offset Register	Enables[1]	Core Register in Which State Information is Saved	Causing Conditions
System reset	none, vector to 0xFFFF_FFFC			• Reset by assertion of $\overline{\text{RESET}}$ • Watchdog timer reset control • Debug reset control
Critical input	IVOR 0	IVOR 0 is not supported in the device		
Machine check	IVOR 1	ME	CSSR[0:1]	Machine check conditions: • Machine check exception (p_mcp_b) asserts and MSR[ME] = 1. • ISI, ITLB error occurred on: the first instruction fetch for the exception handler, and the current MSR[ME] = 1. • Parity error detected on the cache access and the current MSR[ME] = 1. • Write bus error occurred on: a buffered store or cache-line push; and the current MSR[ME] = 1. • Bus error (XTE) with MSR[EE] = 0 and current MSR[ME] = 1.
Data storage	IVOR 2	—	SRR[0:1]	Data storage conditions: • Access control • Byte ordering error from a misaligned access across a page boundary to a page with mismatched E bits • Cache locking exception • Precise external termination error and the current MSR[ME] = 1.

Table 3-11. Interrupts and Conditions (continued)

Interrupt Type	Interrupt Vector Offset Register	Enables[1]	Core Register in Which State Information is Saved	Causing Conditions

Instruction storage	IVOR 3	—	SRR[0:1]	• Access control.
				• Precise external termination error and MSR[EE] = 1.
				• Byte ordering interrupt due to:
				  • misaligned access across page boundary to pages with mismatched VLE bits
				  • access to pages with VLE set
				with E indicating little-endian.
				• Misaligned instruction fetch interrupt when a flow changes to an odd-halfword instruction boundary on a Book E (non-VLE) instruction page, generated by the value of the LR, CTR, or SRR0s field.

External input	IVOR 4 [2]	EE, src	SRR[0:1]	External interrupt is asserted and MSR[EE]=1
Alignment	IVOR 5	—	SRR[0:1]	• **lmw**, **stmw** not word aligned • **lwarx** or **stwcx.** not word aligned • **dcbz** with disabled cache or no cache present, or to W or I storage • SPE ID and ST instructions misaligned
Program	IVOR 6	—	SRR[0:1]	Illegal, privileged, trap, FP enabled, AP enabled, unimplemented operation
Floating-point unavailable	IVOR 7	—	SRR[0:1]	MSR[FP]=0 and attempt to execute a Book E floating point operation
System call	IVOR 8	—	SRR[0:1]	Execution of the system call (**sc**) instruction
AP unavailable	IVOR 9	—	SRR[0:1]	Unused by e200z6.
Decrementer	IVOR 10	EE, DIE	SRR[0:1]	Decrementer timeout, and as specified in *Book E: Enhanced PowerPC™ Architecture, Rev 1.0*, Ch. 8, pg. 194–195 and in the *e200Z6 PowerPC™ Core Reference Manual,* Rev 0.
Fixed interval timer	IVOR 11	EE, FIE	SRR[0:1]	Fixed-interval timer timeout and as specified in *Book E: Enhanced PowerPC™ Architecture, Rev 1.0*, Ch. 8, pg. 195–196 and in the *e200Z6 PowerPC™ Core Reference Manual,* Rev 0.
Watchdog timer	IVOR 12	CE, WIE	CSRR[0:1]	Watchdog timeout: as specified in *Book E: Enhanced PowerPC™ Architecture, Rev 1.0*, Ch. 8, pg. 196–197 and in the *e200Z6 PowerPC™ Core Reference Manual,* Rev 0.
Data TLB error	IVOR 13	—	SRR[0:1]	Data translation lookup did not match a valid entry in the TLB
Instruction TLB error	IVOR 14	—	SRR[0:1]	Instruction translation lookup did not match a valid TLB entry

Table 3-11. Interrupts and Conditions (continued)

Interrupt Type	Interrupt Vector Offset Register	Enables[1]	Core Register in Which State Information is Saved	Causing Conditions
Debug	IVOR 15	DE, IDM	CSSR[0:1]	Debugger when HIDO[DAPUEN] = 0. Caused by trap, instruction address compare, data address compare, instruction complete, branch taken, return from interrupt, interrupt taken, debug counter, external debug event, unconditional debug event
		DE, IDM	DSRR[0:1]	Debugger when HIDO[DAPUEN] = 1, and caused by same conditions as above.
Reserved	IVOR 16–31			
SPE unavailable exception	IVOR 32	—	SRR[0:1]	SPE APU instruction when MSR[SPE] = 0, and see Section 5.6.18 “SPE APU Unavailable Interrupt” in the *e200Z6 PowerPC™ Core Reference Manual,* Rev 0.
SPE data exception	IVOR 33	—	SRR[0:1]	SPE FP data exception and see Section 5.6.19 “SPE Floating-Point Data Interrupt” in the *e200Z6 PowerPC™ Core Reference Manual,* Rev 0.
SPE round exception	IVOR 34	—	SRR[0:1]	Inexact result from floating-point instruction. See Section 5.6.20 “SPE Floating-Point Round Interrupt” in the *e200Z6 PowerPC™ Core Reference Manual,* Rev 0.

[1] CE, ME, EE, DE are in the MSR. DIE, FIE, and WIE are in the TCR. “src” signifies the individual enable for each INTC source. The debug interrupt, IVOR 15, also requires EDM = 0 (EDM and IDM are in the DBCR0 register).

3.3.4 Bus Interface Unit (BIU)

The BIU encompasses control and data signals supporting instruction and data transfers. A data bus width of 64-bits is implemented. The memory interface supports read and write transfers of 8, 16, 24, 32, and 64 bits, supports burst transfers of four doublewords, and operates in a pipelined fashion.

Single-beat transfers are supported for cache-inhibited read and write cycles, and write-buffer writes. Burst transfers of four doublewords are supported for cache linefill and copyback operations.

3.3.5 Timer Facilities

The core provides a set of registers to provide fixed interval timing and watchdog functions for the system. All of these must be initialized during start-up. The registers associated with fixed interval timer and watchdog functions are the following:

- Timer control register (TCR)—provides control of the timer and watchdog facilities.
- Timer status register (TSR)—provides status of the timer facilities.
- Time base registers (TBU and TBL)—two 32-bit registers (upper and lower) that are concatenated to provide a long-period, 64-bit counter.

- Decrementer register (DEC)—a decrementing counter that is updated at the same rate as the time base. The DEC provides a means of signaling an exception after a specified amount of time. The DEC is typically used as a general-purpose software timer. Note that the decrementer always runs when the system is clocked, and can be written to by software at any time.
- Decrementer auto reload register (DECAR)—provides a value that is automatically reloaded (if enabled) into the decrementer register when the decrementer reaches 0.

For more information on the fixed-interval timer, watchdog timer, and timer and counter registers, refer to the *e200z6 PowerPC™ Core Reference Manual* and *EREF: A Programmer's Reference Manual for Freescale Book E Processors.*

3.3.6 Signal Processing Extension APU (SPE APU)

The Power Architecture embedded category 32-bit instructions operate on the lower (least significant) 32 bits of the 64-bit GPRs. New SPE instructions are defined that view the 64-bit register as being composed of a vector of two 32-bit elements, and some of the instructions also read or write 16-bit elements. These new instructions can also be used to perform scalar operations by ignoring the results of the upper 32-bit half of the register file.

Some instructions are defined that produce a 64-bit scalar result. Vector fixed-point instructions operate on a vector of two 32-bit or four 16-bit fixed-point numbers resident in the 64-bit GPRs. Vector floating-point instructions operate on a vector of two 32-bit single-precision floating-point numbers resident in the 64-bit GPRs. Scalar floating-point instructions operate on the lower half of GPRs. These single-precision floating-point instructions do not have a separate register file; there is a single shared register file for all instructions. Figure 3-18 shows two different representations of the 64-bit GPRs. The shaded half is the only region operated on by the 32-bit Power Architecture embedded category instructions.

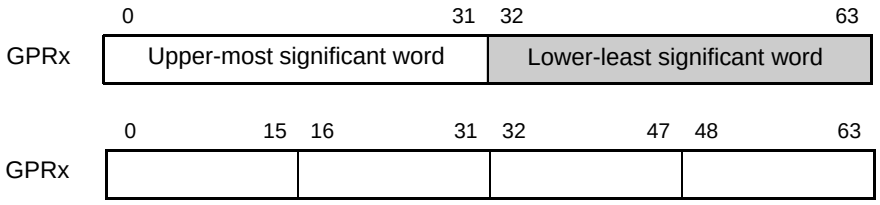


Figure 3-18. 64-bit General-Purpose Registers

3.3.7 SPE Programming Model

Not all SPE instructions record events such as overflow, saturation, and negative/positive result. See the description of the individual SPE instruction in the e200z6 core reference for information on which conditions are recorded and where they are recorded. Most SPE instructions record conditions to the SPEFSCR. Vector compare instructions store the result of the comparison into the condition register (CR).

The e200z6 core has a 64-bit architectural accumulator register that holds the results of the SPE multiply accumulate (MAC) fixed-point instructions. The accumulator allows back-to-back execution of dependent fixed-point MAC instructions, something that is found in the inner loops of DSP code such as filters. The

accumulator is partially visible to the programmer in that its results do not have to be explicitly read to use them. Instead, they are always copied into a 64-bit destination GPR specified as part of the instruction. The accumulator however, has to be explicitly cleared when starting a new MAC loop. Based on the type of instruction, the accumulator can hold either a single 64-bit value or a vector of two 32-bit elements.

3.4 External References

In addition to the Power Architecture instructions, the device supports e200z6 core-specific instructions and SPE APU instructions and VLE instructions. For further information see the following documents:

- *e200z6 PowerPC™ Core Reference Manual*
- *PowerPC™ Microprocessor Family: The Programming Environment for 32-bit Microprocessors*
- *Book E: Enhanced PowerPC™ Architecture*
- *EREF: A Programmer's Reference Manual for Freescale Book E Processors*
- *VLEPIM: Variable Length Encoding (VLE) Extension Programming Interface Manual*
- *Addendum to e200z6 PowerPC™ Core Reference Manual: e200z6 with VLE*
- *Errata to e200z6 PowerPC™ Core Reference Manual, Rev. 0*

3.5 Power Architecture Instruction Extensions – VLE

The variable length encoding (VLE) provides an extension to 32-bit Power Architecture. There are additional operations defined using an alternate instruction encoding to enable reduced code footprint. This alternate encoding set is selected on an instruction page basis. A single page attribute bit selects between standard Power Architecture instruction encodings and VLE instructions for that page of memory. This page attribute is an extension to the Power Architecture page attributes. Pages can be freely intermixed, allowing for a mixture of code using both types of encodings.

Instruction encodings in pages marked as using the VLE extension are either 16 or 32 bits long, and are aligned on 16-bit boundaries. Therefore, all instruction pages marked as VLE are required to use big-endian byte ordering.

This section describes the various extensions to the Power Architecture instructions that support the VLE extension.

rfci, **rfdi**, **rfi**	Not the mask bit 62 of CSRR0, DSRR0, or SRR0 respectively. The destination address is [D,C]SRR0[32:62] || 0b0.
bclr, **bclrl**, **bcctr**, **bcctrl**	Not the mask bit 62 of the LR or CTR respectively. The destination address is [LR,CTR][32:62] || 0b0.

Chapter 4
Reset

4.1 Introduction

The following reset sources are supported in this MCU:

- Power-on reset
- External reset
- Loss-of-lock reset
- Loss-of-clock reset
- Watchdog timer/debug reset
- JTAG reset
- Checkstop reset
- Software system reset
- Software external reset

All reset sources are processed by the reset controller, which is located in the SIU module. The reset controller monitors the reset input sources, and upon detection of a reset event, resets internal logic and controls the assertion of the $\overline{\text{RSTOUT}}$ pin. The $\overline{\text{RSTOUT}}$ signal may be automatically asserted by writing the SER bit in the SIU_SRCR to 1. The $\overline{\text{RSTOUT}}$ signal stays asserted for a number of system clocks[1] determined by the configuration of the PLL. This does not reset the MCU. All other reset sources initiate an internal reset of the MCU.

Refer to Section 4.2.2, “Reset Output (RSTOUT)”.

For all reset sources, the BOOTCFG[0:1] and PLLCFG[0:1] signals can be used to determine the boot mode and the configuration of the FMPLL, respectively. If the $\overline{\text{RSTCFG}}$ pin is asserted during reset, the values on the BOOTCFG[0:1] pins are latched in the SIU_RSR 4 clock cycles prior to the negation of the $\overline{\text{RSTOUT}}$ pin, determining the boot mode. The values on the PLLCFG[0:1] pins are latched at the negation of the $\overline{\text{RSTOUT}}$ pin, determining the configuration of the FMPLL. If the $\overline{\text{RSTCFG}}$ pin is negated during reset, the FMPLL defaults to normal operation (PLL enabled) with a crystal reference and the boot mode (latched in the SIU_RSR) is defaulted to internal boot from flash.

The reset status register (SIU_RSR) gives the source of the last reset and indicates whether a glitch has occurred on the $\overline{\text{RESET}}$ pin. The SIU_RSR is updated for all reset sources except the JTAG reset.

All reset sources initiate execution of the MCU boot assist module (BAM) program with the exception of the software external reset.

1. Unless noted otherwise, the use of ‘clock’ or ‘clocks’ in this section is a reference to the system clock.

The reset configuration halfword (RCHW) provides several basic functions at reset. It provides a means to locate the boot code, determines if flash memory is programmed or erased, enables or disables the watchdog timer, configures the MMU to boot as either classic Power Architecture Book E code or as Freescale VLE code, and if booting externally, sets the bus size. The location of the RCHW is specified by the state of the BOOTCFG[0:1] pins. These pins determine whether the RCHW is located in internal flash, located in external memory, or whether a serial or CAN boot is configured.

Refer to Section Chapter 2, “Signal Description” for a complete description of the BOOTCFG[0:1] pins.

The BAM program reads the values of the BOOTCFG[0:1] pins from the BOOTCFG field of the SIU_RSR, then reads the RCHW from the specified location and uses the RCHW value to determine and execute the specified boot procedure.

Refer to Section 4.4.3, “Reset Configuration and Configuration Pins,” for a complete description.

4.2 External Signal Description

4.2.1 Reset Input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ pin is an active low input that is asserted by an external device during a power-on or external reset. The internal reset signal asserts only if the $\overline{\text{RESET}}$ pin is asserted for 10 clock cycles. Assertion of the $\overline{\text{RESET}}$ pin while the device is in reset causes the reset cycle to start over. The $\overline{\text{RESET}}$ pin also has an associated glitch detector which detects spikes greater than two clocks in duration that fall below the switch point of the input buffer logic.

Refer to Section 6.4.2.1, “RESET Pin Glitch Detect.”

4.2.2 Reset Output ($\overline{\text{RSTOUT}}$)

The $\overline{\text{RSTOUT}}$ pin is an active low output that uses a push/pull configuration. The $\overline{\text{RSTOUT}}$ pin is driven to the low state by the MCU for all internal and external reset sources.

After the negation of the $\overline{\text{RESET}}$ input, if the PLL is configured for 1:1 (dual controller) mode or bypass mode, the $\overline{\text{RSTOUT}}$ signal is asserted for 16000 clocks, plus four clocks for sampling of the configuration pins. If the PLL is configured for any other operating mode, the $\overline{\text{RSTOUT}}$ signal is asserted for 2400 clocks, plus four clocks for sampling of the configuration pins. The $\overline{\text{RSTOUT}}$ pin is asserted by a write to the SER bit of the system reset control register (SIU_SRCR).

Refer to Section 11.1.4, “FMPLL Modes of Operation” for details of PLL configuration.

NOTE

During a power on reset, $\overline{\text{RSTOUT}}$ is tri-stated.

4.2.3 Reset Configuration ($\overline{\text{RSTCFG}}$)

The $\overline{\text{RSTCFG}}$ input is used to enable the BOOTCFG[0:1] and PLLCFG[0:1] pins during reset. If $\overline{\text{RSTCFG}}$ is negated during reset, the BOOTCFG and PLLCFG pins are not sampled at the negation of $\overline{\text{RSTOUT}}$. In that case, the default values for BOOTCFG and PLLCFG are used. If $\overline{\text{RSTCFG}}$ is asserted during reset, the values on the BOOTCFG and PLLCFG pins are sampled and configure the boot and FMPLL modes.

4.2.4 Weak Pull Configuration (WKPCFG)

WKPCFG determines whether specified eTPU and EMIOS pins are connected to a weak pullup or weak pulldown during and immediately after reset.

4.2.5 Boot Configuration (BOOTCFG[0:1])

BOOTCFG determines the function and state of the following pins after execution of the BAM reset: $\overline{\text{CS}}$[0:3], ADDR[:31], DATA[0:31], RD_$\overline{\text{WR}}$, $\overline{\text{BDIP}}$, $\overline{\text{WE}}$[0:3], $\overline{\text{OE}}$, $\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{BB}}$ and TSIZ[0:1].

Refer to the boot modes detailed in Section 6.4.1.1, “Boot Configuration” and in Table 6-144.

4.3 Memory Map/Register Definition

Table 4-1 summarizes the reset controller registers. The base address of the system integration unit is 0xC3F9_0000.

Table 4-1. Reset Controller Memory Map

Address	Register Name	Register Description	Bits
Base + 0x000C	SIU_RSR	Reset status register	32
Base + 0x0010	SIU_SRCR	System reset control register	32

4.3.1 Register Descriptions

This section describes all the reset controller registers. It includes details about the fields in each register, the number of bits per field, the reset value of the register, and the function of the register.

4.3.1.1 Reset Status Register (SIU_RSR)

The reset status register (SIU_RSR) reflects the most recent source, or sources, of reset. This register contains one bit for each reset source. A bit set to logic 1 indicates the type of reset that occurred. Simultaneous reset requests cause more than one bit to be set at the same time. After it is set, the reset source bits in the SIU_RSR remain set until another reset occurs. The SERF bit is set when a software external reset occurs, but no previously set bits in the SIU_RSR are cleared.

Refer to Section 4.3.1.1, “Reset Status Register (SIU_RSR)” for additional information.

The SIU_RSR also contains the values latched at the last reset on the WKPCFG and BOOTCFG[0:1] pins and a $\overline{\text{RESET}}$ input pin glitch flag. The reset glitch flag bit (RGF) is cleared by writing a 1 to the bit. A write of 0 has no effect on the bit state. The SIU_RSR can be read at all times.

The following figure shows the reset status register:

Address: Base + 0x000C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	PORS	ERS	LLRS	LCRS	WDRS	CRS	0	0	0	0	0	0	0	0	SSRS	SERF
W																
Reset[1]	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	WKP CFG	0	0	0	0	0	0	0	0	0	0	0	0	BOOTCFG		RGF
W																
Reset	—[2]	0	0	0	0	0	0	0	0	0	0	0	0	—[3]	—[3]	0

[1] The RESET values for this register are defined for power-on reset only.

[2] The RESET value of this bit or field is determined by the value latched on the pin or pins at the negation of the last reset.

[3] The RESET value of this bit or field is determined by the value latched on the pin or pins at the negation of the last reset. BOOTCFG can also be loaded with a default instead of what is on the pin or pins.

Figure 4-1. Reset Status Register (SIU_RSR)

The following table describes the fields in the reset status register:

Table 4-2. SIU_RSR Field Descriptions

Field	Description
0 PORS	Power-on reset status 0 No power-on reset has occurred. 1 A power-on reset has occurred.
1 ERS	External reset status 0 No external reset has occurred. 1 An external reset has occurred. The ERS bit is also set during a POR event.
2 LLRS	Loss-of-lock reset status 0 No loss-of-lock reset has occurred. 1 A loss-of-lock reset has occurred.
3 LCRS	Loss-of-clock reset status 0 No loss-of-clock reset has occurred. 1 A loss-of-clock reset has occurred due to a loss of the reference or failure of the FMPLL.
4 WDRS	Watchdog timer/debug reset status 0 No watchdog timer or debug reset occurred. 1 A watchdog timer or debug reset occurred.
5 CRS	Checkstop reset status 0 No enabled checkstop reset occurred. 1 An enabled checkstop reset occurred.
6–13	Reserved.

Table 4-2. SIU_RSR Field Descriptions (continued)

Field	Description
14 SSRS	Software system reset status 0 No software system reset occurred. 1 A software system reset occurred.
15 SERF	Software external reset flag 0 No software external reset occurred. 1 A software external reset occurred.
16 WKPCFG	Weak pull configuration pin status 0 WKPCFG pin latched during the last reset was logic 0 and weak pulldown is the default setting. 1 WKPCFG pin latched during the last reset was logic 1 and weak pullup is the default setting.
17–28	Reserved.
29–30 BOOTCFG	Reset configuration pin status. Holds the value of the BOOTCFG[0:1] pins that was latched four clocks before the last negation of the $\overline{\text{RSTOUT}}$ pin, if the $\overline{\text{RSTCFG}}$ pin was asserted. If the $\overline{\text{RSTCFG}}$ pin was negated at the last negation of $\overline{\text{RSTOUT}}$, the BOOTCFG field is set to the value 0b00. The BOOTCFG field is used by the BAM program to determine the location of the reset configuration halfword (RCHW). Refer toTable 4-10 for the RCHW location from the BOOTCFG field value.
31 RGF	$\overline{\text{RESET}}$ glitch flag. Set by the MCU when $\overline{\text{RESET}}$ asserts for more than 2 clocks clock cycles, but less than the minimum $\overline{\text{RESET}}$ assertion time of 10 consecutive clocks to cause a reset. This bit is cleared by the reset controller for a valid assertion of the $\overline{\text{RESET}}$ pin or a power-on reset or a write of 1 to the bit. 0 No glitch was detected on the $\overline{\text{RESET}}$ pin. 1 A glitch was detected on the $\overline{\text{RESET}}$ pin.

4.3.1.2 System Reset Control Register (SIU_SRCR)

The system reset control register (SIU_SRCR) allows software to generate either a software system reset or software external reset. The software system reset causes an internal reset sequence, while the software external reset only asserts the external $\overline{\text{RSTOUT}}$ signal. When written to 1, the SER bit automatically clears after a predetermined number of clock cycles. If the value of the SER bit is 1 and a 0 is written to the bit, the bit is cleared and $\overline{\text{RSTOUT}}$ negates, regardless of the number of clocks that have expired.

Refer to Section 4.2.2, “Reset Output (RSTOUT).”

The CRE bit in the SIU_SRCR allows software to enable a checkstop reset. If enabled, a checkstop reset occurs if the checkstop reset input to the reset controller is asserted. The checkstop reset is enabled by default.

Address: Base + 0x0010 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	SSR	SER	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1[1]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[1] The CRE bit is reset to 1 by POR. Other resets sources do not reset the bit value.

Figure 4-2. System Reset Control Register (SIU_SRCR)

The following table describes the fields in the system reset control register (SIU_SRCR):

Table 4-3. SIU_SRCR Field Descriptions

Field	Description
0 SSR	Software system reset. Writing a 1 to this bit causes an internal reset and assertion of the $\overline{\text{RSTOUT}}$ pin. The bit is automatically cleared by all reset sources except the software external reset. 0 Do not generate a software system reset. 1 Generate a software system reset.
1 SER	Software external reset. Writing a 1 to this bit causes an software external reset. The $\overline{\text{RSTOUT}}$ pin is asserted for a predetermined number of clock cycles (Refer to Section 4.2.2, "Reset Output (RSTOUT)"), but the MCU is not reset. The bit is automatically cleared when the software external reset completes. 0 Do not generate an software external reset. 1 Generate an software external reset.
2–15	Reserved.
16 CRE	Checkstop reset enable Writing a 1 to this bit enables a checkstop reset when the e200z6 core enters a checkstop state. The CRE bit defaults to checkstop reset enabled. This bit is reset at POR. 0 No reset occurs when the e200z6 core enters a checkstop state. 1 A reset occurs when the e200z6 core enters a checkstop state.
17–31	Reserved.

4.4 Functional Description

4.4.1 Reset Vector Locations

The reset vector contains a pointer to the instruction where code execution begins after BAM execution. The address of the reset vector is specified by the boot mode, as listed in Table 4-4.

Table 4-4. Reset Vector Locations

Boot Mode	Reset Vector Location
External Boot	0x0000_0004 (0x0000_0000 is a valid RCHW)
Internal Boot	Next word address after the first valid RCHW located. The BAM searches the lowest address of each of the six low address space blocks in flash memory for a valid RCHW. Hence, the available reset vector addresses are: 0x0000_0004 0x0000_4004 0x0001_0004 0x0001_C004 0x0002_0004 0x0003_0004
Serial Boot	Specified over serial download

4.4.2 Reset Sources

4.4.2.1 FMPLL Lock

A loss of lock of the FMPLL can cause a reset (provided the SIU is enabled by the FMPLL_SYNCR[LOLRE] bit). Furthermore, reset remains asserted, regardless of the reset source, until after the FMPLL locks.

4.4.2.2 Flash High Voltage

There is no flash access gating signal implemented in this device. However, the device is held in reset for a long enough period of time to guarantee that high voltage circuits are reset and stabilized and that flash memory is accessible.

4.4.2.3 Reset Source Descriptions

For the following reset source descriptions refer to the reset flow diagrams in Figure 4-5 and Figure 4-6. Figure 4-5 shows the reset flow when $\overline{\text{RESET}}$ asserts. Figure 4-6 shows the internal reset processing for all reset sources.

4.4.2.3.1 Power-on Reset

The power-on reset (POR) circuit is designed to detect a POR event and ensure that the $\overline{\text{RESET}}$ signal is correctly sensed. The POR is not designed to detect falling power supply voltages. Provide monitoring for external supply. The output signals from the power-on reset circuits are active low signals. All power-on reset output signals are combined into one POR signal at the V_{DD} level and input to the reset controller. Although assertion of the power-on reset signal causes reset, the $\overline{\text{RESET}}$ pin must be asserted during a power-on reset to guarantee proper operation of the MCU.

The PLLCFG[0:1] and $\overline{\text{RSTCFG}}$ pins determine the configuration of the FMPLL. If the $\overline{\text{RSTCFG}}$ pin is asserted at the negation of $\overline{\text{RSTOUT}}$, the PLLCFG[0:1] pins set the operating mode of the FMPLL. If $\overline{\text{RSTCFG}}$ is asserted anytime during the assertion of $\overline{\text{RSTOUT}}$, the FMPLL switches to the mode specified by the PLLCFG[0:1] pins. The values on the $\overline{\text{RSTCFG}}$ and the PLLCFG[0:1] pins must be kept constant after $\overline{\text{RSTCFG}}$ is asserted to avoid transient mode changes in the FMPLL. If $\overline{\text{RSTCFG}}$ is in the negated state at the negation of $\overline{\text{RSTOUT}}$, the FMPLL defaults to enabled with a crystal reference.

Refer to Chapter 11, “Frequency Modulated Phase Locked Loop and System Clocks (FMPLL),” for more details on the operation of the FMPLL and the PLLCFG[0:1] pins.

The signal on the WKPCFG pin determines whether weak pullup or pulldown devices are enabled after reset on the eTPU and eMIOS pins. The WKPCFG pin is applied starting at the assertion of the internal reset signal, as indicated by the assertion of $\overline{\text{RSTOUT}}$.

Refer to Figure 4-4 and see Chapter 2, “Signal Description,” for information on WKPCFG and $\overline{\text{RSTOUT}}$.

After the $\overline{\text{RESET}}$ input pin is negated, the reset controller checks if the FMPLL is locked. The internal reset signal and $\overline{\text{RSTOUT}}$ are kept asserted until the FMPLL is locked. After the FMPLL is locked, the reset controller waits an additional predetermined number of clock cycles before negating the $\overline{\text{RSTOUT}}$ pin. The WKPCFG and BOOTCFG[0:1] pins are sampled 4 clock cycles before the negation of $\overline{\text{RSTOUT}}$,

and the associated bits/fields are updated in the SIU_RSR (the BOOTCFG[0:1] pins are only sampled if RSTCFG asserts). In addition, the PORS and ERS bits are set, and all other reset status bits are cleared in the reset status register.

Refer to Section 4.2.2, “Reset Output (RSTOUT).”

4.4.2.3.2 External Reset

When the reset controller detects assertion of the RESET pin, the internal reset signal and the RSTOUT signal are asserted.

1. Starting when the internal reset signal asserts, as indicated by RSTOUT asserting, the value on the WKPCFG pin is applied. At the same time, the PLLCFG[0:1] values are applied only if RSTCFG asserts.
2. After the RESET signal negates and the FMPLL loss-of-lock request negates, the reset controller waits the predetermined number of clock cycles. After the clock count finishes, WKPCFG and BOOTCFG[0:1] are sampled. BOOTCFG[0:1] is only sampled if RSTCFG asserts.
3. The reset controller then waits four clock cycles before the negating RSTOUT, and updating the fields in the SIU_RSR. The ERS bit is set, and all other reset status bits in the SIU_RSR are cleared.

Refer to Section 4.2.2, “Reset Output (RSTOUT)”.

4.4.2.3.3 Loss-of-Lock Reset

A loss-of-lock reset occurs when the FMPLL loses lock and the loss-of-lock reset enable (LOLRE) bit in the FMPLL synthesizer control register (FMPLL_SYNCR) is set.

1. Starting when the internal reset signal asserts, as indicated by RSTOUT asserting, the value on the WKPCFG pin is applied. At the same time, the PLLCFG[0:1] values are applied only if RSTCFG asserts.
2. After the FMPLL locks, the reset controller waits the predetermined clock count and then samples WKPCFG and BOOTCFG[0:1]. BOOTCFG[0:1] is only sampled if RSTCFG asserts.
3. The reset controller then waits four clock cycles before negating RSTOUT and updating the register fields in the SIU_RSR. The LLRS bit is set, and all other reset status bits in the SIU_RSR are cleared.

Refer to Section 4.2.2, “Reset Output (RSTOUT)”

Refer to Chapter 11, “Frequency Modulated Phase Locked Loop and System Clocks (FMPLL),” for more information on loss-of-lock.

4.4.2.3.4 Loss-of-Clock Reset

A loss-of-clock reset occurs when the FMPLL detects a failure in either the reference signal or FMPLL output, and the loss-of-clock reset enable (LOCRE) bit in the FMPLL_SYNCR is set.

The device comes out of loss-of-clock reset using the following sequence:

1. Starting the internal reset signal asserts, as indicated by $\overline{\text{RSTOUT}}$ asserting, the value on the WKPCFG pin is applied. At the same time, the PLLCFG[0:1] values are applied only if $\overline{\text{RSTCFG}}$ is asserted.
2. After the FMPLL has a clock and is locked, the reset controller waits the predetermined clock cycles before negating $\overline{\text{RSTOUT}}$.When the clock count finishes, WKPCFG and BOOTCFG[0:1] are sampled. BOOTCFG[0:1] is only sampled if $\overline{\text{RSTCFG}}$ asserts.
3. The reset controller then waits four clock cycles before negating $\overline{\text{RSTOUT}}$ and updating the fields in SIU_RSR. The LCRS bit is set, and all other reset status bits in the SIU_RSR are cleared.

Refer to Section 4.2.2, “Reset Output (RSTOUT)”

Refer to Section 11.4.2.6, “Loss-of-Clock Detection,” for more information on loss-of-clock.

4.4.2.3.5 Watchdog Timer/Debug Reset

The WDRS bit in the reset status register (SIU_RSR) is set when the watchdog timer or a debug request reset occurs.

A watchdog timer reset occurs and the WDRS bit is set when all the following conditions occur:

- e200z6 core watchdog timer is enabled with the enable next watchdog timer (EWT)
- Watchdog timer interrupt status (WIS) bits are set in the timer status register (TSR)
- Watchdog reset control (WRC) field in the timer control register (TCR) is configured to reset
- Time-out occurs

The debug tool can issue a debug reset command by writing 2’b10 to the RST bit {DBCR0[2:3]} register in the e200z6 core, which sets the WDRS bit in the reset status register of the systems integration unit (SIU_RSR).

To determine if WDRS was set by a watchdog timer or debug reset, check the WRS field in the e200z6 core TSR.

The effect of a watchdog timer or debug reset request is the same on the reset controller.

The debug tool can also reset the device using one of the following methods:

- Debug tool asserts the $\overline{\text{RESET}}$ signal on the RESET_b pin
- Debug tool sets the software system reset (SSR) bit in the system reset control register (SIU_SRCR)

The debug tool writes a one to the software external reset (SER) bit in the system reset control register (SIU_SRCR) to generate an external software reset.

The device comes out of reset using the following sequence:

1. Starting when the internal reset signal asserts, as indicated by RSTOUT asserting, the value on the WKPCFG pin is applied. At the same time, the PLLCFG[0:1] values are applied only if RSTCFG is asserted.
2. After the FMPLL is locked, the reset controller waits the predetermined number of clock cycles before negating RSTOUT. When the clock count finishes, WKPCFG and BOOTCFG[0:1] are sampled. BOOTCFG[0:1] is only sampled if RSTCFG asserts.
3. The reset controller then waits 4 clock cycles before the negating RSTOUT, and the associated bits/fields are updated in the SIU_RSR.

Refer to the e200z6 Core Guide for more information on the watchdog timer and debug operation.

Refer to Section 4.2.2, “Reset Output (RSTOUT).”

4.4.2.3.6 Checkstop Reset

When the e200z6 core enters a checkstop state, and the checkstop reset is enabled, the CRE bit in the system reset control register (SIU_SRCR) is set and a checkstop reset occurs. Starting when the internal reset signal asserts (RSTOUT), the value on the WKPCFG pin is applied; at the same time the PLLCFG[0:1] values are applied if RSTCFG is asserted. After the FMPLL is locked, the reset controller waits a predetermined number of clock cycles before negating RSTOUT.

Refer to Section 4.2.2, “Reset Output (RSTOUT).”

When the clock count finishes, the WKPCFG and BOOTCFG[0:1] pins are sampled (the BOOTCFG[0:1] pins are only sampled if RSTCFG is asserted). The reset controller then waits four clock cycles before the negating RSTOUT, and updating the data in the SIU_RSR. In addition, the CRS bit is set, and all other reset status bits in the SIU_RSR are cleared. Refer to e200z6 Core Guide for more information.

4.4.2.3.7 JTAG Reset

A system reset occurs when JTAG is enabled and either the EXTEST, CLAMP, or HIGHZ instructions are executed by the JTAG controller. Starting at the assertion of the internal reset signal (as indicated by assertion of RSTOUT), the value on the WKPCFG pin is applied; at the same time the PLLCFG[0:1] values are applied if RSTCFG is asserted.

After the JTAG reset request has negated and the FMPLL is locked, the reset controller waits a predetermined number of clock cycles before negating RSTOUT. When the clock count finishes the WKPCFG and BOOTCFG[0:1] pins are sampled (note that the BOOTCFG[0:1] pins are sampled only if RSTCFG is asserted), and the data is updated in the SIU_RSR. The reset source status bits in the SIU_RSR are unaffected.

Refer to Section 4.2.2, “Reset Output (RSTOUT).”

Refer to Chapter 24, “IEEE 1149.1 Test Access Port Controller (JTAGC),” for more information.

4.4.2.3.8 Software System Reset

A software system reset is caused by a write to the SSR bit in the system reset control register (SIU_SRCR). A write of 1 to the SSR bit causes an internal reset of the MCU. The internal reset signal is asserted (as indicated by assertion of RSTOUT). The value on the WKPCFG pin is applied starting at the assertion of the internal reset signal (as indicated by assertion of RSTOUT); at the same time the PLLCFG[0:1] values are applied if RSTCFG is asserted. After the FMPLL locks, the reset controller waits a predetermined number of clock cycles before negating RSTOUT. When the clock count finishes the WKPCFG and BOOTCFG[0:1] pins are sampled (the BOOTCFG[0:1] pins are only sampled if RSTCFG is asserted). The reset controller then waits 4 clock cycles before negating RSTOUT, and the associated bits/fields are updated in the SIU_RSR. In addition, the SSRS bit is set, and all other reset status bits in the SIU_RSR are cleared.

Refer to Section 4.2.2, “Reset Output (RSTOUT).”

4.4.2.3.9 Software External Reset

A write of 1 to the SER bit in the SIU_SRCR causes the external RSTOUT pin to be asserted for a predetermined number of clocks. The SER bit automatically clears after the clock cycle count expires. A software external reset does not cause a reset of the MCU, the BAM program is not executed, the PLLCFG[0:1], BOOTCFG[0:1], and WKPCFG pins are not sampled. The SERF bit in the SIU_RSR is set, but no other status bits are affected. The SERF bit in the SIU_RSR is not automatically cleared after the clock count expires, and remains set until cleared by software or another reset besides the software external reset occurs.

Refer to Section 4.2.2, “Reset Output (RSTOUT).”

For a software external reset, the e200z6 core continues to execute instructions, timers that are enabled continue to operate, and interrupt requests continue to process. The application must ensure devices connected to RSTOUT are not accessed during a software external reset, and determine how to manage MCU resources.

4.4.3 Reset Configuration and Configuration Pins

The microcontroller and the BAM perform a reset configuration that allows certain functions of the MCU to be controlled and configured at reset. This reset configuration is defined by:

- Configuration pins
- A reset configuration halfword (RCHW), if present
- Serial port, if a serial boot is used

The following sections describe these configuration pins and the RCHW.

4.4.3.1 RSTCFG Pin

Table 4-5 shows the RSTCFG pin settings for configuring the MCU to use a default or a custom configuration.

Table 4-5. RSTCFG Settings

RSTCFG	Description
1	Use default configuration of: – booting from internal flash – clock source is a crystal on FMPLL
0	Get configuration information from: – BOOTCFG[0:1] – PLLCFG[0:1]

Refer to Chapter 2, "Signal Description" for more information about the RSTCFG pin.

4.4.3.2 WKPCFG Pin (Reset Weak Pullup/Pulldown Configuration)

As shown in Table 4-6, the signal on the WKPCFG pin determines whether specific eTPU and eMIOS pins are connected to weak pullup or weak pulldown devices during and after reset.

For all reset sources except the software external reset, the WKPCFG pin is applied starting when the internal reset signal asserts (RSTOUT). If the WKPCFG signal is logic high when RSTOUT asserts, pullup devices are enabled on the eTPU and eMIOS pins. If the WKPCFG signal is logic low when RSTOUT asserts, pulldown devices are enabled on those pins. The value on WKPCFG must remain constant during reset to avoid oscillations on the eTPU and eMIOS pins caused by switching pullup/down states. The final value of WKPCFG is latched four clock cycles before RSTOUT negates. After reset, software can modify the weak pullup/down selection for all I/O pins through the PCRs in the SIU.

Table 4-6. WKPCFG Settings

WKPCFG	Description
0	Weak pulldown applied to eTPU and eMIOS pins at reset
1	Weak pullup applied to eTPU and eMIOS pins at reset

Refer to Chapter 2, "Signal Description" for information about the WKPCFG pin and how the eTPU and eMIOS pins that are affected.

4.4.3.3 BOOTCFG[0:1] Pins (MCU Configuration)

In addition to specifying the RCHW location, the values latched on the BOOTCFG[0:1] pins at reset initialize the internal flash memory enabled/disabled state, and determine whether no arbitration or external arbitration of the external bus interface is selected. Additionally, the RCHW can determine either directly or indirectly how the MMU is configured, how the external bus is configured, the FlexCAN or eSCI module pin configuration, Nexus enabling, and password selection.

Refer to Chapter 2, "Signal Description" for information about the BOOTCFG pins.

4.4.3.4 PLLCFG[0:1] Pins

The PLLCFG pins are explained in Section 11.1.4, "FMPLL Modes of Operation."

Table 4-7. Configurations using PLLCFG[0:1] and $\overline{\text{RSTCFG}}$

$\overline{\text{RSTCFG}}$	PLLCFG0	PLLCFG1	Clock Mode	MODE	PLLSEL	PLLREF
1	PLLCFG pins ignored		Crystal reference (default)	1	1	1
0	0	0	Bypass mode	0	0	0
0	0	1	External reference	1	1	0
0	1	0	Crystal reference	1	1	1
0	1	1	Dual controller mode	1	0	0

Refer to Chapter 2, "Signal Description" for information about the PLLCFG pins.

4.4.3.5 Reset Configuration Halfword

4.4.3.5.1 Reset Configuration Halfword Definition

The RCHW is read from either external memory or internal flash memory. If a valid RCHW is not found, a FlexCAN or eSCI boot is initiated. The RCHW is a collection of control bits that specify a minimum MCU configuration after reset and define the desired mode of operation of the BAM program. At reset the RCHW provides a means to locate the boot code, determines if flash memory is programmed or erased, enables or disables the watchdog timer, configures the MMU to boot as either classic Power Architecture Book E code or as Freescale VLE code, and if booting externally, sets the bus size. Refer to the register indicated in RCHW bit descriptions for a description of each control bit.

NOTE

Do not configure the RCHW to a 32-bit bus size for devices with only a 16-bit data bus.

If booting from internal flash or external memory, the application must ensure that RCHW is the correct value for the configuration, and that it resides in that memory location. The boot ID of the RCHW must read 0x5A. BOOT_BLOCK_ADDRESS is explained in Section 16.3.2.2.5, "Read the Reset Configuration Halfword."

The fields of the RCHW are shown in Figure 4-3.

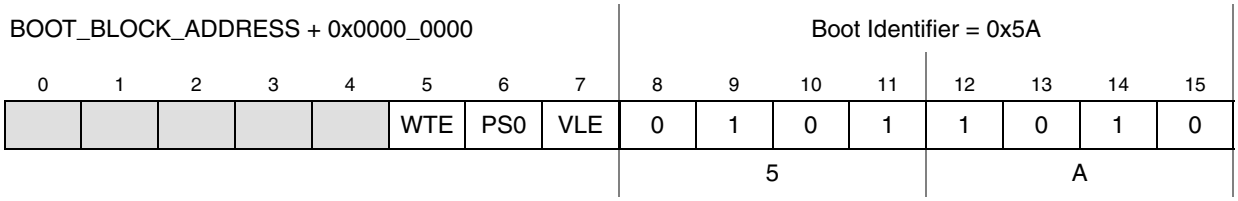


Figure 4-3. RCHW Fields

The following table describes the fields in the reset configuration halfword:

Table 4-8. Internal Boot RCHW Field Descriptions

Field	Description
0–4	Reserved: These bit values are ignored when the halfword is read. Write to 0 for future compatibility.
5 WTE	Watchdog timer enable. This is used to enable or disable the e200z6 watchdog timer through the BAM program. The configuration of the watchdog timer function is managed through the timer control register (TCR). 0 BAM does not write the e200z6 timebase registers (TBU and TBL) nor enable the e200z6 core watchdog timer. 1 BAM writes the e200z6 timebase registers (TBU and TBL) to 0x0000_0000_0000_0000 and enables the e200z6 core watchdog timer with a time-out period of 3 x 2^{17} system clock cycles. (Example: For 8 MHz crystal –> 12MHz system clock–> 32.7mS time-out. For 20 MHz crystal –> 30 MHz system clock –> 13.1mS time-out)
6 PS0	Port size. Defines the width of the data bus connected to the memory on $\overline{CS}$[0]. After system reset, $\overline{CS}$[0] is changed to a 16-bit port by the BAM which fetches the RCHW from either 16- or 32-bit external memories. Then the BAM reconfigures the EBI either as a 16-bit bus or a 32-bit bus, according to the settings of this bit. 0 32-bit $\overline{CS}$[0] port size 1 16-bit $\overline{CS}$[0] port size **Note:** Used only in external boot mode. Do not set the port to 32-bits if the device only has a 16-bit data bus.
7 VLE	VLE Code Indicator. This bit is used to configure the MMU for the boot block to execute as either Classic Power Architecture Book E code or as Freescale VLE code. 0 = Boot code executes as Classic Power Architecture Book E code 1 = Boot code executes as Freescale VLE code
8–15 BOOTID[0:7]	Boot identifier. This field serves two functions. First, it is used to indicate which block in flash memory contains the boot program. Second, it identifies whether the flash memory is programmed or invalid. The value of a valid boot identifier is 0x5A (0b01011010). The BAM program checks the first halfword of each flash memory block starting at block 0 until a valid boot identifier is found. If all blocks in the low address space of the internal flash are checked and no valid boot identifier is found, then the internal flash is assumed to be invalid and a CAN/SCI boot is initiated. For an external boot, only block 0 is checked for a valid boot identifier, and if not found, a CAN/SCI boot is initiated.

4.4.3.5.2 Invalid RCHW

If the device is configured to boot from internal flash, a valid boot ID must be read at the lowest address of one of the six LAS blocks in internal flash memory. If the device is configured to boot from external memory, a valid boot ID must be read at 0x0000_0000 of $\overline{CS}$[0]. Refer to Chapter 16, "Boot Assist Module (BAM)" for more information.

If no valid RCHW is found, a serial boot is initiated which does not use the RCHW. The watchdog timer is enabled. For serial boot entered from a failed external boot, the port size remains configured as 16-bits wide. For serial boot entered from a failed internal boot, the external bus is never configured and remains in the reset state of GPIO inputs.

4.4.3.5.3 Reset Configuration Halfword Source

The reset configuration halfword (RCHW) specifies a minimal MCU configuration after reset. The RCHW also contains bits that control the BAM program flow. Refer to Section 16.3.2.2.5, "Read the Reset Configuration Halfword" for information on the BAM using the RCHW. The RCHW is read and applied each time the BAM program executes, which is for every power-on, external, or internal reset event. The only exception to this is the software external reset.

Refer to Section 4.4.3.5, "Reset Configuration Halfword," for detailed descriptions of the bits in the RCHW. The RCHW is read from one of the following locations:

- The lowest address (0x0000_0000) of an external memory device, enabled by chip select $\overline{CS}$[0] using either a 16- or 32-bit data bus
- The lowest address of one of the six low address space (LAS) blocks in the internal flash memory. (2 x 16K; 2 x 48K; 2 x 64K)

At the negation of the $\overline{RSTOUT}$ pin, the BOOTCFG field in the RSR has been updated. If BOOTCFG[0] is asserted, then the BAM program reads the RCHW from address 0x0000_0000 in the external memory connected to $\overline{CS}$[0] (the BAM first configures the MMU and $\overline{CS}$[0] such that address 0x0000_0000 is translated to 0x2000_0000 and then directed to $\overline{CS}$[0]). When BOOTCFG[0] is asserted, BOOTCFG[1] determines whether external arbitration must be enabled to fetch the RCHW.

If BOOTCFG[0] and BOOTCFG[1] negates when $\overline{RSTOUT}$ negates, the BAM program attempts to read the RCHW from the first address of each of the six blocks in the low address space (LAS) of internal flash. Table 4-9 shows the LAS addresses.

Table 4-9. LAS Block Memory Addresses

Block	Address
0	0x0000_0000
1	0x0000_4000
2	0x0001_0000
3	0x0001_C000
4	0x0002_0000
5	0x0003_0000

If the RCHW stored in either internal or external flash is invalid (boot identifier field of RCHW is not 0x5A), or if BOOTCFG[0] negates and BOOTCFG[1] asserts when RSTOUT negates, then RCHW is not applicable, and serial boot mode is invoked. Table 4-10 summarizes the RCHW location options.

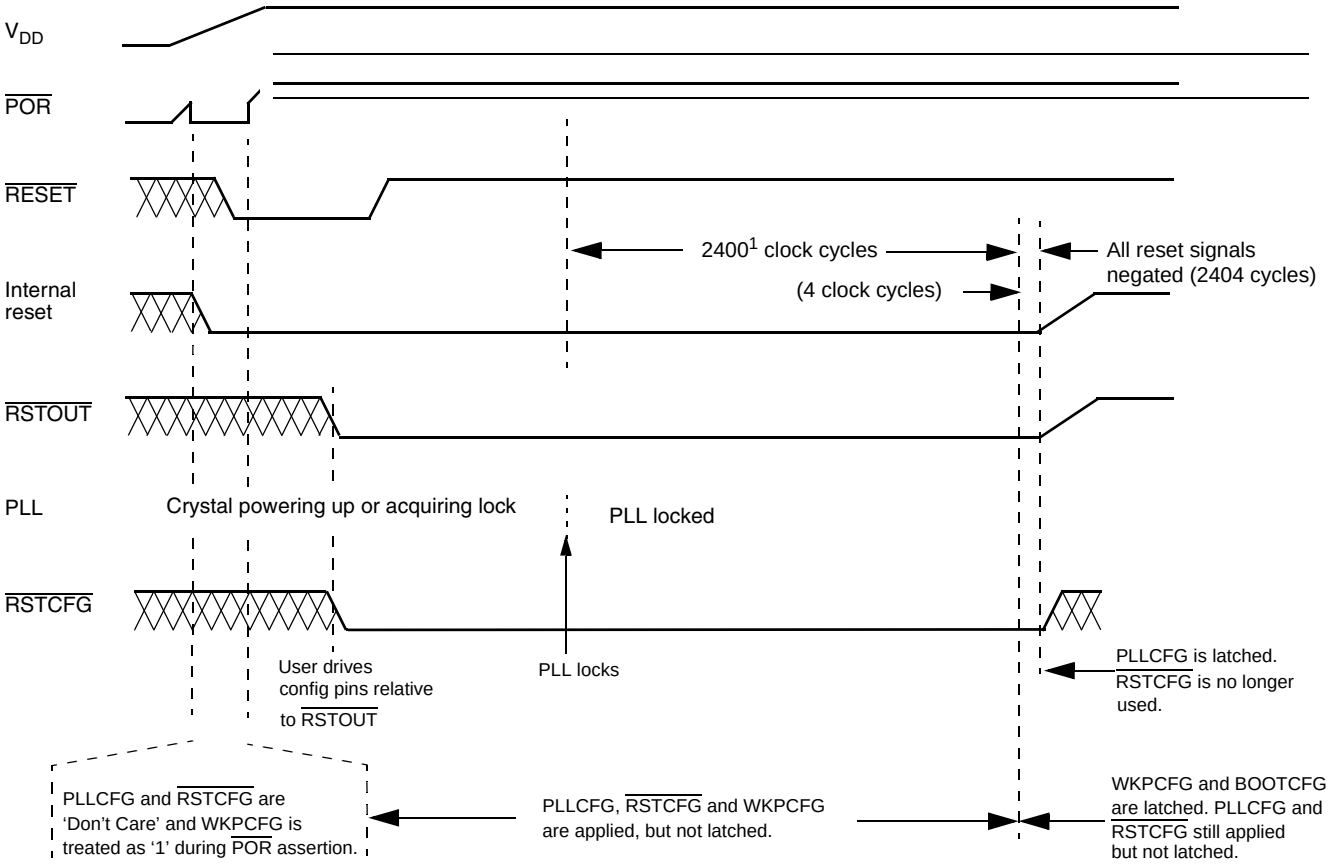
Table 4-10. Reset Configuration Halfword Sources

RSTCFG	BOOTCFG[0]	BOOTCFG[1]	Boot Identifier Field (RCHW)	Boot Mode	Configuration Word Source
1	—	—	Valid	Internal	The lowest address of one of the six low address spaces (LAS) in internal flash memory.
			Invalid	Serial	Not applicable
0	0	0	Valid	Internal	The lowest address of one of the six low address spaces (LAS) in internal flash memory.
			Invalid	Serial	Not applicable
0	0	1	—	Serial	Not applicable
0	1	0	Valid	External boot, no arbitration	The lowest address (0x0000_0000) of an external memory device, enabled by chip select CS[0] using either 16- or 32-bit data bus.
			Invalid	Serial	Not applicable
0	1	1	Valid	External Boot, External Arbitration	The lowest address (0x0000_0000) of an external memory device, enabled by chip select CS[0] using either 16- or 32-bit data bus.
			Invalid	Serial	Not applicable

4.4.4 Reset Configuration Timing

The timing diagram in Figure 4-4 shows the sampling of the BOOTCFG[0:1], WKPCFG, and PLLCFG[0:1] pins for a power-on reset. The timing diagram is also valid for internal/external resets assuming that V_{DD}, V_{DDSYN}, and V_{DDEH6} are within valid operating ranges. The values of the PLLCFG[0:1] pins are latched at the negation of the RSTOUT pin, if the RSTCFG pin is asserted at the negation of RSTOUT. The value of the WKPCFG signal is applied at the assertion of the internal reset signal (as indicated by the assertion of RSTOUT). The values of the WKPCFG and BOOTCFG[0:1] pins are latched 4 clock cycles before the negation of RSTOUT and stored in the reset status register (SIU_RSR). BOOTCFG[0:1] are latched only if RSTCFG is asserted. WKPCFG is not dependent on RSTCFG.

The following figure shows the reset configuration timing:



[1] This clock count is dependent on the configuration of the FMPLL (Refer to Section 4.2.2, "RSTOUT"). If the FMPLL is configured for 1:1 (dual controller) operation or for bypass mode, this clock count is 16000.

Figure 4-4. Reset Configuration Timing

4.4.5 Reset Flow

The following figure shows the process flow used for an external reset:

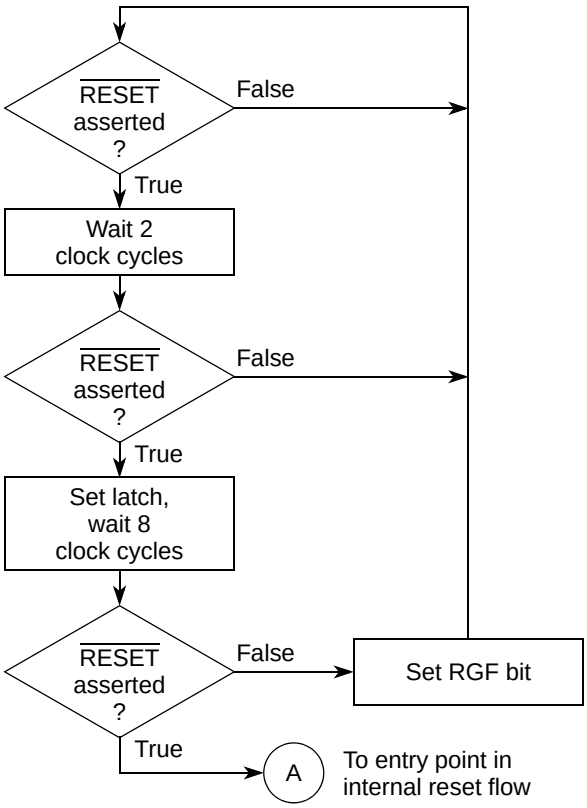
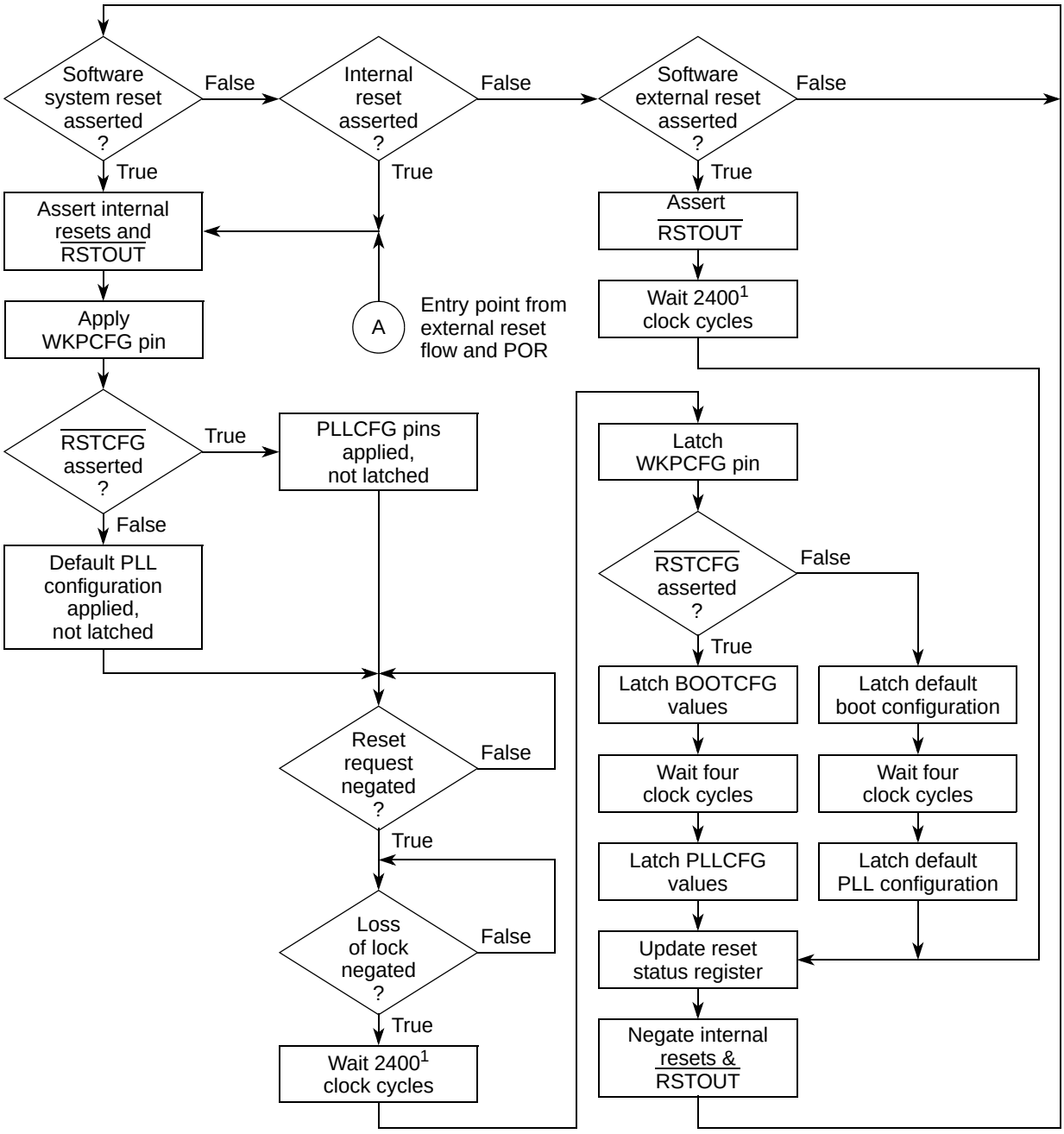


Figure 4-5. External Reset Flow Diagram

The following figure shows the process flow used for an internal reset:



NOTES:
[1] The clock count depends on the FMPLL configuration. Refer to Section 4.2.2, "Reset Output (RSTOUT)." If the FMPLL is configure in dual controller (1:1) or bypass mode, the clock count is 16000.

Figure 4-6. Internal Reset Flow Diagram

Chapter 5
Peripheral Bridge (PBRIDGE A and PBRIDGE B)

5.1 Introduction

There are two peripheral bridges, PBRIDGE_A and PBRIDGE_B, which act as interfaces between the system bus and lower bandwidth peripherals. In this manual, PBRIDGE refers to either of these bridges, as their functionality is identical. The only difference is the peripherals to which they connect. Accesses that fall within the address space of the PBRIDGE are decoded to provide individual module selects for peripheral devices on the slave bus interface.

5.1.1 Block Diagram

The PBRIDGE is the interface between the system bus and on-chip peripherals as shown in Figure 5-1.

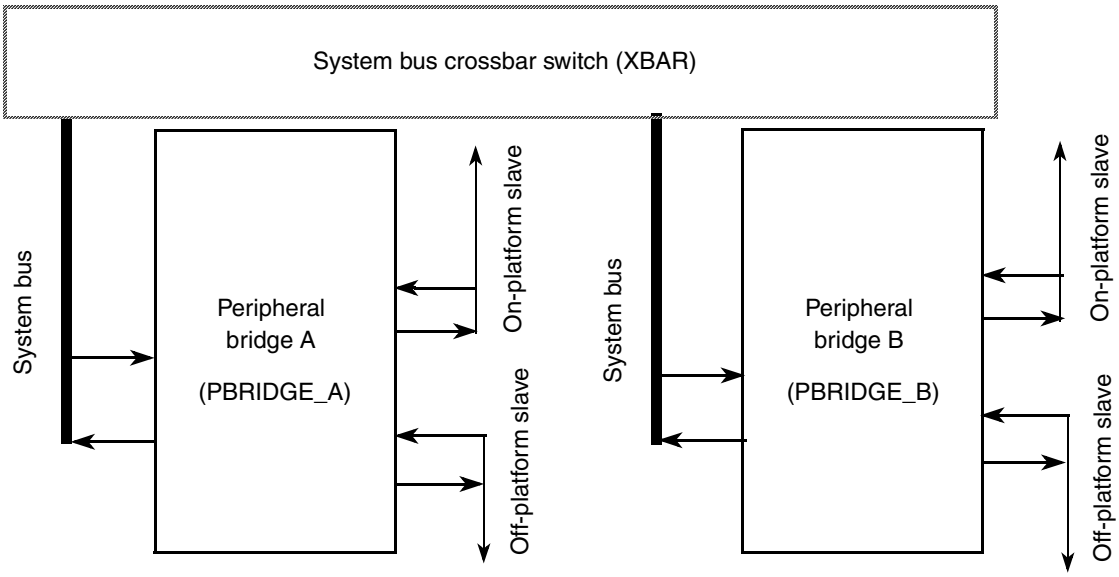


Figure 5-1. PBRIDGE Interface

5.1.2 Access Protections

The PBRIDGE provides programmable access protections for both masters and peripherals. Access protections allow the program to:

- Override the privilege level of a master to change it to user mode privilege
- Designate masters as trusted or untrusted

Peripherals can implement the following restrictions:

- Require supervisor privilege level for access
- Restrict access to a trusted master only
- Write-protect the peripheral to deny all access

Refer to Table 5-1 for a list of master/slave IDs and the peripherals for with each master and slave.

Refer to Section 13.3.2.9, “Flash Bus Interface Unit Access Protection Register (FLASH_BIUAPR)” for more information on access protection

Table 5-1. Peripheral Bridge Master/Slave ID Table

XBAR Port	XBS port Module	Master ID	Peripheral
Master 0	e200z6 Core—CPU	0	—
	e200z6—Nexus	1	—
Master 1	eDMA	2	—
Master 2	EBI	3	—
Master 3	FEC	4	—
Slave 0	FLASH		—
Slave 1	EBI		—
Slave 3	SRAM		—
Slave 6	PBRIDGE A		PBRIDGE A
			FMPLL
			EBI control
			FLASH control
			SIU
			eMIOS
			eTPU reg
			eTPU PRAM
			eTPU PRAM mirror
			eTPU SCM

Table 5-1. Peripheral Bridge Master/Slave ID Table (continued)

XBAR Port	XBS port Module	Master ID	Peripheral
Slave 7	PBRIDGE B		PBRIDGE B
			XBAR
			ESCM
			eDMA control
			INTC
			FEC
			eQADC
			DSPI A
			DSPI B
			DSPI C
			DSPI D
			eSCI A
			eSCI B
			CAN A
			CAN B
			CAN C
			CAN D
			BAM

5.1.3 Features

The following list summarizes the key features of the PBRIDGE:

- Supports the slave interface signals. This interface is only meant for slave peripherals.
- Supports 32-bit slave peripherals. Byte, 16-bit halfword, and 32-bit word reads and writes are supported to each slave peripheral.
- Supports a pair of slave accesses for 64-bit instruction fetches.
- Provides configurable per-module write buffering support.
- Provides configurable per-module and per-master access protections.

5.1.4 Modes of Operation

The PBRIDGE has only one operating mode.

5.2 External Signal Description

The PBRIDGE has no external signals.

5.3 Memory Map and Register Definitions

The memory map for the 32-bit PBRIDGE A registers is shown in Table 5-2.

Table 5-2. PBRIDGE A Memory Map

Address	Register Name	Register Description	Bits
Base (0xC3F0_0000)	PBRIDGE_A_MPCR	Master privilege control register	32
Base + (0x0004–0x001F)	—	Reserved	—
Base + 0x0020	PBRIDGE_A_PACR0	Peripheral access control register 0	32
Base + (0x0024–0x003F)	—	Reserved	—
Base + 0x0040	PBRIDGE_A_OPACR0	Off-platform peripheral access control register 0	32
Base + 0x0044	PBRIDGE_A_OPACR1	Off-platform peripheral access control register 1	32
Base + 0x0048	PBRIDGE_A_OPACR2	Off-platform peripheral access control register 2	32
Base + (0x004C–0x0053)	—	Reserved	—

The memory map for the 32-bit PBRIDGE B registers is shown Table 5-3.

Table 5-3. PBRIDGE B Memory Map

Address	Register Name	Register Description	Bits
Base (0xFFF0_0000)	PBRIDGE_B_MPCR	Master privilege control register	32
Base + (0x0004–0x001F)	—	Reserved	—
Base + 0x0020	PBRIDGE_B_PACR0	Peripheral access control register 0	32
Base + (0x0024–0x0027)	—	Reserved	—
Base + 0x0028	PBRIDGE_B_PACR2	Peripheral access control register 2	32
Base + (0x002C–0x003F)	—	Reserved	—
Base + 0x0040	PBRIDGE_B_OPACR0	Off-platform peripheral access control register 0	32
Base + 0x0044	PBRIDGE_B_OPACR1	Off-platform peripheral access control register 1	32
Base + 0x0048	PBRIDGE_B_OPACR2	Off-platform peripheral access control register 2	32
Base + 0x004C	PBRIDGE_B_OPACR3	Off-platform peripheral access control register 3	32
Base + (0x0050–0x0053)	—	Reserved	—

5.3.1 Register Descriptions

There are three types of registers that control each PBRIDGE. All registers are 32-bit registers and must be accessed in supervisor mode by trusted bus masters. Additionally, these registers must only be read from or written to by a 32-bit aligned access. PBRIDGE registers are mapped into the PBRIDGE A and

PBRIDGE_B address spaces. The protection and access fields of the MPCR, PACR, and OPACR registers are 4-bits wide. Although these registers are read/write, the reserved fields shown do not apply to this device and must remain at the reset value, therefore only write the fields' reset value to the reserved fields of these registers.

5.3.1.1 Master Privilege Control Register (PBRIDGE_*x*_MPCR)

Each master privilege control register (PBRIDGE_*x*_MPCR) specifies 4-bit access fields defining the access privilege level associated with a bus master in the platform, as well as specifying whether write accesses from this master are bufferable. The registers provide one field per bus master. The following table describes the fields in the PBRIDGE *X* master privilege control register:

Address: Base + 0x0000 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Access Field 0				Access Field 1				Access Field 2				Access Field 3			
R	MBW0	MTR0	MTW0	MPL0	MBW1	MTR1	MTW1	MPL1	MBW2	MTR2	MTW2	MPL2	MBW3	MTR3	MTW3	MPL3
W																
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	Access Field 4				Access Field 5				Access Field 6				Access Field 7			
R	MBW4	MTR4	MTW4	MPL4	0	1	1	1	0	1	1	1	0	1	1	1
W																
Reset	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1

Figure 5-2. Master Privilege Control Registers (PBRIDGE_*x*_MPCR)

The following table describes the fields in the PBRIDGE master privilege control register:

Table 5-4. PBRIDGE_*x*_MPCR Field Descriptions

Field	Description
0 MBW0	Master buffer writes. Determines whether the PBRIDGE is enabled to buffer writes from the CPU. Buffered writes are disabled by default. 0 Buffered write accesses from the CPU are disabled 1 Buffered write accesses from the CPU are enabled
1 MTR0	Master trusted for reads. Determines whether the CPU is trusted for read accesses. Trusted by default. 0 Read accesses from the CPU are not trusted 1 Read accesses from the CPU are trusted
2 MTW0	Master trusted for writes. Determines whether the master is trusted for write accesses. Trusted by default. 0 Write accesses from the CPU are not trusted 1 Write accesses from the CPU are trusted

Table 5-4. PBRIDGE_*x*_MPCR Field Descriptions (continued)

Field	Description
3 MPL0	Master privilege level. Determines how the privilege level of the CPU is determined. Accesses not forced to user mode by default. 0 Accesses from the CPU are forced to user mode. 1 Accesses from the CPU are not forced to user mode.
4 MBW1	Master buffer writes. Determines whether the PBRIDGE is enabled to buffer writes from the Nexus. Writes not able to be buffered by default. 0 Write accesses from the Nexus are not bufferable 1 Write accesses from the Nexus are allowed to be buffered
5 MTR1	Master trusted for reads. Determines whether the Nexus is trusted for read accesses. Trusted by default. 0 The Nexus is not trusted for read accesses. 1 The Nexus is trusted for read accesses.
6 MTW1	Master trusted for writes. Determines whether the master is trusted for write accesses. Trusted by default. 0 The Nexus is not trusted for write accesses. 1 The Nexus is trusted for write accesses.
7 MPL1	Master privilege level. Determines how the privilege level of the Nexus is determined. Accesses not forced to user mode by default. 0 Accesses from the Nexus are forced to user mode. 1 Accesses from the Nexus are not forced to user mode.
8 MBW2	Master buffer writes. Determines whether the PBRIDGE is enabled to buffer writes from the eDMA. Writes not able to be buffered by default. 0 Write accesses from the eDMA are not bufferable 1 Write accesses from the eDMA are allowed to be buffered
9 MTR2	Master trusted for reads. Determines whether the eDMA is trusted for read accesses. Trusted by default. 0 The eDMA is not trusted for read accesses. 1 The eDMA is trusted for read accesses.
10 MTW2	Master trusted for writes. Determines whether the master is trusted for write accesses. Trusted by default. 0 The eDMA is not trusted for write accesses. 1 The eDMA is trusted for write accesses.
11 MPL2	Master privilege level. Determines how the privilege level of the eDMA is determined. Accesses not forced to user mode by default. 0 Accesses from the eDMA are forced to user mode. 1 Accesses from the eDMA are not forced to user mode.
12 MBW3	Master buffer writes. Determines whether the PBRIDGE is enabled to buffer writes from the EBI. Writes not able to be buffered by default. 0 Write accesses from the EBI are not bufferable 1 Write accesses from the EBI are allowed to be buffered
13 MTR3	Master trusted for reads. Determines whether the EBI is trusted for read accesses. Trusted by default. 0 The EBI is not trusted for read accesses. 1 The EBI is trusted for read accesses.
14 MTW3	Master trusted for writes. Determines whether the master is trusted for write accesses. Trusted by default. 0 The EBI is not trusted for write accesses. 1 The EBI is trusted for write accesses.
15 MPL3	Master privilege level. Determines how the privilege level of the EBI is determined. Accesses not forced to user mode by default. 0 Accesses from the EBI are forced to user mode. 1 Accesses from the EBI are not forced to user mode.

Table 5-4. PBRIDGE_*x*_MPCR Field Descriptions (continued)

Field	Description
16 MBW4	Master buffer writes. Determines whether the PBRIDGE is enabled to buffer writes from the FEC. Writes not able to be buffered by default. 0 Write accesses from the FEC are not bufferable 1 Write accesses from the FEC are allowed to be buffered
17 MTR4	Master trusted for reads. Determines whether the FEC is trusted for read accesses. Trusted by default. 0 The FEC is not trusted for read accesses. 1 The FEC is trusted for read accesses.
18 MTW4	Master trusted for writes. Determines whether the master is trusted for write accesses. Trusted by default. 0 The FEC is not trusted for write accesses. 1 The FEC is trusted for write accesses.
19 MPL4	Master privilege level. Determines how the privilege level of the FEC is determined. Accesses not forced to user mode by default. 0 Accesses from the FEC are forced to user mode. 1 Accesses from the FEC are not forced to user mode.
20–31	Reserved.

5.3.1.2 Peripheral Access Control Registers (PBRIDGE_*x*_PACR) and Off-Platform Peripheral Access Control Registers (PBRIDGE_*x*_OPACR)

Each of the PBRIDGE on-platform peripherals has a 4-bit access field in a peripheral access control register (PACR) that defines the access levels supported by the given module. A single PACR contains up to eight of these module-access fields, and the PACR register structure is shown in Table 5-2 and Table 5-3. The PACR registers with their access fields are shown in Figure 5-3. There are three PACR registers, one for bridge A and two for bridge B.

Also, each of the off-platform peripherals has a 4-bit access field in an off-platform peripheral access control register (PBRIDGE_*x*_OPACR) that defines the access levels supported by the given module. Each OPACR contains up to eight of these module-access fields, and the OPACR register structure is shown in Table 5-2 and Table 5-3. The OPACR registers with their access fields are shown in Figure 5-4. Seven OPACR registers are used, three for bridge A, and four for bridge B.

NOTE

Not all members of the MPC5500 family have PBRIDGE_x_PACR and PBRIDGE_x_OPACR. On the devices that do not have them, writes to their addresses receive a transfer error. To ensure code compatibility across all the MPC55XX family of products, writes to those addresses must be qualified with SIU_MIDR[PARTNUM].

NOTE

Write PBRIDGE_x_PACR and PBRIDGE_x_OPACR with a read/modify/write for code compatibility.

The type of peripheral designated by each PACR and OPACR access field is shown in Table 5-6.

Address: Base + 0x0020 (PBRIDGE_A_PACR0 and PBRIDGE_B_PACR0) Access: R/W
Base + 0x0028 (PBRIDGE_B_PACR2)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Access Field 0				Access Field 1				Access Field 2				Access Field 3			
R	BW0 [1]	SP0 [2]	WP0	TP0 [2]	BW1	SP1	WP1	TP1	BW2	SP2	WP2	TP2	BW3	SP3	WP3	TP3
W																
Reset A_PACR0	0	1 [3]	0	1 [3]	0	0	0	0	0	0	0	0	0	0	0	0
Reset B_PACR0	0	1 [3]	0	1 [3]	0	1 [3]	0	0	0	0	0	0	0	0	0	0
Reset B_PACR2	0	1 [3]	0	0	0	1 [3]	0	0	0	1 [3]	0	0	0	1 [3]	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	Access Field 4				Access Field 5				Access Field 6				Access Field 7			
R	BW4	SP4	WP4	TP4	BW5	SP5	WP5	TP5	BW6	SP6	WP6	TP6	BW7	SP7	WP7	TP7
W																
Reset A_PACR0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset B_PACR0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset B_PACR2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1 In the PBRIDGE_A_PACR0 and PBRIDGE_B_PACR0 registers, the BW0 bit is not writeable.
2 The SP0 and TP0 bits default values are always used, even though the bits are writeable.
3 The default value is 0b0000 for PACR peripheral access fields that are unused or not connected.

Figure 5-3. Peripheral Access Control Registers (PBRIDGE_*x*_PACR*n*)

Address: Base + 0x0040 (PBRIDGE_x_OPACR0); Access: R/W
Base + 0x0044 (PBRIDGE_x_OPACR1);
Base + 0x0048 (PBRIDGE_x_OPACR2);
Base + 0x004C (PBRIDGE_B_OPACR3)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Access Field 0				Access Field 1				Access Field 2				Access Field 3			
R	BW0 [1]	SP0 [2]	WP0	TP0 [2]	BW1	SP1	WP1	TP1	BW2	SP2	WP2	TP2	BW3	SP3	WP3	TP3
W																
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	Access Field 4				Access Field 5				Access Field 6				Access Field 7			
R	BW4	SP4	WP4	TP4	BW5	SP5	WP5	TP5	BW6	SP6	WP6	TP6	BW7	SP7	WP7	TP7
W																
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

[1] In the PBRIDGE_A_PACR0 and PBRIDGE_B_PACR0 registers, the BW0 bit is not writeable

[2] The SP0 and TP0 bits default values are always used, even though the bits are writeable.

Figure 5-4. Off-platform Peripheral Access Control Registers (PBRIDGE_*x*_OPACR*n*)

Table 5-5. PBRIDGE_*x*_PACR*n* and PBRIDGE_*x*_OPACR*n* Field Descriptions

Field	Description
0, 4, 8, 12, 16, 20, 24, 28 BW*n*	Buffer writes. Determines whether write accesses to this peripheral are allowed to be buffered. Write accesses not bufferable by default 0 No write accesses are bufferable by the PBRIDGE to this peripheral. 1 Write accesses can be buffered by the PBRIDGE to this peripheral. **Note:** In PBRIDGE_A_PACR0 and PBRIDGE_B_PACR0, the BW0 bit is not writeable.
1, 5, 9, 13, 17, 21, 25, 29 SP*n*	Supervisor protect. Determines whether the peripheral requires supervisor privilege level for access. Supervisor privilege level required by default. 0 The peripheral does not require supervisor privilege level for accesses. 1 The peripheral requires supervisor privilege level for accesses. The PBRIDGE_x_MPCR[MPLy] control bit for the master must be set. If not, access is terminated with an error response and no peripheral access is initiated on the slave bus. **Note:** For PBRIDGE_A_PACR0 and PBRIDGE_B_PACR0, you must have supervisor privileges to access PBRIDGE registers. **Note:** Even though the SP0 bit (1) is writeable, the reset value for SP0 is always used.

Table 5-5. PBRIDGE_*x*_PACR*n* and PBRIDGE_*x*_OPACR*n* Field Descriptions (continued)

Field	Description
2, 6, 10, 14, 18, 22, 26, 30 WP*n*	Write protect. Determines whether the peripheral allows write accesses. Write accesses allowed by default. 0 This peripheral allows write accesses. 1 This peripheral is write protected. If a write access is attempted, the access is terminated with an error response and no peripheral access is initiated on the slave bus.
3, 7, 11, 15, 19, 23, 27, 31 TP*n*	Trusted protect. Determines whether the peripheral allows accesses from an untrusted master. Only trusted master privileges can access this register. 0 Accesses from an untrusted master are allowed. 1 Accesses from an untrusted master are not allowed. If an access is attempted by an untrusted master, the access is terminated with an error response and no peripheral access is initiated on the slave bus. **Note:** For PBRIDGE_A_PACR0 and PBRIDGE_B_PACR0, you must have trusted master privileges to access PBRIDGE registers. **Note:** Even though the TP0 bit (1) is writeable, the reset value for TP0 is always used.

The presence or absence of a module's 4-bit access field in PBRIDGE_x_PACR or PBRIDGE_x_OPACR is based on whether the peripheral is present on the device. When no peripheral is connected, the field is not implemented and is read as zero. Writes are ignored.

NOTE

Table 5-6 lists all of the access fields in the PACRs and OPACRs in both PBRIDGE A and PBRIDGE B, and each of the peripherals present on the device.

Table 5-6. PACR and OPACR Access Control Registers and Peripheral Mapping

Register	Register Address	Peripheral Access Field #	Peripheral Type	Access Field Default Value
PBRIDGE A				
PBRIDGE_A_PACR0	PBRIDGE_A_Base + 0x0020	0	PBRIDGE A	0b0101
		1–7	—	0b0000
PBRIDGE_A_OPACR0	PBRIDGE_A_Base + 0x0040	0	FMPLL	0b0100
		1	EBI control	0b0100
		2	Flash control	0b0100
		3	—	0b0100
		4	SIU	0b0100
		5–7	—	0b0100
PBRIDGE_A_OPACR1	PBRIDGE_A_Base + 0x0044	0	eMIOS	0b0100
		1–7	—	0b0100

Table 5-6. PACR and OPACR Access Control Registers and Peripheral Mapping (continued)

Register	Register Address	Peripheral Access Field #	Peripheral Type	Access Field Default Value
PBRIDGE_A_OPACR2	PBRIDGE_A_Base + 0x0048	0	eTPU	0b0100
		1	—	0b0100
		2	eTPU PRAM	0b0100
		3	eTPU PRAM mirror	0b0100
		4	eTPU SCM	0b0100
		5–7	—	0b0100
PBRIDGE B				
PBRIDGE_B_PACR0	PBRIDGE_B_Base + 0x0020	0	PBRIDGE B	0b0101
		1	XBAR	0b0100
		2–7	—	0b0000
PBRIDGE_B_PACR2	PBRIDGE_B_Base + 0x0028	0	ESCM	0b0100
		1	eDMA	0b0100
		2	INTC	0b0100
		3	—	0b0100
		4–7	—	0b0000
PBRIDGE_B_OPACR0	PBRIDGE_B_Base + 0x0040	0	eQADC	0b0100
		1–3	—	0b0100
		4	DSPI A	0b0100
		5	DSPI B	0b0100
		6	DSPI C	0b0100
		7	DSPI D	0b0100
PBRIDGE_B_OPACR1	PBRIDGE_B_Base + 0x0044	0–3	—	0b0100
		4	eSCI A	0b0100
		5	eSCI B	0b0100
		6-7	—	0b0100
PBRIDGE_B_OPACR2	PBRIDGE_B_Base + 0x0048	0	FlexCAN A	0b0100
		1	FlexCAN B	0b0100
		2	FlexCAN C	0b0100
		3	FlexCAN D	0b0100
		4–7	—	0b0100
PBRIDGE_B_OPACR3	PBRIDGE_B_Base + 0x004C	0	—	0b0100
		1–6	—	0b0100
		7	BAM	0b0100

5.4 Functional Description

The PBRIDGE serves as an interface between a system bus and the peripheral (slave) bus. It functions as a protocol translator. Support is provided for generating a pair of 32-bit peripheral accesses when targeted by a 64-bit system bus access. No other bus-sizing access support is provided.

Accesses that fall within the address space of the PBRIDGE are decoded to provide individual module selects for peripheral devices on the slave bus interface.

5.4.1 Access Support

Aligned 64-bit accesses, aligned word and halfword accesses, as well as byte accesses are supported for 32-bit peripherals. Peripheral registers must not be misaligned, although no explicit checking is performed by the PBRIDGE.

NOTE

Data accesses that cross a 32-bit boundary are not supported.

5.4.2 Peripheral Write Buffering

The PBRIDGE provides programmable write buffering capability to buffer write accesses in the PBRIDGE for later completion, while terminating the system bus access early. This provides improved performance in systems where frequent writes to a slow peripheral occur.

Write buffering is controllable on a per-master and per-peripheral basis. Enable write buffering for masters and peripherals only when an error termination from the slave bus does not occur or is safe to ignore. When write buffering is enabled, all accesses through the PBRIDGE must occur in sequence; bypassing buffered writes is *not* supported.

NOTE

Write buffering causes the processor core to believe that the write has completed before it actually has completed in the peripheral. If write buffering is enabled for a peripheral, the actual write takes an additional two system clock cycles plus any additional system clock cycles that the register needs. Most registers in the MPC5500 family delay the write by two clock cycles, but some registers take longer. This early termination, as seen by the processor core, can defeat the **mbar** or **msync** instruction between the write to clear a flag bit and the write to the INTC_EOIR. Therefore, if write buffering is enabled for a peripheral that has a flag bit, insert instructions between the **mbar** or **msync** instruction and the write to the INTC_EOIR that consumes at least the number of system clock cycles that the actual write is delayed.

Refer to Section 10.4.3.1.2, “End-of-Interrupt Exception Handler.”

5.4.2.1 Read Cycles

Read accesses are possible with the PBRIDGE when the requested access size is 32-bits or smaller, and is not misaligned across a 32-bit boundary. 64-bit data reads (not instruction) are not supported.

5.4.2.2 Write Cycles

Write accesses are possible with the PBRIDGE when the requested access size is 32-bits or smaller. Misaligned writes that cross a 32-bit boundary are not supported. 64-bit data writes (not instruction) are not supported.

5.4.2.3 Buffered Write Cycles

Single clock write responses to the system bus are possible with the PBRIDGE when the requested write access is bufferable. If the requested access does not violate the permissions check, and if both master and peripheral are enabled for buffering writes, the PBRIDGE internally buffers the write cycle. The write cycle is terminated early with zero system bus wait states. The access proceeds normally on the slave interface, but error responses are ignored.

All accesses are initiated and completed in order on the slave interface, regardless of buffering. If the buffer is full, a following write cycle stalls until it can either be buffered (if bufferable) or can be initiated. If the buffer has valid entries, a following read cycle stalls until the buffer is emptied and the read cycle can be completed.

5.4.3 General Operation

Slave peripherals are modules that contain readable/writable control and status registers. The system bus master reads and writes these registers through the PBRIDGE. The PBRIDGE generates module enables, the module address, transfer attributes, byte enables, and write data as inputs to the slave peripherals. The PBRIDGE captures read data from the slave interface and drives it on the system bus.

Separate interface ports are provided for on-platform and off-platform peripherals. The distinction between on-platform and off-platform is made to allow platform-based designs incorporating the PBRIDGE to separate the interface ports to allow for ease of timing closure. In addition, module selects and control register storage for on-platform peripherals are allocated at synthesis time, allowing only needed resources to be implemented. Off-platform module selects and control register storage do not have the same degree of configurability.

The modules that are on-platform and those that are off-platform are detailed in Table 5-7.

Table 5-7. On-Platform and Off-Platform Peripherals

On-Platform	Off-Platform
Enhanced direct memory access (eDMA)	Deserial serial peripheral interface (DSPI)
PBridge A and B	Enhanced queued analog-to-digital converter (eQADC)
Interrupt controller (INTC)	Enhanced serial communication interface (eSCI)

Table 5-7. On-Platform and Off-Platform Peripherals (continued)

On-Platform	Off-Platform
Error correction status module (ECSM)	FlexCAN controller area network
System bus crossbar switch (XBAR)	Boot assist module (BAM)
Fast Ethernet Controller (FEC)	System integration unit (SIU)
Parallel Digital Interface (PDI)	Enhanced modular input/output subsystem (eMIOS)
	Frequency modulated phase locked loop (FMPLL)
	Enhanced time processing unit (eTPU)
	External bus interface (EBI)
	Flash bus interface unit (FBIU)

The PBRIDGE occupies a 64 MB portion of the address space. A 0.5 MB portion of this space is allocated to on-platform peripherals. The remaining 63.5 MB is available for off-platform devices. The register maps of the slave peripherals are located on 16-KB boundaries. Each slave peripheral is allocated one 16-KB block of the memory map, and is activated by one of the module enables from the PBRIDGE. Up to thirty-two 16-KB external slave peripherals can be implemented, occupying contiguous blocks of 16 KB. Two global external slave module enables are available for the remaining 63 MB of address space to allow for customization and expansion of addressed peripheral devices. In addition, a single non-global module enable is also asserted whenever any of the 32 non-global module enables is asserted.

The PBRIDGE is responsible for indicating to slave peripherals if an access is in supervisor or user mode. The PBRIDGE can block user mode accesses to certain slave peripherals or it can allow the individual slave peripherals to determine if user mode accesses are allowed. In addition, peripherals can be designated as write-protected. The PBRIDGE supports the notion of trusted masters for security purposes. Masters can be individually designated as trusted for reads, trusted for writes, or trusted for both reads and writes, as well as being forced to look as though all accesses from a master are in user mode privilege level.

The PBRIDGE also supports buffered writes, allowing write accesses to be terminated on the system bus in a single clock cycle, and then subsequently performed on the slave interface. Write buffering is controllable on a per-peripheral basis. The PBRIDGE implements a two-entry 32-bit write buffer.

Chapter 6
System Integration Unit (SIU)

6.1 Introduction

This chapter describes the device system integration unit (SIU) that configures and initializes the following controls:

- MCU reset configuration
- System reset operation
- Pad configuration
- External interrupts
- General-purpose I/O (GPIO)
- Internal peripheral multiplexing

6.1.1 Block Diagram

Figure 6-1 is a block diagram of the SIU. One signal, from the muxed signals shown on the right side of the diagram, is assigned to a ball on the device. The SIU registers are accessed using the crossbar switch.

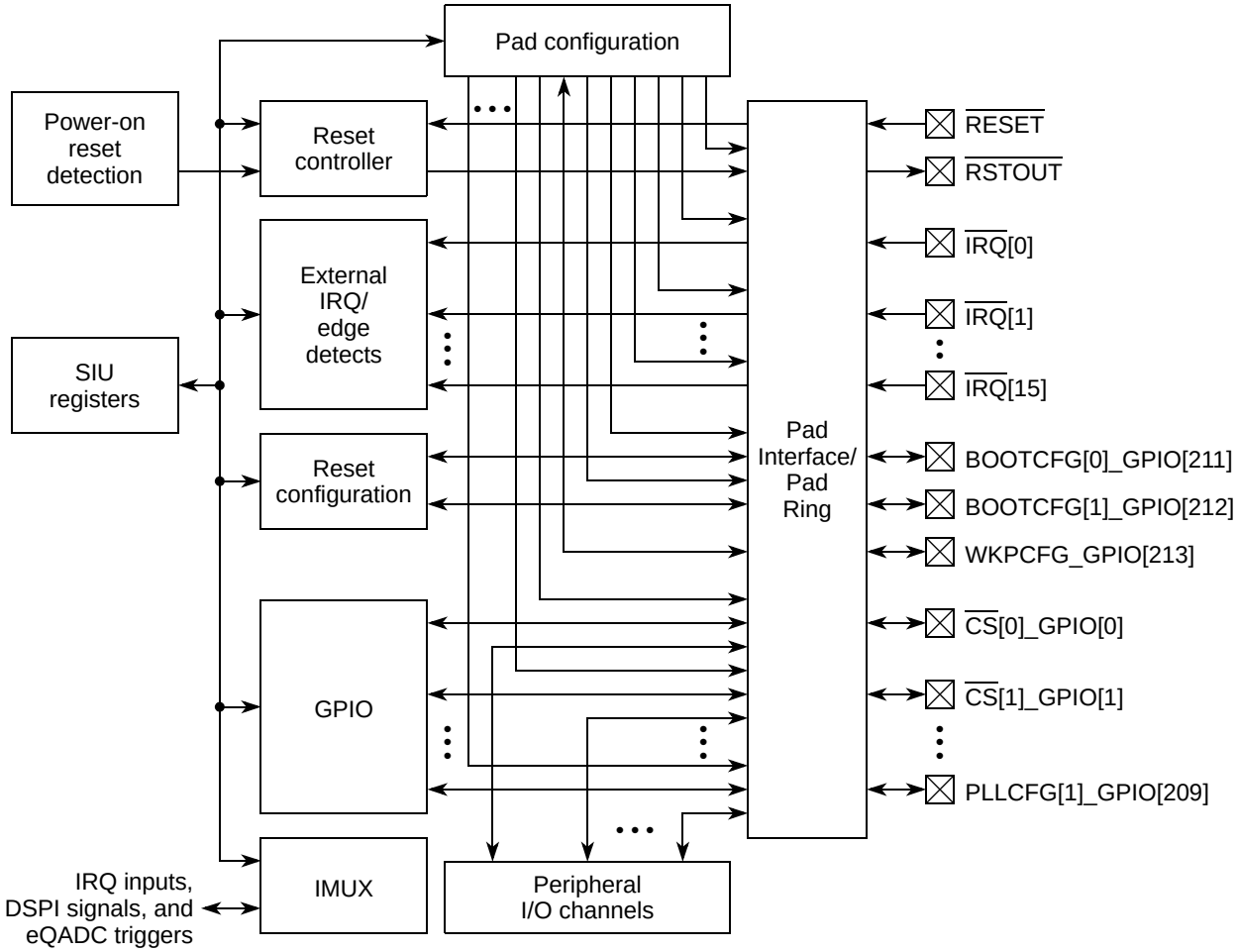


Figure 6-1. SIU Block Diagram

NOTE

The power-on reset detection module, pad interface/pad ring module, and peripheral I/O channels are external to the SIU.

6.1.2 Overview

The system integration unit (SIU) is accessed by the e200z6 core through the system bus crossbar switch (XBAR) and the peripheral bridge A (PBRIDGE_A). Table 6-1 lists the features the SIU configures:

Table 6-1. SIU Features

Feature	Description
MCU reset operations	Controls the external pin boot logic
System reset operations	Monitors internal and external reset sources, and drives the $\overline{\text{RSTOUT}}$ signal • Power-on reset support • Reset status register providing last reset source to software • Glitch detection on reset input • Software controlled reset assertion
Pad configuration registers	Enables the configuration and initialization of the I/O pin electrical characteristics using software to select the following: • Active function from the set of multiplexed functions • Pullup and pulldown characteristics of the pin • Slew rate for slow and medium pads • Open drain mode for output pins • Hysteresis for input pins • Drive strength of bus signals for fast pads
External interrupt operations	• 16 interrupt requests • Rising- or falling-edge event detection • Programmable digital filter for glitch rejection
General-purpose I/O (GPIO)	Provides uniform and discrete I/O control of 178 MCU general-purpose I/O pins, where each GPIO signal has an input register and an output register.
Internal peripheral multiplexing	Provides flexibility to customize signal/pin assignments for application development that allows: • Serial and parallel chaining of DSPIs • Flexible selection of eQADC trigger inputs • Assignment of interrupt requests (IRQs) between external pins and DSPI

6.1.3 Modes of Operation

The MPC5500 family of devices has several operating modes for configuring and testing the chip:

Table 6-2. SIU Operating Modes

Operating Mode	Description
Normal	In normal mode, the SIU provides the register interface and logic that controls the device and system configuration, the reset controller, and GPIO. The SIU continues operation with no changes in stop mode.
Debug	SIU operation in debug mode is identical to operation in normal mode.

6.2 External Signal Description

Table 6-3 lists the external pins used by the SIU.

Table 6-3. SIU Signal Properties

Name	Function	I/O Type	Pad Type	Pullup Pulldown [1]
Resets				
$\overline{\text{RESET}}$	Reset input	Input	—	Up
$\overline{\text{RSTOUT}}$	Reset output	Output	Slow	—
System Configuration				
GPIO[0:210]	General-purpose I/O	I/O	Slow	Up/down
BOOTCFG[0:1]_ GPIO[211:212]	Boot configuration input General-purpose I/O	Input I/O	Slow	Down Up/down
WKPCFG_ GPIO[213]	Weak-pull configuration General-purpose I/O	Input I/O	Slow	Up Up/down
External Interrupt				
$\overline{\text{IRQ}}$[0:15] [2]	External interrupt request input	Input	Slow	—[3]

1 Internal weak pullup/down. The reset weak pullup/down state for the primary signal function is given. For example, the reset weak pullup/down state of the BOOTCFG[0:1]_GPIO[211:212] signal is weak pulldown enabled.

2 The GPIO and IRQ signals are multiplexed with other functions on the device.

3 The weak pullup/down state at reset for the IRQ signals depends on the muxed signals that share the pin. The weak pullup/down state for these pins is as follows:
$\overline{\text{IRQ}}$[0, 1, 4, 5, 6, 7, 12:14]Up
$\overline{\text{IRQ}}$[2, 3, 15] Down
$\overline{\text{IRQ}}$[8:11] WKPCFG

6.2.1 Detailed Signal Descriptions

6.2.1.1 Reset Input ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ is an active-low input signal asserted by an external device during a power-on reset (POR) or external reset. If $\overline{\text{RESET}}$ asserts for ten clock cycles only, the internal reset signal asserts. Asserting the $\overline{\text{RESET}}$ signal while the device is processing a reset restarts the reset process at the beginning.

$\overline{\text{RESET}}$ has a glitch detector logic that senses electrical fluctuations on the V_{DDEH} input pins that drop below the switch point value for more than two clock cycles. The switch point value is between the maximum V_{IL} and minimum V_{IH} specifications for the V_{DDEH} input pins.

6.2.1.2 Reset Output ($\overline{\text{RSTOUT}}$)

$\overline{\text{RSTOUT}}$ is an active-low output signal that uses a push/pull configuration. It is driven to the low state by the MCU for all internal and external reset sources. After the $\overline{\text{RESET}}$ input signal negates, $\overline{\text{RSTOUT}}$ asserts for:

- 16000 clock cycles for devices configured in bypass mode
- 16004 clock cycles for devices configured for FMPLL dual-controller mode (1:1)
- 2404 clock cycles for all other FMPLL modes

To invoke an external software reset, write a 1 to the system external reset (SER) bit in the system reset control register (SIU_SRCR). This asserts $\overline{\text{RSTOUT}}$ for 2400 clock cycles. An external software reset does not execute the BAM module or sample BOOTCFG[0:1].

6.2.1.3 General-Purpose I/O (GPIO[0:213])

The GPIO signals provide general-purpose input and output functions. GPIO signals are generally multiplexed with other I/O pin functions. Each GPIO input and output is separately controlled by an eight-bit general-purpose data input (SIU_GPDI*n*) and a general-purpose data output (SIU_GPDO*n*) register.

Refer to the following sections for more information:

Section 6.3.1.159, “GPIO Pin Data Output Registers 0–213 (SIU_GPDOn)”

Section 6.3.1.160, “GPIO Pin Data Input Registers 0–213 (SIU_GPDIn)”

6.2.1.4 Boot Configuration (BOOTCFG[0:1])

The BOOTCFG value specifies the location and boot mode used by the boot assist module (BAM). All reset sources can read the boot configuration field, BOOTCFG[0:1], except a debug port reset and a software external reset.

The BOOTCFG values are read only if $\overline{\text{RSTCFG}}$ asserts while $\overline{\text{RSTOUT}}$ is asserted. The BOOTCFG signal asserts after $\overline{\text{RSTCFG}}$ to get the boot input information. BOOTCFG[0:1] is sampled four clock cycles before $\overline{\text{RSTOUT}}$ negates, and the latched boot values are stored in the reset status register (SIU_RSR).

If $\overline{\text{RSTCFG}}$ asserts while processing a reset, BOOTCFG[0:1] is sampled. Otherwise, if $\overline{\text{RSTCFG}}$ negates while processing a reset, the following occurs:

1. BOOTCFG[0:1] is not sampled
2. BAM module boots from internal flash (default = 0b00)
3. Boot value from internal flash is written to BOOTCFG[0:1] field in the reset status register (SIU_RSR)
4. BOOTCFG[0:1] values are latched and driven as output signals from the SIU

The BOOTCFG values are used only if the RSTCFG asserts while RSTOUT is asserted. Otherwise, the default value for BOOTCFG (0b00) in the reset status register (SIU_RSR) is used, as shown in Table 6-4.

Table 6-4. BOOTCFG[0:1] Configuration

Value	Meaning
0b00	Boot from internal flash memory (default)
0b01	FlexCAN / eSCI boot
0b10	Boot from external memory (no arbitration)
0b11	Boot from external memory (external arbitration)

6.2.1.5 I/O Weak Pullup Reset Configuration (WKPCFG)

The WKPCFG signal is applied when the internal reset signal asserts (indicated by RSTOUT asserting), and is sampled four clock cycles before RSTOUT negates. The WKPCFG value configures the internal weak pullup or weak pulldown pin characteristics after a reset occurs in the eMIOS or eTPU modules.

The value of WKPCFG is latched at reset, stored in the reset status register (SIU_RSR), and updated for all reset sources except the debug port reset and software external reset. The WKPCFG value must be valid and not change until RSTOUT negates.

6.2.1.6 External Interrupt Request Input (IRQ)

IRQ[0:15] The external interrupt request (IRQ) inputs connect to the SIU IRQ inputs. The external trigger IRQ select register 1 (SIU_ETISR) specifies the IRQ[0:15] signals that are input to the SIU IRQs.

External interrupt requests are triggered by rising- and/or falling-edge events that are enabled by setting a bit in:

- IRQ rising-edge event enable register (SIU_IREER)
- IRQ falling-edge event enable register (SIU_IFEER)

If the bit is set in both registers, both rising- and falling-edge events trigger an interrupt request. Each IRQ has a counter that tracks the number of system clock cycles that occur between the rising- and falling-edge events. An IRQ counter exists for each IRQ rising- or falling-edge event enable bit.

The digital filter length field in the IRQ digital filter register (SIU_IDFR) specifies the minimum number of system clocks that the IRQ signal must hold a logic value to qualify the edge-triggered event as a valid state change. When the number of system clocks in the IRQ counter equals the value in the digital filter length field, the IRQ state latches and the IRQ counter is cleared.

If the previous filtered state of the IRQ does not match the current state, and the rising- or falling-edge event is enabled, the IRQ flag bit is set to 1. For example, the IRQ flag bit is set if a rising-edge event occurs under the following conditions:

- Previous filtered IRQ state was a logic 0
- Current latched IRQ state is a logic 1
- Rising-edge event is enabled for the IRQ

When the counter for an IRQ is not enabled, the state of the IRQ is held in the current and previous state latches. The IRQ counter operates independently of the IRQ or overrun flag bit. Clearing the IRQ flag or overrun flag bits does not clear or reload the counter.

Refer to the following sections for more information:

Section 6.3.1.4, “External Interrupt Status Register (SIU_EISR)”
Section 6.3.1.9, “IRQ Rising-Edge Event Enable Register (SIU_IREER)”
Section 6.3.1.10, “IRQ Falling-Edge Event Enable Register (SIU_IFEER)”
Section 6.3.1.11, “IRQ Digital Filter Register (SIU_IDFR)”

6.2.1.6.1 External Interrupts

The IRQ signals map to 16 independent interrupt requests output from the SIU. The IRQ flag bit is set when a rising-edge and/or falling-edge event occurs for the IRQ. An external IRQ signal is asserted when all of the following occur:

- Enable bit is set in the IRQ rising- and/or falling-edge event registers (SIU_IREER, SIU_IFEER)
- IRQ flag bit is set in the external interrupt status register (SIU_EISR)
- Enable bit is cleared in the DMA/Interrupt request enable register (SIU_DIRER)
- Select bit is cleared in the DMA/Interrupt select register (SIU_DIRSR)

Refer to the following sections for more information:

Section 6.3.1.5, “DMA Interrupt Request Enable Register (SIU_DIRER)”
Section 6.3.1.6, “DMA/Interrupt Request Select Register (SIU_DIRSR)”

6.2.1.6.2 DMA Transfers

DMA IRQ signals ($\overline{\text{IRQ}}$[0] through $\overline{\text{IRQ}}$[3]) map to four independent DMA transfer *or* interrupt request outputs configured in the SIU. A DMA transfer or interrupt request asserts when all of the following occur:

- IRQ flag bit is set in the external interrupt status register (SIU_EISR)
- Enable bit is set in the DMA transfer or interrupt request enable register (SIU_DIRER)
- Select bit is set in the DMA transfer or interrupt request select register (SIU_DIRSR)

The SIU receives a ‘DMA transfer done’ signal for each DMA or interrupt request transmitted. When the ‘DMA done’ signal asserts, the IRQ flag bit is cleared.

Refer to the following sections for more information:

Section 6.3.1.5, “DMA Interrupt Request Enable Register (SIU_DIRER)”
Section 6.3.1.6, “DMA/Interrupt Request Select Register (SIU_DIRSR)”

6.2.1.6.3 Overruns

An overrun IRQ exists for each overrun flag bit in the overrun status register (SIU_OSR). An overrun IRQ asserts when all of the following occur:

- Enable bit is set in the IRQ rising- and/or falling-edge event registers (SIU_IREER, SIU_IFEER)

- IRQ flag bit is set in the external interrupt status register (SIU_EISR)
- Bit is set in the overrun request enable and overrun status registers (SIU_ORER, SIU_OSR)
- Rising- or falling-edge event triggers an interrupt request

The SIU outputs one overrun IRQ bit that is the logical OR of all of the IRQ overrun bits.

Refer to the following sections for more information:

Section 6.3.1.4, “External Interrupt Status Register (SIU_EISR)”
Section 6.3.1.7, “Overrun Status Register (SIU_OSR)”
Section 6.3.1.8, “Overrun Request Enable Register (SIU_ORER)”

6.2.1.6.4 Edge-Detect Events

An IRQ asserts when an:

- Edge-detect event is enabled
- Edge-detect event occurs

To assert an IRQ when an edge-detect event occurs:

1. Set the enable bit in the IRQ rising- and falling-edge event enable registers (SIU_IREER, SIU_IFEER)
2. Clear the enable bits for the DMA/Interrupt request enable register (SIU_DIRER)

The IRQ bit is set in the external IRQ status register (SIU_EISR) when an edge-detect event occurs for that IRQ.

Refer to the following sections for more information:

Section 6.3.1.4, “External Interrupt Status Register (SIU_EISR)”
Section 6.3.1.9, “IRQ Rising-Edge Event Enable Register (SIU_IREER)”
Section 6.3.1.10, “IRQ Falling-Edge Event Enable Register (SIU_IFEER)”

6.3 Memory Map and Register Definition

Table 6-5 is the address map for the SIU registers. All register addresses shown are an offset of the SIU base address.

Table 6-5. SIU Register Address Map

Address	Name	Description	Bits
Base = 0xC3F9_0000	Reserved		
Base + 0x0004	SIU_MIDR	MCU ID register	32
Base + 0x0008	Reserved		
Base + 0x000C	SIU_RSR	Reset status register	32
Base + 0x0010	SIU_SRCR	System reset control register	32
Base + 0x0014	SIU_EISR	SIU external interrupt status register	32

Table 6-5. SIU Register Address Map

Address	Name	Description	Bits
Base + 0x0018	SIU_DIRER	DMA/interrupt request enable register	32
Base + 0x001C	SIU_DIRSR	DMA/interrupt request select register	32
Base + 0x0020	SIU_OSR	Overrun status register	32
Base + 0x0024	SIU_ORER	Overrun request enable register	32
Base + 0x0028	SIU_IREER	IRQ rising-edge event enable register	32
Base + 0x002C	SIU_IFEER	IRQ falling-edge event enable register	32
Base + 0x0030	SIU_IDFR	IRQ digital filter register	32
Base + (0x0034–0x003F)	Reserved		
Base + (0x0040–0x020C)	SIU_PCR0–SIU_PCR230	Pad configuration registers 0–230	16
Base + (0x020E–0x05FF)	Reserved		
Base + (0x0600–0x06D5)	SIU_GPDO0–SIU_GPDO213	GPIO pin data output registers 0–213	8
Base + (0x06D6–0x07FF)	Reserved		
Base + (0x0800–0x08D5)	SIU_GPDI0–SIU_GPDI213	GPIO pin data input registers 0–213	8
Base + (0x08D6–0x08FF)	Reserved		
Base + (0x0900–0x0903)	SIU_ETISR	eQADC trigger input select register	32
Base + (0x0904–0x0907)	SIU_EIISR	External IRQ input select register	32
Base + (0x0908–0x090B)	SIU_DISR	DSPI input select register	32
Base + (0x090C–0x097F)	Reserved		
Base + 0x0980	SIU_CCR	Chip configuration register	32
Base + 0x0984	SIU_ECCR	External clock control register	32
Base + 0x0988	SIU_CARH	Compare A high register	32
Base + 0x098C	SIU_CARL	Compare A low register	32
Base + 0x0990	SIU_CBRH	Compare B high register	32
Base + 0x0994	SIU_CBRL	Compare B low register	32
Base + (0x0998–0x09FF)	Reserved		

6.3.1 Register Descriptions

The register figures use the following notational conventions in this section:

w1c	Write 1 to clear the bit to 0.
—	Not applicable.
	Reserved or unimplemented bit.
U	Bit value is uninitialized upon reset.
u	Bit value is unchanged upon reset.

6.3.1.1 MCU ID Register (SIU_MIDR)

The SIU_MIDR contains the part identification number and mask revision number specific to the device. The part number is a read-only field that is mask programmed with the part number of the device. The part number changes depending on the module versions contained in a device. The part number does not change for bug fixes or process changes.

The mask number is a read-only field that is mask programmed with the specific mask revision level of the device. The current value applies to revision 0 and is updated for each mask revision.

The MCU ID register is 32-bits. Figure 6-2 shows the MCU ID register values.

Address: Base + 0x0004 Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	PARTNUM															
W																
MPC5566 part number	0	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	CSP	PKG			0	0	0	0	MASKNUM_MAJOR				MASKNUM_MINOR			
W																
Default reset values	0	416 = 0b110			0	0	0	0	0b0000				0b0000			
Reset values 496 pckg	1	416 CSP = 0b110														

Figure 6-2. MPC5566 MCU ID Register (SIU_MIDR)

Table 6-6. SIU_MIDR Field Descriptions

Field	Description
0–15 PARTNUM	MCU part number. Read-only, mask programmed part identification number of the MCU. MPC5566 reads 0x5566.
16 CSP	CSP configuration: 0 Standard package 1 CSP package
17–19 PKG	Package settings. PKG selects the pin package for the MPC5566 device. 000 Select for Legacy compatibility 001–01*x* Reserved 100–101Reserved 110 Select the 416 package 110 Select the 496 calibration assembly 111 Reserved
20–23	Reserved

Table 6-6. SIU_MIDR Field Descriptions

Field	Description
24–27 MASKNUM_MAJOR [0:3]	Major revision number of MCU mask. Read-only, mask programmed mask number of the MCU. Reads 0x0 for the initial mask set of the device, and changes sequentially for each mask set.
28–31 MASKNUM_MINOR [0:3]	Minor revision number of MCU mask. Read-only, mask programmed mask number of the MCU. Reads 0x0 for the initial mask set of the device, and changes sequentially for each mask set.

6.3.1.2 Reset Status Register (SIU_RSR)

The SIU_RSR contains the sources of the most recent reset, and the state of the configuration pins at reset. Except for a POR request or a software external reset, all reset requests, regardless of priority, are not serviced until the current reset completes.

This register contains one reset status bit for each of the following reset sources:

- Power-on reset (POR)
- External reset
- Software system reset
- Software external reset
- Watchdog reset
- Loss-of-lock reset
- Loss-of-clock reset
- Checkstop reset

A reset status bit set to 1 indicates a reset request by that source. After the reset status bits are set, they remain set until another reset occurs. Simultaneous reset requests are prioritized. When reset requests with different priorities occur on the same clock cycle, the reset request with the highest priority is serviced and the status bit of only that reset request is set.

The following table lists the reset sources and arbitration priorities:

Table 6-7. Reset Source Priorities

Reset Source	Priority	Group
• Power on reset (POR) • External reset	Highest	0
• Software system reset	Higher	1
• Loss-of-clock • Loss-of-lock • Watchdog • Checkstop	Lower	2
• Software external reset	Lowest	3

The WKPCFG bit retains the latest value of the WKPCFG signal before reset. The BOOTCFG field retains the latest values of the BOOTCFG[0:1] signals before reset.

Address: Base + 0x000C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	PORS	ERS	LLRS	LCRS	WDRS	CRS	0	0	0	0	0	0	0	0	SSRS	SERF
W																
Reset [1]	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	WKP CFG [2]	0	0	0	0	0	0	0	0	0	0	0	0	BOOTCFG		RGF
W																
Reset [1]	U [2]	0	0	0	0	0	0	0	0	0	0	0	0	U [3]		0

[1] The reset status register receives the reset values during power-on reset.

[2] The reset value of the WKPCFG bit is the value on the WKPCFG pin at the time of the last reset.

[3] The reset value of the BOOTCFG bits is the value on the BOOTCFG[0:1] pins at he time of the last reset.

Figure 6-3. Reset Status Register (SIU_RSR)

The following table lists and describes the fields of the reset status register:

Table 6-8. SIU_RSR Field Descriptions

Field	Description
0 PORS	Power-on reset status. 0 Another reset source was acknowledged by the reset controller since the last assertion of the power-on reset input. 1 The power-on reset input to the reset controller was asserted and no other reset source was acknowledged since the assertion of the power-on reset input except an external reset.
1 ERS	External reset status. 0 The last reset source acknowledged by the reset controller was *not* a valid assertion of the $\overline{\text{RESET}}$ pin. 1 The last reset source acknowledged by the reset controller was a valid assertion of the $\overline{\text{RESET}}$ pin.
2 LLRS	Loss-of-lock reset status. 0 The last reset source acknowledged by the reset controller was *not* a loss-of-PLL lock reset. 1 The last reset source acknowledged by the reset controller was a loss-of-PLL lock reset.
3 LCRS	Loss-of-clock reset status. 0 The last reset source acknowledged by the reset controller was *not* a loss-of-clock reset. 1 The last reset source acknowledged by the reset controller was a loss-of-clock reset.
4 WDRS	Watchdog timer/debug reset status. 0 The last reset source acknowledged by the reset controller was *not* a watchdog timer or debug reset. 1 The last reset source acknowledged by the reset controller was a watchdog timer or debug reset.

Table 6-8. SIU_RSR Field Descriptions

Field	Description
5 CRS	Checkstop reset status. 0 The last reset source acknowledged by the reset controller was *not* an enabled checkstop reset. 1 The last reset source acknowledged by the reset controller was an enabled checkstop reset.
6–13	Reserved
14 SSRS	Software system reset status. 0 The last reset source acknowledged by the reset controller was *not* a software system reset. 1 The last reset source acknowledged by the reset controller was a software system reset.
15 SERF	Software external reset flag. 0 The software external reset input to the reset controller was *not* asserted, or this bit has been cleared by writing a 1 to it. 1 The software external reset input to the reset controller was asserted while this bit was 0.
16 WKPCFG	Weak pull configuration pin status 0 The WKPCFG pin value latched during the last reset was a *logical 0 and weak pulldown* is the default setting. 1 The WKPCFG pin value latched during the last reset was a *logical 1 and weak pullup* is the default setting.
17–28	Reserved
29–30 BOOTCFG	Reset configuration pin status. BOOTCFG[0:1] identifies the address of the reset configuration halfword (RCHW) and whether arbitration is used by the boot assist module (BAM). 00 Internal boot mode – lowest address (0x0000_0000) from one of the six LAS fields in internal flash memory. 01 Serial boot mode – lower halfword of the censorship control word. 10 External boot mode – lowest address (0x0000_0000) of external memory as defined by the chip select 0 ($\overline{CS}$[0]) signal with no external arbitration. 11 Invalid value – External boot mode with external arbitration. If $\overline{RSTCFG}$ does not assert before $\overline{RSTOUT}$ negates, and the lower half of the censorship control word (least significant halfword) equals 0xFFFF or 0x0000, the BOOTCFG field is set to 0b10. Otherwise, if the $\overline{RSTCFG}$ pin was negated at the last negation of $\overline{RSTOUT}$, and the lower half of the censorship control word does not equal 0xFFFF or 0x0000, then the BOOTCFG field is set to the value 0b00. Refer to Table 4-10 for a description of RCHW.
31 RGF	Reset glitch flag. Set by the reset controller when a glitch is detected on the $\overline{RESET}$ pin. This bit is cleared by the assertion of the power-on reset input to the reset controller, or a write of 1 to the RGF bit. Refer to Section 6.4.2.1, “RESET Pin Glitch Detect,” for more information on glitch detection. 0 No glitch has been detected on the $\overline{RESET}$ pin. 1 A glitch has been detected on the $\overline{RESET}$ pin.

Except for a POR request or writing a 1 to the software external reset flag (SERF) bit, all reset requests, regardless of priority are not serviced until the current reset completes.

In the following cases, more than one reset bit is set in the reset status register (SIU_RSR):

Table 6-9. Causes That Set Multiple Reset Status Bits

Case 1	
Condition	• POR request negates and the device remains in the reset • External reset requested • POR and external reset status bits are set
Reason	POR request started the reset sequence, but an external reset request was received before the POR reset sequence ended.
Case 2	
Condition	• Software external reset requested • SERF flag bit set but no previously set bits in the SIU_RSR are cleared
Reason	The SERF flag bit is cleared by writing a 1 (write 1 to clear) to the bit location or when another reset source is asserted.
Case 3	
Condition	• Loss-of-clock reset requested • Loss-of-lock reset requested • Watchdog reset requested • Checkstop reset requested
Reason	More than one reset request occurred on the same clock cycle with no reset request by a higher-priority reset source, therefore the status bits for all the requesting resets are set. Refer to Table 6-7.

6.3.1.3 System Reset Control Register (SIU_SRCR)

The system reset control register configures whether a software system reset or a software external reset is generated. An software system reset uses an internal system reset. An software external reset asserts RSTOUT.

Address: Base + 0x0010 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	SER [1]	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	SSR [2]	w1c														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	CRE [3]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1 Write 1 to the SER bit to generate a software external reset. A write of 0 to this bit has no effect. When the reset completes, the SER bit is cleared to 0.

2 The SSR bit always reads 0. A write of 0 to this bit has no effect.

3 The CRE bit is set to 1 by POR. Other reset sources cannot set the CRE bit.

Figure 6-4. System Reset Control Register (SIU_SRCR)

The following table describes the fields in the system reset control register:

Table 6-10. SIU_SRCR Field Descriptions

Field	Description
0 SSR	Software system reset. The software system reset is processed as a synchronous reset. Except for a software external reset, the bit automatically clears if any other reset source asserts. 0 No software system reset. 1 Generate an software internal system reset.
1 SER	Software external reset. Used to generate a software external reset. Writing a 1 to this bit asserts $\overline{\text{RSTOUT}}$ for 2400 clocks, and the internal reset is not asserted. The bit automatically clears when the software external reset completes or any other reset source is asserted. After a software external reset has been initiated, $\overline{\text{RSTOUT}}$ negates if this bit is cleared before the 2400 clock period expires. 0 Do not generate a software external reset. 1 Generate a software external reset. **Note:** If the FMPLL is configured for dual controller mode, a write of 1 to the SER bit asserts $\overline{\text{RSTOUT}}$ for 16000 clocks. Refer to Section 4.2.2, "Reset Output (RSTOUT)."
2–15	Reserved
16 CRE	Checkstop reset enable. Write a 1 to this bit to enable the checkstop reset request input is asserted. The checkstop reset request input is a synchronous internal reset source. The CRE bit defaults to checkstop reset enabled at POR. If this bit is cleared, it remains cleared until the next POR. 0 No reset occurs when the checkstop reset input to the reset controller is asserted. 1 A reset occurs when the checkstop reset input to the reset controller is asserted.
17–31	Reserved

6.3.1.4 External Interrupt Status Register (SIU_EISR)

The external interrupt status register is used to record edge-triggered events on the $\overline{\text{IRQ}}$[0]–$\overline{\text{IRQ}}$[15] inputs to the SIU. When an edge-detect enable bit is set in the SIU_IREER or SIU_IFEER registers for an IRQ and an IRQ edge-event occurs and is detected, the IRQ flag bit is set in the SIU_EISR. The IRQ flag bits are cleared by writing a 1 to the bit. A write of 0 has no effect.

The IRQ flag bit is set regardless of the state of the DMA or interrupt request enable bit in SIU_DIRER. The IRQ flag bit remains set until cleared by software or through the servicing of a DMA or interrupt request.

Address: Base + 0x0014 Access: R/w1c

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	EIF15	EIF14	EIF13	EIF12	EIF11	EIF10	EIF9	EIF8	EIF7	EIF6	EIF5	EIF4	EIF3	EIF2	EIF1	EIF0
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-5. External Interrupt Status Register (SIU_EISR)

The following table describes the fields in the external interrupt status register:

Table 6-11. SIU_EISR Field Descriptions

Field	Description
0–15	Reserved
16–31 EIF*n*	External interrupt request flag *n.* This bit is set when an edge-triggered event occurs on the corresponding $\overline{\text{IRQ}}$[*n*] input. Cleared by writing a 1. 0 No edge-triggered event has occurred on the corresponding $\overline{\text{IRQ}}$[*n*] input. 1 An edge-triggered event has occurred on the corresponding $\overline{\text{IRQ}}$[*n*] input.

6.3.1.5 DMA Interrupt Request Enable Register (SIU_DIRER)

The SIU_DIRER asserts a DMA transfer or external interrupt request if the IRQ flag bit is set in the SIU_EISR. The DMA transfer or external interrupt request enable bits (EIRE flags) enable an external interrupt request or DMA transfer request. The SIU uses one interrupt request to the interrupt controller. The EIRE bits determine the external interrupt requests that assert the SIU interrupt request to the interrupt controller.

Address: Base + 0x0018 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	EIRE 15	EIRE 14	EIRE 13	EIRE 12	EIRE 11	EIRE 10	EIRE 9	EIRE 8	EIRE 7	EIRE 6	EIRE 5	EIRE 4	EIRE 3	EIRE 2	EIRE 1	EIRE 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-6. DMA Interrupt Request Enable Register (SIU_DIRER)

The following table describes the fields in the DMA interrupt request enable register:

Table 6-12. SIU_DIRER Field Descriptions

Field	Description
0–15	Reserved
16–31 EIRE*n*	External interrupt request enable *n.* Enables the assertion of the interrupt request from the SIU to the interrupt controller when an edge-triggered event occurs on the $\overline{\text{IRQ}}$[*n*] pin. 0 External interrupt request is disabled. 1 External interrupt request is enabled.

6.3.1.6 DMA/Interrupt Request Select Register (SIU_DIRSR)

The SIU_DIRSR selects between a DMA or interrupt request for events on the $\overline{\text{IRQ}}$[0]–$\overline{\text{IRQ}}$[3] inputs. If the IRQ flag bits are set in the external IRQ status register (SIU_EISR) and the DMA/interrupt request enable register (SIU_DIRER), then the select bit in the DMA interrupt request select register (SIU_DIRSR) determines whether a DMA or interrupt request is asserted.

Address: Base + 0x001C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	DIRS 3	DIRS 2	DIRS 1	DIRS 0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-7. DMA/Interrupt Request Select Register (SIU_DIRSR)

The following table describes the fields of the request select register:

Table 6-13. SIU_DIRSR Field Descriptions

Field	Description
0–27	Reserved
28–31 DIRS*n*	DMA interrupt request select *n.* Selects between a DMA transfer or external interrupt request when an edge-triggered event occurs on the corresponding $\overline{\text{IRQ}}$[*n*] pin. 0 Interrupt request is selected. 1 DMA request is selected.Reserved

6.3.1.7 Overrun Status Register (SIU_OSR)

The SIU_OSR flag bits indicate that an overrun has occurred.

Address: Base + 0x0020 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	OVF 15	OVF 14	OVF 13	OVF 12	OVF 11	OVF 10	OVF 9	OVF 8	OVF 7	OVF 6	OVF 5	OVF 4	OVF 3	OVF 2	OVF 1	OVF 0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-8. Overrun Status Register (SIU_OSR)

The following table describes the fields in the overrun status register:

Table 6-14. SIU_OSR Field Descriptions

Field	Description
0–15	Reserved
16–31 OVF*n*	Overrun flag *n*. This bit is set when an overrun occurs on $\overline{\text{IRQ}}$[*n*]. Bit 31 (OVF0) is the overrun flag for $\overline{\text{IRQ}}$[0]; bit 16 (OVF15) is overrun flag for $\overline{\text{IRQ}}$[15]. 0 No overrun occurred. 1 An overrun occurred.

6.3.1.8 Overrun Request Enable Register (SIU_ORER)

The SIU_ORER contains bits to enable an overrun if the corresponding flag bit is set in the SIU_OSR. If the overrun request enable bit and the flag bit are set, the single combined overrun request from the SIU to the interrupt controller is asserted.

Address: Base + 0x0024 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	ORE 15	ORE 14	ORE 13	ORE 12	ORE 11	ORE 10	ORE 9	ORE 8	ORE 7	ORE 6	ORE 5	ORE 4	ORE 3	ORE 2	ORE 1	ORE 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-9. Overrun Request Enable Register (SIU_ORER)

The following table describes the fields in the overrun request enable register:

Table 6-15. SIU_ORER Field Descriptions

Field	Function
0–15	Reserved
16–31 ORE*n*	Overrun request enable *n. E*nables the overrun request when an overrun occurs on the $\overline{\text{IRQ}}$[*n*] pin. Bit 31 (ORE0) is the enable overrun flag for $\overline{\text{IRQ}}$[0]; bit 16 (ORE15) is overrun flag for $\overline{\text{IRQ}}$[15]. 0 Overrun request is disabled. 1 Overrun request is enabled.

6.3.1.9 IRQ Rising-Edge Event Enable Register (SIU_IREER)

The SIU_IREER enables rising edge-triggered events on $\overline{\text{IRQ}}[n]$. Rising- and falling-edge events are enabled by setting the bits in SIU_IREER and SIU_IFEER.

Address: Base + 0x0028 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	IREE 15	IREE 14	IREE 13	IREE 12	IREE 11	IREE 10	IREE 9	IREE 8	IREE 7	IREE 6	IREE 5	IREE 4	IREE 3	IREE 2	IREE 1	IREE 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-10. IRQ Rising-Edge Event Enable Register (SIU_IREER)

The following table describes the fields in the IRQ rising-edge event enable register:

Table 6-16. SIU_IREER Field Descriptions

Field	Function
0–15	Reserved
16–31 IREE*n*	IRQ rising-edge event enable *n.* Enables rising-edge-triggered events on the corresponding $\overline{\text{IRQ}}[n]$ pin. 0 Rising-edge event is disabled. 1 Rising-edge event is enabled.

6.3.1.10 IRQ Falling-Edge Event Enable Register (SIU_IFEER)

The SIU_IFEER enables falling edge-triggered events on $\overline{\text{IRQ}}[n]$. Rising- and falling-edge events are enabled by setting the bits in both SIU_IREER and SIU_IFEER.

Address: Base + 0x002C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	IFEE 15	IFEE 14	IFEE 13	IFEE 12	IFEE 11	IFEE 10	IFEE 9	IFEE 8	IFEE 7	IFEE 6	IFEE 5	IFEE 4	IFEE 3	IFEE 2	IFEE 1	IFEE 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-11. IRQ Falling-Edge Event Enable Register (SIU_IFEER)

The following table describes the fields in the IRQ falling-edge event enable register:

Table 6-17. SIU_IFEER Field Descriptions

Field	Function
0–15	Reserved
16–31 IFEE*n*	IRQ falling-edge event enable *n.* Enables falling-edge-triggered events on the corresponding $\overline{\text{IRQ}}$[*n*] pin. 0 Falling-edge event is disabled. 1 Falling-edge event is enabled.

6.3.1.11 IRQ Digital Filter Register (SIU_IDFR)

The SIU_IDFR specifies the amount of digital filtering on $\overline{\text{IRQ}}$[0]–$\overline{\text{IRQ}}$[15]. The digital filter length field specifies the number of system clocks that define the period of the digital filter and the minimum time an IRQ signal must hold the active state to qualify as an edge-triggered event.

Address: Base + 0x0030 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	DFL			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-12. IRQ Digital Filter Register (SIU_IDFR)

The following table describes the field in the IRQ digital filter register:

Table 6-18. SIU_IDFR Field Descriptions

Field	Function
0–27	Reserved
28–31 DFL	Digital filter length. Defines the digital filter period on the IRQ*n* inputs according to the following equation: $\text{Filter Period} = (\text{SystemClockPeriod} \times 2^{\text{DFL}}) + 1(\text{SystemClockPeriod})$ For a 100 MHz system clock, this gives a range of 20 ns to 328 μs. The minimum time of three clocks accounts for synchronization of the IRQ input pins with the system clock.

6.3.1.12 Pad Configuration Registers (SIU_PCR)

The following subsections define pad configuration registers (PCR) in the SIU_PCR segment. These registers define the pad configuration for all configurable device pins that specify that active function, direction, and electrical attributes for the pin. The information presented pertains to which bits and fields are active for a given pin or group of pins, and the reset state of the register.

The reset state of SIU_PCRs given in this section is the value before the BAM program executes. The BAM program can change some pad configuration registers based on the reset configuration. Refer to the BAM chapter for more detailed information.

The SIU_PCRs are 16-bit registers that are read from or written to as:

- 16-bit values aligned on 16-bit boundaries, or
- 32-bit values aligned on 32-bit address boundaries.

NOTE

The fields available in a SIU_PCR depend on the type of pad it controls. Refer to the SIU_PCR definition.

All device pin names begin with the primary function, followed by the alternate function, and then GPIO. In some cases, the third function can be a secondary alternate, which supersedes the GPIO. Those exceptions are noted in the documentation. For example, SIU_PCR85 configures the CNTXB_PCSC[3]_GPIO[85] muxed signal, where CNTXB is the primary function, PCSC[3] is the alternate function. For identification of the source module for primary and alternate functions, and the description of these signals, refer to Chapter 2, “Signal Description” of this manual. Refer to the chapter for the specific module that uses the signal for an additional signal description.

Figure 6-13 shows a sample PCR register with all bit fields displayed:

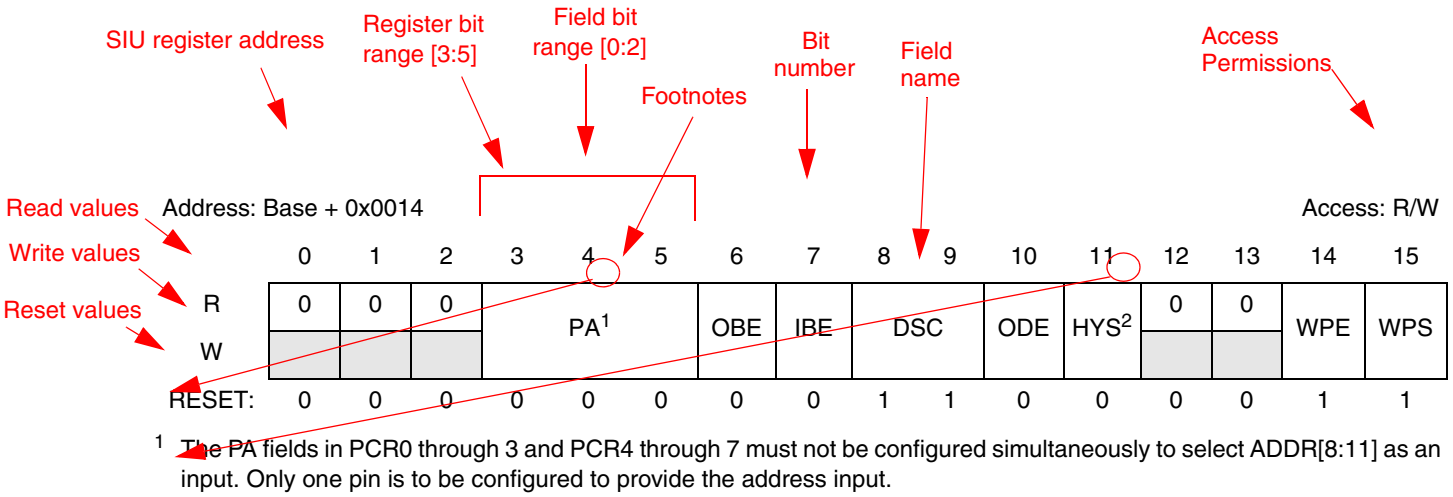


Figure 6-13. Sample PCR Register Description

The following table describes the fields in the pad configuration control registers:

Table 6-19. SIU_PCR Field Descriptions

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>0–2</td><td>Reserved</td></tr>
<tr><td>3–5
PA
[0:2]</td><td>Pin assignment. Selects the function of a multiplexed pad. A separate port enable output signal from the SIU is asserted for each value of this register. The size of the field can be from 1 to 3 bits, depending on the amount of multiplexing on the pad.
<table>
<tr><th colspan="9">PA Bit Field</th><th rowspan="2">Pin Function [1]</th></tr>
<tr><th colspan="3">1-bit [2]
(2 Functions)</th><th colspan="3">2-bit [2]
(4 Functions)</th><th colspan="3">3-bit
(5 Functions)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>GPIO</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Primary function</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Alternate function</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Main primary function [3]</td></tr>
<tr><td colspan="6" rowspan="4">The shaded columns indicate invalid bits in 1- and 2-bit PA fields; the shaded rows indicate invalid values for 3-bit PA fields.</td><td>1</td><td>0</td><td>0</td><td>Alternate function 2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Invalid value</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Invalid value</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Invalid value</td></tr>
</table>
[1] For all SIU_PCRs that do not comply with these rules, the PA definition is given explicitly with the SIU_PCR definition.
[2] For future software compatibility, it is recommended that all PA fields be treated as 3-bit fields, with the unused bits written as 0.
[3] The main primary function is used when the primary function is not available on the package or is used for a different purpose.</td></tr>
<tr><td>6
OBE</td><td>Output buffer enable. Enables the pad as an output and drives the output buffer enable signal.
0 Disable output buffer for the pad.
1 Enable output buffer for the pad is enabled.</td></tr>
<tr><td>7
IBE</td><td>Input buffer enable. Enables the pad as an input and drives the input buffer enable signal.
0 Disable input buffer for the pad.
1 Enable input buffer for the pad is enabled.</td></tr>
<tr><td>8–9
DSC
[0:1]</td><td>Drive strength control. Controls the pad drive strength. Drive strength control pertains to pins with the fast I/O pad type.
00 10 pF drive strength
01 20 pF drive strength
10 30 pF drive strength
11 50 pF drive strength</td></tr>
<tr><td>10
ODE</td><td>Open drain output enable. Controls output driver configuration for the pads. Either open drain or push/pull driver configurations can be selected. This feature applies to output pins only.
0 Disable open drain for the pad (push/pull driver enabled).
1 Enable open drain for the pad.</td></tr>
</table>

Table 6-19. SIU_PCR Field Descriptions

Field	Description
11 HYS	Input hysteresis. Controls whether hysteresis is enabled for the pad. 0 Disable hysteresis for the pad. 1 Enable hysteresis for the pad.
12–13 SRC [0:1]	Slew rate control. Controls slew rate for the pad. Slew rate control pertains to pins with slow or medium I/O pad types, and the output signals are driven according to the value of this field. Actual slew rate depends on the pad type and load. Refer to the electrical specifications for this information. 00 Minimum slew rate 01 Medium slew rate 10 Invalid value 11 Maximum slew rate
14 WPE	Weak pullup/down enable. Controls whether the weak pullup/down devices are enabled/disabled for the pad. Pullup/down devices are enabled by default. 0 Disable weak pull device for the pad. 1 Enable weak pull device for the pad.
15 WPS	Weak pullup/down select. Controls whether weak pullup or weak pulldown devices are used for the pad when weak pullup/down devices are enabled. The WKPCFG pin determines whether pullup or pulldown devices are enabled during reset. The WPS bit determines whether weak pullup or pulldown devices are used after reset, or for pads in which the WKPCFG pin does not determine the reset weak pullup/down state. 0 Pulldown is enabled for the pad. 1 Pullup is enabled for the pad.

6.3.1.13 Pad Configuration Register 0 (SIU_PCR0)

The SIU_PCR0 register controls the function, direction, and electrical attributes of $\overline{CS}$[0]_ADDR[8]_GPIO[0].

Address: Base + 0x0040 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1]		OBE[2]	IBE[3]	DSC		ODE[4]	HYS	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 Do not configure the PA fields in SIU_PCR[0] *and* SIU_PCR[4] to ADDR[8]. Configure only one pin to ADDR[8].

2 When configured as $\overline{CS}$[0] or ADDR[8], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

3 When configured as $\overline{CS}$[0], ADDR[8], or GPDO, set the IBE bit to 1 to show the state in the GPDI register. Clearing the IBE bit to 0 reduces power consumption. When configured as GPDI, set the IBE bit to 1.

4 When configured as $\overline{CS}$[0] or ADDR[8], clear the ODE bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as $\overline{CS}$[0] or ADDR[8].

Figure 6-14. $\overline{CS}$[0]_ADDR[8]_GPIO[0] Pad Configuration Register (SIU_PCR0)

Refer to Table 6-19 for bit field definitions. Table 6-20 lists the PA values for $\overline{CS}$[0]_ADDR[8]_GPIO[0].

Table 6-20. PCR0 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[0]
0b01	$\overline{CS}$[0]
0b10	ADDR[8]
0b11	$\overline{CS}$[0]

6.3.1.14 Pad Configuration Registers 1–3 (SIU_PCR1–SIU_PCR3)

The SIU_PCR1–SIU_PCR3 registers control the function, direction, and electrical attributes of $\overline{CS}$[1:3]_ADDR[9:11]_GPIO[1:3].

Address: Base + (0x0042–0x0046) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1]		OBE[2]	IBE[3]	DSC		ODE[4]	HYS[5]	0	0	WPE[6]	WPS[6]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 Do not configure the PA fields in PCR1–3 and PCR5–7 to select ADDR[9:11]. Configure only one set of pins to ADDR[9:11] for the address input.

2 When configured as $\overline{CS}$[1:3] or ADDR[9:11], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

3 When configured as $\overline{CS}$[1:3], ADDR[9:11], or GPDO, set the IBE bit to 1 to reflect the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

4 When configured as $\overline{CS}$[1:3] or ADDR[9:11], clear the ODE bit to 0.

5 If external master operation is enabled, clear the HYS bit to 0.

6 Refer to the EBI section for weak pullup settings when configured as $\overline{CS}$[1:3] or ADDR[9:11].

Figure 6-15. $\overline{CS}$[1:3]_ADDR[9:11]_GPIO[1:3] Pad Configuration Registers (SIU_PCR1–SIU_PCR3)

Refer to Table 6-19 for bit field definitions. Table 6-21 lists the PA values for $\overline{CS}$[1:3]_ADDR[9:11]_GPIO[1:3].

Table 6-21. PCR1–PCR3 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[1:3]
0b01	$\overline{CS}$[1:3]
0b10	ADDR[9:11]
0b11	$\overline{CS}$[1:3]

6.3.1.15 Pad Configuration Registers 4–7 (SIU_PCR4–SIU_PCR7)

The SIU_PCR4–SIU_PCR7 registers control the function, direction, and electrical attributes of ADDR[8:11]_GPIO[4:7].

Address: Base + (0x0048–0x004E) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA[1]	OBE[2]	IBE[3]	DSC		ODE[4]	HYS[5]	0	0	WPE[6]	WPS[6]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 Do not configure the PA fields in PCR0–3 and PCR4–7 to select ADDR[8:11]. Only configure one set of pins to provide address input.

2 When configured as ADDR[8:11] the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

3 When configured as ADDR[8:11], or GPDO, set the IBE bit to 1 to reflect the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

4 When configured as ADDR[8:11] clear the ODE bit to 0.

5 If external master operation is enabled, clear the HYS bit to 0.

6 Refer to the EBI section for weak pullup settings when configured as ADDR[8:11].

Figure 6-16. ADDR[8:11]_GPIO[4:7] Pad Configuration Registers (SIU_PCR4–SIU_PCR7)

Refer to Table 6-19 for bit field definitions. Table 6-22 lists the PA values for ADDR[8:11]_GPIO[4:7].

Table 6-22. PCR4–PCR7 PA Field Descriptions

PA Field	Pin Function
0b0	GPIO[4:7]
0b1	ADDR[8:11]

6.3.1.16 Pad Configuration Registers 8–22 (SIU_PCR8–SIU_PCR22)

The SIU_PCR8–SIU_PCR22 registers control the function, direction, and electrical attributes of ADDR[12:26]_GPIO[8:22].

Address: Base + (0x0050–0x006C) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as ADDR[12:26], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When configured as ADDR[12:26] or GPDO, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as ADDR[12:26], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as ADDR[8:26].

Figure 6-17. ADDR[12:26]_GPIO[8:22] Pad Configuration Registers (SIU_PCR8–SIU_PCR22)

Refer to Table 6-19 for bit field definitions. Table 6-23 lists the PA field for ADDR[12:26]_GPIO[8:22].

Table 6-23. PCR8–PCR22 PA Field Descriptions

PA Field	Pin Function
0b0	GPIO[8:22]
0b1	ADDR[12:26]

6.3.1.17 Pad Configuration Registers 23–25 (SIU_PCR23–SIU_PCR25)

The SIU_PCR23–SIU_PCR25 registers control the function, direction, and electrical attributes of ADDR[27:29]_GPIO[23:25].

Address: Base + (0x006E–0x0072) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as ADDR[27:29], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When configured as ADDR[27:29] or GPDO, set the IBE bit to 1 to show the value in the GPDI register. Clear the IBE to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as ADDR[27:29], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as ADDR[27:29].

Figure 6-18. ADDR[27:29]_GPIO[23:25] Pad Configuration Registers (SIU_PCR23–SIU_PCR25)

Refer to Table 6-19 for bit field definitions. Table 6-24 lists the PA field for ADDR[27:29]_GPIO[23:25].

Table 6-24. PCR23–PCR25 PA Field Descriptions

PA Field	Pin Function
0b0	GPIO[23:25]
0b1	ADDR[27:29]

6.3.1.18 Pad Configuration Registers 26–27 (SIU_PCR26–SIU_PCR27)

The SIU_PCR26–SIU_PCR27 registers control the function, direction, and electrical attributes of ADDR[30:31]_ADDR[6:7]_GPIO[26:27].

Address: Base + (0x0074–0x0076) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as ADDR[30:31] or ADDR[6:7], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When configured as ADDR[30:31], ADDR[6:7] or GPDO, set the IBE bit to 1 to reflect the pin state in the corresponding GPDI register. Clear the IBE to zero to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as ADDR[30:31] or ADDR[6:7], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as ADDR[30:31] or ADDR[6:7].

Figure 6-19. ADDR[30:31]_ADDR[6:7]_GPIO[26:27] Pad Configuration Registers (SIU_PCR26–SIU_PCR27)

Refer to Table 6-19 for bit field definitions. Table 6-25 lists the PA field for ADDR[30:31]_ADDR[6:7]_GPIO[26:27].

Table 6-25. PCR26–PCR27 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[26:27]
0b01	ADDR[30:31]
0b10	ADDR[6:7]
0b11	ADDR[30:31]

6.3.1.19 Pad Configuration Registers 28–43 (SIU_PCR28–SIU_PCR43)

The SIU_PCR28–SIU_PCR43 registers control the function, direction, and electrical attributes of DATA[0:15]_GPIO[28:43].

Address: Base + (0x0078–0x0096) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[0:15], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When configured as DATA[0:15] or GPDO, set the IBE bit to 1 to reflect the pin state in the GPDI register. Clear the IBE to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[0:15], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[0:15].

Figure 6-20. DATA[0:15]_GPIO[28:43] Pad Configuration Registers (SIU_PCR28–SIU_PCR43)

6.3.1.20 Pad Configuration Registers 44 (SIU_PCR44)

The SIU_PCR44 register controls the function, direction, and electrical attributes of DATA[16]_FEC_TX_CLK_GPIO[44].

Address: Base + 0x0098 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[16] or FEC_TX_CLK, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When configured as DATA[16] or FEC_TX_CLK, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[16], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[16].

Figure 6-21. DATA[16]_FEC_TX_CLK_GPIO[44] Pad Configuration Registers (SIU_PCR44)

6.3.1.21 Pad Configuration Registers 45 (SIU_PCR45)

The SIU_PCR45 register controls the function, direction, and electrical attributes of DATA[17]_FEC_CRS_GPIO[45].

Address: Base + 0x009A Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[17] or FEC_CRS, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When configured as DATA[17] or FEC_CRS, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[17], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[17].

Figure 6-22. DATA[17]_FEC_CRS_GPIO[45] Pad Configuration Registers (SIU_PCR45)

6.3.1.22 Pad Configuration Registers 46 (SIU_PCR46)

The SIU_PCR46 register controls the function, direction, and electrical attributes of DATA[18]_FEC_TX_ER_GPIO[46].

Address: Base + 0x009C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[18] or FEC_TX_ER, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When configured as DATA[18], FEC_TX_ER, or GPDO, set the IBE bit to 1 show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[18], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[18] or FEC_TX_ER.

Figure 6-23. DATA[18]_FEC_TX_ER_GPIO[46] Pad Configuration Registers (SIU_PCR46)

6.3.1.23 Pad Configuration Registers 47 (SIU_PCR47)

The SIU_PCR47 register controls the function, direction, and electrical attributes of DATA[19]_FEC_RX_CLK_GPIO[47].

Address: Base + 0x009E Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[19] or FEC_RX_CLK, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[19], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[19] or FEC_RX_CLK.

Figure 6-24. DATA[19]_FEC_RX_CLK_GPIO[47] Pad Configuration Registers (SIU_PCR47)

6.3.1.24 Pad Configuration Registers 48 (SIU_PCR48)

The SIU_PCR48 register controls the function, direction, and electrical attributes of DATA[20]_FEC_TXD[0]_GPIO[48].

Address: Base + 0x00A0 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[20] or FEC_TXD[0], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[20], set the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[20].

Figure 6-25. DATA[20]_FEC_TXD[0]_GPIO[48] Pad Configuration Registers (SIU_PCR48)

6.3.1.25 Pad Configuration Registers 49 (SIU_PCR49)

The SIU_PCR49 register controls the function, direction, and electrical attributes of DATA[21]_FEC_RX_ER_GPIO[49].

Address: Base + 0x00A2 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[21] or FEC_RX_ER, the OBE bit has no effect. When configured as GPDO (output), set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[21] or FEC_RX_ER, clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[21] or FEC_RX_ER.

Figure 6-26. DATA[21]_FEC_RX_ER_GPIO[49] Pad Configuration Registers (SIU_PCR49)

Refer to Table 6-19 for bit field definitions. Table 6-26 lists the PA fields for DATA[21]_FEC_RX_ER_GPIO[49].

Table 6-26. PCR49 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[49]
0b01	DATA[21]
0b10	FEC_RX_ER
0b11	DATA[21]

6.3.1.26 Pad Configuration Registers 50 (SIU_PCR50)

The SIU_PCR50 register controls the function, direction, and electrical attributes of DATA[22]_FEC_RXD[0]_GPIO[50].

Address: Base + 0x00A4 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[22] FEC_RXD[0], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[22]FEC_RXD[0], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[22] FEC_RXD[0].

Figure 6-27. DATA[22]_FEC_RXD[0]_GPIO[50] Pad Configuration Registers (SIU_PCR50)

Refer to Table 6-19 for bit field definitions. Table 6-27 lists the PA fields for DATA[22]_FEC_RXD[0]GPIO[50].

Table 6-27. PCR50 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[50]
0b01	DATA[22]
0b10	FEC_RXD[0]
0b11	DATA[22]

6.3.1.27 Pad Configuration Registers 51 (SIU_PCR51)

The SIU_PCR51 register controls the function, direction, and electrical attributes of DATA[23]_FEC_TXD[3]_GPIO[51].

Address: Base + 0x00A6 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[23] or FEC_TXD[3], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[23] or FEC_TXD[3], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[23] or FEC_TXD[3].

Figure 6-28. DATA[23]_FEC_TXD[3]_GPIO[51] Pad Configuration Registers (SIU_PCR51)

Refer to Table 6-19 for bit field definitions. Table 6-28 lists the PA fields for DATA[23]_FEC_TXD[3]_GPIO[51].

Table 6-28. PCR51 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[51]
0b01	DATA[23]
0b10	FEC_TXD[3]
0b11	DATA[23]

6.3.1.28 Pad Configuration Registers 52 (SIU_PCR52)

The SIU_PCR52 register controls function, direction, and electrical attributes of DATA[24]_FEC_COL_GPIO[52].

Address: Base + 0x00A8 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[24] or FEC_COL, the OBE bit has no effect.
When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to put the pin state in the GPDI register.
Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[24] or FEC_COL, clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[24] or FEC_COL.

Figure 6-29. DATA[24]_FEC_COL_GPIO[52] Pad Configuration Registers (SIU_PCR52)

Refer to Table 6-19 for bit field definitions. Table 6-29 lists the PA fields for DATA[24]_FEC_COL_GPIO[52].

Table 6-29. PCR52 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[52]
0b01	DATA[24]
0b10	FEC_COL
0b11	DATA[24]

6.3.1.29 Pad Configuration Registers 53 (SIU_PCR53)

The SIU_PCR53 register controls the function, direction, and electrical attributes of DATA[25]_FEC_RX_DV_GPIO[53].

Address: Base + 0x00AA Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[25] or FEC_RX_DV, the OBE bit has no effect.
When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the corresponding GPDI register.
Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[25] or FEC_RX_DV, clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[25] or FEC_RX_DV.

Figure 6-30. DATA[25]_FEC_RX_DV_GPIO[53] Pad Configuration Registers (SIU_PCR53)

Refer to Table 6-19 for bit field definitions. Table 6-30 lists the PA fields for DATA[25]_FEC_RX_DV_GPIO[53].

Table 6-30. PCR53 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[53]
0b01	DATA[25]
0b10	FEC_RX_DV
0b11	DATA[25]

6.3.1.30 Pad Configuration Registers 54 (SIU_PCR54)

The SIU_PCR54 register controls the function, direction, and electrical attributes of DATA[26]_FEC_TX_EN_GPIO[54].

Address: Base + 0x00AC — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[26] or FEC_TX_EN, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to reflect the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[26] or FEC_TX_EN, clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[26] or FEC_TX_EN.

Figure 6-31. DATA[26]_FEC_TX_EN_GPIO[54] Pad Configuration Registers (SIU_PCR54)

Refer to Table 6-19 for bit field definitions. Table 6-31 lists the PA fields for DATA[26]_FEC_TX_EN_GPIO[54].

Table 6-31. PCR54 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[54]
0b01	DATA[26]
0b10	FEC_RX_DV
0b11	DATA[26]

6.3.1.31 Pad Configuration Registers 55 (SIU_PCR55)

The SIU_PCR55 register controls the function, direction, and electrical attributes of DATA[27]_FEC_TXD[2]_GPIO[55].

Address: Base + 0x00AE Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[27] or FEC_TXD[2], the OBE bit has no effect.
When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 shows the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[27] or FEC_TXD[2], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[27] or FEC_TXD[2].

Figure 6-32. DATA[27]_FEC_TXD[2]_GPIO[55] Pad Configuration Registers (SIU_PCR55)

Refer to Table 6-19 for bit field definitions. Table 6-32 lists the PA fields for DATA[27]_FEC_TXD[2]_GPIO[55].

Table 6-32. PCR55 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[55]
0b01	DATA[27]
0b10	FEC_TXD[2]
0b11	DATA[27]

6.3.1.32 Pad Configuration Registers 56 (SIU_PCR56)

The SIU_PCR56 register controls the function, direction, and electrical attributes of DATA[28]_FEC_TXD[1]_GPIO[56].

Address: Base + 0x00B0 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[28] or FEC_TXD[1], the OBE bit has no effect.
When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register.
Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[28] or FEC_TXD[1], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[28] or FEC_TXD[1].

Figure 6-33. DATA[28]_FEC_TXD[1]_GPIO[56] Pad Configuration Registers (SIU_PCR56)

Refer to Table 6-19 for bit field definitions. Table 6-33 lists the PA fields for DATA[28]_FEC_TXD[1]_GPIO[56].

Table 6-33. PCR56 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[56]
0b01	DATA[28]
0b10	FEC_TXD[1]
0b11	DATA[28]

6.3.1.33 Pad Configuration Registers 57 (SIU_PCR57)

The SIU_PCR57 register controls the function, direction, and electrical attributes of DATA[29]_FEC_RXD[1]_GPIO[57].

Address: Base + 0x00B2 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[29] or FEC_RXD[1], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[29] or FEC_RXD[1], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[29] or FEC_RXD[1].

Figure 6-34. DATA[29]_FEC_RXD[1]_GPIO[57] Pad Configuration Registers (SIU_PCR57)

Refer to Table 6-19 for bit field definitions. Table 6-34 lists the PA fields for DATA[29]_FEC_RXD[1]_GPIO[57].

Table 6-34. PCR57 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[57]
0b01	DATA[29]
0b10	FEC_RXD[1]
0b11	DATA[29]

6.3.1.34 Pad Configuration Registers 58 (SIU_PCR58)

The SIU_PCR58 register controls the function, direction, and electrical attributes of DATA[30]_FEC_RXD[2]_GPIO[58].

Address: Base + 0x00B4 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[30] or FEC_RXD[2], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[30] or FEC_RXD[2], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[30] or FEC_RXD[2].

Figure 6-35. DATA[30]_FEC_RXD[2]_GPIO[58] Pad Configuration Registers (SIU_PCR58)

Refer to Table 6-19 for bit field definitions. Table 6-35 lists the PA fields for DATA[30]_FEC_RXD[2]_GPIO[58].

Table 6-35. PCR58 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[58]
0b01	DATA[30]
0b10	FEC_RXD[2]
0b11	DATA[30]

6.3.1.35 Pad Configuration Registers 59 (SIU_PCR59)

The SIU_PCR59 register controls the function, direction, and electrical attributes of DATA[31]_FEC_RXD[3]_GPIO[59].

Address: Base + 0x00B6 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as DATA[31] or FEC_RXD[3], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as DATA[31] or FEC_RXD[3], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as DATA[31] or FEC_RXD[3].

Figure 6-36. DATA[31]_FEC_RXD[3]_GPIO[59] Pad Configuration Registers (SIU_PCR59)

Refer to Table 6-19 for bit field definitions. Table 6-36 lists the PA fields for DATA[31]_FEC_RXD[3]_GPIO[59].

Table 6-36. PCR59 PA Field Descriptions

PA Field	Pin Function
0b00	GPIO[59]
0b01	DATA[31]
0b10	FEC_RXD[3]
0b11	DATA[31]

6.3.1.36 Pad Configuration Registers 60–61 (SIU_PCR60–SIU_PCR61)

The SIU_PCR60–SIU_PCR61 registers control the function, direction, and electrical attributes of TSIZ[0:1]_GPIO[60:61].

Address: Base + (0x00B8–0x00BA) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as TSIZ[0:1], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as TSIZ[0:1], clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as TSIZ[0:1].

Figure 6-37. TSIZ[0:1]_GPIO[60:61] Pad Configuration Register (SIU_PCR60–SIU_PCR61)

Refer to Table 6-19 for bit field definitions. Table 6-46 lists the PA fields for TSIZ[0:1]_GPIO[60:61].

Table 6-37. PCR60–PCR61 PA Field Definition

PA Field	Pin Function
0b0	GPIO[60:61]
0b1	TSIZ[0:1]

6.3.1.37 Pad Configuration Register 62 (SIU_PCR62)

The SIU_PCR62 register controls the function, direction, and electrical attributes of RD_$\overline{WR}$_GPIO[62].

Address: Base + 0x00BC — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as RD_$\overline{WR}$, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as RD_$\overline{WR}$, clear the ODE bit to 0.

4 When external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as RD_$\overline{WR}$.

Figure 6-38. RD_$\overline{WR}$_GPIO[62] Pad Configuration Register (SIU_PCR62)

Refer to Table 6-19 for bit field definitions. Table 6-46 lists the PA fields for RD_$\overline{WR}$_GPIO[62].

Table 6-38. PCR62 PA Field Definition

PA Field	Pin Function
0b0	GPIO[62]
0b1	RD_$\overline{WR}$

6.3.1.38 Pad Configuration Register 63 (SIU_PCR63)

The SIU PCR63 register controls the function, direction, and electrical attributes of $\overline{BDIP}$_GPIO[63].

Address: Base + 0x00BE — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	DSC		ODE[3]	HYS	0	0	WPE[4]	WPS[4]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as $\overline{BDIP}$, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as $\overline{BDIP}$, clear the ODE bit to 0.

4 Refer to the EBI section for weak pullup settings when configured as $\overline{BDIP}$.

Figure 6-39. $\overline{BDIP}$_GPIO[63] Pad Configuration Register (SIU_PCR63)

Refer to Table 6-19 for bit field definitions. Table 6-46 lists the PA fields for $\overline{BDIP}$_GPIO[63].

Table 6-39. PCR63 PA Field Definition

PA Field	Pin Function
0b0	GPIO[63]
0b1	$\overline{BDIP}$

6.3.1.39 Pad Configuration Registers 64–65 (SIU_PCR64–SIU_PCR65)

The SIU_PCR64–SIU_PCR65 registers control the function, direction, and electrical attributes of $\overline{WE}/\overline{BE}$[0:1]_GPIO[64:65]. The PA bit in PCR64 and PCR65 registers select between the write/byte enable functions and the GPIO functions. The WEBS bit in the EBI base registers selects between the write-enable function and byte-enable function.

Address: Base + (0x00C0–0x00C2) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	DSC		ODE[3]	HYS	0	0	WPE[4]	WPS[4]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as $\overline{WE}/\overline{BE}$[0:1], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as $\overline{WE}$/ $\overline{BE}$[0:1], clear the ODE bit to 0.

4 Refer to the EBI section for weak pullup settings when configured as $\overline{WE}$/ $\overline{BE}$[0:1].

Figure 6-40. $\overline{WE}/\overline{BE}$[0:1]_GPIO[64:65] Pad Configuration Registers (SIU_PCR64–SIU_PCR65)

Refer to Table 6-19 for bit field definitions. Table 6-46 lists the PA fields for $\overline{WE}/\overline{BE}$[0:1]_GPIO[64:65].

Table 6-40. PCR64–PCR65 PA Field Definition

PA Field	Pin Function
0b0	GPIO[64:65]
0b1	$\overline{WE}/\overline{BE}$[1:0]

6.3.1.40 Pad Configuration Registers 66–67 (SIU_PCR66–SIU_PCR67)

The SIU_PCR66–SIU_PCR67 registers control the function, direction, and electrical attributes of $\overline{WE}/\overline{BE}$[2:3]_GPIO[66:67]. The PA bit in the PCR66 and PCR67 registers select between write/byte enable functions and the GPIO functions. The WEBS bit in the EBI base registers selects between the write-enable ($\overline{WE}$) function and byte-enable ($\overline{BE}$) function.

Address: Base + (0x00C4–0x00C6) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	DSC		ODE[3]	HYS	0	0	WPE[4]	WPS[4]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as $\overline{WE}/\overline{BE}$[2:3], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as $\overline{WE}/\overline{BE}$[2:3], clear the ODE bit to 0.

4 Refer to the EBI section for weak pullup settings when configured as $\overline{WE}/\overline{BE}$[2:3].

Figure 6-41. $\overline{WE}/\overline{BE}$[2:3]_GPIO[66:67] Pad Configuration Registers (SIU_PCR66–SIU_PCR67)

Refer to Table 6-19 for bit field definitions. Table 6-46 lists the PA fields for $\overline{WE}/\overline{BE}$[2:3]_GPIO[66:67].

Table 6-41. PCR66–PCR67 PA Field Definition

PA Field	Pin Function
0b0	GPIO[66:67]
0b1	$\overline{WE}/\overline{BE}$[2:3]

6.3.1.41 Pad Configuration Register 68 (SIU_PCR68)

The SIU_PCR68 register controls the function, direction, and electrical attributes of the $\overline{OE}$_GPIO[68].

Address: Base + 0x00C8 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as $\overline{OE}$, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as $\overline{OE}$, clear the ODE bit to 0.

4 When EBI is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as $\overline{OE}$.

Figure 6-42. $\overline{OE}$_GPIO[68] Pad Configuration Register (SIU_PCR68)

Refer to Table 6-19 for bit field definitions. Table 6-46 lists the PA fields for $\overline{OE}$_GPIO[68].

Table 6-42. PCR68 PA Field Definition

PA Field	Pin Function
0b0	GPIO[68]
0b1	$\overline{OE}$

6.3.1.42 Pad Configuration Register 69 (SIU_PCR69)

The SIU_PCR69 register controls the function, direction, and electrical attributes of the $\overline{TS}$_GPIO[69].

Address: Base + 0x00CA Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as $\overline{TS}$, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as $\overline{TS}$, clear the ODE bit to 0.

4 When EBI is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as $\overline{TS}$.

Figure 6-43. $\overline{TS}$_GPIO[69] Pad Configuration Register (SIU_PCR69)

Refer to Table 6-19 for bit field definitions. Table 6-43 lists the PA fields for $\overline{TS}$_GPIO[69].

Table 6-43. PCR69 PA Field Definition

PA Field	Pin Function
0b0	GPIO[69]
0b1	$\overline{TS}$

6.3.1.43 Pad Configuration Register 70 (SIU_PCR70)

The SIU_PCR70 register controls the function, direction, and electrical attributes of the $\overline{TA}$_GPIO[70].

Address: Base + 0x00CC Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as $\overline{TA}$, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as $\overline{TA}$ and external master operation is enabled, clear the ODE bit to 0.

4 When EBI is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as $\overline{TA}$.

Figure 6-44. $\overline{TA}$_GPIO[70] Pad Configuration Register (SIU_PCR70)

Refer to Table 6-19 for bit field definitions. Table 6-46 lists the PA fields for $\overline{TA}$_GPIO[70].

Table 6-44. PCR70 PA Field Definition

PA Field	Pin Function
0b0	GPIO[70]
0b1	$\overline{TA}$

6.3.1.44 Pad Configuration Register 71 (SIU_PCR71)

The SIU_PCR71 register controls the function, direction, and electrical attributes of $\overline{TEA}$_GPIO[71].

Address: Base + 0x00CE Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

1 When configured as $\overline{\text{TEA}}$, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as $\overline{\text{TEA}}$ and external master operation is enabled, clear the ODE bit to 0.

4 When EBI is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as $\overline{\text{TEA}}$.

Figure 6-45. $\overline{\text{TEA}}$_GPIO[71] Pad Configuration Register (SIU_PCR71)

Refer to Table 6-19 for bit field definitions. Table 6-45 lists the PA fields for $\overline{\text{TEA}}$_GPIO[71].

Table 6-45. PCR71 PA Field Definition

PA Field	Pin Function
0b0	GPIO[71]
0b1	$\overline{\text{TEA}}$

6.3.1.45 Pad Configuration Register 72 (SIU_PCR72)

The SIU_PCR72 register controls the function, direction, and electrical attributes of $\overline{\text{BR}}$_FEC_MDC_GPIO[72]. This register allows selection of the GPIO functions.

Figure 6-46. To use the $\overline{\text{BR}}$ function, the PA field must be set to $\overline{\text{BR}}$ before EBI_MCR[EXTM] is set.

$\overline{\text{BR}}$_FEC_MDC_GPIO[72] Pad Configuration Register (SIU_PCR72)

Address: Base + 0x00D0 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE	IBE	DSC		ODE[1]	HYS	0	0	WPE	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as BR and external master operation is enabled, clear the ODE bit to 0.

Refer to Table 6-19 for bit field definitions. Table 6-46 lists the PA field for $\overline{\text{BR}}$_FEC_MDC_GPIO[72].

Table 6-46. PCR72 PA Field Definition

PA Field	Pin Function
0b00	GPIO[72]
0b01	$\overline{\text{BR}}$
0b10	FEC_MDC
0b11	Invalid value

6.3.1.46 Pad Configuration Register 73 (SIU_PCR73)

The SIU_PCR73 register controls the function, direction, and electrical attributes of $\overline{BG}$_FEC_MDIO_GPIO[73]. This register allows selection of GPIO functions.

To use the $\overline{BG}$ function, the PA field must be set to $\overline{BG}$ before EBI_MCR[EXTM] is set.

Address: Base + 0x00D2 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as $\overline{BG}$ or FEC_MDIO, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as $\overline{BG}$ or FEC_MDIO, clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as $\overline{BG}$ or FEC_MDIO.

Figure 6-47. $\overline{BG}$_FEC_MDIO_GPIO[73] Pad Configuration Register (SIU_PCR73)

Refer to Table 6-19 for bit field definitions. Table 6-47 lists the PA field for $\overline{BG}$_FEC_MDIO_GPIO[73].

Table 6-47. PCR73 PA Field Definition

PA Field	Pin Function
0b00	GPIO[73]
0b01	$\overline{BG}$
0b10	FEC_MDIO
0b11	Invalid value

6.3.1.47 Pad Configuration Register 74 (SIU_PCR74)

The SIU_PCR74 register controls the function, direction, and electrical attributes of $\overline{BB}$_GPIO[74]. This register allows selection of the GPIO function. To use the $\overline{BB}$ function, the PA field must be set to $\overline{BB}$ before EBI_MCR[EXTM] is set.

Address: Base + 0x00D2 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	DSC		ODE[3]	HYS[4]	0	0	WPE[5]	WPS[5]
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as $\overline{BB}$, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

3 When configured as $\overline{BB}$, clear the ODE bit to 0.

4 If external master operation is enabled, clear the HYS bit to 0.

5 Refer to the EBI section for weak pullup settings when configured as $\overline{BB}$.

Figure 6-48. $\overline{BB}$_GPIO[74] Pad Configuration Register PCR74

Refer to Table 6-19 for bit field definitions. Table 6-48 lists the PA field for $\overline{BB}$_GPIO[74].

Table 6-48. PCR74 PA Field Definition

PA Field	Pin Function
0b00	GPIO[74]
0b01	$\overline{BB}$
0b10	Invalid value
0b11	Invalid value

6.3.1.48 Pad Configuration Register 82–75 (SIU_PCR82–SIU_PCR75)

The SIU_PCR82–SIU_PCR75 registers control the function, direction, and electrical attributes of MDO[11:4]_GPIO[82:75]. GPIO is the default function at reset.

The Full Port Mode (FPM) bit in the Nexus Port Controller (NPC) pad configuration register controls whether the pins function as MDO[11:4] or GPIO[82:75]. The pad interface port enable is driven by the NPC block. When the FPM bit is set, the NPC enables the MDO port enable, and disables GPIO. When the FPM bit is cleared, the NPC disables the MDO port enable, and enables GPIO.

Address: Base + (0x00E4–0x00D6) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	OBE[1]	IBE[1]	DSC		ODE[2]	HYS[3]	0	0	WPE[4]	WPS
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

1 This bit applies only to GPIO operation.

2 Clear the ODE bit to 0 for MDO operation.

3 The HYS bit has no effect on MDO operation.

4 Clear the WPE bit to 0 for MDO operation.

Figure 6-49. MDO[11:4]_GPIO[82:75] Pad Configuration Register (SIU_PCR82–SIU_PCR75)

6.3.1.49 Pad Configuration Register 83 (SIU_PCR83)

The SIU_PCR83 register controls the function, direction, and electrical attributes of CNTXA_TXDA_GPIO[83].

Address: Base + 0x00E6 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as CNTXA or TXDA, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-50. CNTXA_TXDA_GPIO[83] Pad Configuration Register (SIU_PCR83)

Refer to Table 6-19 for bit field definitions. Table 6-49 lists the PA fields for CNTXA_TXDA_GPIO[83].

Table 6-49. PCR83 PA Field Definition

PA Field	Pin Function
0b00	GPIO[83]
0b01	CNTXA
0b10	TXDA
0b11	CNTXA

6.3.1.50 Pad Configuration Register 84 (SIU_PCR84)

The SIU_PCR84 register controls the pin function, direction, and electrical attributes of CNRXA_RXDA_GPIO[84].

Address: Base + 0x00E8 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as CNRXA or RXDA, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-51. CNRXA_RXDA_GPIO[84] Pad Configuration Register (SIU_PCR84)

Refer to Table 6-19 for bit field definitions. Table 6-50 lists the PA fields for CNRXA_RXDA_GPIO[84].

Table 6-50. PCR84 PA Field Definition

PA Field	Pin Function
0b00	GPIO[84]
0b01	CNRXA
0b10	RXDA
0b11	CNRXA

6.3.1.51 Pad Configuration Register 85 (SIU_PCR85)

The SIU_PCR85 register controls the function, direction, and electrical attributes of CNTXB_PCSC[3]_GPIO[85]. This register allows selection of the CNTXB, PCSC[3] and GPIO functions.

Address: Base + 0x00EA Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as CNTXB or PCSC[3], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-52. CNTXB_PCSC[3]_GPIO[85] Pad Configuration Register (SIU_PCR85)

Refer to Table 6-19 for bit field definitions. Table 6-51 lists the PA fields for CNTXB_PCSC[3]_GPIO[85].

Table 6-51. PCR85 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[85]
0b01	CNTXB
0b10	PCSC[3]
0b11	CNTXB

6.3.1.52 Pad Configuration Register 86 (SIU_PCR86)

The SIU_PCR86 register controls the function, direction, and electrical attributes of CNRXB_PCSC[4]_GPIO[86]. This register allows selection of the CNRXB,_PCSC[4], and GPIO[86] functions.

Address: Base + 0x00EC — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as CNRXB or PCSC[4], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-53. CNRXB_PCSC[4]_GPIO[86] Pad Configuration Register (SIU_PCR86)

Refer to Table 6-19 for bit field definitions. Table 6-52 lists the PA fields for CNRXB_PCSC[4]_GPIO[86].

Table 6-52. PCR86 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[86]
0b01	CNRXB
0b10	PCSC[4]
0b11	CNRXB

6.3.1.53 Pad Configuration Register 87 (SIU_PCR87)

The SIU_PCR87 register controls the function, direction, and electrical attributes of CNTXC_PCSD[3]_GPIO[87].

Address: Base + 0x00EE Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as CNTXC or PCSD[3], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-54. CNTXC_PCSD[3]_GPIO[87] Pad Configuration Register (SIU_PCR87)

Refer to Table 6-19 for bit field definitions. Table 6-53 lists the PA fields for CNTXC_PCSD[3]_GPIO[87].

Table 6-53. PCR87 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[87]
0b01	CNTXC
0b10	PCSD[3]
0b11	CNTXC

6.3.1.54 Pad Configuration Register 88 (SIU_PCR88)

The SIU_PCR88 register controls the function, direction, and electrical attributes of CNRXC_PCSD[4]_GPIO[88].

Address: Base + 0x00F0 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as CNRXC or PCSD[4], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-55. CNRXC_PCSD[4]_GPIO[88] Pad Configuration Register (SIU_PCR88)

Refer to Table 6-19 for bit field definitions. Table 6-54 lists the PA fields for CNRXC_PCSD[4]_GPIO[88].

Table 6-54. PCR88 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[88]
0b01	CNRXC
0b10	PCSD[4]
0b11	CNRXC

6.3.1.55 Pad Configuration Register 89 (SIU_PCR89)

The SIU_PCR89 register controls the function, direction, and electrical attributes of TXDA_GPIO[89].

Address: Base + 0x00F2 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as TXDA, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured for eSCI loop back operation or GPDI, set the IBE bit to 1.

Figure 6-56. TXDA_GPIO[89] Pad Configuration Register (SIU_PCR89)

Refer to Table 6-19 for bit field definitions. Table 6-55 lists the PA fields for TXDA_GPIO[89].

Table 6-55. PCR89 PA Field Definitions

PA Field	Pin Function
0b0	GPIO[89]
0b1	TXDA

6.3.1.56 Pad Configuration Register 90 (SIU_PCR90)

The SIU_PCR90 register controls the function, direction, and electrical attributes of RXDA_GPIO[90].

Address: Base + 0x00F4 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as RXDA, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-57. RXDA_GPIO[90] Pad Configuration Register (SIU_PCR90)

Refer to Table 6-19 for bit field definitions. Table 6-56 lists the PA fields for TXDA_GPIO[90].

Table 6-56. PCR90 PA Field Definitions

PA Field	Pin Function
0b0	GPIO[90]
0b1	RXDA

6.3.1.57 Pad Configuration Register 91 (SIU_PCR91)

The SIU_PCR91 register controls the function, direction, and electrical attributes of TXDB_PCSD[1]_GPIO[91].

Address: Base + 0x00F6 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as TXDB or PCSD[1], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured for eSCI loop back operation or GPDI, set the IBE bit to 1.

Figure 6-58. TXDB_PCSD[1]_GPIO[91] Pad Configuration Register (SIU_PCR91)

Refer to Table 6-19 for bit field definitions. Table 6-57 lists the PA fields for TXDB_PCSD[1]_GPIO[91].

Table 6-57. PCR91 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[91]
0b01	TXDB
0b10	PCSD[1]
0b11	TXDB

6.3.1.58 Pad Configuration Register 92 (SIU_PCR92)

The SIU_PCR92 register controls the function, direction, and electrical attributes of RXDB_PCSD[5]_GPIO[92].

Address: Base + 0x00F8 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as RXDB or PCSD[5], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-59. RXDB_PCSD[5]_GPIO[92] Pad Configuration Register (SIU_PCR92)

Refer to Table 6-19 for bit field definitions. Table 6-58 lists the PA fields for RXDB_PCSD[5]_GPIO[92].

Table 6-58. PCR92 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[92]
0b01	RXDB
0b10	PCSD[5]
0b11	RXDB

6.3.1.59 Pad Configuration Register 93 (SIU_PCR93)

The SIU_PCR93 register controls the function, direction, and electrical attributes of SCKA_PCSC[1]_GPIO[93]. This register allows selection of the PCSC[1] and GPIO functions.

Address: Base + 0x00FA — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1]		OBE[2]	IBE[3]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 The SCKA function is available on the MPC5566 only.

2 When SCKA is configured for master operation, set the OBE bit to 1, or clear to 0 for slave operation. When configured as GPDO, set the OBE bit to 1.

3 When configured as SCKA in slave operation, set the IBE bit to 1. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-60. SCKA_PCSC[1]_GPIO[93] Pad Configuration Register (SIU_PCR93)

Refer to Table 6-19 for bit field definitions. Table 6-59 lists the PA fields for SCKA_PCSC[1]_GPIO[93].

Table 6-59. PCR93 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[93]
0b01	SCKA
0b10	PCSC[1]
0b11	Invalid value

6.3.1.60 Pad Configuration Register 94 (SIU_PCR94)

The SIU_PCR94 register controls the function, direction, and electrical attributes of SINA_PCSC[2]_GPIO[94]. This register allows selection of the SINA, PCSC[2] and GPIO functions.

Address: Base + 0x00FC Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1]		OBE[2]	IBE[3]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 The SINA function is available on the MPC5566 only.

2 When configured as SINA or PCSC[2], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

3 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-61. SINA_PCSC[2]_GPIO[94] Pad Configuration Register (SIU_PCR94)

Refer to Table 6-19 for bit field definitions. Table 6-60 lists the PA fields for SINA_PCSC[2]_GPIO[94].

Table 6-60. PCR94 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[94]
0b01	SINA
0b10	PCSC[2]
0b11	SINA

6.3.1.61 Pad Configuration Register 95 (SIU_PCR95)

The SIU_PCR95 register controls the function, direction, and electrical attributes of SOUTA_PCSC[5]_GPIO[95]. This register allows selection of the SOUTA, PCSC[5] and GPIO[95] functions.

Address: Base + 0x00FE Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1]		OBE[2]	IBE[3]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 The SOUTA function is available on the MPC5566 only.

2 When configured as SOUTA or PCSC[5], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

3 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-62. SOUTA_PCSC[5]_GPIO[95] Pad Configuration Register (SIU_PCR95)

Refer to Table 6-19 for bit field definitions. Table 6-61 lists the PA fields for SOUTA_PCSC[5]_GPIO[95].

Table 6-61. PCR95 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[95]
0b01	SOUTA
0b10	PCSC[5]
0b11	SOUTA

6.3.1.62 Pad Configuration Registers 96 (SIU_PCR96)

The SIU_PCR96 registers control the function, direction, and electrical attributes of PCSA[0]_PCSD[2]_GPIO[96]. This register allows selection of the PCSA[0], PCSD[2] and GPIO functions.

Address: Base + 0x0100 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1]		OBE[2]	IBE[3]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 The PCSA[0] function is available on the MPC5566 only.

2 When configured as PSCA[0], set the OBE bit to 1 for master operation, and clear to 0 for slave operation. When configures as PCSD[2], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

3 When configured as PCSA[0] in slave operation, set the IBE bit to 1. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-63. PCSA[0]_PCSD[2]_GPIO[96] Pad Configuration Register (SIU_PCR96)

Refer to Table 6-19 for bit field definitions. Table 6-62 lists the PA fields for PCSA[0]_PCSD[2]_GPIO[96].

Table 6-62. PCR96 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[96]
0b01	PCSA[0]
0b10	PCSD[2]
0b11	PCSA[0]

6.3.1.63 Pad Configuration Registers 97 (SIU_PCR97)

The SIU_PCR97 registers control the function, direction, and electrical attributes of PCSA[1]_PCSB[2]_GPIO[97]. This register allows selection of the PCSA[1], PCSB[2] and GPIO functions.

Address: Base + 0x0102 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1]		OBE[2]	IBE[3]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 The PCSA[1] function is available on the MPC5566 only.

2 When configured as PCSA[1] or PCSB[2], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

3 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-64. PCSA[1]_PCSB[2]_GPIO[97] Pad Configuration Register (SIU_PCR97)

Refer to Table 6-19 for bit field definitions. Table 6-63 lists the PA fields for PCSA[1]_PCSB[2]_GPIO[97].

Table 6-63. PCR97 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[97]
0b01	PCSA[1]
0b10	PCSB[2]
0b11	PCSA[1]

6.3.1.64 Pad Configuration Register 98 (SIU_PCR98)

The SIU_PCR98 register controls the function, direction, and electrical attributes of PCSA[2]_SCKD_GPIO[98]. This register allows selection of the PCSA[2], SCKD, and GPIO functions.

Address: Base + 0x0104 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1]		OBE[2]	IBE[3]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 The PCSA[2] function is available on the MPC5566 only.

2 When configured asPCSA[2] or SCKD, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

3 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-65. PCSA[2]_SCKD_GPIO[98] Pad Configuration Register (SIU_PCR98)

Refer to Table 6-19 for bit field definitions. Table 6-64 lists the PA fields for PCSA[2]_SCKD_GPIO[98].

Table 6-64. PCR98 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[98]
0b01	PCSA[2]
0b10	SCKD
0b11	PCSA[2]

6.3.1.65 Pad Configuration Register 99 (SIU_PCR99)

The SIU_PCR99 register controls the function, direction, and electrical attributes of PCSA[3]_SIND_GPIO[99]. This register allows selection of the PCSA[3], SIND and GPIO functions.

Address: Base + 0x0106 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as PCSA[3] or SIND, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-66. PCSA[3]_SIND_GPIO[99] Pad Configuration Register (SIU_PCR99)

Refer to Table 6-19 for bit field definitions. Table 6-65 lists the PA fields for PCSA[3]_SIND_GPIO[99].

Table 6-65. PCR99 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[99]
0b01	PCSA[3]
0b10	SIND
0b11	PCSA[3]

6.3.1.66 Pad Configuration Register 100 (SIU_PCR100)

The SIU_PCR100 register controls the function, direction, and electrical attributes of PCSA[4]_SOUTD_GPIO[100]. This register allows selection of the PCSA[4], SOUTD, and GPIO functions.

Address: Base + 0x0108 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1]		OBE[2]	IBE[3]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 The PCSA[4] function is available on the MPC5566 only.

2 When configured as PCSA[4] or SOUTD, the OBE bit has no effect. When configured as GPDO, set the OBE to 1.

3 When PCSA[4] or SOUTD is configured for slave operation, set the IBE bit to 1. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-67. PCSA[4]_SOUTD_GPIO[100] Pad Configuration Register (SIU_PCR100)

Refer to Table 6-19 for bit field definitions. Table 6-66 lists the PA fields for PCSA[4]_SOUTD_GPIO[100].

Table 6-66. PCR100 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[100]
0b01	PCSA[4]
0b10	SOUTD
0b11	PCSA[4]

6.3.1.67 Pad Configuration Registers 101 (SIU_PCR101)

The SIU_PCR101 register controls the function, direction, and electrical attributes of PCSA[5]_PCSB[3]_GPIO[101]. This register allows selection of the PCSA[5], PCSB[3] and GPIO functions.

Address: Base + 0x010A Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1]		OBE[2]	IBE[3]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 The PCSA[5] function is available on the MPC5566 only.

2 When configured as PCSA[5] or PCSB[3], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

3 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-68. PCSA[5]_PCSB[3]_GPIO[101] Pad Configuration Register (SIU_PCR101)

Refer to Table 6-19 for bit field definitions. Table 6-67 lists the PA fields for PCSA[5]_PCSB[3]_GPIO[101].

Table 6-67. PCR101 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[101]
0b01	PCSA[5]
0b10	PCSB[3]
0b11	PCSA[5]

6.3.1.68 Pad Configuration Register 102 (SIU_PCR102)

The SIU_PCR102 register controls the function, direction, and electrical attributes of SCKB_PCSC[1]_GPIO[102].

Address: Base + 0x010C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as SCKB or PCSC[1], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-69. SCKB_PCSC[1]_GPIO[102] Pad Configuration Register (SIU_PCR102)

Refer to Table 6-19 for bit field definitions. Table 6-68 lists the PA fields for SCKB_PCSC[1]_GPIO[102].

Table 6-68. PCR102 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[102]
0b01	SCKB
0b10	PCSC[1]
0b11	SCKB

6.3.1.69 Pad Configuration Register 103 (SIU_PCR103)

The SIU_PCR103 register controls the function, direction, and electrical attributes of SINB_PCSC[2]_GPIO[103].

Address: Base + 0x010E Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as SINB, clear the OBE bit to 0. When configured as PCSC[2], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-70. SINB_PCSC[2]_GPIO[103] Pad Configuration Register (SIU_PCR103)

Refer to Table 6-19 for bit field definitions. Table 6-69 lists the PA fields for SINB_PCSC[2]_GPIO[103].

Table 6-69. PCR103 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[103]
0b01	SINB
0b10	PCSC[2]
0b11	SINB

6.3.1.70 Pad Configuration Register 104 (SIU_PCR104)

The SIU_PCR104 register controls the function, direction, and electrical attributes of SOUTB_PCSC[5]_GPIO[104].

Address: Base + 0x0110 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as SOUTB or PCSC[5], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-71. SOUTB_PCSC[5]_GPIO[104] Pad Configuration Register (SIU_PCR104)

Refer to Table 6-19 for bit field definitions. Table 6-44 lists the PA fields for SOUTB_PCSC[5]_GPIO[104].

Table 6-70. PCR104 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[104]
0b01	SOUTB
0b10	PCSC[5]
0b11	SOUTB

6.3.1.71 Pad Configuration Register 105 (SIU_PCR105)

The SIU_PCR105 register controls the function, direction, and electrical attributes of PCSB[0]_PCSD[2]_GPIO[105].

Address: Base + 0x0112 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as PCSB[0], set the OBE bit to 1 for master operation, or clear to 0 for slave operation. When configured as PCSD[2], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When configured as PCSB[0] in slave operation, set the IBE bit to 1. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-72. PCSB[0]_PCSD[2]_GPIO[105] Pad Configuration Register (SIU_PCR105)

Refer to Table 6-19 for bit field definitions. Table 6-71 lists the PA fields for PCSB[0]_PCSD[2]_GPIO[105].

Table 6-71. PCR105 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[105]
0b01	PCSB[0]
0b10	PCSD[2]
0b11	PCSB[0]

6.3.1.72 Pad Configuration Register 106 (SIU_PCR106)

The SIU_PCR106 register controls the function, direction, and electrical attributes of PCSB[1]_PCSD[0]_GPIO[106].

Address: Base + 0x0114 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as PCSD[0], set the OBE bit to 1 for master operation, or clear to 0 for slave operation. When configured as PCSB[1], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When configured as PCSD[0] in slave operation, set the IBE bit to 1. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-73. PCSB[1]_PCSD[0]_GPIO[106] Pad Configuration Register (SIU_PCR106)

Refer to Table 6-19 for bit field definitions. Table 6-72 lists the PA fields for PCSB[1]_PCSD[0]_GPIO[106].

Table 6-72. PCR106 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[106]
0b01	PCSB[1]
0b10	PCSD[0]
0b11	PCSB[1]

6.3.1.73 Pad Configuration Register 107 (SIU_PCR107)

The SIU_PCR107 register controls the function, direction, and electrical attributes of PCSB[2]_SOUTC_GPIO[107].

Address: Base + 0x0116 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as PCSB[2] or SOUTC, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-74. PCSB[2]_SOUTC_GPIO[107] Pad Configuration Register (SIU_PCR107)

Refer to Table 6-19 for bit field definitions. Table 6-73 lists the PA fields for PCSB[2]_SOUTC_GPIO[107].

Table 6-73. PCR107 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[107]
0b01	PCSB[2]
0b10	SOUTC
0b11	PCSB[2]

6.3.1.74 Pad Configuration Register 108 (SIU_PCR108)

The SIU_PCR108 register controls the function, direction, and electrical attributes of PCSB[3]_SINC_GPIO[108].

Address: Base + 0x0118 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as PCSB[3] or SINC, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-75. PCSB[3]_SINC_GPIO[108] Pad Configuration Register (SIU_PCR108)

Refer to Table 6-19 for bit field definitions. Table 6-74 lists the PA fields for PCSB[3]_SINC_GPIO[108].

Table 6-74. PCR108 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[108]
0b01	PCSB[3]
0b10	SINC
0b11	PCSB[3]

6.3.1.75 Pad Configuration Register 109 (SIU_PCR109)

The SIU_PCR109 register controls the function, direction, and electrical attributes of PCSB[4]_SCKC_GPIO[109].

Address: Base + 0x011A — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as PCSB[4] or SCKC, the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-76. PCSB[4]_SCKC_GPIO[109] Pad Configuration Register (SIU_PCR109)

Refer to Table 6-19 for bit field definitions. Table 6-75 lists the PA fields for PCSB[4]_SCKC_GPIO[109].

Table 6-75. PCR109 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[109]
0b01	PCSB[4]
0b10	SCKC
0b11	PCSB[4]

6.3.1.76 Pad Configuration Register 110 (SIU_PCR110)

The SIU_PCR110 register controls the function, direction, and electrical attributes of PCSB[5]_PCSC[0]_GPIO[110].

Address: Base + 0x011C — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as PCSB[5], the OBE bit has no effect. When configured as PCSC[0], set the OBE bit to 1 for master operation, or clear to 0 for slave operation. When configured as GPDO, set the OBE bit to 1.

2 When configured as PCSC[0] in slave operation, set the IBE bit to 1. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-77. PCSB[5]_PCSC[0]_GPIO[110] Pad Configuration Register (SIU_PCR110)

Refer to Table 6-19 for bit field definitions. Table 6-76 lists the PA fields for PCSB[5]_PCSC[0]_GPIO[110].

Table 6-76. PCR110 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[110]
0b01	PCSB[5]
0b10	PCSC[0]
0b11	PCSB[5]

6.3.1.77 Pad Configuration Registers 111–112 (SIU_PCR111–SIU_PCR112)

The SIU_PCR111–SIU_PCR112 registers control the function, direction, and electrical attributes of ETRIG[0:1]_GPIO[111:112].

Address: Base + (0x011E–0x0120) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When ETRIG[0:1] is configured, the OBE has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-78. ETRIG[0:1]_GPIO[111:112] Pad Configuration Register (SIU_PCR111–SIU_PCR112)

Refer to Table 6-19 for bit field definitions. Table 6-77 lists the PA fields for ETRIG[0:1]_GPIO[111:112].

Table 6-77. PCR111–PCR112 PA Field Definitions

PA Field	Pin Function
0b0	GPIO[111:112]
0b1	ETRIG[0:1]

6.3.1.78 Pad Configuration Register 113 (SIU_PCR113)

The SIU_PCR113 register controls the function, direction, and electrical attributes of TCRCLKA_$\overline{\text{IRQ}}$[7]_GPIO[113].

Address: Base + 0x0122 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as TCRCLKA or $\overline{\text{IRQ}}$[7], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-79. TCRCLKA_$\overline{\text{IRQ}}$[7]_GPIO[113] Pad Configuration Register (SIU_PCR113)

Refer to Table 6-19 for bit field definitions. Table 6-78 lists the PA fields for TCRCLKA_IRQ[7]_GPIO[113].

Table 6-78. PCR113 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[113]
0b01	TCRCLKA
0b10	IRQ[7]
0b11	TCRCLKA

6.3.1.79 Pad Configuration Register 114–117 (SIU_PCR114–SIU_PCR117)

The SIU_PCR114–SIU_PCR117 registers control the function, direction, and electrical attributes of ETPUA[0:3]_ETPUA[12:15]_GPIO[114:117]. Only the output channels of ETPUA[12:15] are connected. Both the input and output channels of ETPUA[0:3] are connected.

Address: Base + (0x0124–0x012A) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for ETPUA[0:3], and GPIO[114:117] when configured as outputs. When configured as ETPUA[12:15], the OBE bit has no effect.

2 The IBE bit must be set to 1 for ETPUA[0:3] or GPIO[114:117] when configured as inputs. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register.

3 The weak pullup/down selection at reset for the ETPUA[0:3] pin is determined by the WKPCFG pin.

Figure 6-80. ETPUA[0:3]_ETPUA[12:15]_GPIO[114:117] Pad Configuration Register (SIU_PCR114–SIU_PCR117)

Refer to Table 6-19 for bit field definitions. Table 6-79 lists the PA fields for ETPUA[0:3]_ETPUA[12:15]_GPIO[114:117].

Table 6-79. PCR114–PCR117 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[114:117]
0b01	ETPUA[0:3]
0b10	ETPUA[12:15]
0b11	ETPUA[0:3]

6.3.1.80 Pad Configuration Register 118 (SIU_PCR118)

The SIU_PCR118 registers control the function, direction, and electrical attributes of ETPUA[4]_ETPUA[16]_GPIO[118]. Only the output channel of ETPUA[16] is connected. Both the input and output channels of ETPUA[4] are connected.

Address: Base + 0x012C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for ETPUA[4], ETPUA[16] and GPIO[118] when configured as outputs. When configured as ETPUA[16] the OBE bit has no effect.

2 The IBE bit must be set to 1 for ETPUA[4], ETPUA[16] and GPIO[118] when configured as inputs. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register.

3 The weak pullup/down selection at reset for the ETPUA[16] and ETPUA[4], signals is determined by the WKPCFG pin.

Figure 6-81. ETPUA[4]_ETPUA[16]_GPIO[118] Pad Configuration Register (SIU_PCR118)

Refer to Table 6-19 for bit field definitions. Table 6-80 lists the PA fields for ETPUA[4]_ETPUA[16]_GPIO[118].

Table 6-80. PCR118 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[118]
0b01	ETPUA[4]
0b10	ETPUA[16]
0b11	ETPUA[4]

6.3.1.81 Pad Configuration Register 119 (SIU_PCR119)

The SIU_PCR119 registers control the function, direction, and electrical attributes of ETPUA[5]_ETPUA[17]_GPIO[119]. Only the output channels of ETPUA[17] are connected. Both the input and output channels of ETPUA[5] are connected.

Address: Base + 0x012E Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 When ETPUA[5], or GPIO[119] are configured as outputs, set the OBE bit to 1. When configured as ETPUA[17], the OBE bit has no effect.

2 The IBE bit must be set to one for ETPUA[5], ETPUA[17], and GPIO[119] when configured as inputs. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register.

3 The weak pullup/down value at reset for $\overline{\text{ETPUA[5]}}$ and ETPUA[17], is determined by WKPCFG.

Figure 6-82. ETPUA[5]_ETPUA[17]_GPIO[119] Pad Configuration Register (SIU_PCR119)

Refer to Table 6-19 for bit field definitions. Table 6-81 lists the PA fields for ETPUA[5]_ETPUA[17]_GPIO[119].

Table 6-81. PCR119 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[119]
0b01	ETPUA[5]
0b10	ETPUA[17]
0b11	ETPUA[5]

6.3.1.82 Pad Configuration Register 120 (SIU_PCR120)

The SIU_PCR120 register controls the function, direction, and electrical attributes of ETPUA[6]_ETPUA[18]_GPIO[120]. Only the output channels of ETPUA[18] are connected. Both the input and output channels of ETPUA[6] are connected.

Address: Base + 0x0130 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to one for ETPUA[6] and GPIO[120] when configured as outputs. When configured as ETPUA[18], the OBE bit has no effect.

2 The IBE bit must be set to 1 for ETPUA[6], ETPUA[18], and GPIO[120] when configured as inputs. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register.

3 The weak pullup/down selection at reset for theETPUA[6], ETPUA[18], signals is determined by WKPCFG.

Figure 6-83. ETPUA[6]_ETPUA[18]_GPIO[120] Pad Configuration Register (SIU_PCR120)

Refer to Table 6-19 for bit field definitions. Table 6-82 lists the PA fields for ETPUA[6]_ETPUA[18]_GPIO[120].

Table 6-82. PCR120 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[120]
0b01	ETPUA[6]
0b10	ETPUA[18]
0b11	ETPUA[6]

6.3.1.83 Pad Configuration Register 121 (SIU_PCR121)

The SIU_PCR121 register controls the function, direction, and electrical attributes of ETPUA[7]_ETPUA[19]_GPIO[121]. Only the output channel of ETPUA[19] is connected. Both the input and output channels of ETPUA[7] are connected.

Address: Base + 0x0132 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for ETPUA[7] and GPIO[121] when configured as outputs. When configured as ETPUA[19], the OBE bit has no effect.

2 The IBE bit must be set to 1 for ETPUA[7], ETPUA[19], and GPIO[121] when configured as inputs. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register.

3 The weak pullup/down value at reset for ETPUA[7] and ETPUA[19] is determined by WKPCFG.

Figure 6-84. ETPUA[7]_ETPUA[19]_GPIO[121] Pad Configuration Register (SIU_PCR121)

Refer to Table 6-19 for bit field definitions. Table 6-83 lists the PA fields for ETPUA[7]_ETPUA[19]_GPIO[121].

Table 6-83. PCR121 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[121]
0b01	ETPUA[7]
0b10	ETPUA[19]
0b11	ETPUA[7]

6.3.1.84 Pad Configuration Registers 122–124 (SIU_PCR122–SIU_PCR124)

The SIU_PCR122–SIU_PCR124 registers control the function, direction, and electrical attributes of ETPUA[8:10]_ETPUA[20:22]_GPIO[122:124]. ETPUA[20:22] pins operate as output only channels; ETPUA[8:10] pins can operate as input or output channels.

Address: Base + (0x0134–0x0138) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for ETPUA[8:10], or GPIO[122:124] when configured as outputs. When configured as ETPUA[20], the OBE bit has no effect.

2 The IBE bit must be set to 1 for ETPUA[8:10] or GPIO[122:124] when configured as inputs. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register.

3 The weak pullup/down value at reset for ETPUA[8:10] pin is determined by WKPCFG.

Figure 6-85. ETPUA[8:10]_ETPUA[20:22]_GPIO[122:124] Pad Configuration Register (SIU_PCR122–SIU_PCR124)

Refer to Table 6-19 for bit field definitions. Table 6-84 lists the PA fields for ETPUA[8:10]_ETPUA[20:22]_GPIO[122:124].

Table 6-84. PCR122–PCR124 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[122:124]
0b01	ETPUA[8:10]
0b10	ETPUA[20:22]
0b11	ETPUA[8:10]

6.3.1.85 Pad Configuration Register 125 (SIU_PCR125)

The SIU_PCR125 register controls the function, direction, and electrical attributes of ETPUA[11]_ETPUA[23]_GPIO[125]. Only the output channels of ETPUA[23] are connected. Both the input and output channels of ETPUA[11] are connected.

Address: Base + 0x013A Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for ETPUA[11] or GPIO[125] when configured as outputs. When configured as ETPUA[23], the OBE bit has no effect.

2 The IBE bit must be set to 1 for ETPUA[11] or GPIO[125] when configured as inputs. When the pad is configured as an output, setting the IBE bit to 1 allows the pin state to be reflected in the corresponding GPDI register.

3 The weak pullup/down selection at reset for the ETPUA[11] pin is determined by the WKPCFG pin.

Figure 6-86. ETPUA[11]_ETPUA[23]_GPIO[125] Pad Configuration Register (SIU_PCR125)

Refer to Table 6-19 for bit field definitions. Table 6-85 lists the PA fields for ETPUA[11]_ETPUA[23]_GPIO[125].

Table 6-85. PCR125 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[125]
0b01	ETPUA[11]
0b10	ETPUA[23]
0b11	ETPUA[11]

6.3.1.86 Pad Configuration Register 126 (SIU_PCR126)

The SIU_PCR126 register controls the function, direction, and electrical attributes of ETPUA[12]_PCSB[1]_GPIO[126].

Address: Base + 0x013C — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 When configured as PCSB[1], the OBE bit has no effect. The OBE bit must be set to 1 for ETPUA[12] or GPIO[126] when configured as outputs.

2 The IBE bit must be set to 1 for ETPUA[12] or GPIO[126] when configured as inputs. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register.

3 The weak pullup/down selection at reset for the ETPUA[12] and PCSB[1] pin is determined by the WKPCFG pin.

Figure 6-87. ETPUA[12]_PCSB[1]_GPIO[126] Pad Configuration Register (SIU_PCR126)

Refer to Table 6-19 for bit field definitions. Table 6-86 lists the PA fields for ETPUA[12]_PCSB[1]_GPIO[126].

Table 6-86. PCR126 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[126]
0b01	ETPUA[12]
0b10	PCSB[1]
0b11	ETPUA[12]

6.3.1.87 Pad Configuration Registers 127–129 (SIU_PCR127–SIU_PCR129)

The SIU_PCR127–SIU_PCR129 registers control the function, direction, and electrical attributes of ETPUA[13:15]_PCSB[3:5]_GPIO[127:129].

Address: Base + (0x013E–0x0142) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 When configured as PCSB[3:5], the OBE bit has no effect. The OBE bit must be set to 1 for ETPUA[13:15] or GPIO[127:129] when configured as outputs.

2 The IBE bit must be set to 1 for ETPUA[13:15], PSCB[3:5], or GPIO[127:129] when configured as inputs. When configured as output, set the IBE bit to 1 to show the pin state in the GPDI register.

3 The weak pullup/down selection at reset for the ETPUA[13:15], and PCSB[3:5] pins is determined by the WKPCFG pin.

Figure 6-88. ETPUA[13:15]_PCSB[3:5]_GPIO[127:129]
Pad Configuration Register (SIU_PCR127–SIU_PCR129)

Refer to Table 6-19 for bit field definitions. Table 6-87 lists the PA fields for ETPUA[13:15]_PCSB[3:5]_GPIO[127:129].

Table 6-87. PCR127–PCR129 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[127:129]
0b01	ETPUA[13:15]
0b10	PCSB[3:5]
0b11	ETPUA[13:15]

6.3.1.88 Pad Configuration Register 130–133 (SIU_PCR130–SIU_PCR133)

The SIU_PCR130–SIU_PCR133 registers control the function, direction, and electrical attributes of ETPUA[16:19]_PCSD[1:4]_GPIO[130:133].

Address: Base + (0x0144–0x014A) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 When configured as PCSD[1:4], the OBE bit has no effect. Set the OBE bit to 1 for ETPUA[16:19] or GPIO[130:133] when configured as outputs.

2 The IBE bit must be set to 1 for ETPUA[16:19] or GPIO[130:133] when configured as inputs. When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register.

3 The weak pullup/down selection at reset for the ETPUA[16:19] pin is determined by the WKPCFG pin.

Figure 6-89. ETPUA[16:19]_PCSD[1:4]_GPIO[130:133]
Pad Configuration Register (SIU_PCR130–SIU_PCR133)

Refer to Table 6-19 for bit field definitions. Table 6-88 lists the PA fields for ETPUA[16:19]_PCSD[1:4]_GPIO[130:133].

Table 6-88. PCR130–PCR133 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[130:133]
0b01	ETPUA[16:19]
0b10	PCSD[1:4]
0b11	ETPUA[16:19]

6.3.1.89 Pad Configuration Register 134 (SIU_PCR134)

The SIU_PCR134 register controls the function, direction, and electrical attributes of ETPUA[20]_$\overline{\text{IRQ}}$[8]_GPIO[134]. Both the input and output channels of ETPUA[20] are connected to pins.

Address: Base + 0x014C — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 When configured as $\overline{\text{IRQ}}$[8], the OBE bit has no effect. The OBE bit must be set to 1 for ETPUA[20] or GPIO[134] when configured as output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for ETPUA[20] or GPIO[134] when configured as input.

3 The weak pullup/down selection at reset for the ETPUA[20] pin is determined by the WKPCFG pin.

Figure 6-90. ETPUA[20]_$\overline{\text{IRQ}}$[8]_GPIO[134] Pad Configuration Register (SIU_PCR134)

Refer to Table 6-19 for bit field definitions. Table 6-89 lists the PA fields for ETPUA[20]_$\overline{\text{IRQ}}$[8]_GPIO[134].

Table 6-89. PCR134 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[134]
0b01	ETPUA[20]
0b10	$\overline{\text{IRQ}}$[8]
0b11	ETPUA[20]

6.3.1.90 Pad Configuration Register 135 (SIU_PCR135)

The SIU_PCR135 register controls the function, direction, and electrical attributes of ETPUA[21]_$\overline{\text{IRQ}}$[9]_GPIO[135]. Both the input and output channels of ETPUA[21] are connected.

Address: Base + 0x014E Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 When configured as $\overline{\text{IRQ}}$[9], the OBE bit has no effect. The OBE bit must be set to one for ETPUA[21] or GPIO[135] when configured as outputs.

2 When the pad is configured as an output, setting the IBE bit to 1 allows the pin state to be reflected in the corresponding GPDI register. Setting the IBE bit to zero reduces power consumption. The IBE bit must be set to one for ETPUA[21] or GPIO[135] when configured as inputs.

3 The weak pullup/down selection at reset for the ETPUA[21] pin is determined by the WKPCFG pin.

Figure 6-91. ETPUA[21]_$\overline{\text{IRQ}}$[9]_GPIO[135] Pad Configuration Register (SIU_PCR135)

Refer to Table 6-19 for bit field definitions. Table 6-90 lists the PA fields for ETPUA[21]_$\overline{\text{IRQ}}$[9]_GPIO[135].

Table 6-90. PCR135 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[135]
0b01	ETPUA[21]
0b10	$\overline{\text{IRQ}}$[9]
0b11	ETPUA[21]

6.3.1.91 Pad Configuration Register 136 (SIU_PCR136)

The SIU_PCR136 register controls the function, direction, and electrical attributes of ETPUA[22]_$\overline{\text{IRQ}}$[10]_GPIO[136]. Both the input and output channels of ETPUA[22] are connected.

Address: Base + 0x0150 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 When configured as $\overline{\text{IRQ}}$[10], the OBE bit has no effect. The OBE bit must be set to 1 for ETPUA[22] or GPIO[136] when configured as output.

2 When the pad is configured as an output, setting the IBE bit to 1 allows the pin state to be reflected in the corresponding GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for ETPUA[22] or GPIO[136] when configured as input.

3 The weak pullup/down selection at reset for the ETPUA[22] pin is determined by the WKPCFG pin.

Figure 6-92. ETPUA[22]_$\overline{\text{IRQ}}$[10]_GPIO[136] Pad Configuration Register (SIU_PCR136)

Refer to Table 6-19 for bit field definitions. Table 6-91 lists the PA fields for ETPUA[22]_$\overline{\text{IRQ}}$[10]_GPIO[136].

Table 6-91. PCR136 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[136]
0b01	ETPUA[22]
0b10	$\overline{\text{IRQ}}$[10]
0b11	ETPUA[22]

6.3.1.92 Pad Configuration Register 137 (SIU_PCR137)

The SIU_PCR137 register controls the function, direction, and electrical attributes of ETPUA[23]_$\overline{\text{IRQ}}$[11]_GPIO[137]. Both the input and output channels of ETPUA[23] are connected.

Address: Base + 0x0152 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 When configured as $\overline{\text{IRQ}}$[11], the OBE bit has no effect. The OBE bit must be set to one for ETPUA[23] or GPIO[137] when configured as outputs.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for ETPUA[23] or GPIO[137] when configured as inputs.

3 The weak pullup/down selection at reset for the ETPUA[23] pin is determined by the WKPCFG pin.

Figure 6-93. ETPUA[23]_$\overline{\text{IRQ}}$[11]_GPIO[137] Pad Configuration Register (SIU_PCR137)

Refer to Table 6-19 for bit field definitions. Table 6-92 lists the PA fields for ETPUA[23]_$\overline{\text{IRQ}}$[11]_GPIO[137].

Table 6-92. PCR137 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[137]
0b01	ETPUA[23]
0b10	$\overline{\text{IRQ}}$[11]
0b11	ETPUA[23]

6.3.1.93 Pad Configuration Registers 138–141 (SIU_PCR138–SIU_PCR141)

The SIU_PCR138–SIU_PCR141 registers control the function, direction, and electrical attributes of ETPUA[24:27]_$\overline{\text{IRQ}}$[12:15]_GPIO[138:141]. Only the output channels of ETPUA[24:27] are connected.

Address: Base + (0x0154–0x015A) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 When configured as ETPUA[24:27] or $\overline{\text{IRQ}}$[12:15], the OBE bit has no effect. The OBE bit must be set to 1 for GPIO[138:141] when configured as output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for GPIO[138:141] when configured as input.

3 The weak pullup/down value at reset for ETPUA[24:27] is determined by WKPCFG.

Figure 6-94. ETPUA[24:27]_$\overline{\text{IRQ}}$[12:15]_GPIO[138:141] Pad Configuration Registers (SIU_PCR138–SIU_PCR141)

Refer to Table 6-19 for bit field definitions. Table 6-93 lists the PA fields for ETPUA[24:27]_$\overline{\text{IRQ}}$[12:15]_GPIO[138:141].

Table 6-93. PCR138–PCR141 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[138:141]
0b01	ETPUA[24:27]
0b10	$\overline{\text{IRQ}}$[12:15]
0b11	ETPUA[24:27]

6.3.1.94 Pad Configuration Registers 142–144 (SIU_PCR142–SIU_PCR144)

The SIU_PCR142–SIU_PCR144 registers control the function, direction, and electrical attributes of ETPUA[28:30]_PCSC[1:3]_GPIO[142:144]. Only the output channels of ETPUA[28:30] are connected.

Address: Base + (0x015C–0x0160) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 When configured as ETPUA[28:30] or PCSC[1:3], the OBE bit has no effect. When GPIO[142:144] is configured as output, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI[142:144] registers. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for GPIO when configured as input.

3 The weak pullup/down value at reset for ETPUA[28:30] is determined by WKPCFG.

Figure 6-95. ETPUA[28:30]_PCSC[1:3]_GPIO[142:144] Pad Configuration Register (SIU_PCR142–SIU_PCR144)

Refer to Table 6-19 for bit field definitions. Table 6-94 lists the PA fields for ETPUA[28:30]_PCSC[1:3]_GPIO[142:144].

Table 6-94. PCR142–PCR144 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[142:144]
0b01	ETPUA[28:30]
0b10	$\overline{\text{PCSC}}$[1:3]
0b11	ETPUA[28:30]

6.3.1.95 Pad Configuration Register 145 (SIU_PCR145)

The SIU_PCR145 register controls the function, direction, and electrical attributes of ETPUA[31]_PCSC[4]_GPIO[145].

Address: Base + 0x0162 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 When configured as PCSC[4], the OBE bit has no effect. When configured as ETPUA[31] output or GPDO, set the OBE bit 1.

2 When the pad is configured as an output, set the IBE bit to 1 show the pin state in the corresponding GPDI register. Clear the IBE bit to 0 reduces power consumption. Set the IBE bit to 1 for ETPUA or GPIO when configured as input.

3 The weak pullup/down selection at reset for the ETPUA[31] and PCSC[4] pin is determined by the WKPCFG pin.

Figure 6-96. ETPUA[31]_PCSC[4]_GPIO[145] Pad Configuration Register (SIU_PCR145)

Refer to Table 6-19 for bit field definitions. Table 6-95 lists the PA fields for ETPUA[31]_PCSC[4]_GPIO[145].

Table 6-95. PCR145 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[145]
0b01	ETPUA[31]
0b10	PCSC[4]
0b11	ETPUA[31]

6.3.1.96 Pad Configuration Register 146 (SIU_PCR146)

The SIU_PCR146 register controls the function, direction, and electrical attributes of TCRCLKB_$\overline{\text{IRQ}}$[6]_GPIO[146].

Address: Base + 0x0164 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as TCRCLKB or $\overline{\text{IRQ}}$[6], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-97. TCRCLKB_$\overline{\text{IRQ}}$[6]_GPIO[146] Pad Configuration Register (SIU_PCR146)

Refer to Table 6-19 for bit field definitions. Table 6-96 lists the PA fields for TCRCLKB_$\overline{\text{IRQ}}$[6]_GPIO[146].

Table 6-96. PCR146 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[146]
0b01	TCRCLKB
0b10	$\overline{\text{IRQ}}$[6]
0b11	TCRCLKB

6.3.1.97 Pad Configuration Registers 147–162 (SIU_PCR147–SIU_PCR162)

The SIU_PCR147–SIU_PCR162 registers control the function, direction, and electrical attributes of ETPUB[0:15]_ETPUB[16:31]_GPIO[147:162]. Both the input and output channels of ETPUB[0:15] are connected. Only the output channels of ETPUB[16:31] are connected.

Address: Base + (0x0166–0x0184) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to one for ETPUB[0:15] or GPIO[147:162] when configured as outputs. When configured as ETPUB[16:31], the OBE bit has no effect.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for ETPUB[0:15] or GPIO[147:162] when configured as inputs.

3 The weak pullup/down selection at reset for the ETPUB[0:15] pins is determined by the WKPCFG pin.

Figure 6-98. ETPUB[0:15]_ETPUB[16:31]_GPIO[147:162] Pad Configuration Registers (SIU_PCR147–SIU_PCR162)

Refer to Table 6-19 for bit field definitions. Table 6-97 lists the PA fields for ETPUB[0:15]_ETPUB[16:31]_GPIO[147:162].

Table 6-97. PCR147–PCR162 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[147:162]
0b01	ETPUB[0:15]
0b10	ETPUB[16:31]
0b11	ETPUB[0:15]

6.3.1.98 Pad Configuration Registers 163 (SIU_PCR163–SIU_PCR166)

The SIU_PCR163–SIU_PCR166 registers control the function, direction, and electrical attributes of ETPUB[16:19]_PCSA[1:4]_GPIO[163:166]. Both the input and output channels of ETPUB[16:19] are connected.

Address: Base + (0x0186–0x018C) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to one for ETPUB[16:19] or GPIO[163:166] when configured as outputs. When configured as PCSA[1:4], the OBE bit has no effect.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to one for ETPUB[16:19] or GPIO[163:166] when configured as inputs.

3 The weak pullup/down selection at reset for the ETPUB[16:19] pin is determined by the WKPCFG pin.

Figure 6-99. ETPUB[16:19]_PCSA[1:4]_GPIO[163:166] Pad Configuration Registers (SIU_PCR163–SIU_PCR166)

Refer to Table 6-19 for bit field definitions. Table 6-98 lists the PA fields for ETPUB[16:19]_PCSA[1:4]_GPIO[163:166].

Table 6-98. PCR163–PCR164 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[163:166]
0b01	ETPUB[16:19]
0b10	PCSA[1:4]
0b11	ETPUB[16:19]

6.3.1.99 Pad Configuration Registers 167–178 (SIU_PCR167–SIU_PCR178)

The SIU_PCR167–SIU_PCR178 registers control the function, direction, and electrical attributes of ETPUB[20:31]_GPIO[167:178]. The inputs *and* outputs of ETPUB[20:31] are connected.

Address: Base + (0x018E–0x01A4) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to one for ETPUB[20:31] or GPIO[167:178] when configured as outputs.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to one for ETPUB[20:31] or GPIO[167:178] when configured as inputs.

3 The weak pullup/down value at reset for ETPUB[20:31] pins is determined by WKPCFG.

Figure 6-100. ETPUB[20:31]_GPIO[167:178]
Pad Configuration Register (SIU_PCR167–SIU_PCR178)

Refer to Table 6-19 for bit field definitions. Table 6-99 lists the PA fields for ETPUB[20:31]_GPIO[167:178].

Table 6-99. PCR167–PCR178 PA Field Definitions

PA Field	Pin Function
0b0	GPIO[167:178]
0b1	ETPUB[20:31]

6.3.1.100 Pad Configuration Register 179–188 (SIU_PCR179–SIU_PCR188)

The SIU_PCR179–SIU_PCR188 registers control the function, direction, and electrical attributes of EMIOS[0:9]_ETPUA[0:9]_GPIO[179:188]. The input and output functions of EMIOS[0:9] are connected. Only the output channels of ETPUA[0:9] are connected.

Address: Base + (0x01A6–0x01B8) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for EMIOS[0:9] or GPIO[179:188] when configured as output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for EMIOS[0:9] or GPIO[179:188] when configured as inputs.

3 The weak pullup/down selection at reset for the EMIOS[0:9] pins is determined by the WKPCFG pin.

Figure 6-101. EMIOS[0:9]_ETPUA[0:9]_GPIO[179:188]
Pad Configuration Register (SIU_PCR179–SIU_PCR188)

Refer to Table 6-19 for bit field definitions. Table 6-100 lists the PA fields for EMIOS[0:9]_ETPUA[0:9]_GPIO[179:188].

Table 6-100. PCR179–PCR188 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[179:188]
0b01	EMIOS[0:9]
0b10	ETPUA[0:9]
0b11	EMIOS[0:9]

6.3.1.101 Pad Configuration Register 189–190 (SIU_PCR189–SIU_PCR190)

The SIU_PCR189–SIU_PCR190 registers control the function, direction, and electrical attributes of EMIOS[10:11]_PCSD[3:4]_GPIO[189:190]. Both the input and output functions of EMIOS[10:11] are connected.

Address: Base + (0x01BA–0x01BC) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for EMIOS[10:11] or GPIO[189:190] when configured as output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for EMIOS[10:11] or GPIO[189:190] when configured as input.

3 The weak pullup/down selection at reset for the EMIOS[10:11] pins is determined by the WKPCFG pin.

Figure 6-102. EMIOS[10:11]_PCSD[3:4]_GPIO[189:190] Pad Configuration Register (SIU_PCR189–SIU_PCR190)

Refer to Table 6-19 for bit field definitions. Table 6-101 lists the PA fields for EMIOS[10:11]_PCSD[3:4]_GPIO[189:190].

Table 6-101. PCR189–PCR190 PA Field Definitions

Pin Function
GPIO[189:190]
EMIOS[10:11]
PCSD[3:4]
EMIOS[10:11]

6.3.1.102 Pad Configuration Register 191 (SIU_PCR191)

The SIU_PCR191 register controls the function, direction, and electrical attributes of EMIOS[12]_SOUTC_GPIO[191]. Only the output of EMIOS[12] is connected.

Address: Base + 0x01BE Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for GPIO[191] when configured as an output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for GPIO[191] when configured as an input.

3 The weak pullup/down selection at reset for the EMIOS[12] pin is determined by the WKPCFG pin.

Figure 6-103. EMIOS[12]_SOUTC_GPIO[191] Pad Configuration Register (SIU_PCR191)

Refer to Table 6-19 for bit field definitions. Table 6-102 lists the PA fields for EMIOS[12]_SOUTC_GPIO[191].

Table 6-102. PCR191 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[191]
0b01	EMIOS[12]
0b10	SOUTC
0b11	EMIOS[12]

6.3.1.103 Pad Configuration Register 192 (SIU_PCR192)

The SIU_PCR192 register controls the function, direction, and electrical attributes of EMIOS[13]_SOUTD_GPIO[192]. Only the output of EMIOS[13] is connected.

Address: Base + 0x01C0 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for GPIO[192] when configured as an output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for GPIO[192] when configured as an input.

3 The weak pullup/down selection at reset for the EMIOS[13] pin is determined by the WKPCFG pin.

Figure 6-104. EMIOS[13]_SOUTD_GPIO[192] Pad Configuration Register (SIU_PCR192)

Refer to Table 6-19 for bit field definitions. Table 6-103 lists the PA fields for EMIOS[13]_SOUTD_GPIO[192].

Table 6-103. PCR192 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[192]
0b01	EMIOS[13]
0b10	SOUTD
0b11	EMIOS[13]

6.3.1.104 Pad Configuration Register 193 (SIU_PCR193)

The SIU_PCR193 register controls the function, direction, and electrical attributes of EMIOS[14]_$\overline{\text{IRQ}}$[0]_CNTXD_GPIO[193]. The input and output functions for EMIOS[14] are both connected.

Address: Base + 0x01C2 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	PA			OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for GPIO[193] when configured as output.

2 When the pad is configured as output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When CNTXD or GPIO[193] is configured as input, set the IBE bit 1.

3 The weak pullup/down selection at reset for the EMIOS[14] pin is determined by the WKPCFG pin.

Figure 6-105. EMIOS[14]_$\overline{\text{IRQ}}$[0]_CNTXD_GPIO[193] Pad Configuration Register (SIU_PCR193)

Refer to Table 6-19 for bit field definitions. Table 6-104 lists the PA fields for EMIOS[14]_$\overline{\text{IRQ}}$[0]_CNTXD_GPIO[193].

Table 6-104. PCR193 PA Field Definitions

PA Field	Pin Function
0b000	GPIO[193]
0b001	EMIOS[14]
0b010	$\overline{\text{IRQ}}$[0]
0b011	EMIOS[14]
0b100	CNTXD

6.3.1.105 Pad Configuration Register 194 (SIU_PCR194)

The SIU_PCR194 register controls the function, direction, and electrical attributes of EMIOS[15]_$\overline{IRQ}$[1]_CNRXD_GPIO[194]. Both input and output functions of EMIOS[15] are connected.

Address: Base + 0x01C4 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	PA			OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for GPIO[194] when configured as output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for CNRXD or GPIO[194] when configured as input.

3 The weak pullup/down selection at reset for the EMIOS[15] pin is determined by the WKPCFG pin.

Figure 6-106. EMIOS[15]_$\overline{IRQ}$[1]_CNRXD_GPIO[194] Pad Configuration Register (SIU_PCR194)

Refer to Table 6-19 for bit field definitions. Table 6-105 lists the PA fields for EMIOS[15]_$\overline{IRQ}$[1]_CNRXD_GPIO[194].

Table 6-105. PCR194 PA Field Definitions

PA Field	Pin Function
0b000	GPIO[194]
0b001	EMIOS[15]
0b010	$\overline{IRQ}$[1]
0b011	EMIOS[15]
0b100	CNRXD

6.3.1.106 Pad Configuration Register 195 (SIU_PCR195)

The SIU_PCR195 register controls the function, direction, and electrical attributes of EMIOS[16]_ETPUB[0]_GPIO[195]. Both the input and output functions of EMIOS[16] are connected. Only the output channel of ETPUB[0] is connected.

Address: Base + 0x01C6 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for EMIOS[16] or GPIO[195] when configured as output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for EMIOS[16] or GPIO[195] when configured as input.

3 The weak pullup/down selection at reset for the EMIOS[16] pin is determined by the WKPCFG pin.

Figure 6-107. EMIOS[16]_ETPUB[0]_GPIO[195] Pad Configuration Register (SIU_PCR195)

Refer to Table 6-19 for bit field definitions. Table 6-106 lists the PA fields for EMIOS[16]_ETPUB[0]_GPIO[195].

Table 6-106. PCR195 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[195]
0b01	EMIOS[16]
0b10	ETPUB[0]
0b11	EMIOS[16]

6.3.1.107 Pad Configuration Register 196 (SIU_PCR196)

The SIU_PCR196 register controls the function, direction, and electrical attributes of EMIOS[17]_ETPUB[1]_GPIO[196]. Both the input and output functions of EMIOS[17] are connected. Only the output channels of ETPUB[1] is connected.

Address: Base + 0x01C8 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to one for EMIOS[17] and GPIO[196] when configured as outputs.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for EMIOS[17] or GPIO[196] when configured as input.

3 The weak pullup/down selection at reset for the EMIOS[17] pin is determined by the WKPCFG pin.

Figure 6-108. EMIOS[17]_ETPUB[1]_GPIO[196] Pad Configuration Register (SIU_PCR196)

Refer to Table 6-19 for bit field definitions. Table 6-107 lists the PA fields for EMIOS[17]_ETPUB[1]_GPIO[196].

Table 6-107. PCR196 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[196]
0b01	EMIOS[17]
0b10	ETPUB[1]
0b11	EMIOS[17]

6.3.1.108 Pad Configuration Register 197 (SIU_PCR197)

The SIU_PCR197 register controls the function, direction, and electrical attributes of EMIOS[18]_ETPUB[2]_GPIO[197]. Both the input and output functions of EMIOS[18] is connected. Only the output channels of ETPUB[2] is connected.

Address: Base + 0x01CA Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for EMIOS[18] or GPIO[197] when configured as output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for EMIOS[18] or GPIO[197] when configured as input.

3 The weak pullup/down selection at reset for the EMIOS[18] pin is determined by the WKPCFG pin.

Figure 6-109. EMIOS[18]_ETPUB[2]_GPIO[197] Pad Configuration Register (SIU_PCR197)

Refer to Table 6-19 for bit field definitions. Table 6-108 lists the PA fields for EMIOS[18]_ETPUB[2]_GPIO[197].

Table 6-108. PCR197 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[197]
0b01	EMIOS[18]
0b10	ETPUB[2]
0b11	EMIOS[18]

6.3.1.109 Pad Configuration Register 198 (SIU_PCR198)

The SIU_PCR198 register controls the function, direction, and electrical attributes of the EMIOS[19]_ETPUB[3]_GPIO[198] pin. Both the input and output functions of EMIOS[19] are connected. Only the output channels of ETPUB[3] are connected.

Address: Base + 0x01CC Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for EMIOS[19] and GPIO[198] when configured as output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for EMIOS[19] or GPIO[198] when configured as input.

3 The weak pullup/down selection at reset for the EMIOS[19] pins is determined by the WKPCFG pin.

Figure 6-110. EMIOS[19]_ETPUB[3]_GPIO[198] Pad Configuration Register (SIU_PCR198)

Refer to Table 6-19 for bit field definitions. Table 6-109 lists the PA fields for EMIOS[19]_ETPUB[3]_GPIO[198].

Table 6-109. PCR198 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[198]
0b01	EMIOS[19]
0b10	ETPUB[3]
0b11	EMIOS[19]

6.3.1.110 Pad Configuration Registers 199–200 (SIU_PCR199–SIU_PCR200)

The SIU_PCR199–SIU_PCR200 registers control the function, direction, and electrical attributes of EMIOS[20:21]_ETPUB[4:5]_GPIO[199:200]. Both the input and output functions of EMIOS[20:21] are connected. Only the output channels of ETPUB[4:5] are connected.

Address: Base + (0x01CE–0x01D0) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for EMIOS[20:21] or GPIO[199:200] when configured as output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for EMIOS[20:21] or GPIO[199:200] when configured as input.

3 The weak pullup/down selection at reset for the EMIOS[20:21] pin is determined by the WKPCFG pin.

Figure 6-111. EMIOS[20:21]_ETPUB[4:5]_GPIO[199:200] Pad Configuration Register (SIU_PCR199–SIU_PCR200)

Refer to Table 6-19 for bit field definitions. Table 6-110 lists the PA fields for EMIOS[20:21]_ETPUB[4:5]_GPIO[199:200].

Table 6-110. PCR199–PCR200 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[199:200]
0b01	EMIOS[20:21]
0b10	ETPUB[4:5]
0b11	EMIOS[20:21]

6.3.1.111 Pad Configuration Register 201 (SIU_PCR201)

The SIU_PCR201 register controls the function, direction, and electrical attributes of EMIOS[22]_ETPUB[6]_GPIO[201]. Both the input and output functions of EMIOS[22] are connected. Only the output channel of ETPUB[6] is connected.

Address: Base + 0x01D2 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for EMIOS[22] or GPIO[201] when configured as output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for EMIOS[22] or GPIO[201] when configured as input.

3 The weak pullup/down selection at reset for the EMIOS[22] pin is determined by the WKPCFG pin.

Figure 6-112. EMIOS[22]_ETPUB[6]_GPIO[201] Pad Configuration Register (SIU_PCR201)

Refer to Table 6-19 for bit field definitions. Table 6-111 lists the PA fields for EMIOS[22]_ETPUB[6]_GPIO[201].

Table 6-111. PCR201 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[201]
0b01	EMIOS[22]
0b10	ETPUB[6]
0b11	EMIOS[22]

6.3.1.112 Pad Configuration Register 202 (SIU_PCR202)

The SIU_PCR202 register controls the function, direction, and electrical attributes of EMIOS[23]_ETPUB[7]_GPIO[202]. Both the input and output functions of EMIOS[23] are connected. Only the output channel of ETPUB[7] is connected.

Address: Base + 0x01D4 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	U[3]

1 The OBE bit must be set to 1 for EMIOS[23] or GPIO[202] when configured as output.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. The IBE bit must be set to 1 for EMIOS[23] or GPIO[202] when configured as input.

3 The weak pullup/down selection at reset for the EMIOS[23] pin is determined by the WKPCFG pin.

Figure 6-113. EMIOS[23]_ETPUB[7]_GPIO[202] Pad Configuration Register (SIU_PCR202)

Refer to Table 6-19 for bit field definitions. Table 6-112 lists the PA fields for EMIOS[23]_ETPUB[7]_GPIO[202].

Table 6-112. PCR202 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[202]
0b01	EMIOS[23]
0b10	ETPUB[7]
0b11	EMIOS[23]

6.3.1.113 Pad Configuration Registers 203–204 (SIU_PCR203–SIU_PCR204)

The SIU_PCR203–SIU_PCR204 registers control the function, direction, and electrical attributes of EMIOS[14:15]_GPIO[203:204]. Only the output functions of EMIOS[14:15] are connected. These signals are referred to as GPIO[203:204] because other balls are named EMIOS[14:15]. The primary function is EMIOS, however the default out of reset is GPIO. These signals are not affected by WKPCFG.

Address: Base + (0x01D6–0x01D8) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as EMIOS[14:15] the OBE bit has no effect. When GPIO[203:204] is configured as output, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

Figure 6-114. EMIOS[14:15]_GPIO[203:204] Pad Configuration Registers (SIU_PCR203–SIU_PCR204)

Refer to Table 6-19 for bit field definitions. Table 6-113 lists the PA fields for EMIOS[14:15]_GPIO[203:204].

Table 6-113. PCR203–PCR204 PA Field Definitions

PA Field	Pin Function
0b0	GPIO[203:204]
0b1	EMIOS[14:15]

6.3.1.114 Pad Configuration Register 205 (SIU_PCR205)

The SIU_PCR205 register controls the direction and electrical attributes of the GPIO[205] pin. This register is separate from the PCRs for GPIO[206:207] since GPIO[205] is a medium pad type with slew

rate control and GPIO[206:207] are fast pad types with drive strength control. The PA bit is not implemented for this PCR because GPIO is the only pin function.

Address: Base + 0x01DA — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	OBE[1]	IBE[2]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. When configured as GPDI, set the IBE bit to 1.

Figure 6-115. GPIO[205] Pad Configuration Registers (SIU_PCR205)

6.3.1.115 Pad Configuration Registers 206–207 (SIU_PCR206–SIU_PCR207)

The SIU_PCR206–SIU_PCR207 registers control the function, direction, and electrical attributes of GPIO[206:207]. These registers are separate from the PCR for GPIO[205] since GPIO[206:207] are fast pad types with drive strength control and GPIO[205] is a medium pad type with slew rate control. The PA bit is not implemented for these PCRs since GPIO is the only function.

NOTE

The GPIO[206:207] can trigger the ADCs. For ETRIG functionality, set these pins to GPIO, and then select the GPIO ADC trigger in the SIU_ETISR register. The input source for each SIN, $\overline{SS}$, SCK, and trigger signal is individually specified in the DSPI input select register (SIU_DISR).

Refer to Section 6.3.1.161, “eQADC Trigger Input Select Register (SIU_ETISR).”

Address: Base + (0x01DC–0x01DE) — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	OBE[1]	IBE[2]	DSC		ODE	HYS	0	0	WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

1 When configured as GPDO, set the OBE bit to 1.

2 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. When configured as GPDI, set the IBE bit to 1.

Figure 6-116. GPIO[206:207] Pad Configuration Registers (SIU_PCR206–SIU_PCR207)

6.3.1.116 Pad Configuration Register 208 (SIU_PCR208)

The SIU_PCR208 register controls the function, direction, and electrical attributes of PLLCFG[0]_$\overline{\text{IRQ}}$[4]_GPIO[208].

Address: Base + 0x01E0 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1]		OBE[2]	IBE[3]	0	0	ODE	HYS[4]	SRC		WPE	WPS
W																
RESET:	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	1

1 The PLLCFG[0] function applies only during reset when the $\overline{\text{RSTCFG}}$ pin is asserted. Set the PA field to 0b10 for $\overline{\text{IRQ}}$[4], or to 0b00 for GPIO[208].

2 When configured as $\overline{\text{IRQ}}$[4], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

3 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

4 When configured as $\overline{\text{IRQ}}$[4], set the HYS bit to 1.

Figure 6-117. PLLCFG[0]_$\overline{\text{IRQ}}$[4]_GPIO[208] Pad Configuration Register (SIU_PCR208)

Refer to Table 6-19 for bit field definitions. Table 6-114 lists the PA fields for PLLCFG[0]_$\overline{\text{IRQ}}$[4]_GPIO[208].

Table 6-114. PCR208 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[208]
0b01	PLLCFG[0]
0b10	$\overline{\text{IRQ}}$[4]
0b11	PLLCFG[0]

6.3.1.117 Pad Configuration Register 209 (SIU_PCR209)

The SIU_PCR209 register controls the function, direction, and electrical attributes of PLLCFG[1]_$\overline{\text{IRQ}}$[5]_SOUTD_GPIO[209].

Address: Base + 0x01E2 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	PA[1]			OBE[2]	IBE[3]	0	0	ODE	HYS[4]	SRC		WPE	WPS
W																
RESET:	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	1

1 The PLLCFG[1] function applies only during reset when the $\overline{\text{RSTCFG}}$ pin is asserted during reset. Set the PA field to 0b010 for $\overline{\text{IRQ}}$[5], 0b100 for SOUTD, and 0b000 for GPIO[209].

2 When configured as $\overline{\text{IRQ}}$[5], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

3 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

4 When configured as $\overline{\text{IRQ}}$[5], set the HYS bit to 1.

Figure 6-118. PLLCFG[1]_$\overline{\text{IRQ}}$[5]_SOUTD_GPIO[209] Pad Configuration Register (SIU_PCR209)

Refer to Table 6-19 for bit field definitions. Table 6-115 lists the PA fields for PLLCFG[1]_$\overline{\text{IRQ}}$[5]_SOUTD_GPIO[209].

Table 6-115. PCR209 PA Field Definitions

PA Field	Pin Function
0b000	GPIO[209]
0b001	PLLCFG[1]
0b010	$\overline{\text{IRQ}}$[5]
0b011	PLLCFG[1]
0b100	SOUTD

6.3.1.118 Pad Configuration Register 210 (SIU_PCR210)

The SIU_PCR210 register controls the function, direction, and electrical attributes of $\overline{\text{RSTCFG}}$_GPIO[210].

Address: Base + 0x01E4 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA[1]	OBE[2]	IBE[3]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1

1 $\overline{\text{RSTCFG}}$ function is only applicable during reset. The PA bit must be set to 0 for GPIO operation.

2 When configured as GPDO, set the OBE bit to 1.

3 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. When configured as GPDI, set the IBE bit to 1.

Figure 6-119. $\overline{\text{RSTCFG}}$_GPIO[210] Pad Configuration Register (SIU_PCR210)

Refer to Table 6-19 for bit field definitions. Table 6-116 lists the PA fields for $\overline{\text{RSTCFG}}$_GPIO[210].

Table 6-116. PCR210 PA Field Definitions

PA Field	Pin Function
0b0	GPIO
0b1	$\overline{\text{RSTCFG}}$

6.3.1.119 Pad Configuration Registers 211–212 (SIU_PCR211–SIU_PCR212)

The SIU_PCR211–SIU_PCR212 registers control the function, direction, and electrical attributes of BOOTCFG[0:1]_$\overline{\text{IRQ}}$[2:3]_GPIO[211:212].

Address: Base + (0x01E6–0x01E8) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1]		OBE[2]	IBE[3]	0	0	ODE	HYS[4]	SRC		WPE	WPS
W																
RESET:	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0

1 The BOOTCFG[0:1] function applies only during reset when the $\overline{\text{RSTCFG}}$ pin is asserted during reset. Set the PA field to 0b10 for $\overline{\text{IRQ}}$[2:3], or to 0b00 for GPIO[211:212].

2 When configured as $\overline{\text{IRQ}}$[2:3], the OBE bit has no effect. When configured as GPDO, set the OBE bit to 1.

3 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the GPDI register. Clear the IBE bit to 0 to reduce power consumption. When configured as GPDI, set the IBE bit to 1.

4 When configured as $\overline{\text{IRQ}}$[2:3], set the HYS bit to 1.

Figure 6-120. BOOTCFG[0:1]_$\overline{\text{IRQ}}$[2:3]_GPIO[211:212] Pad Configuration Register (SIU_PCR211–SIU_PCR212)

Refer to Table 6-19 for bit field definitions. Table 6-117 lists the PA fields for BOOTCFG[0:1]_$\overline{\text{IRQ}}$[2:3]_GPIO[211:212].

Table 6-117. PCR211–PCR212 PA Field Definitions

PA Field	Pin Function
0b00	GPIO[211:212]
0b01	BOOTCFG[0:1]
0b10	$\overline{\text{IRQ}}$[2:3]
0b11	BOOTCFG[0:1]

6.3.1.120 Pad Configuration Register 213 (SIU_PCR213)

The SIU_PCR213 register controls the function, direction, and electrical attributes of WKPCFG_GPIO[213].

Address: Base + 0x01EA Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA[1]	OBE[2]	IBE[3]	0	0	ODE	HYS	SRC		WPE	WPS
W																
RESET:	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1

1 WKPCFG function is only applicable during reset. The PA bit must be cleared to 0 for GPIO operation.

2 When configured as GPDO, set the OBE bit to 1.

3 When the pad is configured as an output, set the IBE bit to 1 to show the pin state in the corresponding GPDI register. When configured as GPDI, set the IBE bit to 1.

Figure 6-121. WKPCFG_GPIO[213] Pad Configuration Register (SIU_PCR213)

Table 6-118. PCR213 PA Field Definitions

PA Field	Pin Function
0b0	GPIO
0b1	WKPCFG

6.3.1.121 Pad Configuration Register 214 (SIU_PCR214)

The SIU_PCR214 register enables or disables ENGCLK and controls the drive strength. ENGCLK is enabled or disabled by setting or clearing the OBE bit. ENGCLK is enabled during reset.

Address: Base + 0x01EC Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	OBE	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0

Figure 6-122. ENGLCK Pad Configuration Register (SIU_PCR214)

6.3.1.122 Pad Configuration Register 215 (SIU_PCR215)

The SIU_PCR215 register controls the function, direction, and electrical attributes of AN[12]_MA[0]_$\overline{\text{SDS}}$.

Address: Base + 0x01EE Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1, 2]		0	0	0	0	ODE	0	SRC		0	0
W																
RESET:	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

1 Enable or disable input and output buffers based on the PA selection. Output buffers are disabled for the AN[12] function. Output buffers can be enabled only for MA[0] or $\overline{\text{SDS}}$ functions.

2 To select the $\overline{\text{SDS}}$ function, set the PA field to 0b00.

Figure 6-123. AN[12]_MA[0]_$\overline{\text{SDS}}$ Pad Configuration Register (SIU_PCR215)

Refer to Table 6-19 for bit field definitions. Table 6-119 lists the PA fields for AN[12]_MA[0]_$\overline{\text{SDS}}$.

Table 6-119. PCR215 PA Field Definitions

PA Field	Pin Function
0b00	$\overline{\text{SDS}}$
0b01	Invalid value
0b10	MA[0]
0b11	AN[12]

6.3.1.123 Pad Configuration Register 216 (SIU_PCR216)

The SIU_PCR216 register controls the function, direction, and electrical attributes of AN[13]_MA[1]_SDO.

Address: Base + 0x01F0 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1, 2]		0	0	0	0	ODE	0	SRC		0	0
W																
RESET:	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

1 Input and output buffers are enabled/disabled based on PA selection. Both input and output buffers are disabled for AN[13] function. Output buffers only can be enabled for MA[1] and SDO functions.

2 To select the SDO function, set the PA field to 0b00.

Figure 6-124. AN[13]_MA[1]_SDO Pad Configuration Register (SIU_PCR216)

Refer to Table 6-19 for bit field definitions. Table 6-120 lists the PA fields for AN[13]_MA[1]_SDO.

Table 6-120. PCR216 PA Field Definitions

PA Field	Pin Function
0b00	SDO
0b01	Invalid value
0b10	MA[1]
0b11	AN[13]

6.3.1.124 Pad Configuration Register 217 (SIU_PCR217)

The SIU_PCR217 register controls the pin function, direction, and electrical attributes of AN[14]_MA[2]_SDI.

Address: Base + 0x01F2 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1, 2]		0	0	0	0	ODE	HYS	SRC		WPE[3]	WPS[4]
W																
RESET:	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

1 Input and output buffers are enabled/disabled based on PA selection. Both input and output buffers are disabled for AN[14] function. Output buffers only can be enabled for MA[2] and SDI functions.

2 To select the SDI function, set the PA field to 0b00.

3 Set the WPE bit to 0 when configured as analog input or MA[2], or set to 1 when configured as SDI.

4 Set the WPS bit to 1 when configured as SDI.

Figure 6-125. AN[14]_MA[2]_SDI Pad Configuration Register (SIU_PCR217)

Refer to Table 6-19 for bit field definitions. Table 6-121 lists the PA fields for AN[14]_MA[2]_SDI.

Table 6-121. PCR217 PA Field Definitions

PA Field	Pin Function
0b00	SDI
0b01	Invalid value
0b10	MA[2]
0b11	AN[14]

6.3.1.125 Pad Configuration Register 218 (SIU_PCR218)

The SIU_PCR218 register controls the function, direction, and electrical attributes of AN[15]_FCK.

Address: Base + 0x01F4 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA[1, 2]		0	0	0	0	ODE	0	SRC		0	0
W																
RESET:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

1 Input and output buffers are enabled/disabled based on PA selection. Both input and output buffers are disabled for the AN[15] function. Output buffers only can be enabled for the FCK function.

2 To select the FCK function, set the PA field to 0b10.

Figure 6-126. AN[15]_FCK Pad Configuration Register (SIU_PCR218)

Refer to Table 6-19 for bit field definitions. Table 6-122 lists the PA fields for AN[15]_FCK.

Table 6-122. PCR218 PA Field Definitions

PA Field	Pin Function
0b00	Invalid value
0b01	Invalid value
0b10	FCK
0b11	AN[15]

6.3.1.126 Pad Configuration Register 219 (SIU_PCR219)

The SIU_PCR219 register controls the drive strength of MCKO.

Address: Base + 0x01F6 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Figure 6-127. MCKO Pad Configuration Register (SIU_PCR219)

6.3.1.127 Pad Configuration Register 223–220 (SIU_PCR223–SIU_PCR220)

The SIU_PCR223–SIU_PCR220 registers control the drive strength of MDO[3:0].

Address: Base + (0x01FE–0x01F8) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Figure 6-128. MDO[3:0] Pad Configuration Register (SIU_PCR223–SIU_PCR220)

6.3.1.128 Pad Configuration Register 225–224 (SIU_PCR225–SIU_PCR224)

The SIU_PCR225–SIU_PCR224 registers control the drive strength of $\overline{\text{MSEO}}$[1:0].

Address: Base + (0x0202–0x0200) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Figure 6-129. $\overline{\text{MSEO}}$[1:0] Pad Configuration Register (SIU_PCR225–SIU_PCR224)

6.3.1.129 Pad Configuration Register 226 (SIU_PCR226)

The SIU_PCR226 register controls the drive strength of $\overline{\text{RDY}}$.

Address: Base + 0x0204 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Figure 6-130. $\overline{\text{RDY}}$ Pad Configuration Register (SIU_PCR226)

6.3.1.130 Pad Configuration Register 227 (SIU_PCR227)

The SIU_PCR227 register controls the drive strength of $\overline{\text{EVTO}}$.

Address: Base + 0x0206 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Figure 6-131. $\overline{\text{EVTO}}$ Pad Configuration Register (SIU_PCR227)

6.3.1.131 Pad Configuration Register 228 (SIU_PCR228)

The SIU_PCR228 register controls the drive strength of TDO.

Address: Base + 0x0208 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Figure 6-132. TDO Pad Configuration Register (SIU_PCR228)

6.3.1.132 Pad Configuration Register 229 (SIU_PCR229)

The SIU_PCR229 register controls the enabling/disabling and drive strength of CLKOUT. CLKOUT is enabled and disabled by setting and clearing the OBE bit. CLKOUT is enabled during reset.

Address: Base + 0x020A — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	OBE	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0

Figure 6-133. CLKOUT Pad Configuration Register (SIU_PCR229)

6.3.1.133 Pad Configuration Register 230 (SIU_PCR230)

The SIU_PCR230 register controls the slew rate of $\overline{\text{RSTOUT}}$.

Address: Base + 0x020C — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	SRC		0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Figure 6-134. $\overline{\text{RSTOUT}}$ Pad Configuration Register (SIU_PCR230)

6.3.1.134 Pad Configuration Register 231–255 (SIU_PCR231–SIU_PCR255)

The SIU_PCR231–SIU_PCR255 registers are not implemented in this device.

6.3.1.135 Pad Configuration Register 256 (SIU_PCR256)

The SIU_PCR256 register controls the function, direction, and electrical attributes of CAL_$\overline{\text{CS}}$[0].

Address: Base + 0x0240 — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-135. CAL_$\overline{\text{CS}}$[0] Pad Configuration Register (SIU_PCR256)

Refer to Table 6-19 for bit field definitions. Table 6-123 lists the PA fields for CAL_$\overline{\text{CS}}$[0].

Table 6-123. PCR256 PA Field Definition

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_$\overline{\text{CS}}$[0]

6.3.1.136 Pad Configuration Registers 257–258 (SIU_PCR257–SIU_PCR258)

The SIU_PCR257–SIU_PCR258 registers control the function, direction, and electrical attributes of CAL_$\overline{CS}$[2:3]_CAL_ADDR[10:11].

Address: Base + (0x0242–0x0244) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-136. CAL_$\overline{CS}$[2:3]_CAL_ADDR[10:11] Pad Configuration Registers (SIU_PCR257–SIU_PCR258)

Refer to Table 6-19 for bit field definitions. Table 6-124 lists the PA fields for CAL_$\overline{CS}$[2:3]_CAL_ADDR[10:11].

Table 6-124. PCR257–PCR258 PA Field Definitions

PA Field	Pin Function
0b00	Invalid value
0b01	CAL_$\overline{CS}$[2:3]
0b10	CAL_ADDR[10:11]
0b11	CAL_$\overline{CS}$[2:3]

6.3.1.137 Pad Configuration Register 259 (SIU_PCR259)

The SIU_PCR259 register controls the function, direction, and electrical attributes of CAL_ADDR[12].

Address: Base + 0x0246 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-137. CAL_ADDR[12] Pad Configuration Register (SIU_PCR259)

Refer to Table 6-19 for bit field definitions. Table 6-125 lists the PA fields for CAL_ADDR[12].

Table 6-125. PCR259 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[12]

6.3.1.138 Pad Configuration Register 260 (SIU_PCR260)

The SIU_PCR260 register controls the function, direction, and electrical attributes of CAL_ADDR[13].

Address: Base + 0x0248 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-138. CAL_ADDR[13] Pad Configuration Register (SIU_PCR260)

Refer to Table 6-19 for bit field definitions. Table 6-126 lists the PA fields for CAL_ADDR[13].

Table 6-126. PCR260 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[13]

6.3.1.139 Pad Configuration Register 261 (SIU_PCR261)

The SIU_PCR261 register controls the function, direction, and electrical attributes of CAL_ADDR[14].

Address: Base + 0x024A — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-139. CAL_ADDR[14] Pad Configuration Register (SIU_PCR261)

Refer to Table 6-19 for bit field definitions. Table 6-127 lists the PA fields for CAL_ADDR[14].

Table 6-127. PCR261 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[14]

6.3.1.140 Pad Configuration Register 262 (SIU_PCR262)

The SIU_PCR262 register controls the function, direction, and electrical attributes of CAL_ADDR[15].

Address: Base + 0x024C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-140. CAL_ADDR[15] Pad Configuration Register (SIU_PCR262)

Refer to Table 6-19 for bit field definitions. Table 6-128 lists the PA fields for CAL_ADDR[15].

Table 6-128. PCR262 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[15]

6.3.1.141 Pad Configuration Register 263 (SIU_PCR263)

The SIU_PCR263 register controls the function, direction, and electrical attributes of CAL_ADDR[16].

Address: Base + 0x024E Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-141. CAL_ADDR[16] Pad Configuration Register (SIU_PCR263)

Refer to Table 6-19 for bit field definitions. Table 6-129 lists the PA fields for CAL_ADDR[16].

Table 6-129. PCR263 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[16]

6.3.1.142 Pad Configuration Register 264 (SIU_PCR264)

The SIU_PCR264 register controls the function, direction, and electrical attributes of CAL_ADDR[17].

Address: Base + 0x0250 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-142. CAL_ADDR[17] Pad Configuration Register (SIU_PCR264)

Refer to Table 6-19 for bit field definitions. Table 6-130 lists the PA fields for CAL_ADDR[17].

Table 6-130. PCR264 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[17]

6.3.1.143 Pad Configuration Register 265 (SIU_PCR265)

The SIU_PCR265 register controls the function, direction, and electrical attributes of CAL_ADDR[18].

Address: Base + 0x0252 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-143. CAL_ADDR[18] Pad Configuration Register (SIU_PCR265)

Refer to Table 6-19 for bit field definitions. Table 6-131 lists the PA fields for CAL_ADDR[18].

Table 6-131. PCR265 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[18]

6.3.1.144 Pad Configuration Register 266 (SIU_PCR266)

The SIU_PCR266 register controls the function, direction, and electrical attributes of CAL_ADDR[19].

Address: Base + 0x0254 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-144. CAL_ADDR[19] Pad Configuration Register (SIU_PCR266)

Refer to Table 6-19 for bit field definitions. Table 6-132 lists the PA fields for CAL_ADDR[19].

Table 6-132. PCR266 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[19]

6.3.1.145 Pad Configuration Register 267 (SIU_PCR267)

The SIU_PCR267 register controls the function, direction, and electrical attributes of CAL_ADDR[20].

Address: Base + 0x0256 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-145. CAL_ADDR[20] Pad Configuration Register (SIU_PCR267)

Refer to Table 6-19 for bit field definitions. Table 6-133 lists the PA fields for CAL_ADDR[20].

Table 6-133. PCR267 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[20]

6.3.1.146 Pad Configuration Register 268 (SIU_PCR268)

The SIU_PCR268 register controls the function, direction, and electrical attributes of CAL_ADDR[21].

Address: Base + 0x0258 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-146. CAL_ADDR[21] Pad Configuration Register (SIU_PCR268)

Refer to Table 6-19 for bit field definitions. Table 6-134 lists the PA fields for CAL_ADDR[21].

Table 6-134. PCR268 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[21]

6.3.1.147 Pad Configuration Register 269 (SIU_PCR269)

The SIU_PCR269 register controls the function, direction, and electrical attributes of CAL_ADDR[22].

Address: Base + 0x025A Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-147. CAL_ADDR[22] Pad Configuration Register (SIU_PCR269)

Refer to Table 6-19 for bit field definitions. Table 6-135 lists the PA fields for CAL_ADDR[22].

Table 6-135. PCR269 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[22]

6.3.1.148 Pad Configuration Registers 270–271 (SIU_PCR270–SIU_PCR271)

The SIU_PCR270–SIU_PCR271 registers control the function, direction, and electrical attributes of CAL_ADDR[23:24].

Address: Base + (0x025C–0x025E) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-148. CAL_ADDR[23:24] Pad Configuration Registers (SIU_PCR270–SIU_PCR271)

Refer to Table 6-19 for bit field definitions. Table 6-136 lists the PA fields for CAL_ADDR[23:24].

Table 6-136. PCR270–PCR271 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[23:24]

6.3.1.149 Pad Configuration Register 272–274 (SIU_PCR272–SIU_PCR274)

The SIU_PCR272–SIU_PCR274 registers controls the function, direction, and electrical attributes of CAL_ADDR[25:27].

Address: Base + (0x0260–0x0264) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-149. CAL_ADDR[25:27] Pad Configuration Registers (SIU_PCR272–SIU_PCR274)

Refer to Table 6-19 for bit field definitions. Table 6-137 lists the PA fields for CAL_ADDR[25:27].

Table 6-137. PCR272–PCR274 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[25:27]

6.3.1.150 Pad Configuration Register 275 (SIU_PCR275)

The SIU_PCR275 register controls the function, direction, and electrical attributes of CAL_ADDR[28].

Address: Base + 0x0266 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-150. CAL_ADDR[28] Pad Configuration Registers (SIU_PCR275)

Refer to Table 6-19 for bit field definitions. Table 6-138 lists the PA fields for CAL_ADDR[28].

Table 6-138. PCR275 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[28]

6.3.1.151 Pad Configuration Register 276 (SIU_PCR276)

The SIU_PCR276 register controls the function, direction, and electrical attributes of CAL_ADDR[29].

Address: Base + 0x0268 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-151. CAL_ADDR[29] Pad Configuration Registers (SIU_PCR276)

Refer to Table 6-19 for bit field definitions. Table 6-139 lists the PA fields for CAL_ADDR[29].

Table 6-139. PCR276 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[29]

6.3.1.152 Pad Configuration Register 277 (SIU_PCR277)

The SIU_PCR277 register controls the function, direction, and electrical attributes of CAL_ADDR[30].

Address: Base + 0x026A Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-152. CAL_ADDR[30] Pad Configuration Registers (SIU_PCR277)

Refer to Table 6-19 for bit field definitions. Table 6-140 lists the PA fields for CAL_ADDR[30].

Table 6-140. PCR277 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_ADDR[30]

6.3.1.153 Pad Configuration Register 278–293 (SIU_PCR278–SIU_PCR293)

The SIU_PCR278–293 registers control the function, direction, and electrical attributes of CAL_DATA[0:15].

Address: Base + (0x026C–0x028A) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	HYS	0	0	WPE	WPS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Figure 6-153. CAL_DATA[0:15] Pad Configuration Registers (SIU_PCR278–SIU_PCR293)

Refer to Table 6-19 for bit field definitions. Table 6-141 lists the PA fields for CAL_DATA[0:15].

Table 6-141. PCR278–PCR293 PA Field Definitions

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_DATA[0:15]

6.3.1.154 Pad Configuration Register 294 (SIU_PCR294)

The SIU_PCR294 register controls the function, direction, and electrical attributes of the CAL_RD_$\overline{WR}$.

Address: Base + 0x028C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-154. CAL_RD_$\overline{WR}$ Pad Configuration Registers (SIU_PCR294)

Refer to Table 6-19 for bit field definitions. Table 6-142 lists the PA fields for CAL_RD_$\overline{WR}$.

Table 6-142. PCR294 PA Field Definition

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_RD_$\overline{WR}$

6.3.1.155 Pad Configuration Register 295–296 (SIU_PCR295–SIU_PCR296)

The SIU_PCR295–SIU_PCR296 registers control the function, direction, and electrical attributes of CAL_$\overline{WE}$/$\overline{BE}$[0:1].

Address: Base + (0x028E–0x0290) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-155. CAL_$\overline{WE}$/$\overline{BE}$[0:1] Pad Configuration Registers (SIU_PCR295–296)

Refer to Table 6-19 for bit field definitions. Table 6-143 lists the PA fields for CAL_$\overline{WE}$/$\overline{BE}$[0:1].

Table 6-143. PCR295–PCR296 PA Field Definition

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_$\overline{WE}$/$\overline{BE}$[0:1]

6.3.1.156 Pad Configuration Register 297 (SIU_PCR297)

The SIU_PCR297 register controls the function, direction, and electrical attributes of CAL_$\overline{OE}$.

Address: Base + 0x0292 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-156. CAL_$\overline{OE}$ Pad Configuration Registers (SIU_PCR297)

Refer to Table 6-19 for bit field definitions. Table 6-144 lists the PA fields for CAL_$\overline{OE}$.

Table 6-144. PCR297 PA Field Definition

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_$\overline{OE}$

6.3.1.157 Pad Configuration Register 298 (SIU_PCR298)

The SIU_PCR298 register controls the function, direction, and electrical attributes of CAL_$\overline{TS}$.

Address: Base + 0x0294 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	PA	0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-157. CAL_$\overline{TS}$ Pad Configuration Registers (SIU_PCR298)

Refer to Table 6-19 for bit field definitions. Table 6-145 lists the PA fields for CAL_$\overline{TS}$.

Table 6-145. PCR298 PA Field Definition

PA Field	Pin Function
0b0	Invalid value
0b1	CAL_$\overline{TS}$

6.3.1.158 Pad Configuration Register 299 (SIU_PCR299)

The SIU_PCR299 register controls the function, direction, and electrical attributes of CAL_$\overline{CS}$[1]_CAL_ADDR[9].

Address: Base + 0x0296 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	PA		0	0	DSC		0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-158. CAL_$\overline{CS}$[1]_CAL_ADDR[9] Pad Configuration Registers (SIU_PCR299)

Refer to Table 6-19 for bit field definitions. Table 6-146 lists the PA fields for CAL_$\overline{CS}$[1]_CAL_ADDR[9].

Table 6-146. PCR299 PA Field Definitions

PA Field	Pin Function
0b00	Invalid value
0b01	CAL_$\overline{CS}$[1]
0b10	CAL_ADDR[9]
0b11	CAL_$\overline{CS}$[1]

6.3.1.159 GPIO Pin Data Output Registers 0–213 (SIU_GPDO*n*)

The 8-bit SIU_GPDO*n* registers defined in Figure 6-159 each specify the output data for the function assigned to the GPIO[*n*] pin. The *n* notation in the 214 SIU_GPDO*n* register names relate to the [*n*] in GPIO[*n*] signal name. For example, SIU_GPDO0 contains the PDO0 bit for $\overline{CS}$[0]_GPIO[0]; and SIU_GPDO213 contains the PDO213 bit for WKPCFG_GPIO[213]. The address for a GPDO pin is the GPIO number plus an offset of SIU_BASE + 0x0600.

Software writes to the SIU_GPDO*n* registers to drive data out on the external pin. Each register drives one external pin, which allows independent control of the pin. Writes to the SIU_GPDO*n* registers have no effect if an input function is assigned to the pin by the pad configuration register.

If the direction of a GPIO signal changes from input to output, the SIU_GPDO*n* register value is automatically driven out to the external pin without a software update.

Writes to the SIU_GPDO*n* registers have no effect when a primary or alternate function is assigned.

Address: SIU_BASE + 0x0600 R/W

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	0	0
W	PDO*n*							
Reset	0	0	0	0	0	0	0	0

Figure 6-159. General Purpose Data Output (GPDO) Registers 0–213 (SIU_GPDO*n*)

Table 6-147 describes the PDO*n* bit field in the general purpose data output registers:

Table 6-147. SIU_GPDO*n* Field Descriptions

Name	Description
PDO*n*	Pin data out. Stores the data to drive out the external GPIO. If the register is read, it returns the value written. 0 V_{OL} is driven on the external GPIO pin when the pin is configured as an output. 1 V_{OH} is driven on the external GPIO pin when the pin is configured as an output.

6.3.1.160 GPIO Pin Data Input Registers 0–213 (SIU_GPDI*n*)

The 8-bit read-only SIU_GPDI*n* registers defined in Figure 6-160 each specify the input state for the function assigned to the GPDI[*n*] pin. The *n* notation in the214 SIU_GPDI*n* register names relate to the [*n*] in GPIO[*n*] signal name. For example, SIU_GPDI0 contains the PDI0 bit for $\overline{\text{CS}}$[0]_GPIO[0]; and SIU_GPDI213 contains the PDI213 bit for WKPCFG_GPIO[213]. The GPDI address for a particular pin is the GPIO number plus an offset of SIU_BASE + 0x0800. Gaps exist in the memory where GPIO pins are not implemented in the package.

Software reads the SIU_GPDI*n* registers to get the input state of the external GPIO pin. Each GPDI register contains the input state of one external GPIO pin. If a GPDI register is configured as output, and the input buffer enable bit is set to one in the PCR register, the SIU_GPDI*n* register reflects the state of the output pin.

Address: SIU_BASE + 0x0800 R/O

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	0	PDI*n*
W								
Reset	0	0	0	0	0	0	0	0

Figure 6-160. General Purpose Data Input (GPDI) Registers 0–213 (SIU_GPDI*n*)

Table 6-148 describes the PDI*n* bit field in the general purpose data input registers:

Table 6-148. SIU_GPDI*n* Field Descriptions

Name	Description
PDI*n*	Pin data in. This bit reflects the input state on the external GPIO pin for the register. If PCR*n*[IBE] = 1, then: 0 Signal on pin is less than or equal to V_{IL}. 1 Signal on pin is greater than or equal to V_{IH}.

6.3.1.161 eQADC Trigger Input Select Register (SIU_ETISR)

The SIU_ETISR defines the input sources for the eQADC trigger. The eQADC triggers numbered 0–5 are defined in TSEL 0–5 and correspond to CFIFOs 0–5. To determine the valid input pins a trigger activates, divide the DMA channel number by two, and consult Table 6-149. For example, DMA channel 2 is connected to eQADC CFIFO 1, therefore TSEL[1] can be triggered by eTPUA[31], eMIOS[11] or ETRIG[1]. To use a trigger, TSEL must be initialized.

When an eQADC trigger is connected, the timer output is connected to the eQADC CFIFO trigger input. To trigger the eQADC, the timer output pin must change to the state that the eQADC recognizes as a trigger. Rising or falling edges, and low- or high-gated triggers are all valid events that activate a trigger, therefore, it is possible to activate the eQADC trigger immediately if desired.

The following table lists the interconnections for the eQADC triggers:

Table 6-149. Trigger Interconnections

TSEL Field (Trigger Number)	eQADC CFIFO	eQADC DMA Channel	eTPUA Channel	eMIOS Channel	ETRIG Input	GPIO[206]: GPIO[207]
0	0	0	eTPUA[30]	eMIOS[10]	ETRIG[0]	GPIO[206]
1	1	2	eTPUA[31]	eMIOS[11]	ETRIG[1]	GPIO[207]
2	2	4	eTPUA[29]	eMIOS[15]	ETRIG[0]	GPIO[206]
3	3	6	eTPUA[28]	eMIOS[14]	ETRIG[1]	GPIO[207]
4	4	8	eTPUA[27]	eMIOS[13]	ETRIG[0]	GPIO[206]
5	5	10	eTPUA[26]	eMIOS[12]	ETRIG[1]	GPIO[207]

The following register shows the location of the eQADC trigger input select fields:

Address: Base + 0x0900 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	TSEL5		TSEL4		TSEL3		TSEL2		TSEL1		TSEL0		0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-161. eQADC Trigger Input Select Register (SIU_ETISR)

The following table defines the values for the eQADC trigger input select fields:

Table 6-150. SIU_ETISR Field Descriptions

Bits	Name	Description
0–1	TSEL5 [0:1]	eQADC trigger input select 5. Specifies the input for eQADC trigger 5. 00 GPIO[207] 01 ETPUA[26] channel 10 EMIOS[12] channel 11 ETRIG[1] pin
2–3	TSEL4 [0:1]	eQADC trigger input select 4. Specifies the input for eQADC trigger 4. 00 GPIO[206] 01 ETPUA[27] channel 10 EMIOS[13] channel 11 ETRIG[0] pin
4–5	TSEL3 [0:1]	eQADC trigger input select 3. Specifies the input for eQADC trigger 3. 00 GPIO[207] 01 ETPUA[28] channel 10 EMIOS[14] channel 11 ETRIG[1] pin
6–7	TSEL2 [0:1]	eQADC trigger input select 2. Specifies the input for eQADC trigger 2. 00 GPIO[206] 01 ETPUA[29] channel 10 EMIOS[15] channel 11 ETRIG[0] pin
8–9	TSEL1 [0:1]	eQADC trigger input select 1. Specifies the input for eQADC trigger 1. 00 GPIO[207] 01 ETPUA[31] channel 10 EMIOS[11] channel 11 ETRIG[1] pin

Table 6-150. SIU_ETISR Field Descriptions

Bits	Name	Description
10–11	TSEL0 [0:1]	eQADC trigger input select 0. Specifies the input for eQADC trigger 0. 00 GPIO[206] 01 ETPUA[30] channel 10 EMIOS[10] channel 11 ETRIG[0] pin
12–31	—	Reserved

6.3.1.162 External $\overline{\text{IRQ}}$ Input Select Register (SIU_EIISR)

The SIU_EIISR selects the source for the external interrupt/DMA inputs.

Address: Base + 0x0904 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	ESEL15		ESEL14		ESEL13		ESEL12		ESEL11		ESEL10		ESEL9		ESEL8	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	ESEL7		ESEL6		ESEL5		ESEL4		ESEL3		ESEL2		ESEL1		ESEL0	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-162. External $\overline{\text{IRQ}}$ Input Select Register (SIU_EIISR)

The following table describes the external $\overline{\text{IRQ}}$ input select fields:

Table 6-151. SIU_EIISR Field Descriptions

Bits	Name	Description
0–1	ESEL15 [0:1]	External IRQ input select 15. Specifies the input for $\overline{\text{IRQ}}$[15]. 00 $\overline{\text{IRQ}}$[15] 01 PCSB[15] serialized input (EMIOS[12]) 10 PCSC[0] serialized input (ETPUA[12]) 11 PCSD[1] serialized input (ETPUA[20])
2–3	ESEL14 [0:1]	External IRQ input select 14. Specifies the input for $\overline{\text{IRQ}}$[14]. 00 $\overline{\text{IRQ}}$[14] 01 PCSB[14] serialized input (EMIOS[13]) 10 PCSC[15] serialized input (ETPUA[11]) 11 PCSD[0] serialized input (ETPUA[21])
4–5	ESEL13 [0:1]	External IRQ input select 13. Specifies the input for $\overline{\text{IRQ}}$[13]. 00 $\overline{\text{IRQ}}$[13] 01 PCSB[13] serialized input (ETPUA[24]) 10 PCSC[14] serialized input (ETPUA[10]) 11 PCSD[15] serialized input (ETPUA[24])

Table 6-151. SIU_EIISR Field Descriptions

Bits	Name	Description
6–7	ESEL12 [0:1]	External IRQ input select 12. Specifies the input for $\overline{IRQ}$[12]. 00 $\overline{IRQ}$[12] pin 01 PCSB[12] serialized input (ETPUA[25]) 10 PCSC[13] serialized input (ETPUA[9]) 11 PCSD[14] serialized input (ETPUA[25])
8–9	ESEL11 [0:1]	External IRQ input select 11. Specifies the input for $\overline{IRQ}$[11]. 00 $\overline{IRQ}$[11] 01 PCSB[11] serialized input (ETPUA[26]) 10 PCSC[12] serialized input (ETPUA[8]) 11 PCSD[13] serialized input (ETPUA[26])
10–11	ESEL10 [0:1]	External IRQ input select 10. Specifies the input for $\overline{IRQ}$10]. 00 $\overline{IRQ}$[10] 01 PCSB[10] serialized input (ETPUA[27]) 10 PCSC[11] serialized input (ETPUA[7]) 11 PCSD[12] serialized input (ETPUA[27])
12–13	ESEL9 [0:1]	External IRQ input select 9. Specifies the input for $\overline{IRQ}$[9]. 00 $\overline{IRQ}$[9] 01 PCSB[9] serialized input (ETPUA[28]) 10 PCSC[10] serialized input (ETPUA[6]) 11 PCSD[11] serialized input (ETPUA[28])
14–15	ESEL8 [0:1]	External IRQ input select 8. Specifies the input for $\overline{IRQ}$[8]. 00 $\overline{IRQ}$[8] 01 PCSB[8] serialized input (ETPUA[29]) 10 PCSC[9] serialized input (ETPUA[5]) 11 PCSD[10] serialized input (ETPUA[29])
16–17	ESEL7 [0:1]	External IRQ input select 7. Specifies the input for $\overline{IRQ}$[7]. 00 $\overline{IRQ}$[7] 01 PCSB[7] serialized input (ETPUA[16]) 10 PCSC[8] serialized input (ETPUA[4]) 11 PCSD[9] serialized input (EMIOS[12])
18–19	ESEL6 [0:1]	External IRQ input select 6. Specifies the input for $\overline{IRQ}$[6]. 00 $\overline{IRQ}$[6] 01 PCSB[6] serialized input (ETPUA[17]) 10 PCSC[7] serialized input (ETPUA[3]) 11 PCSD[8] serialized input (EMIOS[13])
20–21	ESEL5 [0:1]	External IRQ input select 5. Specifies the input for $\overline{IRQ}$[5]. 00 $\overline{IRQ}$[5] 01 PCSB[5] serialized input (ETPUA[18]) 10 PCSC[6] serialized input (ETPUA[2]) 11 PCSD[7] serialized input (EMIOS[10])
22–23	ESEL4 [0:1]	External IRQ input select 4. Specifies the input for $\overline{IRQ}$[4]. 00 $\overline{IRQ}$[4] 01 PCSB[4] serialized input (ETPUA[19]) 10 PCSC[5] serialized input (ETPUA[1]) 11 PCSD[6] serialized input (EMIOS[11])

Table 6-151. SIU_EIISR Field Descriptions

Bits	Name	Description
24–25	ESEL3 [0:1]	External IRQ input select 3. Specifies the input for $\overline{IRQ}$[3]. 00 $\overline{IRQ}$[3] 01 PCSB[3] serialized input (ETPUA[20]) 10 PCSC[4] serialized input (ETPUA[0]) 11 PCSD[5] serialized input (ETPUA[16])
26–27	ESEL2 [0:1]	External IRQ input select 2. Specifies the input for $\overline{IRQ}$[2]. 00 $\overline{IRQ}$[2] 01 PCSB[2] serialized input (ETPUA[21]) 10 PCSC[3] serialized input (ETPUA[15]) 11 PCSD[4] serialized input (ETPUA[17])
28–29	ESEL1 [0:1]	External IRQ input select 1. Specifies the input for $\overline{IRQ}$[1]. 00 $\overline{IRQ}$[1] 01 PCSB[1] serialized input (EMIOS[10]) 10 PCSC[2] serialized input (ETPUA[14]) 11 EMIOS[15]
30–31	ESEL0 [0:1]	External IRQ input select 0. Specifies the input for $\overline{IRQ}$[0]. 00 $\overline{IRQ}$[0] 01 PCSB[0] serialized input (EMIOS[11]) 10 PCSC[1] serialized input (ETPUA[5]) 11 EMIOS[14]

6.3.1.163 DSPI Input Select Register (SIU_DISR)

Within the MPC5500 family of devices, the SIU_DISR specifies the following operations for each DSPI:

- Data input source
- Slave select
- Clock input

Trigger input to allow serial and parallel chaining of the DSPI modules.

Address: Base + 0x0908 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	SINSELA		SSSELA		SCKSELA		TRIGSELA		SINSELB		SSSELB		SCKSELB		TRIGSELB	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	SINSELC		SSSELC		SCKSELC		TRIGSELC		SINSELD		SSSELD		SCKSELD		TRIGSELD	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-163. DSPI Input Select Register (SIU_DISR)

The following table describes the DSPI input select fields:

Table 6-152. SIU_DISR Field Descriptions

Bits	Name	Description
0–1	SINSELA [0:1]	DSPI A data input select. Specifies the source of the DSPI A data input. 00 SINA_PCSC[2]_GPIO[94] pin 01 SOUTB 10 SOUTC 11 SOUTD
2–3	SSSELA [0:1]	DSPI A slave select input select. Specifies the source of the DSPI A slave select input. 00 PCSA[0]_GPIO[96] pin 01 PCSB[0] (master) 10 PCSC[0] (master) 11 PCSD[0] (master)
4–5	SCKSELA [0:1]	DSPI A clock input select. Specifies the source of the DSPI A clock input. 00 SCKA_PCSC[1]_GPIO[93] pin 01 SCKB (master) 10 SCKC (master) 11 SCKD (master)
6–7	TRIGSELA [0:1]	DSPI A trigger input select. Specifies the source of the DSPI A trigger input. 00 No Trigger 01 PCSB[4] 10 PCSC[4] 11 PCSD[4]
8–9	SINSELB [0:1]	DSPI B data input select. Specifies the source of DSPI B data input. 00 SINB_PCSC[2]_GPIO[103] pin 01 SOUTA 10 SOUTC 11 SOUTD
10–11	SSSELB [0:1]	DSPI B slave select input select. Specifies the source of the DSPI B slave select input. 00 PCSB[0]_PCSD[2]_GPIO[105] pin 01 PCSA[0] (master) 10 PCSC[0] (master) 11 PCSD[0] (master)
12–13	SCKSELB [0:1]	DSPI B clock input select. Specifies the source of the DSPI B clock input. 00 SCKB_PCSC[1]_GPIO[102] pin 01 SCKA (master) 10 SCKC (master) 11 SCKD (master)
14–15	TRIGSELB [0:1]	DSPI B trigger input select. Specifies the source of the DSPI B trigger input for master or slave mode. 00 Invalid value 01 PCSA[4] 10 PCSC[4] 11 PCSD[4]

Table 6-152. SIU_DISR Field Descriptions

Bits	Name	Description
16–17	SINSELC [0:1]	DSPI C data input select. Specifies the source of the DSPI C data input. 00 PCSB[3]_SINC_GPIO[108] pin 01 SOUTA 10 SOUTB 11 SOUTD
18–19	SSSELC [0:1]	DSPI C slave select input select. Specifies the source of the DSPI C slave select input. 00 PCSB[5]_PCSC[0]_GPIO[110] pin 01 PCSA[0] (master) 10 PCSB[0] (master) 11 PCSD[0] (master)
20–21	SCKSELC [0:1]	DSPI C clock input select. Specifies the source of the DSPI C clock input when in slave mode. 00 PCSB[4]_SCKC_GPIO[109] pin 01 SCKA (master) 10 SCKB (master) 11 SCKD (master)
22–23	TRIGSELC [0:1]	DSPI C trigger input select. Specifies the source of the DSPI C trigger input for master or slave mode. 00 Invalid value 01 PCSA[4] 10 PCSB[4] 11 PCSD[4]
24–25	SINSELD [0:1]	DSPI D data input select. Specifies the source of the DSPI D data input. 00 PCSA[3]_SIND_GPIO[99] pin 01 SOUTA 10 SOUTB 11 SOUTC
26–27	SSSELD [0:1]	DSPI D slave select input select. Specifies the source of the DSPI D slave select input. 00 PCSB[1]_PCSD[0]_GPIO[106] pin 01 PCSA0 (master) 10 PCSB0 (master) 11 PCSC0 (master)
28–29	SCKSELD [0:1]	DSPI D clock input select. Specifies the source of the DSPI D clock input in slave mode. 00 PCSA[2]_SCKD_GPIO[98] pin 01 Invalid value 10 SCKB (master) 11 SCKC (master)
30–31	TRIGSELD [0:1]	DSPI D trigger input select. Specifies the source of the DSPI D trigger input for master or slave mode. 00 Invalid value 01 PCSA4 10 PCSB4 11 PCSC4

6.3.1.164 Chip Configuration Register (SIU_CCR)

The SIU_CCR controls the chip configuration for enabling and disabling Nexus and selecting the calibration bus signals on the external bus interface.

Address: Base + 0x0980 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MATCH	DISNEX
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X[1]

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CSRE	TEST
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[1] When system reset negates, the value in this bit depends on the censorship control word and the boot configuration bits.

Figure 6-164. Chip Configuration Register (SIU_CCR)

The following table describes the chip configuration fields:

Table 6-153. SIU_CCR Field Descriptions

Bits	Name	Description
0–13	—	Reserved
14	MATCH	Compare register match. Holds the value of the match input signal to the SIU. The match input is asserted if the values in the SIU_CARH/SIU_CARL and SIU_CBRH/SIU_CBRL are equal. The MATCH bit is reset by the synchronous reset signal. 0 The contents of SIU_CARH and SIU_CARL does not match the contents of SIU_CBRH and SIU_CBRL 1 The contents of SIU_CARH and SIU_CARL matches the contents of SIU_CBRH and SIU_CBRL
15	DISNEX	Disable Nexus. Holds the value of the Nexus disable input signal to the SIU. When system reset negates, the value in this bit depends on the censorship control word and the boot configuration bits. 0 Nexus disable input signal is negated. 1 Nexus disable input signal is asserted.
16–29	—	Reserved

Table 6-153. SIU_CCR Field Descriptions

Bits	Name	Description
30	CSRE	The CRSE bit enables the suppression of reflection from the EBI's calibration bus onto the non-calibration bus. The EBI drives some outputs to both the calibration and non-calibration busses. When CRSE is asserted, the values driven onto the calibration bus are not reflected onto the non-calibration bus pins. When CRSE is negated, the values driven onto the calibration bus are reflected onto the non-calibration bus. CRSE only enables reflection suppression for the non-calibration bus pins that do not have a negated state to which the pins return at the end of the access. CRSE does not enable reflection suppression for the non-calibration bus pins that have a negated state to which the pins return at the end of an access. Those reflections always are suppressed. Furthermore, the suppression of reflections from the non-calibration bus onto the calibration bus is not enabled by CRSE. Those reflections also always are suppressed. 0 Calibration reflection suppression is enabled. 1 Calibration reflection suppression is disabled.
31	TEST	Test mode enable. Allows reads or writes to undocumented registers used only for production tests. Since these production test registers are undocumented, estimating the impact of errant accesses to them is impossible. Do not change this bit from its negated state at reset. 0 Undocumented production test registers cannot be read or written. 1 Undocumented production test registers can be read or written.

6.3.1.165 External Clock Control Register (SIU_ECCR)

The SIU_ECCR controls the timing relationship between the system clock and the external clocks ENGCLK and CLKOUT. All bits and fields in the SIU_ECCR are read/write and are reset by the synchronous reset signal.

Address: Base + 0x0984 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	ENGDIV						0	0	0	0	EBTS	0	EBDF	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 6-165. External Clock Control Register (SIU_ECCR)

The following table describes the external clock control fields:

Table 6-154. SIU_ECCR Field Descriptions

Bits	Name	Description
0–17	—	Reserved
18–23	ENGDIV [0:5]	Engineering clock division factor. Specifies the frequency ratio between the system clock and ENGCLK. The ENGCLK frequency is divided from the system clock frequency according to the following equation: $\text{Engineering clock frequency} = \frac{\text{System clock frequency}}{\text{ENGDIV} \times 2}$ The maximum ENGCLK frequency is 72 MHz (144 MHz ÷ 2) **Note:** Clearing ENGDIV to 0 is the reset setting. Synchronization between ENGCLK and CLKOUT cannot be guaranteed when ENGDIV is 0.
24–27	—	Reserved
28	EBTS	External bus tap select. Changes the phase relationship between the system clock and CLKOUT. Changing the phase relationship so that CLKOUT is advanced in relation to the system clock increases the output hold time of the external bus signals to a non-zero value. It also increases the output delay times, increases the input hold times to non-zero values, and decreases the input setup times. Refer to the *Electrical Specifications* for how the EBTS bit affects the external bus timing. 0 External bus signals have zero output hold times. 1 External bus signals have non-zero output hold times. **Note:** Do not change EBTS while an external bus transaction is in process.
29	—	Reserved
30–31	EBDF [0:1]	External bus division factor. Specifies the frequency ratio between the system clock and the external clock, CLKOUT. Do not change EBDF during an external bus access or while an access is pending. The CLKOUT frequency is divided from the system clock frequency according to the descriptions below. When operating in dual controller mode (1:1), set the divider to 0b01 (divide-by-2). 00 Invalid value 01 Divide by 2 10 Invalid value 11 Divide by 4

6.3.1.166 Compare A Register High (SIU_CARH)

The compare registers are not intended for general application use, but are used temporarily by the BAM during boot and intended optionally for communication with calibration tools. After reset, calibration tools can immediately write a non-zero value to these registers. The application code, using the registers then as read only, can read them to determine if a calibration tool is attached and operate appropriately.

The compare registers can be used just like 128 bits of memory mapped RAM that is always 0 out of reset, or they can perform a 64-bit to 64-bit compare. The compare function is continuous (combinational logic — not requiring a start or stop). The compare result appears in the MATCH bit in the SIU_CCR register.

The SIU_CARH holds the 32-bit value that is compared against the value in the SIU_CBRH register. The CMPAH field is read/write and is reset by the synchronous reset signal.

Address: Base + 0x0988 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	CMPAH															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	CMPAH															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-166. Compare A Register High (SIU_CARH)

6.3.1.167 Compare A Register Low (SIU_CARL)

The SIU_CARL register holds the 32-bit value that is compared against the value in the SIU_CBRL register. The CMPAL field is read/write and is reset by the synchronous reset signal.

Address: Base + 0x098C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	CMPAL															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	CMPAL															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-167. Compare A Register Low (SIU_CARL)

6.3.1.168 Compare B Register High (SIU_CBRH)

The SIU_CBRH holds the 32-bit value that is compared against the value in the SIU_CARH. The CMPBH field is read/write and is reset by the synchronous reset signal.

Address: Base + 0x0990 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	CMPBH															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	CMPBH															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-168. Compare B Register High (SIU_CBRH)

6.3.1.169 Compare B Register Low (SIU_CBRL)

The SIU_CBRL holds the 32-bit value that is compared against the value in the SIU_CARL. The CMPBL field is read/write and is reset by the synchronous reset signal.

Address: Base + 0x0994 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	CMPBL															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	CMPBL															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-169. Compare B Register Low (SIU_CBRL)

6.4 Functional Description

The following sections provide a functional overview of the SIU operation.

6.4.1 System Configuration

The following sections describe the system configuration.

6.4.1.1 Boot Configuration

The BOOTCFG[0:1] pins determine the boot mode initiated by the BAM program, and whether external arbitration is selected for external booting. The BAM program uses the BOOTCFG[0] to determine where to read the reset configuration halfword (RCHW), and whether to initiate a FlexCAN or eSCI boot.

Table 6-155 defines the boot modes specified by the BOOTCFG[0:1] pins. If the $\overline{\text{RSTCFG}}$ pin is asserted during the assertion of $\overline{\text{RSTOUT}}$, except in the case of a software external reset, the BOOTCFG pins are latched four clock cycles prior to the negation of the $\overline{\text{RSTOUT}}$ pin and are used to update the SIU_RSR and the BAM boot mode. Otherwise, if $\overline{\text{RSTCFG}}$ is negated during the assertion of $\overline{\text{RSTOUT}}$, the BOOTCFG pins are ignored and the boot mode defaults to 'Boot from internal flash memory.'

Table 6-155. BOOTCFG[0:1] Configuration

Value	Meaning
0b00	Boot from internal flash memory
0b01	FlexCAN/eSCI boot
0b10	Boot from external memory (no arbitration)
0b11	Boot from external memory (external arbitration)

Refer to Section 16.3.2.2.5, "Read the Reset Configuration Halfword," for details on the RCHW.

6.4.1.2 Pad Configuration

The pad configuration registers (SIU_PCR) in the SIU allow software control over the following electrical characteristics of the external pads:

- Weak pullup/down enable/disable
- Weak pullup/down selection
- Slew-rate selection for outputs
- Drive strength selection for outputs
- Input buffer enable (when direction is configured for output)
- Input hysteresis enable/disable
- Open drain/push-pull output selection
- Multiplexed function selection
- Data direction selection

The pad configuration registers are provided to allow centralized control over external pins that are shared by more than one module. Each pad configuration register controls a single pin.

6.4.2 Reset Control

The reset controller logic is located in the SIU. Refer to Section 6.2.1.1, “Reset Input (RESET),” and Section 6.2.1.2, “Reset Output (RSTOUT)” for details on the reset operations.

6.4.2.1 $\overline{\text{RESET}}$ Pin Glitch Detect

The reset controller provides a glitch detect feature on the $\overline{\text{RESET}}$ pin. If the reset controller detects that the $\overline{\text{RESET}}$ pin is asserted for more than two clock cycles, the event is latched. After the latch is set, if the $\overline{\text{RESET}}$ pin is negated before 10 clock cycles is reached, the reset controller sets the RGF bit without affecting any of the other bits in the reset status register (SIU_RSR). The latch is cleared when the RGF bit is set or a valid reset is recognized. The RGF bit remains set until cleared by a software or the $\overline{\text{RESET}}$ signal asserts for 10 clock cycles. The reset controller does not respond to assertions of the $\overline{\text{RESET}}$ pin if a reset cycle is already being processed.

6.4.3 External Interrupt

There are 1516 external interrupt inputs $\overline{\text{IRQ}}$[0]–$\overline{\text{IRQ}}$[15] to the SIU. The IRQ inputs can be configured for rising-edge events, falling-edge events, or both. Each $\overline{\text{IRQ}}$ input has a flag bit in the external interrupt status register (SIU_EISR). The flag bits for the $\overline{\text{IRQ}}$[4:15] inputs are OR’ed together to form one interrupt request to the interrupt controller (OR function performed in the integration glue logic). The flag bits for the $\overline{\text{IRQ}}$[0:3] inputs can generate either an interrupt request to the interrupt controller or a DMA transfer request to the DMA controller.

Figure 6-170 shows the DMA and interrupt request connections to the interrupt and DMA controllers.

The SIU contains an overrun request for each IRQ and one combined overrun request which is the logical OR of the individual overrun requests. Only the combined overrun request is used in the device, and the individual overrun requests are not connected.

Each IRQ pin has a programmable filter for rejecting glitches on the IRQ signals. The filter length for the IRQ pins is specified in the external IRQ digital filter register (SIU_IDFR).

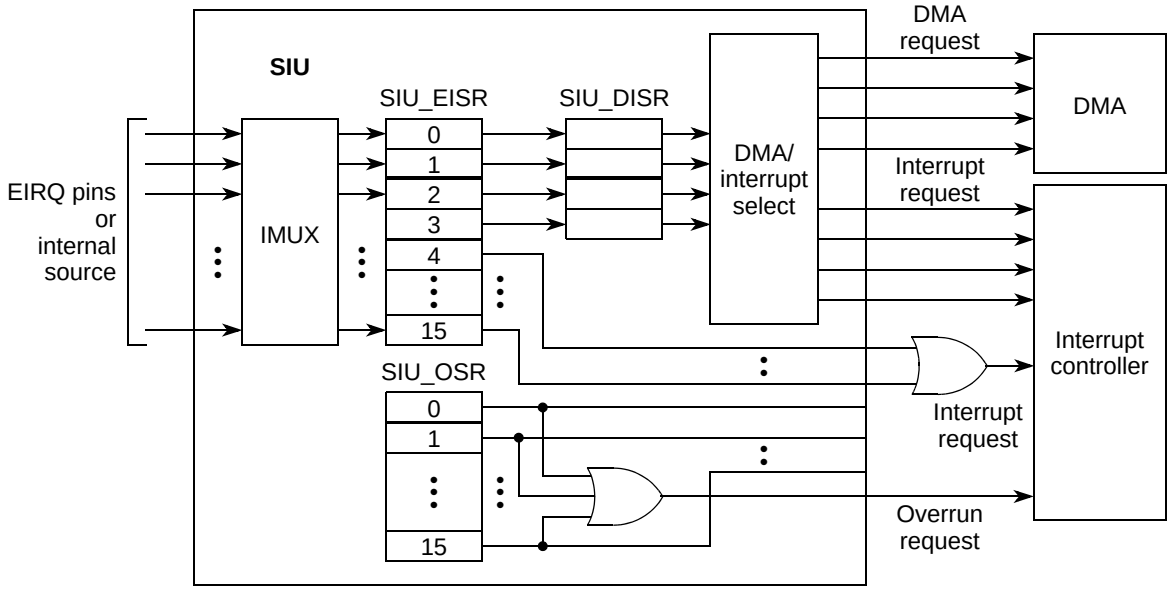


Figure 6-170. SIU DMA/Interrupt Request Diagram

6.4.4 GPIO Operation

All GPIO functions for the device are provided by the SIU. Each device pad that has a GPIO signal has a pin configuration register (PCR) in the SIU where the GPIO function is selected. In addition, each device GPIO signal has an input data register (SIU_GPDI*n*) and an output data register (SIU_GPDO*n*).

6.4.5 Internal Multiplexing

The internal multiplexing select registers (SIU_ETISR, SIU_EIISR, and SIU_DISR) select the input source for the following components:

- eQADC external trigger input signals
- SIU external interrupt request signals
- DSPI signals used for chaining serial and parallel DSPI modules

A block diagram of the internal multiplexing feature is shown in Figure 6-171. The figure shows the multiplexing of four external signals to an SIU output. A 2-bit SEL field from an SIU select register defines the input to the multiplexor.

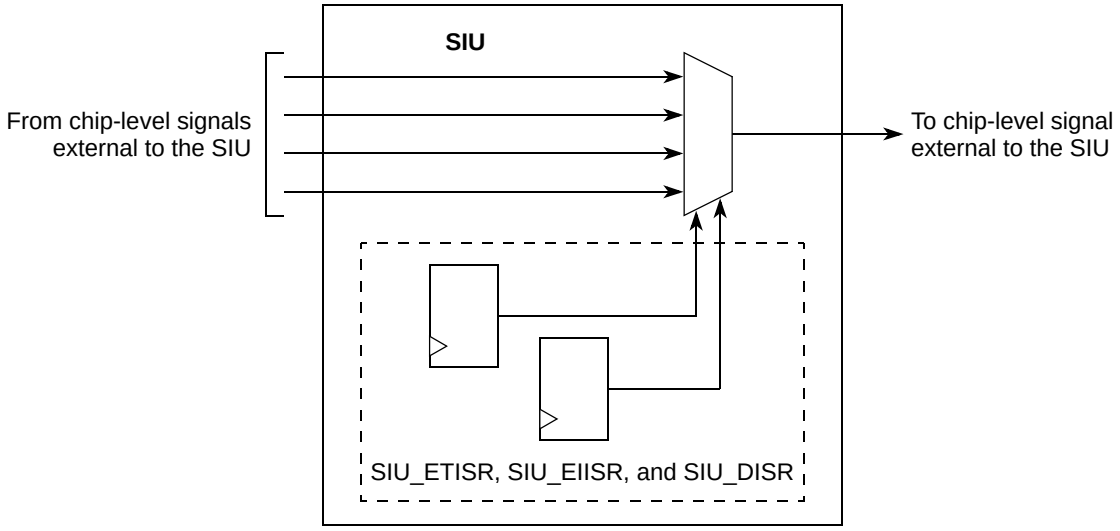


Figure 6-171. Four-to-One Internal Multiplexing Block Diagram

6.4.5.1 eQADC External Trigger Input Multiplexing

The six eQADC external trigger inputs can connect to one of the following pins:

- External pin
- eTPU channel
- eMIOS channel

The input source for each eQADC external trigger is configured in the eQADC trigger input select register (SIU_ETISR). As shown in the figure, you can select one of the following signals to source to the ETRIG[0] input to the eQADC:

- ETRIG[0]_GPIO[111] pin
- ETPUA[30] output channel
- EMIOS[10] output channel
- GPIO[206] pin

All ETRIG inputs are multiplexed in the same manner. If an eTPU or eMIOS channel is selected as an ETRIG input to the eQADC, you can activate the alternate function of that eTPU or eMIOS signal on the external pin.

An example of the multiplexing of an eQADC external trigger input is given in Figure 6-172.

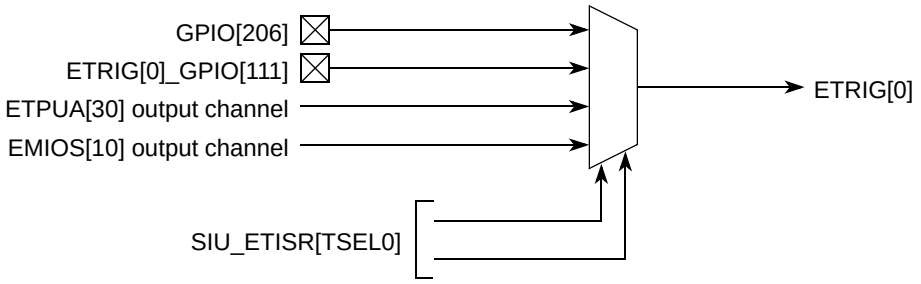


Figure 6-172. eQADC External Trigger Input Multiplexing

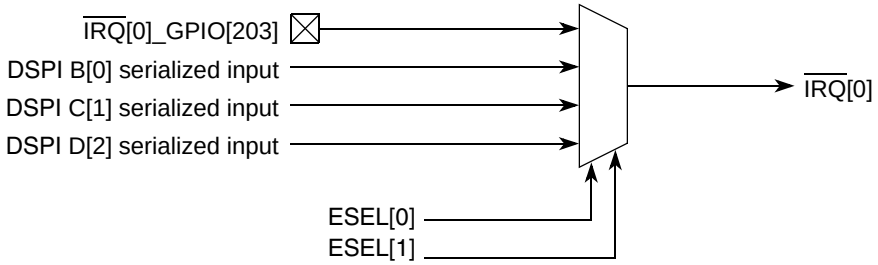
Refer to Section 6.3.1.161, "eQADC Trigger Input Select Register (SIU_ETISR)" for the SIU_ETISR[TSEL0]–SIU_ETISR[TSEL5] bit definitions.

6.4.5.2 SIU External Interrupt Input Multiplexing

The sixteen SIU external interrupt inputs can be connected to either an external pin or to serialized output signals from a DSPI module. The input source for each SIU external interrupt is individually specified in the external IRQ input select register (SIU_EIISR).

As shown in the figure, the $\overline{\text{IRQ}}$[0] input of the SIU can be connected to either the $\overline{\text{IRQ}}$[0]_GPIO[203] pin, the PCSB[0] serial input signal, the PCSC[1] deserialized output signal, or the PCSD[2] deserialized output signal. The remaining IRQ inputs are multiplexed in the same manner. The inputs to the IRQ from each DSPI module are offset by one so that if more than one DSPI module is connected to the same external device type, a separate interrupt can be generated for each device. This also applies to DSPI modules connected to external devices of different type that have status bits in the same bit location of the deserialized information.

An example of the multiplexing of an SIU external interrupt input is given in Figure 6-173.



NOTE: The MPC5566 has DSPI A in addition to B, C, D.

Figure 6-173. DSPI Serialized Input Multiplexing

6.4.5.3 Multiplexed Inputs for DSPI Multiple Transfer Operation

Each DSPI module can be combined in a serial or parallel chain (multiple transfer operation). Serial chaining allows SPI operation with an external device that has more bits than one DSPI module.

In a serial chain, one DSPI module operates as a master, the second, third, or fourth DSPI modules operate as slaves. The data output (SOUT) of the master is connected to the data input (SIN) of the slave. The SOUT of a slave is connected to the SIN of subsequent slaves until the last module in the chain, where the SOUT is connected to an external pin, which connects to the input of an external SPI device. The slave DSPI and external SPI device use the master peripheral chip select (PCS) and clock (SCK). The trigger input of the master allows a slave DSPI to trigger a transfer when a data change occurs in the slave DSPI and the slave DSPI is operating in change in data mode. The trigger input of the master is connected to the $\overline{\text{MTRIG}}$ output of the slave. If more than two DSPIs are chained in change in data mode, a chain must be connected of $\overline{\text{MTRIG}}$ outputs to trigger inputs through the slaves with the last slave $\overline{\text{MTRIG}}$ output connected to the master trigger input.

An example of a serial chain is shown in Figure 6-174.

Parallel chaining allows the PCS and SCK from one DSPI to be used by more than one external SPI device, thus reducing pin utilization of the device MCU. In this example, the SOUT and SIN of the two DSPIs connect to separate external SPI devices, which share a common PCS and SCK.

To support multiple transfer operation of the DSPIs, an input multiplexor is required for the SIN, $\overline{\text{SS}}$, SCK IN, and trigger signals of each DSPI. The input source for the SIN input of a DSPI can be a pin or the SOUT of any of the other three DSPIs. The input source for the $\overline{\text{SS}}$ input of a DSPI can be a pin or the PCS*X*[0] of any of the other three DSPIs. The input source for the SCK input of a DSPI can be a pin or the SCK output of any of the other three DSPIs. The input source for the trigger input can be the $\overline{\text{PCSS}}$ output of any of the other three DSPIs. The input source for each DSPI SIN, $\overline{\text{SS}}$, SCK, and trigger signal is individually specified in the DSPI input select register (SIU_DISR).

An example of a parallel chain is shown in Figure 6-174.

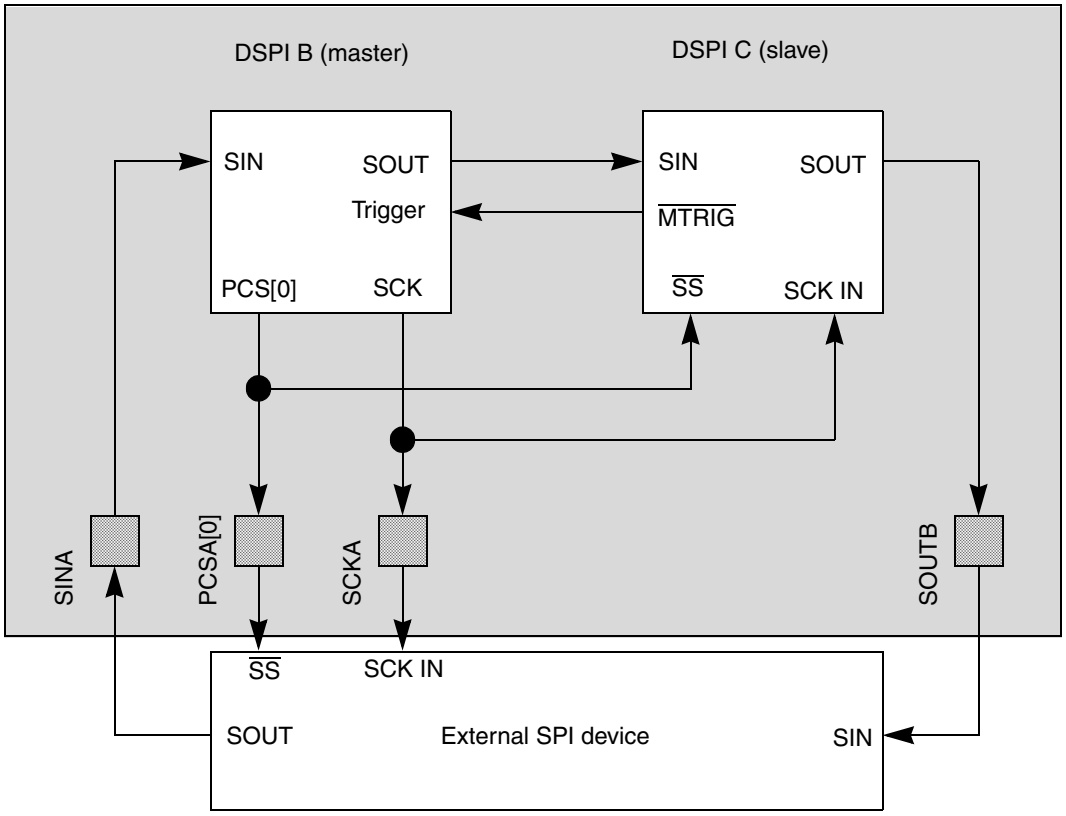


Figure 6-174. DSPI Serial Chaining

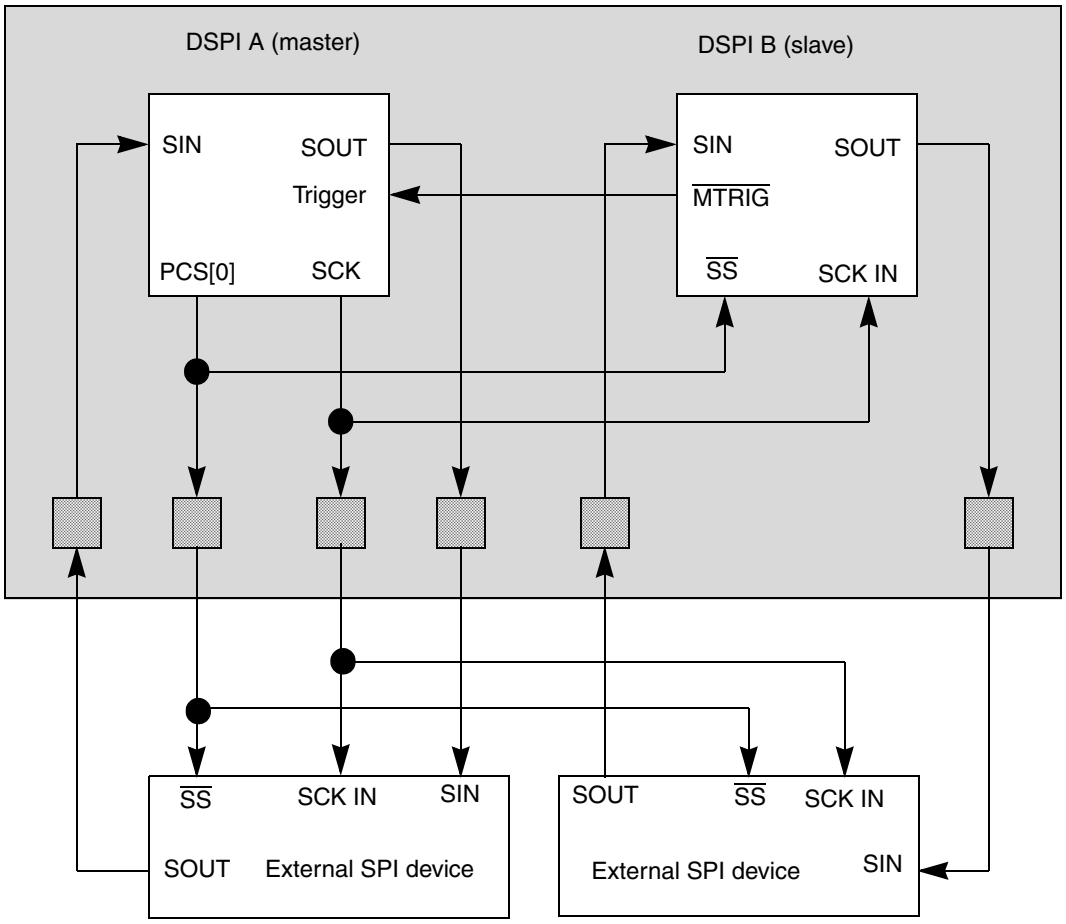


Figure 6-175. DSPI Parallel Chaining

Chapter 7
Crossbar Switch (XBAR)

7.1 Introduction

This chapter describes the multi-port crossbar switch (XBAR), which supports simultaneous connections between master ports and five slave ports. XBAR supports a 32-bit address bus width and a 64-bit data bus width at all master and slave ports.

7.1.1 Block Diagram

Figure 7-1 shows a block diagram of the crossbar switch.

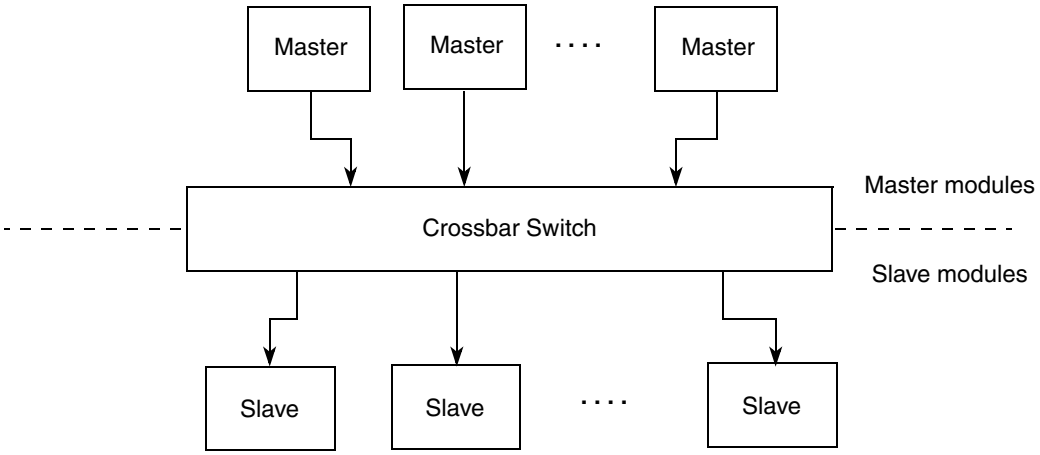


Figure 7-1. XBAR Block Diagram

Table 7-1 gives the crossbar switch port for each master and slave, and the assigned and fixed ID number for each master. The following table shows the master ID numbers as they relate to the master port numbers:

Table 7-1. XBAR Switch Ports

Module	Port		Master ID
	Type	Number	
e200z6 core–CPU instruction / data	Master	0	0
e200z6–Nexus	Master	0	1
eDMA_A	Master	1	2
External bus interface	Master	2	3
FEC	Master	3	4

Table 7-1. XBAR Switch Ports (continued)

Module	Port		Master ID
	Type	Number	
eDMA_B	Master	5	5
Flash	Slave	0	—
External bus interface	Slave	1	—
Internal SRAM	Slave	3	—
Peripheral bridge A (PBRIDGE_A)	Slave	6	—
Peripheral bridge B (PBRIDGE_B)	Slave	7	—

7.1.2 Overview

The XBAR allows for concurrent transactions to occur from any master port to any slave port. It is possible for all master ports and slave ports to be in use at the same time as a result of independent master requests. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions.

By default, requesting masters are granted access based on a fixed priority. A round-robin priority mode also is available. In this mode, requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. A block diagram of the XBAR is shown in Figure 7-1.

The XBAR can place a slave port in a low-power park mode to avoid dissipating any power transitional address, control or data signals when the master port is not actively accessing the slave port. There is a one-cycle arbitration overhead for exiting low-power park mode.

7.1.3 Features

- Four master ports:
  - core: e200z6 core and Nexus
  - eDMA
  - EBI
  - FEC
- Five slave ports
  - Flash (refer to Chapter 13, “Flash Memory” for information on accessing flash memory)
  - EBI
  - Internal SRAM
  - Peripheral bridge A
  - Peripheral bridge B
- 32-bit address, 64-bit data paths
- Fully concurrent transfers between independent master and slave ports

7.1.4 Modes of Operation

7.1.4.1 Normal Mode

In normal mode, the XBAR provides the register interface and logic that controls crossbar switch configuration.

7.1.4.2 Debug Mode

The XBAR operation in debug mode is identical to operation in normal mode.

7.2 Memory Map and Register Definition

The memory map for the XBAR program-visible registers is shown in Table 7-2.

Table 7-2. XBAR Register Memory Map

Address	Register Name	Register Description	Bits
Base = 0xFFF0_4000	XBAR_MPR0	Master priority register for slave port 0	32
Base + (0x0004–0x000F)	—	Reserved	—
Base + 0x0010	XBAR_SGPCR0	General-purpose control register for slave port 0	32
Base + (0x0014–0x00FF)	—	Reserved	—
Base + 0x0100	XBAR_MPR1	Master priority register for slave port 1	32
Base +(0x0104–0x010F)	—	Reserved	—
Base + 0x0110	XBAR_SGPCR1	General-purpose control register for slave port 1	32
Base + (0x0114–0x02FF)	—	Reserved	—
Base + 0x0300	XBAR_MPR3	Master priority register for slave port 3	32
Base + (0x0304–0x030F)	—	Reserved	—
Base + 0x0310	XBAR_SGPCR3	General-purpose control register for slave port 3	32
Base + (0x0314–0x05FF)	—	Reserved	—
Base + 0x0600	XBAR_MPR6	Master priority register for slave port 6	32
Base + (0x0604–0x060F)	—	Reserved	—
Base + 0x0610	XBAR_SGPCR6	General-purpose control register for slave port 6	32
Base + (0x0614–0x06FF)	—	Reserved	—
Base + 0x0700	XBAR_MPR7	Master priority register for slave port 7	32
Base + (0x0704–0x070F)	—	Reserved	—
Base + 0x0710	XBAR_SGPCR7	General-purpose control register for slave port 7	32
Base + 0x0714–0x0003_FFFF	—	Reserved	—

7.2.1 Register Descriptions

There are two registers for each slave port of the XBAR. The registers can only be accessed in supervisor mode using 32-bit accesses.

The slave SGPCR also features a bit (RO), which when written with a 1, prevents all slave registers for that port from being written to again until a reset occurs. The registers remain readable, but future write attempts have no effect on the registers and are terminated with an error response.

The difference in numerical values of XBAR Master Port and Master ID is shown in Table 7-3.

Table 7-3. XBAR Switch Ports

Module	Port		Master ID
	Type	Number	
e200z6 core—CPU instruction / data	Master	0	0
e200z6—Nexus	Master	0	1
eDMA_A	Master	1	2
External bus interface	Master	2	3
FEC	Master	3	4
eDMA B	Master	5	5
Flash	Slave	0	—
External bus interface	Slave	1	—
Internal SRAM	Slave	3	—
Peripheral bridge A (PBRIDGE_A)	Slave	6	—
Peripheral bridge B (PBRIDGE_B)	Slave	7	—

7.2.1.1 Master Priority Registers (XBAR_MPR*n*)

The XBAR_MPR for a slave port sets the priority of each master port when operating in fixed priority mode. They are ignored in round-robin priority mode unless more than one master has been assigned high priority by a slave.

NOTE

Masters must be assigned unique priority levels.

The master priority register can only be accessed in supervisor mode with 32-bit accesses. After the read only (RO) bit is set in the slave general-purpose control register, the master priority register can only be read. Attempts to write to it have no effect on the MPR and result in an error.

NOTE

XBAR_MPR must be written with a read/modify/write for code compatibility.

Addess: Base + 0x0000 (XBAR_MPR0)
Base + 0x0100 (XBAR_MPR1)
Base + 0x0300 (XBAR_MPR3)
Base + 0x0600 (XBAR_MPR6)
Base + 0x0700 (XBAR_MPR7)

Access: Supervisor R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	MSTR6 (not used)			0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	MSTR3			0	MSTR2			0	MSTR1			0	MSTR0		
W																
Reset	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Figure 7-2. Master Priority Registers (XBAR_MPR*n*)

Table 7-4. XBAR_MPR*n* Descriptions

Field	Description
0–16	Reserved, must be cleared.
17–19 MSTR3	Master 3 priority. Set the arbitration priority for master port 3 on the associated slave port. 000 This master has the highest priority when accessing the slave port. ⋮ 100 This master has the lowest priority when accessing the slave port. 101–111 Invalid values
20	Reserved, must be cleared.
21–23 MSTR2	Master 2 priority. Set the arbitration priority for master port 2 on the associated slave port. 000 This master has the highest priority when accessing the slave port. ⋮ 100 This master has the lowest priority when accessing the slave port. 101–111 Invalid values
24	Reserved, must be cleared.
25–27 MSTR1	Master 1 priority. Set the arbitration priority for master port 1 on the associated slave port. 000 This master has the highest priority when accessing the slave port. ⋮ 100 This master has the lowest priority when accessing the slave port. 101–111 Invalid values

Table 7-4. XBAR_MPR*n* Descriptions (continued)

Field	Description
28	Reserved, must be cleared.
29–31 MSTR0	Master 0 priority. Set the arbitration priority for master port 0 on the associated slave port. 000 This master has the highest priority when accessing the slave port. ⋮ 100 This master has the lowest priority when accessing the slave port. 101–111 Invalid values

7.2.1.2 Slave General-Purpose Control Registers (XBAR_SGPCR*n*)

The XBAR_SGPCR*n* of a slave port controls several features of the slave port, including the following:

- Round-robin or fixed arbitration policy for a particular slave port
- Write protection of any slave port registers
- Parking algorithm used for a slave port

The PARK field indicates which master port this slave port parks on when no active access attempts are being made to the slave and the parking control field is set to park on a specific master. XBAR_SGPCR*n*[PARK] must only be programmed to select master ports that are actually available on the device, otherwise undefined behavior results. The low-power park feature can result in an overall power savings if the slave port is not saturated; however, an extra clock of latency results whenever any master tries to access a slave (not being accessed by another master) because it is not parked on any master.

The XBAR_SGPCR can only be accessed in supervisor mode with 32-bit accesses. After the RO (read only) bit is set in the XBAR_SGPCR, the XBAR_SGPCR and the SBAR_MPR can only be read. Attempts to write to them have no effect and results in an error.

NOTE

Some of the unused bits in the SGPCR*n* registers are writeable and readable, but they serve no function. Setting any of these bits has no effect on the operation of this module.

Addess: Base + 0x0010 (XBAR_SGPCR0) Access: R/W
Base + 0x0110 (XBAR_SGPCR1)
Base + 0x0310 (XBAR_SGPCR3)
Base + 0x0610 (XBAR_SGPCR6)
Base + 0x0710 (XBAR_SGPCR7)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	RO[1]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	ARB		0	0	PCTL		0	PARK		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[1] After this bit is set, only a hardware reset clears it.

Figure 7-3. Slave General-Purpose Control Registers (XBAR_SGPCR*n*)

Table 7-5. XBAR_SGPCR*n* Field Descriptions

Field	Description
0 RO	Read only. Used to force all of a slave port's registers to be read only. After written to 1, it can only be cleared by hardware reset. 0 All this slave port's registers can be written. 1 All this slave port's registers are read only and cannot be written (attempted writes have no effect and result in an error response).
1–21	Reserved, must be cleared.
22–23 ARB	Arbitration mode. Used to select the arbitration policy for the slave port. This field is initialized by hardware reset. 00 Fixed priority using MPR 01 Round-robin priority 10 Invalid value 11 Invalid value
24–25	Reserved, must be cleared.
26–27 PCTL	Parking control. Used to select the parking algorithm used by the slave port. This field is initialized by hardware reset. 00 When no master is making a request, the arbiter parks the slave port on the master port defined by the PARK control field. 01 POL—Park on last. When no master is making a request, the arbiter parks the slave port on the last master to own the slave port. 10 LPP—Low-power park. When no master is making a request, the arbiter parks the slave port on no master and drives all slave port outputs to a safe state. 11 Invalid value

Table 7-5. XBAR_SGPCR*n* Field Descriptions (continued)

Field	Description
28	Reserved, must be cleared.
29–31 PARK	Park. Used to determine which master port this slave port parks on when no masters are actively making requests. PCTL must be set to 00. 000 Park on master port 0 001 Park on master port 1 010 Park on master port 2 011 Park on master port 3 100 Invalid value 101 Invalid value 110 Invalid value 111 Invalid value

7.3 Functional Description

This section describes the functionality of the XBAR in more detail.

7.3.1 Overview

The main goal of the XBAR is to increase overall system performance by allowing multiple masters to communicate concurrently with multiple slaves. To maximize data throughput, it is essential to keep arbitration delays to a minimum.

This section examines data throughput from the point of view of masters and slaves, detailing when the XBAR stalls masters, or inserts bubbles on the slave side.

7.3.2 General Operation

When a master makes an access to the XBAR from an idle master state, the access is taken immediately by the XBAR. If the targeted slave port of the access is available (that is, the requesting master is currently granted ownership of the slave port), the access is immediately presented on the slave port. It is possible to make single clock (zero wait state) accesses through the XBAR by a granted master. If the targeted slave port of the access is busy or parked on a different master port, the requesting master receives wait states until the targeted slave port can service the master request. The latency in servicing the request depends on each master's priority level and the responding slave's access time.

Because the XBAR appears to be simply another slave to the master device, the master device has no indication that it owns the slave port it is targeting. While the master does not have control of the slave port it is targeting, it is wait-stated.

A master is given control of a targeted slave port only after a previous access to a different slave port has completed, regardless of its priority on the newly targeted slave port. This prevents deadlock from occurring when a master has the following conditions:

- Outstanding request to slave port A that has a long response time
- Pending access to a different slave port B
- Lower priority master also makes a request to the different slave port B.

In this case, the lower priority master is granted bus ownership of slave port B after a cycle of arbitration, assuming the higher priority master slave port A access is not terminated.

After a master has control of the slave port it is targeting, the master remains in control of that slave port until it gives up the slave port by running an IDLE cycle, leaves that slave port for its next access, or loses control of the slave port to a higher priority master with a request to the same slave port. However, because all masters run a fixed-length burst transfer to a slave port, it retains control of the slave port until that transfer sequence is completed. In round-robin arbitration mode, the current master is forced to hand off bus ownership to an alternately requesting master at the end of its current transfer sequence.

When a slave bus is idled by the XBAR, it can be parked on the master port using the PARK bits in the XBAR_SGPCR (slave general-purpose control register), or on the last master to have control of the slave port. This can avoid the initial clock of the arbitration delay if the master must arbitrate to gain control of the slave port. The slave port can also be put into low-power park mode to save power.

7.3.3 Master Ports

The XBAR terminates an access and it is not allowed to pass through the XBAR unless the master currently is granted access to the slave port to which the access is targeted. A master access is taken if the slave port to which the access decodes is either currently servicing the master or is parked on the master. In this case, the XBAR is completely transparent and the master access is immediately transmitted on the slave bus and no arbitration delays are incurred. A master access stall if the access decodes to a slave port that is busy serving another master, parked on another master or is in low-power park mode.

If the slave port is currently parked on another master or is in low-power park mode, and no other master is requesting access to the slave port, then only one clock of arbitration is incurred. If the slave port is currently serving another master of a lower priority and the master has a higher priority than all other requesting masters, then the master gains control over the slave port as soon as the data phase of the current access is completed. If the slave port is currently servicing another master of a higher priority, then the master gains control of the slave port after the other master releases control of the slave port if no other higher priority master is also waiting for the slave port.

A master access is responded to with an error if the access decodes to a location not occupied by a slave port. This is the only time the XBAR directly responds with an error response. All other error responses received by the master are the result of error responses on the slave ports being passed through the XBAR.

7.3.4 Slave Ports

The goal of the XBAR with respect to the slave ports is to keep them 100% saturated when masters are actively making requests. To do this the XBAR must not insert any bubbles onto the slave bus unless absolutely necessary.

There is only one instance when the XBAR forces a bubble onto the slave bus when a master is actively making a request. This occurs when a handoff of bus ownership occurs and there are no wait states from the slave port. A requesting master which does not own the slave port is granted access after a one clock delay.

The only other time the XBAR has control of the slave port is when no masters are making access requests to the slave port and the XBAR is forced to either park the slave port on a specific master, or place the slave port into low-power park mode. In these cases, the XBAR forces IDLE for the transfer type.

7.3.5 Priority Assignment

Each master port must be assigned a unique 2-bit priority level in fixed priority mode. If multiple master ports are assigned the same priority level within a register (XBAR_MPR) undefined behavior results.

7.3.6 Arbitration

XBAR supports two arbitration schemes; a simple fixed-priority comparison algorithm, and a round-robin fairness algorithm. The arbitration scheme is independently programmable for each slave port.

7.3.6.1 Fixed Priority Operation

When operating in fixed-priority arbitration mode, each master is assigned a unique priority level in the XBAR_MPR. If two masters both request access to a slave port, the master with the highest priority in the selected priority register gains control over the slave port.

Any time a master makes a request to a slave port, the slave port checks to see if the new requesting master's priority level is higher than that of the master that currently has control over the slave port (if any). The slave port does an arbitration check at every clock edge to ensure that the proper master (if any) has control of the slave port.

If the new requesting master's priority level is higher than that of the master that currently has control of the slave port, the higher priority master is granted control at the termination of any currently pending access, assuming the pending transfer is not part of a burst transfer.

A new requesting master must wait until the end of the fixed-length burst transfer, before it is granted control of the slave port. But if the new requesting master's priority level is lower than that of the master that currently has control of the slave port, the new requesting master is forced to wait until the master that currently has control of the slave port is finished accessing the current slave port.

7.3.6.2 Round-Robin Priority Operation

When operating in round-robin mode, each master is assigned a relative priority based on the master port number. This relative priority is compared to the port number of the last master to perform a transfer on the slave bus. The highest priority requesting master becomes the owner of the slave bus at the next transfer boundary (accounting for fixed-length burst transfers). Priority is based on how far ahead the port number of the requesting master is to the port number of the last master.

After granted access to a slave port, a master may perform as many transfers as desired to that port until another master makes a request to the same slave port. The next master in line is granted access to the slave port when the current transfer is completed, or possibly on the next clock cycle if the current master has no pending access request.

As an example of arbitration in round-robin mode, assume the three masters have ID's 0, 1, and 2. If the last master of the slave port was master 1, and masters 0 and 2 make simultaneous requests, they are serviced in the order 2 and then 0 assuming no further requests are made.

As another example, if master 1 is waiting on a response from a slow slave and has no further pending access to that slave, no other masters are requesting, and master 0 then makes a request, master 0's request is granted on the next clock (assuming that master 1's transfer is not a burst transfer), and the request information for master 0 is driven to the slave as a pending access. If master 2 were to make a request after master 0 has been granted access, but prior to master 0's access being accepted by the slave, master 0 maintains the grant on the slave port, and master 2 is delayed until the next arbitration boundary, which occurs after the transfer is complete. The round-robin pointer is reset to 0, so if master 1 has another request that occurs before master 0's transfer completes, master 1 is the granted the bus. This implies a worst case latency of *N* transfers for a system with *N* masters.

Parking may continue to be used in round-robin mode, but affects the round-robin pointer unless the parked master actually performs a transfer. Handoff to the next master in line occurs after one cycle of arbitration.

The slave port does an arbitration check at every clock edge to ensure that the proper master (if any) has control of the slave port.

A new requesting master must wait until the end of the fixed-length burst transfer, before it is granted control of the slave port. If the new requesting master's priority level is lower than that of the master that currently has control of the slave port, the new requesting master is forced to wait until the master that currently has control of the slave port completes its access.

7.3.6.2.1 Parking

If no master is currently requesting the slave port, the slave port is parked. The slave port parks in one of three places, indicated by the value of the PCTL field in the XBAR_SGPCR.

- If park-on-specific master mode is selected, the slave port parks on the master designated by the PARK field. When the master accesses the slave port again, a one clock arbitration penalty is incurred only for an access request made by another master port to the slave port. No other arbitration penalties are incurred. All other masters pay a one clock penalty.
- If park-on-last (POL) mode is selected, then the slave port parks on the last master to access it, passing that master's signals through to the slave bus. When the master accesses the slave port again, no other arbitration penalties are incurred except that a one clock arbitration penalty is incurred for each access request to the slave port made by another master port. All other masters pay a one clock penalty.
- If the low-power-park (LPP) mode is selected, then the slave port enters low-power park mode. It is not under control by any master and does not transmit any master signals to the slave bus. All slave bus activity halts because all slave bus signals are not toggling. This saves power if the slave port is not used for some time. However, when a master does make a request to a slave port parked in low-power-park, a one clock arbitration delay is incurred to get ownership of the slave port.

Chapter 8
Error Correction Status Module (ECSM)

8.1 Introduction

The device includes error-correcting code (ECC) implementations to improve the quality and reliability of internal SRAM and internal flash memories. The error correction status module (ECSM) allows the application to collect information on memory errors reported by ECC and/or generic access error information.

8.1.1 Overview

The ECSM provides a set of registers that configure and report ECC errors for the device including accesses to SRAM and flash memory. The application can configure the device for the types of memory errors to report, and then query a set of read-only status and information registers to identify any errors that have occurred.

There are two types of ECC errors: correctable and non-correctable. A correctable ECC error is generated when only one bit is incorrect in a 64-bit doubleword. In this case, it is corrected automatically by hardware, and no flags or other indicators are set by the error that occurred. A non-correctable ECC error is generated when two bits in a 64-bit doubleword are incorrect. Non-correctable ECC errors cause an interrupt, and if enabled, additional error details are available in the ECSM.

Error correction is implemented on 64 data bits at a time, using eight ECC bits for every 64-bit doubleword of data. The ECC is checked on read accesses, and calculated on write accesses using the following sequence:

1. Read the 64 bits that contain the desired byte / halfword / word or doubleword in memory, and check the ECC.
2. If the access is a write, then:
   a) Merge the new byte / halfword / word into the 64 data bits and calculate a new ECC value.
   b) Write the 64 bits and the new ECC to SRAM.

To use the ECC for SRAM, write to SRAM memory before you enable the ECC. Refer to Section 8.3, “Initialization and Application Information.”

8.1.2 Features

The ECSM includes these features:

- Configurable for reporting non-correctable errors
- Registers for capturing ECC information for RAM and flash access errors

8.2 Memory Map and Register Definition

Table 8-1 is the memory map for the ECSM registers.

Table 8-1. ECSM Memory Map

Address	Register Name	Register Description	Bits
Base (0xFFF4_0000) + 0x0016	ECSM_SWTCR	Software watchdog timer control register [1]	16
Base + (0x0018–0x001A)	—	Reserved	—
Base + 0x001B	ECSM_SWTSR	Software watchdog timer service register [1]	8
Base + (0x001C–0x001E)	—	Reserved	—
Base + 0x001F	ECSM_SWTIR	Software watchdog timer interrupt register [1]	8
Base + (0x0020–0x0023)	—	Reserved	—
Base + (0x0024–0x0027)	FBOMCR	FEC Burst Optimization Master Control Register	32
Base + (0x0028–0x0042)	—	Reserved	—
Base + 0x0043	ECSM_ECR	ECC configuration register	8
Base + (0x0044–0x0046)	—	Reserved	—
Base + 0x0047	ECSM_ESR	ECC status register	8
Base + (0x0048–0x0049)	—	Reserved	—
Base + 0x004A	ECSM_EEGR	ECC error generation register	16
Base + (0x004B–0x004F)	—	Reserved	—
Base + 0x0050	ECSM_FEAR	Flash ECC address register	32
Base + (0x0054–0x0055)	—	Reserved	—
Base + 0x0056	ECSM_FEMR	Flash ECC master register	8
Base + 0x0057	ECSM_FEAT	Flash ECC attribute register	8
Base + 0x0058	ECSM_FEDRH	Flash ECC data high register	32
Base + 0x005C	ECSM_FEDRL	Flash ECC data low register	32
Base + 0x0060	ECSM_REAR	RAM ECC address register	32
Base + (0x0064–0x0065)	—	Reserved	—
Base + 0x0066	ECSM_REMR	RAM ECC master register	8
Base + 0x0067	ECSM_REAT	RAM ECC attributes register	8
Base + 0x0068	ECSM_REDRH	RAM ECC data high register	32
Base + 0x006C	ECSM_REDRL	RAM ECC data low register	32
Base + (0x0070–0x007F)	—	Reserved	—

[1] These registers control and configure a software watchdog timer, and are included as part of a standard Freescale ECSM module. The e200z6 core also provides this functionality and is the preferred method for watchdog implementation. Refer to Section 8.2.1.1, “Software Watchdog Timer Control, Service, and Interrupt Registers (ECSM_SWTCR, ECSM_SWTSR, and ECSM_SWTIR).”

8.2.1 Register Descriptions

Attempted accesses to reserved addresses result in an error termination, while attempted writes to read-only registers are ignored and do not terminate with an error. Unless noted otherwise, writes to the programming model must match the size of the register; for example, an *n*-bit register only supports *n*-bit writes, etc. Attempted writes of a different size than the register width produce an error termination of the bus cycle and no change to the targeted register.

8.2.1.1 Software Watchdog Timer Control, Service, and Interrupt Registers (ECSM_SWTCR, ECSM_SWTSR, and ECSM_SWTIR)

These registers provide control and configuration for a software watchdog timer, and are included as part of a standard Freescale ECSM module incorporated in the device. The e200z6 core also provides this functionality and is the preferred method for watchdog implementation. To optimize code portability to other Power Architecture-based products in the MPC5500 family, use the e200z6 watchdog functions instead of the registers in the ECSM.

NOTE

Do not change the reset values in the ECSM watchdog registers. Any change to the reset values can cause an unintentional ECSM_SWTIR_SWTIC interrupt.

8.2.1.2 ECC Registers

There are a number of program-visible registers for the sole purpose of reporting and logging of memory failures. These registers include the following:

- ECC configuration register (ECSM_ECR)
- ECC status register (ECSM_ESR)
- ECC error generation register (EEGR)
- Flash ECC address register (ECSM_FEAR)
- Flash ECC master number register (ECSM_FEMR)
- Flash ECC attributes register (ECSM_FEAT)
- Flash ECC data register (ECSM_FEDR)
- RAM ECC address register (ECSM_REAR)
- RAM ECC master number register (ECSM_REMR)
- RAM ECC attributes register (ECSM_REAT)
- RAM ECC data register (ECSM_REDR)

The details of each ECC register are in the subsequent sections.

8.2.1.3 ECC Configuration Register (ECSM_ECR)

ECSM_ECR is an 8-bit control register that enables or disables ECC error reporting during RAM and flash accesses. In addition to the interrupt generation, the ECSM captures specific information (memory address, attributes and data, bus master number, etc.) that is useful for failure analysis.

The ECC reporting logic can detect non-correctable memory errors. When a non-correctable error terminates the current access to the flash memory or RAM, an error condition is generated. In many cases, the error termination is reported directly by the initiating bus master.

Base (0xFFF4_0000) + 0x0043 Access: Read/Write

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	ERNCR	EFNCR
W								
Reset	0	0	0	0	0	0	0	0

Figure 8-1. ECC Configuration Register (ECSM_ECR)

The following table describes the fields in the error configuration register:

Table 8-2. ECSM_ECR Field Definitions

Field	Description
0–5	Reserved.
6 ERNCR	Enable RAM non-correctable reporting. The occurrence of a non-correctable multi-bit RAM error generates a ECSM ECC interrupt request by the asserting the ECSM_ESR[RNCE]. The faulting address, attributes and data are also captured in the REAR, REMR, REAT and REDR registers. 0 Reporting of non-correctable RAM errors is disabled. 1 Reporting of non-correctable RAM errors is enabled.
7 EFNCR	Enable flash non-correctable reporting. The occurrence of a non-correctable multi-bit flash error generates a ECSM ECC interrupt request as signalled by the assertion of ECSM_ESR[FNCE]. The faulting address, attributes and data are also captured in the FEAR, FEMR, FEAT and FEDR registers. 0 Reporting of non-correctable flash errors is disabled. 1 Reporting of non-correctable flash errors is enabled.

8.2.1.4 ECC Status Register (ECSM_ESR)

The ECC status register (ECSM_ESR) is an 8-bit control register that defines the types of ECC events detected. The ESR indicates the last, correctly-enabled memory event detected. The ECSM ECC interrupt request is generated as defined by the boolean equation:

```
ECSM_ECC_IRQ
    = ECSM_ECR[ERNCR] & ECSM_ESR[RNCE]      // ram,   noncorrectable error
    | ECSM_ECR[EFNCR] & ECSM_ESR[FNCE]      // flash, noncorrectable error
```

where the combination of the following criteria generates the interrupt request:

- Correctly-enabled category in the ECSM_ECR; and
- Condition in the ECSM_ESR detected.

The ECSM allows a maximum of one bit of the ECSM_ESR to assert at any given time. This preserves the association between the ECSM_ESR and the corresponding address and attribute registers, which are loaded on each occurrence of an correctly-enabled ECC event. If there is a pending ECC interrupt and another correctly-enabled ECC event occurs, the ECSM hardware automatically performs the ECSM_ESR reporting by clearing the previous data and loading the new state, which ensures that only a single flag is asserted.

To maintain the coherent software view of the reported event, use the following sequence in the ECSM error interrupt service routine:

1. Read the ECSM_ESR and save it.
2. Read and save all the address and attribute reporting registers.
3. Re-read the ECSM_ESR and verify the current contents matches the original contents. If the two values are different, return to step 1 and repeat this sequence.
4. When the values are identical, write a 1 to the asserted ECSM_ESR flag to negate the interrupt request.

If multiple status flags are detected simultaneously, the ECSM records the higher priority RAM non-correctable error (RNCE) events before flash non-correctable error (FNCE) events.

Base + 0x0047 Access: Read/Write to clear

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	RNCE	FNCE
W							w1c	w1c
Reset	0	0	0	0	0	0	0	0

Figure 8-2. ECC Status Register (ECSM_ESR)

Table 8-3. ECSM_ESR Field Definitions

Field	Description
0–5	Reserved.
6 RNCE	RAM non-correctable error. A non-correctable RAM error 0ccurred. generates an ECSM ECC interrupt request. The faulting address, attributes and data are also captured in the REAR, REMR, REAT and REDR registers. To clear this interrupt flag, write a 1 to this bit. Writing a 0 has no effect. 0 No reportable non-correctable RAM error has been detected. 1 A reportable non-correctable RAM error has been detected.
7 FNCE	Flash non-correctable error. The occurrence of a correctly-enabled non-correctable flash error generates an ECSM ECC interrupt request. The faulting address, attributes and data are also captured in the FEAR, FEMR, FEAT and FEDR registers. To clear this interrupt flag, write a 1 to this bit. Writing a 0 has no effect. 0 No reportable non-correctable flash error has been detected. 1 A reportable non-correctable flash error has been detected.

8.2.1.5 ECC Error Generation Register (ECSM_EEGR)

The ECSM_EEGR is a 16-bit control register used to generate double-bit data errors in internal SRAM. This allows you to test the software service routines for memory error logging.By generating errors during

data write cycles, subsequent reads of the corrupt address locations generate ECC events, such as double-bit noncorrectable errors that are terminated with an error response.

If an attempt to force a non-correctable error (by asserting ECSM_EEGR[FRCNCI] or ECSM_EEGR[FRC1NCI]) and the ECSM_EEGR[ERRBIT] equals 64, then no data error is generated.

NOTE

Only values {0,0}, {1,0} and {0,1} are allowed for the two control bit enables {FRCNCI, FR1NCI}. The value {1,1} causes undefined results.

Base + 0x004A — Access: Read/Write

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	FRC NCI	FR1 NCI	0	ERRBIT[0:6]						
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 8-3. ECC Error Generation (ECSM_EEGR) Register

Table 8-4. ECSM_EEGR Field Definitions

Field	Description
0–5	Reserved.
6 FRCNCI	Force internal SRAM continuous noncorrectable data errors. 0 No internal SRAM continuous 2-bit data errors are generated. 1 2-bit data errors in the internal SRAM are continuously generated. The assertion of this bit forces the internal SRAM controller to create 2-bit data errors, as defined by the bit position specified in ERRBIT[0:6] and the overall odd parity bit, continuously on every write operation. The normal ECC generation takes place in the RAM controller, but then the polarity of the bit position defined by ERRBIT and the overall odd parity bit are inverted to introduce a 2-bit ECC error in the RAM.
7 FR1NCI	Force internal SRAM one noncorrectable data errors. 0 No internal SRAM single 2-bit data errors are generated. 1 One 2-bit data error in internal SRAM is generated. The assertion of this bit forces the internal SRAM controller to create one 2-bit data error, as defined by the bit position specified in ERRBIT[0:6] and the overall odd parity bit, on the first write operation after this bit is set. The normal ECC generation takes place in the internal SRAM controller, but then the polarity of the bit position defined by ERRBIT and the overall odd parity bit are inverted to introduce a 2-bit ECC error in the RAM. After this bit has been enabled to generate a single 2-bit error, it must be cleared before being set again to properly re-enable the error generation logic.

Table 8-4. ECSM_EEGR Field Definitions (continued)

Field	Description
8	Reserved.
9–15 ERRBIT	Error bit position. Defines the bit position which is complemented to create the data error on the write operation. The bit specified by this field plus the odd parity bit of the ECC code are inverted. The internal SRAM controller follows a vector bit ordering scheme where LSB=0. Errors in the ECC syndrome bits can be generated by setting this field to a value greater than the internal SRAM width. The following association between the ERRBIT field and the corrupted memory bit is defined: if ERRBIT = 0, then RAM[0] is inverted if ERRBIT = 1, then RAM[1] is inverted ... if ERRBIT = 63, then RAM[63] is inverted if ERRBIT = 64, then ECC Parity[0] is inverted if ERRBIT = 65, then ECC Parity[1] is inverted ... if ERRBIT = 71, then ECC Parity[7] is inverted For ERRBIT values greater than 71, no bit position is inverted.

8.2.1.6 Flash ECC Address Register (ECSM_FEAR)

The ECSM_FEAR is a 32-bit register for capturing the address of the last, correctly-enabled ECC event in the flash memory. Depending on the state of the ECSM_ECR, an ECC event in the flash loads the address, attributes and data of the access into the ECSM_FEAR, ECSM_FEMR, ECSM_FEAT, and ECSM_FEDR registers, and asserts the F1BC or FNCE flag in ECSM_ESR.

The address that is captured in ECSM_FEAR is the flash page address as seen on the system bus. Refer to Section 13.3.2.7, “Address Register (FLASH_AR)” to retrieve the doubleword address.

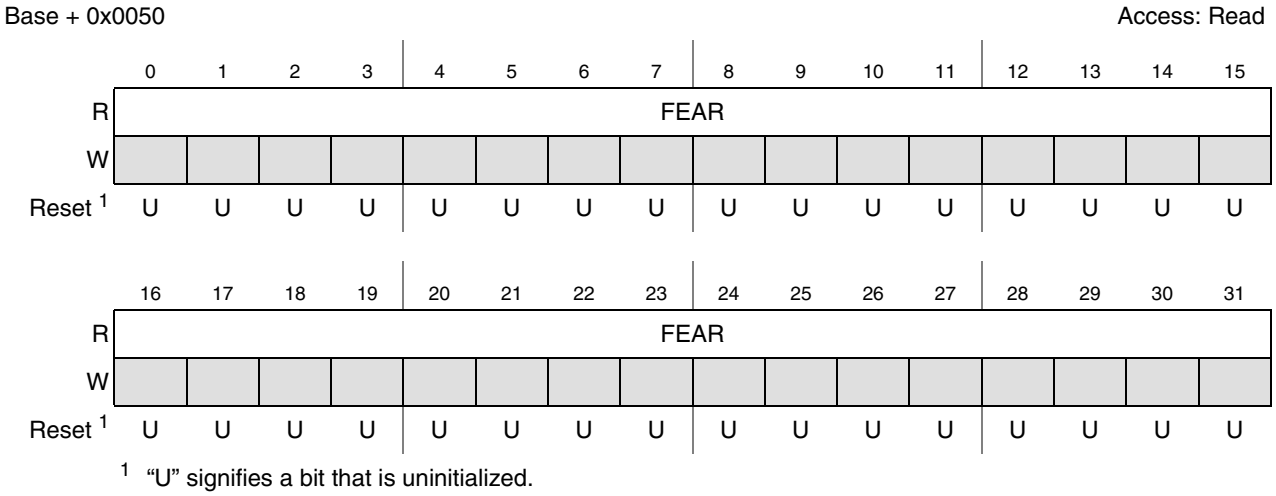


Figure 8-4. Flash ECC Address Register (ECSM_FEAR)

Table 8-5. ECSM_FEAR Field Descriptions

Field	Description
0–31 FEAR [0:31]	Flash ECC address. Contains the faulting access address of the last, correctly-enabled flash ECC event.

8.2.1.7 Flash ECC Master Number Register (ECSM_FEMR)

The FEMR is an 8-bit register for capturing the XBAR bus master number of the last, correctly-enabled ECC event in the flash memory. Depending on the state of the ECSM_ECR, an ECC event in the flash loads the address, attributes and data of the access into the ECSM_FEAR, ECSM_FEMR, ECSM_FEAT and ECSM_FEDR registers, and asserts the FNCE flag in the ECSM_ESR.

ECSM Base + 0x0056 Access: Read

	0	1	2	3	4	5	6	7
R	0	0	0	0	FEMR			
W								
Reset [1]	0	0	0	0	U	U	U	U

[1] "U" signifies a bit that is uninitialized.

Figure 8-5. Flash ECC Master Number Register (ECSM_FEMR)

Table 8-6. ECSM_FEMR Field Descriptions

Field	Description
0–3	Reserved.
4–7 FEMR [0:3]	Flash ECC master number. Contains the XBAR bus master number of the faulting access of the last, correctly-enabled flash ECC event. The reset value of this field is undefined.

8.2.1.8 Flash ECC Attributes Register (ECSM_FEAT)

The ECSM_FEAT is an 8-bit register for capturing the XBAR bus master attributes of the last, correctly-enabled ECC event in the flash memory. Depending on the state of the ECSM_ECR register, an ECC event in the flash loads the address, attributes and data of the access into the ECSM_FEAR, ECSM_FEMR, ECSM_FEAT, and ECSM_FEDR registers, and asserts the FNCE flag in ECSM_ESR.

Base + 0x0057 Access: Read

	0	1	2	3	4	5	6	7
R	WRITE	SIZE			PROT0	PROT1	PROT2	PROT3
W								
Reset [1]	U	U	U	U	U	U	U	U

[1] "U" signifies a bit that is uninitialized.

Figure 8-6. Flash ECC Attributes Register (ECSM_FEAT)

Table 8-7. ECSM_FEAT Field Descriptions

Field	Description
0 WRITE	Write. The reset value of this field is undefined. 0 System bus read access 1 System bus write access
1–3 SIZE [0:2]	Size. The reset value of this field is undefined. 000 8-bit System bus access 001 16-bit System bus access 010 32-bit System bus access 011 64-bit System bus access 1xx Reserved
4 PROT0	Protection: cache. The reset value of this field is undefined. 0 Non-cacheable 1 Cacheable
5 PROT1	Protection: buffer. The reset value of this field is undefined. 0 Non-bufferable 1 Bufferable
6 PROT2	Protection: mode. The reset value of this field is undefined. 0 User mode 1 Supervisor mode
7 PROT3	Protection: type. The reset value of this field is undefined. 0 I-Fetch 1 Data

8.2.1.9 Flash ECC Data High Register (ECSM_FEDRH)

The ECSM_FEDRH and ECSM_FEDRL are 32-bit registers for capturing the data of the last, correctly-enabled ECC event in flash memory. Depending on the state of the ECSM_ECR, an ECC event in the flash loads the address, attributes and data of the access into the ECSM_FEAR, ECSM_FEMR, ECSM_FEAT and ECSM_FEDR registers, and asserts the FNCE flag in ECSM_ESR.

The data captured on a multi-bit non-correctable ECC error is undefined.

Base + 0x0058 Access: Read

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	FEDH															
W																
Reset [1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	FEDH															
W																
Reset [1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

[1] "U" signifies a bit that is uninitialized.

Figure 8-7. Flash ECC Data High Register (ECSM_FEDRH)

Table 8-8. ECSM_FEDRH Field Descriptions

Field	Description
0–31 FEDH [0:31]	Flash ECC data. Contains the data associated with the faulting access of the last, correctly-enabled flash ECC event. The register contains the data value taken directly from the data bus. The reset value of this field is undefined.

8.2.1.10 Flash ECC Data Low Registers (ECSM_FEDRL)

The ECSM_FEDRH and ECSM_FEDRL are 32-bit registers for capturing the data of the last, correctly-enabled ECC event in the flash memory. Depending on the state of the ECSM_ECR, an ECC event in the flash loads the address, attributes and data of the access into the ECSM_FEAR, ECSM_FEMR, ECSM_FEAT and ECSM_FEDR registers, and asserts the FNCE flag in ECSM_ESR.

The data captured on a multi-bit non-correctable ECC error is undefined.

Base + 0x005C Access: Read

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	FEDL															
W																
Reset [1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	FEDL															
W																
Reset [1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

[1] "U" signifies a bit that is uninitialized.

Figure 8-8. Flash ECC Data Low Register (ECSM_FEDRL)

Table 8-9. ECSM_FEDRL Field Descriptions

Field	Description
0–31 FEDL [0:31]	Flash ECC data. Contains the data associated with the faulting access of the last, correctly-enabled flash ECC event. The register contains the data value taken directly from the data bus. The reset value of this field is undefined.

8.2.1.11 RAM ECC Address Register (ECSM_REAR)

The ECSM_REAR is a 32-bit register for capturing the address of the last, correctly-enabled ECC event in the RAM memory. Depending on the state of the ECSM_ECR, an ECC event in the RAM loads the address, attributes and data of the access into the ECSM_REAR, ECSM_REMR, ECSM_REAT and ECSM_REDR registers, and asserts the RNCE flag in ECSM_ESR.

Base + 0x0060 Access: Read

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	REAR															
W																
Reset [1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	REAR															
W																
Reset [1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

[1] "U" signifies a bit that is uninitialized.

Figure 8-9. RAM ECC Address Register (ECSM_REAR)

Table 8-10. ECSM_REAR Field Descriptions

Field	Description
0–31 REAR [0:31]	RAM ECC address. Contains the faulting access address of the last, correctly-enabled RAM ECC event. The reset value of this field is undefined.

8.2.1.12 RAM ECC Master Number Register (ECSM_REMR)

The REMR is an 8-bit register for capturing the XBAR bus master number of the last, correctly-enabled ECC event in the RAM memory. Depending on the state of the ECSM_ECR, an ECC event in the RAM loads the address, attributes and data of the access into the ECSM_REAR, ECSM_REMR, ECSM_REAT and ECSM_REDR registers, and asserts the RNCE flag in ECSM_ESR.

Base + 0x0066 Access: Read

	0	1	2	3	4	5	6	7
R	0	0	0	0	REMR			
W								
Reset [1]	0	0	0	0	U	U	U	U

[1] "U" signifies a bit that is uninitialized.

Figure 8-10. RAM ECC Master Number Register (ECSM_REMR)

Table 8-11. ECSM_REMR Field Descriptions

Field	Description
0–3	Reserved.
4–7 REMR [0:3]	RAM ECC master number. Contains the XBAR bus master number of the faulting access of the last, correctly-enabled RAM ECC event. The reset value of this field is undefined.

8.2.1.13 RAM ECC Attributes Register (ECSM_REAT)

The ECSM_REAT is an 8-bit register for capturing the XBAR bus master attributes of the last, correctly-enabled ECC event in the RAM memory. Depending on the state of the ECSM_ECR, an ECC event in the RAM loads the address, attributes and data of the access into the ECSM_REAR, ECSM_REMR, ECSM_REAT and ECSM_REDR registers, and asserts the RNCE flag in ECSM_ESR.

Base + 0x0067 Access: Read

	0	1	2	3	4	5	6	7
R	WRITE	SIZE			PROT0	PROT1	PROT2	PROT3
W								
Reset [1]	U	U	U	U	U	U	U	U

[1] "U" signifies a bit that is uninitialized.

Figure 8-11. RAM ECC Attributes Register (ECSM_REAT)

Table 8-12. ECSM_REAT Field Descriptions

Field	Description
0 WRITE	Write. The reset value of this field is undefined. 0 System bus read access 1 System bus write access
1–3 SIZE [0:2]	Size. The reset value of this field is undefined. 000 8-bit system bus access 001 16-bit system bus access 010 32-bit system bus access 011 64-bit system bus access 1xx Reserved
4 PROT0	Protection: cache. The reset value of this field is undefined. 0 Non-cacheable 1 Cacheable
5 PROT1	Protection: buffer. The reset value of this field is undefined. 0 Non-bufferable 1 Bufferable
6 PROT2	Protection: mode. The reset value of this field is undefined. 0 User mode 1 Supervisor mode
7 PROT3	Protection: type. The reset value of this field is undefined. 0 I-Fetch 1 Data

8.2.1.14 RAM ECC Data High Register (ECSM_REDRH)

The ECSM_REDRH and ECSM_REDRL are 32-bit registers for capturing the data of the last, correctly-enabled ECC event in the RAM memory. Depending on the state of the ECSM_ECR, an ECC event in the RAM loads the address, attributes and data of the access into the ECSM_REAR, ECSM_REMR, ECSM_REAT, ECSM_REDRH and ECSM_REDRL registers, and asserts the RFNCE flag in ECSM_ESR.

The data captured on a multi-bit non-correctable ECC error is undefined.

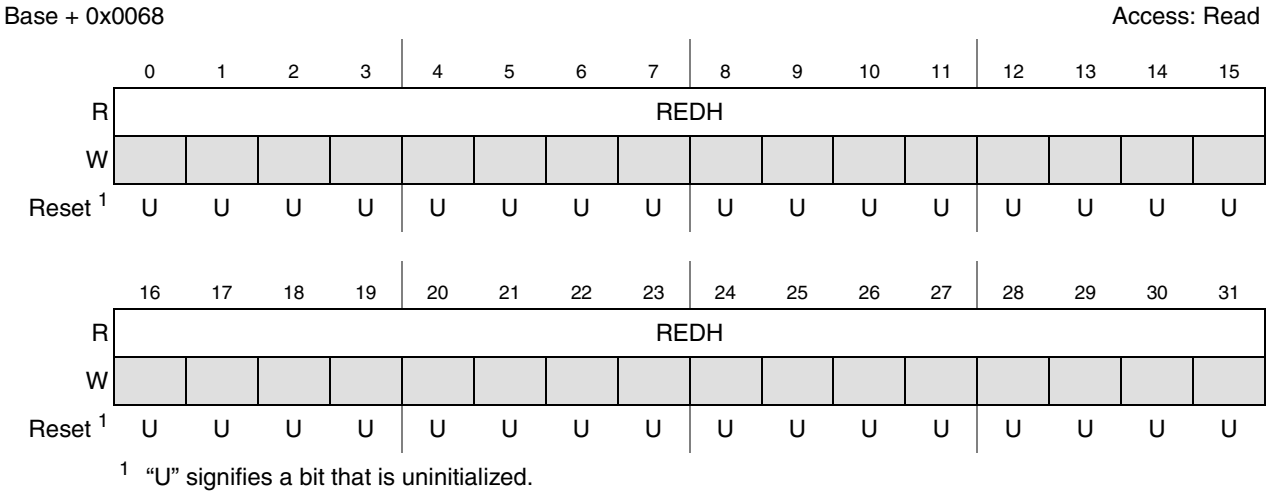


Figure 8-12. RAM ECC Data High Register (ECSM_REDRH)

Table 8-13. ECSM_REDRH Field Descriptions

Field	Description
0–31 REDH [0:31]	RAM ECC data. Contains the data of the faulting access of the last, correctly-enabled RAM ECC event. The register contains the data value taken directly from the data bus. The reset value of this field is undefined.

8.2.1.15 RAM ECC Data Low Registers (ECSM_REDRL)

The ECSM_REDRH and ECSM_REDRL are 32-bit registers for capturing the data for the last, correctly-enabled ECC event in RAM. Depending on the state of the ECSM_ECR, an ECC event in the RAM loads the address, attributes and data of the access to the following registers:

- ECSM_REAR
- ECSM_REMR
- ECSM_REAT
- ECSM_REDRH
- ECSM_REDRL

and asserts the RFNCE flag in ECSM_ESR. The data captured on a multi-bit non-correctable ECC error is undefined.

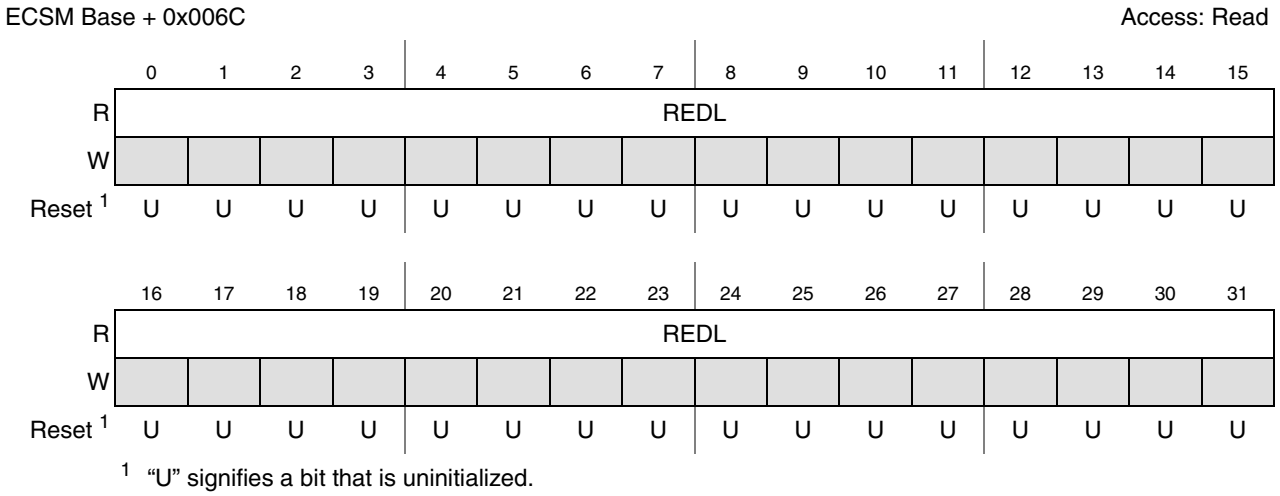


Figure 8-13. RAM ECC Data Low Register (ECSM_REDRL)

The following table describes the RAM ECC data field in the

Table 8-14. ECSM_REDRL Field Descriptions

Field	Description
0–31 REDL [0:31]	RAM ECC data. Contains the data associated with the faulting access of the last, correctly-enabled RAM ECC event. The register contains the data value taken directly from the data bus. The reset value of this field is undefined.

8.3 Initialization and Application Information

The Error Correction Code (ECC) is used to verify the contents of the internal SRAM and flash memories. This is done by generating ECC check bits. Typically ECC check bits are calculated on writes and then used on reads to detect and correct errors.

There are eight ECC check bits for each 64-bit data doubleword.

After Power on Reset (POR), the contents of internal SRAM is random and the corresponding ECC check bits are unknown. To prevent generating ECC errors during reads, an initialization routine must perform 64-bit writes to all SRAM locations. Because the flash module is non-volatile, the ECC check bits are calculated and stored when the flash is programmed.

Transparent to the application, the ECC uses the check bits to automatically correct single-bit memory errors. Multi-bit memory errors are not correctable. If the ECC detects a multi-bit error, an exception is generated. The type of exception generated by a multi-bit error depends on the settings of the EE and ME in the Machine State Register (MSR), as shown in Table 8-15. When error reporting is enabled, as long as its priority is 0, an interrupt request is generated to the interrupt controller (INTC) even though the INTC request is not serviced.

Table 8-15. MSR[EE] and MSR[ME] Bit Settings

Field	Description
EE	External interrupt enable. 0 External input interrupts disabled. 1 External interrupts enabled.
ME	Machine check enable. 0 Machine check interrupts disabled. Enters machine check. 1 Machine interrupts enabled.

A non-correctable data ECC error executes one of the following actions, regardless of whether non-correctable reporting is enabled:

Table 8-16. Non-correctable Data ECC States

MSR[EE]	MSR[ME]	Access Type	Result
0	0	Instruction or data	Enters checkstop state. A reset is required to resume processing.
0	1	Instruction or data	Machine check interrupt (IVOR1).
1	X	Data	Data storage interrupt (IVOR2). External interrupt must be enabled. Machine check can be enabled or disabled.
1	X	Instruction	Instruction storage interrupt (IVOR3).

When the device is in the checkstop state, processing is suspended and cannot resume without a reset. When a debug request is presented to the core while it is in the checkstop state, the core temporarily exits the checkstop state and enters debug mode. When debug mode exits, the core re-enters the checkstop state.

If the external interrupt bit in the MSR is enabled, data or instruction storage interrupts are reported when the ECC errors are a result of CPU accesses, regardless of whether non-correctable reporting is enabled. ECC errors generated by other masters (eDMA, etc.) do not generate data or instruction storage exceptions, and the ECSM is used to report these errors. You must initialize the ECSM to enable non-correctable reporting with interrupt generation to detect and report ECC interrupts from the ECSM.

Error reporting details can be independently enabled for flash memory and SRAM. To enable non-correctable error reporting and save the error details for:

- SRAM, set the ERNCR bit in the ECSM Error Configuration Register (ECSM_ECR).
- Flash, set the EFNCR bit in ECSM_ECR.

When these bits are set and a non-correctable ECC error occurs, error information is recorded in other ECSM registers and an interrupt request is generated on vector 9 of the interrupt controller (INTC).

- If the error was caused by a CPU data access, a data storage exception (IVOR2) is generated.
- If the error was caused by a CPU instruction access, an instruction storage exception (IVOR3) is generated.
- If vector 9 of INTC is enabled, an external exception (IVOR4) is generated.

To prevent generating an ECSM interrupt in response to a non-correctable error:

- Enable non-correctable reporting in the ECSM.
- Ensure the external interrupt is disabled.
- Ensure that the INTC_PSR[PRI] value for the ECC error interrupt request is 0.

To use the detailed data or instruction storage exception information, design an exception handler that can determine:

- The destination that asserted the error, indicated by the value of the ESR[XTE] bit.
- The address of the corrupted instruction for an instruction storage exception (SRR0).
- The address where the error occurred for a data storage exception, indicated in the data exception address register (DEAR).

Chapter 9
Enhanced Direct Memory Access (eDMA)

9.1 Introduction

This chapter describes the enhanced Direct Memory Access (eDMA) controller, a second-generation module capable of performing complex data transfers with minimal intervention from a host processor.

The enhanced direct memory access (eDMA) controller hardware microarchitecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with SRAM-based local memory containing the transfer control descriptors (TCD) for the channels.

Figure 9-1 is a block diagram of the eDMA module.

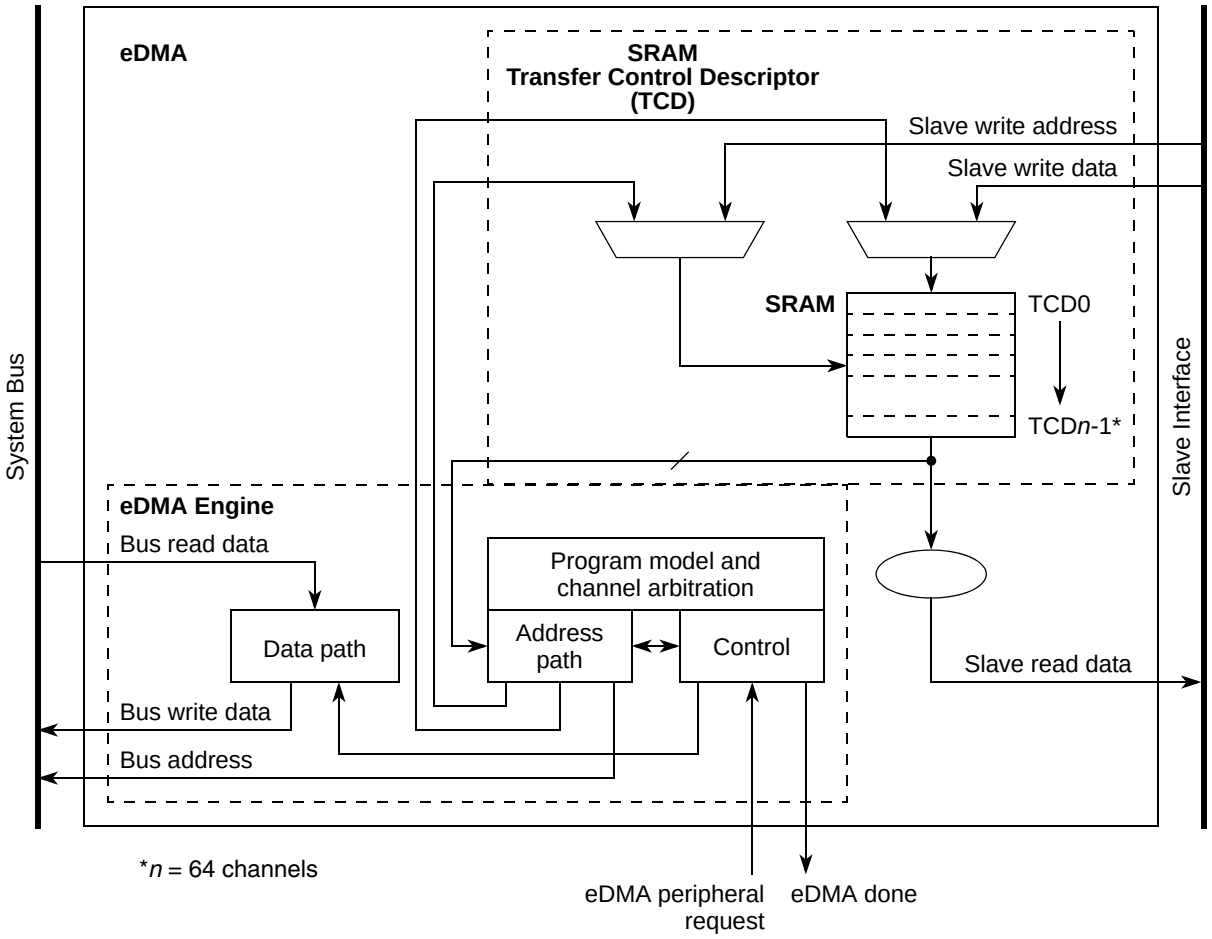


Figure 9-1. eDMA Block Diagram

9.1.1 Features

The eDMA is a highly-programmable data transfer engine, which has been optimized to minimize the required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known, and is *not* defined within the data packet itself. The eDMA module features:

- All data movement via dual-address transfers: read from source, write to destination

  Programmable source, destination addresses, transfer size, plus support for enhanced addressing modes
- 64-channel implementation performs complex data transfers with minimal intervention from a host processor
  - 32 bytes of data registers, used as temporary storage to support burst transfers (refer to SSIZE bit)
  - Connections to the crossbar switch for bus mastering the data movement

- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
  - 32-byte TCD per channel stored in local memory
  - An inner data transfer loop defined by a minor byte transfer count
  - An outer data transfer loop defined by a major iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continual transfers
  - Peripheral-paced hardware requests (one per channel)

NOTE

For all three methods, one activation per execution of the minor loop is required.

- Support for fixed-priority and round-robin channel arbitration
- Support for complex data structures
- Support to cancel transfers via software
- Channel completion reported via optional interrupt requests
  - One interrupt per channel, optionally asserted at completion of major iteration count
  - Error terminations are enabled per channel, and logically summed together to form two error interrupts
- Support for scatter/gather DMA processing
- Any channel can be programmed so that it can be suspended by a higher priority channel's activation, before completion of a minor loop

Throughout this chapter, *n* is used to reference the channel number. Additionally, data sizes are defined as byte (8-bit), halfword (16-bit), word (32-bit) and doubleword (64-bit).

9.1.2 Modes of Operation

9.1.2.1 Normal Mode

In normal mode, the eDMA is used to transfer data between a source and a destination. The source and destination can be a memory block or an I/O block capable of operation with the eDMA.

9.1.2.2 Debug Mode

If enabled by EDMA_CR[EDBG] and the CPU enters debug mode, the eDMA does not grant a service request when the debug input signal is asserted. If the signal asserts during a data block transfer as described by a minor loop in the current active channel's TCD, the eDMA continues the operation until the minor loop completes.

9.2 Memory Map and Register Definition

9.2.1 Memory Map

The eDMA programming model is partitioned into two regions:

Region 1 defines control registers; region 2 defines the local transfer control for the descriptor memory.

Some registers are implemented as two 32-bit registers, and include an “H” and “L” suffix, signaling the “high” and “low” portions of the control function. Table 9-1 is a 32-bit view of the eDMA memory map.

Table 9-1. eDMA 32-bit Memory Map

Address	Register Name	Register Description	Bits
Base (0xFFF4_4000)	EDMA_CR	eDMA control register	32
Base + 0x0004	EDMA_ESR	eDMA error status register	32
Base + 0x0008	EDMA_ERQRH	eDMA enable request high register	32
Base + 0x000C	EDMA_ERQRL	eDMA enable request low register	32
Base + 0x0010	EDMA_EEIRH	eDMA enable error interrupt high register	32
Base + 0x0014	EDMA_EEIRL	eDMA enable error interrupt low register	32
Base + 0x0018	EDMA_SERQR	eDMA set enable request register	8
Base + 0x0019	EDMA_CERQR	eDMA clear enable request register	8
Base + 0x001A	EDMA_SEEIR	eDMA set enable error interrupt register	8
Base + 0x001B	EDMA_CEEIR	eDMA clear enable error interrupt register	8
Base + 0x001C	EDMA_CIRQR	eDMA clear interrupt request register	8
Base + 0x001D	EDMA_CER	eDMA clear error register	8
Base + 0x001E	EDMA_SSBR	eDMA set start bit register	8
Base + 0x001F	EDMA_CDSBR	eDMA clear done status bit register	8
Base + 0x0020	EDMA_IRQRH	eDMA interrupt request high register	32
Base + 0x0024	EDMA_IRQRL	eDMA interrupt request low register	32
Base + 0x0028	EDMA_ERH	eDMA error high register	32
Base + 0x002C	EDMA_ERL	eDMA error low register	32
Base + 0x0030	EDMA_HRSH	eDMA hardware request status high	32
Base + 0x0034–0x00FF	—	Reserved	—
Base + 0x0100	EDMA_CPR0	eDMA channel 0 priority register	8
Base + 0x0101	EDMA_CPR1	eDMA channel 1 priority register	8
Base + 0x0102	EDMA_CPR2	eDMA channel 2 priority register	8
Base + 0x0103	EDMA_CPR3	eDMA channel 3 priority register	8
Base + 0x0104	EDMA_CPR4	eDMA channel 4 priority register	8

Table 9-1. eDMA 32-bit Memory Map (continued)

Address	Register Name	Register Description	Bits
Base + 0x0105	EDMA_CPR5	eDMA channel 5 priority register	8
Base + 0x0106	EDMA_CPR6	eDMA channel 6 priority register	8
Base + 0x0107	EDMA_CPR7	eDMA channel 7 priority register	8
Base + 0x0108	EDMA_CPR8	eDMA channel 8 priority register	8
Base + 0x0109	EDMA_CPR9	eDMA channel 9 priority register	8
Base + 0x010A	EDMA_CPR10	eDMA channel 10 priority register	8
Base + 0x010B	EDMA_CPR11	eDMA channel 11 priority register	8
Base + 0x010C	EDMA_CPR12	eDMA channel 12 priority register	8
Base + 0x010D	EDMA_CPR13	eDMA channel 13 priority register	8
Base + 0x010E	EDMA_CPR14	eDMA channel 14 priority register	8
Base + 0x010F	EDMA_CPR15	eDMA channel 15 priority register	8
Base + 0x0110	EDMA_CPR16	eDMA channel 16 priority register	8
Base + 0x0111	EDMA_CPR17	eDMA channel 17 priority register	8
Base + 0x0112	EDMA_CPR18	eDMA channel 18 priority register	8
Base + 0x0113	EDMA_CPR19	eDMA channel 19 priority register	8
Base + 0x0114	EDMA_CPR20	eDMA channel 20 priority register	8
Base + 0x0115	EDMA_CPR21	eDMA channel 21 priority register	8
Base + 0x0116	EDMA_CPR22	eDMA channel 22 priority register	8
Base + 0x0117	EDMA_CPR23	eDMA channel 23 priority register	8
Base + 0x0118	EDMA_CPR24	eDMA channel 24 priority register	8
Base + 0x0119	EDMA_CPR25	eDMA channel 25 priority register	8
Base + 0x011A	EDMA_CPR26	eDMA channel 26 priority register	8
Base + 0x011B	EDMA_CPR27	eDMA channel 27 priority register	8
Base + 0x011C	EDMA_CPR28	eDMA channel 28 priority register	8
Base + 0x011D	EDMA_CPR29	eDMA channel 29 priority register	8
Base + 0x011E	EDMA_CPR30	eDMA channel 30 priority register	8
Base + 0x011F	EDMA_CPR31	eDMA channel 31 priority register	8
Base + 0x0120	EDMA_CPR32	eDMA channel 32 priority register	8
Base + 0x0121	EDMA_CPR33	eDMA channel 33 priority register	8
Base + 0x0122	EDMA_CPR34	eDMA channel 34 priority register	8
Base + 0x0123	EDMA_CPR35	eDMA channel 35 priority register	8
Base + 0x0124	EDMA_CPR36	eDMA channel 36 priority register	8
Base + 0x0125	EDMA_CPR37	eDMA channel 37 priority register	8

Table 9-1. eDMA 32-bit Memory Map (continued)

Address	Register Name	Register Description	Bits
Base + 0x0126	EDMA_CPR38	eDMA channel 38 priority register	8
Base + 0x0127	EDMA_CPR39	eDMA channel 39 priority register	8
Base + 0x0128	EDMA_CPR40	eDMA channel 40 priority register	8
Base + 0x0129	EDMA_CPR41	eDMA channel 41 priority register	8
Base + 0x012A	EDMA_CPR42	eDMA channel 42 priority register	8
Base + 0x012B	EDMA_CPR43	eDMA channel 43 priority register	8
Base + 0x012C	EDMA_CPR44	eDMA channel 44 priority register	8
Base + 0x012D	EDMA_CPR45	eDMA channel 45 priority register	8
Base + 0x012E	EDMA_CPR46	eDMA channel 46 priority register	8
Base + 0x012F	EDMA_CPR47	eDMA channel 47 priority register	8
Base + 0x0130	EDMA_CPR48	eDMA channel 48 priority register	8
Base + 0x0131	EDMA_CPR49	eDMA channel 49 priority register	8
Base + 0x0132	EDMA_CPR50	eDMA channel 50 priority register	8
Base + 0x0133	EDMA_CPR51	eDMA channel 51 priority register	8
Base + 0x0134	EDMA_CPR52	eDMA channel 52 priority register	8
Base + 0x0135	EDMA_CPR53	eDMA channel 53 priority register	8
Base + 0x0136	EDMA_CPR54	eDMA channel 54 priority register	8
Base + 0x0137	EDMA_CPR55	eDMA channel 55 priority register	8
Base + 0x0138	EDMA_CPR56	eDMA channel 56 priority register	8
Base + 0x0139	EDMA_CPR57	eDMA channel 57 priority register	8
Base + 0x013A	EDMA_CPR58	eDMA channel 58 priority register	8
Base + 0x013B	EDMA_CPR59	eDMA channel 59 priority register	8
Base + 0x013C	EDMA_CPR60	eDMA channel 60 priority register	8
Base + 0x013D	EDMA_CPR61	eDMA channel 61 priority register	8
Base + 0x013E	EDMA_CPR62	eDMA channel 62 priority register	8
Base + 0x013F	EDMA_CPR63	eDMA channel 63 priority register	8
Base + 0x0140–0x0FFF	—	Reserved	—
Base + 0x1000	TCD00	eDMA transfer control descriptor 00	256
Base + 0x1020	TCD01	eDMA transfer control descriptor 01	256
Base + 0x1040	TCD02	eDMA transfer control descriptor 02	256
Base + 0x1060	TCD03	eDMA transfer control descriptor 03	256
Base + 0x1080	TCD04	eDMA transfer control descriptor 04	256
Base + 0x10A0	TCD05	eDMA transfer control descriptor 05	256

Table 9-1. eDMA 32-bit Memory Map (continued)

Address	Register Name	Register Description	Bits
Base + 0x10C0	TCD06	eDMA transfer control descriptor 06	256
Base + 0x10E0	TCD07	eDMA transfer control descriptor 07	256
Base + 0x1100	TCD08	eDMA transfer control descriptor 08	256
Base + 0x1120	TCD09	eDMA transfer control descriptor 09	256
Base + 0x1140	TCD10	eDMA transfer control descriptor 10	256
Base + 0x1160	TCD11	eDMA transfer control descriptor 11	256
Base + 0x1180	TCD12	eDMA transfer control descriptor 12	256
Base + 0x11A0	TCD13	eDMA transfer control descriptor 13	256
Base + 0x11C0	TCD14	eDMA transfer control descriptor 14	256
Base + 0x11E0	TCD15	eDMA transfer control descriptor 15	256
Base + 0x1200	TCD16	eDMA transfer control descriptor 16	256
Base + 0x1220	TCD17	eDMA transfer control descriptor 17	256
Base + 0x1240	TCD18	eDMA transfer control descriptor 18	256
Base + 0x1260	TCD19	eDMA transfer control descriptor 19	256
Base + 0x1280	TCD20	eDMA transfer control descriptor 20	256
Base + 0x12A0	TCD21	eDMA transfer control descriptor 21	256
Base + 0x12C0	TCD22	eDMA transfer control descriptor 22	256
Base + 0x12E0	TCD23	eDMA transfer control descriptor 23	256
Base + 0x1300	TCD24	eDMA transfer control descriptor 24	256
Base + 0x1320	TCD25	eDMA transfer control descriptor 25	256
Base + 0x1340	TCD26	eDMA transfer control descriptor 26	256
Base + 0x1360	TCD27	eDMA transfer control descriptor 27	256
Base + 0x1380	TCD28	eDMA transfer control descriptor 28	256
Base + 0x13A0	TCD29	eDMA transfer control descriptor 29	256
Base + 0x13C0	TCD30	eDMA transfer control descriptor 30	256
Base + 0x13E0	TCD31	eDMA transfer control descriptor 31	256
Base + 0x1400	TCD32	eDMA transfer control descriptor 32	256
Base + 0x1420	TCD33	eDMA transfer control descriptor 33	256
Base + 0x1440	TCD34	eDMA transfer control descriptor 34	256
Base + 0x1460	TCD35	eDMA transfer control descriptor 35	256
Base + 0x1480	TCD36	eDMA transfer control descriptor 36	256
Base + 0x14A0	TCD37	eDMA transfer control descriptor 37	256
Base + 0x14C0	TCD38	eDMA transfer control descriptor 38	256

Table 9-1. eDMA 32-bit Memory Map (continued)

Address	Register Name	Register Description	Bits
Base + 0x14E0	TCD39	eDMA transfer control descriptor 39	256
Base + 0x1500	TCD40	eDMA transfer control descriptor 40	256
Base + 0x1520	TCD41	eDMA transfer control descriptor 41	256
Base + 0x1540	TCD42	eDMA transfer control descriptor 42	256
Base + 0x1560	TCD43	eDMA transfer control descriptor 43	256
Base + 0x1580	TCD44	eDMA transfer control descriptor 44	256
Base + 0x15A0	TCD45	eDMA transfer control descriptor 45	256
Base + 0x15C0	TCD46	eDMA transfer control descriptor 46	256
Base + 0x15E0	TCD47	eDMA transfer control descriptor 47	256
Base + 0x1600	TCD48	eDMA transfer control descriptor 48	256
Base + 0x1620	TCD49	eDMA transfer control descriptor 49	256
Base + 0x1640	TCD50	eDMA transfer control descriptor 50	256
Base + 0x1660	TCD51	eDMA transfer control descriptor 51	256
Base + 0x1680	TCD52	eDMA transfer control descriptor 52	256
Base + 0x16A0	TCD53	eDMA transfer control descriptor 53	256
Base + 0x16C0	TCD54	eDMA transfer control descriptor 54	256
Base + 0x16E0	TCD55	eDMA transfer control descriptor 55	256
Base + 0x1700	TCD56	eDMA transfer control descriptor 56	256
Base + 0x1720	TCD57	eDMA transfer control descriptor 57	256
Base + 0x1740	TCD58	eDMA transfer control descriptor 58	256
Base + 0x1760	TCD59	eDMA transfer control descriptor 59	256
Base + 0x1780	TCD60	eDMA transfer control descriptor 60	256
Base + 0x17A0	TCD61	eDMA transfer control descriptor 61	256
Base + 0x17C0	TCD62	eDMA transfer control descriptor 62	256
Base + 0x17E0	TCD63	eDMA transfer control descriptor 63	256

9.2.2 Register Descriptions

Read operations on reserved bits in a register return undefined data. Do not write operations to reserved bits. Writing to reserved bits in a register can generate errors. The maximum register bit-width for this device is 64-bits wide. These registers are implemented as two 32-bit registers, and include an ‘H’ and ‘L’ suffixes, indicating the high and low portions of the control function.

9.2.2.1 eDMA Control Register (EDMA_CR)

The 32-bit EDMA_CR defines the basic operating configuration of the eDMA.

The eDMA arbitrates channel service requests in four groups (0, 1, 2, 3) of 16 channels each:

- Group 0 contains channels 0–15
- Group 1 contains channels 16–31
- Group 2 contains channels 32-47
- Group 3 contains channels 48-63

Arbitration within a group can be configured to use either fixed-priority or round-robin. In fixed-priority arbitration, the highest priority channel requesting service is selected to execute. The priorities are assigned by the channel priority registers. In round-robin arbitration mode, the channel priorities are ignored and the channels within each group are cycled through, from channel 15 down to channel 0, without regard to priority.

Refer to Section 9.2.2.16, "eDMA Channel n Priority Registers (EDMA_CPRn)."

The group priorities operate in a similar fashion. In group fixed-priority arbitration mode, channel service requests in the highest priority group are executed first where priority level 3 is the highest and priority level 0 is the lowest. The group priorities are assigned in the GRP*n*PRI fields of the eDMA control register (EDMA_CR). All group priorities must have unique values prior to any channel service requests occur, otherwise a configuration error is reported. In group round-robin mode, the group priorities are ignored and the groups are cycled through, from group 3 down to group 0, without regard to priority.

Address: Base + 0x0000 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	GRP3PRI		GRP2PRI		GRP1PRI		GRP0PRI		0	0	0	0	ERGA	ERCA	EDBG	0
W																
Reset	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0

Figure 9-2. eDMA Control Register (EDMA_CR)

Table 9-2. EDMA_CR Field Descriptions

Field	Description
0–15	Reserved
16–17 GRP3PRI	Channel group 3 priority. Group 3 priority level when fixed priority group arbitration is enabled.
18–19 GRP2PRI	Channel group 2 priority. Group 2 priority level when fixed priority group arbitration is enabled.
20–21 GRP1PRI	Channel group 1 priority. Group 1 priority level when fixed-priority group arbitration is enabled.

Table 9-2. EDMA_CR Field Descriptions (continued)

Field	Description
22–23 GRP0PRI	Channel group 0 priority. Group 0 priority level when fixed-priority group arbitration is enabled.
24–27	Reserved
28 ERGA	Enable round-robin group arbitration. 0 Fixed-priority arbitration is used for selection among the groups. 1 Round-robin arbitration is used for selection among the groups.
29 ERCA	Enable round-robin channel arbitration. 0 Fixed-priority arbitration is used for channel selection within each group. 1 Round-robin arbitration is used for channel selection within each group.
30 EDBG	Enable debug. 0 The assertion of the system debug control input is ignored. 1 The assertion of the system debug control input causes the eDMA to stall the start of a new channel. Executing channels are allowed to complete. Channel execution resumes when either the system debug control input is negated or the EDBG bit is cleared.
31	Reserved

9.2.2.2 eDMA Error Status Register (EDMA_ESR)

The EDMA_ESR provides information concerning the last recorded channel error. Channel errors can be caused by a configuration error (an illegal setting in the transfer control descriptor or an illegal priority register setting in fixed arbitration mode) or an error termination to a bus master read or write cycle.

A configuration error is caused when the starting source or destination address, source or destination offsets, minor loop byte count, and the transfer size represent an inconsistent state. The addresses and offsets must be aligned on 0-modulo-transfer_size boundaries, and the minor loop byte count must be a multiple of the source and destination transfer sizes. All source reads and destination writes must be configured to the natural boundary of the programmed transfer size respectively.

In fixed arbitration mode, a configuration error is caused by any two channel priorities being equal within a group, or any group priority levels being equal among the groups. For either type of priority configuration error, the ERRCHN field is undefined. All channel priority levels within a group must be unique and all group priority levels among the groups must be unique when fixed arbitration mode is enabled.

If a scatter/gather operation is enabled upon channel completion, a configuration error is reported if the scatter/gather address (DLAST_SGA) is not aligned on a 32-byte boundary. If minor loop channel linking is enabled upon channel completion, a configuration error is reported when the link is attempted if the TCD.CITER.E_LINK bit does not equal the TCD.BITER.E_LINK bit. All configuration error conditions except scatter/gather and minor loop link error are reported as the channel is activated and assert an error interrupt request if enabled. When properly enabled, a scatter/gather configuration error is reported when the scatter/gather operation begins at major loop completion. A minor loop channel link configuration error is reported when the link operation is serviced at minor loop completion.

If a system bus read or write is terminated with an error, the data transfer is immediately stopped and the appropriate bus error flag is set. In this case, the state of the channel’s transfer control descriptor is updated

by the eDMA engine with the current source address, destination address, and minor loop byte count at the point of the fault. If a bus error occurs on the last read prior to beginning the write sequence, the write executes using the data captured during the bus error. If a bus error occurs on the last write prior to switching to the next read sequence, the read sequence executes before the channel is terminated due to the destination bus error.

The occurrence of any type of error causes the eDMA engine to stop the active channel, and the appropriate channel bit in the eDMA error register to be asserted. At the same time, the details of the error condition are loaded into the EDMA_ESR. The major loop complete indicators, setting the transfer control descriptor DONE flag and the possible assertion of an interrupt request, are *not* affected when an error is detected. After the error status has been updated, the eDMA engine continues to operate by servicing the next appropriate channel. A channel that experiences an error condition is not automatically disabled. If a channel is terminated by an error and then issues another service request before the error is fixed, that channel executes and terminates with the same error condition.

Address: Base + 0x0004 Access: User R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	VLD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	GPE	CPE	ERRCHN						SAE	SOE	DAE	DOE	NCE	SGE	SBE	DBE
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9-3. eDMA Error Status Register (EDMA_ESR)

Table 9-3. EDMA_ESR Field Descriptions

Field	Description
0 VLD	Logical OR of all EDMA_ERH and EDMA_ERL status bits. 0 No EDMA_ER bits are set. 1 At least one EDMA_ER bit is set indicating a valid error exists that has not been cleared.
1–15	Reserved
16 GPE	Group priority error. 0 No group priority error. 1 The last recorded error was a configuration error among the group priorities indicating not all group priorities are unique.
17 CPE	Channel priority error. 0 No channel priority error. 1 The last recorded error was a configuration error in the channel priorities within a group, indicating not all channel priorities within a group are unique.

Table 9-3. EDMA_ESR Field Descriptions (continued)

Field	Description
18–23 ERRCHN[0:5]	Error channel number. Channel number of the last recorded error (excluding GPE and CPE errors). **Note:** Do not rely on the number in the ERRCHN field for group and channel priority errors. Group and channel priority errors need to be resolved by inspection. The application code must interrogate the priority registers to find groups or channels with duplicate priority level.
24 SAE	Source address error. 0 No source address configuration error. 1 The last recorded error was a configuration error detected in the TCD.SADDR field, indicating TCD.SADDR is inconsistent with TCD.SSIZE.
25 SOE	Source offset error. 0 No source offset configuration error. 1 The last recorded error was a configuration error detected in the TCD.SOFF field, indicating TCD.SOFF is inconsistent with TCD.SSIZE.
26 DAE	Destination address error. 0 No destination address configuration error. 1 The last recorded error was a configuration error detected in the TCD.DADDR field, indicating TCD.DADDR is inconsistent with TCD.DSIZE.
27 DOE	Destination offset error. 0 No destination offset configuration error. 1 The last recorded error was a configuration error detected in the TCD.DOFF field, indicating TCD.DOFF is inconsistent with TCD.DSIZE.
28 NCE	NBYTES/CITER configuration error. 0 No NBYTES/CITER configuration error. 1 The last recorded error was a configuration error detected in the TCD.NBYTES or TCD.CITER fields, indicating the following conditions exist: • TCD.NBYTES is not a multiple of TCD.SSIZE and TCD.DSIZE, or • TCD.CITER is equal to zero, or • TCD.CITER.E_LINK is not equal to TCD.BITER.E_LINK.
29 SGE	Scatter/gather configuration error. 0 No scatter/gather configuration error. 1 The last recorded error was a configuration error detected in the TCD.DLAST_SGA field, indicating TCD.DLAST_SGA is not on a 32-byte boundary. This field is checked at the beginning of a scatter/gather operation after major loop completion if TCD.E_SG is enabled.
30 SBE	Source bus error. 0 No source bus error. 1 The last recorded error was a bus error on a source read.
31 DBE	Destination bus error. 0 No destination bus error. 1 The last recorded error was a bus error on a destination write.

9.2.2.3 eDMA Enable Request Registers (EDMA_ERQRH, EDMA_ERQRL)

The EDMA_ERQRH and EDMA_ERQRL provide a bit map for the 64 implemented channels to enable the request signal for each channel. EDMA_ERQRH supports channels 63–32, while EDMA_ERQRL covers channels 31–0.

The state of any given channel enable is directly affected by writes to these registers; the state is also affected by writes to the EDMA_SERQR and EDMA_CERQR. The EDMA_CERQR and

EDMA_SERQR are provided so that the request enable for a *single* channel can easily be modified without the need to perform a read-modify-write sequence to the EDMA_ERQRH and EDMA_ERQRL.

Both the DMA request input signal and this enable request flag must be asserted before a channel's hardware service request is accepted. The state of the eDMA enable request flag does *not* affect a channel service request made explicitly through software or a linked channel request.

Address: Base + 0x0008 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	ERQ 63	ERQ 62	ERQ 61	ERQ 60	ERQ 59	ERQ 58	ERQ 57	ERQ 56	ERQ 55	ERQ 54	ERQ 53	ERQ 52	ERQ 51	ERQ 50	ERQ 49	ERQ 48
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	ERQ 47	ERQ 46	ERQ 45	ERQ 44	ERQ 43	ERQ 42	ERQ 41	ERQ 40	ERQ 39	ERQ 38	ERQ 37	ERQ 36	ERQ 35	ERQ 34	ERQ 33	ERQ 32
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9-4. eDMA Enable Request High Register (EDMA_ERQRH)

Address: Base + 0x000C Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	ERQ 31	ERQ 30	ERQ 29	ERQ 28	ERQ 27	ERQ 26	ERQ 25	ERQ 24	ERQ 23	ERQ 22	ERQ 21	ERQ 20	ERQ 19	ERQ 18	ERQ 17	ERQ 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	ERQ 15	ERQ 14	ERQ 13	ERQ 12	ERQ 11	ERQ 10	ERQ 09	ERQ 08	ERQ 07	ERQ 06	ERQ 05	ERQ 04	ERQ 03	ERQ 02	ERQ 01	ERQ 00
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9-5. eDMA Enable Request Low Register (EDMA_ERQRL)

Table 9-4. EDMA_ERQRH, EDMA_ERQRL Field Descriptions

Field	Description
0–63 ERQ*n*	Enable DMA hardware service request *n.* 0 The DMA request signal for channel n is disabled. 1 The DMA request signal for channel n is enabled.

As a given channel completes the processing of its major iteration count, there is a flag in the transfer control descriptor that can affect the ending state of the EDMA_ERQR bit for that channel. If the TCD.D_REQ bit is set, then the corresponding EDMA_ERQR bit is cleared after the major loop is

complete, disabling the DMA hardware request. Otherwise if the D_REQ bit is cleared, the state of the EDMA_ERQR bit is unaffected.

9.2.2.4 eDMA Enable Error Interrupt Registers (EDMA_EEIRH, EDMA_EEIRL)

The EDMA_EEIRH and EDMA_EEIRL provide a bit map for the 64 channels to enable the error interrupt signal for each channel.EDMA_EEIRH supports channels 63–32, while EDMA_EEIRL covers channels 31–0.

The state of any given channel's error interrupt enable is directly affected by writes to these registers; it is also affected by writes to the EDMA_SEEIR and EDMA_CEEIR. The EDMA_SEEIR and EDMA_CEEIR are provided so that the error interrupt enable for a *single* channel can easily be modified without the need to perform a read-modify-write sequence to the EDMA_EEIRH and EDMA_EEIRL.

Both the DMA error indicator and this error interrupt enable flag must be asserted before an error interrupt request for a given channel is asserted.

Address: Base + 0x0010 Access: User read/write

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	EEI 63	EEI 62	EEI 61	EEI 60	EEI 59	EEI 58	EEI 57	EEI 56	EEI 55	EEI 54	EEI 53	EEI 52	EEI 51	EEI 50	EEI 49	EEI 48
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	EEI 47	EEI 46	EEI 45	EEI 44	EEI 43	EEI 42	EEI 41	EEI 40	EEI 39	EEI 38	EEI 37	EEI 36	EEI 35	EEI 34	EEI 33	EEI 32
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9-6. eDMA Enable Error Interrupt High Register (EDMA_EEIRH)

Address: Base + 0x0014 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	EEI 31	EEI 30	EEI 29	EEI 28	EEI 27	EEI 26	EEI 25	EEI 24	EEI 23	EEI 22	EEI 21	EEI 20	EEI 19	EEI 18	EEI 17	EEI 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	EEI 15	EEI 14	EEI 13	EEI 12	EEI 11	EEI 10	EEI 09	EEI 08	EEI 07	EEI 06	EEI 05	EEI 04	EEI 03	EEI 02	EEI 01	EEI 00
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9-7. eDMA Enable Error Interrupt Low Register (EDMA_EEIRL)

Table 9-5. EDMA_EEIRH, EDMA_EEIRL Field Descriptions

Field	Description
0–63 EEI*n*	Enable error interrupt *n.* 0 The error signal for channel *n* does not generate an error interrupt. 1 The assertion of the error signal for channel *n* generate an error interrupt request.

9.2.2.5 eDMA Set Enable Request Register (EDMA_SERQR)

The EDMA_SERQR provides a simple memory-mapped mechanism to set a given bit in the EDMA_ERQRH or EDMA_ERQRL to enable the DMA request for a given channel. The data value on a register write causes the corresponding bit in the EDMA_ERQRH or EDMA_ERQRL to be set. Setting bit 1 (SERQ*n*) provides a global set function, forcing the entire contents of EDMA_ERQRH and EDMA_ERQRL to be asserted. Reads of this register return all zeroes.

Address: Base + 0x0018 Access: User W/O

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	0	0
W		SERQ[0:6]						
Reset	0	0	0	0	0	0	0	0

Figure 9-8. eDMA Set Enable Request Register (EDMA_SERQR)

Table 9-6. EDMA_SERQR Field Descriptions

Field	Descriptions
0	Reserved
1–7 SERQ[0:6]	Set enable request. 0–63 Set corresponding bit in EDMA_ERQRH or EDMA_ERQRL 64–127 Set all bits in EDMA_ERQRH and EDMA_ERQRL

9.2.2.6 eDMA Clear Enable Request Register (EDMA_CERQR)

The EDMA_CERQR provides a simple memory-mapped mechanism to clear a given bit in the EDMA_ERQRH or EDMA_ERQRL to disable the DMA request for a given channel. The data value on a register write causes the corresponding bit in the EDMA_ERQRH or EDMA_ERQRL to be cleared. Setting bit 1 (CERQ*n*) provides a global clear function, forcing the entire contents of the EDMA_ERQRH and EDMA_ERQRL to be zeroed, disabling all DMA request inputs. Reads of this register return all zeroes.

Address: Base + 0x0019 Access: User W/O

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	0	0
W		CERQ[0:6]						
Reset	0	0	0	0	0	0	0	0

Figure 9-9. eDMA Clear Enable Request Register (EDMA_CERQR)

Table 9-7. EDMA_CERQR Field Descriptions

Field	Description
0	Reserved
1–7 CERQ[0:6]	Clear enable request. 0–63 Clear corresponding bit in EDMA_ERQRH or EDMA_ERQRL 64–127 Clear all bits in EDMA_ERQRH and EDMA_ERQRL

9.2.2.7 eDMA Set Enable Error Interrupt Register (EDMA_SEEIR)

The EDMA_SEEIR provides a simple memory-mapped mechanism to set a given bit in the EDMA_EEIRH or EDMA_EEIRL to enable the error interrupt for a given channel. The data value on a register write causes the corresponding bit in the EDMA_EEIRH or EDMA_EEIRL to be set. Setting bit 1 (SEEI*n*) provides a global set function, forcing the entire contents of EDMA_EEIRH or EDMA_EEIRL to be asserted. Reads of this register return all zeroes.

Address: Base + 0x001A Access: User W/O

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	0	0
W		SEEI[0:6]						
Reset	0	0	0	0	0	0	0	0

Figure 9-10. eDMA Set Enable Error Interrupt Register (EDMA_SEEIR)

Table 9-8. EDMA_SEEIR Field Descriptions

Field	Description
0	Reserved
1–7 SEEI[0:6]	Set enable error interrupt. 0–63 Set corresponding bit in EDMA_EEIRH or EDMA_EEIRL 64–127 Set all bits in EDMA_EEIRH or EDMA_EEIRL

9.2.2.8 eDMA Clear Enable Error Interrupt Register (EDMA_CEEIR)

The EDMA_CEEIR provides a simple memory-mapped mechanism to clear a given bit in the EDMA_EEIRH or EDMA_EEIRL to disable the error interrupt for a given channel. The data value on a register write causes the corresponding bit in the EDMA_EEIRH or EDMA_EEIRL to be cleared. Setting bit 1 (CEEI*n*) provides a global clear function, forcing the entire contents of the EDMA_EEIRH or EDMA_EEIRL to be zeroed, disabling error interrupts for all channels. Reads of this register return all zeroes.

Address: Base + 0x001B Access: User W/O

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	0	0
W		CEEI[0:6]						
Reset	0	0	0	0	0	0	0	0

Figure 9-11. eDMA Clear Enable Error Interrupt Register (EDMA_CEEIR)

Table 9-9. EDMA_CEEIR Field Descriptions

Field	Description
0	Reserved
1–7 CEEI[0:6]	Clear enable error interrupt. 0–63 Clear corresponding bit in EDMA_EEIRH or EDMA_EEIRL 64–127 Clear all bits in EDMA_EEIRH or EDMA_EEIRL

9.2.2.9 eDMA Clear Interrupt Request Register (EDMA_CIRQR)

The EDMA_CIRQR provides a simple memory-mapped mechanism to clear a given bit in the EDMA_IRQRH or EDMA_IRQRL to disable the interrupt request for a given channel. The given value on a register write causes the corresponding bit in the EDMA_IRQRH or EDMA_IRQRL to be cleared. Setting bit 1 (CINT*n*) provides a global clear function, forcing the entire contents of the EDMA_IRQRH or EDMA_IRQRL to be zeroed, disabling all DMA interrupt requests. Reads of this register return all zeroes.

Address: Base + 0x001C Access: User W/O

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	0	0
W		CINT[0:6]						
Reset	0	0	0	0	0	0	0	0

Figure 9-12. eDMA Clear Interrupt Request (EDMA_CIRQR)

Table 9-10. EDMA_CIRQR Field Descriptions

Field	Description
0	Reserved
1–7 CINT[0:6]	Clear interrupt request. 0–63 Clear corresponding bit in EDMA_IRQRH or EDMA_IRQRL 64–127 Clear all bits in EDMA_IRQRH or EDMA_IRQRL

9.2.2.10 eDMA Clear Error Register (EDMA_CER)

The EDMA_CER provides a simple memory-mapped mechanism to clear a given bit in the EDMA_ERH or EDMA_ERL to disable the error condition flag for a given channel. The given value on a register write causes the corresponding bit in the EDMA_ERH or EDMA_ERL to be cleared. Setting bit 1 (CERR*n*) provides a global clear function, forcing the entire contents of the EDMA_ERH and EDMA_ERL to be zeroed, clearing all channel error indicators. Reads of this register return all zeroes.

Address: Base + 0x001D Access:User W/O

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	0	0
W		CERR[0:6]						
Reset	0	0	0	0	0	0	0	0

Figure 9-13. eDMA Clear Error Register (EDMA_CER)

Table 9-11. EDMA_CER Field Descriptions

Field	Description
0	Reserved
1–7 CERR[0:6]	Clear error indicator. 0–63 Clear corresponding bit in EDMA_ERH or EDMA_ERL 64–127 Clear all bits in EDMA_ERH or EDMA_ERL

9.2.2.11 eDMA Set START Bit Register (EDMA_SSBR)

The EDMA_SSBR provides a memory-mapped mechanism to set the START bit in the TCD for a channel. The data value on a register write sets the START bit in the transfer control descriptor. SSB*n* is a global set function that sets all START bits for a channel. Reads of this register return all zeroes.

Address: Base + 0x001E Access: User W/O

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	0	0
W		SSB[0:6]						
Reset	0	0	0	0	0	0	0	0

Figure 9-14. eDMA Set START Bit Register (EDMA_SSBR)

Table 9-12. EDMA_SSBR Field Descriptions

Field	Description
0	Reserved
1–7 SSB[0:6]	Set START bit (channel service request). 0–63 Set the corresponding channel's TCD.START

9.2.2.12 eDMA Clear DONE Status Bit Register (EDMA_CDSBR)

The EDMA_CDSBR provides a simple memory-mapped mechanism to clear the DONE bit in the TCD of the given channel. The data value on a register write causes the DONE bit in the corresponding transfer control descriptor to be cleared. Setting bit 1 (CDSB*n*) provides a global clear function, forcing all DONE bits to be cleared.

Address: Base + 0x001F Access: User W/O

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	0	0
W		CDSB[0:6]						
Reset	0	0	0	0	0	0	0	0

Figure 9-15. eDMA Clear DONE Status Bit Register (EDMA_CDSBR)

Table 9-13. EDMA_CDSBR Field Descriptions

Field	Description
0	Reserved
1–7 CDSB[0:6]	Clear DONE status bit. 0–63 Clear the corresponding channel's DONE bit 64–127 Clear all TCD DONE bits

9.2.2.13 eDMA Interrupt Request Registers (EDMA_IRQRH, EDMA_IRQRL)

The EDMA_IRQRH and EDMA_IRQRL provide a bit map for the 64 channels signaling the presence of an interrupt request for each channel. EDMA_IRQRH supports channels 63–32, while EDMA_IRQRL covers channels 31–0.

The eDMA engine signals the occurrence of a programmed interrupt upon the completion of a data transfer as defined in the transfer control descriptor by setting the appropriate bit in this register. The outputs of this register are directly routed to the interrupt controller (INTC). During the execution of the interrupt service routine associated with any given channel, it is software's responsibility to clear the appropriate bit, negating the interrupt request. Typically, a write to the EDMA_CIRQR in the interrupt service routine is used for this purpose.

The state of any given channel's interrupt request is directly affected by writes to this register; it is also affected by writes to the EDMA_CIRQR. On writes to the EDMA_IRQRH or EDMA_IRQRL, a 1 in any bit position clears the corresponding channel's interrupt request. A zero in any bit position has no affect on the corresponding channel's current interrupt status. The EDMA_CIRQR is provided so the interrupt request for a *single* channel can easily be cleared without the need to perform a read-modify-write sequence to the EDMA_IRQRH and EDMA_IRQRL.

Address: Base + 0x0020 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	INT 63	INT 62	INT 61	INT 60	INT 59	INT 58	INT 57	INT 56	INT 55	INT 54	INT 53	INT 52	INT 51	INT 50	INT 49	INT 48
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	INT 47	INT 46	INT 45	INT 44	INT 43	INT 42	INT 41	INT 40	INT 39	INT 38	INT 37	INT 36	INT 35	INT 34	INT 33	INT 32
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9-16. eDMA Interrupt Request High Register (EDMA_IRQRH)

Address: Base + 0x0024 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	INT 31	INT 30	INT 29	INT 28	INT 27	INT 26	INT 25	INT 24	INT 23	INT 22	INT 21	INT 20	INT 19	INT 18	INT 17	INT 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	INT 15	INT 14	INT 13	INT 12	INT 11	INT 10	INT 09	INT 08	INT 07	INT 06	INT 05	INT 04	INT 03	INT 02	INT 01	INT 00
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9-17. eDMA Interrupt Request Low Register (EDMA_IRQRL)

Table 9-14. EDMA_IRQRH, EDMA_IRQRL Field Descriptions

Field	Description
0–63 INT*n*	eDMA interrupt request *n.* 0 The interrupt request for channel *n* is cleared. 1 The interrupt request for channel *n* is active.

9.2.2.14 eDMA Error Registers (EDMA_ERH, EDMA_ERL)

The EDMA_ERH and EDMA_ERL provide a bit map for the 64channels signaling the presence of an error for each channel. EDMA_ERH supports channels 63–32, while EDMA_ERL covers channels 31–0.

The eDMA engine signals the occurrence of a error condition by setting the appropriate bit in this register. The outputs of this register are enabled by the contents of the EDMA_EEIR, then logically summed across groups of 16, 32, and 64 channels to form several group error interrupt requests which is then routed to the interrupt controller. During the execution of the interrupt service routine associated with any DMA errors, it is software's responsibility to clear the appropriate bit, negating the error interrupt request. Typically, a write to the EDMA_CER in the interrupt service routine is used for this purpose. Recall the normal DMA

channel completion indicators, setting the transfer control descriptor DONE flag and the possible assertion of an interrupt request, are *not* affected when an error is detected.

The contents of this register can also be polled and a non-zero value indicates the presence of a channel error, regardless of the state of the EDMA_EEIR. The EDMA_ESR[VLD] bit is a logical OR of all bits in this register and it provides a single bit indication of any errors. The state of any given channel's error indicators is affected by writes to this register; it is also affected by writes to the EDMA_CER. On writes to EDMA_ERH or EDMA_ERL, a 1 in any bit position clears the corresponding channel's error status. A 0 in any bit position has no affect on the corresponding channel's current error status. The EDMA_CER is provided so the error indicator for a *single* channel can easily be cleared.

Address: Base + 0x0028 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	ERR 63	ERR 62	ERR 61	ERR 60	ERR 59	ERR 58	ERR 57	ERR 56	ERR 55	ERR 54	ERR 53	ERR 52	ERR 51	ERR 50	ERR 49	ERR 48
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	ERR 47	ERR 46	ERR 45	ERR 44	ERR 43	ERR 42	ERR 41	ERR 40	ERR 39	ERR 38	ERR 37	ERR 36	ERR 35	ERR 34	ERR 33	ERR 32
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9-18. eDMA Error High Register (EDMA_ERH)

Address: Base + 0x002C Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	ERR 31	ERR 30	ERR 29	ERR 28	ERR 27	ERR 26	ERR 25	ERR 24	ERR 23	ERR 22	ERR 21	ERR 20	ERR 19	ERR 18	ERR 17	ERR 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	ERR 15	ERR 14	ERR 13	ERR 12	ERR 11	ERR 10	ERR 09	ERR 08	ERR 07	ERR 06	ERR 05	ERR 04	ERR 03	ERR 02	ERR 01	ERR 00
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9-19. eDMA Error Low Register (EDMA_ERL)

Table 9-15. EDMA_ERH, EDMA_ERL Field Descriptions

Field	Description
0–63 ERR*n*	eDMA Error *n.* 0 An error in channel *n* has not occurred. 1 An error in channel *n* has occurred.

9.2.2.15 DMA Hardware Request Status (EDMA_HRSH, EDMA_HRSL)

The EDMA_HRSH and EDMA_HRSL registers provide a bit map for the implemented channels (16,32, and 64) to show the current hardware request status for each channel. EDMA_HRSH supports channels 63–32, while EDMA_HRSL supports channels 31–00.

Address: Base + 0x0030 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	HRS 63	HRS 62	HRS 61	HRS 60	HRS 59	HRS 58	HRS 57	HRS 56	HRS 55	HRS 54	HRS 53	HRS 52	HRS 51	HRS 50	HRS 49	HRS 48
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	HRS 47	HRS 46	HRS 45	HRS 44	HRS 43	HRS 42	HRS 41	HRS 40	HRS 39	HRS 38	HRS 37	HRS 36	HRS 35	HRS 34	HRS 33	HRS 32
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9-20. EDMA Hardware Request Status Register High (EDMA_HRSH)

Address: Base + 0x0034 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	HRS 31	HRS 30	HRS 29	HRS 28	HRS 27	HRS 26	HRS 25	HRS 24	HRS 23	HRS 22	HRS 21	HRS 20	HRS 19	HRS 18	HRS 17	HRS 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	HRS 15	HRS 14	HRS 13	HRS 12	HRS 11	HRS 10	HRS 09	HRS 08	HRS 07	HRS 06	HRS 05	HRS 04	HRS 03	HRS 02	HRS 01	HRS 00
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 9-21. EDMA Hardware Request Status Register Low (EDMA_HRSL)

Table 9-16. EDMA_HRSH and EDMA_HRSL Field Descriptions

Field	Description
0–63 HRSn	DMA Hardware Request Status 0 A hardware service request for channel n is not present. 1 A hardware service request for channel n is present. **Note:** The hardware request status reflects the state of the request as seen by the arbitration logic. Therefore, this status is affected by the EDMA_ERQRL[ERQn] bit.

9.2.2.16 eDMA Channel *n* Priority Registers (EDMA_CPR*n*)

When the fixed-priority channel arbitration mode is enabled (EDMA_CR[ERCA] = 0), the contents of these registers define the unique priorities associated with each channel within a group. The channel priorities are evaluated by numeric value; that is, 0 is the lowest priority, 1 is the next higher priority, then 2, 3, etc. If software chooses to modify channel priority values, then the software must ensure that the channel priorities contain unique values, otherwise a configuration error is reported. The range of the priority value is limited to the values of 0 through 15. When read, the GRPPRI bits of the EDMA_CPR*n* register reflect the current priority level of the group of channels in which the corresponding channel resides. GRPPRI bits are not affected by writes to the EDMA_CPR*n* registers. The group priority is assigned in the EDMA_CR.

Refer to Figure 9-2 and Table 9-2 for the EDMA_CR definition.

Channel preemption is enabled on a per-channel basis by setting the ECP bit in the EDMA_CPR*n* register. Channel preemption allows the executing channel's data transfers to be temporarily suspended in favor of starting a higher priority channel. After the preempting channel has completed all of its minor loop data transfers, the preempted channel is restored and resumes execution. After the restored channel completes one read/write sequence, it is again eligible for preemption. If any higher priority channel is requesting service, the restored channel is suspended and the higher priority channel is serviced. Nested preemption (attempting to preempt a preempting channel) is not supported. After a preempting channel begins execution, it cannot be preempted. Preemption is only available when fixed arbitration is selected for both group and channel arbitration modes.

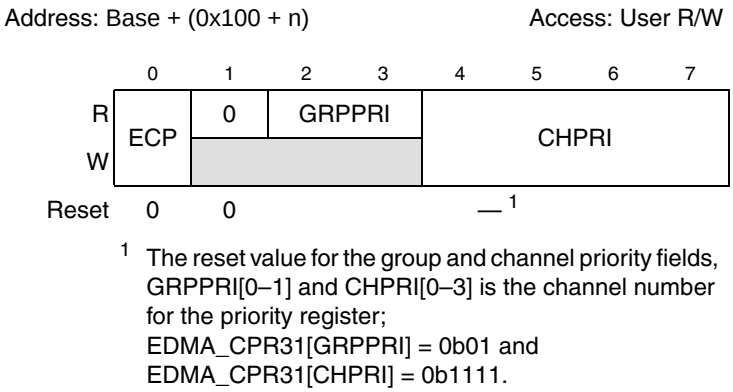


Figure 9-22. eDMA Channel *n* Priority Register (EDMA_CPR*n*)

The following table describes the fields in the eDMA channel *n* priority register:

Table 9-17. EDMA_CPR*n* Field Descriptions

Field	Description
0 ECP	Enable channel preemption. 0 Channel *n* cannot be suspended by a higher priority channel's service request. 1 Channel *n* can be temporarily suspended by the service request of a higher priority channel.
1	Reserved

Table 9-17. EDMA_CPR*n* Field Descriptions (continued)

Field	Description
2–3 GRPPRI [0:1]	Channel *n* current group priority. Group priority assigned to this channel group when fixed-priority arbitration is enabled. These two bits are read only; writes are ignored. The reset value for the group priority fields, is equal to the corresponding channel number for each priority register; that is, EDMA_CPR31[GRPPRI] = 0b01.
4–7 CHPRI [0:3]	Channel *n* arbitration priority. Channel priority when fixed-priority arbitration is enabled. The reset value for the channel priority fields CHPRI[0–3], is equal to the corresponding channel number for each priority register; that is, EDMA_CPR31[CHPRI] = 0b1111.

9.2.2.17 Transfer Control Descriptor (TCD)

Each channel requires a 256-bit transfer control descriptor for defining the desired data movement operation. The channel descriptors are stored in the local memory in sequential order: channel 0, channel 1,... channel 63. The definitions of the TCD are presented as 23 variable-length fields.

Table 9-18 defines the fields of the basic TCD structure.

Table 9-18. TCD*n* 32-bit Memory Structure

eDMA Bit Offset	Bit Length	TCD*n* Field Name	TCD*n* Abbreviation	Word #
0x1000 + (32 x n) + 0	32	Source address	SADDR	Word 0
0x1000 + (32 x n) + 32	5	Source address modulo	SMOD	Word 1
0x1000 + (32 x n) + 37	3	Source data transfer size	SSIZE	
0x1000 + (32 x n) + 40	5	Destination address modulo	DMOD	
0x1000 + (32 x n) + 45	3	Destination data transfer size	DSIZE	
0x1000 + (32 x n) + 48	16	Signed source address offset	SOFF	
0x1000 + (32 x n) + 64	32	Inner minor byte count	NBYTES	Word 2
0x1000 + (32 x n) + 96	32	Last source address adjustment	SLAST	Word 3
0x1000 + (32 x n) + 128	32	Destination address	DADDR	Word 4
0x1000 + (32 x n) + 160	1	Channel-to-channel linking on minor loop complete	CITER.E_LINK	Word 5
0x1000 + (32 x n) + 161	6	Current major iteration count or Link channel number	CITER or CITER.LINKCH	
0x1000 + (32 x n) + 167	9	Current major iteration count	CITER	
0x1000 + (32 x n) + 176	16	Destination address offset (signed)	DOFF	
0x1000 + (32 x n) + 192	32	Last destination address adjustment / scatter gather address	DLAST_SGA	Word 6
0x1000 + (32 x n) + 224	1	Channel-to-channel Linking on Minor Loop Complete	BITER.E_LINK	Word 7
0x1000 + (32 x n) + 225	6	Starting major iteration count or link channel number	BITER or BITER.LINKCH	
0x1000 + (32 x n) + 231	9	Starting major iteration count	BITER	
0x1000 + (32 x n) + 240	2	Bandwidth control	BWC	
0x1000 + (32 x n) + 242	6	Link channel number	MAJOR.LINKCH	
0x1000 + (32 x n) + 248	1	Channel done	DONE	
0x1000 + (32 x n) + 249	1	Channel active	ACTIVE	
0x1000 + (32 x n) + 250	1	Channel-to-channel linking on major loop complete	MAJOR.E_LINK	
0x1000 + (32 x n) + 251	1	Enable scatter/gather processing	E_SG	
0x1000 + (32 x n) + 252	1	Disable request	D_REQ	
0x1000 + (32 x n) + 253	1	Channel interrupt enable when current major iteration count is half complete	INT_HALF	
0x1000 + (32 x n) + 254	1	Channel interrupt enable when current major iteration count complete	INT_MAJ	
0x1000 + (32 x n) + 255	1	Channel start	START	

Figure 9-23 defines the fields of the TCD*n* structure.

Word Offset	0 1 2 3	4 5 6 7	8 9 10 11	12 13 14 15	16 17 18 19	20 21 22 23	24 25 26 27	28 29 30 31
0x0000	SADDR							
0x0004	SMOD	SSIZE	DMOD	DSIZE	SOFF			
0x0008	NBYTES							
0x000C	SLAST							
0x0010	DADDR							
0x0014	CITER.E_ LINK	CITER[1] or CITER.LINKCH	CITER[1]		DOFF			
0x0018	DLAST_SGA							
0x001C	BITER.E_ LINK	BITER[2] or BITER.LINKCH	BITER[2]	BWC	MAJOR LINKCH	DONE	ACTIVE	MAJOR.E_LINK E_SG D_REQ INT_HALF INT_MAJ START

Figure 9-23. TCD Structure

1 If channel linking on minor link completion is disabled, TCD bits [161:175] are used to form a 15-bit CITER field; if channel-to-channel linking is enabled, CITER becomes a 9-bit field.

2 If channel linking on minor link completion is disabled, TCD bits [225:239] are used to form a 15-bit BITER field; if channel-to-channel linking is enabled, BITER becomes a 9-bit field.

NOTE

The TCD structures for the eDMA channels shown in Figure 9-23 are implemented in internal SRAM. These structures are not initialized at reset. Therefore, all channel TCD parameters must be initialized by the application code before activating that channel.

The following table gives a detailed description of the TCD*n* fields:

Table 9-19. TCD*n* Field Descriptions

Bits Word Offset [n:n]	Field Name	Description
0–31 0x0 [0:31]	SADDR [0:31]	Source address. Memory address pointing to the source data. Word 0x0, bits 0–31.
32–36 0x4 [0:4]	SMOD [0:4]	Source address modulo. 0 Source address modulo feature is disabled. not 0 This value defines a specific address range which is specified to be either the value after SADDR + SOFF calculation is performed or the original register value. The setting of this field provides the ability to easily implement a circular data queue. For data queues requiring power-of-2 “size” bytes, start the queue at a 0-modulo-size address and set the SMOD field to the value for the queue, freezing the desired number of upper address bits. The value programmed into this field specifies the number of lower address bits that are allowed to change. For this circular queue application, the SOFF is typically set to the transfer size to implement post-increment addressing with the SMOD function constraining the addresses to a 0-modulo-size range.
37–39 0x4 [5:7]	SSIZE [0:2]	Source data transfer size. 000 8-bit 001 16-bit 010 32-bit 011 64-bit 100 Reserved 64-bit 101 32-byte burst (64-bit x 4) 110 Reserved 111 Reserved The attempted specification of a ‘reserved’ encoding causes a configuration error.
40–44 0x4 [8:12]	DMOD [0:4]	Destination address modulo. Refer to the SMOD[0:5] definition.
45–47 0x4 [13:15]	DSIZE [0:2]	Destination data transfer size. Refer to the SSIZE[0:2] definition.
48–63 0x4 [16:31]	SOFF [0:15]	Source address signed offset. Sign-extended offset applied to the current source address to form the next-state value as each source read is completed.
64–95 0x8 [0:31]	NBYTES [0:31]	Inner “minor” byte transfer count. Number of bytes to be transferred in each service request of the channel. As a channel is activated, the contents of the appropriate TCD is loaded into the eDMA engine, and the appropriate reads and writes performed until the complete byte transfer count has been transferred. This is an indivisible operation and cannot be stalled or halted. Once the minor count is exhausted, the current values of the SADDR and DADDR are written back into the local memory, the major iteration count is decremented and restored to the local memory. If the major iteration count is completed, additional processing is performed. **Note:** The NBYTES value of 0x0000_0000 is interpreted as 0x1_0000_0000, thus specifying a four GB transfer.

Table 9-19. TCD*n* Field Descriptions (continued)

Bits Word Offset [n:n]	Field Name	Description
96–127 0xC [0:31]	SLAST [0:31]	Last source address adjustment. Adjustment value added to the source address at the completion of the outer major iteration count. This value can be applied to “restore” the source address to the initial value, or adjust the address to reference the next data structure.
128–159 0x10 [0:31]	DADDR [0:31]	Destination address. Memory address pointing to the destination data.
160 0x14 [0]	CITER.E_LINK	Enable channel-to-channel linking on minor loop completion. As the channel completes the inner minor loop, this flag enables the linking to another channel, defined by CITER.LINKCH[0:5]. The link target channel initiates a channel service request via an internal mechanism that sets the TCD.START bit of the specified channel. If channel linking is disabled, the CITER value is extended to 15 bits in place of a link channel number. If the major loop is exhausted, this link mechanism is suppressed in favor of the MAJOR.E_LINK channel linking. 0 The channel-to-channel linking is disabled. 1 The channel-to-channel linking is enabled. **Note:** This bit must be equal to the BITER.E_LINK bit otherwise a configuration error is reported.
161–166 0x14 [1:6]	CITER [0:5] or CITER.LINKCH [0:5]	Current “major” iteration count or link channel number. If channel-to-channel linking is disabled (TCD.CITER.E_LINK = 0), then • No channel-to-channel linking (or chaining) is performed after the inner minor loop is exhausted. TCD bits [161:175] are used to form a 15-bit CITER field. otherwise • After the minor loop is exhausted, the eDMA engine initiates a channel service request at the channel defined by CITER.LINKCH[0:5] by setting that channel’s TCD.START bit.
167–175 0x14 [7:15]	CITER [6:14]	Current “major” iteration count. This 9 or 15-bit count represents the current major loop count for the channel. It is decremented each time the minor loop is completed and updated in the transfer control descriptor memory. After the major iteration count is exhausted, the channel performs a number of operations (for example, final source and destination address calculations), optionally generating an interrupt to signal channel completion before reloading the CITER field from the beginning iteration count (BITER) field. **Note:** When the CITER field is initially loaded by software, it must be set to the same value as that contained in the BITER field. **Note:** If the channel is configured to execute a single service request, the initial values of BITER and CITER must be 0x0001.
176–191 0x14 [16:31]	DOFF [0:15]	Destination address signed offset. Sign-extended offset applied to the current destination address to form the next-state value as each destination write is completed.

Table 9-19. TCD*n* Field Descriptions (continued)

Bits Word Offset [n:n]	Field Name	Description
192–223 0x18 [0:31]	DLAST_SGA [0:31]	Last destination address adjustment or the memory address for the next transfer control descriptor to be loaded into this channel (scatter/gather). If scatter/gather processing for the channel is disabled (TCD.E_SG = 0) then • Adjustment value added to the destination address at the completion of the outer major iteration count. This value can be applied to “restore” the destination address to the initial value, or adjust the address to reference the next data structure. Otherwise • This address points to the beginning of a 0-modulo-32 byte region containing the next transfer control descriptor to be loaded into this channel. This channel reload is performed as the major iteration count completes. The scatter/gather address must be 0-modulo-32 byte, otherwise a configuration error is reported.
224 0x1C [0]	BITER.E_LINK	Enables channel-to-channel linking on minor loop complete. As the channel completes the inner minor loop, this flag enables the linking to another channel, defined by BITER.LINKCH[0:5]. The link target channel initiates a channel service request via an internal mechanism that sets the TCD.START bit of the specified channel. If channel linking is disabled, the BITER value is extended to 15 bits in place of a link channel number. If the major loop is exhausted, this link mechanism is suppressed in favor of the MAJOR.E_LINK channel linking. 0 The channel-to-channel linking is disabled. 1 The channel-to-channel linking is enabled. **Note:** When the TCD is first loaded by software, this field must be set equal to the corresponding CITER field, otherwise a configuration error is reported. As the major iteration count is exhausted, the contents of this field is reloaded into the CITER field.
225–230 0x1C [1:6]	BITER [0:5] or BITER.LINKCH [0:5]	Beginning or starting “major” iteration count or link channel number. If channel-to-channel linking is disabled (TCD.BITER.E_LINK = 0), then • No channel-to-channel linking (or chaining) is performed after the inner minor loop is exhausted. TCD bits [225:239] are used to form a 15-bit BITER field. Otherwise • After the minor loop is exhausted, the eDMA engine initiates a channel service request at the channel, defined by BITER.LINKCH[0:5], by setting that channel’s TCD.START bit. **Note:** When the TCD is first loaded by software, this field must be set equal to the corresponding CITER field, otherwise a configuration error is reported. As the major iteration count is exhausted, the contents of this field is reloaded into the CITER field.
231–239 0x1C [7:15]	BITER [6:14]	Beginning or starting major iteration count. As the transfer control descriptor is first loaded by software, this field must be equal to the value in the CITER field. As the major iteration count is exhausted, the contents of this field is reloaded into the CITER field. **Note:** If the channel is configured to execute a single service request, the initial values of BITER and CITER must be 0x0001.

Table 9-19. TCD*n* Field Descriptions (continued)

Bits Word Offset [n:n]	Field Name	Description
240–241 0x1C [16:17]	BWC [0:1]	Bandwidth control. This two-bit field provides a mechanism to effectively throttle the amount of bus bandwidth consumed by the eDMA. In general, as the eDMA processes the inner minor loop, it continuously generates read/write sequences until the minor count is exhausted. This field forces the eDMA to stall after the completion of each read/write access to control the bus request bandwidth seen by the system bus crossbar switch (XBAR). To minimize start-up latency, bandwidth control stalls are suppressed for the first two system bus cycles and after the last write of each minor loop. 00 No eDMA engine stalls 01 Reserved 10 eDMA engine stalls for four cycles after each r/w 11 eDMA engine stalls for eight cycles after each r/w
242–247 0x1C [18:23]	MAJOR.LINKCH [0:5]	Link channel number. If channel-to-channel linking on major loop complete is disabled (TCD.MAJOR.E_LINK = 0) then: • No channel-to-channel linking (or chaining) is performed after the outer major loop counter is exhausted. Otherwise • After the major loop counter is exhausted, the eDMA engine initiates a channel service request at the channel defined by MAJOR.LINKCH[0:5] by setting that channel's TCD.START bit.
248 0x1C [24]	DONE	Channel done. This flag indicates the eDMA has completed the outer major loop. It is set by the eDMA engine as the CITER count reaches zero; it is cleared by software or hardware when the channel is activated (when the channel has begun to be processed by the eDMA engine, not when the first data transfer occurs). **Note:** This bit must be cleared to write the MAJOR.E_LINK or E_SG bits.
249 0x1C [25]	ACTIVE	Channel active. This flag signals the channel is currently in execution. It is set when channel service begins, and is cleared by the eDMA engine as the inner minor loop completes or if any error condition is detected.
250 0x1C [26]	MAJOR.E_LINK	Enable channel-to-channel linking on major loop completion. As the channel completes the outer major loop, this flag enables the linking to another channel, defined by MAJOR.LINKCH[0:5]. The link target channel initiates a channel service request via an internal mechanism that sets the TCD.START bit of the specified channel. NOTE: To support the dynamic linking coherency model, this field is forced to zero when written to while the TCD.DONE bit is set. 0 The channel-to-channel linking is disabled. 1 The channel-to-channel linking is enabled.
251 0x1C [27]	E_SG	Enable scatter/gather processing. As the channel completes the outer major loop, this flag enables scatter/gather processing in the current channel. If enabled, the eDMA engine uses DLAST_SGA as a memory pointer to a 0-modulo-32 address containing a 32-byte data structure which is loaded as the transfer control descriptor into the local memory. NOTE: To support the dynamic scatter/gather coherency model, this field is forced to zero when written to while the TCD.DONE bit is set. 0 The current channel's TCD is "normal" format. 1 The current channel's TCD specifies a scatter gather format. The DLAST_SGA field provides a memory pointer to the next TCD to be loaded into this channel after the outer major loop completes its execution.

Table 9-19. TCD*n* Field Descriptions (continued)

Bits Word Offset [n:n]	Field Name	Description
252 0x1C [28]	D_REQ	Disable hardware request. If this flag is set, the eDMA hardware automatically clears the corresponding EDMA_ERQH or EDMA_ERQL bit when the current major iteration count reaches zero. 0 The channel's EDMA_ERQH or EDMA_ERQL bit is not affected. 1 The channel's EDMA_ERQH or EDMA_ERQL bit is cleared when the outer major loop is complete.
253 0x1C [29]	INT_HALF	Enable an interrupt when major counter is half complete. If this flag is set, the channel generates an interrupt request by setting the bit in the EDMA_ERQH or EDMA_ERQL when the current major iteration count reaches the halfway point. The eDMA engine performs the compare (CITER == (BITER >> 1)). This halfway point interrupt request supports double-buffered (aka ping-pong) schemes, or where the processor needs an early indication of the data transfer's progress during data movement. CITER = BITER = 1 with INT_HALF enabled generates an interrupt as it satisfies the equation (CITER == (BITER >> 1)) after a single activation. 0 The half-point interrupt is disabled. 1 The half-point interrupt is enabled.
254 0x1C [30]	INT_MAJ	Enable an interrupt when major iteration count completes. If this flag is set, the channel generates an interrupt request by setting the appropriate bit in the EDMA_ERQH or EDMA_ERQL when the current major iteration count reaches zero. 0 The end-of-major loop interrupt is disabled. 1 The end-of-major loop interrupt is enabled.
255 0x1C [31]	START	Channel start. If this flag is set, the channel is requesting service. The eDMA hardware automatically clears this flag after the channel begins execution. 0 The channel is not explicitly started. 1 The channel is explicitly started via a software initiated service request.

9.3 Functional Description

This section provides an overview of the microarchitecture and functional operation of the eDMA module.

9.3.1 eDMA Microarchitecture

The eDMA module is partitioned into two major modules: the eDMA engine and the transfer control descriptor local memory. Additionally, the eDMA engine is further partitioned into four submodules, which are detailed below.

- eDMA engine
  - — *Address path*: This module implements registered versions of two channel transfer control descriptors: channel ‘x’ and channel ‘y,’ and is responsible for all the master bus address calculations. All the implemented channels provide the exact same functionality. This hardware structure allows the data transfers associated with one channel to be preempted after the completion of a read/write sequence if a higher priority channel service request is asserted while the first channel is active. After a channel is activated, it runs until the minor loop is completed unless preempted by a higher priority channel. This capability provides a mechanism (optionally enabled by EDMA_CPR*n*[ECP]) where a large data move operation can be preempted to minimize the time another channel is blocked from execution.

    When any other channel is activated, the contents of its transfer control descriptor is read from the local memory and loaded into the registers of the other address path channel{x,y}. After the inner minor loop completes execution, the address path hardware writes the new values for the TCDn.{SADDR, DADDR, CITER} back into the local memory. If the major iteration count is exhausted, additional processing is performed, including the final address pointer updates, reloading the TCDn.CITER field, and a possible fetch of the next TCD*n* from memory as part of a scatter/gather operation.
  - — *Data path*: This module implements the actual bus master read/write datapath. It includes 32 bytes of register storage (matching the maximum transfer size) and the necessary mux logic to support any required data alignment. The system read data bus is the primary input, and the system write data bus is the primary output.

    The address and data path modules directly support the 2-stage pipelined system bus. The address path module represents the 1st stage of the bus pipeline (the address phase), while the data path module implements the 2nd stage of the pipeline (the data phase).
  - — *Program model/channel arbitration*: This module implements the first section of eDMA’s programming model as well as the channel arbitration logic. The programming model registers are connected to the slave bus (not shown). The eDMA peripheral request inputs and eDMA interrupt request outputs are also connected to this module (via the Control logic).
  - — *Control*: This module provides all the control functions for the eDMA engine. For data transfers where the source and destination sizes are equal, the eDMA engine performs a series of source read, destination write operations until the number of bytes specified in the inner ‘minor loop’ byte count has been moved.

A minor loop interaction is defined as the number of bytes to transfer (*n*bytes) divided by the transfer size. Transfer size is defined as the following:

if (SSIZE < DSIZE)

transfer size = destination transfer size (# of bytes)

else

transfer size = source transfer size (# of bytes)

Minor loop TCD variables are SOFF, SMOD, DOFF, DMOD, NBYTES, SADDR, DADDR, BWC, ACTIVE, AND START. Major loop TCD variables are DLAST, SLAST, CITER, BITER, DONE, D_REQ, INT_MAJ, MAJOR_LNKCH, and INT_HALF.

For descriptors where the sizes are not equal, multiple access of the smaller size data are required for each reference of the larger size. As an example, if the source size references 16-bit data and the destination is 32-bit data, two reads are performed, then one 32-bit write.

- TCD local memory
  - — *Memory controller*: This logic implements the required dual-ported controller, handling accesses from both the eDMA engine as well as references from the slave bus. As noted earlier, in the event of simultaneous accesses, the eDMA engine is given priority and the slave transaction is stalled. The hooks to a BIST controller for the local TCD memory are included in this module.
  - — *Memory array*: The TCD is implemented using a single-ported, synchronous compiled RAM memory array.

9.3.2 eDMA Basic Data Flow

The basic flow of a data transfer can be partitioned into three segments. As shown in Figure 9-24, the first segment involves the channel service request. In the diagram, this example uses the assertion of the eDMA peripheral request signal to request service for channel *n*. Channel service request via software and the TCDn.START bit follows the same basic flow as an eDMA peripheral request. The eDMA peripheral request input signal is registered internally and then routed to through the eDMA engine, first through the control module, then into the program model/channel arbitration module. In the next cycle, the channel arbitration is performed, either using the fixed-priority or round-robin algorithm. After the arbitration is complete, the activated channel number is sent through the address path and converted into the required address to access the TCD local memory. Next, the TCD memory is accessed and the required descriptor read from the local memory and loaded into the eDMA engine address path channel{x,y} registers. The TCD memory is organized 64-bits in width to minimize the time needed to fetch the activated channel's descriptor and load it into the eDMA engine address path channel{x,y} registers.

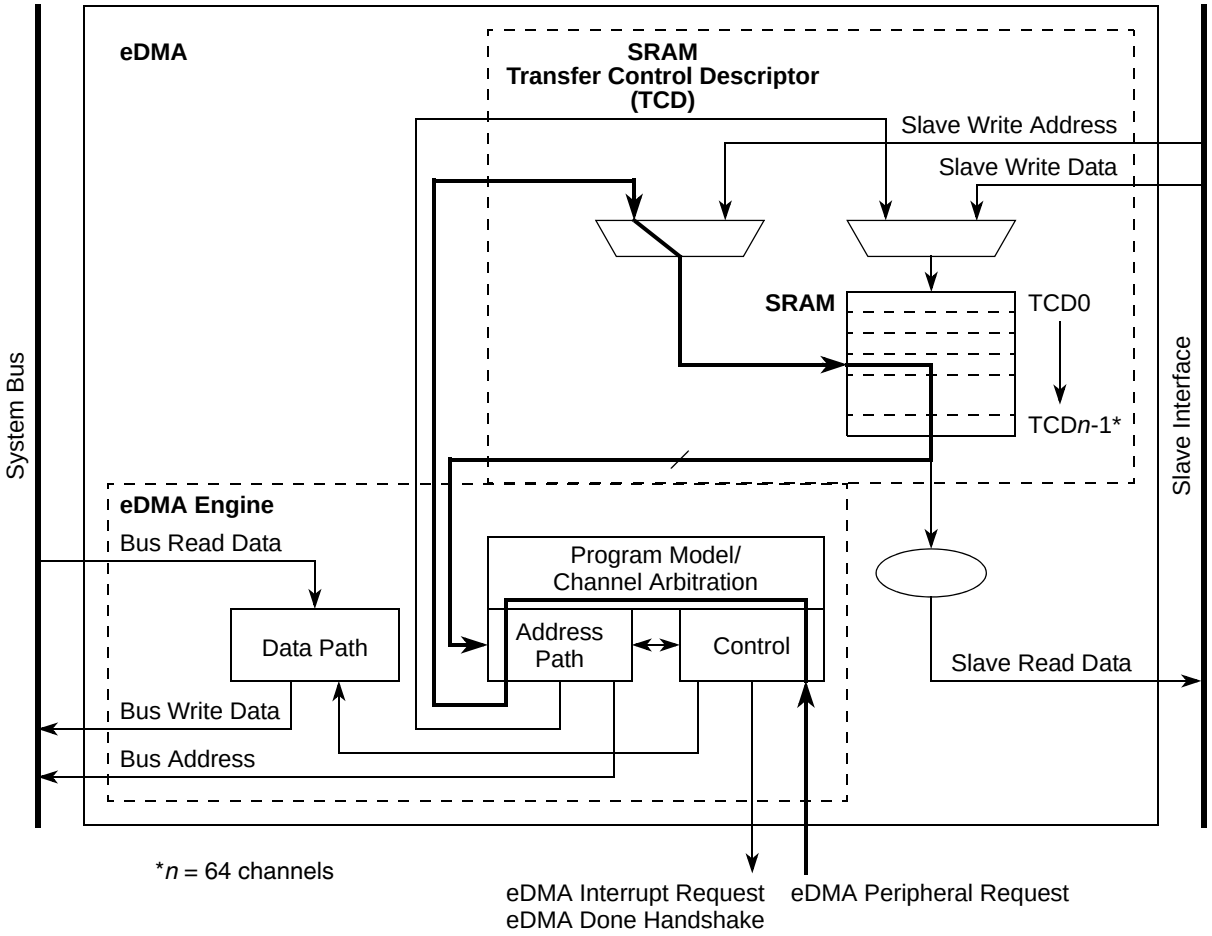


Figure 9-24. eDMA Operation, Part 1

In the second part of the basic data flow as shown in Figure 9-25, the modules associated with the data transfer (address path, data path and control) sequence through the required source reads and destination writes to perform the actual data movement. The source reads are initiated and the fetched data is temporarily stored in the data path module until it is gated onto the system bus during the destination write. This source read/destination write processing continues until the inner minor byte count has been transferred. The eDMA Done Handshake signal is asserted at the end of the minor byte count transfer.

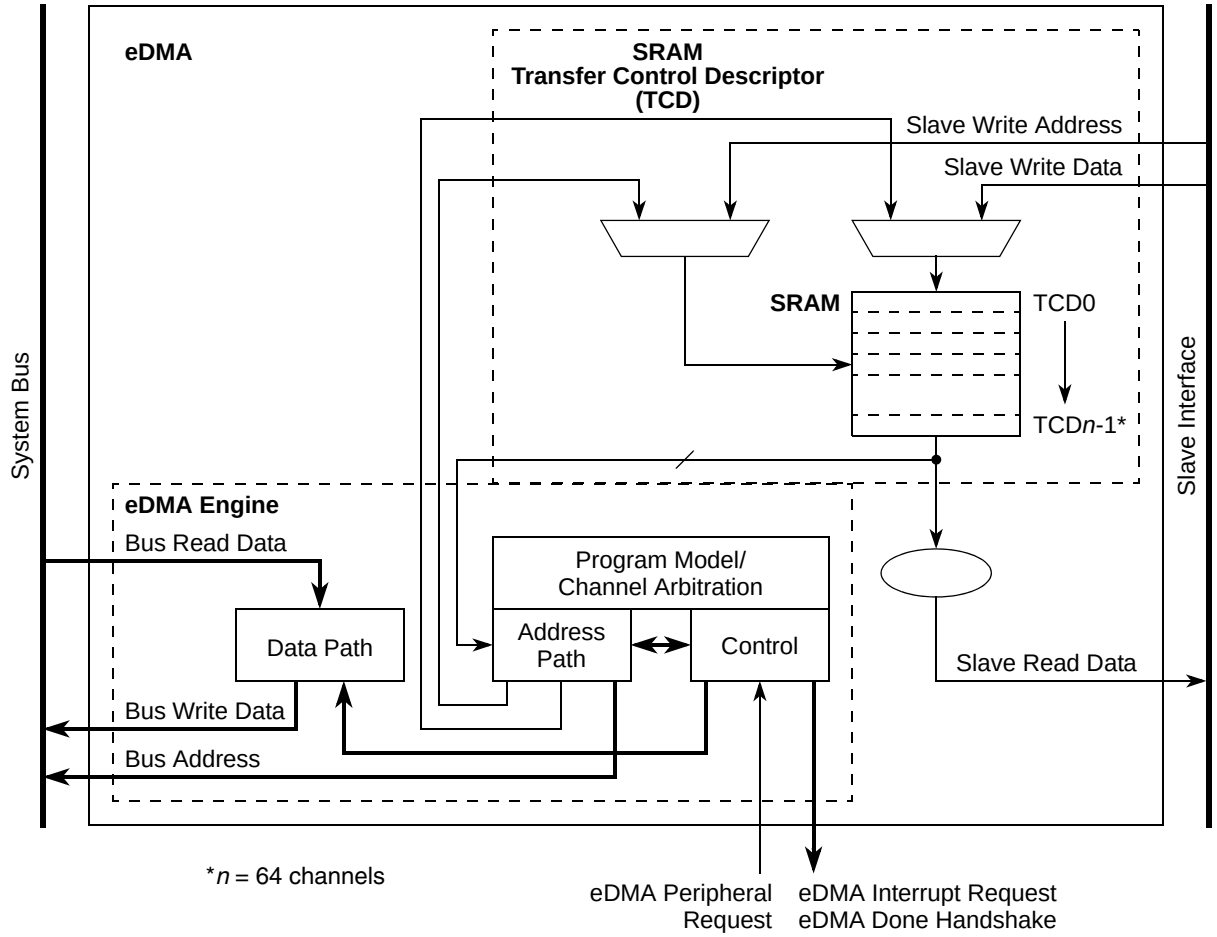


Figure 9-25. eDMA Operation, Part 2

After the inner minor byte count has been moved, the final phase of the basic data flow is performed. In this segment, the address path logic performs the required updates to certain fields in the channel's TCD: for example., SADDR, DADDR, CITER. If the outer major iteration count is exhausted, then there are additional operations which are performed. These include the final address adjustments and reloading of the BITER field into the CITER. Additionally, assertion of an optional interrupt request occurs at this time, as does a possible fetch of a new TCD from memory using the scatter/gather address pointer included in the descriptor. The updates to the TCD memory and the assertion of an interrupt request are shown in Figure 9-26.

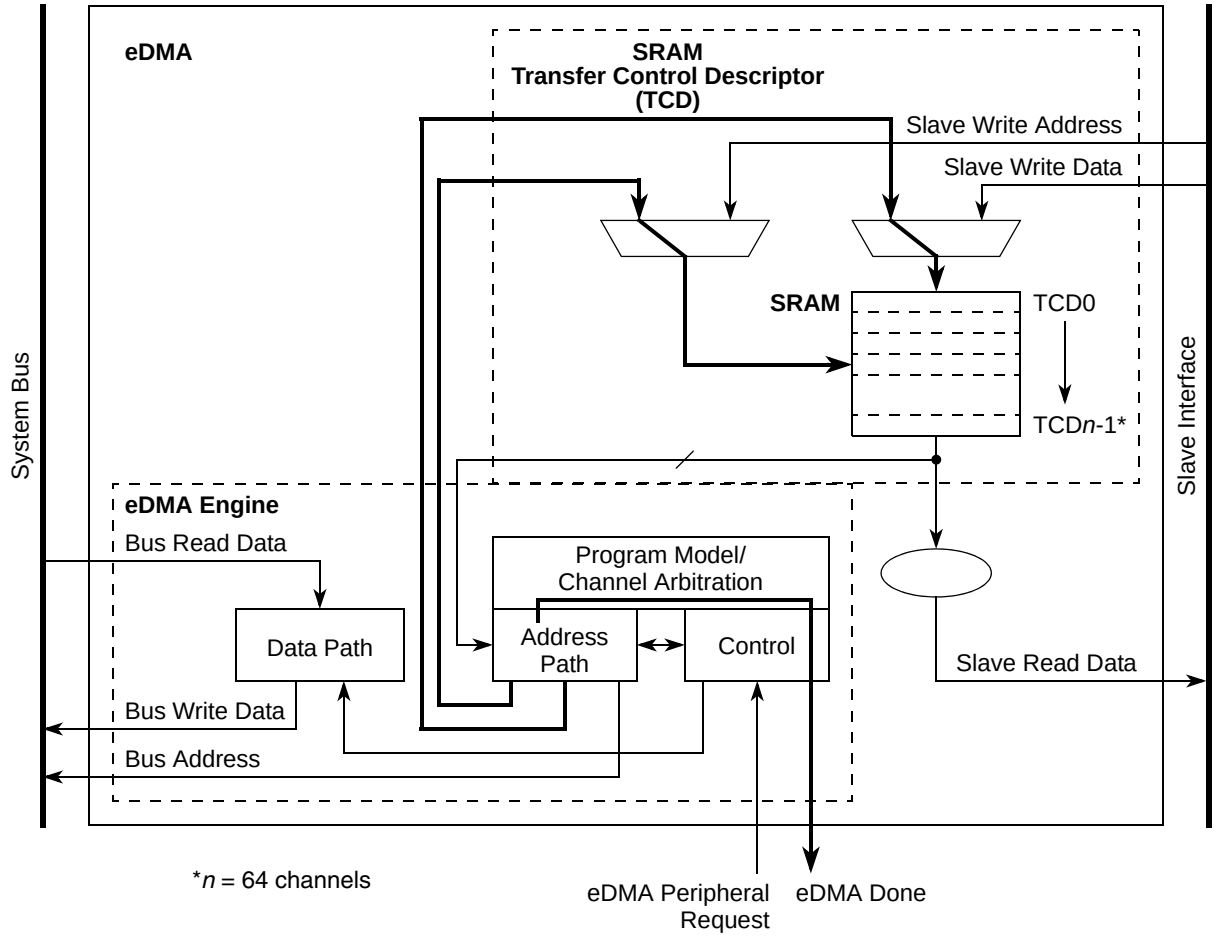


Figure 9-26. eDMA Operation, Part 3

9.3.3 eDMA Performance

This section addresses the performance of the eDMA module, focusing on two separate metrics. In the traditional data movement context, performance is best expressed as the peak data transfer rates achieved using the eDMA. In most implementations, this transfer rate is limited by the speed of the source and destination address spaces. In a second context where device-paced movement of single data values to/from peripherals is dominant, a measure of the requests that can be serviced in a fixed time is a more useful metric. In this environment, the speed of the source and destination address spaces remains important, but the microarchitecture of the eDMA also factors significantly into the resulting metric.

The peak transfer rates for several different source and destination transfers are shown in Table 9-20. The following assumptions apply to Table 9-20 and Table 9-21:

- Internal SRAM can be accessed with zero wait-states when viewed from the system bus data phase.
- All slave reads require two wait-states, and slave writes three wait-states, again viewed from the system bus data phase.
- All slave accesses are 32-bits in size.

Table 9-20. eDMA Peak Transfer Rates (MB/Sec)

System Speed, Transfer Size	Internal SRAM-to-Internal SRAM	32-Bit Slave-to-Internal SRAM	Internal SRAM-to-32-Bit Slave (buffering disabled)	Internal SRAM-to-32-Bit Slave (buffering enabled)
66.7 MHz, 32 bit	66.7	66.7	53.3	88.7
66.7 MHz, 64 bit	133.3	66.7	53.3	88.7
66.7 MHz, 256 bit[1]	213.4	N/A[2]	N/A[2]	N/A[2]
83.3 MHz, 32 bit	83.3	83.3	66.7	110.8
83.3 MHz, 64 bit	166.7	83.3	66.7	110.8
83.3 MHz, 256 bit[1]	266.6	N/A[2]	N/A[2]	N/A[2]
100.0 MHz, 32 bit	100.0	100.0	80.0	133.0
100.0 MHz, 64 bit	200.0	100.0	80.0	133.0
100.0 MHz, 256 bit[1]	320.0	N/A[2]	N/A[2]	N/A[2]
132.0 MHz, 32 bit	132.0	132.0	105.6	175.6
132.0 MHz, 64 bit	264.0	132.0	105.6	175.6
132.0 MHz, 256 bit[1]	422.4	N/A[2]	N/A[2]	N/A[2]

1 A 256-bit transfer occurs as a burst of four 64-bit beats.

2 Not applicable: burst access to a slave port is not supported.

Table 9-20 presents a peak transfer rate comparison, measured in MBs per second where the internal-SRAM-to-internal-SRAM transfers occur at the core's datapath width; that is, either 32- or 64-bits per access. For all transfers involving the slave bus, 32-bit transfer sizes are used. In all cases, the transfer rate includes the time to read the source plus the time to write the destination.

The second performance metric is a measure of the number of DMA requests that can be serviced in a given amount of time. For this metric, it is assumed the peripheral request causes the channel to move a single slave-mapped operand to/from internal SRAM. The same timing assumptions used in the previous example apply to this calculation. In particular, this metric also reflects the time required to activate the channel. The eDMA design supports the following hardware service request sequence:

- Cycle 1: eDMA peripheral request is asserted.
- Cycle 2: The eDMA peripheral request is registered locally in the eDMA module and qualified. (TCD.START bit initiated requests start at this point with the registering of the slave write to TCD bit 255).
- Cycle 3: Channel arbitration begins.
- Cycle 4: Channel arbitration completes. The transfer control descriptor local memory read is initiated.
- Cycle 5–6: The first two parts of the activated channel's TCD is read from the local memory. The memory width to the eDMA engine is 64 bits, so the entire descriptor can be accessed in four cycles.

- Cycle 7: The first system bus read cycle is initiated, as the third part of the channel's TCD is read from the local memory. Depending on the state of the crossbar switch, arbitration at the system bus can insert an additional cycle of delay here.
- Cycle 8 – *n*: The last part of the TCD is read in. This cycle represents the 1st data phase for the read, and the address phase for the destination write.

  The exact timing from this point is a function of the response times for the channel's read and write accesses. In this case of an slave read and internal SRAM write, the combined data phase time is 4 cycles. For an SRAM read and slave write, it is 5 cycles.
- Cycle *n* + 1: This cycle represents the data phase of the last destination write.
- Cycle *n* + 2: The eDMA engine completes the execution of the inner minor loop and prepares to write back the required TCD*n* fields into the local memory. The control/status fields at word offset 0x1C in TCD*n* are read. If the major loop is complete, the MAJOR.E_LINK and E_SG bits are checked and processed if enabled.
- Cycle *n* + 3: The appropriate fields in the first part of the TCD*n* are written back into the local memory.
- Cycle *n* + 4: The fields in the second part of the TCD*n* are written back into the local memory. This cycle coincides with the next channel arbitration cycle start.
- Cycle *n* + 5: The next channel to be activated performs the read of the first part of its TCD from the local memory. This is equivalent to Cycle 4 for the first channel's service request.

Assuming zero wait states on the system bus, DMA requests can be processed every 9 cycles. Assuming an average of the access times associated with slave-to-SRAM (4 cycles) and SRAM-to-slave (5 cycles), DMA requests can be processed every 11.5 cycles (4 + (4+5)/2 + 3). This is the time from Cycle 4 to Cycle "*n* + 5." The resulting peak request rate, as a function of the system frequency, is shown in Table 9-21. This metric represents millions of requests per second.

Table 9-21. eDMA Peak Request Rate (MReq/Sec)

System Frequency (MHz)	Request Rate (Zero Wait States)	Request Rate (with Wait States)
66.6	7.4	5.8
83.3	9.2	7.2
100.0	11.1	8.7
133.3	14.8	11.6
150.0	16.6	13.0

A general formula to compute the peak request rate (with overlapping requests) is:

PEAKreq = freq / [entry + (1 + read_ws) + (1 + write_ws) + exit]

where:

PEAKreq – peak request rate

freq – system frequency

entry – channel startup (four cycles)

read_ws – wait states seen during the system bus read data phase

write_ws – wait states seen during the system bus write data phase

exit – channel shutdown (three cycles)

For example: consider a system with the following characteristics:

- Internal SRAM can be accessed with one wait-state when viewed from the system bus data phase.
- All slave reads require two wait-states, and slave writes three wait-states, again viewed from the system bus data phase.
- System operates at 150 MHz.

For an SRAM to slave transfer,

PEAKreq = 150 MHz / [4 + (1 + 1) + (1 + 3) + 3] cycles = 11.5 Mreq/sec

For an slave to SRAM transfer,

PEAKreq = 150 MHz / [4 + (1 + 2) + (1 + 1) + 3] cycles = 12.5 Mreq/sec

Assuming an even distribution of the two transfer types, the average peak request rate is:

PEAKreq = (11.5 Mreq/sec + 12.5 Mreq/sec) / 2 = 12.0 Mreq/sec

The minimum number of cycles to perform a single read/write, zero wait states on the system bus, from a cold start (no channel is executing, eDMA is idle) are the following:

- 11 cycles for a software (TCD.START bit) request
- 12 cycles for a hardware (eDMA peripheral request signal) request

Two cycles account for the arbitration pipeline and one extra cycle on the hardware request resulting from the internal registering of the eDMA peripheral request signals. For the peak request rate calculations above, the arbitration and request registering is absorbed in or overlap the previous executing channel.

NOTE

When channel linking or scatter/gather is enabled, a two-cycle delay is imposed on the next channel selection and startup. This allows the link channel or the scatter/gather channel to be eligible and considered in the arbitration pool for next channel selection.

9.4 Initialization and Application Information

9.4.1 eDMA Initialization

A typical initialization of the eDMA has the following sequence:

1. Write the EDMA_CR if a configuration other than the default is desired.
2. Write the channel priority levels into the EDMA_CPR*n* registers if a configuration other than the default is desired.
3. Enable error interrupts in the EDMA_EEIRL and/or EDMA_EEIRH registers (optional).

4. Write the 32-byte TCD for each channel that can request service.
5. Enable any hardware service requests via the EDMA_ERQRH and/or EDMA_ERQRL registers.
6. Request channel service by either software (setting the TCD.START bit) or by hardware (slave device asserting its eDMA peripheral request signal).

After any channel requests service, a channel is selected for execution based on the arbitration and priority levels written into the programmer's model. The eDMA engine reads the entire TCD, including the primary transfer control parameter shown in Table 9-22, for the selected channel into its internal address path module. As the TCD is being read, the first transfer is initiated on the system bus unless a configuration error is detected. Transfers from the source (as defined by the source address, TCD.SADDR) to the destination (as defined by the destination address, TCD.DADDR) continue until the specified number of bytes (TCD.NBYTES) have been transferred. When the transfer is complete, the eDMA engine's local TCD.SADDR, TCD.DADDR, and TCD.CITER are written back to the main TCD memory and any minor loop channel linking is performed, if enabled. If the major loop is exhausted, further post processing is executed: for example, interrupts, major loop channel linking, and scatter/gather operations, if enabled.

Table 9-22. TCD Primary Control and Status Fields

TCD Field Name	Description
START	Control bit to explicitly start channel when using a software initiated DMA service (Automatically cleared by hardware)
ACTIVE	Status bit indicating the channel is currently in execution
DONE	Status bit indicating major loop completion (Cleared by software when using a software initiated DMA service)
D_REQ	Control bit to disable DMA request at end of major loop completion when using a hardware-initiated DMA service
BWC	Control bits for “throttling” bandwidth control of a channel
E_SG	Control bit to enable scatter-gather feature
INT_HALF	Control bit to enable interrupt when major loop is half complete
INT_MAJ	Control bit to enable interrupt when major loop completes

Figure 9-27 shows how each DMA request initiates one minor loop transfer (iteration) without CPU intervention. DMA arbitration can occur after each minor loop, and one level of minor loop DMA preemption is allowed. The number of minor loops in a major loop is specified by the beginning iteration count (biter).

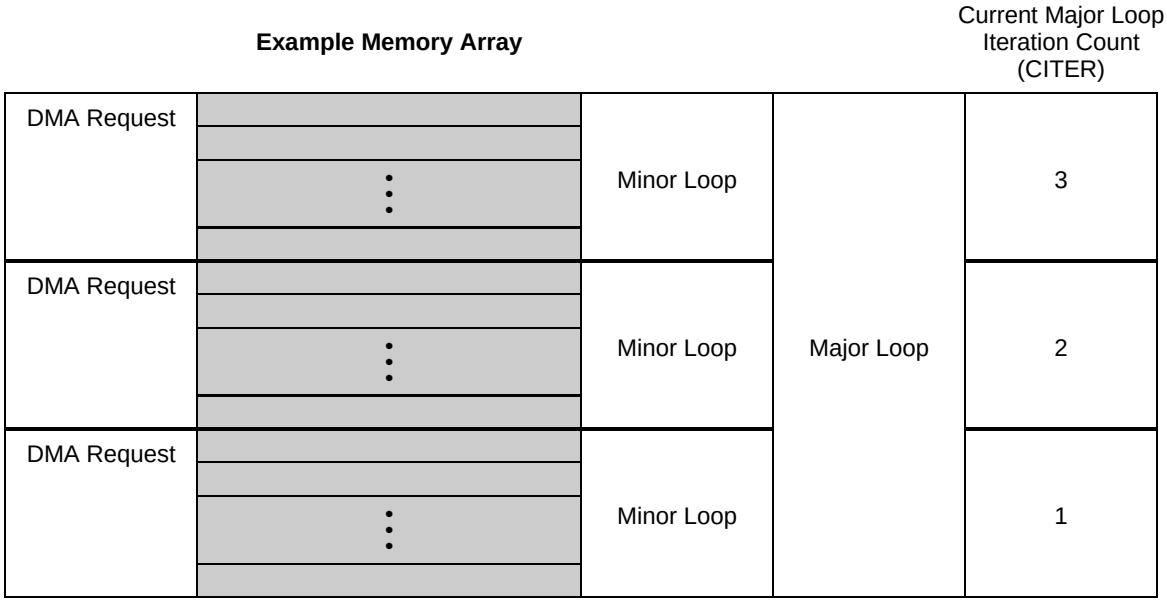


Figure 9-27. Example of Multiple Loop Iterations

Figure 9-28 lists the memory array terms and how the TCD settings interrelate.

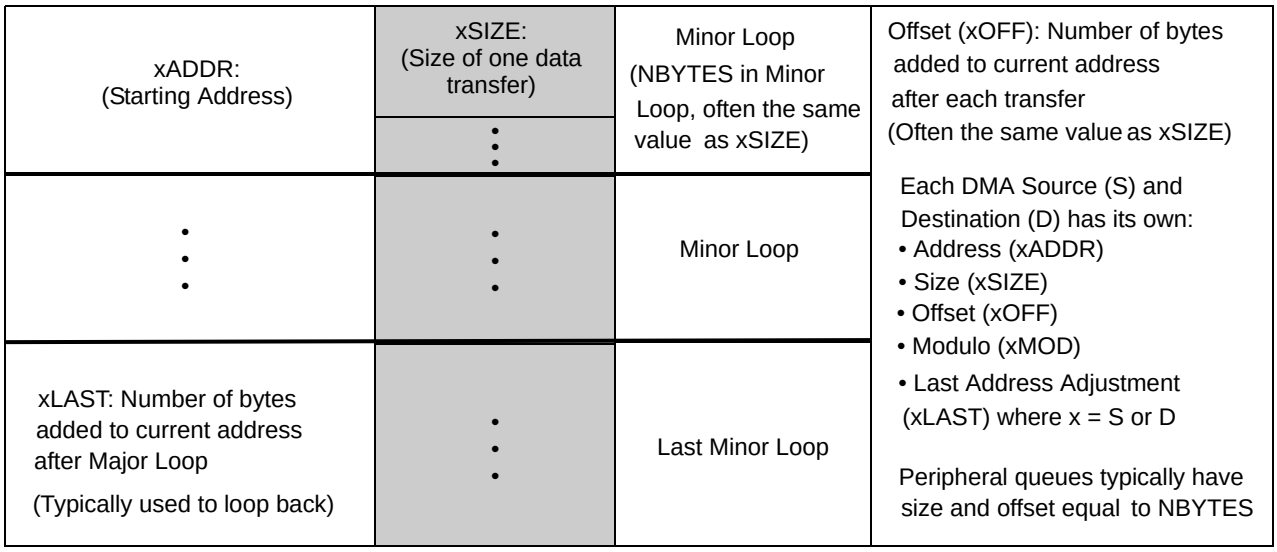


Figure 9-28. Memory Array Terms

9.4.2 DMA Programming Errors

The eDMA performs various tests on the transfer control descriptor to verify consistency in the descriptor data. Most programming errors are reported on a per channel basis with the exception of two errors: group priority error and channel priority error, or EDMA_ESR[GPE] and EDMA_ESR[CPE], respectively.

For all error types other than group or channel priority errors, the channel number causing the error is recorded in the EDMA_ESR. If the error source is not removed before the next activation of the problem channel, the error is detected and recorded again.

Channel priority errors are identified within a group after that group has been selected as the active group. For the example that follows, all of the channel priorities in Group 1 are unique, but some of the channel priorities in Group 0 are the same:

1. Configure the eDMA for fixed-group and fixed-channel arbitration modes.
2. Group 1 is the highest priority and all channels are unique in that group.
3. Group 0 is the next highest priority and two channels have the same priority level.
4. If Group 1 has service requests pending, those requests are executed.
5. After all Group 1 requests have completed, Group 0 becomes the active group.
6. If Group 0 has a service request, the eDMA selects the undefined channel in Group 0 and generates a channel priority error.
7. Repeat Step 6 until the all Group 0 requests are serviced or a higher-priority Group 1 request is received.

In step 2, the eDMA acknowledge lines assert only if the selected channel is requesting service via the eDMA peripheral request signal. If interrupts are enabled for all channels, an error interrupt is generated. However, the channel number for the EDMA_ER and the error interrupt request line contain undefined data because the channel is ‘undefined’. A group priority error is global and any request in any group causes a group priority error.

If priority levels are not unique, the highest (channel/group) priority that has an active request is selected, but the lowest numbered (channel/group) with that priority is selected by arbitration and executed by the eDMA engine. The hardware service request handshake signals, error interrupts and error reporting are associated with the selected channel.

9.4.3 DMA Request Assignments

The assignments between the DMA requests from the modules to the channels of the eDMA are shown in Table 9-23. The source column is written in C language syntax. The syntax is module_instance.register[bit].

Table 9-23. DMA Request Summary for eDMA

DMA Request	Channel	Source	Description
eQADC_FISR0_CFFF0	0	EQADC.FISR0[CFFF0]	eQADC Command FIFO 0 Fill Flag
eQADC_FISR0_RFDF0	1	EQADC.FISR0[RFDF0]	eQADC Receive FIFO 0 Drain Flag
eQADC_FISR1_CFFF1	2	EQADC.FISR1[CFFF1]	eQADC Command FIFO 1 Fill Flag
eQADC_FISR1_RFDF1	3	EQADC.FISR1[RFDF1]	eQADC Receive FIFO 1 Drain Flag
eQADC_FISR2_CFFF2	4	EQADC.FISR2[CFFF2]	eQADC Command FIFO 2 Fill Flag
eQADC_FISR2_RFDF2	5	EQADC.FISR2[RFDF2]	eQADC Receive FIFO 2 Drain Flag
eQADC_FISR3_CFFF3	6	EQADC.FISR3[CFFF3]	eQADC Command FIFO 3 Fill Flag

Table 9-23. DMA Request Summary for eDMA (continued)

DMA Request	Channel	Source	Description
eQADC_FISR3_RFDF3	7	EQADC.FISR3[RFDF3]	eQADC Receive FIFO 3 Drain Flag
eQADC_FISR4_CFFF4	8	EQADC.FISR4[CFFF4]	eQADC Command FIFO 4 Fill Flag
eQADC_FISR4_RFDF4	9	EQADC.FISR4[RFDF4]	eQADC Receive FIFO 4 Drain Flag
eQADC_FISR5_CFFF5	10	EQADC.FISR5[CFFF5]	eQADC Command FIFO 5 Fill Flag
eQADC_FISR5_RFDF5	11	EQADC.FISR5[RFDF5]	eQADC Receive FIFO 5 Drain Flag
DSPIB_SR_TFFF	12	DSPIB.SR[TFFF]	DSPIB Transmit FIFO Fill Flag
DSPIB_SR_RFDF	13	DSPIB.SR[RFDF]	DSPIB Receive FIFO Drain Flag
DSPIC_SR_TFFF	14	DSPIC.SR[TFFF]	DSPIC Transmit FIFO Fill Flag
DSPIC_SR_RFDF	15	DSPIC.SR[RFDF]	DSPIC Receive FIFO Drain Flag
DSPID_SR_TFFF	16	DSPID.SR[TFFF]	DSPID Transmit FIFO Fill Flag
DSPID_SR_RFDF	17	DSPID.SR[RFDF]	DSPID Receive FIFO Drain Flag
eSCIA_COMBTX	18	ESCIA.SR[TDRE] || ESCIA.SR[TC] || ESCIA.SR[TXRDY]	eSCIA combined DMA request of the Transmit Data Register Empty, Transmit Complete, and LIN Transmit Data Ready DMA requests
eSCIA_COMBRX	19	ESCIA.SR[RDRF] || ESCIA.SR[RXRDY]	eSCIA combined DMA request of the Receive Data Register Full and LIN Receive Data Ready DMA requests
eMIOS_GFR_F0	20	EMIOS.GFR[F0]	eMIOS channel 0 Flag
eMIOS_GFR_F1	21	EMIOS.GFR[F1]	eMIOS channel 1 Flag
eMIOS_GFR_F2	22	EMIOS.GFR[F2]	eMIOS channel 2 Flag
eMIOS_GFR_F3	23	EMIOS.GFR[F3]	eMIOS channel 3 Flag
eMIOS_GFR_F4	24	EMIOS.GFR[F4]	eMIOS channel 4 Flag
eMIOS_GFR_F8	25	EMIOS.GFR[F8]	eMIOS channel 8 Flag
eMIOS_GFR_F9	26	EMIOS.GFR[F9]	eMIOS channel 9 Flag
eTPU_CDTRSR_A_DTRS0	27	ETPU.CDTRSR_A[DTRS0]	eTPUA Channel 0 Data Transfer Request Status
eTPU_CDTRSR_A_DTRS1	28	ETPU.CDTRSR_A[DTRS1]	eTPUA Channel 1 Data Transfer Request Status
eTPU_CDTRSR_A_DTRS2	29	ETPU.CDTRSR_A[DTRS2]	eTPUA Channel 2 Data Transfer Request Status
eTPU_CDTRSR_A_DTRS14	30	ETPU.CDTRSR_A[DTRS14]	eTPUA Channel 14 Data Transfer Request Status
eTPU_CDTRSR_A_DTRS15	31	ETPU.CDTRSR_A[DTRS15]	eTPUA Channel 15 Data Transfer Request Status
DSPIA_SR_TFFF	32	DSPIAISR[TFFF]	DSPIA Transmit FIFO Fill Flag
DSPIA_SR_RFDF	33	DSPIA.SR[RFDF]	DSPIA Receive FIFO Drain Flag
eSCIB_COMBTX	34	ESCIB.SR[TDRE] || ESCIB.SR[TC] || ESCIB.SR[TXRDY]	eSCIB combined DMA request of the Transmit Data Register Empty, Transmit Complete, and LIN Transmit Data Ready DMA requests

Table 9-23. DMA Request Summary for eDMA (continued)

DMA Request	Channel	Source	Description
eSCIB_COMBRX	35	ESCIB.SR[RDRF] || ESCIB.SR[RXRDY]	eSCIB combined DMA request of the Receive Data Register Full and LIN Receive Data Ready DMA requests
eMIOS_GFR_F6	36	EMIOS.GFR[F6]	eMIOS channel 6 Flag
eMIOS_GFR_F7	37	EMIOS.GFR[F7]	eMIOS channel 7 Flag
eMIOS_GFR_F10	38	EMIOS.GFR[F10]	eMIOS channel 10 Flag
eMIOS_GFR_F11	39	EMIOS.GFR[F11]	eMIOS channel 11 Flag
eMIOS_GFR_F16	40	EMIOS.GFR[F16]	eMIOS channel 16 Flag
eMIOS_GFR_F17	41	EMIOS.GFR[F17]	eMIOS channel 17 Flag
eMIOS_GFR_F18	42	EMIOS.GFR[F18]	eMIOS channel 18 Flag
eMIOS_GFR_F19	43	EMIOS.GFR[F19]	eMIOS channel 19 Flag
eTPU_CDTRSR_A_DTRS12	44	ETPU.CDTRSR_A[DTRS12]	eTPUA Channel 12 Data Transfer Request Status
eTPU_CDTRSR_A_DTRS13	45	ETPU.CDTRSR_A[DTRS13]	eTPUA Channel 13 Data Transfer Request Status
eTPU_CDTRSR_A_DTRS28	46	ETPU.CDTRSR_A[DTRS28]	eTPUA Channel 28 Data Transfer Request Status
eTPU_CDTRSR_A_DTRS29	47	ETPU.CDTRSR_A[DTRS29]	eTPUA Channel 29 Data Transfer Request Status
SIU_EISR_EIF0	48	SIU.SIU_EISR[EIF0]	SIU External Interrupt Flag 0
SIU_EISR_EIF1	49	SIU.SIU_EISR[EIF1]	SIU External Interrupt Flag 1
SIU_EISR_EIF2	50	SIU.SIU_EISR[EIF2]	SIU External Interrupt Flag 2
SIU_EISR_EIF3	51	SIU.SIU_EISR[EIF3]	SIU External Interrupt Flag 3
eTPU_CDTRSR_B_DTRS0	52	ETPU.CDTRSR_B[DTRS0]	eTPUB Channel 0 Data Transfer Request Status
eTPU_CDTRSR_B_DTRS1	53	ETPU.CDTRSR_B[DTRS1]	eTPUB Channel 1 Data Transfer Request Status
eTPU_CDTRSR_B_DTRS2	54	ETPU.CDTRSR_B[DTRS2]	eTPUB Channel 2 Data Transfer Request Status
eTPU_CDTRSR_B_DTRS3	55	ETPU.CDTRSR_B[DTRS3]	eTPUB Channel 3 Data Transfer Request Status
eTPU_CDTRSR_B_DTRS12	56	ETPU.CDTRSR_B[DTRS12]	eTPUB Channel 12 Data Transfer Request Status
eTPU_CDTRSR_B_DTRS13	57	ETPU.CDTRSR_B[DTRS13]	eTPUB Channel 13 Data Transfer Request Status
eTPU_CDTRSR_B_DTRS14	58	ETPU.CDTRSR_B[DTRS14]	eTPUB Channel 14 Data Transfer Request Status
eTPU_CDTRSR_B_DTRS15	59	ETPU.CDTRSR_B[DTRS15]	eTPUB Channel 15 Data Transfer Request Status
eTPU_CDTRSR_B_DTRS28	60	ETPU.CDTRSR_B[DTRS28]	eTPUB Channel 28 Data Transfer Request Status
eTPU_CDTRSR_B_DTRS29	61	ETPU.CDTRSR_B[DTRS29]	eTPUB Channel 29 Data Transfer Request Status
eTPU_CDTRSR_B_DTRS30	62	ETPU.CDTRSR_B[DTRS30]	eTPUB Channel 30 Data Transfer Request Status
eTPU_CDTRSR_B_DTRS31	63	ETPU.CDTRSR_B[DTRS31]	eTPUB Channel 31 Data Transfer Request Status

9.4.4 DMA Arbitration Mode Considerations

9.4.4.1 Fixed-Group Arbitration and Fixed-Channel Arbitration

In this mode, the channel service request from the highest priority channel in the highest priority group is selected to execute. If the eDMA is programmed so the channels within one group use ‘fixed’ priorities, and that group is assigned the highest ‘fixed’ priority of all groups, it is possible for that group to take all the bandwidth of the eDMA controller; that is, no other groups is serviced if there is always at least one DMA request pending on a channel in the highest priority group when the controller arbitrates the next DMA request. The advantage of this scenario is that latency can be small for channels that need to be serviced quickly. Preemption is available in this scenario only.

9.4.4.2 Round-Robin Group Arbitration, Fixed-Channel Arbitration

The occurrence of one or more DMA requests from one or more groups, the channel with the highest priority from a specific group is serviced first. Groups are serviced starting with the highest group number with a service request and rotating through to the lowest group number containing a service request.

After the channel request is serviced, the group round-robin algorithm selects the highest pending request from the next group in the round-robin sequence. Servicing continues using the round-robin method, always servicing the highest priority channel in the next group in the sequence, or just skipping a group if it has no pending requests.

If a channel requests service at a rate that equals or exceeds the round-robin service rate, then that channel is always serviced before lower priority channels in the same group, and thus the lower priority channels never are serviced. The advantage of this scenario is that no one group uses all the eDMA bandwidth. The highest priority channel selection latency is potentially greater than fixed/fixed arbitration. Excessive request rates on high priority channels can prevent the servicing of lower priority channels in the same group.

9.4.4.3 Round-Robin Group Arbitration, Round-Robin Channel Arbitration

Groups are serviced as described in Section 9.4.4.2, “Round-Robin Group Arbitration, Fixed-Channel Arbitration, but this time channels are serviced in channel number order. Only one channel is serviced from each requesting group for each round-robin pass through the groups.

Within each group, channels are serviced starting with the highest channel number and rotating through to the lowest channel number without regard to channel priority levels.

Because channels are serviced using a round-robin method, any channel that generates DMA requests faster than a combination of the group round-robin service rate and the channel service rate for its group does not prevent the servicing of other channels in its group.

This scenario ensures that all channels are guaranteed service at some point, regardless of the request rates. However, the potential latency can be quite high. All channels are treated equally. Priority levels are not used in round-robin/round-robin mode.

9.4.4.4 Fixed-Group Arbitration, Round-Robin Channel Arbitration

The highest priority group with a request is serviced. Lower priority groups are serviced if no pending requests exist in the higher priority groups.

Within each group, channels are serviced starting with the highest channel number and rotating through to the lowest channel number without regard to the channel priority levels assigned within the group.

This can cause the same bandwidth problem indicated in Section 9.4.4.1, but all the channels in the highest priority group are serviced. Service latency is short on the highest-priority group, but increases as the group priority decreases.

9.4.5 DMA Transfer

9.4.5.1 Single Request

To perform a simple transfer of '*n*' bytes of data with one activation, set the major loop to 1 (TCD.CITER = TCD.BITER = 1). The data transfer begins after the channel service request is acknowledged and the channel is selected to execute. After the transfer completes, the TCD.DONE bit is set and an interrupt is generated if correctly enabled.

For example, the following TCD entry is configured to transfer 16 bytes of data. The eDMA is programmed for one iteration of the major loop transferring 16 bytes per iteration. The source memory has a byte-wide memory port located at 0x1000. The destination memory has a word-wide port located at 0x2000. The address offsets are programmed in increments to match the size of the transfer; one byte for the source and four bytes for the destination. The final source and destination addresses are adjusted to return to their beginning values.

TCD.CITER = TCD.BITER = 1
TCD.NBYTES = 16
TCD.SADDR = 0x1000
TCD.SOFF = 1
TCD.SSIZE = 0
TCD.SLAST = –16
TCD.DADDR = 0x2000
TCD.DOFF = 4
TCD.DSIZE = 2
TCD.DLAST_SGA= –16
TCD.INT_MAJ = 1
TCD.START = 1 (Initialize all other fields before writing to this bit)
All other TCD fields = 0

This generates the following sequence of events:

1. Slave write to the TCD.START bit requests channel service.
2. The channel is selected by arbitration for servicing.

3. eDMA engine writes: TCD.DONE = 0, TCD.START = 0, TCD.ACTIVE = 1.
4. eDMA engine reads: channel TCD data from local memory to internal register file.
5. The source to destination transfers are executed as follows:
   a) read_byte (0x1000), read_byte(0x1001), read_byte(0x1002), read_byte(0x1003)
   b) write_word (0x2000) -> first iteration of the minor loop
   c) read_byte (0x1004), read_byte(0x1005), read_byte(0x1006), read_byte(0x1007)
   d) write_word (0x2004) -> second iteration of the minor loop
   e) read_byte (0x1008), read_byte(0x1009), read_byte(0x100a), read_byte(0x100b)
   f) write_word (0x2008) -> third iteration of the minor loop
   g) read_byte (0x100c), read_byte(0x100d), read_byte(0x100e), read_byte(0x100f)
   h) write_word (0x200c) -> last iteration of the minor loop -> major loop complete
6. eDMA engine writes: TCD.SADDR = 0x1000, TCD.DADDR = 0x2000, TCD.CITER = 1 (TCD.BITER).
7. eDMA engine writes: TCD.ACTIVE = 0, TCD.DONE = 1, EDMA_IRQR*n* = 1.
8. The channel retires.

The eDMA goes idle or services the next channel.

9.4.5.2 Multiple Requests

The next example is the same as previous with the exception of transferring 32 bytes via two hardware requests. The only fields that change are the major loop iteration count and the final address offsets. The eDMA is programmed for two iterations of the major loop transferring 16 bytes per iteration. After the channel's hardware requests are enabled in the EDMA_ERQR, channel service requests are initiated by the slave device (set ERQR after TCD; TCD.START = 0).

TCD.CITER = TCD.BITER = 2

TCD.NBYTES = 16

TCD.SADDR = 0x1000

TCD.SOFF = 1

TCD.SSIZE = 0

TCD.SLAST = –32

TCD.DADDR = 0x2000

TCD.DOFF = 4

TCD.DSIZE = 2

TCD.DLAST_SGA= –32

TCD.INT_MAJ = 1

TCD.START = 0 (Initialize all other fields before writing this bit.)

All other TCD fields = 0

This generates the following sequence of events:

1. First hardware (eDMA peripheral request) request for channel service.
2. The channel is selected by arbitration for servicing.
3. eDMA engine writes: TCD.DONE = 0, TCD.START = 0, TCD.ACTIVE = 1.
4. eDMA engine reads: channel TCD data from local memory to internal register file.
5. The source to destination transfers execute as follows:
   a) read_byte (0x1000), read_byte (0x1001), read_byte (0x1002), read_byte (0x1003)
   b) write_word (0x2000) -> first iteration of the minor loop
   c) read_byte (0x1004), read_byte (0x1005), read_byte (0x1006), read_byte (0x1007)
   d) write_word (0x2004) -> second iteration of the minor loop
   e) read_byte (0x1008), read_byte (0x1009), read_byte (0x100a), read_byte (0x100b)
   f) write_word (0x2008) -> third iteration of the minor loop
   g) read_byte (0x100c), read_byte (0x100d), read_byte (0x100e), read_byte (0x100f)
   h) write_word (0x200c) -> last iteration of the minor loop
6. eDMA engine writes: TCD.SADDR = 0x1010, TCD.DADDR = 0x2010, TCD.CITER = 1.
7. eDMA engine writes: TCD.ACTIVE = 0.
8. The channel retires -> one iteration of the major loop.

The eDMA goes idle or services the next channel.

9. Second hardware (eDMA peripheral request) requests channel service.
10. The channel is selected by arbitration for servicing.
11. eDMA engine writes: TCD.DONE = 0, TCD.START = 0, TCD.ACTIVE = 1.
12. eDMA engine reads: channel TCD data from local memory to internal register file.
13. The source to destination transfers execute as follows:
    a) read_byte (0x1010), read_byte (0x1011), read_byte (0x1012), read_byte (0x1013)
    b) write_word (0x2010) -> first iteration of the minor loop
    c) read_byte (0x1014), read_byte (0x1015), read_byte (0x1016), read_byte (0x1017)
    d) write_word (0x2014) -> second iteration of the minor loop
    e) read_byte (0x1018), read_byte (0x1019), read_byte (0x101a), read_byte (0x101b)
    f) write_word (0x2018) -> third iteration of the minor loop
    g) read_byte (0x101c), read_byte (0x101d), read_byte (0x101e), read_byte (0x101f)
    h) write_word (0x201c) -> last iteration of the minor loop -> major loop complete
14. eDMA engine writes: TCD.SADDR = 0x1000, TCD.DADDR = 0x2000, TCD.CITER = 2 (TCD.BITER).
15. eDMA engine writes: TCD.ACTIVE = 0, TCD.DONE = 1, EDMA_IRQR*n* = 1.
16. The channel retires -> major loop complete.

The eDMA goes idle or services the next channel.

9.4.5.3 Modulo Feature

The modulo feature of the eDMA provides the ability to easily implement a circular data queue in which the size of the queue is a power of 2. MOD is a 5-bit field for the source and destination in the TCD, and specifies which lower address bits are incremented from their original value after the address + offset calculation. All upper address bits remain the same as in the original value. Clearing this field to 0 disables the modulo feature.

Table 9-24 shows how the transfer addresses are specified based on the setting of the MOD field. Here a circular buffer is created where the address wraps to the original value while the 28 upper address bits (0x1234567x) retain their original value. In this example the source address is set to 0x12345670, the offset is set to 4 bytes and the mod field is set to 4, allowing for a 2^4 byte (16-byte) size queue.

Table 9-24. Modulo Feature Example

Transfer Number	Address
1	0x1234_5670
2	0x1234_5674
3	0x1234_5678
4	0x1234_567C
5	0x1234_5670
6	0x1234_5674

9.4.6 TCD Status

9.4.6.1 Minor Loop Complete

There are two methods to test for minor loop completion when using software initiated service requests. The first method is to read the TCD.CITER field and test for a change. Another method can be extracted from the following sequence. The second method is to test the TCD.START bit AND the TCD.ACTIVE bit. The minor loop complete condition is indicated by both bits reading zero after the TCD.START was written to a one. Polling the TCD.ACTIVE bit can be inconclusive because the active status can be missed if the channel execution is short in duration.

The TCD status bits execute the following sequence for a software activated channel:

1. TCD.START = 1, TCD.ACTIVE = 0, TCD.DONE = 0 (issued service request via software)
2. TCD.START = 0, TCD.ACTIVE = 1, TCD.DONE = 0 (executing)
3. TCD.START = 0, TCD.ACTIVE = 0, TCD.DONE = 0 (completed minor loop and is idle) or
4. TCD.START = 0, TCD.ACTIVE = 0, TCD.DONE = 1 (completed major loop and is idle)

The best method to test for minor loop completion when using hardware initiated service requests is to read the TCD.CITER field and test for a change. The hardware request and acknowledge handshakes signals are not visible in the programmer’s model.

The TCD status bits execute the following sequence for a hardware activated channel:

1. eDMA peripheral request asserts (issued service request via hardware)
2. TCD.START = 0, TCD.ACTIVE = 1, TCD.DONE = 0 (executing)
3. TCD.START = 0, TCD.ACTIVE = 0, TCD.DONE = 0 (completed minor loop and is idle) or
4. TCD.START = 0, TCD.ACTIVE = 0, TCD.DONE = 1 (completed major loop and is idle)

For both activation types, the major loop complete status is explicitly indicated via the TCD.DONE bit.

The TCD.START bit is cleared automatically when the channel begins execution regardless of how the channel was activated.

9.4.6.2 Active Channel TCD Reads

The eDMA reads the true TCD.SADDR, TCD.DADDR, and TCD.NBYTES values if read while a channel is executing. The true values of the SADDR, DADDR, and NBYTES are the values the eDMA engine is currently using in its internal register file and not the values in the TCD local memory for that channel. The addresses (SADDR and DADDR) and NBYTES (decrements to zero as the transfer progresses) can give an indication of the progress of the transfer. All other values are read back from the TCD local memory.

9.4.6.3 Preemption Status

Preemption is only available when fixed arbitration is selected for both group and channel arbitration modes. A preempt-able situation is one in which a preempt-enabled channel is running and a higher priority request becomes active. When the eDMA engine is not operating in fixed group, fixed channel arbitration mode, the determination of the relative priority of the actively running and the outstanding requests become undefined. Channel and/or group priorities are treated as equal (or more exactly, constantly rotating) when round-robin arbitration mode is selected.

The TCD.ACTIVE bit for the preempted channel remains asserted throughout the preemption. The preempted channel is temporarily suspended while the preempting channel executes one iteration of the major loop. Two TCD.ACTIVE bits set at the same time in the overall TCD map indicates a higher priority channel is actively preempting a lower priority channel.

9.4.7 Channel Linking

Channel linking (or chaining) is a mechanism where one channel sets the TCD.START bit of another channel (or itself) thus initiating a service request for that channel. This operation is automatically performed by the eDMA engine at the conclusion of the major or minor loop when properly enabled.

The minor loop channel linking occurs at the completion of the minor loop (or one iteration of the major loop). The TCD.CITER.E_LINK field are used to determine whether a minor loop link is requested. When enabled, the channel link is made after each iteration of the minor loop except for the last.

When the major loop is exhausted, only the major loop channel link fields are used to determine whether to make a channel link. For example, with the initial fields of:

TCD.CITER.E_LINK = 1

TCD.CITER.LINKCH = 0xC

TCD.CITER value = 0x4

TCD.MAJOR.E_LINK = 1

TCD.MAJOR.LINKCH = 0x7

channel linking executes as:

1. Minor loop done -> set channel 12 TCD.START bit
2. Minor loop done -> set channel 12 TCD.START bit
3. Minor loop done -> set channel 12 TCD.START bit
4. Minor loop done, major loop done -> set channel 7 TCD.START bit

When minor loop linking is enabled (TCD.CITER.E_LINK = 1), the TCD.CITER field uses a nine bit vector to form the current iteration count.

When minor loop linking is disabled (TCD.CITER.E_LINK = 0), the TCD.CITER field uses a 15-bit vector to form the current iteration count. The bits associated with the TCD.CITER.LINKCH field are concatenated onto the CITER value to increase the range of the CITER.

NOTE

After configuration, the TCD.CITER.E_LINK bit and the TCD.BITER.E_LINK bit must be equal or a configuration error is reported. The CITER and BITER vector widths must be equal to calculate the major loop, half-way done interrupt point.

Table 9-25 summarizes how a DMA channel can “link” to another DMA channel, i.e, use another channel’s TCD, at the end of a loop.

Table 9-25. Channel Linking Parameters

Desired Link Behavior	TCD Control Field Name	Description
Link at end of Minor Loop	citer.e_link	Enable channel-to-channel linking on minor loop completion (current iteration)
	citer.linkch	Link channel number when linking at end of minor loop (current iteration)
Link at end of Major Loop	major.e_link	Enable channel-to-channel linking on major loop completion
	major.linkch	Link channel number when linking at end of major loop

9.4.8 Dynamic Programming

This section provides recommended methods to change the programming model during channel execution.

9.4.8.1 Dynamic Channel Linking and Dynamic Scatter/Gather

Dynamic channel linking and dynamic scatter/gather is the process of changing the TCD.MAJOR.E_LINK or TCD.E_SG bits during channel execution. These bits are read from the TCD local memory at the *end* of channel execution thus allowing the user to enable either feature during channel execution.

Because the user is allowed to change the configuration during execution, a coherency model is needed. Consider the scenario where the user attempts to execute a dynamic channel link by enabling the TCD.MAJOR.E_LINK bit at the same time the eDMA engine is retiring the channel. The TCD.MAJOR.E_LINK is set in the programmer's model, but it is unclear whether the link completed before the channel retired.

Use the following coherency model when executing a dynamic channel link or dynamic scatter/gather request:

1. Set the TCD.MAJOR.E_LINK bit
2. Read the TCD.MAJOR.E_LINK bit
3. Test the TCD.MAJOR.E_LINK request status:
   a) If the bit is set, the dynamic link attempt was successful.
   b) If the bit is cleared, the channel had already retired before the dynamic link completed.

This same coherency model is true for dynamic scatter/gather operations. For both dynamic requests, the TCD local memory controller forces the TCD.MAJOR.E_LINK and TCD.E_SG bits to zero on any writes to a channel's TCD after that channel's TCD.DONE bit is set indicating the major loop is complete.

NOTE

The user must clear the TCD.DONE bit before writing the TCD.MAJOR.E_LINK or TCD.E_SG bits. The TCD.DONE bit is cleared automatically by the eDMA engine after a channel begins execution.

Chapter 10
Interrupt Controller (INTC)

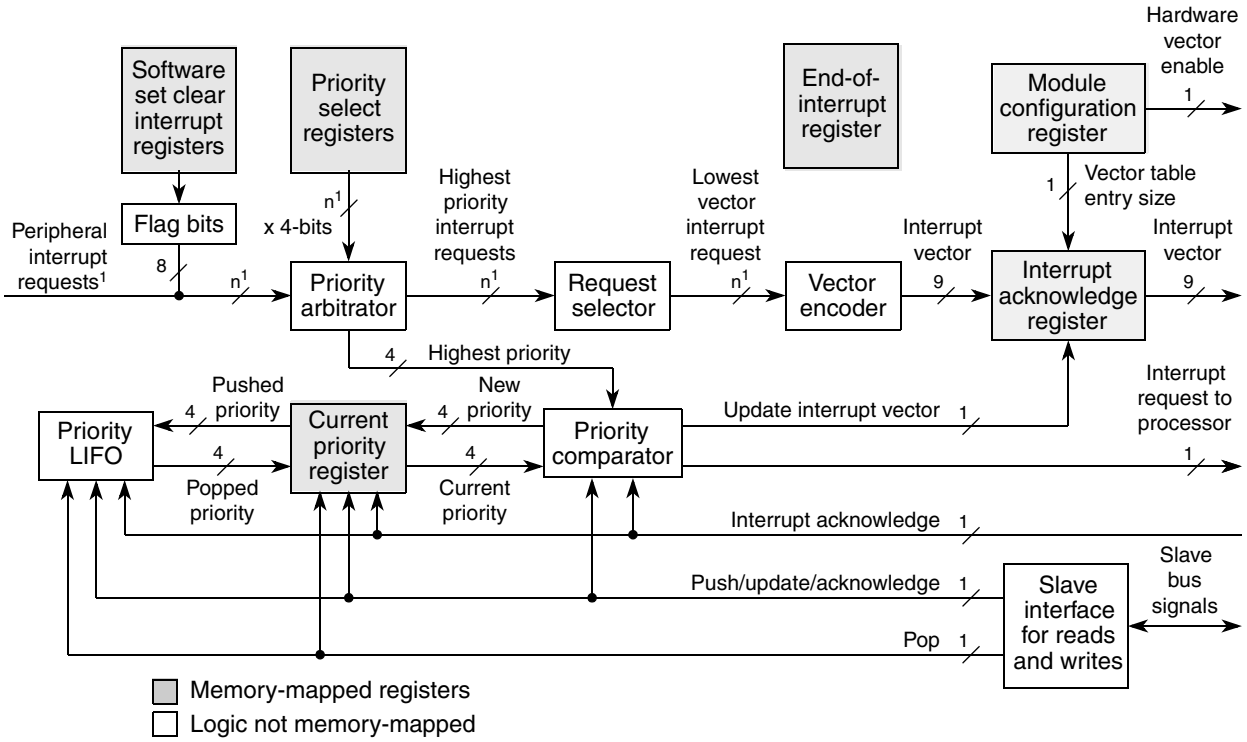
10.1 Introduction

This chapter describes the interrupt controller (INTC), which schedules interrupt requests (IRQs) from software and internal peripherals to the e200z6 core. The INTC provides interrupt prioritization and preemption, interrupt masking, interrupt priority elevation, and protocol support.

Interrupts implemented by the MCU are defined in the *e200z6 PowerPC™ Core Reference Manual*.

10.1.1 Block Diagram

Figure 4-1 shows details of the interrupt controller.



[1] Although N (largest addressable IRQ vector number) = 329, this does not indicate the total number of interrupts available on this device. The total number of available interrupts on this device is 332: 298 peripheral IRQs, eight software-configurable IRQs, and 16 reserved.

Figure 10-1. INTC Block Diagram

10.1.2 Overview

Interrupt functionality for the device is handled between the e200z6 core and the interrupt controller. The CPU core has 19 exception sources, each of which can interrupt the core. One exception source is from the interrupt controller (INTC). The INTC provides priority-based preemptive scheduling of interrupt requests. This scheduling scheme is suitable for statically scheduled hard real-time systems. The INTC is optimized for a large number of interrupt requests. It is targeted to work with a PowerPC book E processor and automotive powertrain applications where the ISRs nest to multiple levels.

Table 10-1 displays the interrupt sources and the number of interrupts available for each module; Figure 10-2 shows a general diagram of INTC software vector mode.

Table 10-1. Interrupt Sources Available

Interrupt Source (IRQs)	Number of Interrupts Available
Software	8
Watchdog	1
Memory	1
eDMA	66
FMPLL	2
External IRQ input pins	6
eMIOS	24
eTPU engine A	33
eTPU engine B	32
eQADC	31
DSPI	20
eSCI	2
FlexCAN	80
FEC	3

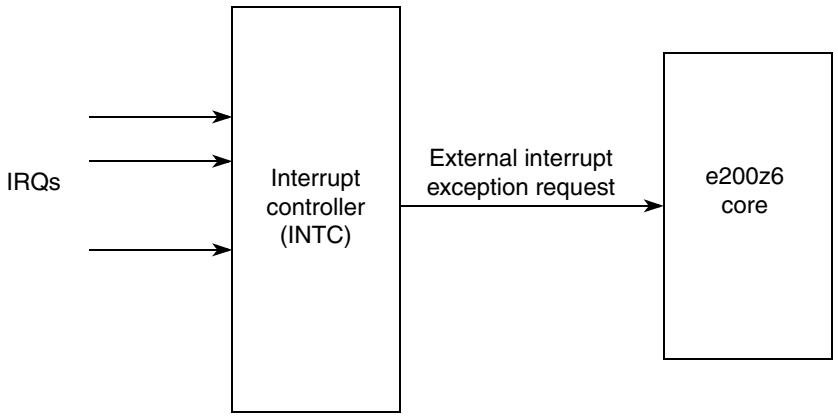


Figure 10-2. INTC Software Vector Mode

Two modes are available to determine the vector for the interrupt request source: software vector mode and hardware vector mode. In software vector mode, as shown in Figure 10-2, the e200z6 branches to a common interrupt exception handler whose location is determined by an address derived from special purpose registers IVPR and IVOR4. The interrupt exception handler reads the INTC_IACKR to determine the vector of the interrupt request source. Typical program flow for software vector mode is shown in Figure 10-3.

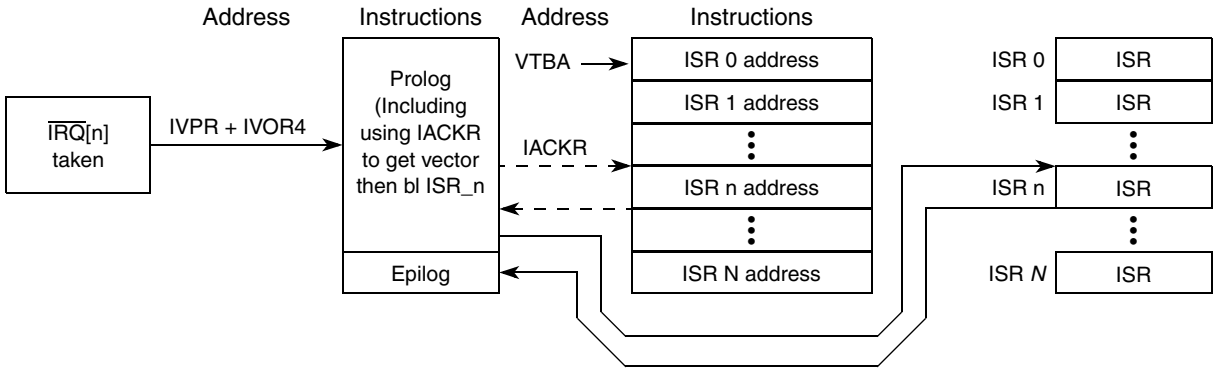


Figure 10-3. Program Flow–Software Vector Mode

N is the largest vector number (329) with the greatest hexadecimal address (IVPR + 0x1480) that is available in the interrupt memory map for this device. However, this number has no relationship to the total number of interrupts available on this device.

The total number of available interrupts on this device is 332: 298 peripheral IRQs, eight software-configurable IRQs, and 16 reserved.

Because the memory is mapped in four-byte words, the total number of interrupt vectors must be a multiple of four:

- If the total number of available interrupts is *not* a multiple of four, additional interrupt vectors exist up to the next four-byte boundary.

- If the total number of available interrupts *is* a multiple of four, no additional interrupt vectors exist.

In hardware vector mode, the core branches to an interrupt exception handler unique for each interrupt request source. Typical program flow for hardware vector mode is shown in Figure 10-4.

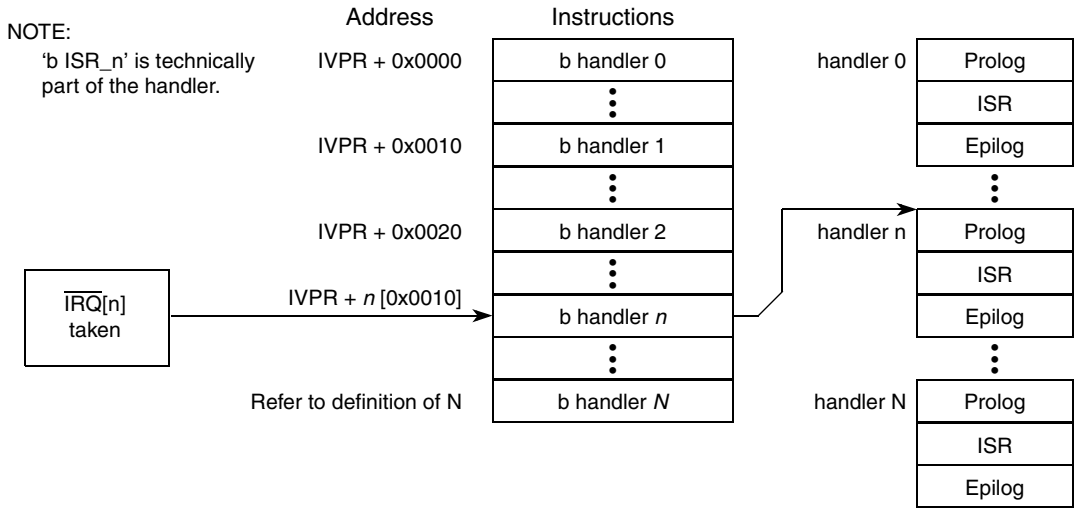


Figure 10-4. Program Flow–Hardware Vector Mode

For high priority interrupt requests in these target applications, the time from the assertion of the interrupt request from the peripheral to when the processor is performing useful work to service the interrupt request needs to be minimized. The INTC can be optimized to support this goal through the hardware vector mode, where a unique vector is provided for each interrupt request source. It also provides 16 priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. Since each individual application has different priorities for each source of interrupt request, the priority of each interrupt request is configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority level can be raised temporarily so that no task can preempt another task that shares the same resource.

Multiple processors can assert interrupt requests to each other through software settable interrupt requests, i.e., by using application software to assert an interrupt request. These same software settable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR can assert a software settable interrupt request to finish the servicing in a lower priority ISR.

10.1.3 Features

Features include the following:

- Total number of interrupt vectors is 332[1], of which:
  - 298 are peripheral interrupt vectors
  - 8 are software settable sources

  - 16 are reserved sources
- 9-bit unique vector for each interrupt request source in hardware vector mode.
- Each interrupt source can be programmed to one of 16 priorities.
- Preemption.
  - Preemptive prioritized interrupt requests to processor.
  - ISR at a higher priority preempts ISRs or tasks at lower priorities.
  - Automatic pushing or popping of preempted priority to or from a LIFO.
  - Ability to modify the ISR or task priority. Modifying the priority can be used to implement the priority ceiling protocol for accessing shared resources.
- Low latency–three clocks from receipt of interrupt request from peripheral to interrupt request to processor.

10.1.4 Modes of Operation

The interrupt controller has two handshaking modes with the processor: software vector mode and hardware vector mode. The state of the hardware vector enable bit, INTC_MCR[HVEN], determines which mode is used.

In debug mode the interrupt controller operation is identical to its normal operation of software vector mode or hardware vector mode.

10.1.4.1 Software Vector Mode

In software vector mode, there is a common interrupt exception handler address which is calculated by hardware as shown in Figure 10-5. The upper half of the interrupt vector prefix register (IVPR) is added to the offset contained in the external input interrupt vector offset register (IVOR4). Note that since bits IVOR4[28:31] are not part of the offset value, the vector offset must be located on a quad-word (16-byte) aligned location in memory.

In software vector mode, the interrupt exception handler software must read the INTC interrupt acknowledge register (INTC_IACKR) to obtain the vector associated with the corresponding peripheral or software interrupt request. The INTC_IACKR register contains a 32-bit address for a vector table base address (VTBA) plus an offset to access the interrupt vector (INTVEC). The address is then used to branch to the corresponding routine for that peripheral or software interrupt source.

1. The total number of available interrupts on this device is 332: 298 peripheral IRQs, eight software-configurable IRQs, and 16 reserved. Because the memory is mapped in four-byte words, the total number of interrupt vectors must be a multiple of four, therefore additional interrupt vectors exist to complete the word. This results in a total of 332 interrupt vectors. However, interrupt vectors 330–332 are reserved and not available.

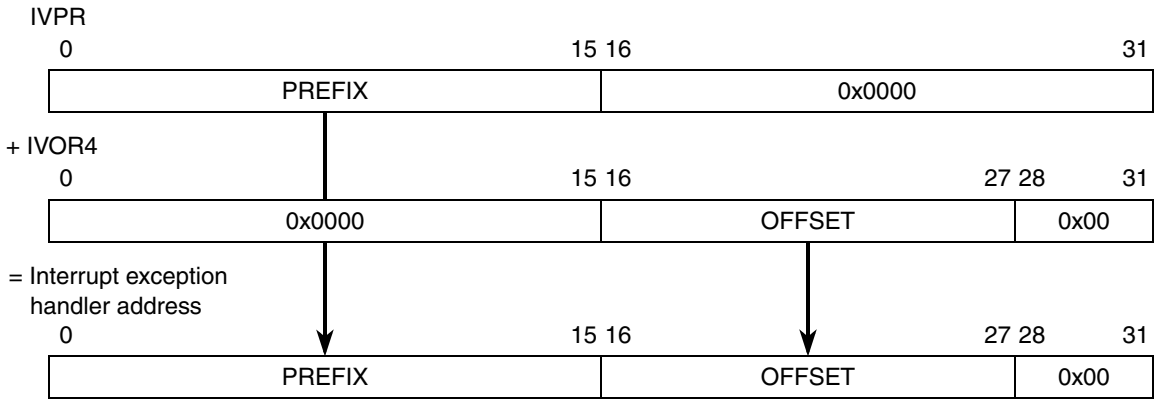


Figure 10-5. Software Vector Mode: Interrupt Exception Handler Address Calculation

Reading the INTC_IACKR acknowledges the INTC's interrupt request and negates the interrupt request to the processor. The interrupt request to the processor does not clear if a higher priority interrupt request arrives. Even in this case, INTVEC does not update to the higher priority request until the lower priority interrupt request is acknowledged by reading the INTC_IACKR. The reading also pushes the PRI value in the INTC current priority register (INTC_CPR) onto the LIFO and updates PRI in the INTC_CPR with the priority of the interrupt request. The INTC_CPR masks any peripheral or software settable interrupt request at the same or lower priority of the current value of the PRI field in INTC_CPR from generating an interrupt request to the processor.

The interrupt exception handler must write to the end-of-interrupt register (INTC_EOIR) to complete the operation. Writing to the INTC_EOIR ends the servicing of the interrupt request. The INTC's LIFO is popped into the INTC_CPR's PRI field by writing to the INTC_EOIR, and the size of a write does not affect the operation of the write. Those values and sizes written to this register neither update the INTC_EOIR contents nor affect whether the LIFO pops. For possible future compatibility, write four bytes of all 0s to the INTC_EOIR. The timing relationship between popping the LIFO and disabling recognition of external input has no restriction. The writes can happen in either order.

However, disabling recognition of the external input before popping the LIFO eases the calculation of the maximum stack depth at the cost of postponing the servicing of the next interrupt request.

10.1.4.2 Hardware Vector Mode

In hardware vector mode, the interrupt exception handler address is specific to the peripheral or software settable interrupt source rather than being common to all of them. No IVOR is used. The interrupt exception handler address is calculated by hardware as shown in Figure 10-6. The upper half of the interrupt vector prefix register (IVPR) is added to an offset which corresponds to the peripheral or software interrupt source which caused the interrupt request. The offset matches the value in the Interrupt Vector field, INTC_IACKR[INTVEC]. Each interrupt exception handler address is aligned on a four-word (16-byte) boundary. IVOR4 is not used in this mode, and software does not need to read INTC_IACKR to get the interrupt vector number.

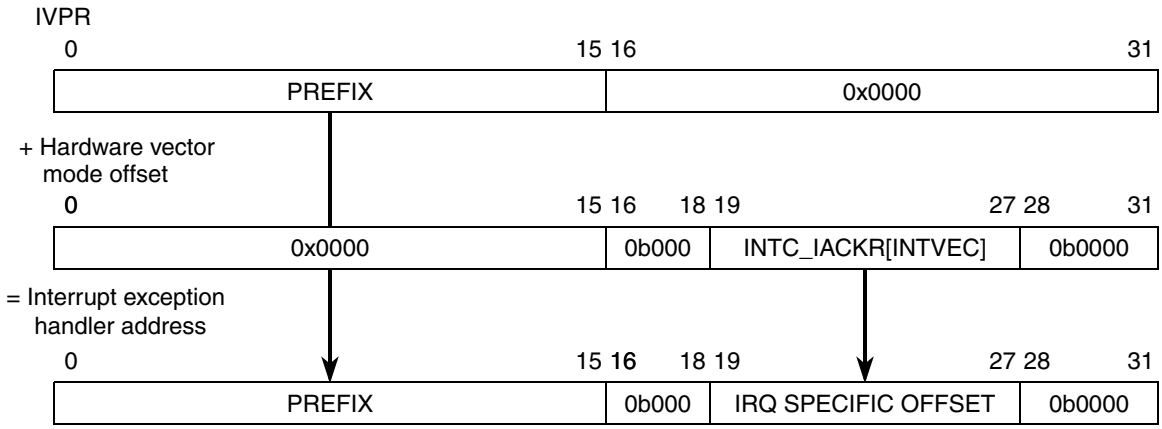


Figure 10-6. Hardware Vector Mode: Interrupt Exception Handler Address Calculation

The processor negates INTC's interrupt request when automatically acknowledging the interrupt request. However, the interrupt request to the processor do not negate if a higher priority interrupt request arrives. Even in this case, the interrupt vector number does not update to the higher priority request until the lower priority request is acknowledged by the processor.

The assertion of the interrupt acknowledge signal pushes the PRI value in the INTC_CPR onto the LIFO and updates PRI in the INTC_CPR with the new priority.

10.2 External Signal Description

The INTC does not have any direct external MCU signals. However, there are sixteen external pins which can be configured in the SIU as external interrupt request input pins. When configured for an external interrupt request function, an interrupt on that pin sets an external interrupt flag. These flags cause one of five peripheral interrupt requests to the interrupt controller.

For more information on external interrupts, the pins used, and how to configure them:

- Refer to Table 10-2 for a list and number of the external interrupt pins.
- Refer to the SIU chapter for more information on these pins.

Table 10-2. External Interrupt Signals

Function[1]	P/A/G[2]	Description	I/O Type	Reset Function/ State[3]	Post Reset Function/ State[4]
EMIOS[14]_	P	eMIOS channel	O	— / WKPCFG	— / WKPCFG
$\overline{\text{IRQ}}$[0]_	A	External interrupt request	I		
CNTXD	A	CAN D transmit	O		
GPIO[193]	G	GPIO	I/O		

Table 10-2. External Interrupt Signals (continued)

Function[1]	P/A/G[2]	Description	I/O Type	Reset Function/ State[3]	Post Reset Function/ State[4]
EMIOS[15]_	P	eMIOS channel	O		
$\overline{\text{IRQ}}$[1]_	A	External interrupt request	I	— / WKPCFG	— / WKPCFG
CNRXD	A	CAN D receive	I		
GPIO[194]	G	GPIO	I/O		
BOOTCFG[0:1]_	P	Boot configuration input	I		
$\overline{\text{IRQ}}$[2:3]_	A	External interrupt request	I	BOOTCFG / Down	— / Down
GPIO[211:212]	G	GPIO	I/O		
PLLCFG[0]_	P	FMPLL mode selection	I		
$\overline{\text{IRQ}}$[4]_	A	External interrupt request	I	PLLCFG / Up	— / Up
GPIO[208]	G	GPIO	I/O		
PLLCFG[1]_	P	FMPLL reference selection	I		
$\overline{\text{IRQ}}$[5]_	A	External interrupt request	I	PLLCFG / Up	— / Up
GPIO[209]	G	GPIO	I/O		
TCRCLKB_	P	eTPU B TCR clock	I		
$\overline{\text{IRQ}}$[6]_	A	External interrupt request	I	— / Up	— / Up
GPIO[146]	G	GPIO	I/O		
TCRCLKA_	P	eTPU A TCR clock	I		
$\overline{\text{IRQ}}$[7]_	A	External interrupt request	I		
GPIO[113]	G	GPIO	I/O		
ETPUA[20]_	P	eTPU A channel	I/O		
$\overline{\text{IRQ}}$[8]_	A	External interrupt request	I	— / Up	— / Up
GPIO[134]	G	GPIO	I/O		
ETPUA[21]_	P	eTPU A channel	I/O		
$\overline{\text{IRQ}}$[9]_	A	External interrupt request	I		
GPIO[135]	G	GPIO	I/O		
ETPUA[22]_	P	eTPU A channel	I/O		
$\overline{\text{IRQ}}$[10]_	A	External interrupt request	I	— / WKPCFG	— / WKPCFG
GPIO[136]	G	GPIO	I/O		
ETPUA[23]_	P	eTPU A channel	I/O		
$\overline{\text{IRQ}}$[11]_	A	External interrupt request	I		
GPIO[137]	G	GPIO	I/O		
ETPUA[24:27]_	P	eTPU A channel (output only)	O		
$\overline{\text{IRQ}}$[12:15]_	A	External interrupt request	I		
GPIO[138:141]_	G	GPIO	I/O		

[1] For each pin in the table, each line in the function column is a separate function muxed to the pin. For all device I/O pins, the selection of a primary, secondary or tertiary function is done in the SIU module except where explicitly noted.

[2] Primary, alternate, or GPIO function. The primary name labels the pin on the PBGA pinout.
[3] Terminology is O - output, I - input, Up - weak pullup enabled, Down - weak pulldown enabled, Low - output driven low, High - output driven high.
[4] Function after reset of GPI is general-purpose input.

10.3 Memory Map and Register Definition

Table 10-3 is the INTC memory map.

Table 10-3. INTC Memory Map

Address	Register Name	Register Description	Bits
Base (0xFFF4_8000)	INTC_MCR	INTC module configuration register	32
Base + 0x0004	—	Reserved	—
Base + 0x0008	INTC_CPR	INTC current priority register	32
Base + 0x000C	—	Reserved	—
Base + 0x0010	INTC_IACKR	INTC interrupt acknowledge register [1]	32
Base + 0x0014	—	Reserved	—
Base + 0x0018	INTC_EOIR	INTC end-of-interrupt register	32
Base + 0x001C	—	Reserved	—
Base + 0x0020	INTC_SSCIR0	INTC software set/clear interrupt register 0	8
Base + 0x0021	INTC_SSCIR1	INTC software set/clear interrupt register 1	8
Base + 0x0022	INTC_SSCIR2	INTC software set/clear interrupt register 2	8
Base + 0x0023	INTC_SSCIR3	INTC software set/clear interrupt register 3	8
Base + 0x0024	INTC_SSCIR4	INTC software set/clear interrupt register 4	8
Base + 0x0025	INTC_SSCIR5	INTC software set/clear interrupt register 5	8
Base + 0x0026	INTC_SSCIR6	INTC software set/clear interrupt register 6	8
Base + 0x0027	INTC_SSCIR7	INTC software set/clear interrupt register 7	8
Base + (0x0028–0x003F)	—	Reserved	—
Base + (0x0040–0x01A7)	INTC_PSR*n*	INTC priority select registers [2] 0–329	8

[1] When the HVEN bit in the INTC_MCR is asserted, a read of the INTC_IACKR has no side effects.
[2] The PRI fields are “Reserved” for peripheral interrupt requests whose vectors are labeled as Reserved in Table 10-9.

10.3.1 Register Descriptions

With the exception of the INTC_SSCI*n* and INTC_PSR*n* registers, all of the registers are 32-bits wide. Any combination of accessing the 4 bytes of a register with a single access is supported, provided that the access does not cross a register boundary. These supported accesses include types and sizes of 8 bits, aligned 16 bits, and aligned 32 bits.

Although INTC_SSCI*n* and INTC_PSR*n* are 8 bits wide, they can be accessed with a single 16-bit or 32-bit access, provided that the access does not cross a 32-bit boundary.

In software vector mode, the side effects of a read of the INTC interrupt acknowledge register (INTC_IACKR) are the same regardless of the size of the read. In either software or hardware vector mode, the size of a write to the INTC end-of-interrupt register (INTC_EOIR) does not affect the operation of the write.

10.3.1.1 INTC Module Configuration Register (INTC_MCR)

The INTC_MCR is used to configure options of the INTC.

Address: Base + 0x0000 (INTC_MCR) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VTES	0	0	0	0	HVEN
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 10-7. INTC Module Configuration Register (INTC_MCR)

Table 10-4. INTC_MCR Field Descriptions

Field	Description
0–25	Reserved, must be cleared.
26 VTES	Vector table entry size. Controls the number of ‘0’s to the right of INTVEC in Section 10.3.1.3, “INTC Interrupt Acknowledge Register (INTC_IACKR). If the contents of INTC_IACKR are used as an address of an entry in a vector table as in software vector mode, then the number of rightmost ‘0’s determines the size of each vector table entry. VTES impacts software vector mode operation but also affects the INTC_IACKR[INTVEC] position in both hardware vector mode and software vector mode. 0 4 bytes (Normal expected use) 1 8 bytes
27–30	Reserved, must be cleared.
31 HVEN	Hardware vector enable. Controls whether the INTC is in hardware vector mode or software vector mode. Refer to Section 10.1.4, “Modes of Operation”, for the details of the handshaking with the processor in each mode. 0 Software vector mode 1 Hardware vector mode

10.3.1.2 INTC Current Priority Register (INTC_CPR)

The INTC_CPR masks any peripheral or software settable interrupt request set at the same or lower priority as the current value of the INTC_CPR[PRI] field from generating an interrupt request to the processor. When the INTC interrupt acknowledge register (INTC_IACKR) is read in software vector mode or the interrupt acknowledge signal from the processor is asserted in hardware vector mode, the value of PRI is pushed onto the LIFO, and PRI is updated with the priority of the preempting interrupt request. When the INTC end-of-interrupt register (INTC_EOIR) is written, the LIFO is popped into the INTC_CPR's PRI field.

The masking priority can be raised or lowered by writing to the PRI field, supporting the PCP. Refer to Section 10.5.5, "Priority Ceiling Protocol."

NOTE

On some Power Architecture MCUs, a store to raise the PRI field which closely precedes an access to a shared resource can result in a non-coherent access to that resource unless an **mbar** or **msync** followed by an **isync** sequence of instructions is executed between the accesses. An **mbar** or **msync** instruction is also necessary after accessing the resource but before lowering the PRI field. Refer to Section 10.5.5.2, "Ensuring Coherency."

Address: Base + 0x0008 (INTC_CPR) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PRI			
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Figure 10-8. INTC Current Priority Register (INTC_CPR)

Table 10-5. INTC_CPR Field Descriptions

Field	Description
0–27	Reserved, must be cleared.
28–31 PRI	Priority. PRI is the priority of the currently executing ISR according to the field values defined below. 1111 Priority 15 (highest) 1110 Priority 14 ... 0001 Priority 1 0000 Priority 0 (lowest)

10.3.1.3 INTC Interrupt Acknowledge Register (INTC_IACKR)

The INTC_IACKR provides a value that can be used to load the address of an ISR from a vector table. The vector table can be composed of addresses of the ISRs specific to their respective interrupt vectors.

In software vector mode, reading the INTC_IACKR acknowledges the INTC's interrupt request. Refer to Section 10.1.4.1, "Software Vector Mode" for a detailed description of the effect on the interrupt request to the processor. The reading also pushes the PRI value in the INTC current priority register (INTC_CPR) onto the LIFO and updates PRI in the INTC_CPR with the priority of the interrupt request. The side effect

from the reads in software vector mode, that is, the effect on the interrupt request to the processor, the current priority, and the LIFO, are the same regardless of the size of the read

Reading the INTC_IACKR does not have side effects in hardware vector mode.

NOTE

The INTC_IACKR must not be read speculatively while in software vector mode. Therefore, for future compatibility, the TLB entry covering the INTC_IACKR must be configured to be guarded.

In software vector mode, the INTC_IACKR must be read before setting MSR[EE]. No synchronization instruction is needed after reading the INTC_IACKR and before setting MSR[EE].

However, the time for the processor to recognize the assertion or negation of the external input to it is not defined by the book E architecture and can be greater than 0. Therefore, insert instructions between the reading of the INTC_IACKR and the setting of MSR[EE] that consumes at least two processor clock cycles. This length of time allows the interrupt request negation to propagate through the processor before MSR[EE] is set.

Address: Base + 0x0010 (INTC_IACKR) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	VTBA																				INTVEC										0	0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 10-9. INTC Interrupt Acknowledge Register (INTC_IACKR)—INTC_MCR[VTES] = 0

Address: Base + 0x0010 (INTC_IACKR) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	VTBA																				INTVEC									0	0	0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 10-10. INTC Interrupt Acknowledge Register (INTC_IACKR)—INTC_MCR[VTES] = 1

Table 10-6. INTC_IACKR Field Descriptions

Field	Description
0–20 *or* 0–19 VTBA	Vector table base address. Can be the base address of a vector table of addresses of ISRs. The VTBA only uses the left-most 20 bits when the VTES bit in INTC_MCR is asserted.

Table 10-6. INTC_IACKR Field Descriptions (continued)

Field	Description
21–29 *or* 20–28 INTVEC	Interrupt vector. Vector of peripheral or software-settable interrupt requests that caused the interrupt request to the processor. When the interrupt request to the processor asserts, the INTVEC is updated, whether the INTC is in software or hardware vector mode. **Note:** If INTC_MCR[VTES] = 1, then the INTVEC field is shifted left one position to bits 20–28. VTBA is then shortened by one bit to bits 0–19.
30–31 or 29–31	Reserved, must be cleared.

10.3.1.4 INTC End-of-Interrupt Register (INTC_EOIR)

Writing to the INTC_EOIR signals the end of the servicing of the interrupt request. When the INTC_EOIR is written, the priority last pushed on the LIFO is popped into INTC_CPR. The values and size of data written to the INTC_EOIR are ignored. Those values and sizes written to this register neither update the INTC_EOIR contents or affect whether the LIFO pops. For possible future compatibility, write four bytes of all 0's to the INTC_EOIR.

Reading the INTC_EOIR has no effect on the LIFO.

Address: Base + 0x0018 (INTC_EOIR) Access: W/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	EOIR																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 10-11. INTC End-of-Interrupt Register (INTC_EOIR)

10.3.1.5 INTC Software Set/Clear Interrupt Registers (INTC_SSCIR0–7)

The INTC_SSCIR*n* support the setting or clearing of software settable interrupt requests. These registers contain eight independent sets of bits to set and clear a corresponding flag bit by software. With the exception of being set by software, this flag bit behaves the same as a flag bit set within a peripheral. This flag bit generates an interrupt request within the INTC just like a peripheral interrupt request. Writing a 1 to SET*n* leaves SET*n* unchanged at 0 but sets CLR*n*. Writing a 0 to SET*n* has no effect. CLR*n* is the flag bit. Writing a 1 to CLR*n* clears it. Writing a 0 to CLR*n* has no effect. If a 1 is written to a pair SET*n* and CLR*n* bits at the same time, CLR*n* is asserted, regardless of whether CLR*n* was asserted before the write.

Although INTC_SSCI*n* is 8 bits wide, it can be accessed with a single 16-bit or 32-bit access, provided that the access does not cross a 32-bit boundary.

Address: Base + 0x0020 + *n* (INTC_SSCIR*n*); *n* = 0–7 Access: R/W

	0	1	2	3	4	5	6	7
R	0	0	0	0	0	0	0	CLR*n*
W							SET*n*	
Reset	0	0	0	0	0	0	0	0

Figure 10-12. INTC Software Set/Clear Interrupt Register (INTC_SSCIR*n*)

Table 10-7. INTC_SSCIR*n* Field Descriptions

Field	Description
0–5	Reserved, must be cleared.
6 SET*n*	Set flag bits. Writing a 1 sets the corresponding CLR*n* bit. Writing a 0 has no effect. Each SET*n* is always read as a 0.
7 CLR*n*	Clear flag bits. CLR*n* is the flag bit. Writing a 1 to CLR*n* clears it provided that a 1 is not written simultaneously to its corresponding SET*n* bit. Writing a 0 to CLR*n* has no effect. 0 Interrupt request not pending within INTC. 1 Interrupt request pending within INTC.

10.3.1.6 INTC Priority Select Registers (INTC_PSR0–329)

The INTC_PSR*n* allows you to select a priority for each interrupt request source (peripheral IRQs or software-settable IRQs). Each priority select register (INTC_PSR*n)* is assigned to the IRQ source vector with the same number. For example, the software-settable IRQs 0–7 are assigned vectors 0–7, and their priorities are configured in INTC_PSR0–INTC_PSR7, respectively. The peripheral interrupt requests are assigned vectors 8–329 and their priorities are configured in priority select registers INTC_PSR8 through INTC_PSR329, respectively.

Although INTC_PSR*n* is 8 bits wide, you can use a single 16-bit or 32-bit access, provided that it does not cross a 32-bit boundary.

NOTE

Do not modify the PRI*n* field in INTC_PSR*n* when the IRQ is asserted.

Address: Base + 0x0040 + *n* (INTC_PSR*n*); *n* = 0–329 Access: R/W

	0	1	2	3	4	5	6	7
R	0	0	0	0	PRI*n*			
W								
Reset	0	0	0	0	0	0	0	0

Figure 10-13. INTC Priority Select Registers (INTC_PSR*n*)

Table 10-8. INTC_PSR*n* Field Descriptions

Field	Description
0–3	Reserved, must be cleared.
4–7 PRI*n*	Priority select. Selects the priority for corresponding interrupt request. 1111 Priority 15 (highest) 1110 Priority 14 ... 0001 Priority 1 0000 Priority 0 (lowest)

10.4 Functional Description

10.4.1 Interrupt Request Sources

The INTC has two types of interrupt requests, peripheral and software settable. The assignments between the interrupt requests from the modules to the vectors for input to the e200z6 are shown in Table 10-9. The Hardware Vector Mode Offset column lists the IRQ-specific offsets when using hardware vector mode. The Source column shows the C language syntax for the register bit label: module_register[bit]. Interrupt requests from the same module location are ORed together. The individual interrupt priorities are selected in INTC_PSR*n*, where the priority select register is assigned according to the vector number.

Table 10-9. MPC5566 Interrupt Request Sources

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
Software			
0x0000	0	INTC_SSCIR0[CLR0]	INTC software settable. Clear flag 0
0x0010	1	INTC_SSCIR1[CLR1]	INTC software settable. Clear flag 1
0x0020	2	INTC_SSCIR2[CLR2]	INTC software settable. Clear flag 2
0x0030	3	INTC_SSCIR3[CLR3]	INTC software settable. Clear flag 3
0x0040	4	INTC_SSCIR4[CLR4]	INTC software settable. Clear flag 4
0x0050	5	INTC_SSCIR5[CLR5]	INTC software settable. Clear flag 5
0x0060	6	INTC_SSCIR6[CLR6]	INTC software settable. Clear flag 6
0x0070	7	INTC_SSCIR7[CLR7]	INTC software settable. Clear flag 7
Watchdog / ECC			
0x0080	8	ECSM_SWTIR[SWTIC]	ECSM software watchdog interrupt flag
0x0090	9	ECSM_ESR[RNCE] ECSM_ESR[FNCE]	ECSM combined interrupt requests: • Internal SRAM non-correctable error • Flash non-correctable error
eDMA			
0x00A0	10	EDMA_ERL[ERR31:ERR0]	eDMA channel error flags 31–0
0x00B0	11	EDMA_IRQRL[INT00]	eDMA channel interrupt 0
0x00C0	12	EDMA_IRQRL[INT01]	eDMA channel interrupt 1
0x00D0	13	EDMA_IRQRL[INT02]	eDMA channel interrupt 2
0x00E0	14	EDMA_IRQRL[INT03]	eDMA channel interrupt 3
0x00F0	15	EDMA_IRQRL[INT04]	eDMA channel interrupt 4
0x0100	16	EDMA_IRQRL[INT05]	eDMA channel interrupt 5
0x0110	17	EDMA_IRQRL[INT06]	eDMA channel interrupt 6
0x0120	18	EDMA_IRQRL[INT07]	eDMA channel interrupt 7

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
0x0130	19	EDMA_IRQRL[INT08]	eDMA channel interrupt 8
0x0140	20	EDMA_IRQRL[INT09]	eDMA channel interrupt 9
0x0150	21	EDMA_IRQRL[INT10]	eDMA channel interrupt 10
0x0160	22	EDMA_IRQRL[INT11]	eDMA channel interrupt 11
0x0170	23	EDMA_IRQRL[INT12]	eDMA channel interrupt 12
0x0180	24	EDMA_IRQRL[INT13]	eDMA channel interrupt 13
0x0190	25	EDMA_IRQRL[INT14]	-eDMA channel interrupt 14
0x01A0	26	EDMA_IRQRL[INT15]	eDMA channel interrupt 15
0x01B0	27	EDMA_IRQRL[INT16]	eDMA channel interrupt 16
0x01C0	28	EDMA_IRQRL[INT17]	eDMA channel interrupt 17
0x01D0	29	EDMA_IRQRL[INT18]	eDMA channel interrupt 18
0x01E0	30	EDMA_IRQRL[INT19]	eDMA channel interrupt 19
0x01F0	31	EDMA_IRQRL[INT20]	eDMA channel interrupt 20
0x0200	32	EDMA_IRQRL[INT21]	eDMA channel interrupt 21
0x0210	33	EDMA_IRQRL[INT22]	eDMA channel interrupt 22
0x0220	34	EDMA_IRQRL[INT23]	eDMA channel interrupt 23
0x0230	35	EDMA_IRQRL[INT24]	eDMA channel interrupt 24
0x0240	36	EDMA_IRQRL[INT25]	eDMA channel interrupt 25
0x0250	37	EDMA_IRQRL[INT26]	eDMA channel interrupt 26
0x0260	38	EDMA_IRQRL[INT27]	eDMA channel interrupt 27
0x0270	39	EDMA_IRQRL[INT28]	eDMA channel interrupt 28
0x0280	40	EDMA_IRQRL[INT29]	eDMA channel interrupt 29
0x0290	41	EDMA_IRQRL[INT30]	eDMA channel interrupt 30
0x02A0	42	EDMA_IRQRL[INT31]	eDMA channel interrupt 31
FMPLL			
0x02B0	43	FMPLL_SYNSR[LOCF]	FMPLL loss-of-clock flag
0x02C0	44	FMPLL_SYNSR[LOLF]	FMPLL loss-of-lock flag
SIU			
0x02D0	45	SIU_OSR[OVF15:OVF0]	SIU combined overrun interrupt requests of the external interrupt overrun flags 15–0
0x02E0	46	SIU_EISR[EIF0]	SIU external interrupt flag 0
0x02F0	47	SIU_EISR[EIF1]	SIU external interrupt flag 1

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
0x0300	48	SIU_EISR[EIF2]	SIU external interrupt flag 2
0x0310	49	SIU_EISR[EIF3]	SIU external interrupt flag 3
0x0320	50	SIU_EISR[EIF15:EIF4]	SIU external interrupt flags 15–4
eMIOS			
0x0330	51	EMIOS_GFR[F0]	eMIOS channel 0 flag
0x0340	52	EMIOS_GFR[F1]	eMIOS channel 1 flag
0x0350	53	EMIOS_GFR[F2]	eMIOS channel 2 flag
0x0360	54	EMIOS_GFR[F3]	eMIOS channel 3 flag
0x0370	55	EMIOS_GFR[F4]	eMIOS channel 4 flag
0x0380	56	EMIOS_GFR[F5]	eMIOS channel 5 flag
0x0390	57	EMIOS_GFR[F6]	eMIOS channel 6 flag
0x03A0	58	EMIOS_GFR[F7]	eMIOS channel 7 flag
0x03B0	59	EMIOS_GFR[F8]	eMIOS channel 8 flag
0x03C0	60	EMIOS_GFR[F9]	eMIOS channel 9 flag
0x03D0	61	EMIOS_GFR[F10]	eMIOS channel 10 flag
0x03E0	62	EMIOS_GFR[F11]	eMIOS channel 11 flag
0x03F0	63	EMIOS_GFR[F12]	eMIOS channel 12 flag
0x0400	64	EMIOS_GFR[F13]	eMIOS channel 13 flag
0x0410	65	EMIOS_GFR[F14]	eMIOS channel 14 flag
0x0420	66	EMIOS_GFR[F15]	eMIOS channel 15 flag
eTPU A			
0x0430	67	ETPU_MCR[MGEA] ETPU_MCR[MGEB] ETPU_MCR[ILFA] ETPU_MCR[ILFB] ETPU_MCR[SCMMISF]	eTPU global exception
0x0440	68	ETPU_CISR_A[CIS0]	eTPU engine A channel 0 interrupt status
0x0450	69	ETPU_CISR_A[CIS1]	eTPU engine A channel 1 interrupt status
0x0460	70	ETPU_CISR_A[CIS2]	eTPU engine A channel 2 interrupt status
0x0470	71	ETPU_CISR_A[CIS3]	eTPU engine A channel 3 interrupt status
0x0480	72	ETPU_CISR_A[CIS4]	eTPU engine A channel 4 interrupt status
0x0490	73	ETPU_CISR_A[CIS5]	eTPU engine A channel 5 interrupt status
0x04A0	74	ETPU_CISR_A[CIS6]	eTPU engine A channel 6 interrupt status

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
0x04B0	75	ETPU_CISR_A[CIS7]	eTPU engine A channel 7 interrupt status
0x04C0	76	ETPU_CISR_A[CIS8]	eTPU engine A channel 8 interrupt status
0x04D0	77	ETPU_CISR_A[CIS9]	eTPU engine A channel 9 interrupt status
0x04E0	78	ETPU_CISR_A[CIS10]	eTPU engine A channel 10 interrupt status
0x04F0	79	ETPU_CISR_A[CIS11]	eTPU engine A channel 11 interrupt status
0x0500	80	ETPU_CISR_A[CIS12]	eTPU engine A channel 12 interrupt status
0x0510	81	ETPU_CISR_A[CIS13]	eTPU engine A channel 13 interrupt status
0x0520	82	ETPU_CISR_A[CIS14]	eTPU engine A channel 14 interrupt status
0x0530	83	ETPU_CISR_A[CIS15]	eTPU engine A channel 15 interrupt status
0x0540	84	ETPU_CISR_A[CIS16]	eTPU engine A channel 16 interrupt status
0x0550	85	ETPU_CISR_A[CIS17]	eTPU engine A channel 17 interrupt status
0x0560	86	ETPU_CISR_A[CIS18]	eTPU engine A channel 18 interrupt status
0x0570	87	ETPU_CISR_A[CIS19]	eTPU engine A channel 19 interrupt status
0x0580	88	ETPU_CISR_A[CIS20]	eTPU engine A channel 20 interrupt status
0x0590	89	ETPU_CISR_A[CIS21]	eTPU engine A channel 21 interrupt status
0x05A0	90	ETPU_CISR_A[CIS22]	eTPU engine A channel 22 interrupt status
0x05B0	91	ETPU_CISR_A[CIS23]	eTPU engine A channel 23 interrupt status
0x05C0	92	ETPU_CISR_A[CIS24]	eTPU engine A channel 24 interrupt status
0x05D0	93	ETPU_CISR_A[CIS25]	eTPU engine A channel 25 interrupt status
0x05E0	94	ETPU_CISR_A[CIS26]	eTPU engine A channel 26 interrupt status
0x05F0	95	ETPU_CISR_A[CIS27]	eTPU engine A channel 27 interrupt status
0x0600	96	ETPU_CISR_A[CIS28]	eTPU engine A channel 28 interrupt status
0x0610	97	ETPU_CISR_A[CIS29]	eTPU engine A channel 29 interrupt status
0x0620	98	ETPU_CISR_A[CIS30]	eTPU engine A channel 30 interrupt status
0x0630	99	ETPU_CISR_A[CIS31]	eTPU engine A channel 31 interrupt status
eQADC			
0x0640	100	EQADC_FISR*x*[TORF] EQADC_FISR*x*[RFOF] EQADC_FISR*x*[CFUF]	eQADC combined overrun interrupt request s from all of the FIFOs: • Trigger Overrun • Receive FIFO Overflow • Command FIFO Underflow
0x0650	101	EQADC_FISR0[NCF]	eQADC command FIFO 0 non-coherency flag
0x0660	102	EQADC_FISR0[PF]	eQADC command FIFO 0 pause flag

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
0x0670	103	EQADC_FISR0[EOQF]	eQADC command FIFO 0 command queue end-of-queue flag
0x0680	104	EQADC_FISR0[CFFF]	eQADC command FIFO 0 fill flag
0x0690	105	EQADC_FISR0[RFDF]	eQADC receive FIFO 0 drain flag
0x06A0	106	EQADC_FISR1[NCF]	eQADC command FIFO 1 non-coherency flag
0x06B0	107	EQADC_FISR1[PF]	eQADC command FIFO 1 pause flag
0x06C0	108	EQADC_FISR1[EOQF]	eQADC command FIFO 1 command queue end-of-queue flag
0x06D0	109	EQADC_FISR1[CFFF]	eQADC command FIFO 1 fill flag
0x06E0	110	EQADC_FISR1[RFDF]	eQADC receive FIFO 1 drain flag
0x06F0	111	EQADC_FISR2[NCF]	eQADC command FIFO 2 non-coherency flag
0x0700	112	EQADC_FISR2[PF]	eQADC command FIFO 2 pause flag
0x0710	113	EQADC_FISR2[EOQF]	eQADC command FIFO 2 command queue end-of-queue flag
0x0720	114	EQADC_FISR2[CFFF]	eQADC command FIFO 2 fill flag
0x0730	115	EQADC_FISR2[RFDF]	eQADC receive FIFO 2 drain flag
0x0740	116	EQADC_FISR3[NCF]	eQADC command FIFO 3 non-coherency flag
0x0750	117	EQADC_FISR3[PF]	eQADC command FIFO 3 pause flag
0x0760	118	EQADC_FISR3[EOQF]	eQADC command FIFO 3 command queue end-of-queue flag
0x0770	119	EQADC_FISR3[CFFF]	eQADC command FIFO 3 fill flag
0x0780	120	EQADC_FISR3[RFDF]	eQADC receive FIFO 3 drain flag
0x0790	121	EQADC_FISR4[NCF]	eQADC command FIFO 4 non-coherency flag
0x07A0	122	EQADC_FISR4[PF]	eQADC command FIFO 4 pause flag
0x07B0	123	EQADC_FISR4[EOQF]	eQADC command FIFO 4 command queue end-of-queue flag
0x07C0	124	EQADC_FISR4[CFFF]	eQADC command FIFO 4 fill flag
0x07D0	125	EQADC_FISR4[RFDF]	eQADC receive FIFO 4 drain flag
0x07E0	126	EQADC_FISR5[NCF]	eQADC command FIFO 5 non-coherency flag
0x07F0	127	EQADC_FISR5[PF]	eQADC command FIFO 5 pause flag
0x0800	128	EQADC_FISR5[EOQF]	eQADC command FIFO 5 command queue end-of-queue flag
0x0810	129	EQADC_FISR5[CFFF]	eQADC command FIFO 5 fill flag
0x0820	130	EQADC_FISR5[RFDF]	eQADC receive FIFO 5 drain flag

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
DSPI B, C, and D			
0x0830	131	DSPI_BSR[TFUF] DSPI_BSR[RFOF]	DSPI B combined overrun interrupt requests: • Transmit FIFO underflow • Receive FIFO overflow
0x0840	132	DSPI_BSR[EOQF]	DSPI B transmit FIFO end-of-queue flag
0x0850	133	DSPI_BSR[TFFF]	DSPI B transmit FIFO fill flag
0x0860	134	DSPI_BSR[TCF]	DSPI B transmit complete
0x0870	135	DSPI_BSR[RFDF]	DSPI B Rx FIFO drain request
0x0880	136	DSPI_CSR[TFUF] DSPI_CSR[RFOF]	DSPI C combined overrun interrupt requests: • Transmit FIFO underflow • Receive FIFO overflow
0x0890	137	DSPI_CSR[EOQF]	DSPI C transmit FIFO end-of-queue flag
0x08A0	138	DSPI_CSR[TFFF]	DSPI C transmit FIFO fill flag
0x08B0	139	DSPI_CSR[TCF]	DSPI C transmit complete
0x08C0	140	DSPI_CSR[RFDF]	DSPI C Rx FIFO drain request
0x08D0	141	DSPI_DSR[TFUF] DSPI_DSR[RFOF]	DSPI D combined overrun interrupt requests: • Transmit FIFO underflow • Receive FIFO overflow
0x08E0	142	DSPI_DSR[EOQF]	DSPI D transmit FIFO end-of-queue flag
0x08F0	143	DSPI_DSR[TFFF]	DSPI D transmit FIFO fill flag
0x0900	144	DSPI_DSR[TCF]	DSPI D transfer complete
0x0910	145	DSPI_DSR[RFDF]	DSPI D Rx FIFO drain request

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
eSCI			
0x0920	146	ESCIA_SR[TDRE] ESCIA_SR[TC] ESCIA_SR[RDRF] ESCIA_SR[IDLE] ESCIA_SR[OR] ESCIA_SR[NF] ESCIA_SR[FE] ESCIA_SR[PF] ESCIA_SR[BERR] ESCIA_SR[RXRDY] ESCIA_SR[TXRDY] ESCIA_SR[LWAKE] ESCIA_SR[STO] ESCIA_SR[PBERR] ESCIA_SR[CERR] ESCIA_SR[CKERR] ESCIA_SR[FRC] ESCIA_SR[OVFL]	Combined interrupt requests of eSCI Module A: • LIN status register 1 • LIN status register 2 • SCI status register 2 • Transmit data register empty • Transmit complete • Receive data register full • Idle line • Overrun • Noise flag • Framing error flag • Parity error flag interrupt requests • Bit error interrupt request • Receive data ready • Transmit data ready • Received LIN wakeup signal • Slave timeout • Physical bus error • CRC error • Checksum error • Frame complete interrupts requests • Receive register overflow
0x0930–0x0940	147–148	Reserved	
0x0950	149	ESCIB_SR[TDRE] ESCIB_SR[TC] ESCIB_SR[RDRF] ESCIB_SR[IDLE] ESCIB_SR[OR] ESCIB_SR[NF] ESCIB_SR[FE] ESCIB_SR[PF] ESCIB_SR[BERR] ESCIB_SR[RXRDY] ESCIB_SR[TXRDY] ESCIB_SR[LWAKE] ESCIB_SR[STO] ESCIB_SR[PBERR] ESCIB_SR[CERR] ESCIB_SR[CKERR] ESCIB_SR[FRC] ESCIB_SR[OVFL]	Combined interrupt requests of eSCI Module B: • LIN status register 1 • LIN status register 2 • SCI status register 2 • Transmit data register empty • Transmit complete • Receive data register full • Idle line • Overrun • Noise flag • Framing error flag • Parity error flag interrupt requests • Bit error interrupt request • Receive data ready • Transmit data ready • Received LIN wakeup signal • Slave timeout • Physical bus error • CRC error • Checksum error • Frame complete interrupts requests • Receive register overflow
0x0960–0x0970	150–151	Reserved	

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
FlexCAN A and FlexCAN C			
0x0980	152	CANA_ESR[BOFF_INT] CANA_ESR[TWRN_INT] CANA_ESR[RWRN_INT]	FlexCAN A bus off interrupt FlexCAN A transmit warning interrupt FlexCAN A receive warning interrupt
0x0990	153	CANA_ESR[ERR_INT]	FlexCAN A error interrupt
0x09A0	154	Reserved	
0x09B0	155	CANA_IFRL[BUF0]	FlexCAN A buffer 0 interrupt
0x09C0	156	CANA_IFRL[BUF1]	FlexCAN A buffer 1 interrupt
0x09D0	157	CANA_IFRL[BUF2]	FlexCAN A buffer 2 interrupt
0x09E0	158	CANA_IFRL[BUF3]	FlexCAN A buffer 3 interrupt
0x09F0	159	CANA_IFRL[BUF4]	FlexCAN A buffer 4 interrupt
0x0A00	160	CANA_IFRL[BUF5]	FlexCAN A buffer 5 interrupt
0x0A10	161	CANA_IFRL[BUF6]	FlexCAN A buffer 6 interrupt
0x0A20	162	CANA_IFRL[BUF7]	FlexCAN A buffer 7 interrupt
0x0A30	163	CANA_IFRL[BUF8]	FlexCAN A buffer 8 interrupt
0x0A40	164	CANA_IFRL[BUF9]	FlexCAN A buffer 9 interrupt
0x0A50	165	CANA_IFRL[BUF10]	FlexCAN A buffer 10 interrupt
0x0A60	166	CANA_IFRL[BUF11]	FlexCAN A buffer 11 interrupt
0x0A70	167	CANA_IFRL[BUF12]	FlexCAN A buffer 12 interrupt
0x0A80	168	CANA_IFRL[BUF13]	FlexCAN A buffer 13 interrupt
0x0A90	169	CANA_IFRL[BUF14]	FlexCAN A buffer 14 interrupt
0x0AA0	170	CANA_IFRL[BUF15]	FlexCAN A buffer 15 interrupt
0x0AB0	171	CANA_IFRL[BUF31I:BUF16]	FlexCAN A buffers 31–16 interrupts
0x0AC0	172	CANA_IFRH[BUF63I:BUF32]	FlexCAN A buffers 63–32 interrupts
0x0AD0	173	CANC_ESR[BOFF_INT] CANC_ESR[TWRN_INT] CANC_ESR[RWRN_INT]	FlexCAN C bus off interrupt FlexCAN C transmit warning interrupt FlexCAN C receive warning interrupt
0x0AE0	174	CANC_ESR[ERR_INT]	FlexCAN C error interrupt
0x0AF0	175	Reserved	
0x0B00	176	CANC_IFRL[BUF0]	FlexCAN C buffer 0 interrupt
0x0B10	177	CANC_IFRL[BUF1]	FlexCAN C buffer 1 interrupt
0x0B20	178	CANC_IFRL[BUF2]	FlexCAN C buffer 2 interrupt
0x0B30	179	CANC_IFRL[BUF3]	FlexCAN C buffer 3 interrupt

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
0x0B40	180	CANC_IFRL[BUF4]	FlexCAN C buffer 4 interrupt
0x0B50	181	CANC_IFRL[BUF5]	FlexCAN C buffer 5 interrupt
0x0B60	182	CANC_IFRL[BUF6]	FlexCAN C buffer 6 interrupt
0x0B70	183	CANC_IFRL[BUF7]	FlexCAN C buffer 7 interrupt
0x0B80	184	CANC_IFRL[BUF8]	FlexCAN C buffer 8 interrupt
0x0B90	185	CANC_IFRL[BUF9]	FlexCAN C buffer 9 interrupt
0x0BA0	186	CANC_IFRL[BUF10]	FlexCAN C buffer 10 interrupt
0x0BB0	187	CANC_IFRL[BUF11]	FlexCAN C buffer 11 interrupt
0x0BC0	188	CANC_IFRL[BUF12]	FlexCAN C buffer 12 interrupt
0x0BD0	189	CANC_IFRL[BUF13]	FlexCAN C buffer 13 interrupt
0x0BE0	190	CANC_IFRL[BUF14]	FlexCAN C buffer 14 interrupt
0x0BF0	191	CANC_IFRL[BUF15]	FlexCAN C buffer 15 interrupt
0x0C00	192	CANC_IFRL[BUF31:BUF16]	FlexCAN C buffers 31–16 interrupts
0x0C10	193	CANC_IFRH[BUF63:BUF32]	FlexCAN C buffers 63–32 interrupts
FEC			
0x0C20	194	EIR[TXF]	FEC transmit frame flag
0x0C30	195	EIR[RXF]	FEC receive frame flag
0x0C40	196	EIR[HBERR] EIR[BABR] EIR[BABT] EIR[GRA] EIR[TXB] EIR[RXB] EIR[MII] EIR[EBERR] EIR[LC] EIR[RL] EIR[UN]	Combined interrupt requests of the FEC Ethernet interrupt event register: • Heartbeat error • Babbling receive error • Babbling transmit error • Graceful stop complete • Transmit buffer • Receive buffer • Media independent interface • Ethernet bus error • Late collision • Collision retry limit • Transmit FIFO underrun
0x0C50–0x0C90	197–201	Reserved	
eMIOS			
0x0CA0	202	EMIOS_GFR[F16]	eMIOS channel 16 flag
0x0CB0	203	EMIOS_GFR[F17]	eMIOS channel 17 flag
0x0CC0	204	EMIOS_GFR[F18]	eMIOS channel 18 flag
0x0CD0	205	EMIOS_GFR[F19]	eMIOS channel 19 flag

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
0x0CE0	206	EMIOS_GFR[F20]	eMIOS channel 20 flag
0x0CF0	207	EMIOS_GFR[F21]	eMIOS channel 21 flag
0x0D00	208	EMIOS_GFR[F22]	eMIOS channel 22 flag
0x0D10	209	EMIOS_GFR[F23]	eMIOS channel 23 flag
eDMA			
0x0D20	210	EDMA_ERRH[ERR63:ERR32]	eDMA channel error flags 63–32
0x0D30	211	EDMA_IRQRH[INT32]	eDMA channel interrupt 32
0x0D40	212	EDMA_IRQRH[INT33]	eDMA channel interrupt 33
0x0D50	213	EDMA_IRQRH[INT34]	eDMA channel interrupt 34
0x0D60	214	EDMA_IRQRH[INT35]	eDMA channel interrupt 35
0x0D70	215	EDMA_IRQRH[INT36]	eDMA channel interrupt 36
0x0D80	216	EDMA_IRQRH[INT37]	eDMA channel interrupt 37
0x0D90	217	EDMA_IRQRH[INT38]	eDMA channel interrupt 38
0x0DA0	218	EDMA_IRQRH[INT39]	eDMA channel interrupt 39
0x0DB0	219	EDMA_IRQRH[INT40]	eDMA channel interrupt 40
0x0DC0	220	EDMA_IRQRH[INT41]	eDMA channel interrupt 41
0x0DD0	221	EDMA_IRQRH[INT42]	eDMA channel interrupt 42
0x0DE0	222	EDMA_IRQRH[INT43]	eDMA channel interrupt 43
0x0DF0	223	EDMA_IRQRH[INT44]	eDMA channel interrupt 44
0x0E00	224	EDMA_IRQRH[INT45]	eDMA channel interrupt 45
0x0E10	225	EDMA_IRQRH[INT46]	eDMA channel interrupt 46
0x0E20	226	EDMA_IRQRH[INT47]	eDMA channel interrupt 47
0x0E30	227	EDMA_IRQRH[INT48]	eDMA channel interrupt 48
0x0E40	228	EDMA_IRQRH[INT49]	eDMA channel interrupt 49
0x0E50	229	EDMA_IRQRH[INT50]	eDMA channel interrupt 50
0x0E60	230	EDMA_IRQRH[INT51]	eDMA channel interrupt 51
0x0E70	231	EDMA_IRQRH[INT52]	eDMA channel interrupt 52
0x0E80	232	EDMA_IRQRH[INT53]	eDMA channel interrupt 53
0x0E90	233	EDMA_IRQRH[INT54]	eDMA channel interrupt 54
0x0EA0	234	EDMA_IRQRH[INT55]	eDMA channel interrupt 55
0x0EB0	235	EDMA_IRQRH[INT56]	eDMA channel interrupt 56

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
0x0EC0	236	EDMA_IRQRH[INT57]	eDMA channel interrupt 57
0x0ED0	237	EDMA_IRQRH[INT58]	eDMA channel interrupt 58
0x0EE0	238	EDMA_IRQRH[INT59]	eDMA channel interrupt 59
0x0EF0	239	EDMA_IRQRH[INT60]	eDMA channel interrupt 60
0x0F00	240	EDMA_IRQRH[INT61]	eDMA channel interrupt 61
0x0F10	241	EDMA_IRQRH[INT62]	eDMA channel interrupt 62
0x0F20	242	EDMA_IRQRH[INT63]	eDMA channel interrupt 63
eTPU B			
0x0F30	243	ETPU_CISR_B[CIS0]	eTPU engine B channel 0 interrupt status
0x0F40	244	ETPU_CISR_B[CIS1]	eTPU engine B channel 1 interrupt status
0x0F50	245	ETPU_CISR_B[CIS2]	eTPU engine B channel 2 interrupt status
0x0F60	246	ETPU_CISR_B[CIS3]	eTPU engine B channel 3 interrupt status
0x0F70	247	ETPU_CISR_B[CIS4]	eTPU engine B channel 4 interrupt status
0x0F80	248	ETPU_CISR_B[CIS5]	eTPU engine B channel 5 interrupt status
0x0F90	249	ETPU_CISR_B[CIS6]	eTPU engine B channel 6 interrupt status
0x0FA0	250	ETPU_CISR_B[CIS7]	eTPU engine B channel 7 interrupt status
0x0FB0	251	ETPU_CISR_B[CIS8]	eTPU engine B channel 8 interrupt status
0x0FC0	252	ETPU_CISR_B[CIS9]	eTPU engine B channel 9 interrupt status
0x0FD0	253	ETPU_CISR_B[CIS10]	eTPU engine B channel 10 interrupt status
0x0FE0	254	ETPU_CISR_B[CIS11]	eTPU engine B channel 11 interrupt status
0x0FF0	255	ETPU_CISR_B[CIS12]	eTPU engine B channel 12 interrupt status
0x1000	256	ETPU_CISR_B[CIS13]	eTPU engine B channel 13 interrupt status
0x1010	257	ETPU_CISR_B[CIS14]	eTPU engine B channel 14 interrupt status
0x1020	258	ETPU_CISR_B[CIS15]	eTPU engine B channel 15 interrupt status
0x1030	259	ETPU_CISR_B[CIS16]	eTPU engine B channel 16 interrupt status
0x1040	260	ETPU_CISR_B[CIS17]	eTPU engine B channel 17 interrupt status
0x1050	261	ETPU_CISR_B[CIS18]	eTPU engine B channel 18 interrupt status
0x1060	262	ETPU_CISR_B[CIS19]	eTPU engine B channel 19 interrupt status
0x1070	263	ETPU_CISR_B[CIS20]	eTPU engine B channel 20 interrupt status
0x1080	264	ETPU_CISR_B[CIS21]	eTPU engine B channel 21 interrupt status
0x1090	265	ETPU_CISR_B[CIS22]	eTPU engine B channel 22 interrupt status

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
0x10A0	266	ETPU_CISR_B[CIS23]	eTPU engine B channel 23 interrupt status
0x10B0	267	ETPU_CISR_B[CIS24]	eTPU engine B channel 24 interrupt status
0x10C0	268	ETPU_CISR_B[CIS25]	eTPU engine B channel 25 interrupt status
0x10D0	269	ETPU_CISR_B[CIS26]	eTPU engine B channel 26 interrupt status
0x10E0	270	ETPU_CISR_B[CIS27]	eTPU engine B channel 27 interrupt status
0x10F0	271	ETPU_CISR_B[CIS28]	eTPU engine B channel 28 interrupt status
0x1100	272	ETPU_CISR_B[CIS29]	eTPU engine B channel 29 interrupt status
0x1110	273	ETPU_CISR_B[CIS30]	eTPU engine B channel 30 interrupt status
0x1120	274	ETPU_CISR_B[CIS31]	eTPU engine B channel 31 interrupt status
DSPI A			
0x1130	275	DSPI_ASR[TFUF] DSPI_ASR[RFOF]	DSPI A combined overrun interrupt requests: • Transmit FIFO underflow • Receive FIFO overflow
0x1140	276	DSPI_ASR[EOQF]	DSPI A transmit FIFO end-of-queue flag
0x1150	277	DSPI_ASR[TFFF]	DSPI A Tx FIFO fill flag
0x1160	278	DSPI_ASR[TCF]	DSPI A transmit complete flag
0x1170	279	DSPI_ASR[RFDF]	DSPI A Rx FIFO drain flag
FlexCAN B			
0x1180	280	CANB_ESR[BOFF_INT] CANB_ESR[TWRN_INT] CANB_ESR[RWRN_INT]	FlexCAN B bus off interrupt FlexCAN B transmit warning interrupt FlexCAN B receive warning interrupt
0x1190	281	CANB_ESR[ERR_INT]	FlexCAN B error interrupt
0x11A0	282	Reserved	
0x11B0	283	CANB_IFRL[BUF0]	FlexCAN B buffer 0 interrupt
0x11C0	284	CANB_IFRL[BUF1]	FlexCAN B buffer 1 interrupt
0x11D0	285	CANB_IFRL[BUF2]	FlexCAN B buffer 2 interrupt
0x11E0	286	CANB_IFRL[BUF3]	FlexCAN B buffer 3 interrupt
0x11F0	287	CANB_IFRL[BUF4]	FlexCAN B buffer 4 interrupt
0x1200	288	CANB_IFRL[BUF5]	FlexCAN B buffer 5 interrupt
0x1210	289	CANB_IFRL[BUF6]	FlexCAN B buffer 6 interrupt
0x1220	290	CANB_IFRL[BUF7]	FlexCAN B buffer 7 interrupt
0x1230	291	CANB_IFRL[BUF8]	FlexCAN B buffer 8 interrupt
0x1240	292	CANB_IFRL[BUF9]	FlexCAN B buffer 9 interrupt

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
0x1250	293	CANB_IFRL[BUF10]	FlexCAN B buffer 10 interrupt
0x1260	294	CANB_IFRL[BUF11]	FlexCAN B buffer 11 interrupt
0x1270	295	CANB_IFRL[BUF12]	FlexCAN B buffer 12 interrupt
0x1280	296	CANB_IFRL[BUF13]	FlexCAN B buffer 13 interrupt
0x1290	297	CANB_IFRL[BUF14]	FlexCAN B buffer 14 interrupt
0x12A0	298	CANB_IFRL[BUF15]	FlexCAN B buffer 15 interrupt
0x12B0	299	CANB_IFRL[BUF31:BUF16]	FlexCAN B buffers 31–16 interrupts
0x12C0	300	CANB_IFRH[BUF63:BUF32]	FlexCAN B buffers 63–32 interrupts
0x12D0–0x1330	301–307	Reserved	
FlexCAN D			
0x1340	308	CAND_ESR[BOFF_INT] CAND_ESR[TWRN_INT] CAND_ESR[RWRN_INT]	FlexCAN D bus off interrupt FlexCAN D transmit warning interrupt FlexCAN D receive warning interrupt
0x1350	309	CAND_ESR[ERR_INT]	FlexCAN D error interrupt
0x1360	310	Reserved	
0x1370	311	CAND_IFRL[BUF0]	FlexCAN D buffer 0 interrupt
0x1380	312	CAND_IFRL[BUF1]	FlexCAN D buffer 1 interrupt
0x1390	313	CAND_IFRL[BUF2]	FlexCAN D buffer 2 interrupt
0x13A0	314	CAND_IFRL[BUF3]	FlexCAN D buffer 3 interrupt
0x13B0	315	CAND_IFRL[BUF4]	FlexCAN D buffer 4 interrupt
0x13C0	316	CAND_IFRL[BUF5]	FlexCAN D buffer 5 interrupt
0x13D0	317	CAND_IFRL[BUF6]	FlexCAN D buffer 6 interrupt
0x13E0	318	CAND_IFRL[BUF7]	FlexCAN D buffer 7 interrupt
0x13F0	319	CAND_IFRL[BUF8]	FlexCAN D buffer 8 interrupt
0x1400	320	CAND_IFRL[BUF9]	FlexCAN D buffer 9 interrupt
0x1410	321	CAND_IFRL[BUF10]	FlexCAN D buffer 10 interrupt
0x1420	322	CAND_IFRL[BUF11]	FlexCAN D buffer 11 interrupt
0x1430	323	CAND_IFRL[BUF12]	FlexCAN D buffer 12 interrupt
0x1440	324	CAND_IFRL[BUF13]	FlexCAN D buffer 13 interrupt
0x1450	325	CAND_IFRL[BUF14]	FlexCAN D buffer 14 interrupt
0x1460	326	CAND_IFRL[BUF15]	FlexCAN D buffer 15 interrupt
0x1470	327	CAND_IFRL[BUF31:BUF16]	FlexCAN D buffers 31–16 interrupts

Table 10-9. MPC5566 Interrupt Request Sources (continued)

Hardware Vector Mode Offset	Vector Number [1]	Source[2]	Description
0x1480	328	CAND_IFRH[BUF63:BUF32]	FlexCAN D buffers 63–32 interrupts
0x1490–0x14B0	329–331	Reserved	

1 The vector number is used to identify the interrupt priority select register; it does not indicate the maximum number of usable interrupt sources.

2 Interrupt requests from the same module location are ORed together.

NOTE

The peripheral or software settable interrupt request asserts when the PRI*n* value in the interrupt priority select register (INTC_PSR*n*) is greater than the PRI*n* value in interrupt current priority register (INTC_CPR).

If an asserted peripheral or software settable interrupt request negates before the processor acknowledges its request, the interrupt request can reassert and remain asserted. If this occurs, the processor uses the INTC_PSR*n* value to locate the IRQ vector, and updates the PRI*n* value in the INTC_CPR with the PRI*n* value in INTC_PSR*n*.

Clearing the peripheral interrupt request enable bit for the peripheral initiating the request, or setting the IRQ mask bit has the same consequences as clearing its flag bit. Setting its enable bit or clearing its mask bit while its flag bit is asserted has the same effect on the INTC as an interrupt event setting the flag bit.

10.4.1.1 Peripheral Interrupt Requests

An interrupt event in a peripheral's hardware sets a flag bit which resides in that peripheral. The interrupt request from the peripheral is driven by that flag bit.

The time from when the peripheral starts to drive its peripheral interrupt request to the INTC to the time that the INTC starts to drive the interrupt request to the processor is three clocks.

10.4.1.2 Software Settable Interrupt Requests

The software set/clear interrupt registers (INTC_SSCIR*x_x*) support the setting or clearing of software-settable interrupt requests. These registers contain eight independent sets of bits to set and clear a corresponding flag bit by software. With the exception of being set by software, this flag bit behaves the same as a flag bit set within a peripheral. This flag bit generates an interrupt request within the INTC just like a peripheral interrupt request.

An interrupt request is triggered by software writing a 1 to the SET*n* bit in INTC software set/clear interrupt registers (INTC_SSCIR0–INTC_SSCIR7). This write sets a CLR*n* flag bit that generates an

interrupt request. The interrupt request is cleared by writing a 1 to the CLR*n* bit. Specific behavior includes the following:

- Writing a 1 to SET*n* leaves SET*n* unchanged at 0 but sets the flag bit (CLR*n* bit).
- Writing a 0 to SET*n* has no effect.
- Writing a 1 to CLR*n* clears the flag (CLR*n*) bit.
- Writing a 0 to CLR*n* has no effect.
- If a 1 is written to a pair of SET*n* and CLR*n* bits at the same time, the flag (CLR*n*) is set, regardless of whether CLR*n* was asserted before the write.

The time from the write to the SET*n* bit to the time that the INTC starts to drive the interrupt request to the processor is four clocks.

10.4.1.3 Unique Vector for Each Interrupt Request Source

Each peripheral and software settable interrupt request is assigned a hardwired unique 9-bit vector. Software settable interrupts 0–7 are assigned vectors 0–7, respectively. The peripheral interrupt requests are assigned vectors 8 to as high as needed to cover all of the peripheral interrupt requests.

10.4.2 Priority Management

The asserted interrupt requests are compared to each other based on their PRI*n* values in INTC priority select registers (INTC_PSR0–INTC_PSR329). The result of that comparison also is compared to PRI in INTC current priority register (INTC_CPR). The results of those comparisons are used to manage the priority of the ISR being executed by the processor. The LIFO also assists in managing that priority.

10.4.2.1 Current Priority and Preemption

The priority arbitrator, selector, encoder, and comparator submodules shown in Figure 10-1 are used to compare the priority of the asserted interrupt requests to the current priority. If the priority of any asserted peripheral or software settable interrupt request is higher than the current priority, then the interrupt request to the processor is asserted. Also, a unique vector for the preempting peripheral or software settable interrupt request is generated for INTC interrupt acknowledge register (INTC_IACKR), and if in hardware vector mode, for the interrupt vector provided to the processor.

10.4.2.1.1 Priority Arbitrator Submodule

The priority arbitrator submodule compares all the priorities of all of the asserted interrupt requests, both peripheral and software settable. The output of the priority arbitrator submodule is the highest of those priorities. Also, any interrupt requests which have this highest priority are output as asserted interrupt requests to the request selector submodule.

10.4.2.1.2 Request Selector Submodule

If only one interrupt request from the priority arbitrator submodule is asserted, then it is passed as asserted to the vector encoder submodule. If multiple interrupt requests from the priority arbitrator submodule are asserted, then only the one with the lowest vector is passed as asserted to the vector encoder submodule.

The lower vector is chosen regardless of the time order of the assertions of the peripheral or software settable interrupt requests.

10.4.2.1.3 Vector Encoder Submodule

The vector encoder submodule generates the unique 9-bit vector for the asserted interrupt request from the request selector submodule.

10.4.2.1.4 Priority Comparator Submodule

The priority comparator submodule compares the highest priority output from the priority arbitrator submodule with PRI in INTC_CPR. If the priority comparator submodule detects that this highest priority is higher than the current priority, then it asserts the interrupt request to the processor. This interrupt request to the processor asserts whether this highest priority is raised above the value of PRI in INTC_CPR or the PRI value in INTC_CPR is lowered below this highest priority. This highest priority then becomes the new priority which is written to PRI in INTC_CPR when the interrupt request to the processor is acknowledged. Interrupt requests whose PRI*n* in INTC_PSR*n* are zero does not cause a preemption because their PRI*n* is not higher than PRI in INTC_CPR.

10.4.2.2 LIFO

The LIFO stores the preempted PRI values from the INTC_CPR. Therefore, because these priorities are stacked within the INTC, if interrupts need to be enabled during the ISR, at the beginning of the interrupt exception handler the PRI value in the INTC_CPR does not need to be loaded from the INTC_CPR and stored onto the context stack. Likewise at the end of the interrupt exception handler, the priority does not need to be loaded from the context stack and stored into the INTC_CPR.

The PRI value in the INTC_CPR is pushed onto the LIFO when the INTC_IACKR is read in software vector mode or the interrupt acknowledge signal from the processor is asserted in hardware vector mode. The priority is popped into PRI in the INTC_CPR whenever the INTC_EOIR is written.

Although the INTC supports 16 priorities, an ISR executing with PRI in the INTC_CPR equal to 15 is not preempted. Therefore, the LIFO supports the stacking of 15 priorities. However, the LIFO is only 14 entries deep. An entry for a priority of 0 is not needed because of how pushing onto a full LIFO and popping an empty LIFO are treated. If the LIFO is pushed 15 or more times than it is popped, the priorities first pushed are overwritten. A priority of 0 is an overwritten priority. However, the LIFO pop zeros if it is popped more times than it is pushed. Therefore, although a priority of 0 was overwritten, it is regenerated with the popping of an empty LIFO.

The LIFO is not memory mapped.

10.4.3 Details on Handshaking with Processor

10.4.3.1 Software Vector Mode Handshaking

10.4.3.1.1 Acknowledging Interrupt Request to Processor

A timing diagram of the interrupt request and acknowledge handshaking in software vector mode, along with the handshaking near the end of the interrupt exception handler, is shown in Figure 10-14. The INTC examines the peripheral and software settable interrupt requests. When it finds an asserted peripheral or software settable interrupt request with a higher priority than PRI in INTC current priority register (INTC_CPR), it asserts the interrupt request to the processor. The INTVEC field in INTC interrupt acknowledge register (INTC_IACKR) is updated with the preempting interrupt request's vector when the interrupt request to the processor is asserted. The INTVEC field retains that value until the next time the interrupt request to the processor is asserted. The rest of the handshaking is described in Section 10.1.4.1, "Software Vector Mode."

10.4.3.1.2 End-of-Interrupt Exception Handler

Before the interrupt exception handling completes, INTC end-of-interrupt register (INTC_EOIR) must be written. When it is written, the LIFO is popped so that the preempted priority is restored into PRI of the INTC_CPR. Before it is written, the peripheral or software settable flag bit must be cleared so that the peripheral or software settable interrupt request is negated.

NOTE

To ensure proper operation across all Power Architecture MCUs, execute an MBAR or MSYNC instruction between the access to clear the flag bit and the write to the INTC_EOIR.

When returning from the preemption, the INTC does not search for the peripheral or software settable interrupt request whose ISR was preempted. Depending on how much the ISR progressed, that interrupt request can no longer be asserted. When PRI in INTC_CPR is lowered to the priority of the preempted ISR, the interrupt request for the preempted ISR or any other asserted peripheral or software settable interrupt request at or below that priority does not cause a preemption. Instead, after the restoration of the preempted context, the processor returns to the instruction address that it was to next execute before it was preempted. This next instruction is part of the preempted ISR or the interrupt exception handler's prolog or epilog.

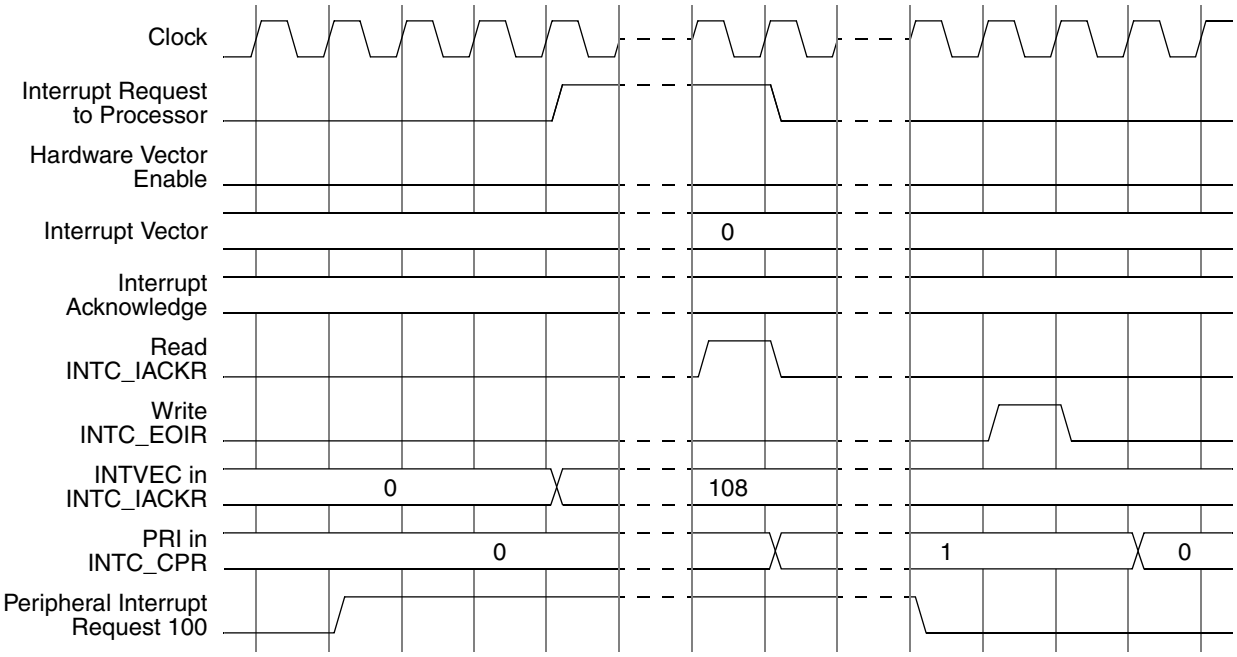


Figure 10-14. Software Vector Mode Handshaking Timing Diagram

10.4.3.2 Hardware Vector Mode Handshaking

A timing diagram of the interrupt request and acknowledge handshaking in hardware vector mode, along with the handshaking near the end of the interrupt exception handler, is shown in Figure 10-15. As in software vector mode, the INTC examines the peripheral and software settable interrupt requests, and when it finds an asserted one with a higher priority than PRI in INTC_CPR, it asserts the interrupt request to the processor. The INTVEC field in the INTC_IACKR is updated with the preempting peripheral or software settable interrupt request's vector when the interrupt request to the processor is asserted. The INTVEC field retains that value until the next time the interrupt request to the processor is asserted. In addition, the value of the interrupt vector to the processor matches the value of the INTVEC field in the INTC_IACKR. The rest of the handshaking is described in Section 10.1.4.2, "Hardware Vector Mode."

The handshaking near the end of the interrupt exception handler, that is the writing to the INTC_EOIR, is the same as in software vector mode. Refer to Section 10.4.3.1.2, "End-of-Interrupt Exception Handler."

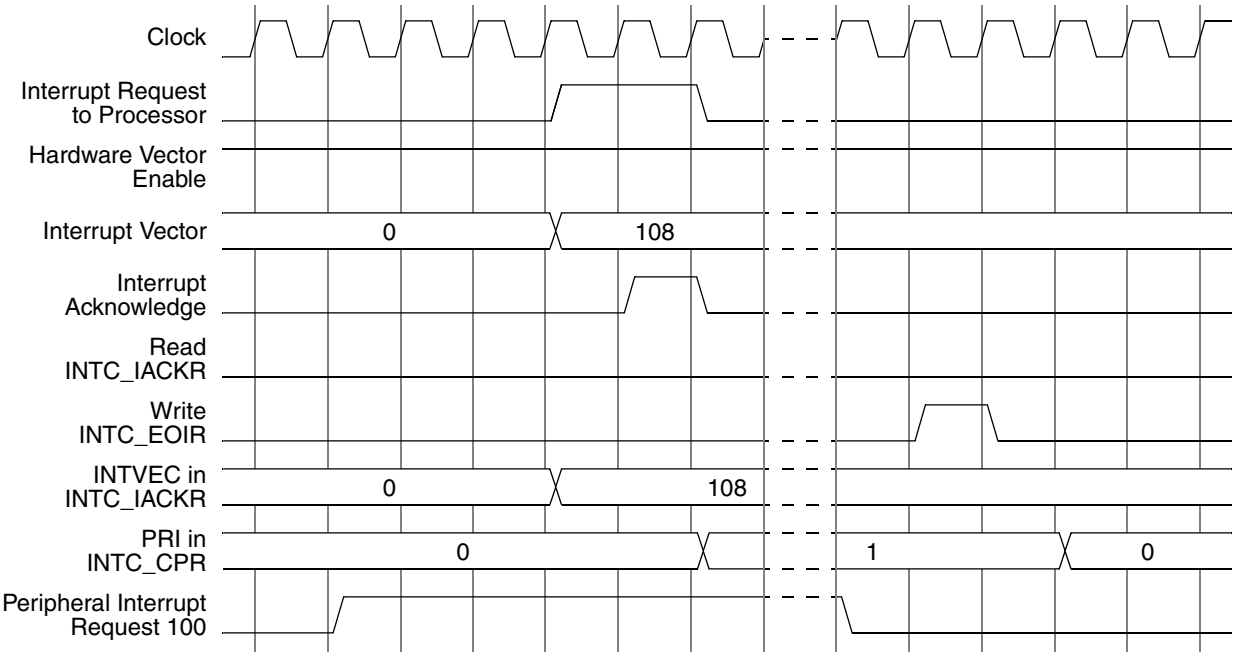


Figure 10-15. Hardware Vector Mode Handshaking Timing Diagram

10.5 Initialization and Application Information

10.5.1 Initialization Flow

After exiting reset, all of the PRI*n* fields in INTC priority select registers (INTC_PSR0–INTC_PSR329) is zero, and PRI in INTC current priority register (INTC_CPR) is 15. These reset values prevent the INTC from asserting the interrupt request to the processor. The enable or mask bits in the peripherals are reset such that the peripheral interrupt requests are negated.

An initialization sequence that allows the peripheral and software settable interrupt requests to generate an interrupt request to the processor is:

```
interrupt_request_initialization:
configure VTES and HVEN in INTC_MCR
configure VTBA in INTC_IACKR
raise the PRIn fields in INTC_PSRn
set the enable bits or clear the mask bits for the peripheral interrupt requests
lower PRI in INTC_CPR to zero
enable processor recognition of interrupts
```

10.5.2 Interrupt Exception Handler

These example interrupt exception handlers use Power Architecture assembly code.

10.5.2.1 Software Vector Mode

```
interrupt_exception_handler:
code to create stack frame, save working register, and save SRR0 and SRR1

lis      r3,INTC_IACKR@ha          # form adjusted upper half of INTC_IACKR address
lwz      r3,INTC_IACKR@l(r3)       # load INTC_IACKR, which clears request to processor
lwz      r3,0x0(r3)                # load address of ISR from vector table
wrteei   1                         # enable processor recognition of interrupts

code to save rest of context required by e500 EABI

mtlr     r3                        # move the INTC_IACKR address into the link register
blrl                               # branch to ISR; link register updated with epilog
                                   # address

epilog:
code to restore most of context required by e500 EABI

# Popping the LIFO after the restoration of most of the context and the disabling of processor
# recognition of interrupts eases the calculation of the maximum stack depth at the cost of
# postponing the servicing of the next interrupt request.
mbar                               # ensure store to clear flag bit has completed
lis      r3,INTC_EOIR@ha           # form adjusted upper half of INTC_EOIR address
li       r4,0x0                    # form 0 to write to INTC_EOIR
wrteei   0                         # disable processor recognition of interrupts
stw      r4,INTC_EOIR@l(r3)        # store to INTC_EOIR, informing INTC to lower priority

code to restore SRR0 and SRR1, restore working registers, and delete stack frame

rfi

vector_table_base_address:
address of ISR for interrupt with vector 0
address of ISR for interrupt with vector 1
         .
         .
         .
address of ISR for interrupt with vector 510
address of ISR for interrupt with vector 511


ISRx:
code to service the interrupt event
code to clear flag bit which drives interrupt request to INTC

blr                                # return to epilog
```

10.5.2.2 Hardware Vector Mode

This interrupt exception handler is useful with processor and system bus implementations that support a hardware vector. In this example, each `interrupt_exception_handler`*x* has space for only four instructions, and therefore a branch to `interrupt_ exception_handler_continued`*x* is needed.

```
interrupt_exception_handlerx:
b       interrupt_exception_handler_continuedx# 4 instructions available, branch to continue


interrupt_exception_handler_continuedx:
code to create stack frame, save working register, and save SRR0 and SRR1

wrteei   1                          # enable processor recognition of interrupts

code to save rest of context required by e500 EABI

bl       ISRx                       # branch to ISR for interrupt with vector x


epilog:
code to restore most of context required by e500 EABI

# Popping the LIFO after the restoration of most of the context and the disabling of processor
# recognition of interrupts eases the calculation of the maximum stack depth at the cost of
# postponing the servicing of the next interrupt request.
mbar                                # ensure store to clear flag bit has completed
lis      r3,INTC_EOIR@ha            # form adjusted upper half of INTC_EOIR address
li       r4,0x0                     # form 0 to write to INTC_EOIR
wrteei   0                          # disable processor recognition of interrupts
stw      r4,INTC_EOIR@l(r3)         # store to INTC_EOIR, informing INTC to lower priority

code to restore SRR0 and SRR1, restore working registers, and delete stack frame

rfi


ISRx:
code to service the interrupt event
code to clear flag bit which drives interrupt request to INTC

blr                                 # branch to epilog
```

10.5.3 ISR, RTOS, and Task Hierarchy

The RTOS and all of the tasks under its control typically execute with PRI in INTC current priority register (INTC_CPR) having a value of 0. The RTOS execute the tasks according to whatever priority scheme that it has, but that priority scheme is independent and has a lower priority of execution than the priority scheme of the INTC. In other words, the ISRs execute above INTC_CPR priority 0 and outside the control of the RTOS, the RTOS executes at INTC_CPR priority 0, and while the tasks execute at different priorities under the control of the RTOS, they also execute at INTC_CPR priority 0.

If a task shares a resource with an ISR and the PCP is being used to manage that shared resource, then the task's priority can be elevated in the INTC_CPR while the shared resource is being accessed.

An ISR whose PRI*n* in INTC priority select registers (INTC_PSR0–INTC_PSR329) has a value of 0 does not cause an interrupt request to the processor, even if its peripheral or software settable interrupt request is asserted. For a peripheral interrupt request, not setting its enable bit or disabling the mask bit causes it to remain negated, which consequently also does not cause an interrupt request to the processor. Since the ISRs are outside the control of the RTOS, this ISR does not run unless called by another ISR or the interrupt exception handler, perhaps after executing another ISR.

10.5.4 Order of Execution

An ISR with a higher priority can preempt an ISR with a lower priority, regardless of the unique vectors associated with each of their peripheral or software settable interrupt requests. However, if multiple peripheral or software settable interrupt requests are asserted, more than one has the highest priority, and that priority is high enough to cause preemption, the INTC selects the one with the lowest unique vector regardless of the order in time that they asserted. However, the ability to meet deadlines with this scheduling scheme is no less than if the ISRs execute in the time order that their peripheral or software settable interrupt requests asserted.

The example in Table 10-10 shows the order of execution of both ISRs with different priorities, and with the same priority.

Table 10-10. Order of ISR Execution Example

Step	Step Description	Code Executing At End of Step						PRI in INTC_CPR at End of Step
		RTOS	ISR108[1]	ISR208	ISR308	ISR408	Interrupt Exception Handler	
1	RTOS at priority 0 is executing.	X						0
2	Peripheral interrupt request 100 at priority 1 asserts. Interrupt taken.		X					1
3	Peripheral interrupt request 400 at priority 4 asserts. Interrupt taken.					X		4
4	Peripheral interrupt request 300 at priority 3 asserts.					X		4
5	Peripheral interrupt request 200 at priority 3 asserts.					X		4
6	ISR408 completes. Interrupt exception handler writes to INTC_EOIR.						X	1
7	Interrupt taken. ISR208 starts to execute, even though peripheral interrupt request 300 asserted first.			X				3
8	ISR208 completes. Interrupt exception handler writes to INTC_EOIR.						X	1
9	Interrupt taken. ISR308 starts to execute.				X			3

Table 10-10. Order of ISR Execution Example (continued)

Step	Step Description	Code Executing At End of Step						PRI in INTC_CPR at End of Step
		RTOS	ISR108[1]	ISR208	ISR308	ISR408	Interrupt Exception Handler	
10	ISR308 completes. Interrupt exception handler writes to INTC_EOIR.						X	1
11	ISR108 completes. Interrupt exception handler writes to INTC_EOIR.						X	0
12	RTOS continues execution.	X						0

[1] ISR108 executes for peripheral interrupt request 100 because the first eight ISRs are for software settable interrupt requests.

10.5.5 Priority Ceiling Protocol

10.5.5.1 Elevating Priority

The PRI field in INTC current priority register (INTC_CPR) is elevated in the OSEK PCP to the ceiling of all of the priorities of the ISRs that share a resource. This protocol therefore allows coherent accesses of the ISRs to that shared resource.

For example, ISR1 has a priority of 1, ISR2 has a priority of 2, and ISR3 has a priority of 3. They all share the same resource. Before ISR1 or ISR2 can access that resource, they must raise the PRI value in INTC_CPR to 3, the ceiling of all of the ISR priorities. After they release the resource, the PRI value in INTC_CPR can be lowered. If they do not raise their priority, then ISR2 can preempt ISR1, and ISR3 can preempt ISR1 or ISR2, possibly corrupting the shared resource. Another possible failure mechanism is deadlock if the higher priority ISR needs the lower priority ISR to release the resource before it can continue, but the lower priority ISR can not release the resource until the higher priority ISR completes and execution returns to the lower priority ISR.

Using the PCP instead of disabling processor recognition of all interrupts eliminates the time when accessing a shared resource that all higher priority interrupts are blocked. For example, while ISR3 cannot preempt ISR1 while it is accessing the shared resource, all of the ISRs with a priority higher than 3 can preempt ISR1.

10.5.5.2 Ensuring Coherency

Non-coherent accesses to a shared resource can occur. As an example, ISR1 and ISR2 both share a resource. ISR1 has a lower priority, therefore it executes and then writes the new PRI value in the current priority register (INTC_CPR). The next instruction writes a value to a shared coherent data block.

If INTC asserts the ISR2 interrupt request to the processor just before or at the same time as the first ISR1 write, it is possible for both the ISR1 and ISR2 writes to execute while the processor responds to the INTC request, discards the transactions, and flushes the processing pipeline. However, ISR2 cannot access the data block coherently because the data block is now corrupted.

OSEK uses the GetResource and ReleaseResource system services to manage access to a shared resource. To prevent corrupting a coherent data block, use the following code to modify the PRI in INTC_CPR. Interrupts must be enabled before executing the following GetResource code sequence:

```
GetResource:
raise PRI
mbar
isync

ReleaseResource:
mbar
lower PRI
```

10.5.6 Selecting Priorities According to Request Rates and Deadlines

The selection of the priorities for the ISRs can be made using rate monotonic scheduling (RMS) or a superset of it, deadline monotonic scheduling (DMS). In RMS, the ISRs which have higher request rates have higher priorities. In DMS, if the deadline is before the next time the ISR is requested, then the ISR is assigned a priority according to the time from the request for the ISR to the deadline, not from the time of the request for the ISR to the next request for it.

For example, ISR1 executes every 100 μs, ISR2 executes every 200 μs, and ISR3 executes every 300 μs. ISR1 has a higher priority than ISR2 which has a higher priority than ISR3. However, if ISR3 has a deadline of 150 μs, then it has a higher priority than ISR2.

The INTC has 16 priorities, which can be much less than the number of ISRs. In this case, group the ISRs with other ISRs that have similar deadlines. For example, when a priority is allocated for every time the request rate doubles: ISRs with request rates around 1 ms share a priority; ISRs with request rates around 500 μs share a priority; ISRs with request rates around 250 μs share a priority, etc. With this approach, a range of ISR request rates of 2^{16} can be covered, regardless of the number of ISRs.

Reducing the number of priorities does reduce the processor's ability to meet its deadlines. However, it also allows easier management of ISRs with similar deadlines that share a resource. They do not need to use the PCP to access the shared resource.

10.5.7 Software Settable Interrupt Requests

The software settable interrupt requests can be used in two ways. They can be used to schedule a lower priority portion of an ISR and for processors to interrupt other processors in a multiple processor system.

10.5.7.1 Scheduling a Lower Priority Portion of an ISR

A portion of an ISR needs to be executed at the PRI*n* value in INTC priority select registers (INTC_PSR0–INTC_PSR329), which becomes the PRI value in INTC current priority register (INTC_CPR) with the interrupt acknowledgement. The ISR, however, can have a portion of it which does not need to be executed at this higher priority. Therefore, executing this later portion which does not need to be executed at this higher priority can prevent the execution of ISRs which do not have a higher priority

than the earlier portion of the ISR but do have a higher priority than what the later portion of the ISR needs. This preemptive scheduling inefficiency reduces the processor's ability to meet its deadlines.

One option is for the ISR to complete the earlier higher priority portion, but then schedule through the RTOS a task to execute the later lower priority portion. However, some RTOSs can require a large amount of time for an ISR to schedule a task. Therefore, a second option is for the ISR, after completing the higher priority portion, to set a SET*n* bit in INTC software set/clear interrupt registers (INTC_SSCIR0–INTC_SSCIR7). Writing a 1 to SET*n* causes a software settable interrupt request. This software settable interrupt request, which usually has a lower PRI*n* value in the INTC_PSR*n*, therefore does not cause preemptive scheduling inefficiencies.

After generating a software settable interrupt request, the higher priority ISR completes. The lower priority ISR is scheduled according to its priority. Execution of the higher priority ISR is not resumed after the completion of the lower priority ISR.

10.5.7.2 Scheduling an ISR on Another Processor

Since the SET*n* bits in the INTC_SSCIR*n* are memory mapped, processors in multiple processor systems can schedule ISRs on the other processors. One application is that one processor simply wants to command another processor to perform a piece of work, and the initiating processor does not need to use the results of that work. If the initiating processor is concerned that processor executing the software settable ISR has not completed the work before asking it to again execute that ISR, it can check if the corresponding CLR*n* bit in INTC_SSCIR*n* is asserted before again writing a 1 to the SET*n* bit.

Another application is the sharing of a block of data. For example, a first processor has completed accessing a block of data and wants a second processor to then access it. Furthermore, after the second processor has completed accessing the block of data, the first processor again wants to access it. The accesses to the block of data must be done coherently. The procedure is that the first processor writes a 1 to a SET*n* bit on the second processor. The second processor, after accessing the block of data, clears the corresponding CLR*n* bit and then writes 1 to a SET*n* bit on the first processor, informing it that it now can access the block of data.

10.5.8 Lowering Priority Within an ISR

In implementations without the software-settable interrupt requests in the INTC software set/clear interrupt registers (INTC_SSCIR0–INTC_SSCIR7), a way — besides scheduling a task through an RTOS — to prevent preemptive scheduling inefficiencies with an ISR whose work spans multiple priorities (as described in Section 10.5.7.1, “Scheduling a Lower Priority Portion of an ISR,”) is to lower the current priority. However, the INTC has a LIFO whose depth is determined by the number of priorities.

NOTE

Lowering the PRI value in INTC current priority register (INTC_CPR) within an ISR to below the ISR’s corresponding PRI value in INTC priority select registers (INTC_PSR0–INTC_PSR329) allows more preemptions than the depth of the LIFO can support.

Therefore, through its use of the LIFO the INTC does not support lowering the current priority within an ISR as a way to avoid preemptive scheduling inefficiencies.

10.5.9 Negating an Interrupt Request Outside of its ISR

10.5.9.1 Negating an Interrupt Request as a Side Effect of an ISR

Some peripherals have flag bits which can be cleared as a side effect of servicing a peripheral interrupt request. For example, reading a specific register can clear the flag bits, and consequently their corresponding interrupt requests too. This clearing as a side effect of servicing a peripheral interrupt request can cause the negation of other peripheral interrupt requests besides the peripheral interrupt request whose ISR presently is executing. This negating of a peripheral interrupt request outside of its ISR can be a desired effect.

10.5.9.2 Negating Multiple Interrupt Requests in One ISR

An ISR can clear other flag bits besides its own flag bit. One reason that an ISR clears multiple flag bits is because it serviced those other flag bits, and therefore the ISRs for these other flag bits do not need to be executed.

10.5.9.3 Proper Setting of Interrupt Request Priority

Whether an interrupt request negates outside of its own ISR due to the side effect of an ISR execution or the intentional clearing a flag bit, the priorities of the peripheral or software settable interrupt requests for these other flag bits must be selected properly. Their PRI*n* values in INTC priority select registers (INTC_PSR0–INTC_PSR329) must be selected to be at or lower than the priority of the ISR that cleared their flag bits. Otherwise, those flag bits still can cause the interrupt request to the processor to assert. Furthermore, the clearing of these other flag bits also has the same timing relationship to the writing to INTC end-of-interrupt register (INTC_EOIR) as the clearing of the flag bit that caused the present ISR to be executed. Refer to Section 10.4.3.1.2, “End-of-Interrupt Exception Handler,” for more information.

A flag bit whose enable bit or mask bit is negating its peripheral interrupt request can be cleared at any time, regardless of the peripheral interrupt request’s PRI*n* value in INTC_PSR*n*.

10.5.10 Examining LIFO contents

Normally you do not need to know the contents of the LIFO, or even how deep the LIFO is nested. Although the LIFO contents are not memory mapped, you can read the contents by popping the LIFO and reading the PRI field in the INTC current priority register (INTC_CPR). Disabling processor recognition of interrupts while examining the LIFO contents provides a coherent view of the preempted priorities.

The code sequence is:

```
pop_lifo:
store to INTC_EOIR
load INTC_CPR, examine PRI, and store onto stack
if PRI is not zero or value when interrupts were enabled, branch to pop_lifo
```

When you are finished examining the LIFO contents, you can restore it in software vector mode using the following code sequence. In hardware vector mode, reading the INTC_IACKR does not push the INTC_CPR[PRI] onto the LIFO, therefore the LIFO contents cannot be restored in hardware vector mode.

```
push_lifo:
load stacked PRI value and store to INTC_CPR
load INTC_IACKR
if stacked PRI values are not depleted, branch to push_lifo
```

NOTE

Reading the INTC_IACKR acknowledges the interrupt request to the processor and updates the INTC_CPR[PRI] with the priority of the preempting interrupt request. If the processor recognition of interrupts is disabled during the LIFO restoration, interrupt requests to the processor can go undetected. However, since the peripheral or software settable interrupt requests are not cleared, the peripheral interrupt request to the processor re-asserts when INTC_CPR[PRI] is lower than the priorities of those peripheral or software settable interrupt requests.

Chapter 11
Frequency Modulated Phase Locked Loop and System Clocks (FMPLL)

11.1 Introduction

This section describes the features and function of the FMPLL module.

11.1.1 Block Diagrams

This section contains block diagrams that illustrate the FMPLL, the clock architecture, and the various FMPLL and clock configurations that are available. The following diagrams are provided:

- Figure 11-1, “FMPLL and Clock Architecture”
- Figure 11-2, “FMPLL Bypass Mode”
- Figure 11-3, “FMPLL External Reference Mode”
- Figure 11-4, “FMPLL Crystal Reference Mode Without FM”
- Figure 11-5, “FMPLL Crystal Reference Mode With FM”
- Figure 11-6, “FMPLL Dual-Controller (1:1) Mode”

11.1.1.1 FMPLL and Clock Architecture

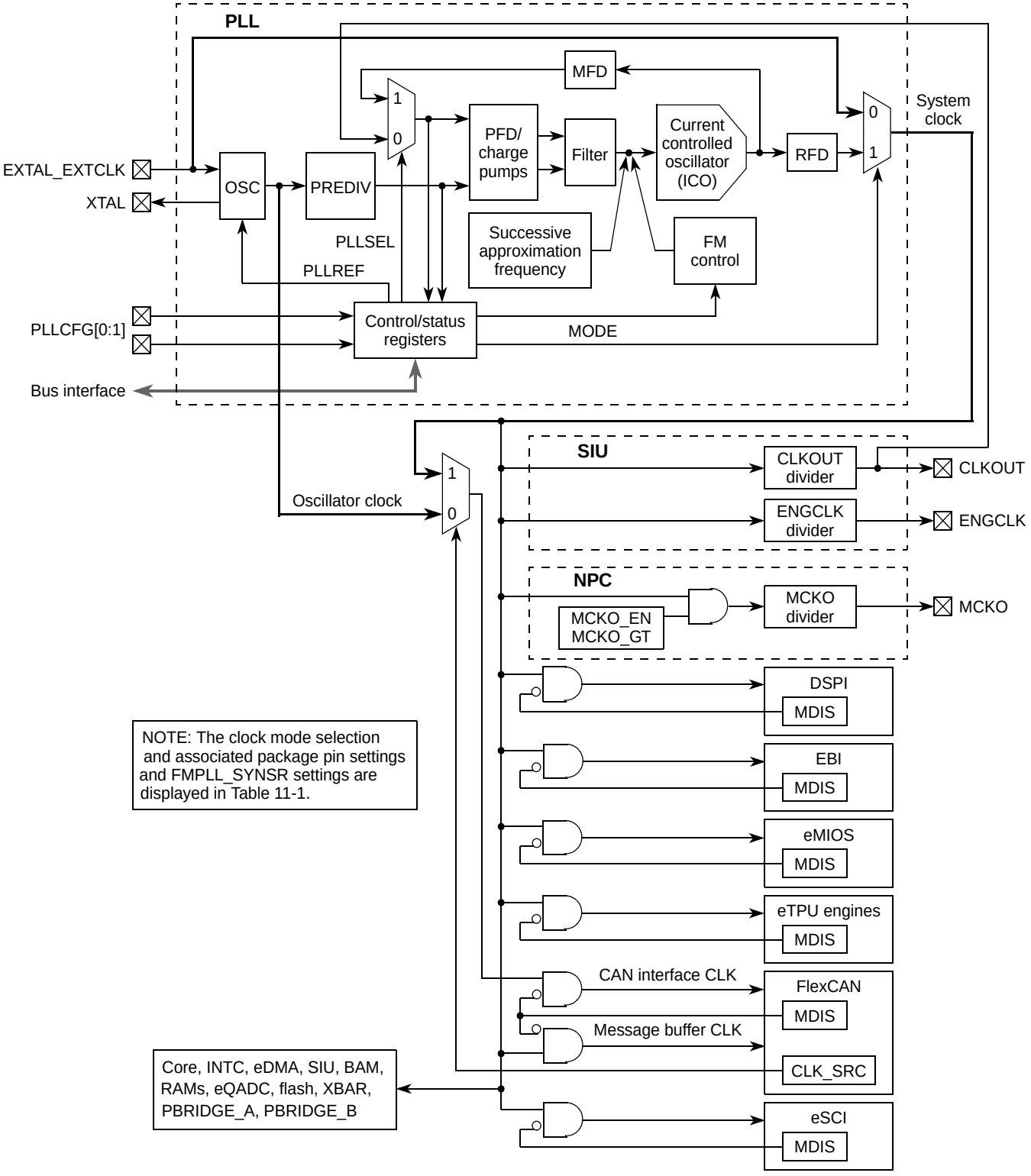


Figure 11-1. FMPLL Block and Clock Architecture

11.1.1.2 FMPLL Bypass Mode

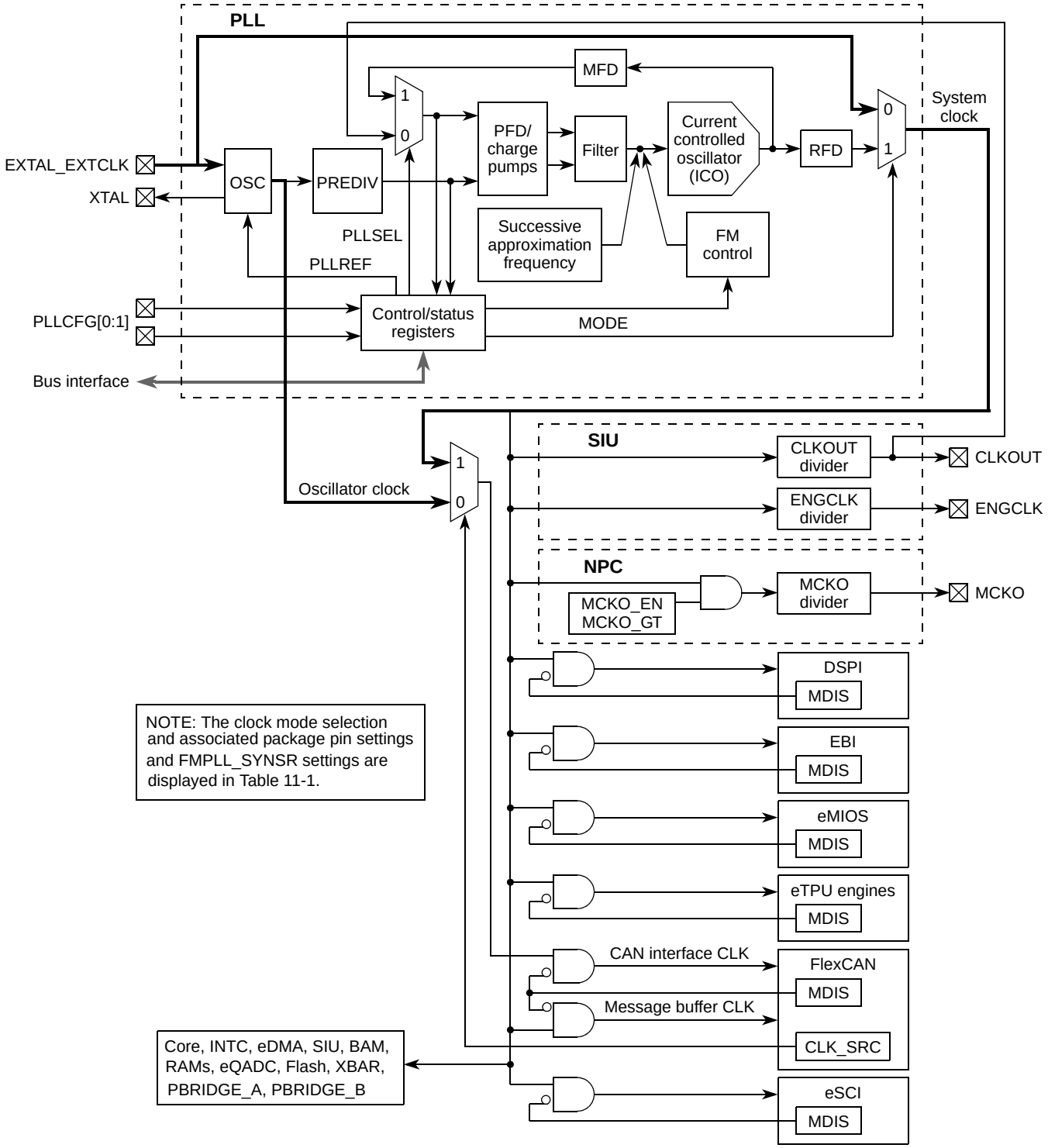


Figure 11-2. FMPLL Bypass Mode

11.1.1.3 FMPLL External Reference Mode

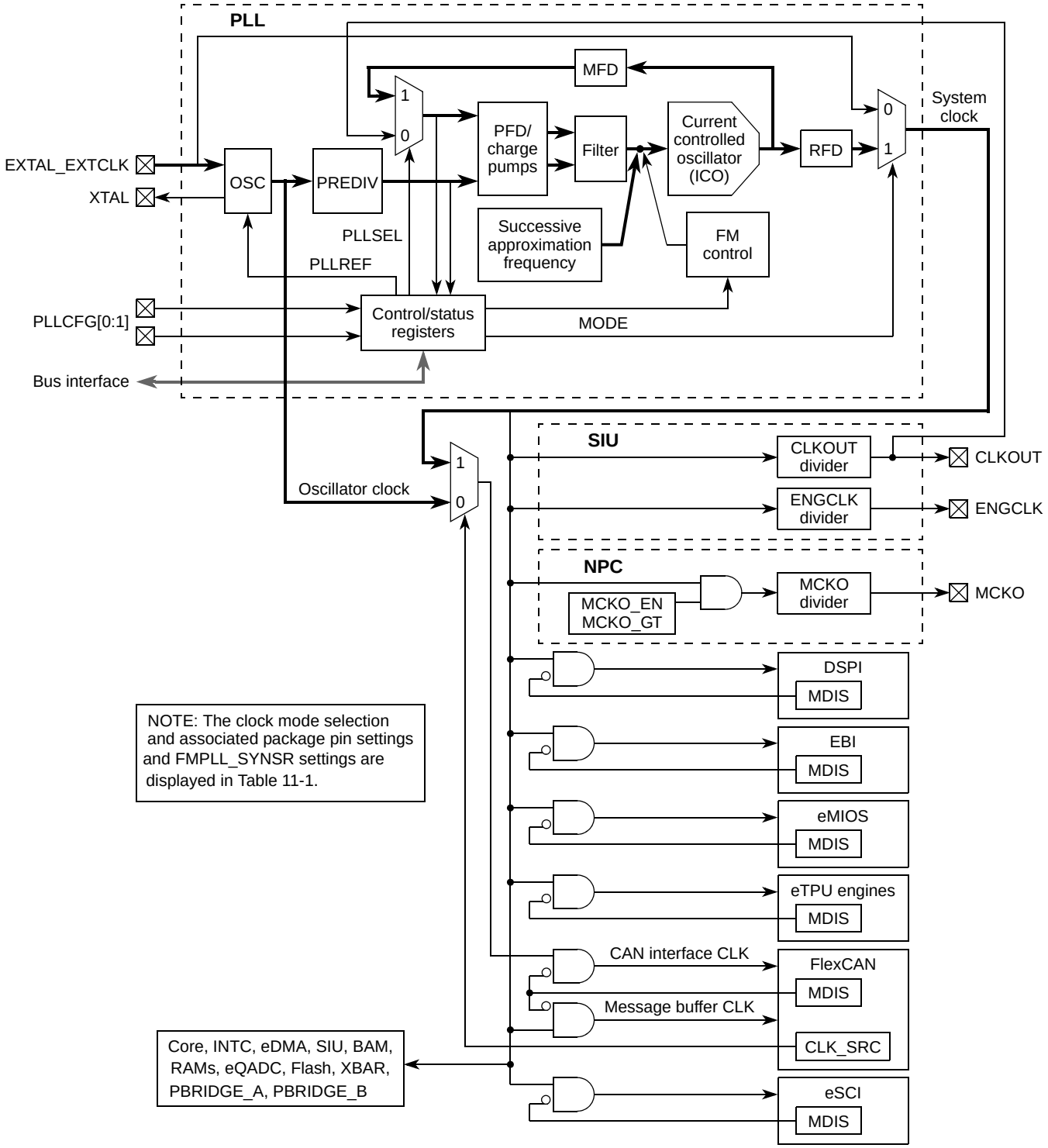


Figure 11-3. FMPLL External Reference Mode

11.1.1.4 FMPLL Crystal Reference Mode Without FM

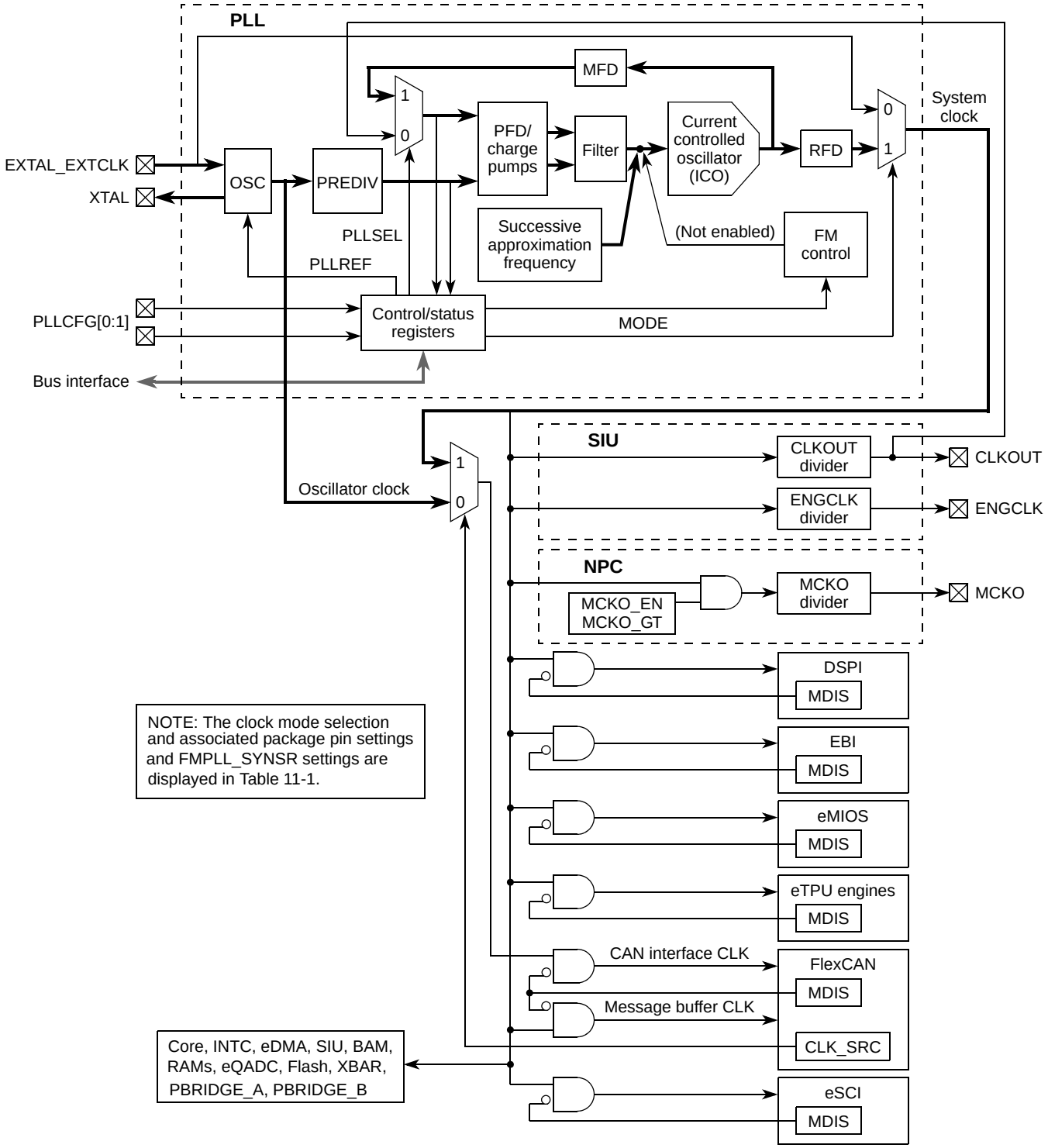


Figure 11-4. FMPLL Crystal Reference Mode without FM

11.1.1.5 FMPLL Crystal Reference Mode With FM

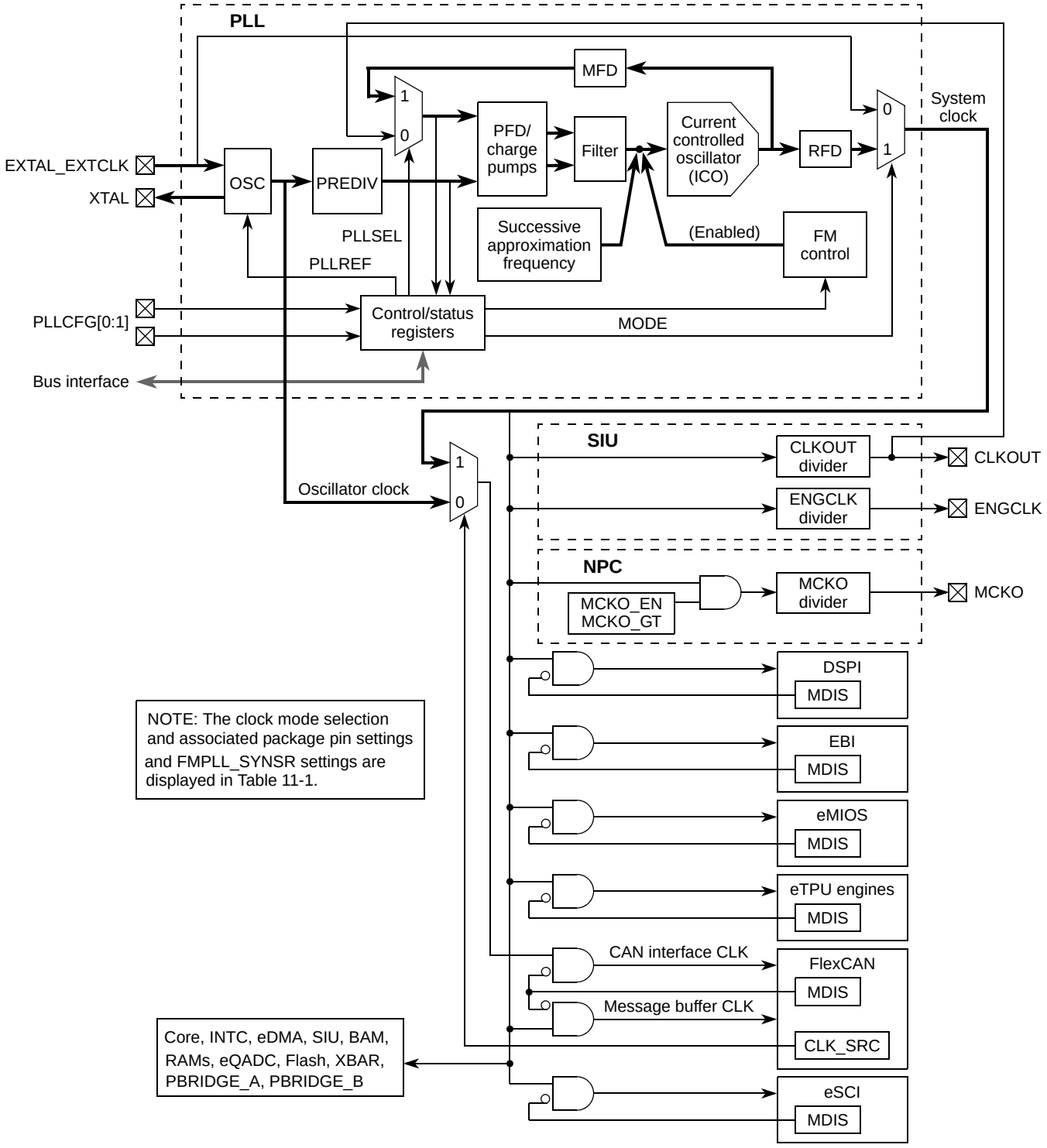


Figure 11-5. FMPLL Crystal Reference Mode with FM

11.1.1.6 FMPLL Dual-Controller Mode (1:1)

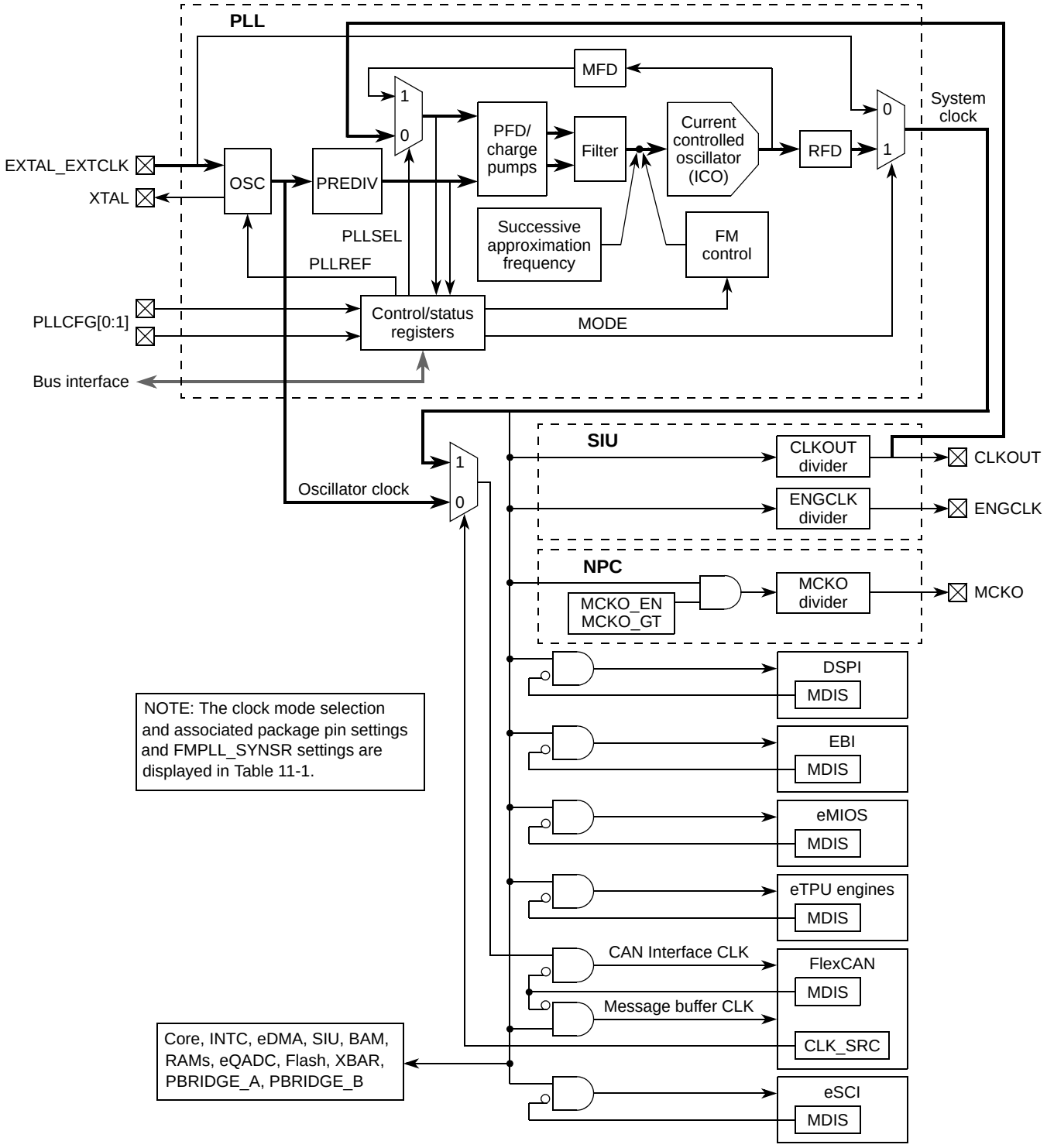


Figure 11-6. FMPLL Dual Controller (1:1) Mode

11.1.2 Overview

The frequency modulated phase locked loop (FMPLL) allows the user to generate high speed system clocks from an 8–20 MHz crystal oscillator or from an external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, reference clock pre-divider factor, output clock divider ratio, modulation depth, and modulation rate are all controllable through a bus interface.

11.1.3 Features

The FMPLL has the following major features:

- Input clock frequency from 8–20 MHz
- Current controlled oscillator (ICO) range from 48 MHz to maximum device frequency
- Reference frequency pre-divider (PREDIV) for finer frequency synthesis resolution
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the FMPLL to re-lock
- Four modes of operation:
  - Bypass mode.
  - Crystal reference mode. This is the default mode for the 416 package (with or without the 496 assembly). Refer to Section 11.1.4.1, “Crystal Reference (Default Mode).”
  - External reference mode. Refer to Section 11.1.4.2, “External Reference Mode.”
  - PLL dual-controller (1:1) mode for EXTAL_EXTCLK to CLKOUT skew minimization.
- Programmable frequency modulation
  - Modulation enabled/disabled via bus interface
  - Triangle wave modulation
  - Register programmable modulation depth (±1% to ±2% deviation from center frequency)
  - Register programmable modulation frequency dependent on reference frequency; limited to 100–250 MHz.
- Lock detect circuitry reports when the FMPLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
  - User-selectable ability to generate an interrupt request upon loss of lock. Refer to Chapter 10, “Interrupt Controller (INTC),” for details.
  - User-selectable ability to generate a system reset upon loss of lock. Refer to Chapter 4, “Reset,” for details.
- Loss-of-clock (LOC) detection for reference and feedback clocks
  - User-selectable ability to generate an interrupt request upon loss of clock. Refer to Chapter 10, “Interrupt Controller (INTC),” for details.
  - User-selectable ability to generate a system reset upon loss of clock Refer to Chapter 4, “Reset,” for details.
- Self-clocked mode (SCM) operation in event of input clock failure

11.1.4 FMPLL Modes of Operation

The FMPLL operational mode is configured during reset. For devices in the 416 package (with or without the 496 assembly if available), the FMPLL operating mode defaults to crystal reference mode. If you change the FMPLL to a different mode for devices that use these packages, the RSTCFG and PLLCFG[0:1] package pins must be driven to the state for the new mode from the time RSTOUT asserts until it negates. As shown in Table 11-3, if RSTCFG is not asserted during reset, the state of the PLLCFG package pins is ignored, and the FMPLL operates in the default crystal reference mode. The table also shows that to enter any other mode, RSTCFG must be asserted during reset.

Table 11-1 shows clock mode selection during reset configuration for the 416 (with or without the 496 assembly) pin package. Additional information on reset configuration options for the FMPLL are in Chapter 4, "Reset."

Table 11-1. Clock Mode Selection in 416 (with or without the 496 assembly) Package

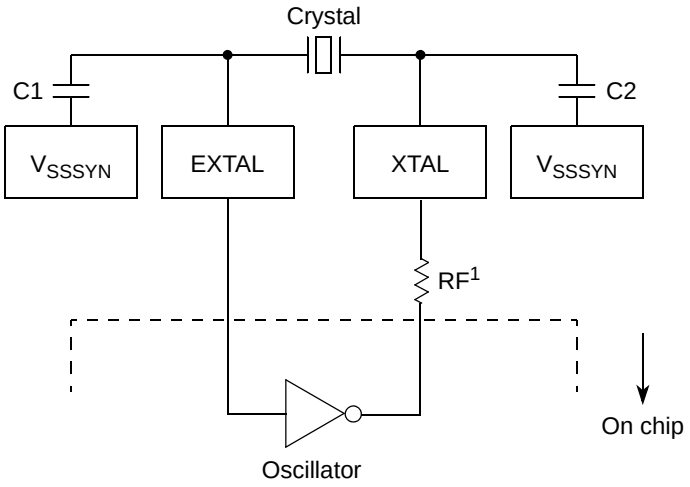
Clock Mode	Package Pins			Synthesizer Status Register (FMPLL_SYNSR)[1] Bits		
	RSTCFG	PLLCFG[0]	PLLCFG[1]	MODE	PLLSEL	PLLREF
Crystal reference (default mode)	1	PLLCFG pins ignored.		1	1	1
	0	1	0			
External reference	0	0	1	1	1	0
Bypass mode	0	0	0	0	0	0
Dual-controller mode	0	1	1	1	0	0

[1] Refer to Section 11.3.1.2, "Synthesizer Status Register (FMPLL_SYNSR)" for more information on these bits.

11.1.4.1 Crystal Reference (Default Mode)

In crystal reference mode, the FMPLL receives an input clock frequency ($F_{ref\_crystal}$) from the crystal oscillator circuit (EXTAL_EXTCLK) and the pre-divider, and multiplies the frequency to create the FMPLL output clock. You must supply a crystal oscillator that is within the appropriate input frequency range, the crystal manufacture's recommended external support circuitry, and a short signal route from the MCU to the crystal.

The external support circuitry for the crystal oscillator is shown in Figure 11-7. Example component values are shown as well. Review the actual circuit with the crystal manufacturer. A block diagram illustrating crystal reference mode is shown in Figure 11-4.



1 For an 8–20 MHz crystal, the resistor must be 1–2.8 KΩ. The exact value depends on the crystal characteristics, thus consult the crystal manufacturer.

Figure 11-7. Crystal Oscillator Network

In crystal reference mode, the FMPLL can generate a frequency modulated clock or a non-modulated clock (locked on a single frequency). The modulation rate, modulation depth, output clock divide ratio (RFD), and whether the FMPLL is modulating or not can be programmed by writing to the FMPLL registers. Crystal reference is the default clock mode for the 416 pin package. It is not necessary to force PLLCFG[0:1] to enter this mode.

PLLCFG[2] is tied low to operate in the 8–20 MHz range. Refer to FMPLL_SYNCR[PREDIV].

11.1.4.2 External Reference Mode

This external reference mode functions the same as crystal reference mode except that EXTAL_EXTCLK is driven by an external clock generator rather than a crystal oscillator. Also, the input frequency range (F_{ref_ext}) in external reference mode is the same as the input frequency reference range ($F_{ref\text{-}crystal}$) in the crystal reference mode; frequency modulation is available. To enter external reference mode, the default FMPLL configuration must be overridden by following the procedure outlined in Section 11.1.4, “FMPLL Modes of Operation.” A block diagram illustrating external reference mode is shown in Figure 11-3.

NOTE

In addition to supplying power for the CLKOUT signal, when the FMPLL is configured for external reference mode of operation, the V_{DDE5} supply voltage also controls the voltage level at which the signal presented to the EXTAL_EXTCLK pin causes a switch in the clock logic levels. The EXTAL_EXTCLK accepts a clock source with a voltage range of 1.6–3.6 V, however the transition voltage is determined by V_{DDE5} supply voltage divided by two. As an example, if V_{DDE5} is 3.3 V, then the clock transitions at approximately 1.6 V. The V_{DDE5} supply voltage and the voltage level of the external clock reference must be compatible, or the device does not clock properly.

11.1.4.3 Bypass Mode

In FMPLL bypass mode, the FMPLL is completely bypassed and the user must supply an external clock on the EXTAL_EXTCLK pin. The external clock is used directly to produce the internal system clocks. In bypass mode, the analog portion of the FMPLL is disabled and no clocks are generated at the FMPLL output. Consequently, frequency modulation is not available. In bypass mode the pre-divider is bypassed and has no effect on the system clock. The frequency in bypass mode is F_{ref_ext}.

To enter bypass mode, the default FMPLL configuration must be overridden by following the procedure outlined in Section 11.1.4, “FMPLL Modes of Operation.” A block diagram illustrating bypass mode is shown in Figure 11-2.

11.1.4.4 Dual-Controller Mode (1:1)

FMPLL dual-controller mode is used by the slave MCU device of a dual-controller system. The slave FMPLL facilitates skew reduction between the input and output clock signals. To enter dual-controller mode, the default FMPLL configuration must be overridden by the procedure outlined in Section 11.1.4, “FMPLL Modes of Operation.”

In this mode, the system clock runs at twice the frequency of the EXTAL_EXTCLK input pin and is phase aligned. Note that crystal operation is not supported in dual-controller mode and an external clock must be provided. In this mode, the frequency and phase of the signal at the EXTAL_EXTCLK pin and the CLKOUT pin of the slave MCU are matched. A block diagram illustrating dual-controller mode (1:1) is shown in Figure 11-6.

Frequency modulation is not available when configured for dual-controller mode for both the master and slave devices. Enabling frequency modulation on the device supplying the reference clock to the slave in dual-controller mode produces unreliable clocks on the slave.

NOTE

When configured for dual-controller mode, the CLKOUT clock divider on the slave device must not be changed from its reset state of divide-by-two. Increasing or decreasing this divide ratio produces unpredictable results from the FMPLL.

11.2 External Signal Description

Table 11-2 lists external signals used by the FMPLL during normal operation.

Table 11-2. PLL External Pin Interface

Name	I/O Type	Function	Pull
PLLCFG[0]_GPIO[208]	I/O	Configures the mode during reset. GPIO used otherwise.	Up
PLLCFG[1]_GPIO[209]	I/O	Configures the mode during reset. GPIO used otherwise.	Up
PLLCFG[2][1]	I	Configures the crystal oscillator range	—
XTAL	Output	Output drive for external crystal	—
EXTAL_EXTCLK	Input	Crystal external clock input	—
V_{DDSYN}	Power	Analog power supply (3.3 V ±10%)	—
V_{SSSYN}	Ground	Analog ground	—

1 In this device, PLLCFG[2] is tied to ground.

11.3 Memory Map/Register Definition

Table 11-3 shows the FMPLL memory map locations.

Table 11-3. FMPLL Module Memory Map

Address	Register Name	Register Description	Bits
Base (0xC3F8_0000)	FMPLL_SYNCR	Synthesizer control register	32
Base + 0x0004	FMPLL_SYNSR	Synthesizer status register	32
Base + 0x0008–0xC3F8_3FFF	—	Reserved	—

11.3.1 Register Descriptions

The clock operation is controlled by the synthesizer control register (FMPLL_SYNCR) and status is reported in the synthesizer status register (FMPLL_SYNSR). The following sections describe these registers in detail.

11.3.1.1 Synthesizer Control Register (FMPLL_SYNCR)

The synthesizer control register (FMPLL_SYNCR) contains bits for defining the clock operation for the system.

NOTE

To ensure proper operation for all MPC5500s, execute an **mbar** or **msync** instruction between: the write to change the FMPLL_SYNCR[MFD], and the read to check the lock status shown by FMPLL_SYNSR[LOCK].

Buffered writes to the FMPLL, as controlled by PBRIDGE_A_OPACR[BW0], must be disabled.

Address: Base + 0x0000 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	PREDIV			MFD				0	RFD				LOC EN	LOL RE	LOC RE
W																
Reset	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	DIS CLK	LOL IRQ	LOC IRQ	RATE	DEPTH		EXP									
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 11-8. Synthesizer Control Register (FMPLL_SYNCR)

Table 11-4. FMPLL_SYNCR Field Descriptions

Field	Description
0	Reserved.
1–3 PREDIV [0:2]	The PREDIV bits control the value of the divider on the input clock. The output of the pre-divider circuit generates the reference clock (F_{prediv}) to the FMPLL analog loop. When the PREDIV bits are changed, the FMPLL immediately loses lock. To prevent an immediate reset, the LOLRE bit must be cleared before writing the PREDIV bits. In 1:1 (dual-controller) mode, the PREDIV bits are ignored and the input clock is fed directly to the analog loop. 000 Divide by 1 001 Divide by 2 010 Divide by 3 011 Divide by 4 100 Divide by 5 101–111 Invalid values **Note:** Programming a PREDIV value such that the ICO operates outside its specified range causes unpredictable results and the FMPLL does not lock. Refer to the device *Data Sheet* for details on the ICO range. **Note:** To avoid unintentional interrupt requests, disable LOLIRQ before changing PREDIV and then reenable it after acquiring lock. **Note:** When using crystal reference mode or external reference mode, The PREDIV value must not be set to any value that causes the phase/frequency detector to go below 4 MHz. That is, the crystal ($F_{ref\_crystal}$) or external clock (F_{ref_ext}) frequency divided by the PREDIV value creates the F_{prediv} frequency that must be greater than or equal to 4–20 MHz. Refer to the device *Data Sheet* for F_{prediv} values. **Note:** To use the 8–20 MHz OSC, the PLL predivider must be configured for divide-by-two operation by tying PLLCFG[2] low (set PREDIV to 0b000).

Table 11-4. FMPLL_SYNCR Field Descriptions (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>4–8
MFD
[0:4]</td><td>Multiplication factor divider. The MFD bits control the value of the divider in the FMPLL feedback loop. The value specified by the MFD bits establish the multiplication factor applied to the reference frequency. The decimal equivalent of the MFD binary number is substituted into the equation from Table 11-9 for F_{sys} to determine the equivalent multiplication factor.
When the MFD bits are changed, the FMPLL loses lock. At this point, if modulation is enabled, the calibration sequence is reinitialized. To prevent an immediate reset, the LOLRE bit must be cleared before writing the MFD bits. In dual-controller mode, the MFD bits are ignored and the multiplication factor is equivalent to 2X. In bypass mode the MFD bits have no effect.
Note: Programming an MFD value such that the ICO operates outside its specified range causes unpredictable results and the FMPLL does not lock. Refer to the device Data Sheet for details on the ICO range.
Note: To avoid unintentional interrupt requests, disable LOLIRQ before changing MFD and then reenable it after acquiring lock.</td></tr>
<tr><td>9</td><td>Reserved.</td></tr>
<tr><td>10–12
RFD
[0:2]</td><td>Reduced frequency divider. The RFD bits control a divider at the output of the FMPLL. The value specified by the RFD bits establish the divisor applied to the FMPLL frequency.
<table>
<tr><th>RFD[0:2]</th><th>Output Clock Divide Ratio</th></tr>
<tr><td>000</td><td>Divide by 1</td></tr>
<tr><td>001</td><td>Divide by 2</td></tr>
<tr><td>010</td><td>Divide by 4</td></tr>
<tr><td>011</td><td>Divide by 8</td></tr>
<tr><td>100</td><td>Divide by 16</td></tr>
<tr><td>101</td><td>Divide by 32</td></tr>
<tr><td>110</td><td>Divide by 64</td></tr>
<tr><td>111</td><td>Divide by 128</td></tr>
</table>
Changing the RFD bits does not affect the FMPLL; hence, no re-lock delay is incurred. Resulting changes in clock frequency are synchronized to the next falling edge of the current system clock. However these bits must only be written when the lock bit (LOCK) is set, to avoid exceeding the allowable system operating frequency. In bypass mode, the RFD bits have no effect.</td></tr>
<tr><td>13
LOCEN</td><td>Loss-of-clock enable. The LOCEN bit determines whether the loss of clock function is operational. Refer to Section 11.4.2.6, “Loss-of-Clock Detection” and Section 11.4.2.6.1, “Alternate and Backup Clock Selection” for more information.
In bypass mode, this bit has no effect.
LOCEN does not affect the loss of lock circuitry.
0 Loss of clock disabled.
1 Loss of clock enabled.</td></tr>
</table>

Table 11-4. FMPLL_SYNCR Field Descriptions (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>14
LOLRE</td><td>Loss-of-lock reset enable. The LOLRE bit determines how the integration module (the SIU) handles a loss of lock indication. When operating in crystal reference, external reference, or dual-controller mode, the FMPLL must be locked before setting the LOLRE bit. Otherwise reset is immediately asserted. The LOLRE bit has no effect in bypass mode.
0 Ignore loss of lock, reset not asserted.
1 Assert reset on loss of lock. Reset remains asserted, regardless of the source of reset, until after the FMPLL has locked.</td></tr>
<tr><td>15
LOCRE</td><td>Loss-of-clock reset enable. The LOCRE bit determines how the integration module (the SIU) handles a loss of clock condition when LOCEN = 1. LOCRE has no effect when LOCEN = 0. If the LOCF bit in the SYNSR indicates a loss of clock condition, setting the LOCRE bit causes an immediate reset. In bypass mode LOCRE has no effect.
0 Ignore loss of clock, reset not asserted.
1 Assert reset on loss of clock.</td></tr>
<tr><td>16
DISCLK</td><td>Disable CLKOUT. The DISCLK bit determines whether CLKOUT is active. When CLKOUT is disabled it is driven low.
0 CLKOUT driven normally
1 CLKOUT driven low</td></tr>
<tr><td>17
LOLIRQ</td><td>Loss-of-lock interrupt request. The LOLIRQ bit enables an interrupt request for LOLF when it (LOLIRQ) is asserted and when LOLF is asserted. If either LOLF or LOLIRQ is negated, the interrupt request is negated. When operating in crystal reference, external reference, or dual-controller mode, the FMPLL must be locked before setting the LOLIRQ bit. Otherwise an interrupt is immediately requested. The LOLIRQ bit has no effect in bypass mode.
0 Ignore loss of lock, interrupt not requested
1 Request interrupt</td></tr>
<tr><td>18
LOCIRQ</td><td>Loss-of-clock interrupt request. The LOCIRQ bit determines how the integration module (the SIU) handles a loss of clock condition when LOCEN = 1. LOCIRQ has no effect when LOCEN = 0. If the LOCF bit in the SYNSR indicates a loss of clock condition, setting (or having previously set) the LOCIRQ bit causes an interrupt request. In bypass mode LOCIRQ has no effect.
0 Ignore loss of clock, interrupt not requested
1 Request interrupt on loss of clock.</td></tr>
<tr><td>19
RATE</td><td>Modulation rate. Controls the rate of frequency modulation applied to the system frequency. The allowable modulation rates are shown below. Changing the rate by writing to the RATE bit initiates the FM calibration sequence.
<table>
<tr><th>RATE</th><th>Modulation Rate (Hz)</th></tr>
<tr><td rowspan="2">0</td><td>$F_{mod} = F_{ref\_crystal} \div [(PREDIV + 1) \times 80]$</td></tr>
<tr><td>$F_{mod} = F_{ref\_ext} \div [(PREDIV + 1) \times 80]$</td></tr>
<tr><td rowspan="2">1</td><td>$F_{mod} = F_{ref\_crystal} \div [(PREDIV + 1) \times 40]$</td></tr>
<tr><td>$F_{mod} = F_{ref\_ext} \div [(PREDIV + 1) \times 40]$</td></tr>
</table>
Note: To prevent unintentional interrupt requests, clear LOLIRQ before changing RATE.
Note: F_{mod} must be between 100–250 MHz. Refer to Section 11.4.3.2, “Programming System Clock Frequency with Frequency Modulation.”</td></tr>
</table>

Table 11-4. FMPLL_SYNCR Field Descriptions (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>20–21
DEPTH
[0:1]</td><td>Controls the frequency modulation depth and enables the frequency modulation. When programmed to a value other than 0x0, the frequency modulation is automatically enabled. The programmable frequency deviations from the system frequency are shown below. If the depth is changed to a value other than 0x0, the calibration sequence is reinitialized.
<table>
<tr><th>DEPTH[1]</th><th>DEPTH[0]</th><th>Modulation Depth (% of Fsys)</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1.0 ± 0.2</td></tr>
<tr><td>1</td><td>0</td><td>2.0 ± 0.2</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
Note: To prevent unintentional interrupt requests, clear LOLIRQ before changing DEPTH.</td></tr>
<tr><td>22–31
EXP
[0:9]</td><td>Expected difference value. Holds the expected value of the difference of the reference and the feedback counters. Refer to Section 11.4.3.3, “FM Calibration Routine” to determine the value of these bits. This field is written by the application before entering calibration mode.</td></tr>
</table>

11.3.1.2 Synthesizer Status Register (FMPLL_SYNSR)

The synthesizer status register (FMPLL_SYNSR) is a 32-bit register. Only the LOLF and LOCF flag bits are writable in this register. Writes to bits other than the LOLF and LOCF have no effect.

Address: Base + 0x0004 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	LOLF	LOC	MODE	PLL SEL	PLL REF	LOCKS	LOCK	LOCF	CALD ONE	CAL PASS
W							w1c							w1c		
Reset	0	0	0	0	0	0	0	0	—[1]	—[1]	—[1]	—[1]	—[2]	0	0	0

[1] Reset state determined during reset configuration. (Refer to Section 11.1.4, “FMPLL Modes of Operation,” for more information.)

[2] Reset state determined during reset.

Note: “w1c” signifies that this bit is cleared by writing a 1 to it.

Figure 11-9. Synthesizer Status Register (FMPLL_SYNSR)

Table 11-5. FMPLL_SYNSR Field Descriptions

Field	Description
0–21	Reserved.
22 LOLF	Loss-of-lock flag. Provides the interrupt request flag. This is a write 1 to clear (w1c) bit; to clear the flag, the user must write a 1 to the bit. Writing 0 has no effect. This flag is not set and an interrupt is not requested, if the loss-of-lock condition was caused by: • a system reset • a write to the FMPLL_SYNCR which modifies the MFD bits • enabling frequency modulation If the flag is set due to a system failure, writing the MFD bits or enabling FM does not clear the flag. Asserting reset clears the flag. This flag bit is sticky; if lock is reacquired, the bit remains set until either a write of 1 or reset is asserted. 0 Interrupt service not requested 1 Interrupt service requested **Note:** Upon a loss-of-lock that is not generated by: •a system reset •a write to the FMPLL_SYNCR that modifies the MFD or PREDIV bits •enabling of frequency modulation the LOLF is set *only if* LOLIRQ is set. If the FMPLL reacquires lock and any of the previous conditions in the bulleted list occurs, the LOLF is set again. To avoid generating an unintentional interrupt, clear LOLIRQ before changing MFD or PREDIV, or before enabling FM after a previous interrupt and relock occurred.
23 LOC	Loss-of-clock status. Indicates whether a loss-of-clock condition is present when operating in crystal reference, external reference, or dual-controller mode, If LOC = 0, the system clocks are operating normally. If LOC = 1, the system clocks have failed due to a reference failure or a FMPLL failure. If the read of the LOC bit and the loss-of-clock condition occur simultaneously, the bit does not reflect the current loss of clock condition. If a loss-of-clock condition occurs which sets this bit and the clocks later return to normal, this bit is cleared. A loss of clock condition can only be detected if LOCEN = 1. LOC is always 0 in bypass mode. 0 Clocks are operating normally 1 Clocks are not operating normally.
24 MODE	Clock mode. Determined at reset, this bit indicates which clock mode the system is utilizing. Refer to Chapter 4, “Reset,” for details on how to configure the system clock mode during reset. 0 PLL bypass mode. 1 PLL clock mode.
25 PLLSEL	PLL mode select. Determined at reset, this bit indicates in which mode the FMPLL operates. This bit is cleared in dual-controller and bypass mode. Refer to Chapter 4, “Reset,” for details on how to configure the system clock mode during reset. Refer to Table 11-1 for more information. 0 Dual-controller mode. 1 Crystal reference or external reference mode.

Table 11-5. FMPLL_SYNSR Field Descriptions (continued)

Field	Description
26 PLLREF	PLL clock reference source. Determined at reset, this bit indicates whether the PLL reference source is an external clock or a crystal reference. This bit is cleared in dual controller mode and bypass mode. Refer to Chapter 4, "Reset," for details on how to configure the system clock mode during reset. 0 External clock reference chosen. 1 Crystal clock reference chosen.
27 LOCKS	Sticky FMPLL lock status bit. A sticky indication of FMPLL lock status. LOCKS is set by the lock detect circuitry when the FMPLL acquires lock after one of the following: • System reset • Write to the FMPLL_SYNCR that modifies the MFD and PREDIV bits • Enable frequency modulation Whenever the FMPLL loses lock, LOCKS is cleared. LOCKS remains cleared even after the FMPLL relocks, until one of the three previously-stated conditions occurs. Furthermore, if the LOCKS bit is read when the FMPLL simultaneously loses lock, the bit does not reflect the current loss of lock condition. If operating in bypass mode, LOCKS remains cleared after reset. In crystal reference, external reference, and dual-controller mode, LOCKS is set after reset. 0 PLL has lost lock since last system reset, a write to FMPLL_SYNCR to modify the MFD and PREDIV bit fields, or frequency modulation enabled. 1 PLL has not lost lock since last system reset, a write to FMPLL_SYNCR to modify the MFD and PREDIV bit fields, or frequency modulation enabled.
28 LOCK	PLL lock status bit. Indicates whether the FMPLL has acquired lock. If the LOCK bit is read when the FMPLL simultaneously loses lock or acquires lock, the bit does not reflect the current condition of the FMPLL. If operating in bypass mode, LOCK remains cleared after reset. Refer to the frequency as defined in the *MPC5566 Microcontroller Data Sheet* for the lock/unlock range. 0 PLL is unlocked. 1 PLL is locked.
29 LOCF	Loss-of-clock flag. This bit provides the interrupt request flag. This is a write 1 to clear (w1c) bit; to clear the flag, the user must write a 1 to the bit. Writing 0 has no effect. Asserting reset clears the flag. This flag is sticky in the sense that if clocks return to normal after the flag has been set, the bit remains set until cleared by either writing 1 or asserting reset. 0 Interrupt service not requested 1 Interrupt service requested

Table 11-5. FMPLL_SYNSR Field Descriptions (continued)

Field	Description
30 CALDONE	Calibration complete. Indicates whether the calibration sequence has been completed since the last time modulation was enabled. If CALDONE = 0 then the calibration sequence is either in progress or modulation is disabled. If CALDONE = 1 then the calibration sequence has been completed, and frequency modulation is operating. 0 Calibration not complete. 1 Calibration complete. **Note:** FM relocking does not start until calibration is complete.
31 CALPASS	Calibration passed. Indicates whether the calibration routine was successful. If CALPASS = 1 and CALDONE = 1 then the routine was successful. If CALPASS = 0 and CALDONE = 1, then the routine was unsuccessful. When the calibration routine is initiated the CALPASS is asserted. CALPASS remains asserted until either modulation is disabled by clearing the DEPTH bits in the FMPLL_SYNCR or a failure occurs within the FMPLL calibration sequence. 0 Calibration unsuccessful. 1 Calibration successful. If calibration is unsuccessful, then actual depth is not guaranteed to match the desired depth.

11.4 Functional Description

This section explains clock architecture, clock operation, and clock configuration.

11.4.1 Clock Architecture

This section describes the clocks and clock architecture in the MCU.

11.4.1.1 Overview

The system clocks are generated from one of four FMPLL modes: crystal reference mode, external reference mode, dual-controller (1:1) mode, and bypass mode. Refer to Section 11.1, “Introduction” for information on the different clocking modes available in the FMPLL.

The peripheral IP modules have been designed to allow software to gate the clocks to the non-memory-mapped logic of the modules.

The MCU has three clock output pins that are driven by programmable clock dividers. The clock dividers divide the system clock down by even integer values. The three clock output pins are the following:

- CLKOUT – External address/data bus clock
- MCKO – Nexus auxiliary port clock
- ENGCLK – Engineering clock

The MCU has been designed so that the oscillator clock can be selected as the clock source for the CAN interface in the FlexCAN blocks resulting in very low jitter performance.

Figure 11-1 shows a block diagram of the FMPLL and the system clock architecture.

11.4.1.2 Software Controlled Power Management/Clock Gating

Some of the IP modules on this device support software controlled power management/clock gating whereby the application software can disable the non-memory-mapped portions of the modules by writing to module disable (MDIS) bits in registers within the modules. The memory-mapped portions of the modules are clocked by the system clock when they are being accessed. The NPC can be configured to disable the MCKO signal when there are no Nexus messages pending. The H7FA flash array can be disabled by writing to a bit in the Flash register map.

The modules that implemented software controlled power management and clock gating are listed in Table 11-6 along with the registers and bits that disable each module. The software controlled clocks are enabled when the MCU comes out of reset.

Table 11-6. Software Controlled Power Management/Clock Gating Support

Module Name	Register Name	Bit Names
DSPI A	DSPI_A_MCR	MDIS
DSPI B	DSPI_B_MCR	MDIS
DSPI C	DSPI_C_MCR	MDIS
DSPI D	DSPI_D_MCR	MDIS
EBI	EBI_MCR	MDIS
eTPU engine A	ETPU_ECR_1	MDIS
eTPU engine B	ETPU_ECR_2	MDIS
FlexCAN A	CAN_A_MCR	MDIS
FlexCAN B	CAN_B_MCR	MDIS
FlexCAN C	CAN_C_MCR	MDIS
FlexCAN D	CAN_D_MCR	MDIS
eMIOS	EMIOS_MCR	MDIS
eSCI A	ESCI_A_CR2	MDIS
eSCI B	ESCI_B_CR2	MDIS
Nexus port controller (NPC)	NPC_PCR	MCKO_EN, MCKO_GT [1]
Flash array	FLASH_MCR	STOP [2]

[1] Refer to Chapter 25, “Nexus Development Interface.”

[2] Refer to Chapter 13, “Flash Memory.”

11.4.1.3 Clock Dividers

Each of the CLKOUT, MCKO, and ENGCLK dividers provides a nominal 50% duty cycle clock to an output pin. There is no guaranteed phase relationship between CLKOUT, MCKO, and ENGCLK. ENGCLK is not synchronized to any I/O pins.

11.4.1.3.1 External Bus Clock (CLKOUT)

The external bus clock (CLKOUT) divider can be programmed to divide the system clock by two or four based on the settings of the EBDF bit field in the SIU external clock control register (SIU_ECCR). The reset value of the EBDF selects a CLKOUT frequency of one half of the system clock frequency. The EBI supports gating of the CLKOUT signal when there are no external bus accesses in progress. Refer to the Chapter 6, “System Integration Unit (SIU)” for more information on CLKOUT.

The hold-time for the external bus pins can be changed by writing to the external bus tap select (EBTS) bit in the SIU_ECCR. Refer to Chapter 6, “System Integration Unit (SIU)” for more information.

11.4.1.3.2 Nexus Message Clock (MCKO)

The Nexus message clock (MCKO) divider can be programmed to divide the system clock by two, four or eight based on the MCKO_DIV bit field in the port configuration register (PCR) in the Nexus port controller (NPC). The reset value of the MCKO_DIV selects an MCKO clock frequency one half of the system clock frequency. The MCKO divider is configured by writing to the NPC through the JTAG port. Refer to Chapter 25, “Nexus Development Interface” for more information.

11.4.1.3.3 Engineering Clock (ENGCLK)

The engineering clock (ENGCLK) divider can be programmed to divide the system clock by factors from 2 to 126 in increments of two. The ENGDIV bit field in the SIU_ECCR determines the divide factor. The reset value of ENGDIV selects an ENGCLK frequency of system clock divided by 32.

11.4.1.3.4 FlexCAN_*x* Clock Domains

The FlexCAN modules have two distinct software controlled clock domains. One of the clock domains is always derived from the system clock. This clock domain includes the message buffer logic. The source for the second clock domain can be either the system clock or a direct feed from the oscillator pin EXTAL_EXTCLK. The logic in the second clock domain controls the CAN interface pins. The CLK_SRC bit in the FlexCAN CTRL register selects between the system clock and the oscillator clock as the clock source for the second domain. Selecting the oscillator as the clock source ensures very low jitter on the CAN bus. System software can gate both clocks by writing to the MDIS bit in the FlexCAN MCR register. Figure 11-1 shows the two clock domains in the FlexCAN modules.

Refer to Chapter 22, “FlexCAN2 Controller Area Network” for more information on the FlexCAN modules.

11.4.1.3.5 FEC Clocks

The FEC TX_CLK and FEC_RX_CLK are inputs. An external source provides the clocks to these pins.

11.4.2 Clock Operation

11.4.2.1 Input Clock Frequency

The FMPLL is designed to operate over an input clock frequency range as determined by the operating mode. The operating ranges for each mode are given in Table 11-7.

Table 11-7. Input Clock Frequency

Mode	Symbol	Input Frequency Range
Crystal reference External reference	$F_{ref\_crystal}$ F_{ref_ext}	8–20 MHz
Bypass	F_{extal}	0–132 MHz
Dual-controller (1:1)	$F_{ref\_1:1}$	25–66 MHz

11.4.2.2 Reduced Frequency Divider (RFD)

The RFD can be used for reducing the FMPLL system clock frequency. To protect the system from frequency overshoot during the PLL lock detect phase, the RFD must be programmed to be greater than or equal to 1 when changing MFD or PREDIV or when enabling frequency modulation.

11.4.2.3 Programmable Frequency Modulation

The FMPLL provides for frequency modulation of the system clock. The modulation is applied as a triangular waveform with modulation depth and rate controlled by fields in the FMPLL_SYNCR. The modulation depth can be set to ±1% or ±2% of the system frequency. The modulation rate is dependent on the reference clock frequency.

Complete details for configuring the programmable frequency modulation is given in Section 11.4.3.2, “Programming System Clock Frequency with Frequency Modulation.”

11.4.2.4 FMPLL Lock Detection

A pair of counters monitor the reference and feedback clocks to determine when the system has acquired frequency lock. After the FMPLL has locked, the counters continue to monitor the reference and feedback clocks and reports if/when the FMPLL has lost lock. The FMPLL_SYNCR provides the flexibility to select whether to generate an interrupt, assert system reset, or do nothing in the event that the FMPLL loses lock. Refer to Section 11.3.1.1, “Synthesizer Control Register (FMPLL_SYNCR) for details.

When the frequency modulation is enabled, the loss of lock continues to function as described but with the lock and loss of lock criteria reduced to ensure that false loss of lock conditions are not detected.

In bypass mode, the FMPLL cannot lock since the FMPLL is disabled.

11.4.2.5 FMPLL Loss-of-Lock Conditions

After the FMPLL acquires lock after reset, the FMPLL_SYNSR[LOCK] and FMPLL_SYNSR[LOCKS] status bits are set. If the MFD is changed or if an unexpected loss of lock condition occurs, the LOCK and

LOCKS status bits are negated. While the FMPLL is in an unlocked condition, the system clocks continue to be sourced from the FMPLL as the FMPLL attempts to re-lock. Consequently, during the re-locking process, the system clock frequency is not well defined and can exceed the maximum system frequency thereby violating the system clock timing specifications (when changing MFD and PREDIV, this is avoided by following the procedure detailed in Section 11.4.3, "Clock Configuration"). Because this condition can arise during unexpected loss of lock events, it is recommended to use the loss of lock reset functionality, Refer to Section 11.4.2.5.1, "FMPLL Loss-of-Lock Reset," below. However, LOLRE must be cleared while changing the MFD otherwise a reset occurs.

After the FMPLL has relocked, the LOCK bit is set. The LOCKS bit remains cleared if the loss of lock was unexpected. The LOCKS bit is set to 1 when the loss of lock was caused by changing the MFD.

11.4.2.5.1 FMPLL Loss-of-Lock Reset

The FMPLL provides the ability to assert reset when a loss of lock condition occurs by programming the FMPLL_SYNCR[LOLRE] bit. Reset is asserted if LOLRE is set and loss of lock occurs. Because the FMPLL_SYNSR[LOCK] and FMPLL_SYNSR[LOCKS] bits are reinitialized after reset, the system reset status register (SIU_RSR) must be read to determine that a loss of lock condition occurred.

To exit reset, the reference must be present and the FMPLL must acquire lock. In bypass mode, the FMPLL cannot lock. Therefore a loss of lock condition cannot occur, and LOLRE has no effect.

11.4.2.5.2 FMPLL Loss-of-Lock Interrupt Request

The FMPLL provides the ability to request an interrupt when a loss of lock condition occurs by programming the FMPLL_SYNCR[LOLIRQ] bit. An interrupt is requested by the FMPLL if LOLIRQ is set and loss of lock occurs.

In bypass mode, the FMPLL cannot lock. Therefore a loss of lock condition cannot occur, and the LOLIRQ bit has no effect.

11.4.2.6 Loss-of-Clock Detection

The FMPLL continuously monitors the reference and feedback clocks. In the event either of the clocks fall below a threshold frequency, the system reports a loss of clock condition. You can enable a feature to have the FMPLL switch the system clocks to a backup clock in the event of such a failure. Additionally, you can enter a system RESET, assert an interrupt request, or do nothing if the FMPLL reports this condition.

11.4.2.6.1 Alternate and Backup Clock Selection

If the user enables loss of clock by setting FMPLL.SYNCR[LOCEN] = 1, then the FMPLL transitions system clocks to a backup clock source in the event of a clock failure as per Table 11-8.

If loss of clock is enabled and the reference clock is the source of the failure, the FMPLL enters self-clock mode (SCM). The exact frequency during self-clock mode operation is indeterminate due to process, voltage, and temperature variation but is guaranteed to be below the maximum system frequency. If the FMPLL clocks have failed, the FMPLL transitions the system clock source to the reference clock.

The FMPLL remains in SCM until the next reset. If the FMPLL is operated in SCM, writes to FMPLL_SYNCR[RFD] have no effect on clock frequency. The SCM system frequency stated in the device *Data Sheet* assumes that the RFD has been programmed to 0x0.

If loss of clock is enabled and the loss-of-clock is due to a FMPLL failure (for example, loss of feedback clock), the FMPLL reference becomes the system clock's source until the next reset, even if the FMPLL regains itself and re-locks.

Table 11-8. Loss of Clock Summary

Clock Mode	System Clock Source before Failure	REFERENCE FAILURE Alternate Clock Selected by LOC Circuitry until Reset	PLL FAILURE Alternate Clock Selected by LOC Circuitry until Reset
Crystal Reference External Reference	PLL	PLL self-clocked mode	PLL reference
Bypass	External clock(s)	None	N/A

A special loss of clock condition occurs when both the reference and the FMPLL fail. The failures can be simultaneous or the FMPLL can fail first. In either case, the reference clock failure takes priority and the FMPLL attempts to operate in SCM. If successful, the FMPLL remains in SCM until the next reset. During SCM, modulation is always disabled. If the FMPLL cannot operate in SCM, the system remains static until the next reset. Both the reference and the FMPLL must be functioning properly to exit reset.

11.4.2.6.2 Loss-of-Clock Reset

When a loss of clock condition is recognized, reset is asserted if the FMPLL_SYNCR[LOCRE] bit is set. The LOCF and LOC bits in FMPLL_SYNSR are cleared after reset, therefore, the SIU_RSR must be read to determine that a loss of clock condition occurred. LOCRE has no effect in bypass mode.

To exit reset in FMPLLmode, the reference must be present and the FMPLL must acquire lock.

11.4.2.6.3 Loss-of-Clock Interrupt Request

When a loss of clock condition is recognized, the FMPLL requests an interrupt if the FMPLL_SYNCR[LOCIRQ] bit is set. The LOCIRQ bit has no effect in bypass mode or if FMPLL_SYNCR[LOCEN] = 0.

11.4.3 Clock Configuration

In crystal reference and external reference clock mode, the default system frequency is determined by the MFD, RFD, and PREDIV reset values. Refer to Section 11.3.1.1, "Synthesizer Control Register (FMPLL_SYNCR)." The frequency multiplier is determined by the RFD, PREDIV, and multiplication frequency divisor (MFD) bits in FMPLL_SYNCR.

Table 11-9 shows the clock-out to clock-in frequency relationships for the possible clock modes.

Table 11-9. Clock-out vs. Clock-in Relationships

Clock Mode	PLL Option
Crystal Reference Mode	$F_{sys} = F_{ref\_crystal} \times \frac{(MFD + 4)}{[(PREDIV + 1) \times 2^{RFD}]}$
External Reference Mode	$F_{sys} = F_{ref\_ext} \times \frac{(MFD + 4)}{[(PREDIV + 1) \times 2^{RFD}]}$
Dual Controller (1:1) Mode	$F_{sys} = 2 \times F_{ref\_1:1}$
Bypass Mode	$F_{sys} = F_{ref\_ext}$

NOTES:
F_{sys} = system frequency
F_{prediv} = clock frequency after PREDIV.
$F_{ref\_crystal}$ and F_{ref_ext} = clock frequencies at the EXTAL_EXTCLK signal. (Refer to Figure 11-1).
MFD ranges from 0 to 31.
RFD ranges from 0 to 7.
PREDIV normal reset value is 0. Caution: Programming a PREDIV value such that the ICO operates outside its specified range causes unpredictable results and the FMPLL does not lock. Refer to the device *Data Sheet* for details on the ICO range.

When programming the FMPLL, do not violate the maximum system clocks frequency, or maximum and minimum ICO frequency specifications. For determining the MFD value, use a value of zero for the RFD (translates to divide-by-one). This ensures that the FMPLL does not try to synthesize a frequency out of its range. Refer to the device *Data Sheet* for more information.

11.4.3.1 Programming System Clock Frequency Without Frequency Modulation

The following steps are required to accommodate the frequency overshoot that can occur when the PREDIV or MFD bits are changed. If frequency modulation is going to be enabled, the maximum allowable frequency must be reduced by the programmed ΔF_m.

NOTE

Following these steps produces immediate changes in supply current, therefore make sure the power supply is decoupled with low ESR capacitors.

The following steps program the clock frequency without frequency modulation:

1. Determine the value for the PREDIV, MFD, and RFD fields in the synthesizer control register (FMPLL_SYNCR). Remember to include the ΔF_m if frequency modulation is enabled. The amount of jitter in the system clocks can be minimized by selecting the maximum MFD factor that can be paired with an RFD factor to provide the desired frequency. The maximum MFD value that can be used is determined by the ICO range. Refer to the *Data Sheet* for the maximum frequency of the ICO.
2. Change the following in FMPLL_SYNCR:
   a) Make sure frequency modulation is disabled (FMPLL_SYNCR[DEPTH] = 00). A change to PREDIV, MFD, or RATE while modulation is enabled invalidates the previous calibration results.
   b) Clear FMPLL_SYNCR[LOLRE]. If this bit is set, the MCU goes into reset when MFD is written.
   c) Initialize the FMPLL for less than the desired final system frequency (done in one single write to FMPLL_SYNCR):
      – Disable LOLIRQ.
      – Write FMPLL_SYNCR[PREDIV] to a desired final value.
      – Write FMPLL_SYNCR[MFD] to a desired final value.
      – Write the RFD control field value to a desired final RFD value plus one.
3. Wait for the FMPLL to lock by monitoring the FMPLL_SYNSR[LOCK] bit. Refer to Section 11.3.1.1, "Synthesizer Control Register (FMPLL_SYNCR)," for memory synchronization between changing FMPLL_SYNCR[MFD] and monitoring the lock status.
4. Initialize the FMPLL to the desired final system frequency by changing FMPLL_SYNCR[RFD]. The FMPLL does not need to re-lock if only the RFD changes, and the RFD must be set to greater than one to protect from overshoot.
5. Re-enable LOLIRQ.

NOTE

When using crystal reference mode or external reference mode, do not set the PREDIV value to any value that causes the phase and frequency detector to go below 4 MHz. That is, the crystal or external clock frequency divided by the PREDIV value must be in the range of 4–20 MHz.

NOTE

This first register write causes the FMPLL to switch to an initial system frequency which is less than the final one. Keeping the change of frequency to a lower initial value helps minimize the current surge to the external power supply caused by the change in frequency. The last step changes the RFD to get the desired final frequency.

NOTE

Changing the MFD or PREDIV values causes the FMPLL to perform a search for the lock frequency that results in the system clock frequency changing rapidly across the complete frequency range. All MCU peripherals, including the external bus are subjected to this frequency sweep. Operation of timers and serial communications during this search sequence produces unpredictable results.

11.4.3.2 Programming System Clock Frequency with Frequency Modulation

In crystal reference and external reference clock modes, the default mode is without frequency modulation enabled. When frequency modulation is enabled, however, three parameters must be set to generate the desired level of modulation: the RATE, DEPTH, and EXP bit fields of the FMPLL_SYNCR. RATE and DEPTH determine the modulation rate and the modulation depth. The EXP field controls the FM calibration routine. Section 11.4.3.3, "FM Calibration Routine," shows how to obtain the values to be programmed for EXP. Figure 11-10 illustrates the effects of the parameters and the modulation waveform built into the modulation hardware. The modulation waveform is always a triangle wave and its shape is not programmable.

The modulation rates given are specific to a reference frequency of 8 MHz. F_{prediv} is the frequency after the predivider.

$$F_{mod} = F_{ref\_crystal} \quad \text{or} \quad F_{ref\_ext} \div [(PREDIV + 1) \times Q]$$

where:

Q = 40 or 80. This gives modulation rates of 200 kHz and 100 kHz, respectively.

NOTE

The following relationship between F_{mod} and modulation rates must be maintained:

$$100\ KHz \leq F_{mod} \leq 250\ KHz$$

Therefore, the use of a non 8 MHz reference results in scaled modulation rates.

Here are the steps to program the clock frequency with frequency modulation. These steps ensure proper operation of the calibration routine and prevent frequency overshoot from the sequence:

1. Change the following in FMPLL_SYNCR:
   a) Make sure frequency modulation is disabled (FMPLL_SYNCR[DEPTH] = 00). A change to PREDIV, MFD, or RATE while modulation is enabled invalidates the previous calibration results.
   b) Clear FMPLL_SYNCR[LOLRE]. If this bit is set, the MCU goes into reset when MFD is written.
   c) Initialize the FMPLL for less than the desired final frequency:
   — Disable LOLIRQ.
   — Write FMPLL_SYNCR[PREDIV] to the desired final value.

— Write FMPLL_SYNCR[MFD] to the desired final value.
— Write FMPLL_SYNCR[EXP] to the desired final value.
— Write FMPLL_SYNCR[RATE] to the desired final value.
— Write the RFD control field to 1 plus the desired final RFD value (RFD must be greater than one to protect from overshoot).

2. Wait for the FMPLL to lock by monitoring the FMPLL_SYNSR[LOCK] bit. Refer to Section 11.3.1.1, "Synthesizer Control Register (FMPLL_SYNCR)," for memory synchronization between changing FMPLL_SYNCR[MFD] and monitoring the lock status.
3. If using the frequency modulation feature, then:
   a) Enable FM by setting FMPLL_SYNCR[DEPTH] = 1 or 2.
   b) Also set FMPLL_SYNCR[RATE] if not done previously in step 2.
4. Calibration starts. After calibration is done, then the FMPLL re-locks. Wait for the FMPLL to re-lock by monitoring the FMPLL_SYNSR[LOCK] bit.
5. Verify FM calibration completed and was successful by testing the FMPLL_SYNSR[CALDONE] and FMPLL_SYNSR[CALPASS] bitfields.
6. If FM calibration did not complete or was not successful, attempt again by going back to step 1.
7. Initialize the FMPLL to the desired final system frequency by changing FMPLL_SYNCR[RFD]. Note that the FMPLL does not need to re-lock when only changing the RFD.
8. Re-enable LOLIRQ.

NOTE

This first register write causes the FMPLL to switch to an initial frequency which is less than the final one. Keeping the change of frequency to a lower initial value helps minimize the current surge to the external power supply caused by change of frequency. The last step changes the RFD to get the final frequency.

NOTE

Changing the MFD or PREDIV values causes the FMPLL to perform a search for the lock frequency that results in the system clock frequency changing rapidly across the complete frequency range. All MCU peripherals, including the external bus, are subjected to this frequency sweep. Operation of timers and serial communications during this search sequence produces unpredictable results.

The frequency modulation system is dependent upon several the accuracies of these factors:

- V_{DDSYN} and V_{SSSYN} voltages
- Crystal oscillator frequency
- Manufacturing variation

For example, if a 5% accurate supply voltage is used, then a 5% modulation depth error results. If the crystal oscillator frequency is skewed from 8 MHz, the resulting modulation frequency is proportionally

skewed. Finally, the error due to the manufacturing and environment variation alone can cause the frequency modulation depth error to be greater than 20%.

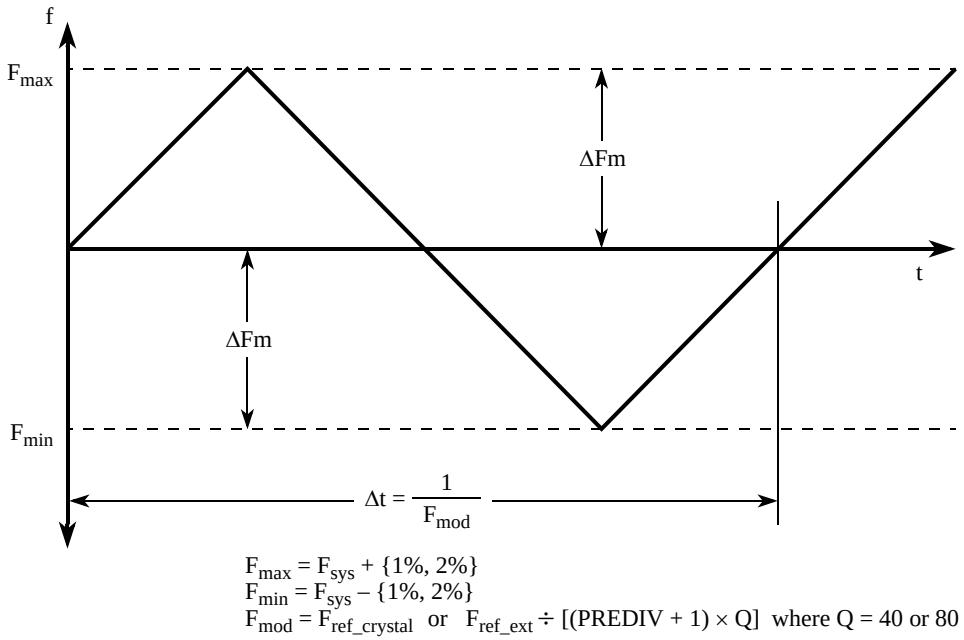


Figure 11-10. Frequency Modulation Waveform

11.4.3.3 FM Calibration Routine

Upon enabling frequency modulation, a new calibration routine is performed. This routine tunes a reference current into the modulation D/A so that the modulation depth (F_{max} and F_{min}) remains within specification.

Entering the FM calibration mode requires you to program SYNCR[EXP]. The EXP is the expected value of the difference between the reference and feedback counters used in the calibration of the FM equation:

$$EXP = \frac{((MFD + 4) \times M \times P)}{100}$$

For example, if 80 MHz is the desired final frequency and an 8 MHz crystal is used, the final values of MFD = 6 and RFD = 0 produces the desired 80 MHz. For a desired frequency modulation with a 1% depth, then EXP is calculated using P = 1, MFD = 6 and M = 480. Refer to Table 11-10 for a complete list of values to be used for the variable (M) based on MFD setting. To obtain a percent modulation (P) of 1%, the EXP field must be set at: $EXP = ((6 + 4) \times 480 \times 1) \div 100 = 48$

Rounding this value to the closest integer yields 48, which is entered into the EXP field for this example.

Table 11-10. Multiplied Factor Dividers with M Values

MFD	M
0–2	960
3–5	640

Table 11-10. Multiplied Factor Dividers with M Values (continued)

MFD	M
6–8	480
9–14	320
15–20	240
21–31	160

This routine corrects for process variations, but because temperature can change after calibration is performed, the variation caused by temperature drift remains. This frequency modulation calibration system is also voltage dependent, so if the supply changes after the sequence occurs, errors incurred are not corrected. The calibration system reuses the two counters in the lock detect circuit, and the reference and feedback counters. The reference counter remains clocked by the reference clock, but the feedback counter is clocked by the ICO clock.

When the calibration routine is initiated by writing to the DEPTH bits, the CALPASS status bit is immediately set and the CALDONE status bit is immediately cleared.

When calibration is induced, the ICO is given time to settle. Then both the feedback and reference counters start counting. Full ICO clock cycles are counted by the feedback counter during this time to give the initial center frequency count. When the reference counter has counted to the programmed number of reference count cycles, the input to the feedback counter is disabled and the result is placed in the COUNT0 register. The calibration system then enables modulation at programmed ΔFm. The ICO is given time to settle. Both counters are reset and restarted. The feedback counter begins to count full ICO clock cycles again to obtain the delta-frequency count. When the reference counter has counted to the new programmed number of reference count cycles, the feedback counter is stopped again.

The delta-frequency count minus the center frequency count (COUNT0) results in a delta count proportional to the reference current into the modulation D/A. That delta count is subtracted from the expected value given in the EXP field of the FMPLL_SYNCR resulting in an error count. The sign of this error count determines the direction taken by the calibration D/A to update the calibration current. After obtaining the error count for the present iteration, both counters are cleared. The stored count of COUNT0 is preserved while a new feedback count is obtained, and the process to determine the error count is repeated. The calibration system repeats this process eight times, once for each bit of the calibration D/A.

After the last decision is made, the CALDONE bit of the SYNSR is written to a one. If an error occurs during the calibration routine, then CALPASS is immediately written to a zero. If the routine completed successfully then CALPASS remains a one.

Figure 11-11 shows a block diagram of the calibration circuitry and its associated registers. Figure 11-12 shows a flow chart showing the steps taken by the calibration circuit.

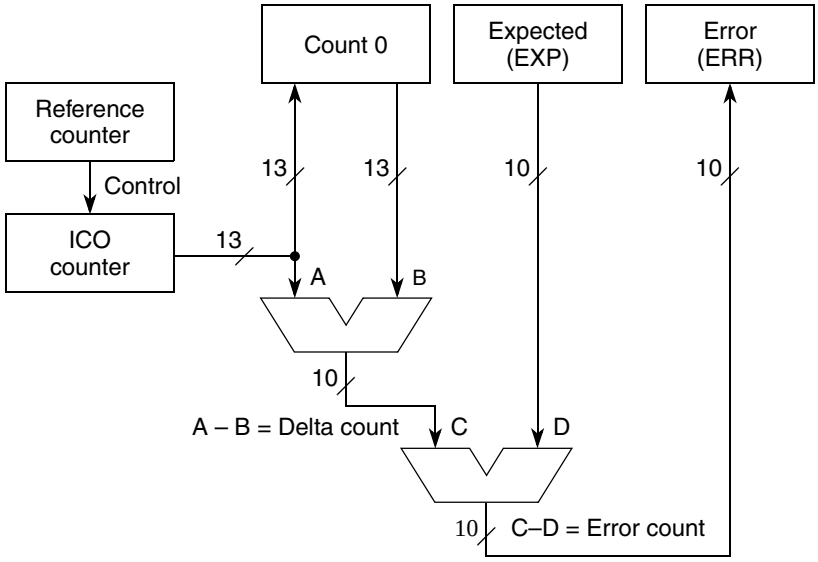


Figure 11-11. FM Auto-Calibration Data Flow

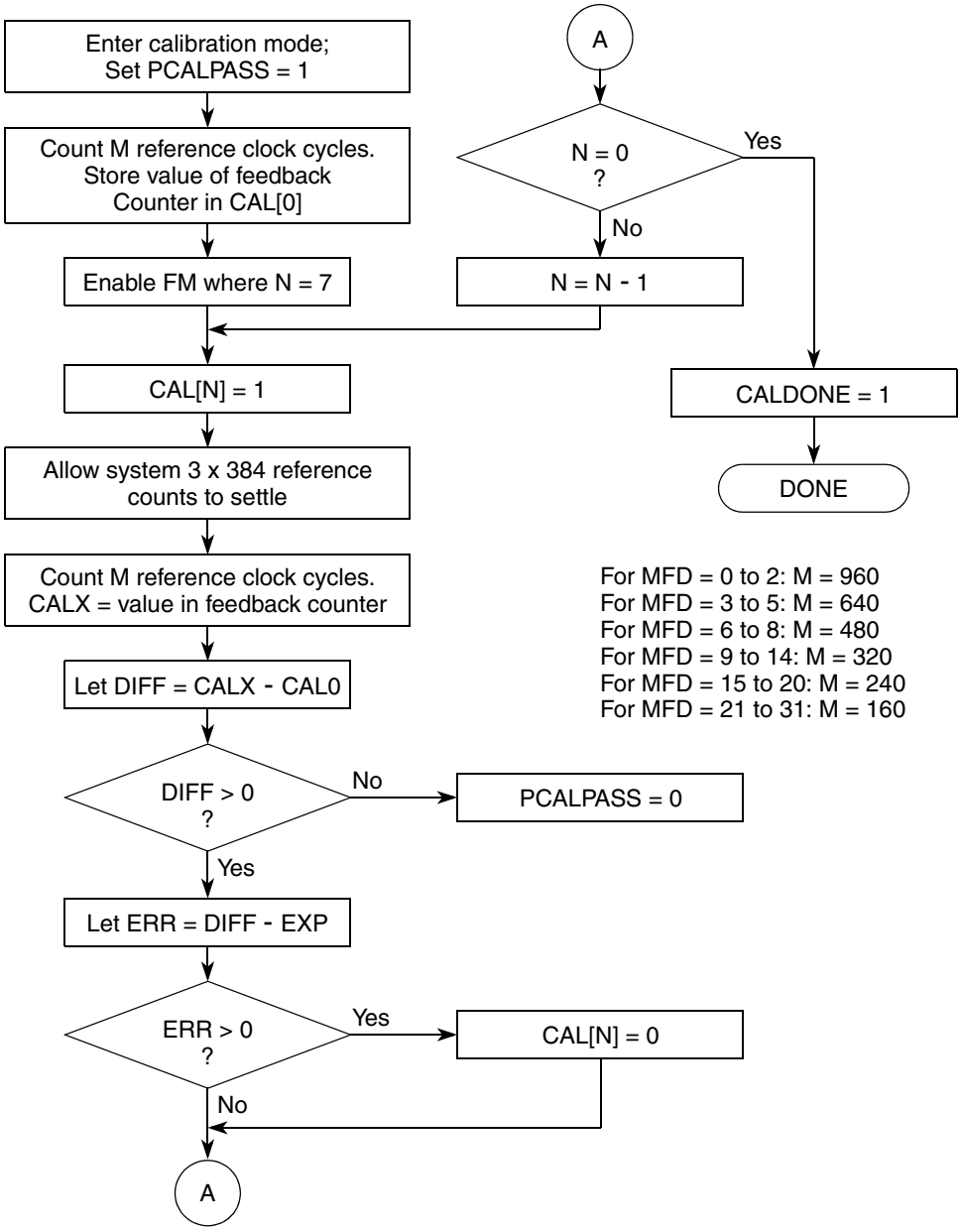


Figure 11-12. FM Auto-Calibration Flow Chart

Chapter 12
External Bus Interface (EBI)

12.1 Introduction

This chapter describes the external bus interface (EBI), which handles the transfer of information between the internal buses and the memories or peripherals in the external address space and enables an external master to access internal address space. For an overview of how the EBI used in the MPC5500 differs from the EBI used in MPC500 devices, see Section 12.5.5, "Summary of Differences from MPC5xx."

12.1.1 Block Diagram

Figure 12-1 is a block diagram of the EBI. The signals shown are external pins to the MCU.

NOTE

See the Signal Description table in the Signals chapter, as not all signals are implemented in all device packages. See the last two columns in the table for a list of available signals on the 416 package and the VertiCal assembly. The VertiCal assembly has ball connections for all the *available* signals on the device.

The following figure shows the MPC5566 EBI block diagram on the 416 package. The $\overline{BR}$, $\overline{BG}$, and $\overline{BB}$ signals are used for arbitration on the external bus:

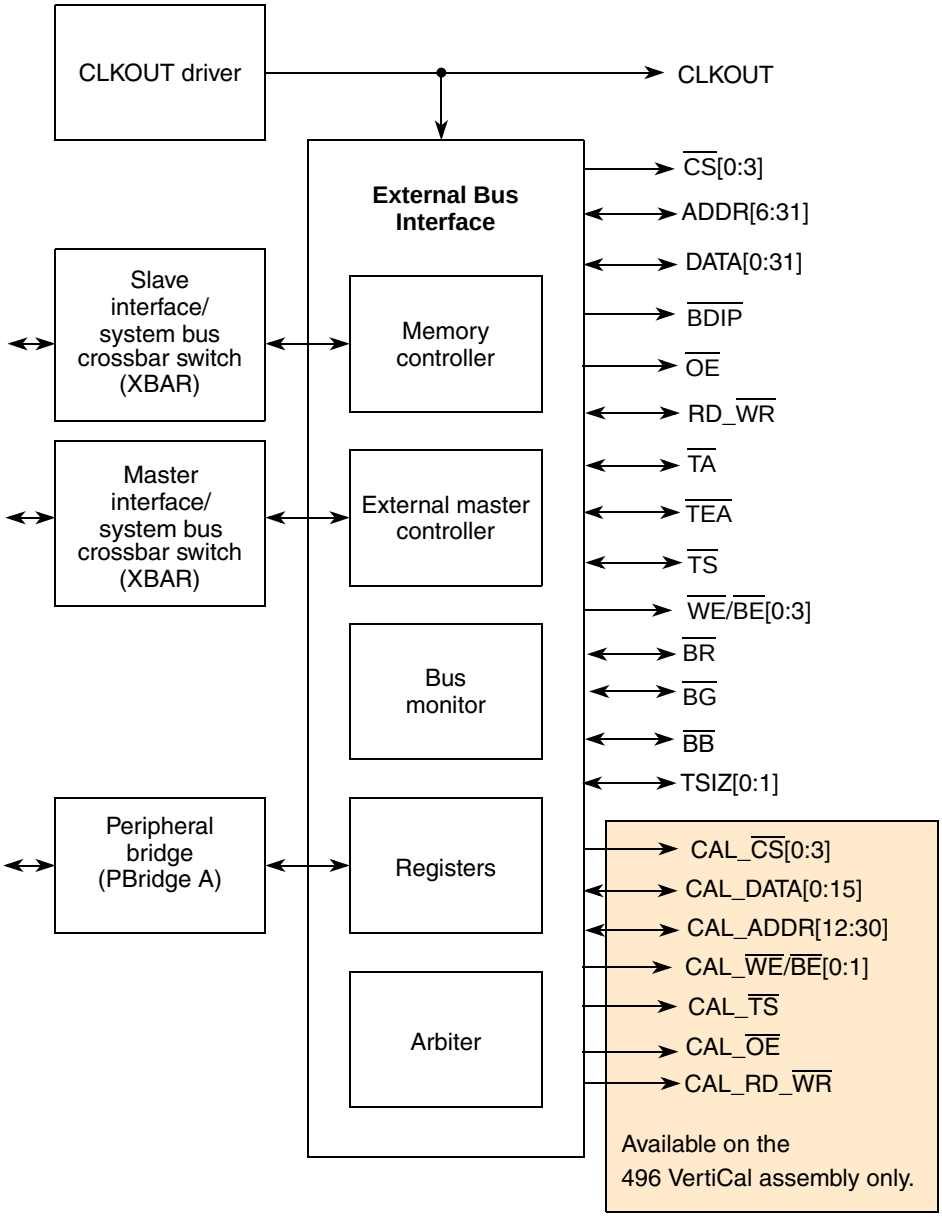


Figure 12-1. EBI Block Diagram

12.1.2 Overview

The EBI includes a memory controller that generates interface signals to support a variety of external memories. This includes single data rate (SDR) burst mode flash, external SRAM, and asynchronous memories. It supports up to four regions (via chip selects), each with its own programmed attributes.

12.1.3 Features

The device includes design for the following features:

- 1.8–3.3 V I/O
- Address bus is 32-bit with transfer size indication
- 32-bit internal address bus with transfer size indication; Table 12-1 shows the address bus packages supported.

Table 12-1. Address Bus Sizes in MPC5566

MPC5566 Packaging	416	
EBI Address Bus Size	24 bit [1]	20 bit [2]
Calibration Address Bus Size	19 or 21 bits [3]	

[1] 24 bits available: In the 416 package, three configurations can be used to attain a 24-bit size:
-- ADDR[8:11]_GPIO[4:7] can be added to ADDR[12:31],
-- $\overline{CS}$[0:3]_ADDR[8:11]_GPIO [0:3] can be configured by PCR to ADDR[8:11] and add the ADDR[12:31] signals, or
-- ADDR[30:31]_ADDR[6:7]_GPIO[26:27] can be configured to ADDR[6:7] and add the ADDR[8:29] signals. This space cannot be used for slave accesses.
You can use one configuration only of the ADDR[8:11] signals for address input.

[2] The default EBI size is 20 bits (ADDR[12:31]).

[3] The default calibration bus interface (CBI) is 19 bits using CAL_ADDR[12:30]. However, it can be configured to use CAL_ADDR[10:11] of the muxed signals CAL_CS[2:3]_CAL_ADDR[10:11] to increase the calibration bus size to 21 bits.

- 32-bit data bus available for external memory accesses and transactions involving an external master: Table 12-2 shows the data bus package supported.

Table 12-2. Data Bus Size in MPC5566

Bus Interface	416 BGA
EBI data bus size	32 bit
Calibration data bus size	16 bit

- Support for external master accesses to internal addresses.
- Memory controller with support for various memory types:
  - Synchronous burst SDR flash and SRAM
  - Asynchronous/legacy flash and SRAM
- Burst support (wrapped only)

- Bus monitor
  - User selectable
  - Programmable timeout period (with 8 external bus clock resolution)
- Port size configuration per chip select (16 or 32 bits)
- Port size for calibration chip select is 16 bits
- Configurable wait states (via chip selects)
- Four chip select ($\overline{CS}$[0:3]) signals
- Write/byte enable ($\overline{WE}$/$\overline{BE}$) signals depend on the package: 416 BGA: four signals ($\overline{WE}$/$\overline{BE}$[0:3])
- Support for dynamic calibration with up to four calibration chip selects (CAL_$\overline{CS}$[0:3])
- Configurable bus speed modes (½ or ¼ of the system clock frequency)
- Module disable modes for power savings
- Optional automatic CLKOUT gating to save power and reduce EMI
- Compatible with MPC5xx external bus
  Section 12.4.1.17, "Compatible with MPC5xx External Bus (with Some Limitations)."

12.1.4 Modes of Operation

The mode of the EBI is determined by the MDIS and EXTM bits in the EBI_MCR. See Section 12.3.1.3, "EBI Module Configuration Register (EBI_MCR)" for details. Configurable bus speed modes and debug mode are modes that the MCU can enter, in parallel to the EBI being configured in one of its module-specific modes.

12.1.4.1 Single Master Mode

In single master mode, the EBI responds to internal requests matching one of its regions, but ignores all externally-initiated bus requests. The MCU is the only master allowed to initiate transactions on the external bus in this mode; therefore, it acts as a parked master and does not have to arbitrate for the bus before starting each cycle. The $\overline{BR}$, $\overline{BG}$, and $\overline{BB}$ signals are not used by the EBI in this mode, and are available for use in an alternate function by another module of the MCU. Single master mode is entered when EXTM = 0 and MDIS = 0 in the EBI_MCR.

12.1.4.2 External Master Mode

When the MCU is in external master mode, the EBI responds to internal requests matching one of its regions, and also to external master accesses to internal address space. In this mode, the $\overline{BR}$, $\overline{BG}$, and $\overline{BB}$ signals are all used by the EBI to handle arbitration between the MCU and an external master. External master mode is entered when EXTM = 1 and MDIS = 0 in the EBI_MCR register.

The MPC5566 has arbitration pins ($\overline{BB}$, $\overline{BR}$, $\overline{BG}$), therefore dual-master operation (multiple masters initiating external bus cycles) is supported. A multi-MCU system with one master and one slave is supported. In a dual-controller system, if the EBI is configured to internal arbitration (EARB = 0 in EBI_MCR), it must be used as the system master. If configured to external arbitration (EARB = 1 in EBI_MCR), it must be the system slave.

NOTE

The internal bus grant input of the EBI is tied to a negated state. In a dual controller system in which the EBI is programmed to External Master Mode with external arbitration, if the CPU tries to access a memory region within the EBI space, no bus grant is received, and the operation times out.

External master mode operation is described in Section 12.4.2.10, "Bus Operation in External Master Mode."

12.1.4.3 Module Disable Mode

The module disable mode is used for MCU power management. The clock to the non-memory mapped logic in the EBI is stopped while in module disable mode. Requests (other than to memory-mapped logic) must not be made to the EBI while it is in module disable mode, even if the clocks have not yet been shut off. In this case, the behavior is undefined. Module disable mode is entered when MDIS = 1 in the EBI_MCR.

12.1.4.4 Configurable Bus Speed Modes

In configurable bus speed modes, the external CLKOUT frequency is reduced to ½ or ¼ compared to the internal system clock frequency. The EBI continues to operate according to the EBI mode selected, except that the EBI drives and samples signals at the scaled CLKOUT frequency rate rather than the internal system clock. This mode is selected by writing the external clock control register in the system integration module (SIU_ECCR). The configurable bus speed modes supports both ½ or ¼ speed modes, meaning that the external CLKOUT frequency is scaled (divided) by two or four compared with that of the internal system clock, which remains unchanged.

NOTE

In a multi-master system with the PLL in dual-controller mode, only ½ speed mode is supported.

12.1.4.5 16-Bit Data Bus Mode

The EBI has an internal 32-bit data bus, but for MCUs that have only 16 data bus signals pinned out, or for systems that use multiplexed signals (e.g. GPIO) on 16 of the 32 data pins, the EBI supports a 16-bit data bus mode. In this mode, DATA[0:15] are the only data signals used by the EBI. To enter 16-bit data bus mode, set the data bus mode field [DBM] in the EBI master control register (EBI_MCR[DBM]) to one. The reset value of DBM is 0.

For EBI-mastered accesses, the operation in 16-bit data bus mode (EBI_MCR[DBM] = 1, EBI_BR*n*[PS] = x) is similar to a chip select access to a 16-bit port in 32-bit data bus mode (EBI_MCR[DBM] = 0, EBI_BR*n*[PS] = 1), except for the case of an EBI-mastered non-chip select access of exactly 32-bit size.

External master accesses and EBI-mastered non-chip select accesses of exactly 32-bit size are supported using a two beat (16-bit) burst for both reads and writes. Except for chip-select ($\overline{CS}$[*n*]) data transmissions, all data transmissions that are not 32 bits are supported in standard non-burst fashion.

See Section 12.4.2.11, “Non-Chip-Select Burst in 16-bit Data Bus Mode.”

12.1.4.6 Debug Mode

When the MCU is in debug mode, the EBI mode is unaffected and retains control of the EBI.

12.2 External Signal Description

The EBI signal pinouts depend on the type of package. Table 12-3 alphabetically lists the external signals used by the EBI.

See Chapter 2, “Signal Description,” as not all signals are implemented in all device packages.

Table 12-3. MPC5566 Signal Properties

Signal Name	I/O Type	Function	Pull [1]	416 Package	496 [2] Assembly
ADDR[6:7] [3]	I/O	Address bus	Up	416	496
ADDR[8:11]	I/O	Address bus	Up	416	496
ADDR[12:31]	I/O	Address bus	Up	416	496
$\overline{\text{BDIP}}$	Output	Burst data in progress	Up	416	496
CAL_ADDR[10:11] [4]	Output	Calibration address bus (output)	Up	—	496
CAL_ADDR[12:30]	Output	Calibration address bus (output)	Up	—	496
CAL_$\overline{\text{CS}}$[0:3] [2]	Output	Calibration chip selects	Up	—	496
CAL_DATA[0:15]	I/O	Calibration data bus	Up	—	496
CAL_RD_$\overline{\text{WR}}$	I/O	Calibration read/write	Up	—	496
CAL_$\overline{\text{OE}}$	Output	Calibration output enable	Up	—	496
CAL_$\overline{\text{TS}}$	Output	Calibration transfer start	Up	—	496
CAL_$\overline{\text{WE}}$/$\overline{\text{BE}}$[0:3]	I/O	Calibration write/byte enables	Up	—	496
CLKOUT [5]	Output	Clockout	Enabled	416	496
$\overline{\text{CS}}$[0:3]	Output	Chip selects	Up	416	496
DATA[0:31]	I/O	Data bus	Up	416	496
$\overline{\text{OE}}$	Output	Output enable	Up	416	496
RD_$\overline{\text{WR}}$	I/O	Read/write	Up	416	496
$\overline{\text{TA}}$	I/O	Transfer acknowledge	Up	416	496
$\overline{\text{TEA}}$	I/O	Transfer error acknowledge	Up	416	496
$\overline{\text{TS}}$	I/O	Transfer start	Up	416	496
$\overline{\text{WE}}$/$\overline{\text{BE}}$[0:3]	Output	Write/byte enables	Up	416	496
TSIZ[0:1]	I/O	Transfer size	Up	416	496
$\overline{\text{BB}}$	I/O	Bus busy	Up	416	496

Table 12-3. MPC5566 Signal Properties (continued)

Signal Name	I/O Type	Function	Pull [1]	416 Package	496 [2] Assembly
$\overline{BG}$	I/O	Bus grant	Up	416	496
$\overline{BR}$	I/O	Bus request	Up	416	496

1 This column shows which signals require a weak pullup or pulldown. The EBI module does not configure the pullup or pulldown mechanisms; use the pad configuration registers (PCRs) in the System Integration Unit (SIU_PCRs) to configure the signal direction and strength requirements.

2 All EBI and calibration signals designed for this device are available on the 496 VertiCal assembly.

3 ADDR[6:7] are separate signals from EBI block, but are muxed onto ADDR[30:31] pins on MCU.

4 CAL_ADDR[10:11] are separate signals from the EBI block, and are muxed onto CAL_$\overline{CS}$[2:3] pins on MCU.

5 The CLKOUT signal is driven by the FMPLL Module.

12.2.1 Detailed Signal Descriptions

See Chapter 2, "Signal Description," as not all signals are implemented in all device packages.

12.2.1.1 Address Lines: ADDR[8:31] or ADDR[6:29]

The ADDR[8:31] or ADDR[6:29] signals specify the physical address of the bus transaction. See Table 12-1 for details on address bus configuration. The 24 address lines are bits 8 through 31 of the EBI 32-bit internal address bus. Bits 0 through 7 are internally driven by the EBI for externally initiated accesses depending on the internal slave accessed.

See Section 12.4.2.10.1, "Address Decoding for External Master Accesses," for more details.

ADDR[8:31] is driven by the EBI or an external master depending on the module that controls the external bus. During a calibration bus access, ADDR[*n*] reflects the same values as the CAL_ADDR[*n*] signals.

12.2.1.2 Data Lines: DATA[0:31]

In the 416 BGA package and 496 assembly, DATA[0:31] signals transfer the data for the current transaction.

DATA[0:31] is driven by the EBI when it owns the external bus and it initiates a write transaction to an external device. The EBI also drives DATA[0:31] when an external master owns the external bus and initiates a read transaction to an internal module.

DATA[0:31] is driven by an external device during a read transaction from the EBI. An external master drives DATA[0:31] when it owns the bus and initiates a write transaction to an internal module or shared external memory.

For 8-bit and 16-bit transactions, the unused byte lanes do not supply valid data.

During a calibration bus access, the DATA bus is not driven by the EBI.

12.2.1.3 Burst Data in Progress ($\overline{\text{BDIP}}$)

$\overline{\text{BDIP}}$ is asserted by a master requesting the next data beat to follow the current data beat.

$\overline{\text{BDIP}}$ is driven by the EBI or an external master depending on the module in control of the external bus. This signal is driven by the EBI on all EBI-mastered external burst cycles, but is only sampled by burst mode memories that have a burst pin. See Section 12.4.2.5, "Burst Transfer."

12.2.1.4 Clockout (CLKOUT)

CLKOUT is a general-purpose clock output signal to connect to the clock input of SDR external memories and in some cases to the input clock of another MCU in multi-master configurations.

12.2.1.5 Chip Selects 0 through 3 ($\overline{\text{CS}}$[0:3])

$\overline{\text{CS}}$[*n*] is asserted by the master to indicate that this transaction is targeted for a particular memory bank.

The chip selects are driven by the EBI or an external master depending on who owns the external bus. $\overline{\text{CS}}$ is driven in the same clock as the assertion of $\overline{\text{TS}}$ and valid address, and is kept valid until the cycle is terminated. See Section 12.4.1.5, "Memory Controller with Support for Various Memory Types" for details on chip select operation.

$\overline{\text{CS}}$[0:3] are implemented in the 496 VertiCal assembly and the 416 package.

During a calibration bus access, the $\overline{\text{CS}}$ signals are held negated.

12.2.1.6 Output Enable ($\overline{\text{OE}}$)

$\overline{\text{OE}}$ is used to indicate when an external memory is permitted to drive back read data. External memories must have their data output buffers off when $\overline{\text{OE}}$ is negated. $\overline{\text{OE}}$ is only asserted for chip select accesses.

$\overline{\text{OE}}$ is driven by the EBI or an external master depending on which module owns the external bus. For read cycles, $\overline{\text{OE}}$ is asserted one clock after $\overline{\text{TS}}$ assertion and held until the termination of the transfer. For write cycles, $\overline{\text{OE}}$ is negated throughout the cycle.

During a calibration bus access, $\overline{\text{OE}}$ is held negated.

12.2.1.7 Read/Write (RD_$\overline{\text{WR}}$)

RD_$\overline{\text{WR}}$ indicates whether the current transaction is a read access or a write access.

RD_$\overline{\text{WR}}$ is driven by the EBI or an external master depending on which module owns the external bus. RD_$\overline{\text{WR}}$ is driven in the same clock as the assertion of $\overline{\text{TS}}$ and valid address, and is kept valid until the cycle is terminated.

During a calibration bus access, RD_$\overline{\text{WR}}$ reflects the same value as the CAL_RD_$\overline{\text{WR}}$ signal.

12.2.1.8 Transfer Acknowledge ($\overline{TA}$)

$\overline{TA}$ is asserted to indicate that the slave device has received the data (and completed the access) for a write cycle, or returned data for a read cycle. If the transaction is a burst read, $\overline{TA}$ is asserted for each one of the transaction beats. For write transactions, $\overline{TA}$ is only asserted once at access completion, even if more than one write data beat is transferred.

$\overline{TA}$ is driven by the EBI when the access is controlled by the chip selects or when an external master initiates the transaction to an internal module. Otherwise, $\overline{TA}$ is driven by the slave device to which the current transaction was addressed.

During a calibration bus access, $\overline{TA}$ is held negated.

See Section 12.4.2.9, “Termination Signals Protocol” for more details.

12.2.1.9 Transfer Error Acknowledge ($\overline{TEA}$)

In the 416 BGA package and 496 assembly, $\overline{TEA}$ is asserted by either the EBI or an external device to indicate that an error condition has occurred during the bus cycle. $\overline{TEA}$ assertion terminates the cycle immediately, overriding the value of the $\overline{TA}$ signal.

$\overline{TEA}$ is asserted by the EBI when the internal bus monitor detected a timeout error, or when an external master initiated a transaction to an internal module and an internal error was detected.

The VertiCal assembly supports the $\overline{TEA}$ signal.

During a calibration bus access, $\overline{TEA}$ is held negated.

See Section 12.4.2.9, “Termination Signals Protocol” for more details.

12.2.1.10 Transfer Start ($\overline{TS}$)

$\overline{TS}$ is asserted by the current bus owner to indicate the start of a transaction on the external bus.

$\overline{TS}$ is driven by the EBI or an external master depending on the module that controls the external bus. $\overline{TS}$ is only asserted for the first clock cycle of the transaction, and is negated in the successive clock cycles until the end of the transaction.

During a calibration bus access, $\overline{TS}$ is held negated.

12.2.1.11 Write/Byte Enables ($\overline{WE}$/$\overline{BE}$)

Write enables are used to enable program operations to a particular memory. These signals can also be used as byte enables for read and write operation by setting the WEBS bit in the appropriate base register. The $\overline{WE}$/$\overline{BE}$ signals are only asserted for chip select accesses.

The $\overline{WE}$/$\overline{BE}$ signals are driven by the EBI or an external master depending on the module that controls the external bus.

The VertiCal assembly and the 416 BGA package use $\overline{WE}$/$\overline{BE}$[0:3].

During a calibration bus access, the $\overline{WE}$/$\overline{BE}$ signals are held negated.

See Section 12.4.1.13, "Four Write/Byte Enable (WE/BE) Signals — 416 BGA Package and VertiCal Assembly" for more details on the $\overline{WE}$/$\overline{BE}$ functionality.

12.2.1.12 Bus Busy ($\overline{BB}$)

$\overline{BB}$ is asserted to indicate that the current bus master is using the bus. The $\overline{BB}$ signal is only used by the EBI when the EBI is in external master mode. In single master mode, the $\overline{BB}$ signal is never asserted or sampled by the EBI.

When configured for internal arbitration, the EBI asserts $\overline{BB}$ to indicate that it is currently using the bus. An external master must not begin a transfer until this signal is negated for two cycles. The EBI does not negate this signal until its transfer is complete. When not driving $\overline{BB}$, the EBI samples this signal to get an indication of when the external master is no longer using the bus ($\overline{BB}$ negated for two cycles).

When configured for external arbitration, the EBI asserts this signal when it is ready to start the transaction after the external arbiter has granted ownership of the bus to the MCU. When not driving $\overline{BB}$, the EBI samples this signal to properly qualify the $\overline{BG}$ line when an external bus transaction is to be executed by the MCU.

12.2.1.13 Bus Grant ($\overline{BG}$)

$\overline{BG}$ is asserted to grant ownership of the external bus to the requesting master. The $\overline{BG}$ signal is only used by the EBI when the EBI is in external master mode. In single master mode, the $\overline{BG}$ signal is never asserted or sampled by the EBI.

When configured for internal arbitration, $\overline{BG}$ is an output only signal. The EBI asserts $\overline{BG}$ to when an external master can take control of the bus. The master requesting the bus must qualify the $\overline{BG}$ signal to ensure it controls the bus before beginning a bus transaction. A qualified bus grant includes the bus busy time ($\overline{BG}$ = ~$\overline{BB}$ and $\overline{BG}$). The EBI negates $\overline{BG}$ following the negation of $\overline{BR}$ if it has an internal request for the external bus pending. Otherwise, $\overline{BG}$ remains asserted to park the bus for the external master. The parked external master can then assert $\overline{BB}$ to run subsequent transactions without the normal requirement to assert $\overline{BR}$.

When configured for external arbitration, $\overline{BG}$ is an input only signal. The EBI must sample and qualify ($\overline{BG}$ = ~$\overline{BB}$ and $\overline{BG}$) the bus grant when an external bus transaction is ready for execution by the MCU.

12.2.1.14 Bus Request ($\overline{BR}$)

$\overline{BR}$ is asserted to request ownership of the external bus. The $\overline{BR}$ signal is only used by the EBI when the EBI is in external master mode. In single master mode, the $\overline{BR}$ signal is never asserted or sampled by the EBI.

When configured for internal arbitration, $\overline{BR}$ is input only and is asserted by an external master when it is requesting the bus.

When configured for external arbitration, $\overline{BR}$ is output only and is asserted by the EBI when it is requesting the bus. The EBI negates $\overline{BR}$ as soon as it is granted the bus and the bus is not busy, provided it has no other internal requests pending. If more requests are pending, the EBI keeps $\overline{BR}$ asserted as long as needed.

12.2.1.15 Transfer Size 0 through 1 (TSIZ[0:1])

TSIZ[0:1] indicates the size of the requested data transfer. TSIZ[0:1] is driven by the EBI or an external master depending on which component controls the external bus. The TSIZ[0:1] signals can be used with ADDR[30:31] to determine which byte lanes of the data bus are involved in the transfer. For non-burst transfers, the TSIZ[0:1] signals specify the number of bytes starting from the byte location addressed by ADDR[30:31]. In burst transfers, the value of TSIZ[0:1] is always 00.

Table 12-4. TSIZ[0:1] Encoding

Burst Cycle	TSIZ[0:1]	Transfer Size
N	01	8-bit
N	10	16-bit
N	11	Invalid value
N	00	32-bit
Y	00	Burst

If the SIZEN bit in the EBI_MCR is 1, then TSIZ[0:1] is ignored by the EBI as an input for external master transactions and the size is instead determined by the SIZE field in the EBI_MCR. The SIZEN bit has no effect on the EBI when it is mastering a transaction on the external bus. TSIZ[0:1] is still driven by the EBI and is used by the external master depending on the SIZEN setting for the external master's EBI. See Section 12.3.1.3, "EBI Module Configuration Register (EBI_MCR)."

12.2.1.16 Calibration Chip Selects (CAL_$\overline{\text{CS}}$[0:3])

CAL_$\overline{\text{CS}}$[*n*] is asserted by the master to indicate that this transaction is targeted for a particular memory bank on the calibration external bus.

The calibration chip selects are driven only by the EBI. External master accesses on the calibration bus are not supported. In all other aspects, the calibration chip selects behave exactly as the primary chip selects. See Section 12.4.1.5, "Memory Controller with Support for Various Memory Types" for details on chip select operation.

12.2.1.17 Calibration Signals

The calibration signal functions are explained in Chapter 2, "Signal Description."

DATA is not driven by the EBI during a calibration bus access. During a calibration bus access, the non-calibration bus signals (other than DATA) are held in a negated state, with the exception of RD_$\overline{\text{WR}}$ and ADDR, which reflect the same values shown on the calibration version of those signals. Because the $\overline{\text{TS}}$ and $\overline{\text{CS}}$ signals are held negated on the non-calibration bus during calibration accesses, no transfer occurs on the EBI.

During an EBI bus access, the calibration bus signals (other than CAL_DATA) are held in a negated state. CAL_DATA is not driven during non-calibration accesses.

12.2.2 Signal Function and Direction by Mode

The EBI operating mode is configured using two fields in the EBI Master Control register (EBI_MCR): EXTM and MDIS. Their settings determine which EBI signals are valid and the I/O direction. When the a signal is configured for non-EBI function in the EBI_MCR, the EBI always negates the signal if the EBI controls the corresponding pad (determined by SIU configuration). Table 12-5 lists the function and direction of the external signals in each of the EBI modes of operation. The clock signals are not included because they are output only (from the FMPLL module) and are not affected by EBI modes. See Section 12.3.1.3, "EBI Module Configuration Register (EBI_MCR)" for details on the EXTM and MDIS bits.

Table 12-5. Signal Function According to EBI Mode Settings

Signal Function	EBI Modes		
	Module Disable Mode EXTM = *n*, MDIS = 1	**Single Master Mode I/O Direction EXTM = 0, MDIS = 0**	**External Master Mode I/O Direction EXTM = 1, MDIS = 0**
ADDR[6:11] [1]	non-EBI function	Address bus (output)	Address bus (I/O) [2]
ADDR[12:30]	non-EBI function	Address bus (output)	Address bus (I/O) [2]
$\overline{\text{BDIP}}$	non-EBI function	Burst data in progress (output) [3]	
$\overline{\text{CS}}$[0:3] [1]	non-EBI function	Chip selects (output) [3]	
DATA[0:31] [4]	non-EBI function	Data bus (I/O)	
$\overline{\text{OE}}$	non-EBI function	Output enable (output)	
RD_$\overline{\text{WR}}$	non-EBI function	Read/write (output)	Read/write (I/O)
$\overline{\text{TA}}$	non-EBI function	Transfer acknowledge (I/O)	
$\overline{\text{TEA}}$	non-EBI function	Transfer Error Acknowledge (I/O)	
$\overline{\text{TS}}$	non-EBI function	Transfer start (output)	Transfer start (I/O)
$\overline{\text{WE}}$/$\overline{\text{BE}}$[0:3] [4]	non-EBI function	Write/byte enables (output)[3]	
CAL_$\overline{\text{CS}}$[0:3] [5]	non-EBI function	Chip selects (output) for the 416 package	
CAL_ADDR[12:30] [6,5]	non-EBI function	Calibrate the address bus (output)	
CAL_DATA[0:15] [6,5]	non-EBI function	Calibrate the data bus (I/O)	
CAL_$\overline{\text{OE}}$ [6,5]	non-EBI function	Calibrate the bus to enable output	
CAL_$\overline{\text{TS}}$ [6,5]	non-EBI function	Calibrate the transfer start (output)	
CAL_$\overline{\text{WE}}$/$\overline{\text{BE}}$[0:1] [5]	non-EBI function	Calibrate the write/byte enables (output)[3]	
$\overline{\text{BB}}$	non-EBI function	Non-EBI function	Bus Busy (I/O)
$\overline{\text{BG}}$	non-EBI function	Non-EBI function	Bus Grant (I/O)
$\overline{\text{BR}}$	non-EBI function	Non-EBI function	Bus Request (I/O)
TSIZ[0:1]	non-EBI function	Transfer Size (Output)	Transfer Size (I/O)

1 These signals are muxed with the chip select ($\overline{CS}$) signals on this device. Use the pad configuration registers (PCR) in the system integration module (SIU) to configure the balls to use the address signals *or* chip select signals–not both.

2 All I/O signals are three-stated by the EBI when not actively involved in a transfer.

3 Although external master accesses can drive these pins, the EBI three-states the pins and does not sample them for input.

4 This device is designed to support a 32-bit EBI data bus (DATA[0:31]) and four write/byte enable signals ($\overline{WE}$/$\overline{BE}$[0:3]) using the VertiCal assembly.

5 The calibration signals for this device are available on the VertiCal assembly only.

NOTE

The open drain mode of the pads configuration module is not used for any EBI signals. For a description of how signals are driven by multiple devices in external master mode, see Section 12.4.2.10, "Bus Operation in External Master Mode."

12.3 Memory Map and Register Definition

Table 12-6 is a memory map of the EBI registers.

Table 12-6. EBI Memory Map

Address	Register Name	Register Description	Bits
Base (0xC3F8_4000)	EBI_MCR	EBI module configuration register	32
Base + 0x0004	—	Reserved	—
Base + 0x0008	EBI_TESR	EBI transfer error status register	32
Base + 0x000C	EBI_BMCR	EBI bus monitor control register	32
Base + 0x0010	EBI_BR0	EBI base register bank 0	32
Base + 0x0014	EBI_OR0	EBI option register bank 0	32
Base + 0x0018	EBI_BR1	EBI base register bank 1	32
Base + 0x001C	EBI_OR1	EBI option register bank 1	32
Base + 0x0020	EBI_BR2	EBI base register bank 2	32
Base + 0x0024	EBI_OR2	EBI option register bank 2	32
Base + 0x0028	EBI_BR3	EBI base register bank 3	32
Base + 0x002C	EBI_OR3	EBI option register bank 3	32
Base + 0x0058	EBI_CAL_BR3	EBI calibration base register bank 3	32
Base + 0x005C	EBI_CAL_OR3	EBI calibration option register bank 3	32

12.3.1 Register Descriptions

12.3.1.1 Writing EBI Registers While a Transaction is in Progress

Other than the exceptions below, EBI registers must *not* be written while a transaction to the EBI (from internal or external master) is in progress (or within 2 CLKOUT cycles after a transaction has just completed, to allow internal state machines to go IDLE). In such cases, the behavior is undefined.

Exceptions that can be written while an EBI transaction is in progress are the following:

- All bits in EBI_TESR
- SIZE, SIZEN fields in EBI_MCR

See Section 12.5.1, "Booting from External Memory," for additional information.

12.3.1.2 Separate Input Clock for Registers

The EBI registers are accessed with a clock signal separate from the clock used by the rest of the EBI. In module disable mode, the clock used by the non-register portion of the EBI is disabled to reduce power consumption. The dedicated clock signal allows access to the registers even while the EBI module is in disable mode. Flag bits in the EBI transfer error status register (EBI_TESR), however, are set and cleared with the clock used by the non-register portion of the EBI. Consequently, in module disable mode, the EBI_TESR does not have a clock signal and is therefore not writable.

12.3.1.3 EBI Module Configuration Register (EBI_MCR)

The EBI_MCR contains bits that configure various attributes associated with EBI operation.

Base (0xC3F8_4000) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	SIZEN	SIZE		0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	ACGE	EXTM	EARB	EARP		0	0	0	0	MDIS	0	0	0	0	0	DBM
W																
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Figure 12-2. EBI Module Configuration Register (EBI_MCR)

The following table describes the fields in the EBI module configuration register:

Table 12-7. EBI_MCR Field Descriptions

Field	Description
0–4	Reserved.
5 SIZEN	SIZE enable. The SIZEN bit enables the control of transfer size by the SIZE field (as opposed to external TSIZ pins) for external master transactions to internal addresses. 0 Transfer size controlled by TSIZ[0:1] pins 1 Transfer size controlled by SIZE field
6–7 SIZE	Transfer size. The SIZE field determines the transfer size of external master transactions to internal address space when SIZEN = 1. This field is ignored when SIZEN = 0. SIZE encoding: 00 32-bit 01 Byte 10 16-bit 11 Invalid value
8–15	Reserved.
16 ACGE	Automatic CLKOUT gating enable. Enables the EBI feature of turning off CLKOUT (holding it high) during idle periods in-between external bus accesses. 0 Automatic CLKOUT gating is disabled 1 Automatic CLKOUT gating is enabled
17 EXTM	External master mode. The EBI module must be enabled (MDIS = 0) to configure the external master mode. When the EBI module is disabled (MDIS = 1), the value of the EXTM bit is ignored and read as 0. External master mode (EXTM = 1) allows the external master device to access any internal memory area that is mapped, as long as the internal e200z6 core is fully operational. Single master mode (EXTM = 0) only allows internal masters can access internal memory. This bit also determines the functionality of the $\overline{BR}$, $\overline{BG}$, and $\overline{BB}$ signals. **Note:** The SIU PCR registers must configure $\overline{BR}$, $\overline{BG}$, and $\overline{BB}$ for EBI function (as opposed to default GPIO) *prior* to EXTM being set to 1, or operations can result. 0 Single master mode (external master mode disabled) 1 External master mode
18 EARB	External arbitration. See Section 12.4.2.8, “Arbitration” for details on internal and external arbitration. When EXTM = 0, the EARB bit is not used, and is treated as 0. 0 Internal arbitration 1 External arbitration
19–20 EARP [0:1]	External arbitration request priority. Defines the priority of an external master’s arbitration request (0–2), with 2 as the highest priority level (EARP = 3 is reserved). This field is valid only when EARB = 0 (internal arbitration). The internal masters of the MCU have a fixed priority of 1. By default, internal and external masters have equal priority. See Section 12.4.2.8.2, “Internal Bus Arbiter,” for the internal and external priority detailed description. 00 MCU has priority 01 Equal priority, round robin used 10 External master has priority 11 Invalid value
21–24	Reserved.

Table 12-7. EBI_MCR Field Descriptions (continued)

Field	Description
25 MDIS	Module disable mode. Allows the clock to be stopped to the non-memory mapped logic in the EBI, effectively putting the EBI in a software controlled power-saving state. See Section 12.1.4.3, "Module Disable Mode," for more information. No external bus accesses can be performed when the EBI is in module disable mode (MDIS = 1). 0 Module disable mode inactive 1 Module disable mode active
26–30	Reserved.
31 DBM	Data bus mode. Controls whether the EBI is in 32-bit or 16-bit data bus mode. 0 32-bit data bus mode 1 16-bit data bus mode

12.3.1.4 EBI Transfer Error Status Register (EBI_TESR)

The EBI_TESR contains a bit for each type of transfer error on the external bus. A bit set to logic 1 indicates what type of transfer error occurred since the last time the bits were cleared. Each bit can be cleared by reset or by writing a 1 to it. Writing a 0 has no effect.

This register is not writable in module disable mode due to the use of power saving clock modes.

Base + 0x0008 Access: R/W1c

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TEAF	BMTF
W															w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 12-3. EBI Transfer Error Status Register (EBI_TESR)

The following table describes the fields in the EBI transfer error status register:

Table 12-8. EBI_TESR Field Descriptions

Field	Description
0–29	Reserved.
30 TEAF	Transfer error acknowledge flag. Set if the cycle was terminated by an externally generated $\overline{\text{TEA}}$ signal. 0 No error 1 External $\overline{\text{TEA}}$ occurred This bit can be cleared by writing a 1 to it.
31 BMTF	Bus monitor timeout flag. Set if the cycle was terminated by a bus monitor timeout. 0 No error 1 Bus monitor timeout occurred This bit can be cleared by writing a 1 to it.

12.3.1.5 EBI Bus Monitor Control Register (EBI_BMCR)

The EBI_BMCR controls the timeout period of the bus monitor and whether it is enabled or disabled.

Base + 0x000C — Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	BMT								BME	0	0	0	0	0	0	0
W																
Reset	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0

Figure 12-4. EBI Bus Monitor Control Register (EBI_BMCR)

The following table describes the fields in the EBI bus monitor control register:

Table 12-9. EBI_BMCR Field Descriptions

Field	Description
0–15	Reserved.
16–23 BMT[0:7]	Bus monitor timing. Defines the timeout period, in 8 external bus clock resolution, for the bus monitor. See Section 12.4.1.7, “Bus Monitor,” for more details on bus monitor operation. $\text{Timeout period} = \frac{2 + (8 \times \text{BMT})}{\text{External bus clock frequency}}$

Table 12-9. EBI_BMCR Field Descriptions (continued)

Field	Description
24 BME	Bus monitor enable. Controls whether the bus monitor is enabled for internal to external bus cycles. Regardless of the BME value, the bus monitor is always disabled for chip select accesses, since these always use internal $\overline{TA}$ and thus have no danger of hanging the system. 0 Disable bus monitor 1 Enable bus monitor (for non-chip select accesses only)
25–31	Reserved.

12.3.1.6 EBI Base Registers 0–3 (EBI_BR*n*) and EBI Calibration Base Registers 0–3 (EBI_CAL_BR*n*)

The EBI_BR*n* are used to define the base address and other attributes for the corresponding chip select. The EBI_CAL_BR*n* are used to define the base address and other attributes for the corresponding calibration chip select.

Address: Base + 0x0010 (EBI_BR0) Access: R/W
Base + 0x0018 (EBI_BR1)
Base + 0x0020 (EBI_BR2)
Base + 0x0028 (EBI_BR3)
Base + 0x0040 (EBI_CAL_BR0)
Base + 0x0048 (EBI_CAL_BR1)
Base + 0x0050 (EBI_CAL_BR2)
Base + 0x0058 (EBI_CAL_BR3)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	1	BA												
W																
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	BA	0	0	0	PS	0	0	0	0	BL	WEBS	TBDIP	0	0	BI	V
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Figure 12-5. EBI Base Registers 0–3 (EBI_BR*n*) and EBI Calibration Base Registers 0–3 (EBI_CAL_BR*n*)

The following table describes the fields in the EBI calibration base register:

Table 12-10. EBI_BR*n* and EBI_CAL_BR*n* Field Descriptions

Field	Description
0–16 BA [0:16]	Base address. Compared to the corresponding unmasked address signals among ADDR[0:16] of the internal address bus to determine if a memory bank controlled by the memory controller is being accessed by an internal bus master. **Note:** The upper three bits of the base address (BA) field, EBI_BR*n*[0:2], and EBI_CAL_BR*n*[0:2], are tied to a fixed value of 001. These bits reset to their fixed value.
17–19	Reserved.
20 PS	Port size. Determines the data bus width of transactions to this chip select bank.[1] 0 32-bit port 1 16-bit port **Note:** The calibration port size must be 16-bits wide.
21–24	Reserved.
25 BL	Burst length. Determines the amount of data transferred in a burst for this chip select, measured in 32-bit words. The number of beats in a burst is automatically determined by the EBI to be 4, 8, or 16 according to the port size so that the burst fetches the number of words chosen by BL. 0 8-word burst length 1 4-word burst length
26 WEBS	Write enable/byte select. Controls the functionality of the $\overline{WE}$/$\overline{BE}$ signals. 0 The $\overline{WE}$/$\overline{BE}$ signals function as write enable ($\overline{WE}$). 1 The $\overline{WE}$/$\overline{BE}$ signals function as byte enable ($\overline{BE}$). **Note:** The 416-pin package implements $\overline{WE}$/$\overline{BE}$[0:3] **Note:**
27 TBDIP	Toggle burst data in progress. Determines how long the $\overline{BDIP}$ signal is asserted for each data beat in a burst cycle. See Section 12.4.2.5.1, “TBDIP Effect on Burst Transfer,” for details. 0 Assert $\overline{BDIP}$ throughout the burst cycle, regardless of wait state configuration. 1 Only assert $\overline{BDIP}$ (BSCY + 1) external bus cycles before expecting subsequent burst data beats.
28–29	Reserved.
30 BI	Burst inhibit. Determines whether or not burst read accesses are allowed for this chip select bank. 0 Enable burst accesses for this bank. 1 Disable burst accesses for this bank. This is the default value out of reset.
31 V	Valid bit. Indicates that the contents of this base register and option register pair are valid. The $\overline{CS}$ signal does not assert unless its V-bit is set. 0 This bank is not valid. 1 This bank is valid.

[1] In the case where EBI_MCR[DBM] is set for 16-bit data bus mode, the PS bit value is forced to one (16-bit port) and the actual value is ignored.

12.3.1.7 EBI Option Registers 0–3 (EBI_OR*n*) and EBI Calibration Option Registers 0–3 (EBI_CAL_OR*n*)

The EBI_OR*n* registers are used to define the address mask and other attributes for the corresponding chip select. The EBI_CAL_OR*n* registers are used to define the address mask and other attributes for the corresponding calibration chip select.

Address: Base + 0x0014 (EBI_OR0) Access: R/W
Base + 0x001C (EBI_OR1)
Base + 0x0024 (EBI_OR2)
Base + 0x002C (EBI_OR3)
Base + 0x0044 (EBI_CAL_OR0)
Base + 0x004C (EBI_CAL_OR1)
Base + 0x0054 (EBI_CAL_OR2)
Base + 0x005C (EBI_CAL_OR3)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	1	1	1	AM												
W																
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	AM	0	0	0	0	0	0	0	SCY				0	BSCY		0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 12-6. EBI Option Registers 0–3 (EBI_OR*n*) and EBI Calibration Option Registers

The following table describes the fields in the EBI calibration option registers:

Table 12-11. EBI_OR*n* and EBI_CAL_OR*n* Field Descriptions

Field	Description
0–16 AM [0:16]	Address mask. Allows masking of any corresponding bits in the associated base register. Masking the address independently allows external devices of different size address ranges to be used. Any clear bit masks the corresponding address bit. Any set bit causes the corresponding address bit to be used in comparison with the address pins. Address mask bits can be set or cleared in any order in the field, allowing a resource to reside in more than one area of the address map. This field can be read or written at any time. **Note:** The upper 3 bits of the address mask (AM) field, EBI_ORx[0:2], and EBI_CAL_OR*n*[0:2], are tied to a fixed value of 111. These bits reset to their fixed value.
17–23	Reserved.
24–27 SCY [0:3]	Cycle length in clocks. Represents the number of wait states (external bus cycles) inserted after the address phase in the single cycle case, or in the first beat of a burst, when the memory controller handles the external memory access. Values range from 0 to 15. This is the main parameter for determining the length of the cycle. • The total cycle length for the first beat (including the $\overline{TS}$ cycle): (2 + SCY) external clock cycles See Section 12.5.3.1, “Example Wait State Calculation”.
28	Reserved.

Table 12-11. EBI_OR*n* and EBI_CAL_OR*n* Field Descriptions (continued)

Field	Description
29–30 BSCY [0:1]	Burst beats length in clocks. This field determines the number of wait states (external bus cycles) inserted in all burst beats except the first, when the memory controller starts handling the external memory access and thus is using SCY[0:3] to determine the length of the first beat. • Total memory access length for each beat: (1 + BSCY) external clock cycles • Total cycle length (including the $\overline{TS}$ cycle): (2 + SCY) + [(number of beats – 1) x (BSCY + 1)] **Note:** The number of beats (4, 8, 16) is determined by BL and PS bits in the base register. 00 0-clock cycle wait states (1 clock per data beat) 01 1-clock cycle wait states (2 clocks per data beat) 10 2-clock cycle wait states (3 clocks per data beat) 11 3-clock cycle wait states (4 clocks per data beat)
31	Reserved.

12.4 Functional Description

12.4.1 External Bus Interface Features

12.4.1.1 32-Bit Address Bus with Transfer Size Indication

The transfer size for an external transaction is indicated by the TSIZ[0:1] signals during the clock where address is valid. Valid transaction sizes are 8, 16, and 32 bits. In the 416 and 496 BGA packaged devices, only 24 or 26 address lines are pinned out externally, but a full 32-bit decode is done internally to determine the target of the transaction and whether to assert a chip select.

12.4.1.2 32-Bit Data Bus

The entire 32-bit data bus is available for both external memory accesses and transactions involving an external master in the 416 and 496 BGA packaged devices.

12.4.1.3 16-Bit Data Bus

A 16-bit data bus mode is available via the DBM bit in EBI_MCR. See Section 12.1.4.5, “16-Bit Data Bus Mode.”

12.4.1.4 Support for External Master Accesses to Internal Addresses

The EBI allows an external master to access internal address space when the EBI is configured for external master mode in the EBI_MCR. External master operations are described in detail in Section 12.4.2.10, “Bus Operation in External Master Mode.”

12.4.1.5 Memory Controller with Support for Various Memory Types

The EBI contains a memory controller that supports a variety of memory types, including

- Synchronous burst mode flash with external SRAM
- Asynchronous and legacy flash with external SRAM and a compatible interface

Each $\overline{CS}$ bank is configured via its own pair of base and option registers. Each time an internal to external bus cycle access is requested, the internal address is compared with the base address of each valid base register (17 bits are masked) as shown in Figure 12-7. If a match is found, the attributes defined for this bank in its BR and OR are used to control the memory access. If a match is found in more than one bank, the lowest bank matched handles the memory access. For example, bank zero is selected over bank one.

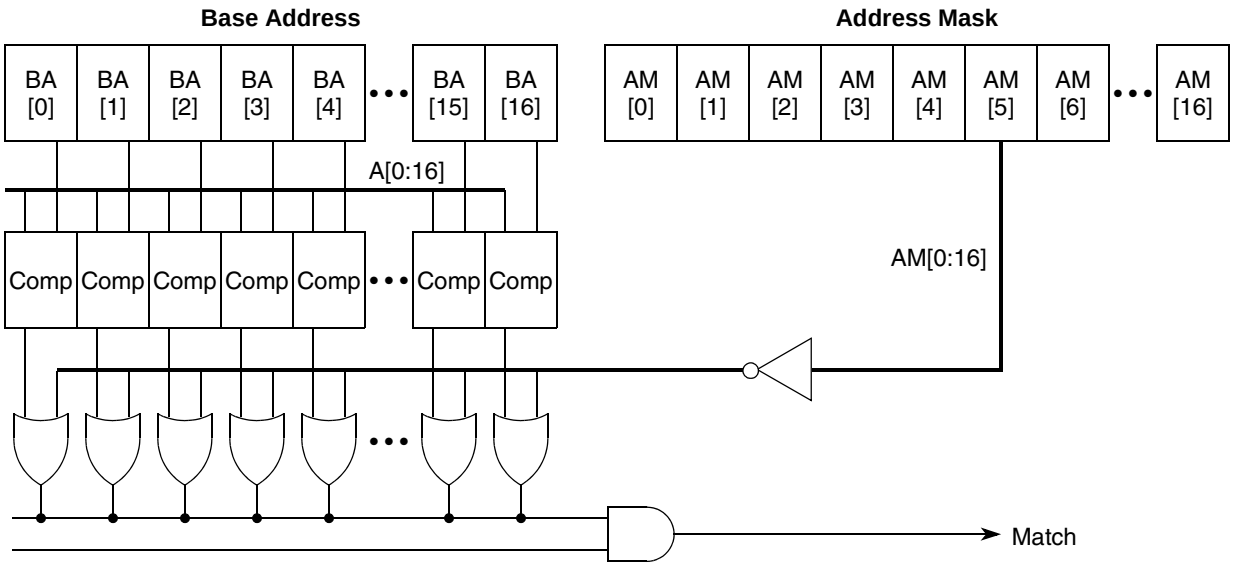


Figure 12-7. Bank Base Address and Match Structure

A match on a valid calibration chip select register overrides a match on any non-calibration chip select register, with CAL_$\overline{CS}$[0] having the highest priority. Thus the full priority of the chip selects is: CAL_$\overline{CS}$[0]....CAL_$\overline{CS}$[3], and then $\overline{CS}$[0]....$\overline{CS}$[3]. When a match is found on one of the chip select banks, all its attributes (from the appropriate base and option registers) are selected for the functional operation of the external memory access, such as:

- Number of wait states for a single memory access, and for any beat in a burst access
- Burst enable
- Port size for the external accessed device

See the following sections for a full description of all chip select attributes:

- Section 12.3.1.6, “EBI Base Registers 0–3 (EBI_BRn) and EBI Calibration Base Registers 0–3 (EBI_CAL_BRn)”
- Section 12.3.1.7, “EBI Option Registers 0–3 (EBI_ORn) and EBI Calibration Option Registers 0–3 (EBI_CAL_ORn)”

When no match is found on any of the chip select banks, the default transfer attributes shown in Table 12-12 are used.

Table 12-12. Default Attributes for Transfers Other than Chip Select

$\overline{CS}$ Attribute	Default Value	Comment
PS	0	32-bit port size
BL	0	Burst is disabled – length is variable
WEBS	0	Write enables
TBDIP	0	Burst is disabled – length variable
BI	1	Burst inhibited
SCY	0	Transfer acknowledge ($\overline{TA}$) used – length variable
BSCY	0	Transfer acknowledge ($\overline{TA}$) used – length variable

12.4.1.6 Burst Support (Wrapped Only)

The EBI supports burst read accesses of external burstable memory. To enable bursts to a particular memory region, clear the BI (Burst Inhibit) bit in the appropriate base register. External burst lengths of 4 and 8 words are supported. Burst length is configured for each chip select by using the BL bit in the appropriate base register. See Section 12.4.2.5, “Burst Transfer” for more details.

In 16-bit data bus mode (EBI_MCR[DBM] = 1), a special 2-beat burst case is supported for reads and writes for 32-bit non-chip select accesses only. This is to allow 32-bit coherent accesses to another MCU. See Section 12.4.2.11, “Non-Chip-Select Burst in 16-bit Data Bus Mode.”

Bursting of accesses that are not controlled by the chip selects is not supported for any other case besides the special case of 32-bit accesses in 16-bit data bus mode.

Burst writes are not supported for any other case besides the special case of 32-bit non-chip select writes in 16-bit data bus mode. Internal requests to write more than 32 bits (such as a cache line) externally are broken up into separate 32-bit or 16-bit external transactions according to the port size. See Section 12.4.2.6, “Small Accesses (Small Port Size and Short Burst Length)” for more detail on these cases.

12.4.1.7 Bus Monitor

When enabled (via the BME bit in the EBI_BMCR), the bus monitor detects when no $\overline{TA}$ assertion is received within a maximum timeout period for non-chip select accesses (that is, accesses that use external $\overline{TA}$). The timeout for the bus monitor is specified by the BMT field in the EBI_BMCR. Each time a timeout error occurs, the BMTF bit is set in the EBI_TESR. The timeout period is measured in external bus (CLKOUT) cycles. Thus the effective real-time period is multiplied (by two or four) when a configurable bus speed mode is used, even though the BMT field itself is unchanged.

12.4.1.8 Port Size Configuration per Chip Select (16 or 32 Bits)

The EBI supports memories with data widths of 16 or 32 bits. The port size (PS) for a chip select is configured using the PS bit in the base register.

12.4.1.9 Port Size Configuration per Calibration Chip Select (16 Bits)

The port size for calibration must be 16 bits wide.

12.4.1.10 Configurable Wait States

From zero to 15 wait states can be programmed for any cycle that the memory controller generates, via the SCY bits in the appropriate option register. From zero to three wait states between burst beats can be programmed using the BSCY bits in the appropriate option register.

12.4.1.11 Four Chip Select ($\overline{CS}$[0:3]) Signals

The EBI contains four chip select signals, controlling four independent memory banks. See Section 12.4.1.5, “Memory Controller with Support for Various Memory Types,” for more details on chip select bank configuration.

12.4.1.12 Support for Dynamic Calibration with Up to Four Chip Selects

The EBI contains four calibration chip select signals, controlling four independent memory banks on an optional second external bus for calibration. See Section 12.4.2.12, “Calibration Bus Operation” for more details on using the calibration bus.

12.4.1.13 Four Write/Byte Enable ($\overline{WE}$/$\overline{BE}$) Signals — 416 BGA Package and VertiCal Assembly

The functionality of the $\overline{WE}$/$\overline{BE}$[0:3] signals depends on the value of the WEBS bit in the base register. Setting WEBS to 1 configures these pins as $\overline{BE}$[0:3], while clearing them to 0 configures them as $\overline{WE}$[0:3]. $\overline{WE}$[0:3] signals are asserted only during write accesses, while $\overline{BE}$[0:3] signals are asserted for both read and write accesses. The timing of the $\overline{WE}$/$\overline{BE}$[0:3] signals remains the same in either case.

The upper write/byte enable ($\overline{WE}$/$\overline{BE}$[0]) indicates that the upper eight bits of the data bus (DATA[0:7]) contain valid data during a write/read cycle. The upper middle write/byte enable ($\overline{WE}$/$\overline{BE}$[1]) indicates that the upper middle eight bits of the data bus (DATA[8:15]) contain valid data during a write/read cycle. The lower middle write/byte enable ($\overline{WE}$/$\overline{BE}$[2]) indicates that the lower middle eight bits of the data bus (DATA[16:23]) contain valid data during a write/read cycle. The lower write/byte enable ($\overline{WE}$/$\overline{BE}$[3]) indicates that the lower eight bits of the data bus (DATA[24:31]) contain valid data during a write/read cycle.

The write/byte enable lines affected in a transaction for a 32-bit port (PS = 0) and a 16-bit port (PS = 1) are shown in Table 12-13. Only big endian byte ordering is supported by the EBI.

Table 12-13. Write/Byte Enable Signal Functions

Transfer Size	TSIZ[0:1]	Address		32-Bit				16-Bit [1]			
		A30	A31	WE/BE[0]	WE/BE[1]	WE/BE[2]	WE/BE[3]	WE/BE[0]	WE/BE[1]	WE/BE[2]	WE/BE[3]
Byte	01	0	0	X	—	—	—	X	—	—	—
	01	0	1	—	X	—	—	—	X	—	—
	01	1	0	—	—	X	—	X	—	—	—
	01	1	1	—	—	—	X		X	—	—
16-bit	10	0	0	X	X	—	—	X	X	—	—
	10	1	0	—	—	X	X	X	X	—	—
32-bit	00	0	0	X	X	X	X	X [2]	X [2]	—	—
Burst	00	0	0	X	X	X	X	X	X	—	—

1 Also applies when DBM = 1 for 16-bit data bus mode.

2 This case consists of two 16-bit external transactions, but for both transactions the WE/BE[0:1] signals are the only WE/BE signals affected.

NOTE: “X” indicates that valid data is transferred on these bits.

12.4.1.14 Configurable Bus Speed Clock Modes

The EBI supports configurable bus speed clock modes. See Section 12.1.4.4, “Configurable Bus Speed Modes,” for more details on this feature.

12.4.1.15 Stop and Module Disable Modes for Power Savings

See Section 12.1.4, “Modes of Operation,” for a description of the power saving modes.

12.4.1.16 Optional Automatic CLKOUT Gating

The EBI has the ability to hold the external CLKOUT pin high when the EBI internal master state machine is idle and no requests are pending. The EBI outputs a signal to the pads logic in the MCU to disable CLKOUT. This feature is disabled out of reset, and can be enabled or disabled by the ACGE bit in the EBI_MCR.

NOTE

This feature must be disabled for multi-master systems. In those cases, one master is getting its clock source from the other master and needs the other master to stay valid continuously.

12.4.1.17 Compatible with MPC5xx External Bus (with Some Limitations)

The EBI is compatible with the external bus of the MPC5xx parts, meaning that it supports most devices supported by the MPC5xx family of parts. However, there are some differences between this EBI and that of the MPC5xx parts that the user needs to be aware of before assuming that an MPC5xx-compatible device works with this EBI. See Section 12.5.5, “Summary of Differences from MPC5xx,” for details.

NOTE

Due to testing and complexity concerns, multi-master (or master/slave) operation between an MPC55xx and MPC5xx is not guaranteed.

12.4.1.18 Misaligned Access Support

The EBI supports misaligned non-burst chip-select transfers only from internal masters. The EBI aligns the accesses when it transmits data to the external bus (splitting them into multiple-aligned accesses) to connect external devices that only support aligned accesses. Burst accesses (internal master) must be 32-bit aligned.

12.4.1.18.1 Misaligned Access Support (32-bit)

Table 12-14 shows the misaligned access cases supported by a 32-bit implementation, as detected on the internal master bus. No support is available for all other misaligned access cases. If a misaligned access occurs that is not supported (such as a non-chip-select or misaligned burst access), the EBI generates a misaligned access error on the internal bus and does not start the access (nor assert $\overline{\text{TEA}}$) externally.

Table 12-14. Misalignment Cases Supported by a 32-bit Internal EBI

Case Numbers [1]	Program Size and Byte Offset	Address [30:31] [2, 3]	Data Bus Byte Strobes [4]		Port Size (HSIZE [5])	Byte Alignment (HUNALIGN)
			External bus big-endian	AHB bus little-endian		
1	Half-word @ 0x0001	01	0110	0110	10 = 32 bits	1 = Misaligned
4	Half-word @ 0x0003 (two AHB transfers)	11 z00	0001 1000	1000 0001	01 = 16 bits [6] 00 = 8 bits	1 = Misaligned 0 = Aligned
8	Word @ 0x0001 (two AHB transfers)	01	0111 1000	1110 0001	10 = 32 bits 00 = 8 bits	1 = Misaligned 0 = Aligned
9	Word @ 0x0002 (two AHB transfers)	10	0011 1100	1100 0011	10 = 32 bits 01 = 16 bits	1 = Misaligned 0 = Aligned
10 11	Word @ 0x0003 (two AHB transfers)	11 z00	0001 1110	1000 0111	10 = 32 bits [6] 10 = 32 bits	1 = Misaligned 1 = Misaligned

1 This is the misaligned case number. Only transfers where HUNALIGN = 1 are numbered as misaligned cases. All other case numbers for byte misalignment do not apply to a 32-bit EBI implementation.

2 The address on internal master AHB bus is not necessarily the address on external ADDR pins.

3 The addresses with a 'z' increment an additional 32-bit word compared to the previous AHB access.

4 Internal byte strobe signals.

5 Internal signal on the AHB bus: 00 = 8 bits; 01 = 16 bits; 10 = 32 bits. HSIZE uses the smallest aligned container that has all the requested bytes, which can result in extra EBI external transfers.

6 The EBI internally treats this case as if HSIZE = 00 (1-byte access).

Table 12-15 shows which external transfers are generated by the EBI for the misaligned access cases in Table 12-14, for each port size.

The number of external transfers for each internal AHB master request is determined by the HSIZE value for that request relative to the port size. For example, a halfword write to 0×0003 (misaligned case #4) with 16-bit port size results in four external 16-bit transfers because of the transfer granularity of 32 bits. For

cases where two or more external transfers are required for one internal transfer request, the external accesses are a small access set, as described in Section 12.4.2.6, “Small Accesses (Small Port Size and Short Burst Length).”

Because all transfers are aligned on the external bus, normal timing diagrams and protocol apply. Do not use the TSIZ[0:1] signals for misaligned accesses.

Table 12-15. Misalignment Cases Supported by a 32-bit EBI (external bus)

Case Number [1]	Program Size and Byte Offset	Port Size	ADDR[30:31] [2, 3]	$\overline{WE}$[0:3] [4]
1	Halfword @ 0x0001	0 = 32 bits	00	1001
		1 = 16 bits	00 10	1011 0111
4	Halfword @ 0x0003 Two AHB transfers	0 = 32 bits	11 [5] z00	1110 0111
		1 = 16 bits	11 [5] z00	1011 0111
8	Word @ 0x0001 Two AHB transfers	0 = 32 bits	00 z00	1000 0111
		1 = 16 bits	00 10	1011 0011
9	Word @ 0x0002 Two AHB transfers	0 = 32 bits	00 z00	1100 0011
		1 = 16 bits	10 z00	0011 0011
10	Word @ 0x0003 Two AHB transfers	0 = 32 bits	11 [5]	1110
		1 = 16 bits	11 [5]	1011
11	Word @ 0x0003 Two AHB transfers	0 = 32 bits	z00	0001
		1 = 16 bits	z00 z10	0011 0111

1 Misaligned case numbers, from Table 12-14.

2 External ADDR pins are not necessarily the address on the internal master AHB bus.

3 Addresses designated by a ‘z’ use bit 29 to increment the transmit address to the next word. For all other cases, address bit 29 is unchanged.

4 External $\overline{WE}$ pins. These pins have negative polarity, opposite of the internal byte strobes in Table 12-14.

5 Treated as 1-byte access.

12.4.2 External Bus Operations

The following sections provide a functional description of the external bus, the bus cycles provided for data transfer operations, bus arbitration, and error conditions.

12.4.2.1 External Clocking

The CLKOUT signal sets the frequency of operation for the bus interface directly. Internally, the MCU uses a phase-locked loop (PLL) circuit to generate a master clock for all of the MCU circuitry (including the EBI) which is phase-locked to the CLKOUT signal. In general, all signals for the EBI are specified with respect to the rising-edge of the CLKOUT signal, and they are guaranteed to be sampled as inputs or changed as outputs with respect to that edge.

12.4.2.2 Reset

Upon detection of internal reset, the EBI immediately terminates all transactions.

12.4.2.3 Basic Transfer Protocol

The basic transfer protocol defines the sequence of actions that must occur on the external bus to perform a complete bus transaction. A simplified scheme of the basic transfer protocol is shown in Figure 12-8.

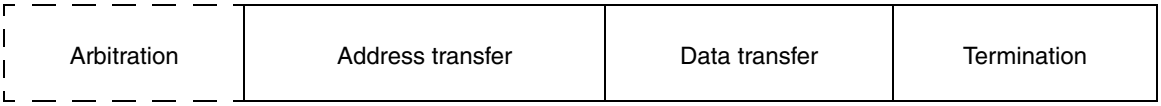


Figure 12-8. Basic Transfer Protocol

The arbitration phase is where bus ownership is requested and granted. This phase is not needed in single master mode because the EBI is the permanent bus owner in this mode. Arbitration is discussed in detail in Section 12.4.2.8, “Arbitration.”

The address transfer phase specifies the address for the transaction and the transfer attributes that describe the transaction. The signals related to the address transfer phase are $\overline{TS}$, ADDR, $\overline{CS}$[0:3], RD_$\overline{WR}$, TSIZ[0:1], and $\overline{BDIP}$. The address and its related signals (with the exception of $\overline{TS}$, $\overline{BDIP}$) are driven on the bus with the assertion of the $\overline{TS}$ signal, and kept valid until the bus master receives $\overline{TA}$ asserted (the EBI holds them one cycle beyond $\overline{TA}$ for writes and external $\overline{TA}$ accesses). For writes with internal $\overline{TA}$, RD_$\overline{WR}$ is not held one cycle past $\overline{TA}$.

The data transfer phase performs the transfer of data, from master to slave (in write cycles) or from slave to master (on read cycles), if any is to be transferred. The data phase transfer a single beat of data (one to four bytes) for non-burst operations or a 2-beat (special EBI_MCR[DBM] = one case only), 4-beat, 8-beat, or 16-beat burst of data (two or four bytes per beat depending on port size) when burst is enabled.

On a write cycle, the master must not drive write data until after the address transfer phase is complete. This avoids electrical contentions when switching between drivers. The master must start driving write data one cycle after the address transfer cycle. The master can stop driving the data bus as soon as it samples the $\overline{TA}$ line asserted on the rising edge of CLKOUT. To facilitate asynchronous write support, the EBI keeps driving valid write data on the data bus until one clock after the rising edge when RD_$\overline{WR}$ (and $\overline{WE}$ for chip select accesses) are negated. See Figure 12-14 for an example of write timing.

On a read cycle, the master accepts the data bus contents as valid on the rising edge of the CLKOUT in which the $\overline{TA}$ signal is sampled asserted. See Figure 12-10 for an example of read timing.

The termination phase is where the cycle is terminated by the assertion of either $\overline{TA}$ (normal termination) or $\overline{TEA}$ (termination with error). Termination is discussed in detail in Section 12.4.2.9, "Termination Signals Protocol."

12.4.2.4 Single-Beat Transfer

The flow and timing diagrams in this section are for the EBI configured as single master mode. Therefore, arbitration is not needed and is not shown in these diagrams. See Section 12.4.2.10, "Bus Operation in External Master Mode," to read how the flow and timing diagrams change for external master mode.

12.4.2.4.1 Single-Beat Read Flow

The handshakes for a single beat read cycle are illustrated in the following flow and timing diagrams.

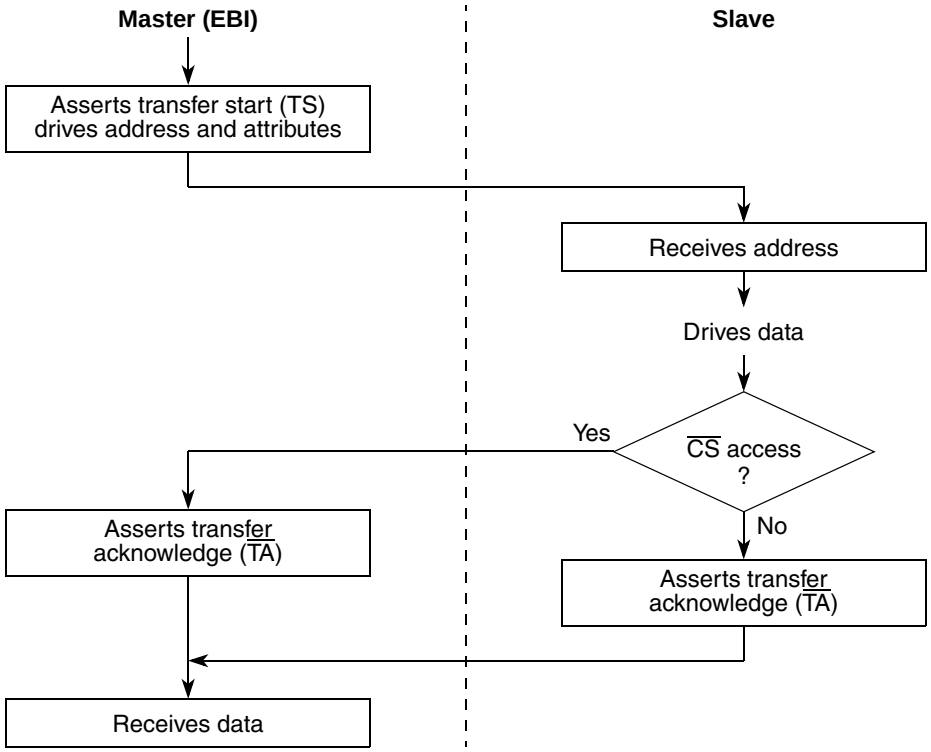


Figure 12-9. Basic Flow Diagram of a Single-Beat Read Cycle

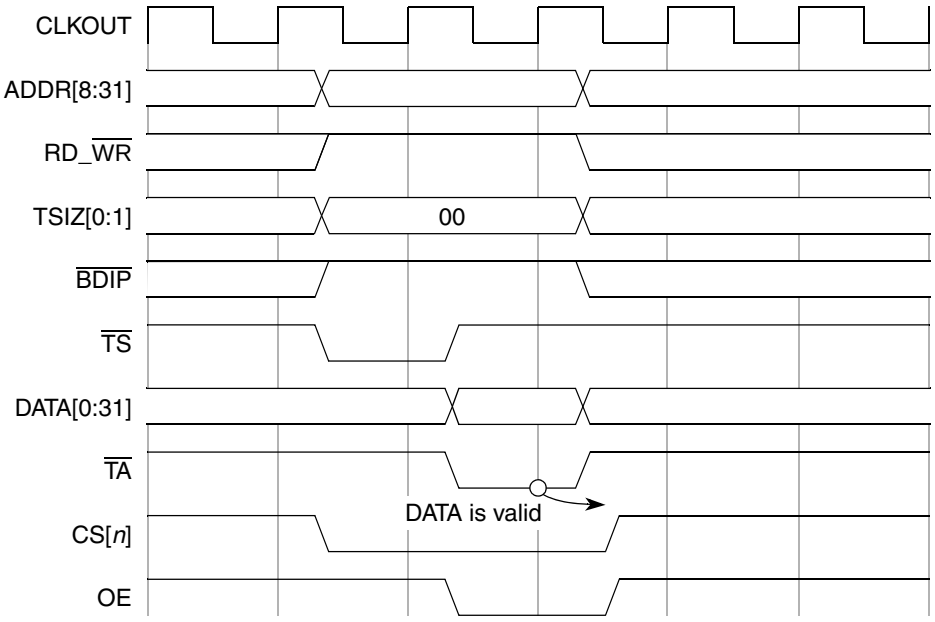


Figure 12-10. Single-Beat 32-bit Read Cycle, CS Access, Zero Wait States

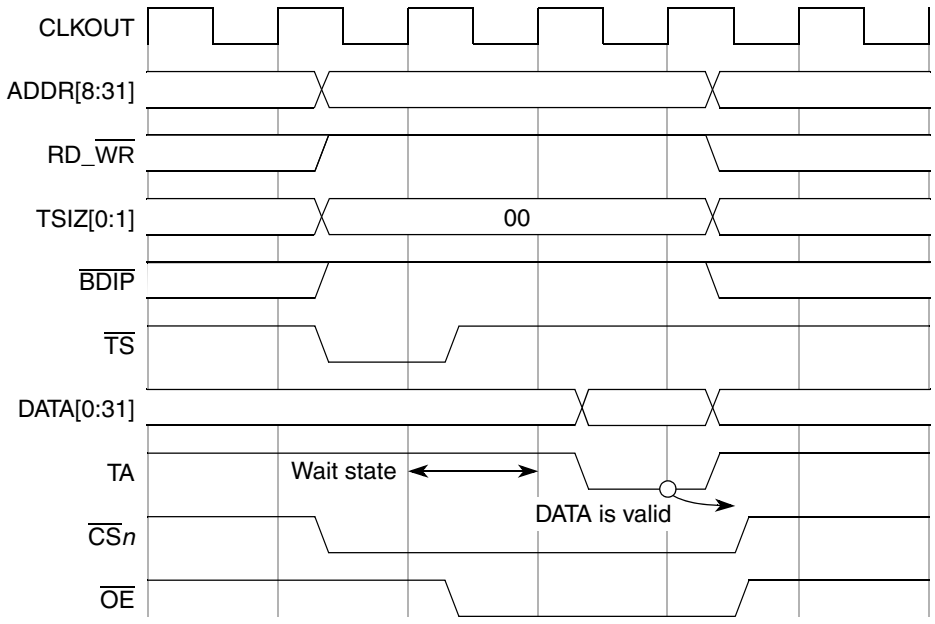
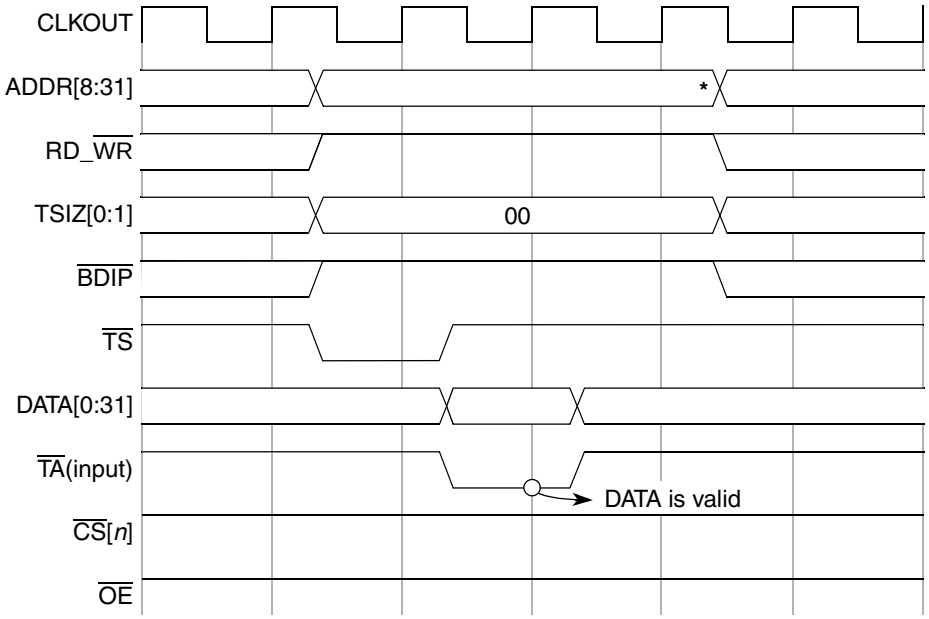


Figure 12-11. Single-Beat 32-bit Read Cycle, CS Access, One Wait State



* The EBI drives address and control signals an extra cycle because it uses a latched version of the external TA (1 cycle delayed) to terminate the cycle.

Figure 12-12. Single-Beat 32-bit Read Cycle, Non-CS Access, Zero Wait States

12.4.2.4.2 Single-Beat Write Flow

The handshakes for a single beat write cycle are illustrated in the following flow and timing diagrams.

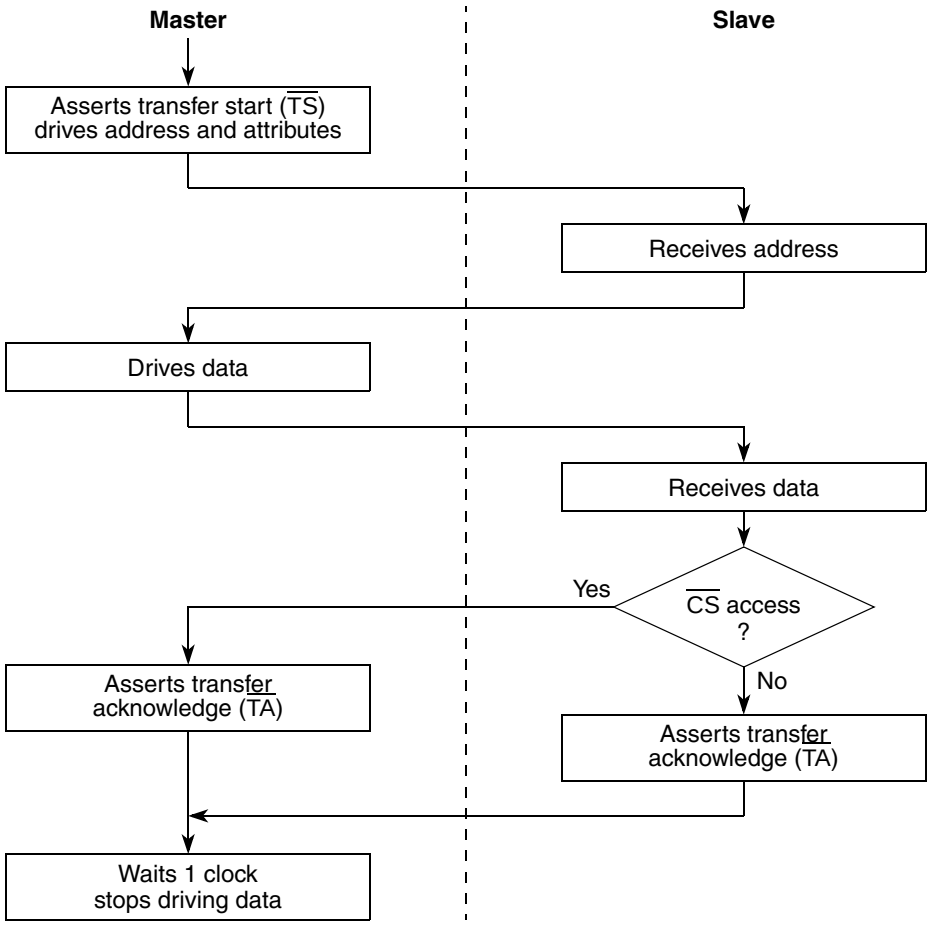


Figure 12-13. Basic Flow Diagram of a Single-Beat Write Cycle

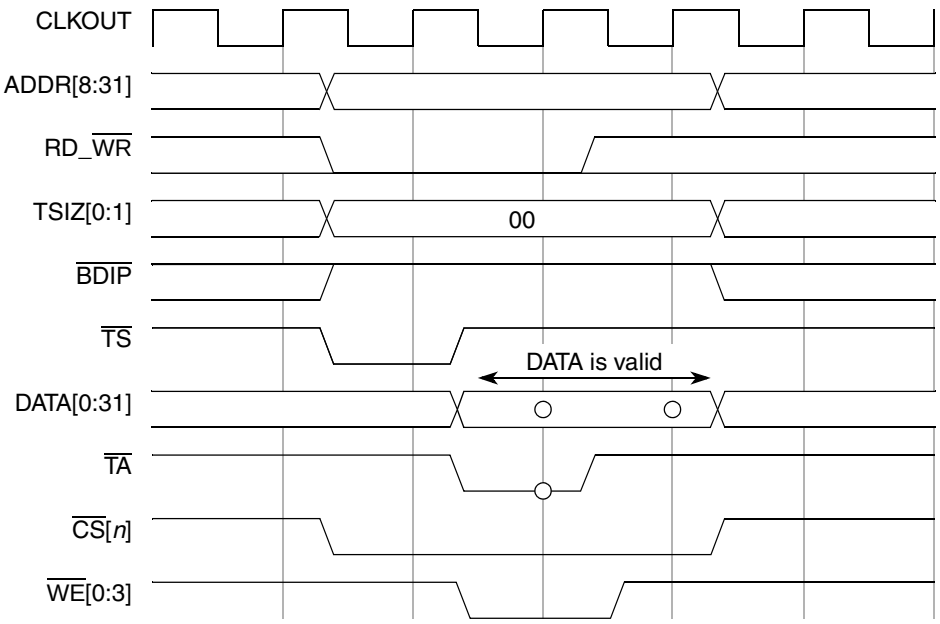


Figure 12-14. Single-Beat 32-bit Write Cycle, CS Access, Zero Wait States

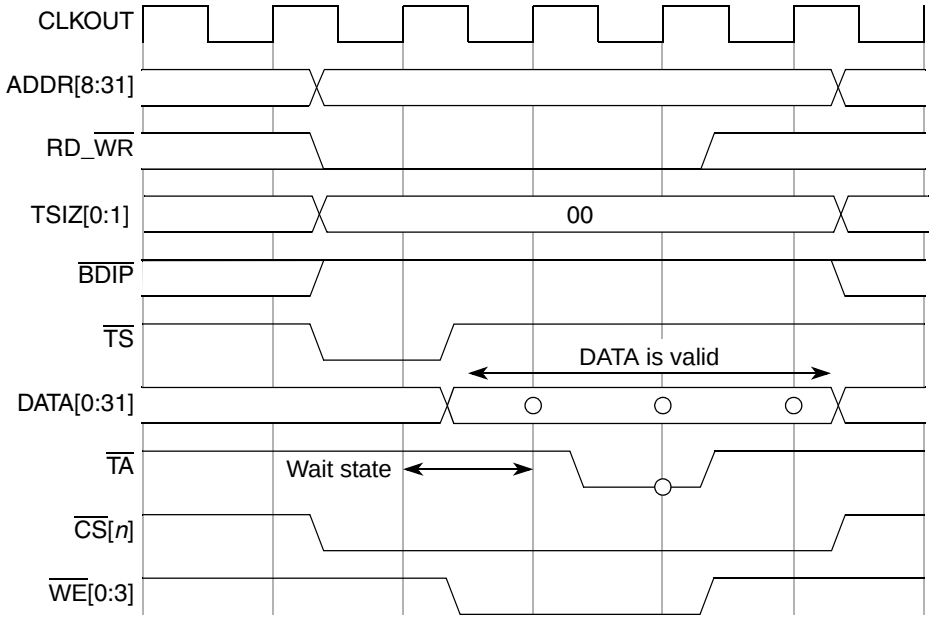
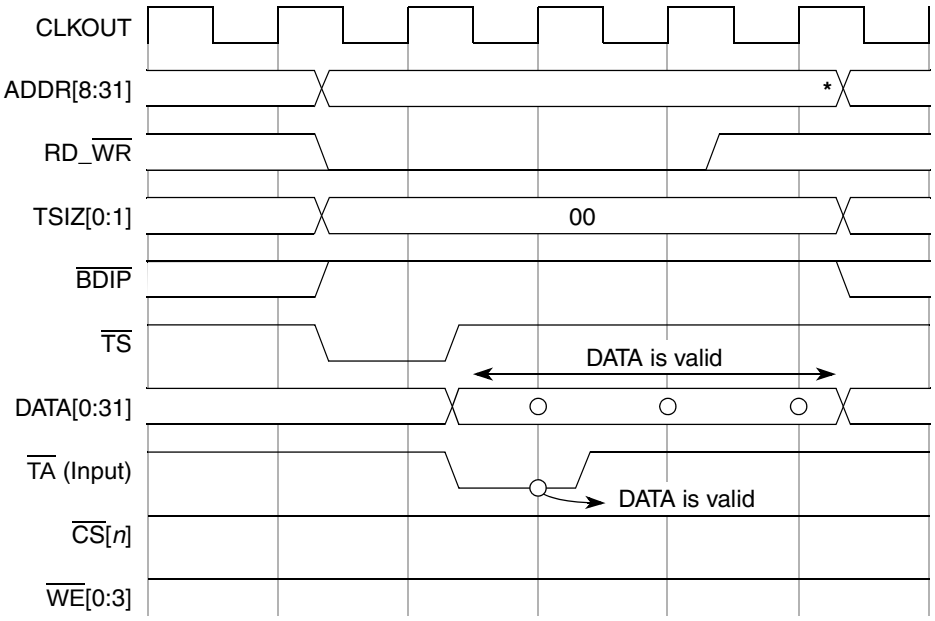


Figure 12-15. Single-Beat 32-bit Write Cycle, CS Access, One Wait State



* The EBI drives address and control signals an extra cycle because it uses a latched version of the external TA (1 cycle delayed) to terminate the cycle.

Figure 12-16. Single-Beat 32-bit Write Cycle, Non-CS Access, Zero Wait States

12.4.2.4.3 Back-to-Back Accesses

Due to internal bus protocol, one dead cycle is necessary between back-to-back external bus accesses that are not part of a set of small accesses (see Section 12.4.2.6, "Small Accesses (Small Port Size and Short Burst Length)" for small access timing). A dead cycle refers to a cycle between the TA of a previous transfer and the TS of the next transfer.

NOTE

In some cases, CS remains asserted during this dead cycle, such as the cases of back-to-back writes or read-after-write to the same chip-select. See Figure 12-20 and Figure 12-21.

Besides this dead cycle, in most cases, back-to-back accesses on the external bus do not cause any change in the timing from that shown in the previous diagrams, and the two transactions are independent of each other.

The only exception to this is back-to-back accesses when the first access ends with an externally-driven TA or TEA. In these cases, an extra cycle is required between the end of the first access and the TS assertion of the second access. See Section 12.4.2.9, "Termination Signals Protocol," for more details. Figure 12-17, Figure 12-18, and Figure 12-19 show a few examples of back-to-back accesses on the external bus.

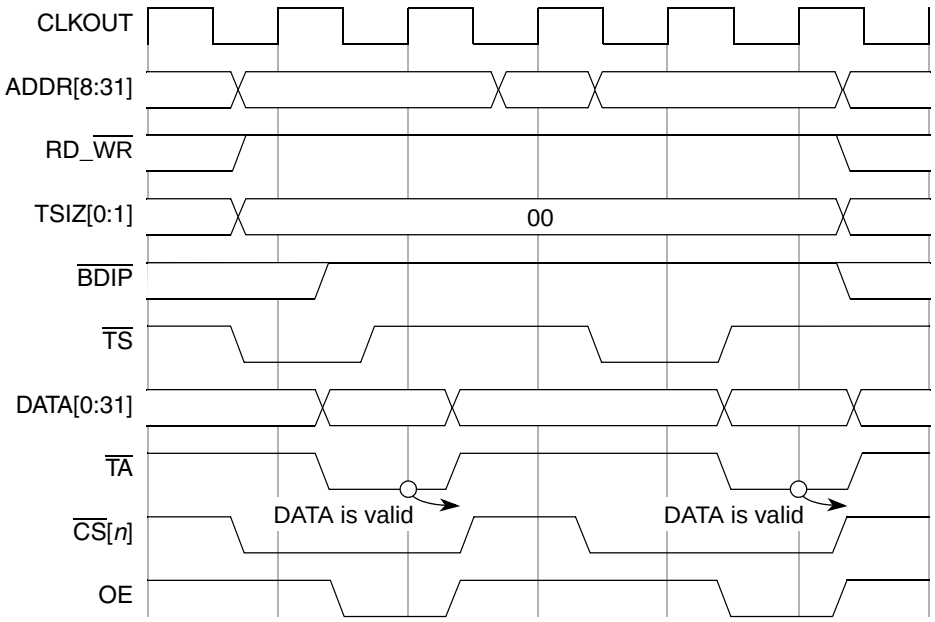


Figure 12-17. Back-to-Back 32-bit Reads to the Same $\overline{CS}$ Bank

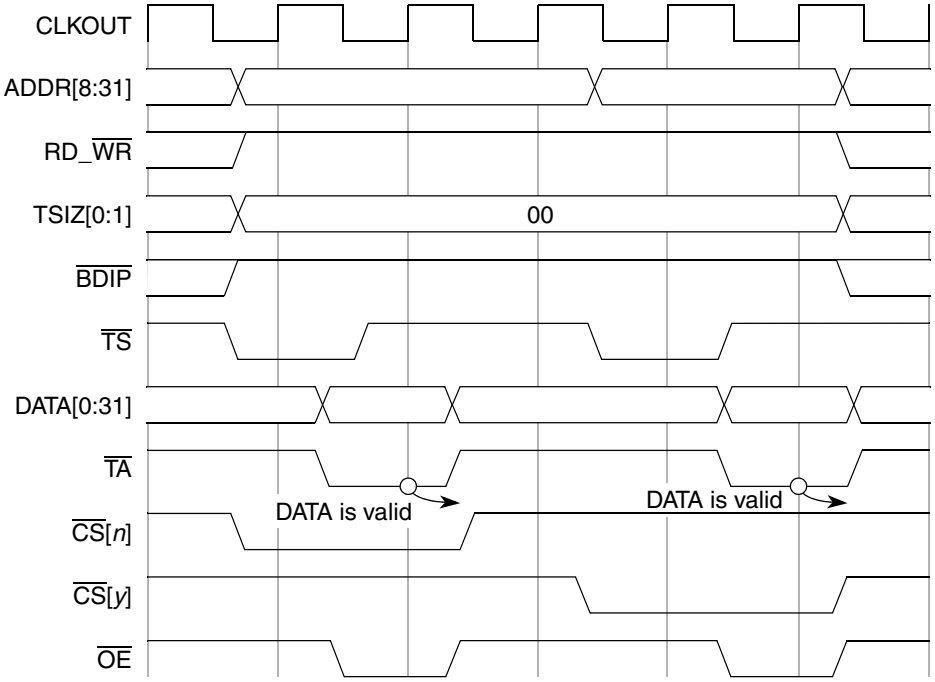


Figure 12-18. Back-to-Back 32-bit Reads to Different $\overline{CS}$ Banks

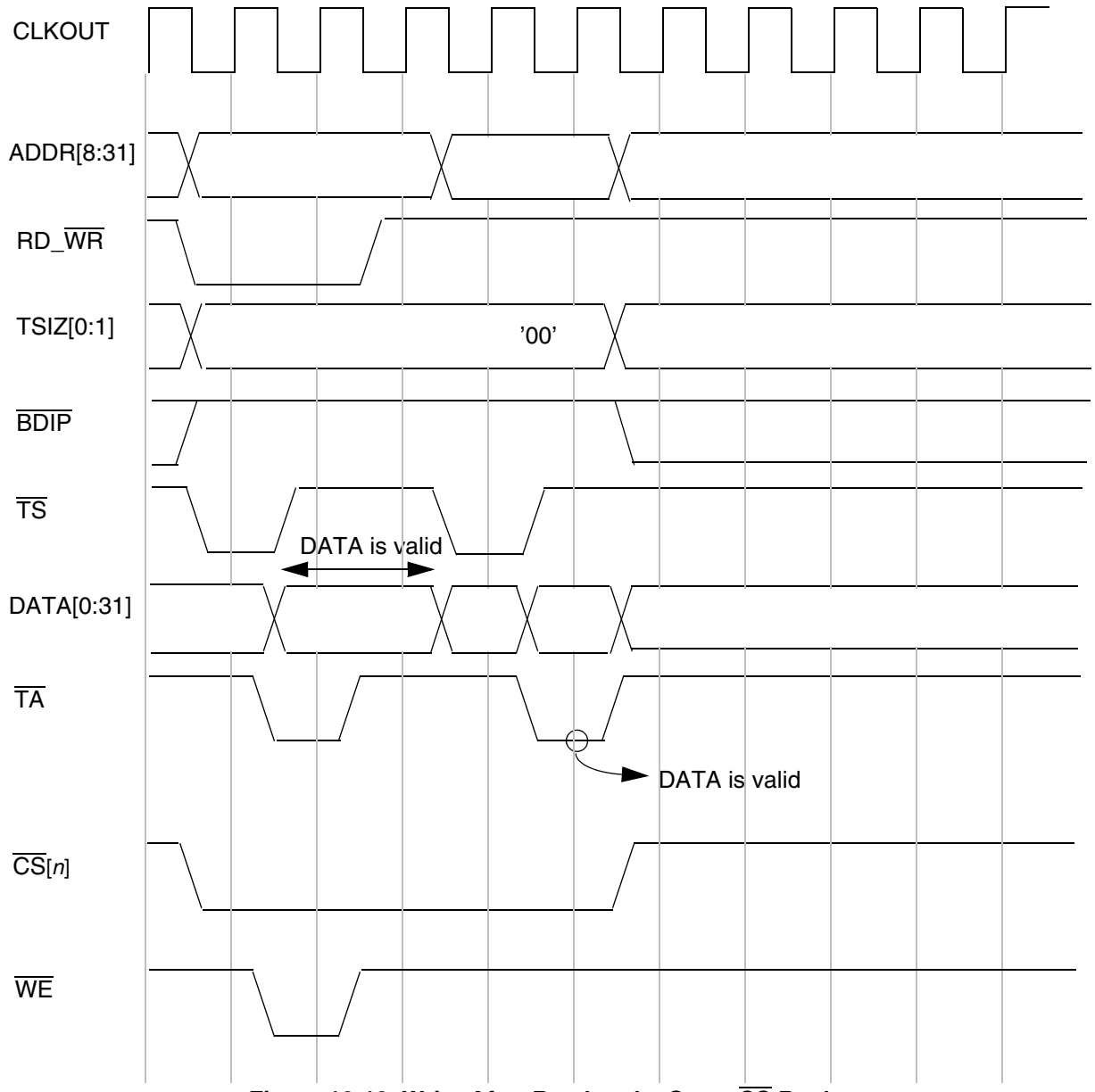


Figure 12-19. Write-After-Read to the Same CS Bank

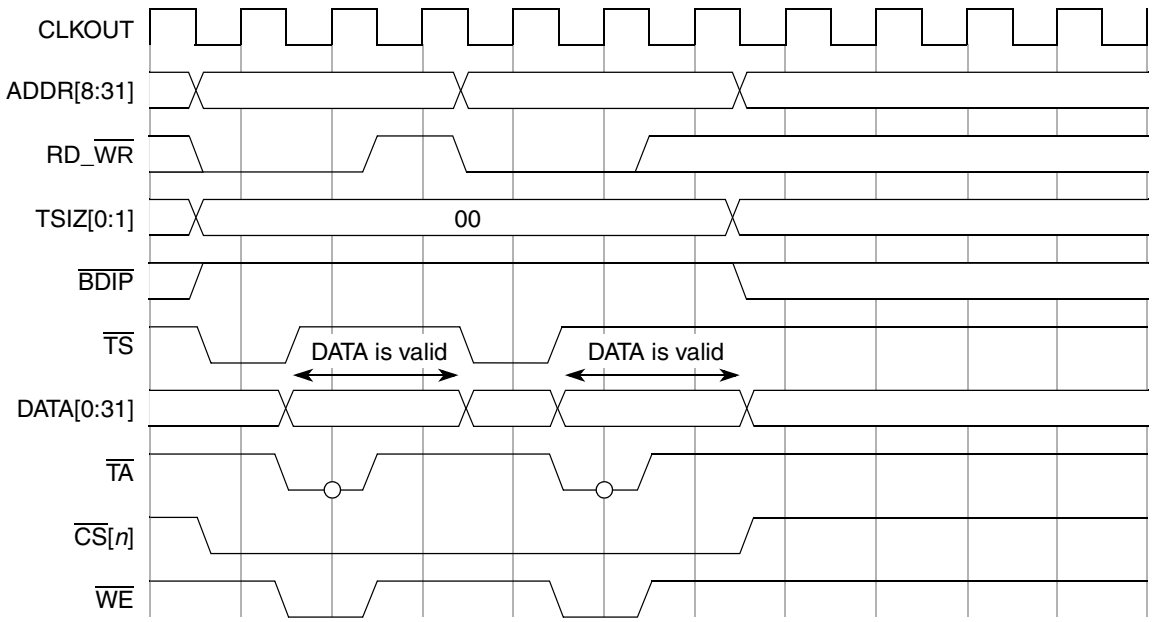


Figure 12-20. Back-to-Back 32-bit Writes to the Same $\overline{CS}$ Bank

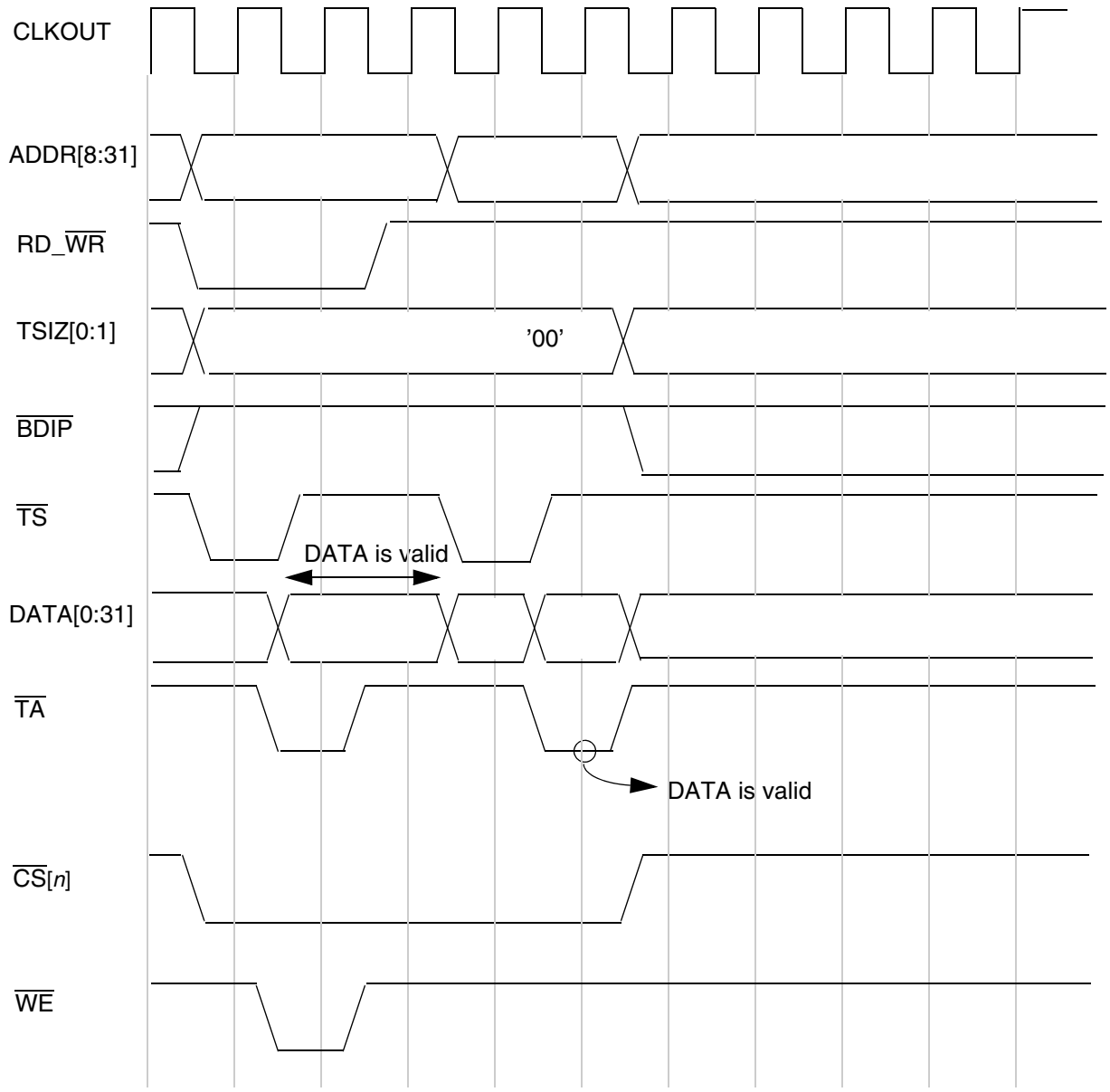


Figure 12-21. Read-After-Write to the Same $\overline{CS}$ Bank

12.4.2.5 Burst Transfer

The EBI supports wrapping 32-byte critical-doubleword-first burst transfers. Bursting is supported only for internally-requested cache-line size (32-byte) read accesses to external devices that use the chip selects[1]. Accesses from an external master or to devices operating without a chip select are always single beat. If an internal request to the EBI indicates a size of less than 32 bytes, the request is fulfilled by running one or more single-beat external transfers, not by an external burst transfer.

1. Except for the special case of a 32-bit non-chip select access in 16-bit data bus mode. See Section 12.4.2.11.

An 8-word wrapping burst reads eight 32-bit words by supplying a starting address that points to one of the words (doubleword aligned) and requiring the memory device to sequentially drive each word on the data bus. The selected slave device must internally increment ADDR[27:29] (also ADDR[30] in the case of a 16-bit port size device) of the supplied address for each transfer, until the address reaches an 8-word boundary, and then wrap the address to the beginning of the 8-word boundary. The address and transfer attributes supplied by the EBI remain stable during the transfers, and the EBI terminates each beat transfer by asserting $\overline{\text{TA}}$. The EBI requires that addresses be aligned to a doubleword boundary on all burst cycles.

Table 12-16 shows the burst order of beats returned for an 8-word burst to a 32-bit port.

Table 12-16. Wrap Bursts Order

Burst Starting Address ADDR[27:28]	Burst Order (Using 32-bit Port Size)
00	word0 –> word1 –> word2 –> word3 –> word4 –> word5 –> word6 –> word7
01	word2 –> word3 –> word4 –> word5 –> word6 –> word7 –> word0 –> word1
10	word4 –> word5 –> word6 –> word7 –> word0 –> word1 –> word2 –> word3
11	word6 –> word7 –> word0 –> word1 –> word2 –> word3 –> word4 –> word5

The general case of burst transfers assumes that the external memory has 32-bit port size and 8-word burst length. The EBI can also burst from 16-bit port size memories, taking twice as many external beats to fetch the data as compared to a 32-bit port with the same burst length. The EBI can also burst from 16-bit or 32-bit memories that have a 4-word burst length (BL = 1 in the appropriate base register). In this case, two external 4-word burst transfers (wrapping on 4-word boundary) are performed to fulfill the internal 8-word request. This operation is considered atomic by the EBI, so the EBI does not allow other unrelated master accesses or bus arbitration to intervene between the transfers. For more details and a timing diagram, see Section 12.4.2.6.3, “Small Access Example #3: 32-byte Read to 32-bit Port with BL = 1.”

During burst cycles, the $\overline{\text{BDIP}}$ (burst data in progress) signal is used to indicate the duration of the burst data. During the data phase of a burst read cycle, the EBI receives data from the addressed slave. If the EBI needs more than one data, it asserts the $\overline{\text{BDIP}}$ signal. Upon receiving the data prior to the last data, the EBI negates $\overline{\text{BDIP}}$. Thus, the slave stops driving new data after it receives the negation of $\overline{\text{BDIP}}$ on the rising edge of the clock. Some slave devices have their burst length and timing configurable internally and thus not support connecting to a $\overline{\text{BDIP}}$ pin. In this case, $\overline{\text{BDIP}}$ is driven by the EBI normally, but the output is ignored by the memory and the burst data behavior is determined by the internal configuration of the EBI and slave device. When the TBDIP bit is set in the appropriate base register, the timing for $\overline{\text{BDIP}}$ is altered. See Section 12.4.2.5.1, “TBDIP Effect on Burst Transfer,” for this timing.

Since burst writes are not supported by the EBI[1], the EBI negates $\overline{\text{BDIP}}$ during write cycles.

1. Except for the special case of a 32-bit non-chip select access in 16-bit data bus mode. See Section 12.4.2.11.

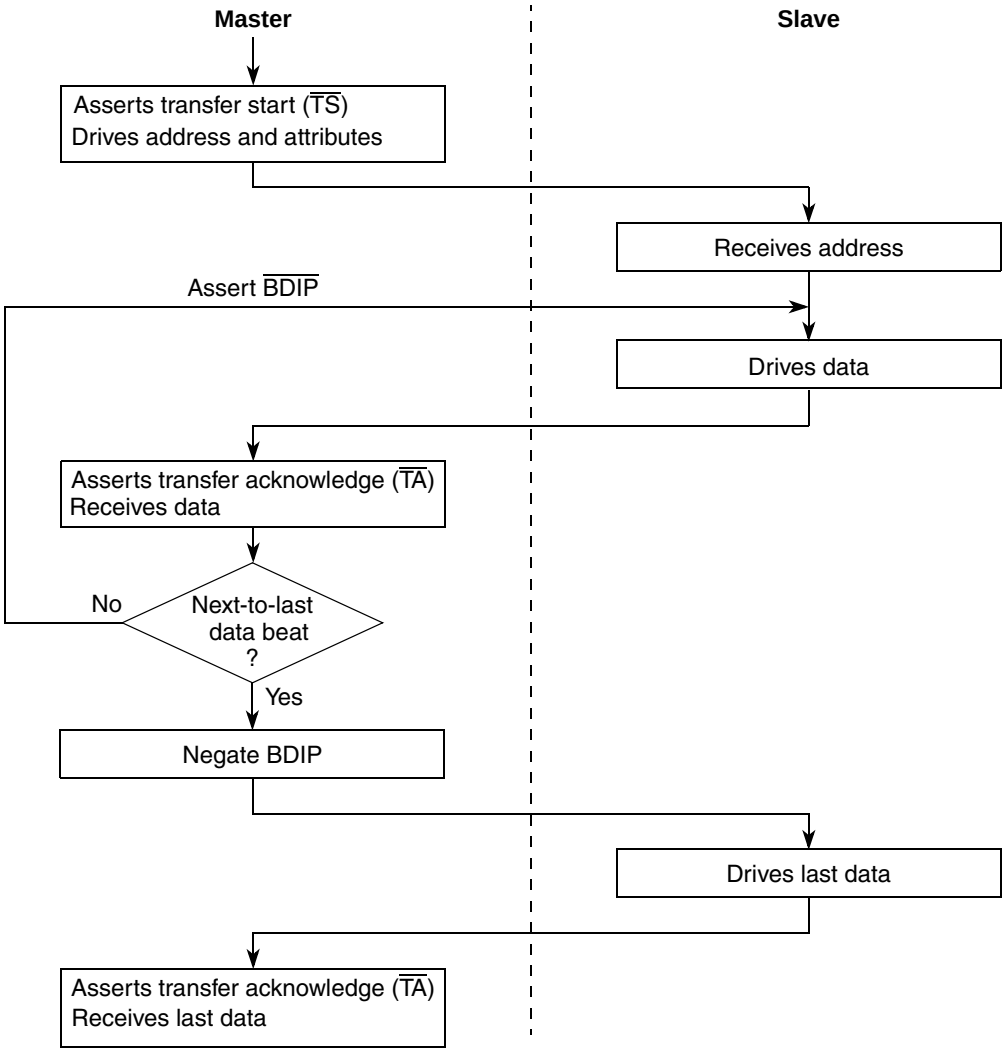


Figure 12-22. Basic Flow Diagram of a Burst Read Cycle

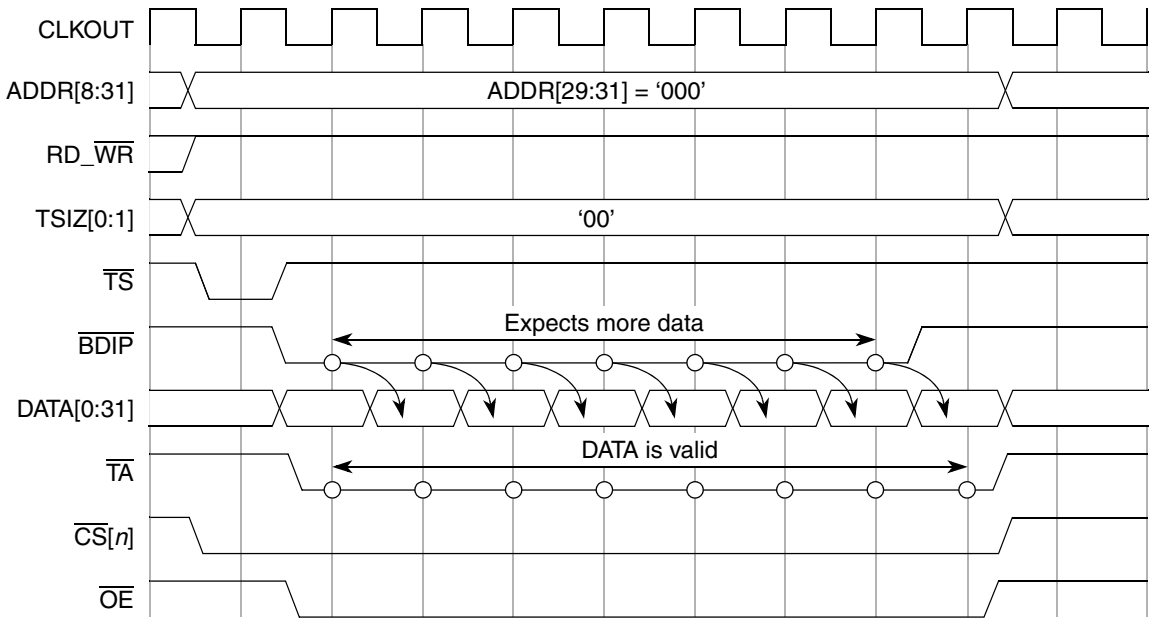


Figure 12-23. Burst 32-bit Read Cycle, Zero Wait States

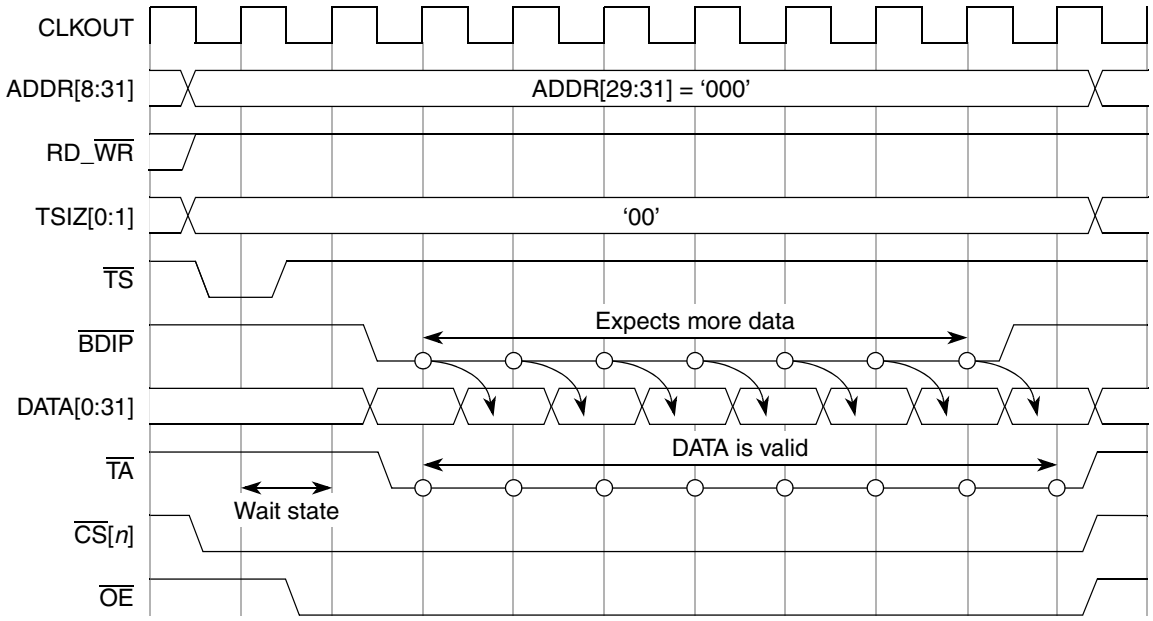


Figure 12-24. Burst 32-bit Read Cycle, One Initial Wait State

12.4.2.5.1 TBDIP Effect on Burst Transfer

Some memories require different timing on the $\overline{\text{BDIP}}$ signal than the default to run burst cycles. Using the default value of TBDIP = 0 in the appropriate EBI base register results in $\overline{\text{BDIP}}$ being asserted (SCY + 1) cycles after the address transfer phase, and being held asserted throughout the cycle regardless of the wait states between beats (BSCY). Figure 12-25 shows an example of the TBDIP = 0 timing for a four-beat burst with BSCY = 1.

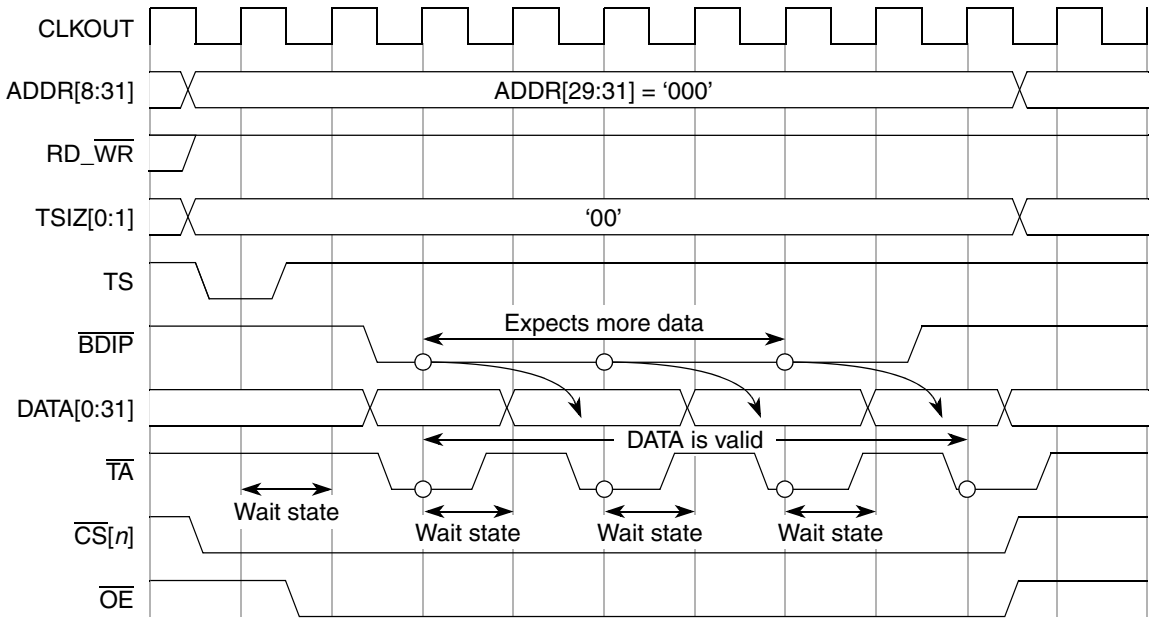


Figure 12-25. Burst 32-bit Read Cycle, One Wait State between Beats, TBDIP = 0

When using TBDIP = 1, the $\overline{\text{BDIP}}$ behavior changes to toggle between every beat when BSCY is a non-zero value. Figure 12-26 shows an example of the TBDIP = 1 timing for the same four-beat burst shown in Figure 12-25.

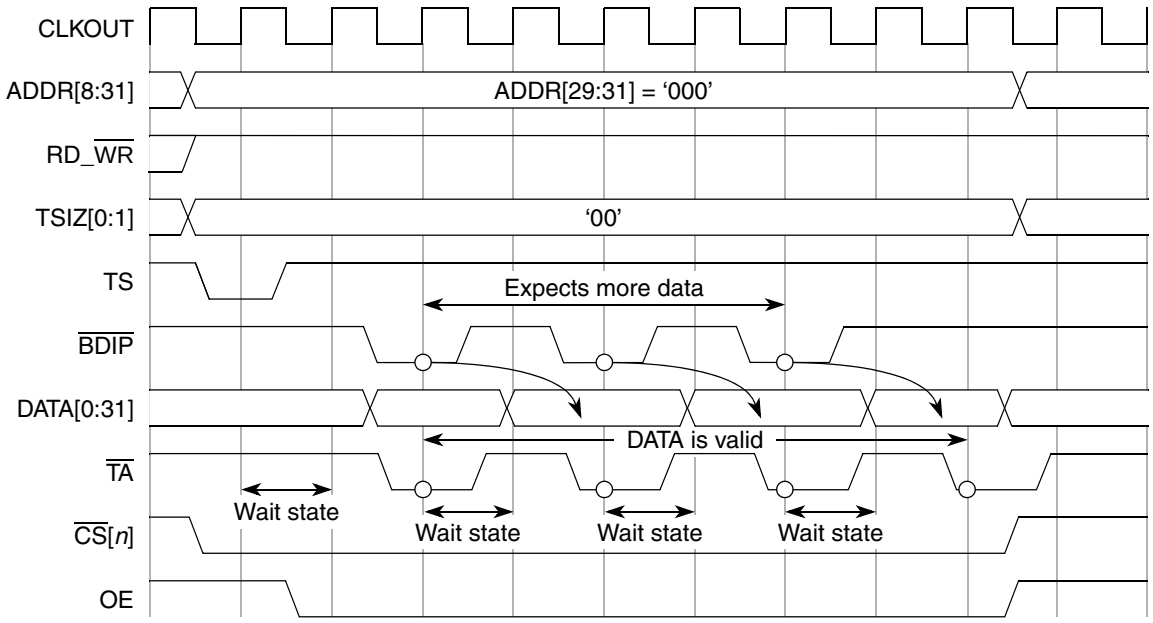


Figure 12-26. Burst 32-bit Read Cycle, One Wait State between Beats, TBDIP = 1

12.4.2.6 Small Accesses (Small Port Size and Short Burst Length)

In this context, a small access refers to an access whose burst length and port size are such that the number of bytes requested by the internal master cannot all be fetched (or written) in one external transaction. This is the case when the base register's burst length bit (EBI_BR*n*[BL]) and port size bit (EBI_BR*n*[PS]) are set such that one of two situations occur:

- Burst accesses are inhibited and the number of bytes requested by the master is greater than the port size (16 or 32 bit) can accommodate in a single access.
- Burst accesses are enabled and the number of bytes requested by the master is greater than the selected burst length (four words or eight words).

If this is the case, the EBI initiates multiple transactions until all the requested data is transferred. All the transactions initiated to complete the data transfer are considered as an atomic transaction, so the EBI does not allow other unrelated master accesses to intervene between the transfers. In external master mode, this means that the EBI keeps $\overline{\text{BB}}$ asserted and does not grant the bus to another master until the atomic transaction is complete.

Table 12-17 shows all the combinations of burst length, port size, and requested byte count that cause the EBI to run multiple external transactions to fulfill the request.

Table 12-17. Small Access Cases

Byte Count Requested by Internal Master	Burst Length	Port Size	Number of External Accesses to Fulfill Request
Non-burstable Chip-Select Banks (BI = 1) or Non-Chip-Select Access			
4	1 beat	16-bit	2 or 1[1]
8	1 beat	32-bit	2
8	1 beat	16-bit	4
32	1 beat	32-bit	8
32	1 beat	16-bit	16
Burstable Chip-Select Banks (BI = 0)			
32	4 words	16-bit (8 beats) 32-bit (4 beats)	2

[1] In 32-bit data bus mode (DBM = 0 in EBI_MCR), two accesses are performed. In 16-bit data bus mode (DBM = 1), one 2-beat burst access is performed and this is not considered a small access case. See Section 12.4.2.11, "Non-Chip-Select Burst in 16-bit Data Bus Mode" for this special DBM = 1 case.

In most cases, the timing for small accesses is the same as for normal single-beat and burst accesses, except that multiple back-to-back external transfers are executed for each internal request. These transfers have no additional dead cycles in-between that are not present for back-to-back stand-alone transfers except for the case of writes with an internal request size greater than 64 bits, discussed in Section 12.4.2.6.2, "Small Access Example #2: 32-byte Write with External TA."

The following sections show a few examples of small accesses. The timing for the remaining cases in Table 12-17 can be extrapolated from these and the other timing diagrams in this document.

12.4.2.6.1 Small Access Example #1: 32-bit Write to 16-bit Port

Figure 12-27 shows an example of a 32-bit write to a 16-bit port, requiring two 16-bit external transactions.

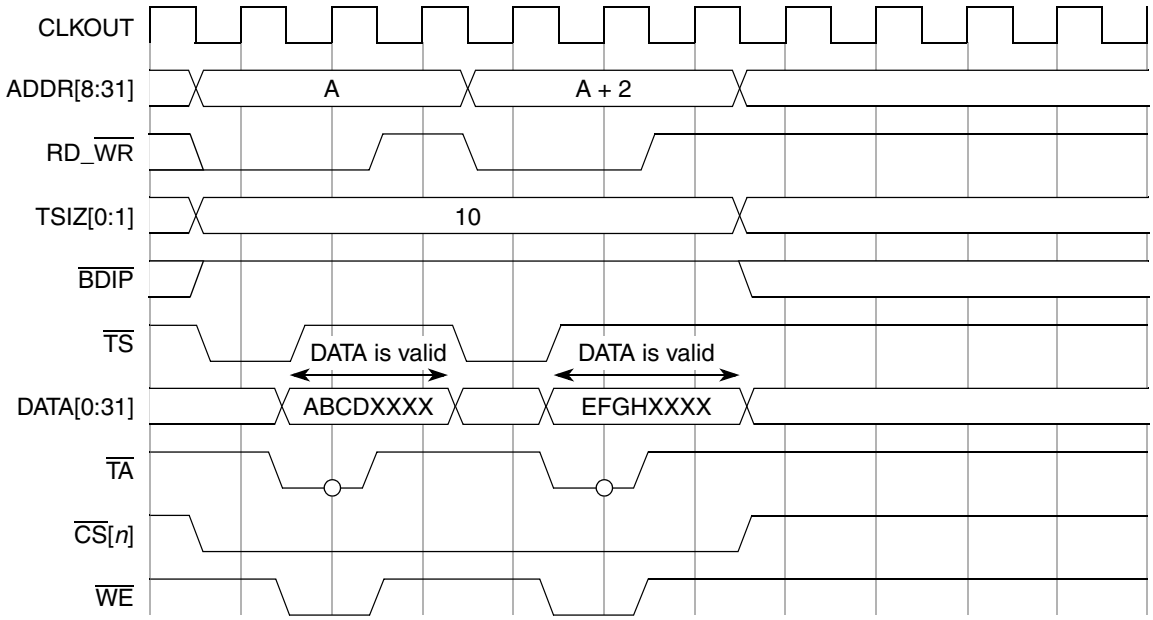
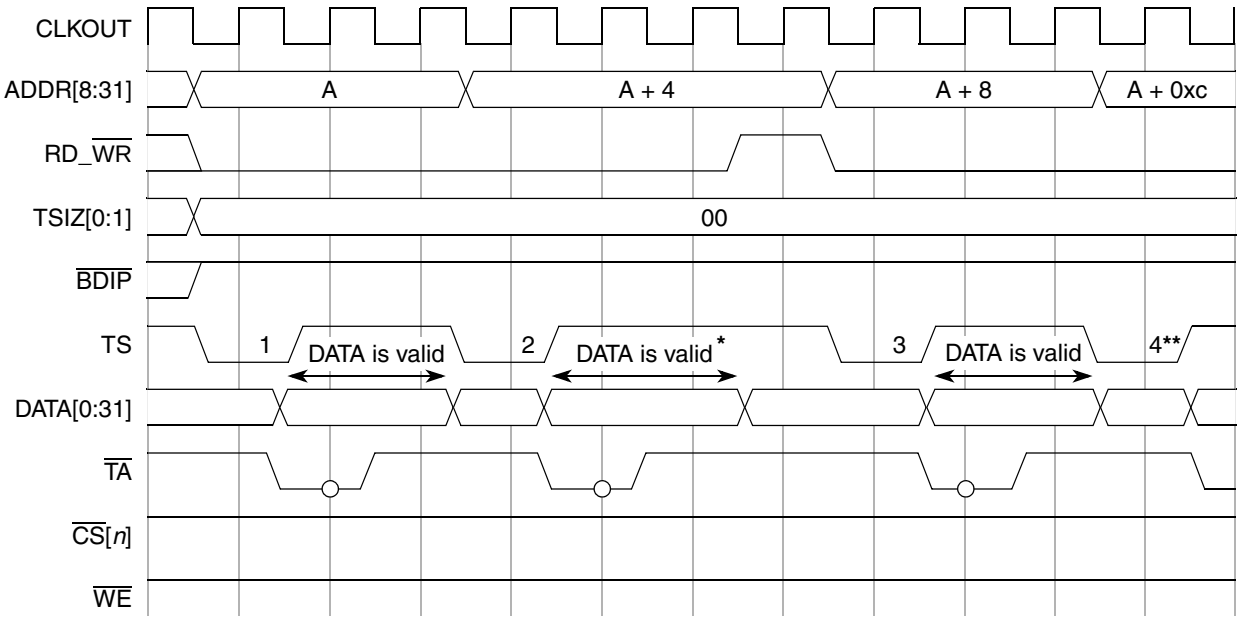


Figure 12-27. Single Beat 32-bit Write Cycle, 16-bit Port Size, Basic Timing

12.4.2.6.2 Small Access Example #2: 32-byte Write with External TA

Figure 12-28 shows an example of a 32-byte write to a non-chip select device, such as an external master, using external TA, requiring eight 32-bit external transactions. Due to the use of external TA, RD_WR does not toggle between the accesses unless that access is the end of a 64-bit boundary. In this case, an extra cycle is required between TA and the next TS to get the next 64-bits of write data internally and RD_WR negates during this extra cycle.



* This extra cycle is required after accesses 2, 4, and 6 to get the next 64-bits of internal write data.

** Four more external accesses (not shown) are required to complete the internal 32-byte request. The timing of these is the same as accesses 1-4 shown in this diagram.

Figure 12-28. 32-Byte Write Cycle with External TA, Basic Timing

12.4.2.6.3 Small Access Example #3: 32-byte Read to 32-bit Port with BL = 1

Figure 12-29 shows an example of a 32-byte read to a 32-bit burst enabled port with burst length of 4 words, requiring two 16-byte external transactions. For this case, the address for the second 4-word burst access is calculated by adding 0x10 to the lower 5 bits of the first address (no carry), and then masking out the lower 4 bits to fix them at zero.

Table 12-18. Examples of 4-word Burst Addresses

First Address	Lower 5 bits of the First Address + 0x10 (no carry)	Final Second Address (after masking lower 4 bits)
0x000	0x10	0x10
0x008	0x18	0x10
0x010	0x00	0x00
0x018	0x08	0x00
0x020	0x30	0x30
0x028	0x38	0x30
0x030	0x20	0x20
0x038	0x28	0x20

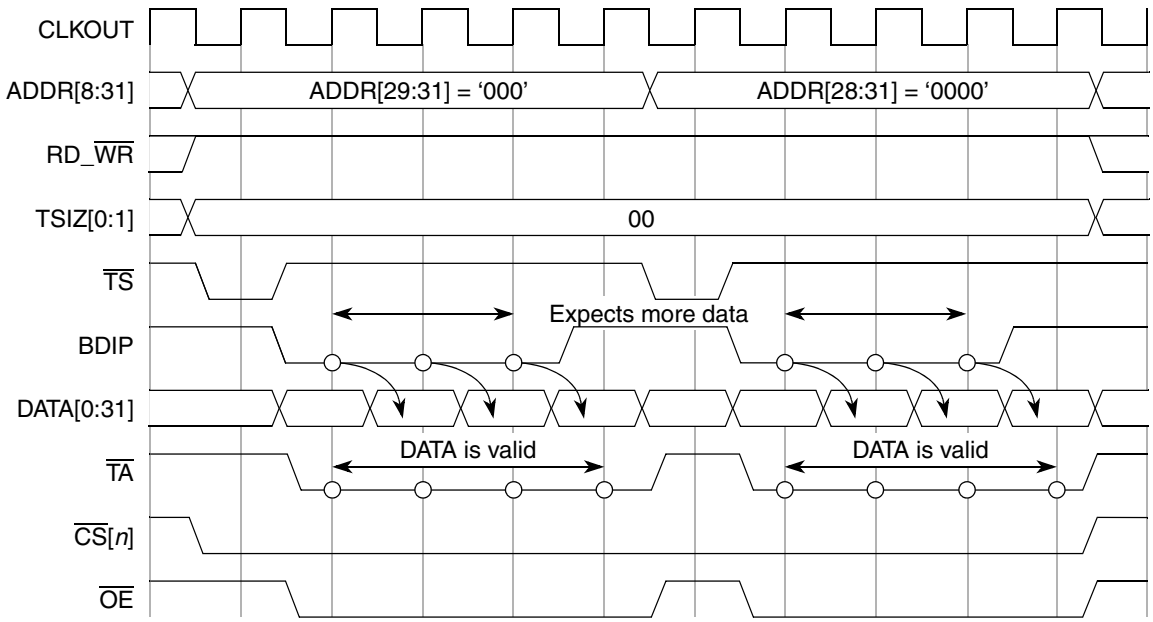


Figure 12-29. 32-Byte Read with Back-to-Back 16-Byte Bursts to 32-Bit Port, Zero Wait States

12.4.2.7 Size, Alignment, and Packaging on Transfers

Table 12-19 shows the allowed sizes that an internal or external master can request from the EBI. EBI transfer request sizes not listed in the table are undefined. No error signal is asserted for these invalid cases.

Table 12-19. Valid EBI Transaction Sizes (Number of Bytes)

Internal Master	External Master
1	1
2	2
4	4
3 [1]	
8	
32	

[1] Some misaligned access cases can result in 3-byte writes. These cases are treated as power-of-2 sized requests by the EBI, using WE/BE[0:3], to ensure only the correct 3 bytes are written.

Even though misaligned non-burst transfers from internal masters are supported, the EBI naturally aligns the accesses when it sends them out to the external bus, splitting them into multiple aligned accesses if necessary.

Natural alignment for the EBI means:

- Byte access can have any address
- 16-bit access, address bit 31 must equal zero

- 32-bit access, address bits 30–31 must equal zero
- For burst accesses of any size, address bits 29–31 must equal zero

The EBI never generates a misaligned external access, so a multi-master system with two MCUs can never have a misaligned external access. In the erroneous case that an externally-initiated misaligned access does occur, the EBI errors the access (by asserting $\overline{\text{TEA}}$ externally) and does not initiate the access on the internal bus.

The EBI requires that the portion of the data bus used for a transfer to/from a particular port size be fixed. A 32-bit port must reside on data bus bits 0–31, and a 16-bit port must reside on bits 0–15.

The figures and tables in this section use the following conventions:

- The most significant byte of a 32-bit operand is OP0; OP3 is the least significant byte.
- Depending on the address of the access, the two bytes of a 16-bit operand are:
  - OP0 (most significant) and OP1; or
  - OP2 (most significant) and OP3
- The single byte of a byte-length operand is OP0, OP1, OP2, or OP3, depending on the address of the access.

The convention can be seen in Figure 12-30.

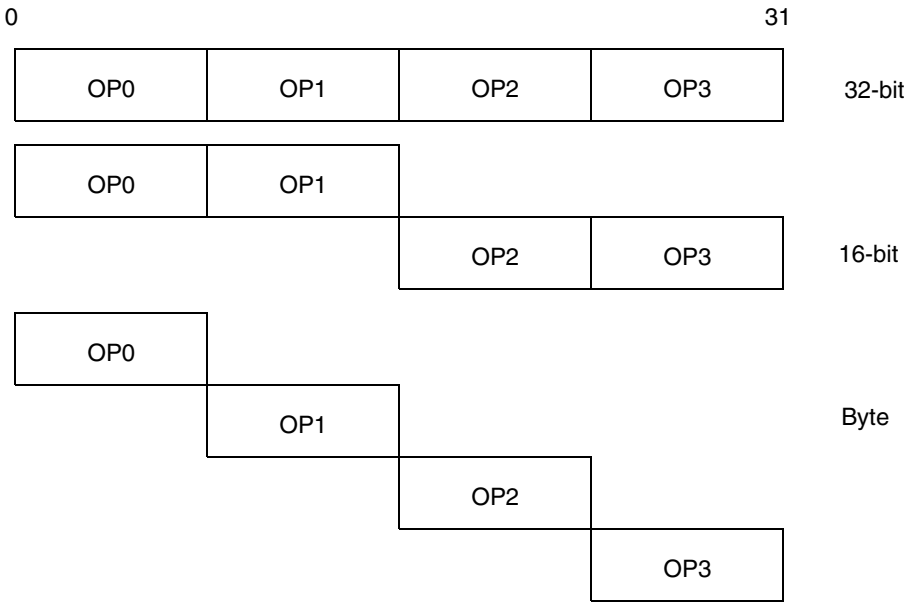


Figure 12-30. Internal Operand Representation

Figure 12-31 shows the device connections on the DATA[0:31] bus.

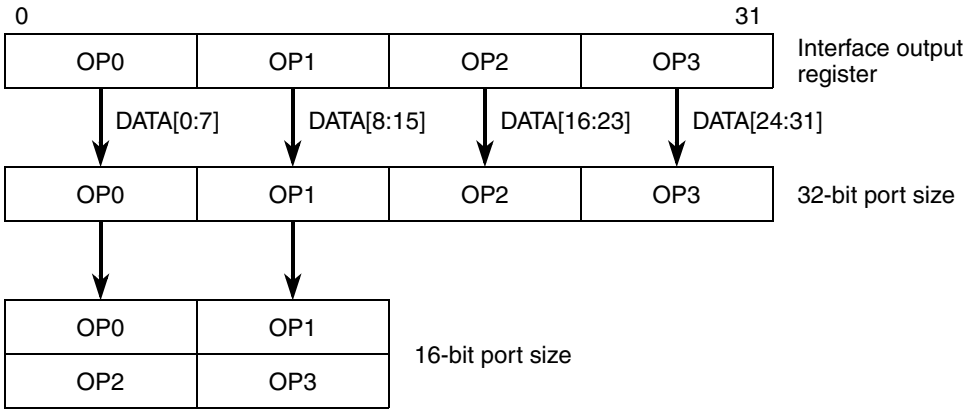


Figure 12-31. Interface to Different Port Size Devices

Table 12-20 lists the bytes required on the data bus for read cycles. The bytes indicated as '—' are not required during that read cycle.

Table 12-20. Data Bus Requirements for Read Cycles

Transfer Size	TSIZ[0:1]	Address		32-Bit Port Size				16-Bit Port Size [1]	
		A[30]	A[31]	D[0:7]	D[8:15]	D[16:23]	D[24:31]	D[0:7]	D[8:15]
Byte	01	0	0	OP0	—	—	—	OP0	—
	01	0	1	—	OP1	—	—	—	OP1
	01	1	0	—	—	OP2	—	OP2	—
	01	1	1	—	—	—	OP3	—	OP3
16-bit	10	0	0	OP0	OP1	—	—	OP0	OP1
	10	1	0	—	—	OP2	OP3	OP2	OP3
32-bit	00	0	0	OP0	OP1	OP2	OP3	OP0 or OP2 [2]	OP1 or OP3

[1] Also applies when DBM = 1 for 16-bit data bus mode.

[2] This case consists of two 16-bit external transactions, the first fetching OP0 and OP1, the second fetching OP2 and OP3.

Table 12-21 lists the patterns of the data transfer for write cycles when accesses are initiated by the MCU. The bytes indicated as '—' are not driven during that write cycle.

Table 12-21. Data Bus Contents for Write Cycles

Transfer Size	TSIZ[0:1]	Address		32-Bit Port Size				16-Bit Port Size[1]	
		A[30]	A[31]	D[0:7]	D[8:15]	D[16:23]	D[24:31]	D[0:7]	D[8:15]
Byte	01	0	0	OP0	—	—	—	OP0	—
	01	0	1	OP1	OP1	—	—	—	OP1
	01	1	0	OP2	—	OP2	—	OP2	—
	01	1	1	OP3	OP3	—	OP3	—	OP3
16-bit	10	0	0	OP0	OP1	—	—	OP0	OP1
	10	1	0	OP2	OP3	OP2	OP3	OP2	OP3
32-bit	00	0	0	OP0	OP1	OP2	OP3	OP0 or OP2 [2]	OP1 or OP3

1 Also applies when DBM = 1 for 16-bit data bus mode.

2 This case consists of two 16-bit external transactions, the first writing OP0 and OP1, the second writing OP2 and OP3.

12.4.2.8 Arbitration

The external bus design provides for a single bus master at any one time, either the MCU or an external device. One of the external devices on the bus has the capability of becoming bus master for the external bus. Bus arbitration be handled either by an external central bus arbiter or by the internal on-chip arbiter. The arbitration configuration (external or internal) is set via the EARB bit in the EBI_MCR.

Each bus master must have bus request, bus grant, and bus busy signals. The signals are described in detail in Section 12.2.1, "Detailed Signal Descriptions." The device that needs the bus asserts the bus request ($\overline{BR}$) signal. The device then waits for the arbiter to assert the bus grant ($\overline{BG}$) signal. In addition, the new master must sample the bus busy ($\overline{BB}$) signal to ensure that no other master is driving the bus before it can assert bus busy to assume ownership of the bus. The new master must sample bus busy negated for two cycles before asserting bus busy, to avoid any potential conflicts. Any time the arbiter has taken the bus grant away from the master, and the master wants to execute a new cycle, the master must re-arbitrate before a new cycle can begin. The EBI, however, whether the internal or external arbiter is used, guarantees data coherency for access to a small port size and for decomposed bursts. This means that the EBI does not release the bus before the completion of the transactions which are considered as atomic.

Figure 12-32 describes the basic protocol for bus arbitration.

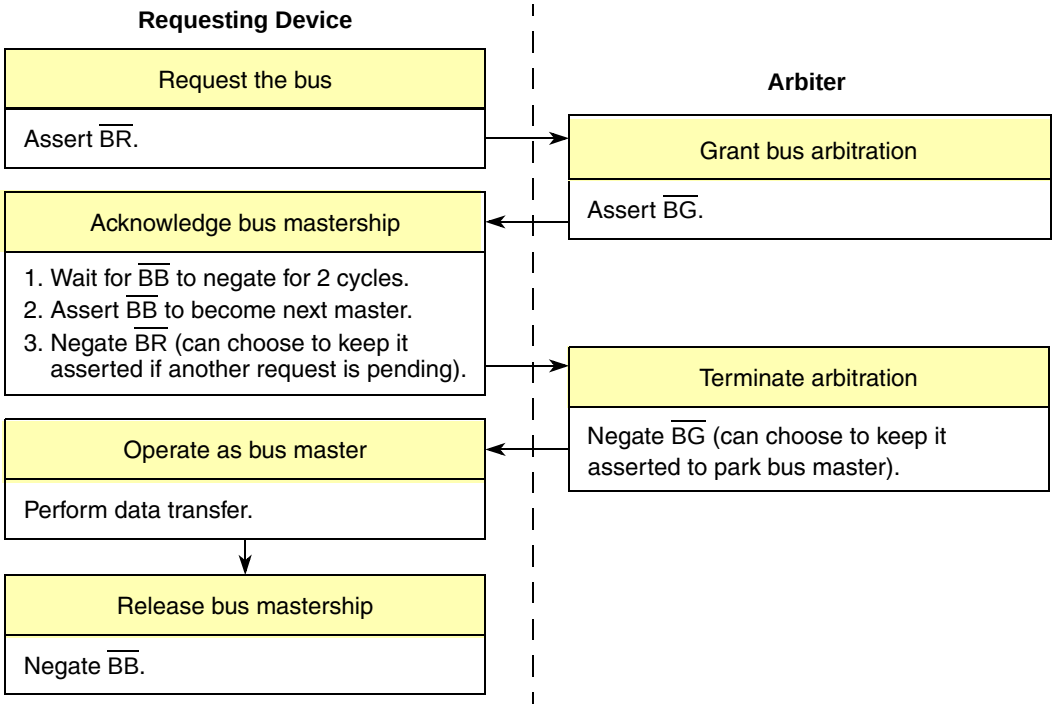
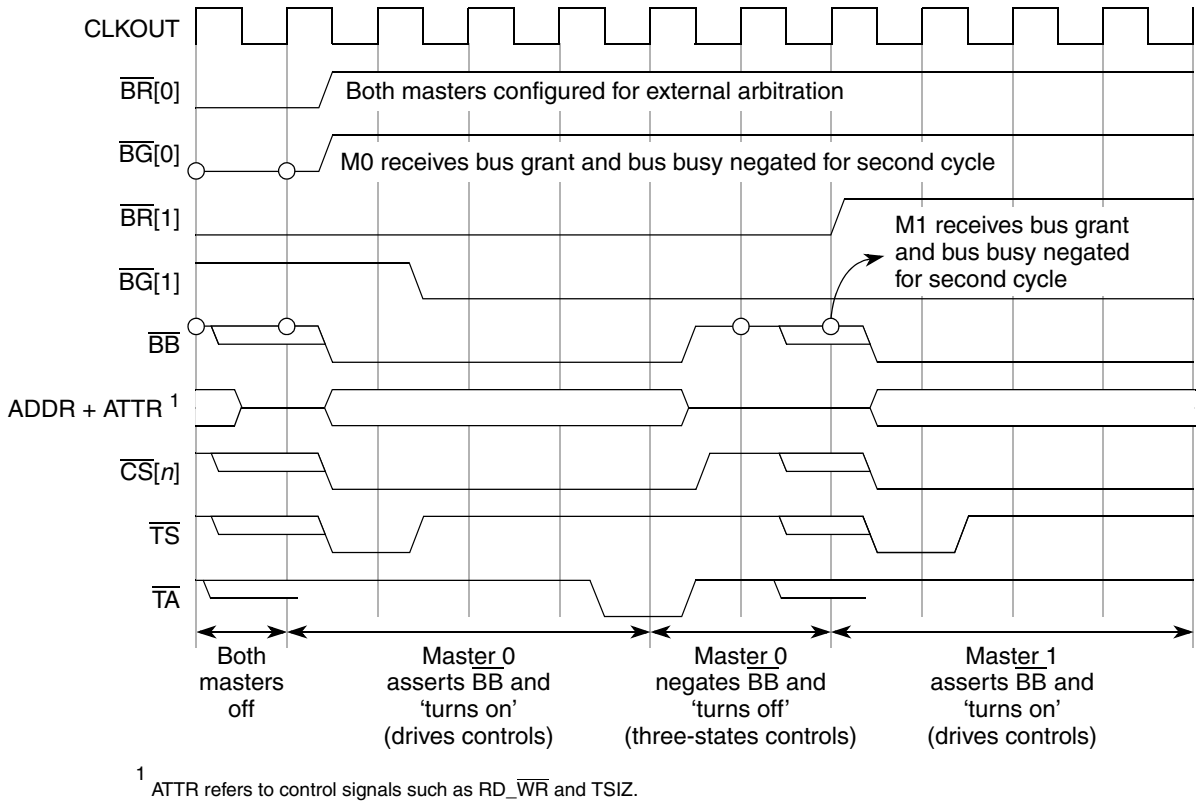


Figure 12-32. Bus Arbitration Flow Chart

12.4.2.8.1 External (or Central) Bus Arbiter

The external arbiter can be either another MCU in a two master system, or a separate central arbiter device. When an MCU is configured to use external arbitration, that MCU asserts $\overline{BR}$ when it needs ownership of the external bus, and it waits for $\overline{BG}$ to be asserted from the external arbiter. For timing reasons, a latched (one cycle delayed) version of $\overline{BG}$ is used by the EBI in external arbitration mode. This is not a requirement of the protocol. After $\overline{BG}$ assertion is received and $\overline{BB}$ is sampled negated for two cycles, the MCU asserts $\overline{BB}$ and initiates the transaction. An MCU operating under external arbitration run back-to-back accesses without rearbitration as long as it is still receiving $\overline{BG}$ asserted. If $\overline{BG}$ is negated during a transaction, the MCU must rearbitrate for the bus before the next transaction. The determination of priority between masters is determined entirely by the external arbiter in this mode.

Figure 12-33 shows example timing for the case of two masters connected to a central arbiter. In this case, the $\overline{BR}$ 0 and $\overline{BR}$ 1 signals shown are inputs to the arbiter from the $\overline{BR}$ pin of each master. The $\overline{BG}$ 0 and $\overline{BG}$ 1 signals are outputs from the arbiter that connect to the $\overline{BG}$ pin of each master.



1 ATTR refers to control signals such as RD_WR and TSIZ.

Figure 12-33. Central Arbitration Timing Diagram

12.4.2.8.2 Internal Bus Arbiter

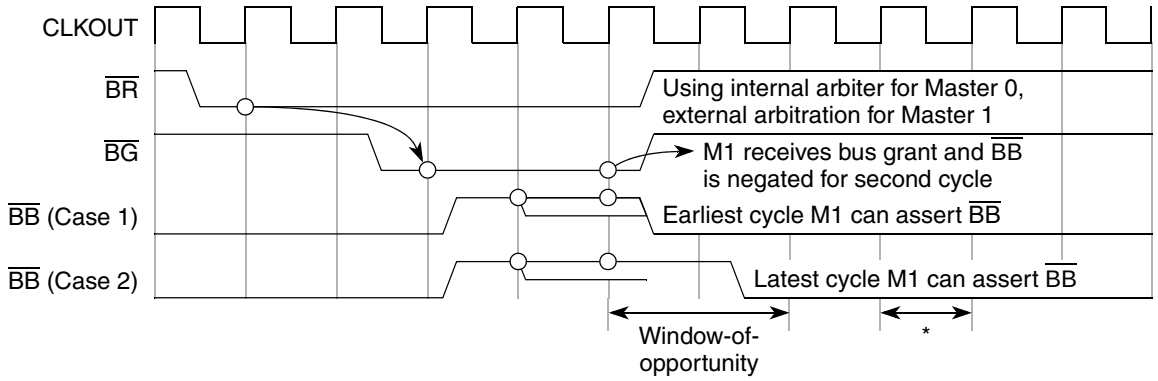
When an MCU is configured to use the internal bus arbiter, that MCU is parked on the bus. The parking feature allows the MCU to skip the bus request phase, and if BB is negated, assert BB, and initiate the transaction without waiting for bus grant from the arbiter. The priority between internal and external masters over the external bus is determined by the EARP field of the EBI_MCR. See Table 12-7 for the EARP field description.

By default, internal and external masters are treated with equal priority, with each having to relinquish the bus after the current transaction if another master is requesting it. If internal and external requests for the bus occur in the same cycle, the internal arbiter grants the bus to the master who least recently used the bus. If no other master is requesting the bus, the bus continues to be granted to the current master, and the current master start another access without re-arbitrating for the bus.

If the priority field is configured for unequal priority between internal and external masters, then whenever requests are pending from both masters, the one with higher priority is always granted the bus. However, in all cases, a transaction in progress (or that has already been granted, for example MCU bus wait and external bus wait states) is allowed to complete, even when a request from a higher priority master is pending.

There is a minimum of one cycle between the positive edge CLKOUT that a BR assertion is sampled by the EBI and the positive edge CLKOUT where BG is driven out asserted by the EBI. This is to prevent timing problems that can limit the operating frequency in external master mode.

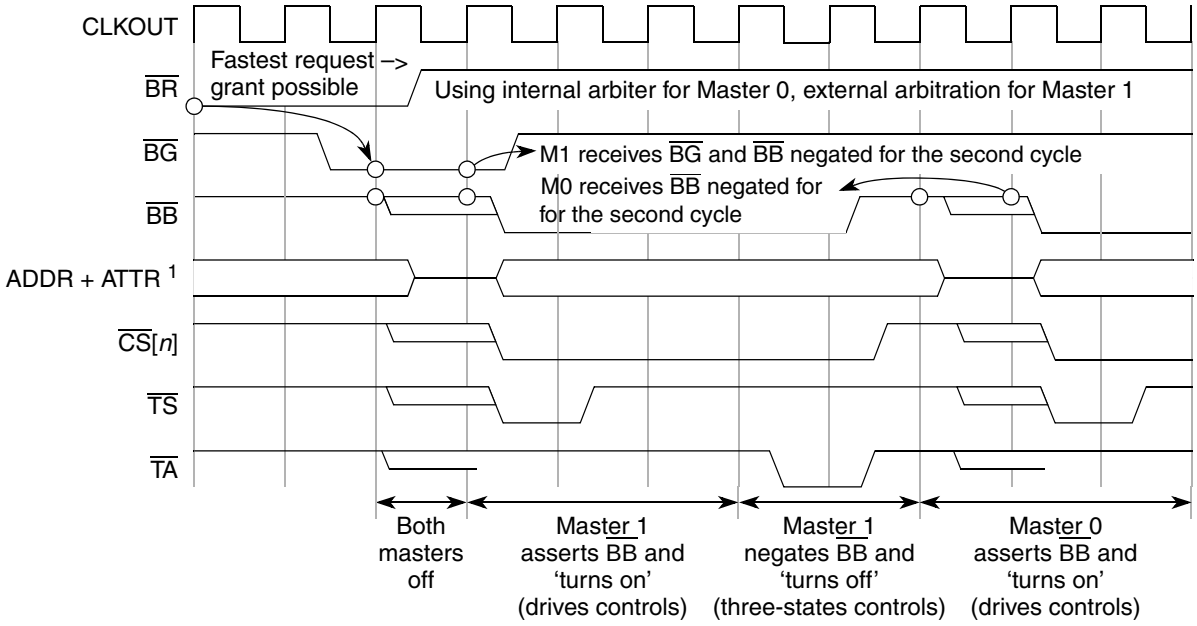
The external master is given two cycles to start its access after a posed CLKOUT in which bus grant was given to it by the internal arbiter ($\overline{BG}$ asserted, $\overline{BB}$ negated for 2 cycles). This means when $\overline{BG}$ is negated (to take away bus grant from the external master), the EBI does not start an access of its own for three cycles (one extra cycle in order to detect external $\overline{BB}$ assertion). If the external master jumps on the bus (by asserting $\overline{BB}$) during the two-cycle window, the EBI detects the $\overline{BB}$ assertion and delays starting its access until the external master access has completed ($\overline{BB}$ negated for two cycles). Figure 12-34 shows this 2-cycle window of opportunity.



* Earliest cycle M0 can assert $\overline{BB}$ if M1 has not asserted $\overline{BB}$ yet.

Figure 12-34. Internal Arbitration, Two-Cycle Window-of-Opportunity

Figure 12-35 shows example timing for the case of one master using internal arbitration (master 0), while another master is configured for external arbitration (master 1). In this case, the $\overline{BR}$ signals of each master are connected together, since only master 1 drives $\overline{BR}$. The $\overline{BG}$ signals of each master are also connected together, since only master 0 drives $\overline{BG}$. See Figure 12-38 for an example of these connections.



1 ATTR refers to control signals such as RD_$\overline{WR}$ and TSIZ.

Figure 12-35. Internal/External Arbitration Timing Diagram (EARP = 1)

Table 12-22 shows a description of the states defined for the internal arbiter protocol.

Table 12-22. Internal Arbiter State Descriptions

State	Description	Outputs
MCU owner idle	MCU controls the bus, but is not currently running a transaction	$\overline{BG}$ = 1, $\overline{BB}$ = hiZ
External owner	External master controls the bus; can be running a transaction or not	$\overline{BG}$ = 0, $\overline{BB}$ = hiZ
MCU bus wait	MCU controls the bus for the next transaction Waiting for the external master to negate $\overline{BB}$ for the current transaction in progress	$\overline{BG}$ = 1, $\overline{BB}$ = hiZ
MCU owner busy	MCU controls the bus Currently running a transaction	$\overline{BG}$ = 1, $\overline{BB}$ = 0 or 1
External bus wait	External master controls the bus for next transaction Waiting for MCU to negate $\overline{BB}$ for the current transaction in progress	$\overline{BG}$ = 0, $\overline{BB}$ = 0 or 1

Table 12-23 shows the truth table for the internal arbiter protocol.

Table 12-23. Truth Table for Internal Arbiter

State	Outputs		Previous Inputs			External Status			Next State
	$\overline{BG}$	$\overline{BB}$ [1]	BR [2]	$\overline{BB}$ [3]	MCU internal request pending (IRP) [4]	External has higher priority (EHP) [5]	MCU external transaction in progress (or starting next cycle) (ETP) [6]	Recent $\overline{BG}$ (RBG) [7]	
MCU owner idle	1	hiZ	1	X	0	0	0	X [8]	MCU owner idle
MCU owner idle	1	hiZ	X	X	0	1	0	X [9]	External owner
MCU owner idle	1	hiZ	0	X	0	X	0	X	External owner
MCU owner idle	1	hiZ	0	X	X	1	0	X	External owner
MCU owner idle	1	hiZ	X	X	1	0	X	X	MCU owner busy
MCU owner idle	1	hiZ	1	X	1	X	X	X	MCU owner busy
MCU owner idle	1	hiZ	X	X	X	X	1	X	MCU owner busy
External owner	0	hiZ	X	X	0	X	X [10]	X [11]	External owner
External owner	0	hiZ	0	X	X	1	X	X	External owner
External owner	0	hiZ	X	X	1	0	X	X	MCU bus wait
External owner	0	hiZ	1	X	1	X	X	X	MCU bus wait
MCU bus wait	1	hiZ	X	0	X [12]	X	X [10]	X	MCU bus wait
MCU bus wait	1	hiZ	X	X	X	X	X	1	MCU bus wait
MCU bus wait	1	hiZ	X	1	X	X	X	0	MCU owner busy
MCU owner busy	1	0 or 1 [13]	1	X	X	X	1	X [8]	MCU owner busy
MCU owner busy	1	0 or 1	1	X	1	X	X	X	MCU owner busy
MCU owner busy	1	0 or 1	X	X	1	0	X	X	MCU owner busy
MCU owner busy	1	0 or 1	0	X	X	1	1	X	External bus wait

Table 12-23. Truth Table for Internal Arbiter (continued)

State	Outputs		Previous Inputs			External Status			Next State
	$\overline{BG}$	$\overline{BB}$ [1]	BR [2]	$\overline{BB}$ [3]	MCU internal request pending (IRP) [4]	External has higher priority (EHP) [5]	MCU external transaction in progress (or starting next cycle) (ETP) [6]	Recent $\overline{BG}$ (RBG) [7]	
MCU owner busy	1	0 or 1	0	X	0	X	1	X	External bus wait
MCU owner busy	1	0 or 1	0	X	X	1	0	X	External owner
MCU owner busy	1	0 or 1	0	X	0	X	0	X	External owner
MCU owner busy	1	0 or 1	1	X	0	X	0	X	MCU owner idle
External bus wait	0	0 or 1 [13]	X [14]	X	X	X	1	X [8]	External bus wait
External bus wait	0	0 or 1	X	X	X	X	0	X	External owner

[1] The Output column for $\overline{BB}$ shows the value EBI drives on $\overline{BB}$ for each state.

[2] The Input column for $\overline{BR}$ shows the value driven on $\overline{BR}$ the previous cycle from an external source. The state machine uses the previous clock value to avoid potential speed paths with trying to calculate bus grant based on a late-arriving external $\overline{BR}$ signal.

[3] The Input column for $\overline{BB}$ shows the value driven on $\overline{BB}$ the previous cycle from an external source. The state machine uses the previous clock value to ensure adequate switching time between masters driving the same signal and to avoid potential speed paths.

[4] This represents an internal EBI signal that indicates whether an internal request for use of the external bus is pending. Once a transaction for a pending request has been started on the external bus, this internal signal is cleared. The state machine uses the previous clock value to avoid potential speed paths with trying to calculate bus grant based on a late-arriving internal request signal.

[5] This represents an internal EBI signal that indicates whether the internal MCU (0) or external master (1) currently has higher priority.

[6] This represents an internal EBI signal that indicates whether an EBI-mastered transaction on the bus is in progress this cycle or is going to start the next cycle (and thus has already been committed internally).

[7] This represents an internal EBI signal that indicates whether the bus was granted to an external master ($\overline{BG}$ = 0, previous $\overline{BB}$ = 1) during the previous 3 cycles.

[8] RGB is always low in this state, thus it is ignored in the transition logic.

[9] RGB is always low in this state, thus it is ignored in the transition logic.

[10] The ETP signal is never asserted in states where it is shown as an ‘X’ for all transitions.

[11] RGB is always high in this state, thus it is ignored in the transition logic.

[12] IRP is ignored (treated as 1) in the MCU_WAIT state because the EBI does not optimally support an internal master cancelling its bus request. If IRP is negated in this state, the EBI still grants the internal master the bus as if IRP was still asserted, and a few cycles be wasted before the external master be able to grab the bus again (depending on $\overline{BR}$, $\overline{BB}$, etc., according to normal transition logic).

[13] The default $\overline{BB}$ output is 0 for this state. However, anytime the EBI transitions from a state where $\overline{BB}$ = 0 to a state where $\overline{BB}$ = hiZ, there is one external cycle (in this state) where the EBI drives $\overline{BB}$ = 1 to actively negate the pin before letting go to hiZ. In the case where a second granted internal request (IRP = 1, ETP=1) is ready to start just before the transition to the hiZ state is about to occur (during the $\overline{BB}$ = 1active negate cycle), then $\overline{BB}$ is driven back to 0 to start the next access without ever leaving this state or going to hiZ.

[14] $\overline{BR}$ is ignored (treated as 0) in the EXT_WAIT state because the EBI does not optimally support an external master cancelling its bus request. If $\overline{BR}$ is negated in this state, the EBI still grants the external master the bus as if $\overline{BR}$ was still asserted, and a few cycles be wasted while the external master ‘window-of-opportunity’ is satisfied before the internal master be able to grab the bus again (depending on $\overline{BR}$, $\overline{BB}$, etc., according to normal transition logic).

Figure 12-36 shows the internal finite state machine that implements the arbiter protocol.

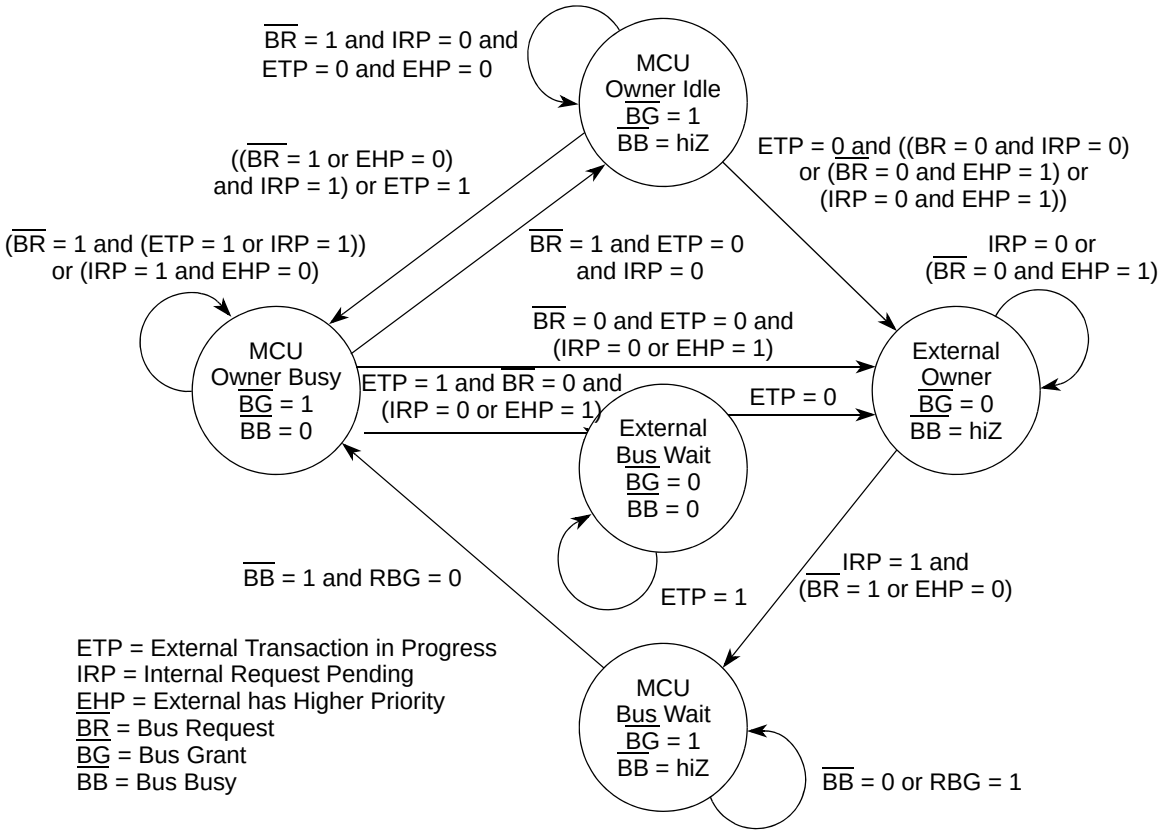


Figure 12-36. Internal Bus Arbitration State Machine

12.4.2.9 Termination Signals Protocol

The termination signals protocol was defined to avoid electrical contention on lines that can be driven by various sources. To do that, a slave must not drive signals associated with the data transfer until the address phase is completed and it recognizes the address as its own. The slave must disconnect from signals immediately after it acknowledges the cycle and not later than the termination of the next address phase cycle.

For EBI-mastered non-chip select accesses, the EBI requires assertion of TA from an external device to signal that the bus cycle is complete. The EBI uses a latched version of TA (delayed one cycle) for these accesses to help make timing at high frequencies. This results in the EBI driving the address and control signals one cycle longer than required, as seen in Figure 12-37. However, the DATA does not need to be held one cycle longer by the slave, because the EBI latches DATA every cycle during non-chip select accesses. During these accesses, the EBI does not drive the TA signal, leaving it up to an external device (or weak internal pullup) to drive TA.

For EBI-mastered chip select accesses, the EBI drives TA the entire cycle, asserting according to internal wait state counters to terminate the cycle. During idle periods on the external bus, the EBI drives TA negated as long as it is granted the bus; when it no longer owns the bus it lets go of TA. When an external

master does a transaction to internal address space, the EBI only drives $\overline{TA}$ for the cycle it asserts $\overline{TA}$ to return data and for one cycle afterwards to ensure fast negation.

If no device responds by asserting $\overline{TA}$ within the programmed timeout period (BMT in EBI_BMCR) after the EBI initiates the bus cycle, the internal bus monitor (if enabled) asserts $\overline{TEA}$ to terminate the cycle. An external device also drive $\overline{TEA}$ when it detects an error on an external transaction. $\overline{TEA}$ assertion causes the cycle to terminate and the processor to enter exception processing for the error condition. To properly control termination of a bus cycle for a bus error with external circuitry, $\overline{TEA}$ must be asserted at the same time or before (external) $\overline{TA}$ is asserted. $\overline{TEA}$ must be negated before the second rising edge after it was sampled asserted to avoid the detection of an error for the following bus cycle initiated. $\overline{TEA}$ is only driven by the EBI during the cycle where the EBI is asserting $\overline{TEA}$ and the cycle immediately following this assertion (for fast negation). During all other cycles, the EBI relies on a weak internal pullup to hold $\overline{TEA}$ negated. This allows an external device to assert $\overline{TEA}$ when it needs to indicate an error. External devices must follow the same protocol as the EBI, only driving $\overline{TEA}$ during the assertion cycle and one cycle afterwards for negation.

NOTE

When an external master asserts $\overline{TEA}$ to timeout a transaction to an internal address on the MCU, the EBI cannot terminate the transfer internally. Therefore, subsequent $\overline{TS}$ assertions by the external master are not serviced by the EBI until the original transfer is complete internally and the EBI returns to an idle state. The internal slaves must respond with either valid data or an error indication within a reasonable period of time to avoid hanging the system.

When $\overline{TEA}$ is asserted from an external source, the EBI uses a latched version of $\overline{TEA}$ (one cycle delayed) to help make timing at high frequencies. This means that for any accesses where the EBI drives $\overline{TA}$ (chip select accesses and external master accesses to EBI), a $\overline{TEA}$ assertion that occurs one cycle before or during the last $\overline{TA}$ of the access is not needed by the EBI, since it completes the access internally before it detects the latched $\overline{TEA}$ assertion. This means that non-burst chip select accesses with no wait states (SCY equal to zero) cannot be reliably terminated by external $\overline{TEA}$. If external error termination is required for such a device, the EBI must configure SCY greater than or equal to one.

NOTE

In some access cases that use a chip select and internally-driven $\overline{TA}$, a $\overline{TEA}$ that occurs one cycle before or during the $\overline{TA}$ cycle, or when SCY equals zero, the cycle can terminate with an incorrect error. Because correct error termination is not guaranteed, always assert $\overline{TEA}$ at least two cycles before an internally-driven $\overline{TA}$ cycle for the error to terminate correctly.

External $\overline{TEA}$ assertion that occurs during the same cycle that $\overline{TS}$ is asserted by the EBI is always treated as an error (terminating the access) regardless of SCY.

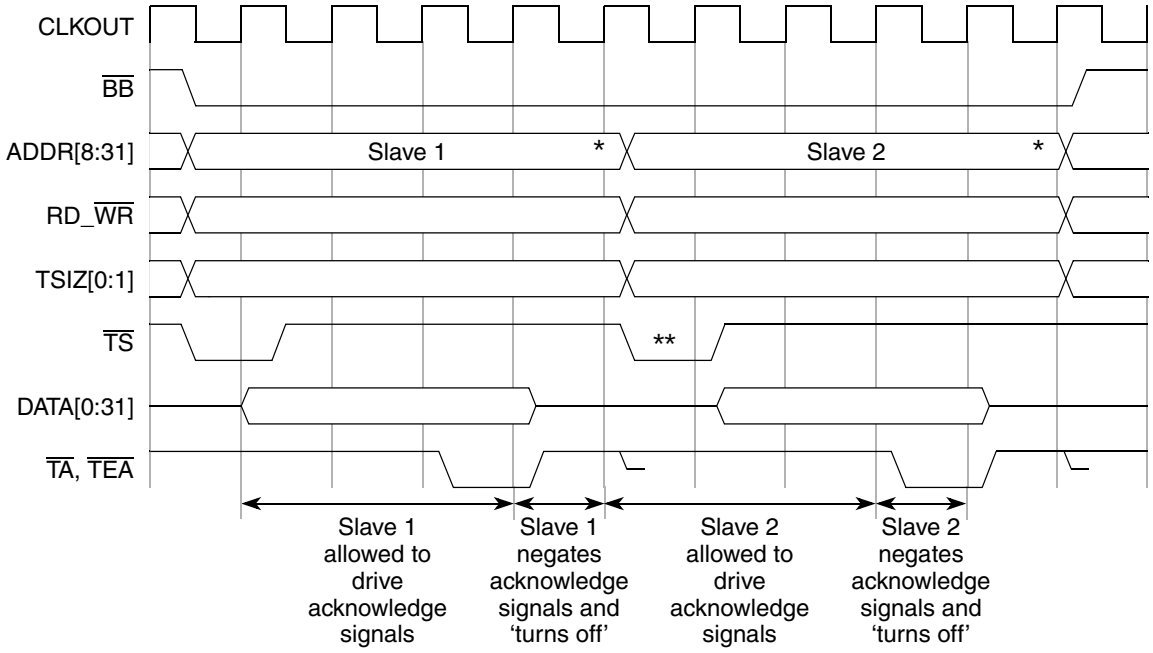
Table 12-24 summarizes how the EBI recognizes the termination signals provided from an external device.

Table 12-24. Termination Signals Protocol

$\overline{\text{TEA}}$ [1]	$\overline{\text{TA}}$ [1]	Action
Negated	Negated	No termination
Asserted	–	Transfer error termination
Negated	Asserted	Normal transfer termination

[1] Latched version (delayed one cycle) is used for the externally driven $\overline{\text{TEA}}$ and $\overline{\text{TA}}$.

Figure 12-37 shows an example of the termination signals protocol for back-to-back reads to two different slave devices who properly take turns driving the termination signals. This assumes a system using slave devices that drive termination signals.



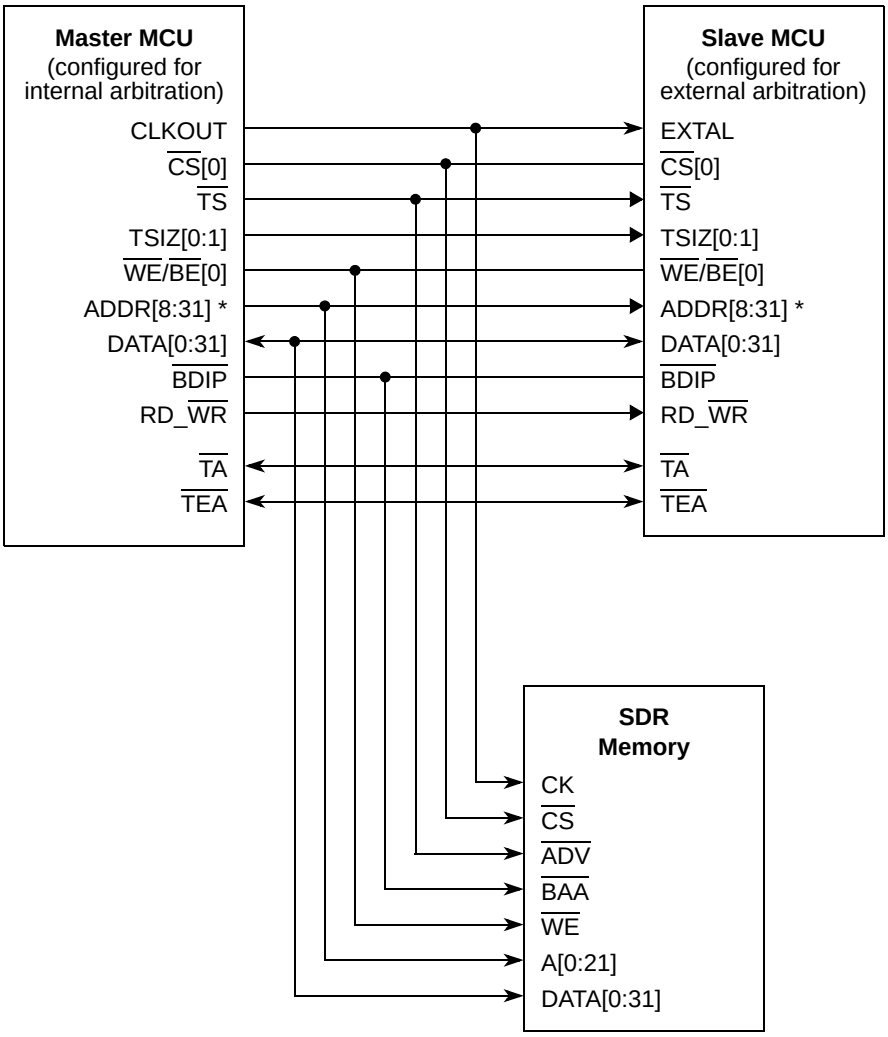
* The EBI drives address and control signals an extra cycle because it uses a latched version of $\overline{\text{TA}}$ (1 cycle delayed) to terminate the cycle. An external master is not required to do this.

** This is the earliest that the EBI can start another transfer, in the case of continuing a set of small accesses. For all other cases, an extra cycle is needed before the EBI can start another $\overline{\text{TS}}$.

Figure 12-37. Termination Signals Protocol Timing Diagram

12.4.2.10 Bus Operation in External Master Mode

External master mode enables an external master to access the internal address space of the MCU. Figure 12-38 shows how to connect an MCU to an external master (a second MCU) and a shared SDR memory to operate in external master mode. Full multi-master support is available.



* Only ADDR[8:29] are connected to the 32-bit SDR memory.

Figure 12-38. MCU Connected to External Master and SDR Memory

When the external master requires external bus accesses, it takes ownership on the external bus, and the direction of most of the bus signals is inverted, relative to its direction when the MCU owns the bus.

To operate two masters in external master mode, one must be configured for internal arbitration and the other must be configured for external arbitration. Connecting three or more masters together in the same system is not supported by this EBI.

Most of the bidirectional signals shown in Figure 12-38 are only driven by the EBI when the EBI owns the external bus. The only exceptions are the $\overline{TA}$ and $\overline{TEA}$ signals (described in Section 12.4.2.9, "Termination Signals Protocol") and the DATA bus, which are driven by the EBI for external master reads to internal address space. As long as the external master device follows the same protocol for driving signals as this EBI, there is no need to use the open drain mode of the pads configuration module for any EBI pins.

The Power Architecture storage reservation protocol is not supported by the EBI. Coherency between multiple masters must be maintained via software techniques, such as event passing.

The EBI does not provide memory controller services to an external master that accesses shared external memories. Each master must properly configure its own memory controller and drive its own chip selects when sharing a memory between two masters.

The EBI does not support burst accesses from an external master; only single accesses of 8, 16, or 32 bits can be performed.[1]

12.4.2.10.1 Address Decoding for External Master Accesses

The EBI allows external masters to access internal address space when the EBI is configured for external master mode. The external address is compared for any external master access, to determine if EBI operation is required. Because only 24 address bits are available on the external bus, decoding logic is required to allow an external master to access on-chip locations that have non-zero values in the upper eight address bits. This is done by using the upper 4 external address bits (ADDR[8:11]) as a code to determine whether the access is on-chip and if so, for which internal slave it is targeted.

NOTE

Even though the address bus has 26 bits available, only 24 bits are used for external master accesses. External master accesses are not supported to the Calibration bus.

The options for the address compare sequence are explained in the following bullets:

- External master access to another device — If ADDR[8] = 0, then the access is assumed to be to another device and is ignored by the EBI.
- External master access to valid internal slave — If ADDR[8] = 1, then ADDR[9:11] are checked versus a list of 3-bit codes to determine which internal slave to forward the access to. The upper eight internal address bits are set appropriately by the EBI according to this 3-bit code, and internal address bits [8:11] are set appropriately to match the internal slave selected.
- External master access to invalid internal slave — If the 3-bit code does not match a valid internal slave, then the EBI responds with a bus error.

1. Except for the special case of a 32-bit non-chip select access in 16-bit data bus mode. See Section 12.4.2.11, "Non-Chip-Select Burst in 16-bit Data Bus Mode".

Table 12-25 shows the 3-bit values that indicate slaves in the MCU, as well as the resulting upper 12 address bits required to appropriately match up with the memory map of each internal slave.

Table 12-25. EBI Internal Slave Address Decoding

Internal Slave	External ADDR[8:11] [1]	Internal Addr[0:7] [2]	Internal Addr[8:11] [3]
(off-chip)	0b0xxx	—	—
Internal flash	0b10xx	0b0000_0000	0b00, ADDR[10:11]
Internal SRAM	0b1100	0b0100_0000	0b0000
Reserved	0b1101	0b0110_0000	0b0000
Bridge A peripherals	0b1110	0b1100_0011	0b1111
Bridge B peripherals	0b1111	0b1111_1111	0b1111

1 Value on upper 4 bits of 24-bit external address bus ADDR[8:31]. ADDR[8] determines whether the access is on or off chip.

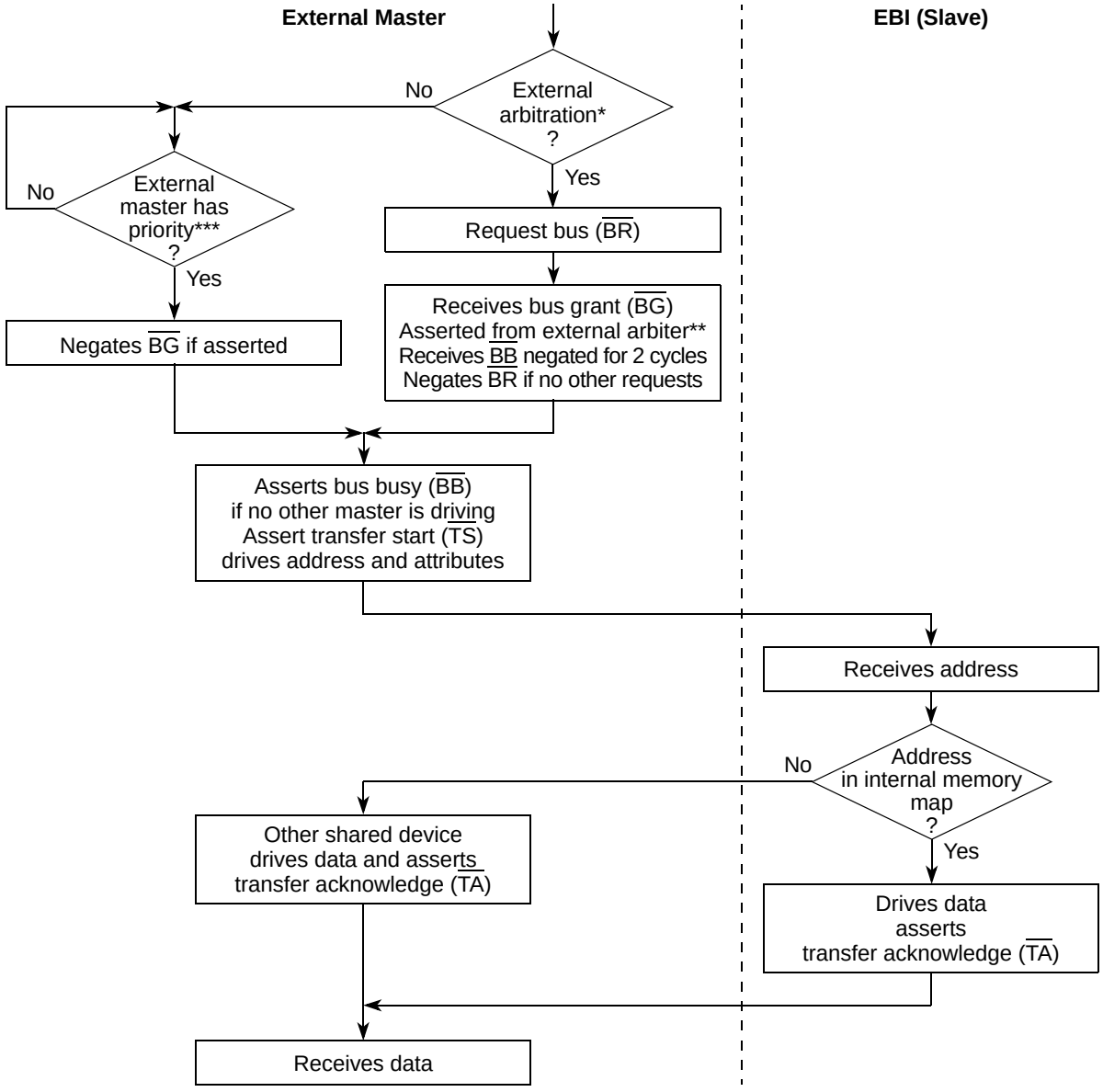
2 Value on upper 8 bits of 32-bit internal address bus.

3 Value on bits 8:11 of 32-bit internal address bus.

12.4.2.10.2 Bus Transfers Initiated by an External Master

The external master gets ownership of the bus (see Section 12.4.2.8, “Arbitration”) and asserts $\overline{\text{TS}}$ to initiate an external master access. The access is directed to the internal bus only if the input address matches to the internal address space. The access is terminated with either $\overline{\text{TA}}$ or $\overline{\text{TEA}}$. If the access was successfully completed, the MCU asserts $\overline{\text{TA}}$, and the external master can proceed with another external master access, or relinquish the bus. If an address or data error was detected internally, the MCU asserts $\overline{\text{TEA}}$ for one clock.

Figure 12-39 and Figure 12-40 illustrate the basic flow of read and write external master accesses.

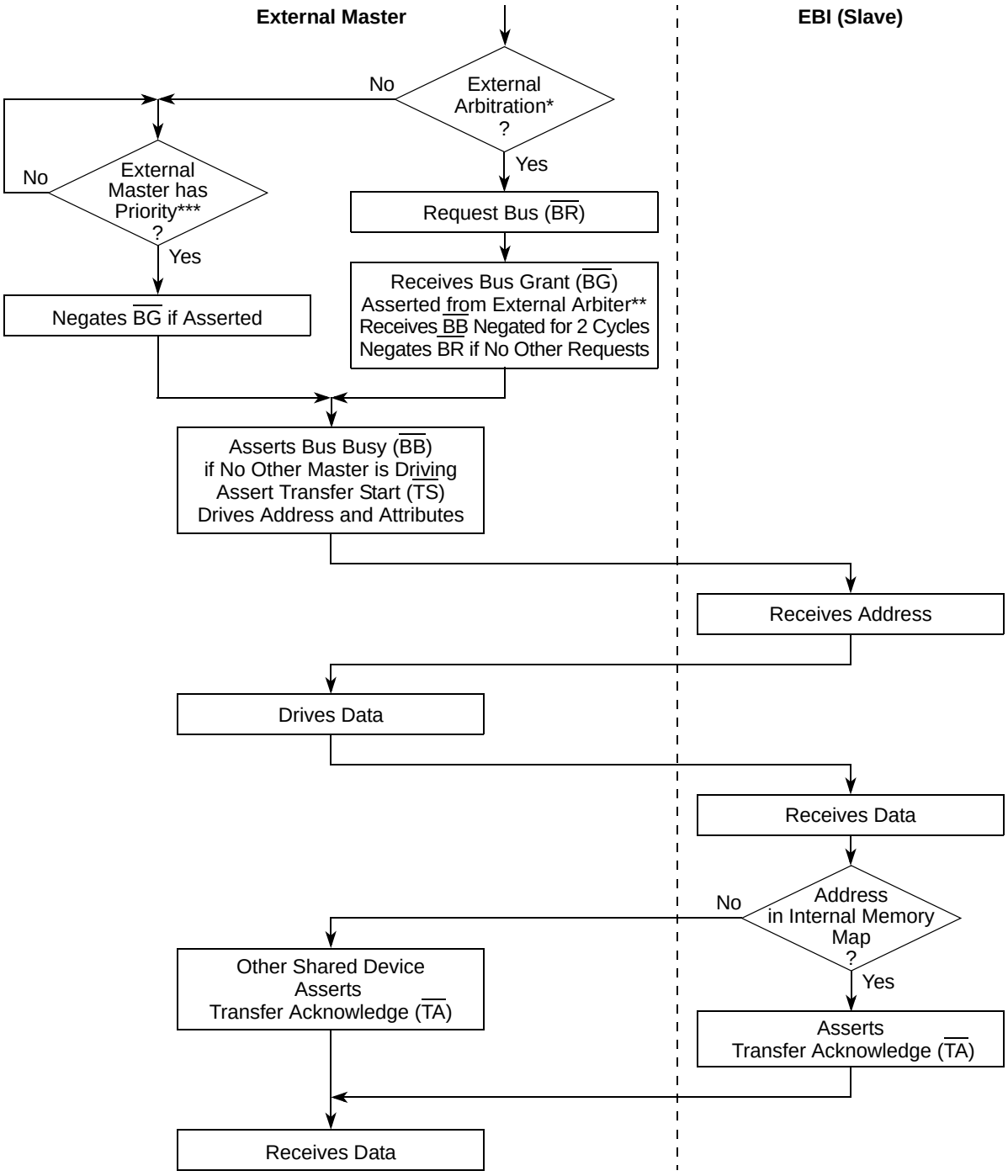


* This refers to whether the external master device is configured for external or internal arbitration.

** External arbiter is the EBI unless a central arbiter device is used.

*** Determined by the internal arbiter of the external master device.

Figure 12-39. Basic Flow Diagram of an External Master Read Access



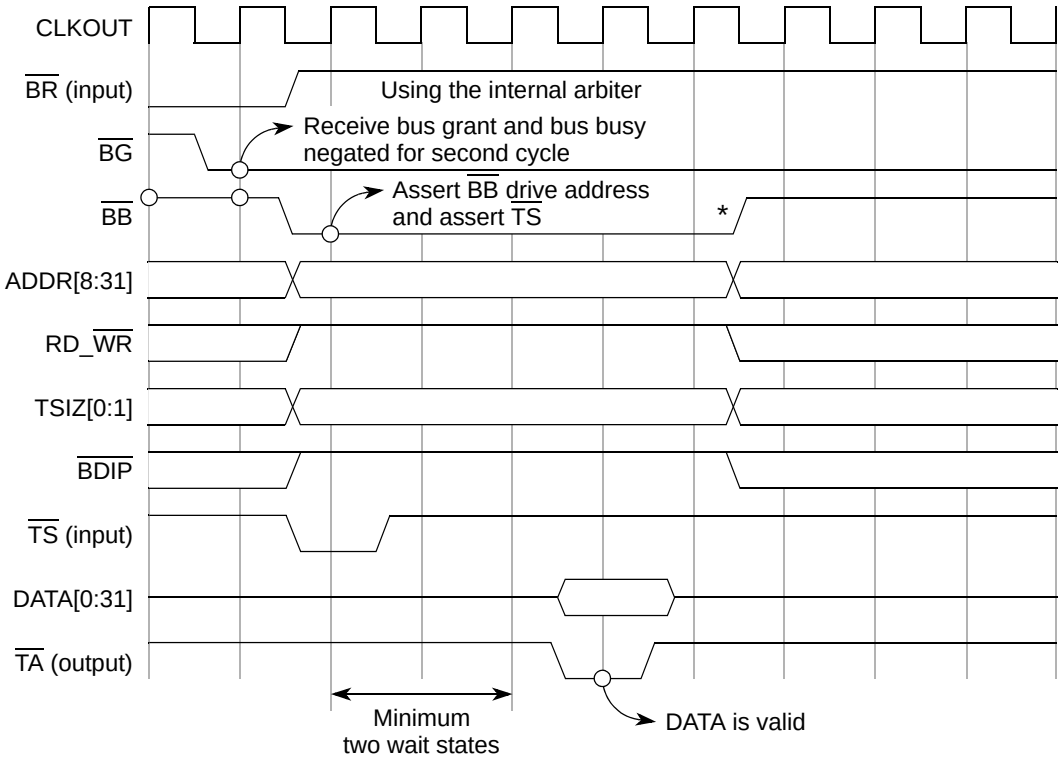
* This refers to whether the external master device is configured for external or internal arbitration.

** External arbiter is the EBI unless a central arbiter device is used.

*** Determined by the internal arbiter of the external master device.

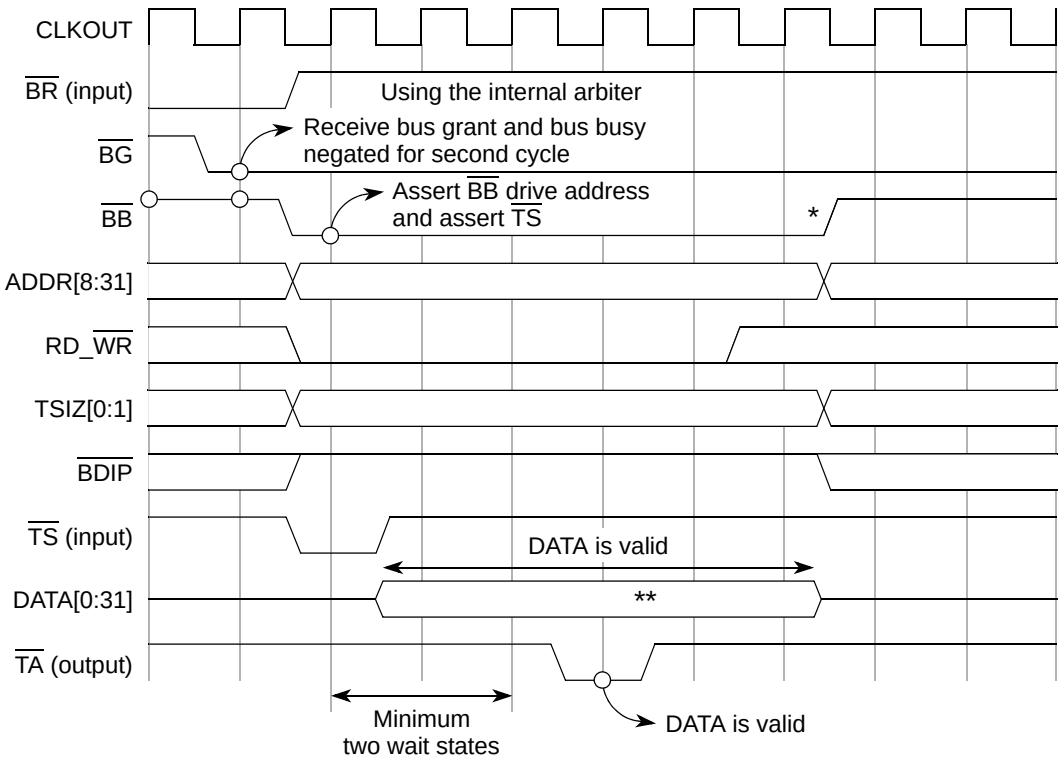
Figure 12-40. Basic Flow Diagram of an External Master Write Cycle

Figure 12-41 and Figure 12-42 describe read and write cycles from an external master accessing internal space in the MCU. The minimal latency for an external master access is three clock cycles. The actual latency of an external to internal cycle varies depending on which internal module is being accessed and how much internal bus traffic is going on at the time of the access.



* If the external master is another MCU with this EBI, then BB and other control pins are turned off as shown due to use of latched TA internally. This extra cycle is not required by the slave EBI.

Figure 12-41. External Master Read from MCU



* If the external master is another MCU with this EBI, then BB and other control pins are turned off as shown due to use of latched TA internally. This extra cycle is not required by the slave EBI.

** If the external master is another MCU with this EBI, then DATA remains valid as shown due to use of latched TA internally. These extra data valid cycles (past TA) are not required by the slave EBI.

Figure 12-42. External Master Write to MCU

12.4.2.10.3 Bus Transfers Initiated by the EBI in External Master Mode

The flow and timing for EBI-mastered transactions in external master mode is the same as described for single master mode, except that the EBI arbitrates bus transmissions for each transaction.

The following flow and timing diagrams show the arbitration sequence added to Figure 12-9 and Figure 12-10 for the basic single-beat read operation. The remaining operations (writes, bursts, etc.) add the arbitration sequence to the flow and timing diagrams shown for single-master mode. See Section 12.4.2.4, “Single-Beat Transfer,” and Section 12.4.2.5, “Burst Transfer.”

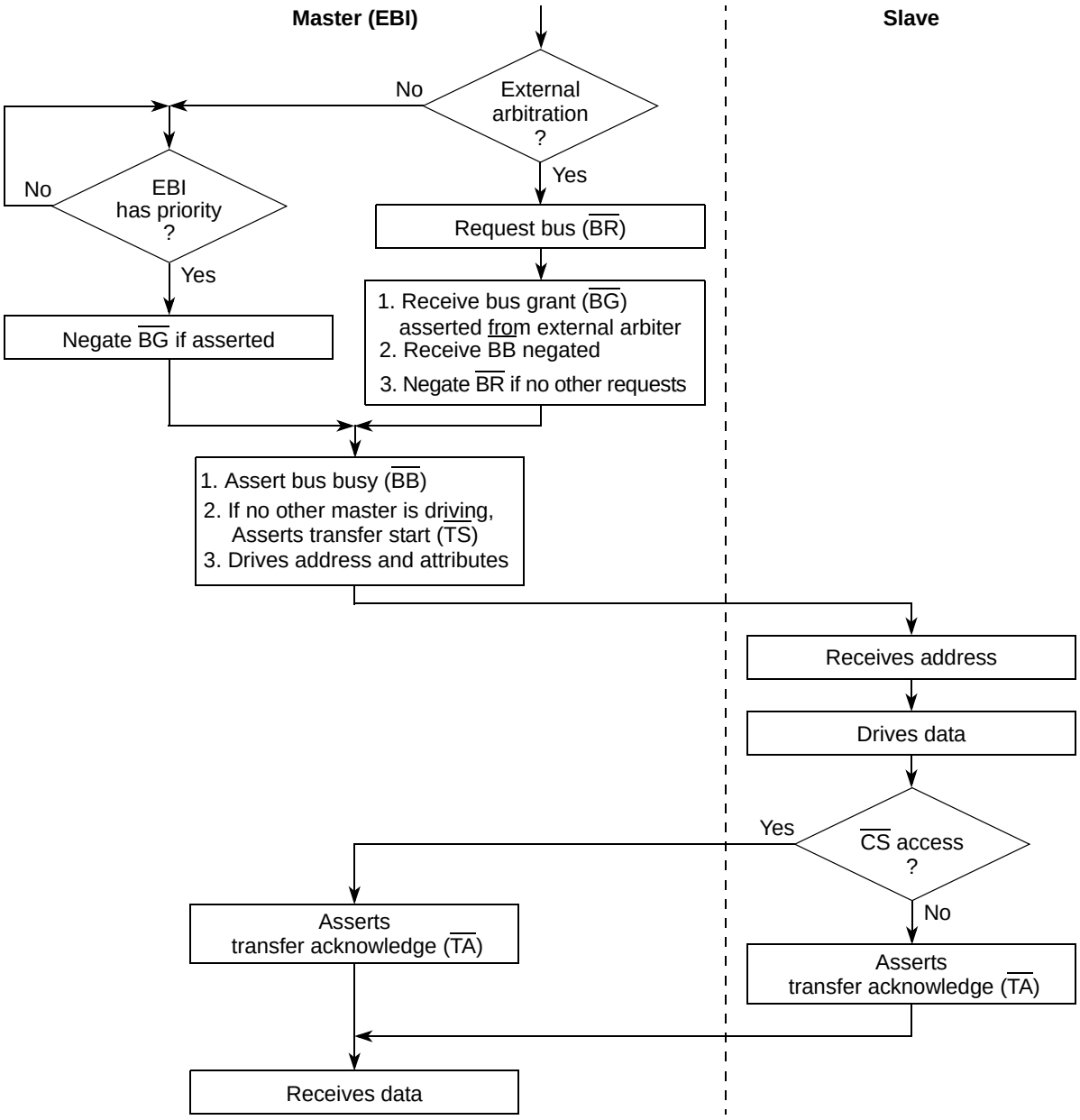


Figure 12-43. Basic Flow Diagram of an EBI Read Access in External Master Mode

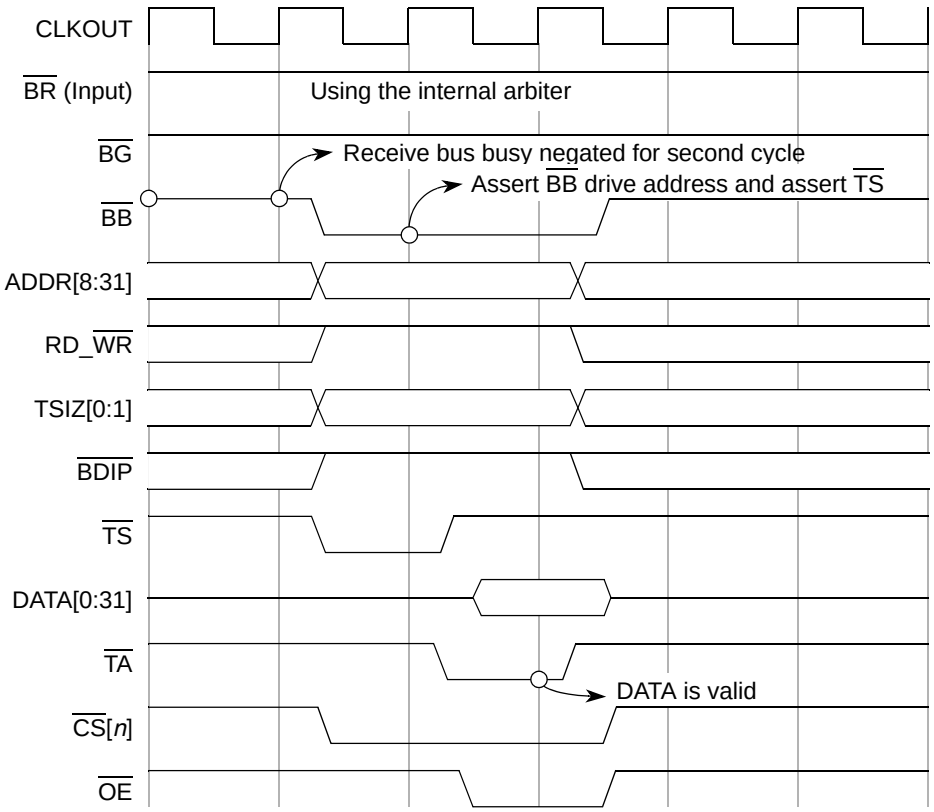


Figure 12-44. Single-Beat CS Read Cycle in External Master Mode, Zero Wait States

12.4.2.10.4 Back-to-Back Transfers in External Master Mode

The following timing diagrams show examples of back-to-back accesses in external master mode. In these examples, the reads and writes shown are to a shared external memory, and the EBI is assumed to be configured for internal arbitration while the external master is configured for external arbitration.

Figure 12-45 shows an external master read followed by an MCU read to the same chip select bank. Figure 12-46 shows an MCU read followed by an external master read to a different chip select bank. Figure 12-47 shows an external master read followed by an external master write to a different chip select bank. This case assumes the MCU has no higher priority internal request pending and is able to park the external master on the bus.

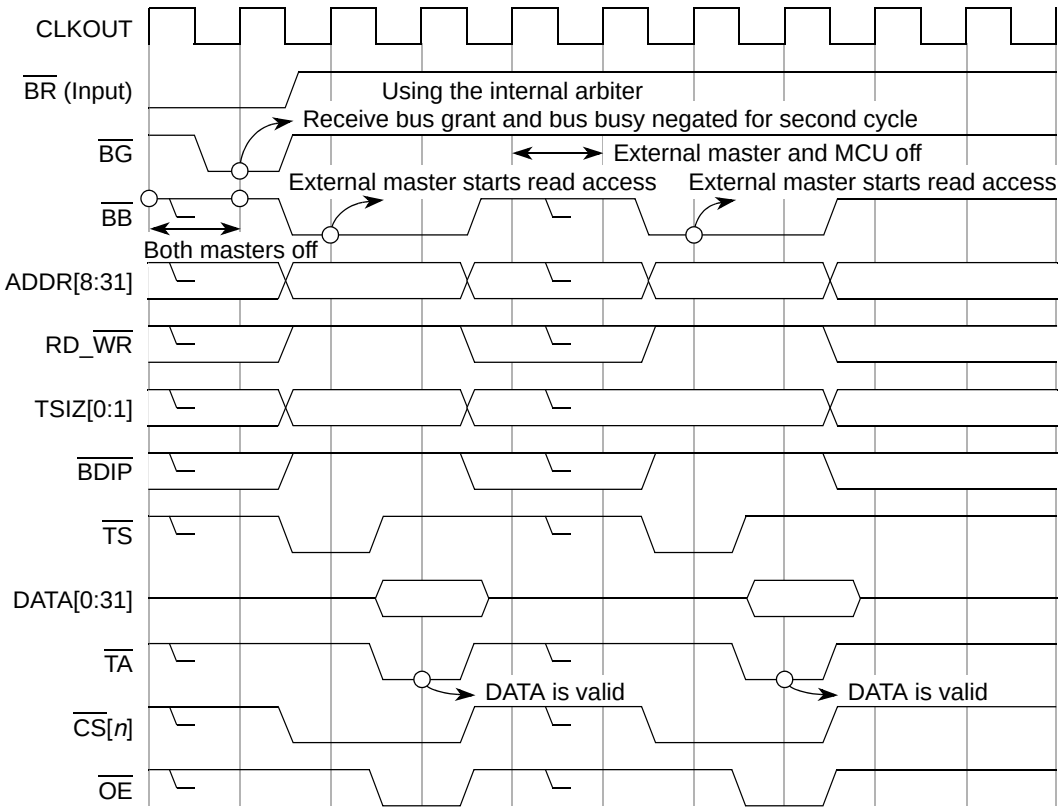


Figure 12-45. External Master Read followed by MCU Read to Same $\overline{CS}$ Bank

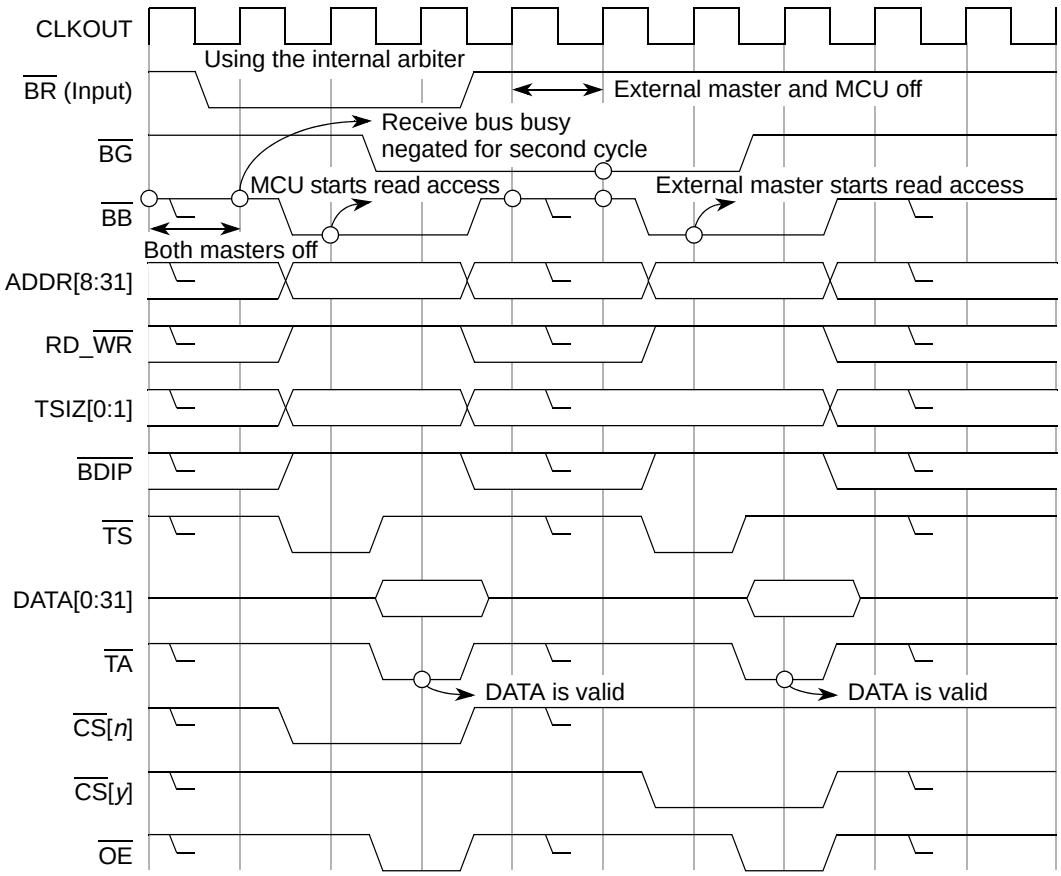


Figure 12-46. MCU Read followed by External Master Read to Different $\overline{CS}$ Bank

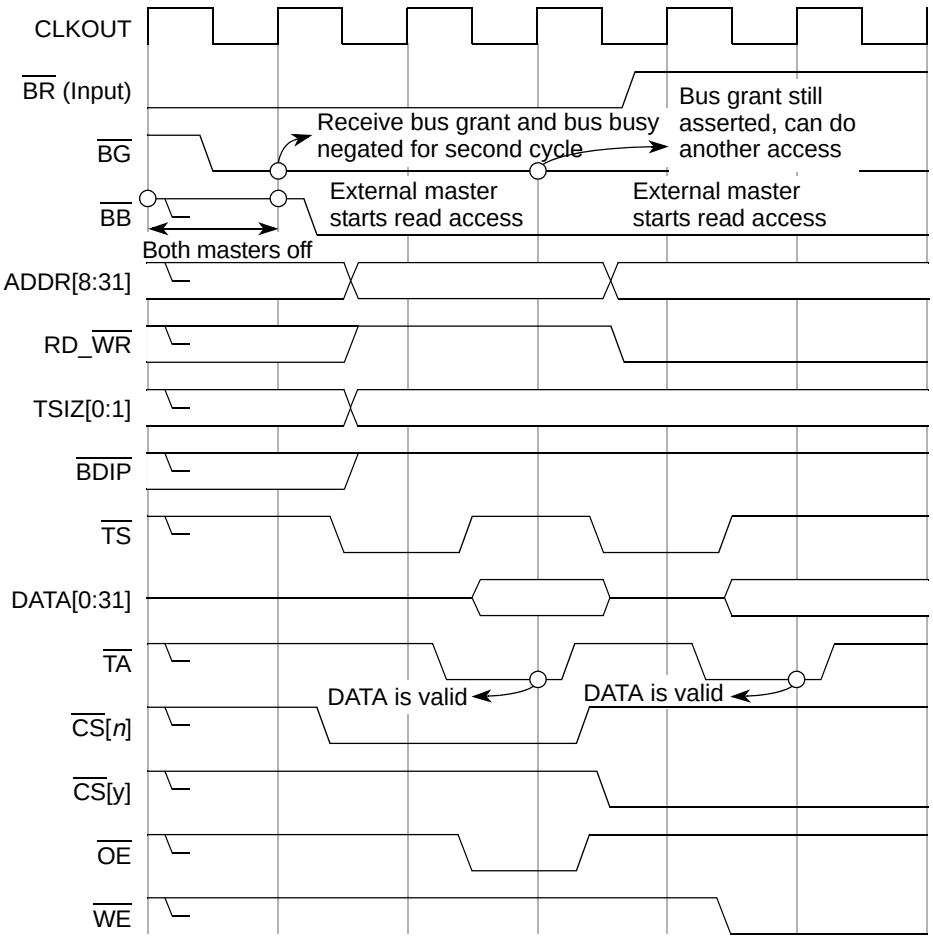


Figure 12-47. External Master Read followed by External Master Write to Different $\overline{CS}$ Bank

12.4.2.11 Non-Chip-Select Burst in 16-bit Data Bus Mode

The timing diagrams in this section apply only to the special case of a non-chip select 32-bit access in 16-bit data bus mode. They specify the behavior for both the EBI-master and EBI-slave, as the external master is expected to be another MCU with this EBI.

For this case, a special two-beat burst protocol is used for reads and writes, so that the EBI-slave can internally generate one 32-bit read or write access (thus 32-bit coherent), as opposed to two separate 16-bit accesses.

Figure 12-48 shows a 32-bit read from an external master in 16-bit data bus mode.

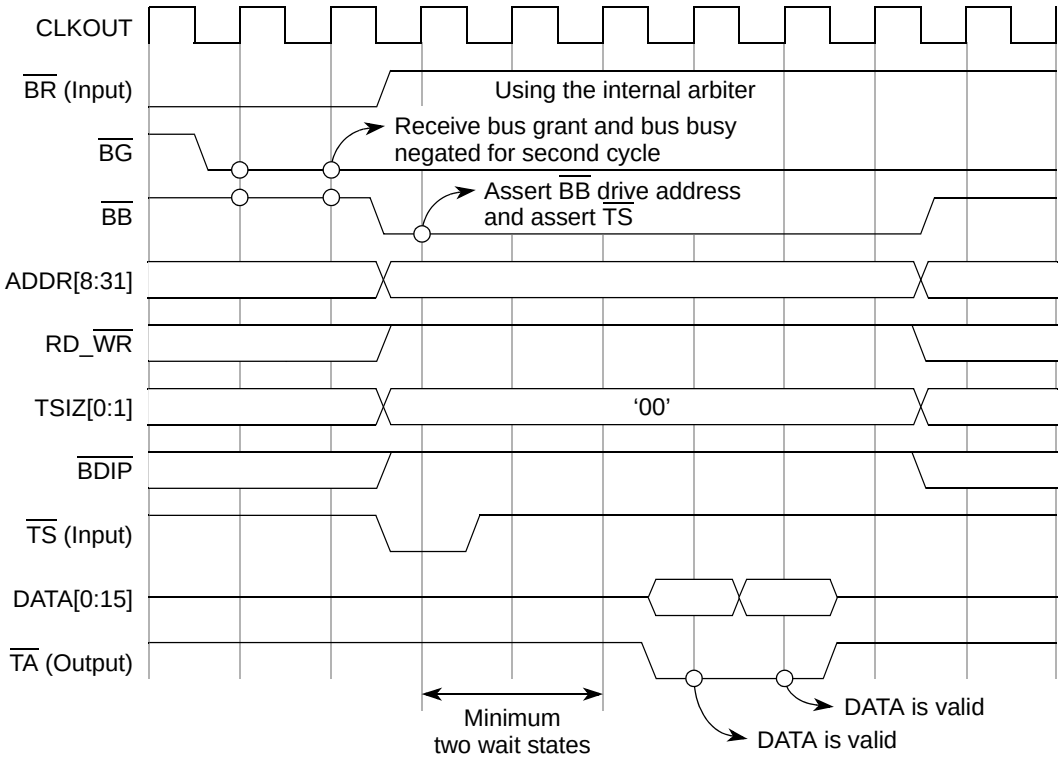


Figure 12-48. External Master 32-bit Read from MCU with DBM = 1

Figure 12-49 shows a 32-bit write from an external master in 16-bit data bus mode.

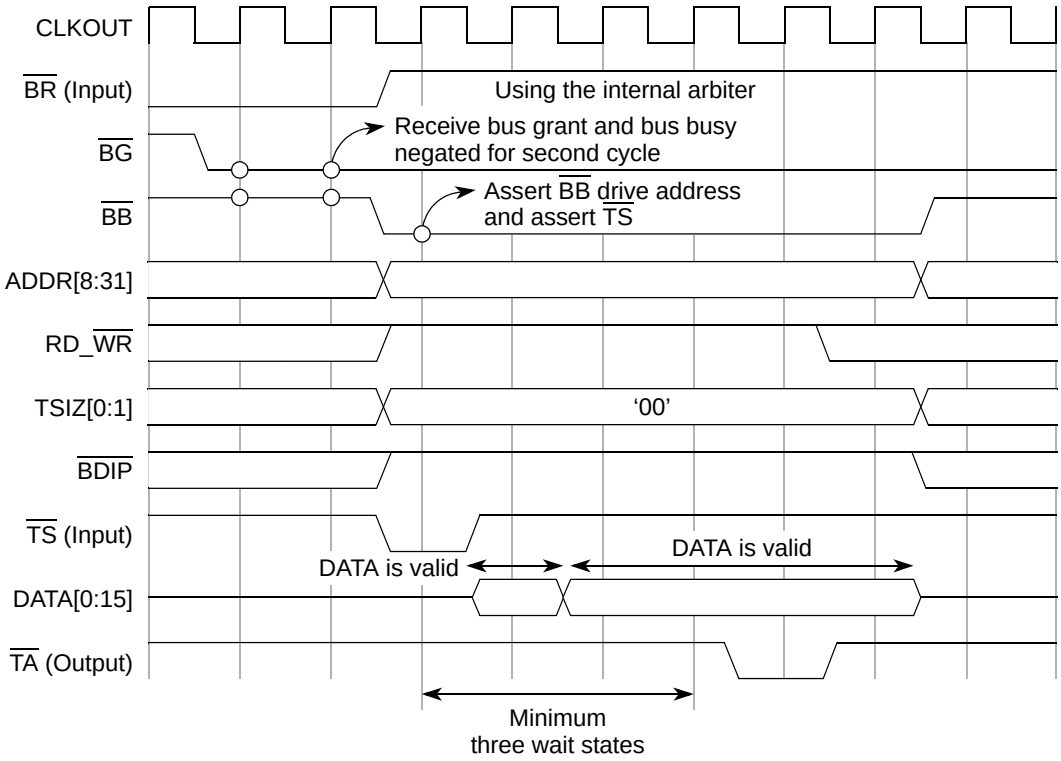


Figure 12-49. External Master 32-bit Write to MCU with DBM = 1

12.4.2.12 Calibration Bus Operation

The EBI has a second external bus, intended for calibration use. This bus consists of a second set of the same signals present on the primary external bus, except that arbitration, (and optionally other signals also) are excluded. Both busses are supported by the EBI by using the calibration chip selects to steer accesses to the calibration bus instead of to the primary external bus.

Because the calibration bus has no arbitration signals, the arbitration on the primary bus controls accesses on the calibration bus as well, and no external master accesses can be performed on the calibration bus. Accesses cannot be performed in parallel on both external busses. However, back-to-back accesses can switch from one bus to the other, as determined by the type of chip select each address matches.

The timing diagrams and protocol for the calibration bus are identical to those for the primary bus, except that some signals are not available on the calibration bus. There is an inherent dead cycle between a calibration chip select access and a non-calibration access (chip select or non-chip select), just like the one between accesses to two different non-calibration chip selects (described in Section 12.4.2.4.3, "Back-to-Back Accesses").

Figure 12-50 shows an example of a non-calibration chip select read access followed by a calibration chip select read access. This figure is identical to Figure 12-18, except the $\overline{CS}[y]$ is replaced by CAL_$\overline{CS}[y]$. Timing for other cases on the calibration bus can similarly be derived from other figures in this document (by replacing $\overline{CS}$ with CAL_$\overline{CS}$).

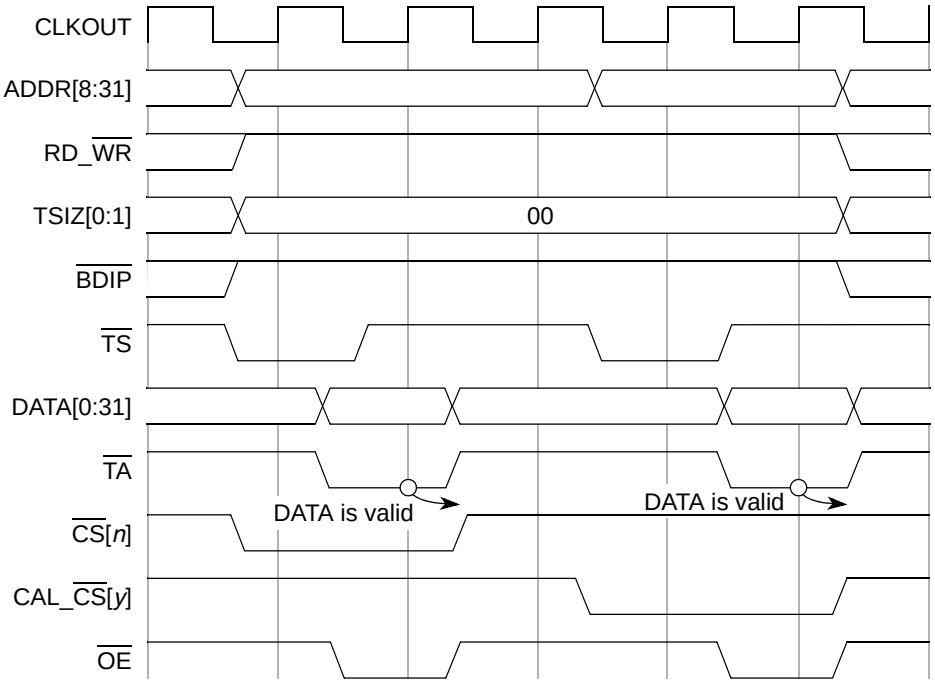


Figure 12-50. Back-to-Back 32-bit Reads to CS, CAL_CS Banks

12.5 Initialization and Application Information

12.5.1 Booting from External Memory

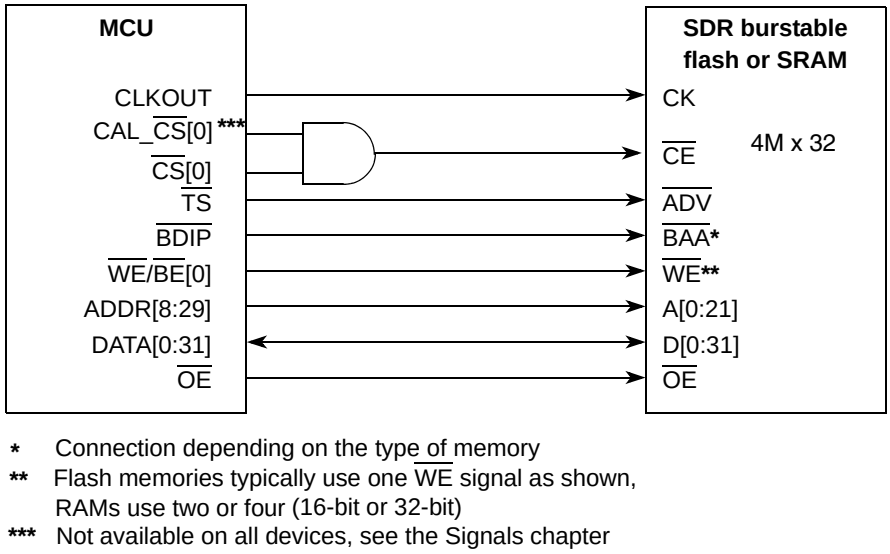
The EBI block does not support booting directly to external memory (i.e. fetching the first instruction after reset externally). The MCU uses an internal boot assist module, which executes after each reset. The BAM code performs basic configuration of the EBI block, allowing for external boot if desired. See 16.1.3, "Modes of Operation," for detail information about the boot modes supported by the MCU; booting is not possible from external memory on the calibration bus.

If code in external memory must write EBI registers, avoid modifying EBI registers while external accesses are in progress by using the following method:

1. Copy to internal SRAM the code that writes to the EBI registers (plus a return branch)
2. Branch to internal SRAM to run the code, ending with a branch back to external flash

12.5.2 Running with SDR (Single Data Rate) Burst Memories

This includes flash and external SRAM memories with a compatible burst interface. BDIP is required only for some SDR memories. Figure 12-48 shows a block diagram of an MCU connected to a 32-bit SDR burst memory.



* Connection depending on the type of memory
** Flash memories typically use one WE signal as shown, RAMs use two or four (16-bit or 32-bit)
*** Not available on all devices, see the Signals chapter

Figure 12-51. MCU Connected to SDR Burst Memory

See Figure 12-23 for an example of the timing of a typical burst read operation to an SDR burst memory. See Figure 12-14 for an example of the timing of a typical single write operation to SDR memory.

12.5.3 Running with Asynchronous Memories

The EBI also supports asynchronous memories. In this case, the CLKOUT, TS, and BDIP pins are not used by the memory and bursting is not supported. However, the EBI still drives these outputs, and always drives and latches all signals at positive edge CLKOUT (i.e., there is no asynchronous mode for the EBI). The data timing is controlled by setting the SCY bits in the appropriate option register to the proper number of wait states to work with the access time of the asynchronous memory, just as done for a synchronous memory.

12.5.3.1 Example Wait State Calculation

This example applies to any chip select memory, synchronous or asynchronous.

As an example, say we have a memory with 50 ns access time, and we are running the external bus at 66 MHz (CLKOUT period: 15.2 ns). When the input data specification for the MCU is 4 ns:

Number of wait states = (access time) ÷ [(CLKOUT period) + (0 or 1; depending on setup time)]

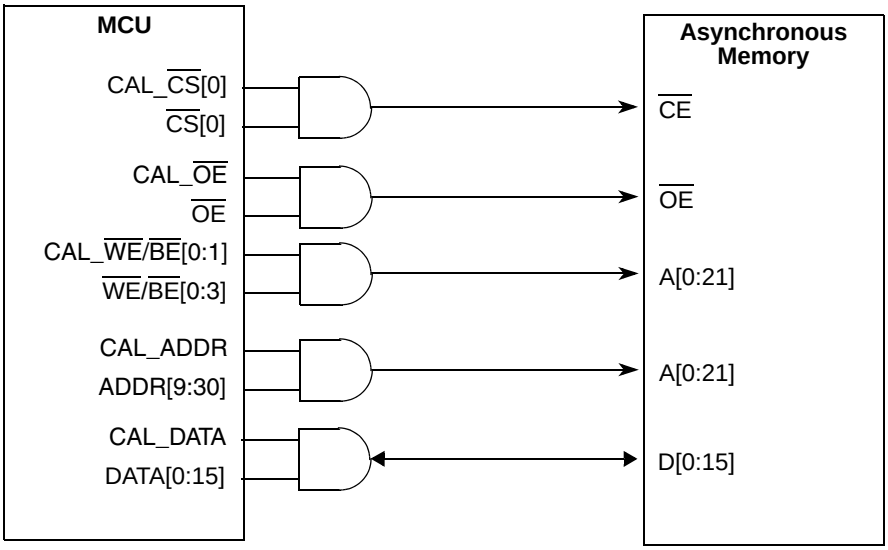
50 ÷ 15.2 = 3 with 4.4 ns remaining (minimum of three wait states)

15.2 – 4.4 = 10.8 ns (achieved input data setup time)

Because actual input setup (10.8 ns) is greater than the input setup specification (4.0 ns), three wait states is sufficient. If the input setup is less than 4.0 ns, use four wait states.

12.5.3.2 Timing and Connections for Asynchronous Memories

The connections to an asynchronous memory are the same as for a synchronous memory, except that the CLKOUT, TS, and BDIP signals are not used. Figure 12-52 shows a block diagram of an MCU connected to an asynchronous memory.



* Flash memories typically use one WE signal as shown.

Note: On a 32-bit bus, RAM memories use all four WE/BE[0:3]. On a 16-bit bus, one RAM memory uses WE/BE[0:1] and the other uses WE/BE[2:3].

Figure 12-52. MCU Connected to Asynchronous Memory

Figure 12-53 shows a timing diagram of a *read* operation to a 16-bit asynchronous memory using three wait states.

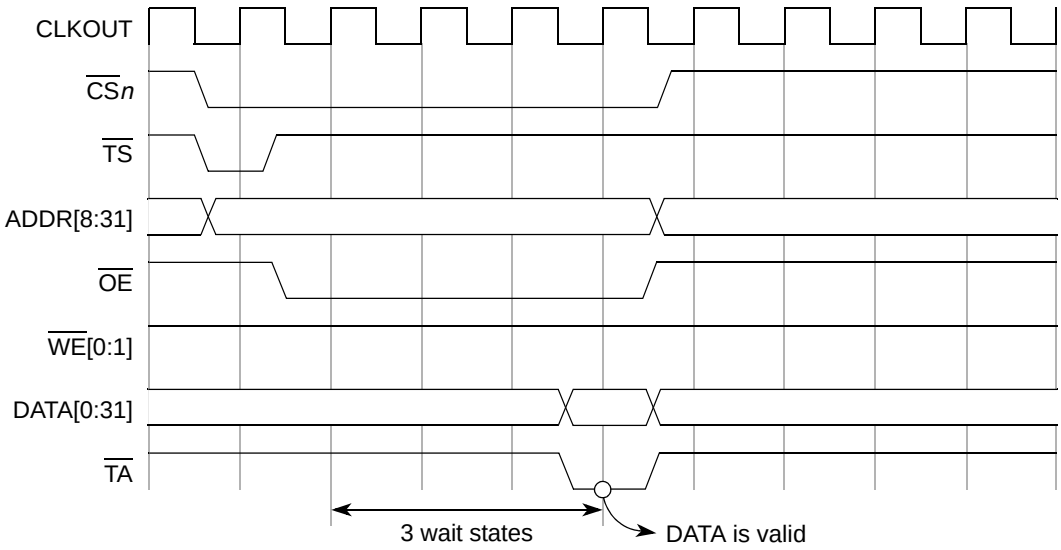


Figure 12-53. Read Operation to Asynchronous Memory, Three Initial Wait States

Figure 12-54 shows a timing diagram of a *write* operation to a 16-bit asynchronous memory using three wait states.

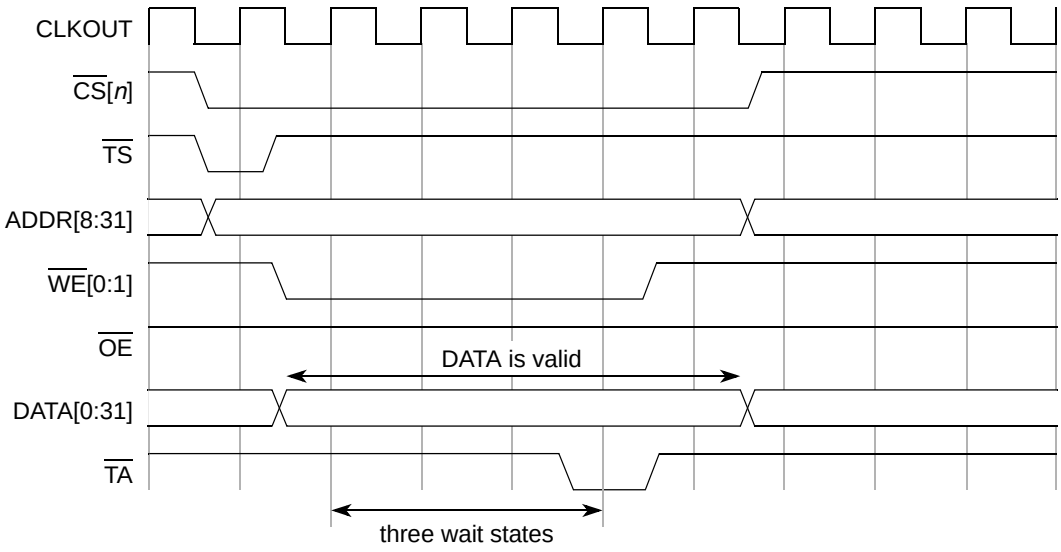
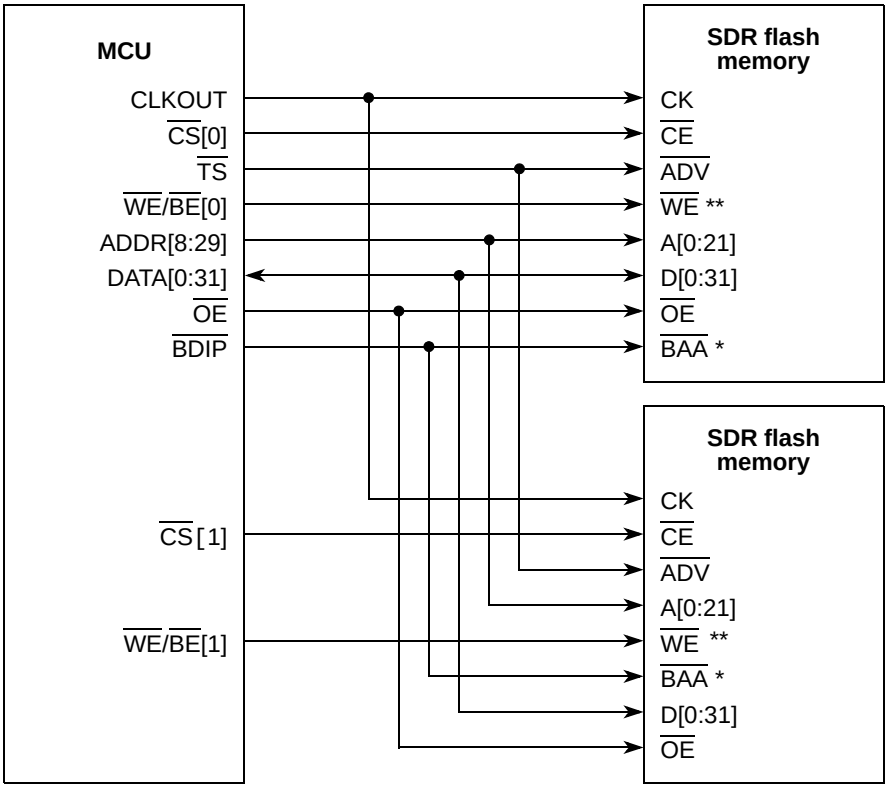


Figure 12-54. Write Operation to Asynchronous Memory, Three Initial Wait States

12.5.4 Connecting an MCU to Multiple Memories

The MCU can be connected to more than one memory at a time. Figure 12-55 shows an example of how to connect two memories to one MCU.



* Connected depending on the memory used.

** Flash memories typically use one WE signal as shown.

Note: On a 32-bit bus, RAM memories use all four WE/BE[0:3]. On a 16-bit bus, one RAM memory uses WE/BE[0:1] and the other uses WE/BE[2:3].

Figure 12-55. MCU Connected to Multiple Flash Memories

12.5.5 Summary of Differences from MPC5xx

The following summary lists the significant differences between this EBI used in the MPC5xxx and that of the MPC5xx parts:

- SETA feature is no longer available: chip select devices cannot use external TA, instead must use wait state configuration.
- No memory controller support for external masters: must configure each master in multi-master system to drive its own chip selects
- Changes in bit fields:
  - Removed these variable timing attributes from option register: CSNT, ACS, TRLX, EHTR
  - Removed LBDIP base register bit, now late BDIP assertion is default behavior

  - — Modified TSIZ[0:1] functionality to only indicate size of current transfer, not give information on ensuing transfers that be part of the same atomic sequence
  - — The BL field of the base register has inverted logic from the MPC56x devices (0 = eight-beat burst on the MPC5xxx, 1 = eight-beat burst on the MPC56x)
- Removed reservation support on external bus
- Removed address type (AT), write-protect (WP), and dual-mapping features because these functions can be replicated by memory management unit (MMU) in e200z6 core
- Removed support for 8-bit ports
- Removed boot chip select operation: on-chip boot assist module (BAM) handles boot (and configuration of EBI registers)
- Open drain mode and pullup resistors no longer required for multi-master systems, extra cycle needed to switch between masters
- Modified arbitration protocol to require extra cycles when switching between masters
- Added support for 32-bit coherent read and write non-chip select accesses in 16-bit data bus mode
- Misaligned accesses are not supported
- Calibration features implemented by four calibration chip selects
- Removed support for three-master systems
- Address decoding for external master accesses uses 4-bit code to determine internal slave instead of straight address decode

Chapter 13
Flash Memory

13.1 Introduction

This section provides information about the flash bus interface unit (FBIU) and the flash memory block.

13.1.1 Block Diagram

Figure 13-1 shows a block diagram of the flash memory module. The FBIU is addressed through the system bus while the flash control and status registers are addressed through the slave (peripheral) bus.

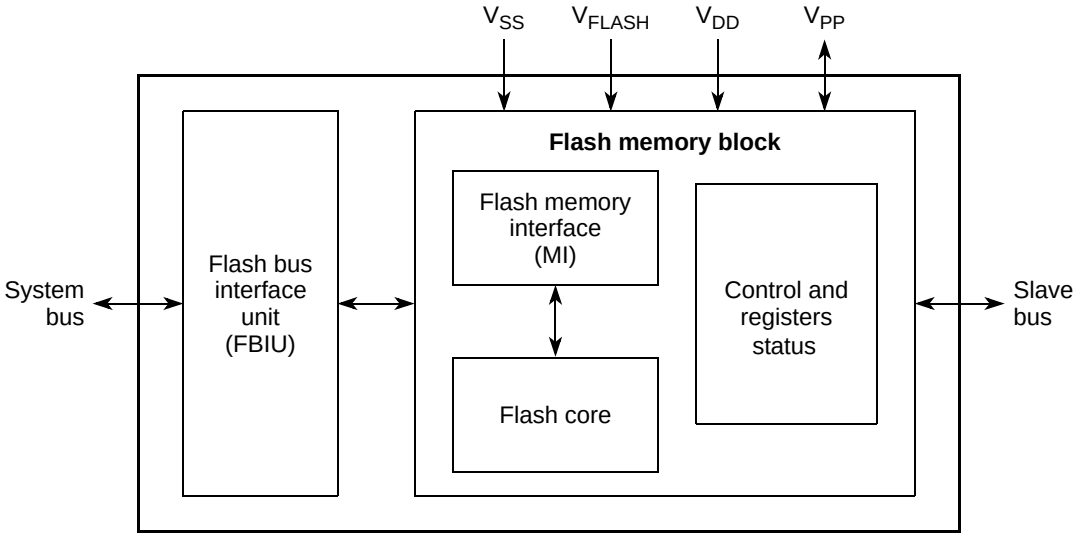


Figure 13-1. Flash System Block Diagram

13.1.2 Overview

The flash module serves as electrically programmable and erasable non-volatile memory (NVM) that is ideal for program and data storage for single-chip applications allowing for field reprogramming without requiring external programming voltage sources. The module is a solid-state silicon memory device consisting of blocks of single-transistor storage elements.

The device flash contains a flash bus interface unit (FBIU) and a flash memory array. The Flash BIU interfaces the system bus to a dedicated flash memory array controller. The FBIU supports a 64-bit data bus width at the system bus port, and a 256-bit read data interface from the flash memory array. If enabled, the Flash BIU contains a two-entry prefetch buffer, each entry containing 256 bits of data, and an associated controller that prefetches sequential lines of data from the flash array into the buffer. Prefetch

buffer hits support zero-wait responses. Normal flash array accesses (i.e. those accesses that do not hit in the prefetch buffers) are registered in the FBIU and are forwarded to the system bus on the following cycle, incurring at least three wait states (depending on the frequency), with additional wait states being determined by FLASH_BUICR[RWSC] (refer to Table 13-14).

Prefetch operations can be automatically controlled, and can be restricted to servicing a single bus master. Prefetches can also be restricted to being triggered for instruction or data accesses.

The flash memory block is arranged as two functional units, the first being the flash core. The flash core is composed of arrayed non-volatile storage elements, sense amplifiers, row selects, column selects, charge pumps, ECC logic and redundancy logic. The arrayed storage elements in the flash core are subdivided into physically separate units referred to as blocks.

The second functional unit of flash memory is the memory interface (MI). The MI contains the registers and logic that control the operation of the flash core. The MI is also the interface between the flash module and the FBIU. The FBIU connects the MCU system bus to the flash module, and provides all system level customization and configuration functionality.

The flash array has three address spaces. Low address space (LAS) is 256-KB in size. Mid address space (MAS) is also 256-KB in size. High address space (HAS) is 2.5 in size. Total address space is 3.0 MB.

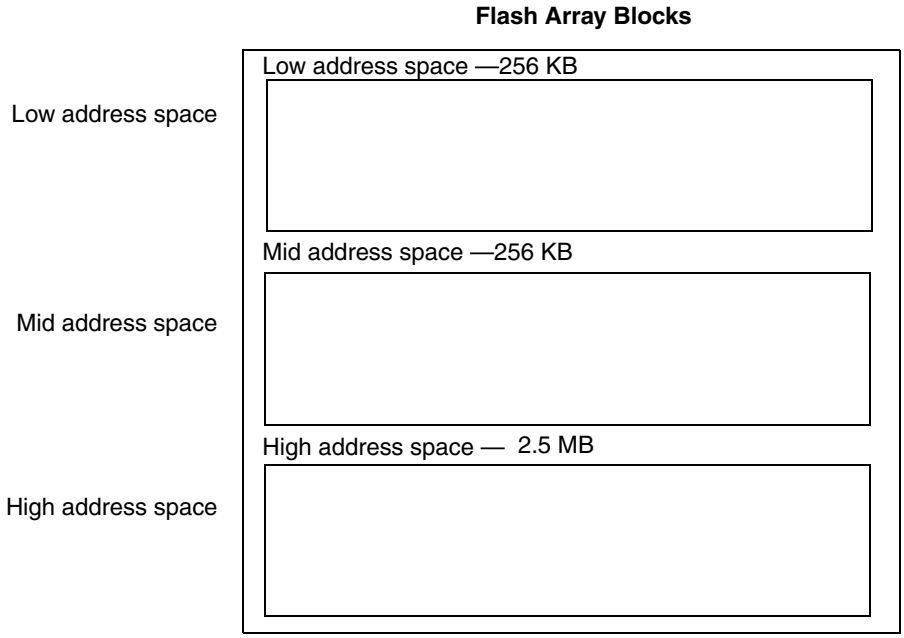


Figure 13-2. Flash Array Diagram

13.1.3 Features

The following list summarizes the key features of the FBIU:

- The FBIU system bus interface supports a 64-bit data bus. Byte, halfword, word, and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- The FBIU provides configurable read buffering and line prefetch support. Two line read buffers (each 256 bits wide) and a prefetch controller are used to support single-cycle read responses for hits in the buffers.
- The FBIU provides hardware and software configurable read and write access protections on a per-master basis.
- The FBIU interface to the flash array controller is pipelined with a depth of 1.
- The FBIU allows configurable access timing.
- The FBIU provides multiple-mapping support and mapping-based block access timing (0–31 additional cycles) allowing use for emulation of other memory types.

The flash memory array has the following features:

- Software programmable block program/erase restriction control for low, mid, and high address spaces.
- Erase of selected blocks.
- ECC with single-bit correction, double-bit detection.
- Page program size of 256 bits allows programming from one to four consecutive 64-bit doublewords within a page.
- Embedded hardware program and erase algorithm.
- Read while write with multiple partitions.
- Stop mode for low power stand-by.
- Erase suspend, program suspend, and erase-suspended program.
- Automotive flash that meets automotive endurance and reliability requirements.
- Shadow information is stored in a non-volatile shadow block.
- Independent program/erase of the shadow block.

13.1.4 Modes of Operation

13.1.4.1 User Mode

User mode is the default operating mode of the flash memory block. In this mode, you can read, write, program, and erase the flash. Refer to Section 13.4.2, “Flash Memory Array: User Mode.”

13.1.4.2 Stop Mode

In stop mode (FLASH_MCR[STOP] = 1), all DC current sources in the flash are disabled. Refer to Section 13.4.3, “Flash Memory Array: Stop Mode.”

13.2 External Signal Description

Table 13-1 shows a list of signals required for flash.

Table 13-1. Signal Properties

Name	Function	Reset State
V_{FLASH}	Flash read power supply	N/A
V_{PP}	Flash program / erase power supply	N/A

13.2.1 Voltage for Flash Only (V_{FLASH})

V_{FLASH} is a supply required for reads of the flash core. This voltage is specified as 3.3 V with a tolerance of ± 0.3 V.

13.2.2 Program and Erase Voltage for Flash Only (V_{PP})

V_{PP} is a supply required for program and erase of the flash core. This voltage is specified as 5 V with a tolerance of -0.5 V to +0.25 V during program and erase operations. V_{PP} is required at all times, even during normal reads of flash memory.

During read operations, V_{PP} can be as high as 5.3 V and as low as 3.0 V.

13.3 Memory Map and Register Description

The Flash BIU occupies a 512-MB portion of the address space. The actual flash array is multiply-mapped within this space.

The MCU's internal flash has a feature that allows the internal flash timing to be modified to emulate an external memory, hence the name, external emulation mode. The upper five address lines are used to provide additional timing control that allows the FBIU response timing on the system bus (which must be controlled to provide for timing emulation of alternate memory types). Refer to Figure 13-3.

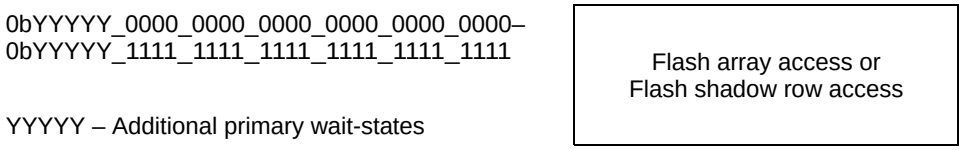


Figure 13-3. Flash BIU Address Scheme

This feature allows calibration parameters to be tested using an external memory; and then in production, the internal flash access timing is modified to match timing of the external memory. The access time of the internal flash is lengthened based on the address range being accessed. To access an area with a slower access time, the address is modified per Table 13-3.

Table 13-2. Internal Flash External Emulation Mode

Address Range		YYYYY	Wait States
0x0000_0000	0x002F_FFFF	00000	0
0x0100_0000	0x012F_FFFF	01000	8
0x0200_0000	0x022F_FFFF	10000	16
0x0300_0000	0x032F_FFFF	11000	24
0x0400_0000	0x042F_FFFF	00001	1
0x0500_0000	0x052F_FFFF	01001	9
0x0600_0000	0x062F_FFFF	10001	17
0x0700_0000	0x072F_FFFF	11001	25
0x0800_0000	0x082F_FFFF	00010	2
0x0900_0000	0x092F_FFFF	01010	10
0x0A00_0000	0x0A2F_FFFF	10010	18
0x0B00_0000	0x0B2F_FFFF	11010	26
0x0C00_0000	0x0C2F_FFFF	00011	3
0x0D00_0000	0x0D2F_FFFF	01011	11
0x0E00_0000	0x0E2F_FFFF	10011	19
0x0F00_0000	0x0F2F_FFFF	11011	27
0x1000_0000	0x102F_FFFF	00100	4
0x1100_0000	0x112F_FFFF	01100	12
0x1200_0000	0x122F_FFFF	10100	20
0x1300_0000	0x132F_FFFF	11100	28
0x1400_0000	0x142F_FFFF	00101	5
0x1500_0000	0x152F_FFFF	01101	13
0x1600_0000	0x162F_FFFF	10101	21
0x1700_0000	0x172F_FFFF	11101	29
0x1800_0000	0x182F_FFFF	00110	6
0x1900_0000	0x192F_FFFF	01110	14
0x1A00_0000	0x1A2F_FFFF	10110	22
0x1B00_0000	0x1B2F_FFFF	11110	30
0x1C00_0000	0x1C2F_FFFF	00111	7
0x1D00_0000	0x1D2F_FFFF	01111	15
0x1E00_0000	0x1E2F_FFFF	10111	23
0x1F00_0000	0x1F2F_FFFF	11111	31

13.3.1 Flash Memory Map

Table 13-3 shows the flash array memory map and how it is mapped using byte addressing.

Base addresses for the device are the following:

- Shadow base address = 0x00FF_FC00
- Array base address = 0x0000_0000
- Control registers base address = 0xC3F8_8000

Table 13-3. Module Flash Array Memory Map

Byte Address	Type and Amount of Space Used	Access
Shadow base + (0x0000_0000–0x0000_03FF)	Shadow block space (1024 bytes)	User
Array base + (0x0000_0000–0x0003_FFFF)	Low address space (256 KB)	User
Array base + (0x0004_0000–0x0007_FFFF)	Mid address space (256 KB)	User
Array base + (0x0008_0000–0x2F00_FFFF)	High address space (2.5 MB)	User

Table 13-4 shows how the array is partitioned into three address spaces — low, mid, and high — and into partitions and blocks.

Table 13-4. Flash Partitions

Address	Use	Block	Size	Partition
Array base + 0x0000_0000	Low address space	L0	16 KB	1
Array base + 0x0000_4000		L1	48 KB	
Array base + 0x0001_0000		L2	48 KB	
Array base + 0x0001_C000		L3	16 KB	
Array base + 0x0002_0000		L4	64 KB	2
Array base + 0x0003_0000		L5	64 KB	
Array base + 0x0004_0000	Middle address space	M0	128 KB	3
Array base + 0x0006_0000		M1	128 KB	
Array base + 0x0008_0000	High address space	H0	128 KB	4
Array base + 0x000A_0000		H1	128 KB	
Array base + 0x000C_0000		H2	128 KB	5
Array base + 0x000E_0000		H3	128 KB	
Array base + 0x0010_0000		H4	128 KB	6
Array base + 0x0012_0000		H5	128 KB	
Array base + 0x0014_0000		H6	128 KB	7
Array base + 0x0016_0000		H7	128 KB	
Array base + 0x0018_0000		H8	128 KB	8
Array base + 0x001A_0000		H9	128 KB	
Array base + 0x001C_0000		H10	128 KB	9
Array base + 0x001E_0000		H11	128 KB	
Array base + 0x0020_0000		H12	128 KB	10
Array base + 0x0022_0000		H13	128 KB	
Array base + 0x0024_0000		H14	128 KB	11
Array base + 0x0026_0000		H15	128 KB	
Array base + 0x0028_0000		H16	128 KB	12
Array base + 0x002A_0000		H17	128 KB	
Array base + 0x002C_0000		H18	128 KB	13
Array base + 0x002E_0000		H19	128 KB	

Table 13-4. Flash Partitions (continued)

Address	Use	Block	Size	Partition
Array base + 0x00FF_FC00	Shadow block space	S	472 KB	All[1]
Array base + 0x00FF_FDD8	Flash shadow row, serial passcode		8 KB	
Array base + 0x00FF_FDE0	Flash shadow row, control word		4 KB	
Array base + 0x00FF_FDE4	General use		4 KB	
Array base + 0x00FF_FDE8	Flash shadow row, FLASH_LMLR reset configuration		4 KB	
Array base + 0x00FF_FDEC	General use		4 KB	
Array base + 0x00FF_FDF0	Flash shadow row, FLASH_HLR reset configuration		4 KB	
Array base + 0x00FF_FDF4	For general use		4 KB	
Array base + 0x00FF_FDF8	Flash Shadow Row, FLASH_SLMLR reset configuration		4 KB	
Array base + (0x00FF_FDFC–0x00FF_FFFF)	For general use		516 KB	

[1] The shadow row does not support RWW. Refer to Section 13.4.2.5, “Flash Shadow Block.”

Table 13-5 shows the register set for the flash module.

Table 13-5. Module Register Memory Map

Byte Address	Register Name	Register Description	Bits
Register base + 0x0000	FLASH_MCR	Module configuration register	32
Register base + 0x0004	FLASH_LMLR	Low and middle address space block locking register	32
Register base + 0x0008	FLASH_HLR	High address space block locking register	32
Register base + 0x000C	FLASH_SLMLR	Secondary low/mid address space block locking register	32
Register base + 0x0010	FLASH_LMSR	Low and middle address space block select register	32
Register base + 0x0014	FLASH_HSR	High address space block select register	32
Register base + 0x0018	FLASH_AR	Address register	32
Register base + 0x001C	FLASH_BIUCR	Flash bus interface unit control register	32
Register base + 0x0020	FLASH_BIUAPR	Flash bus interface unit access protection register	32
Register base + (0x0030–0x7FFF)	—	Reserved	—

13.3.2 Register Descriptions

The flash registers are detailed in the following sections.

13.3.2.1 Module Configuration Register (FLASH_MCR)

A number of module configuration register (FLASH_MCR) bits are protected from a write while another bit or set of bits are in a specific state. These locks are discussed in relationship to each bit in this section. Simultaneously writing bits which lock each other out is discussed in Section 13.3.2.1.1, “MCR Simultaneous Register Writes.” The MCR is always available to be read except when the flash module is disabled.

Address: Base (0xC3F8_8000) + 0x0000 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	SIZE				0	LAS			0	0	0	MAS
W																
Reset	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	EER	RWE	1	1	PEAS	DONE	PEG	0	0	STOP	0	PGM	PSUS	ERS	ESUS	EHV
W	w1c	w1c														
Reset	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0

Figure 13-4. Module Configuration Register (FLASH_MCR)

Table 13-6. FLASH_MCR Field Descriptions

Field	Description
0–3	Reserved.
4–7 SIZE[0:3]	Array space size. Dependent upon the size of the flash module. SIZE is read only. 1011 Total array size is 3 MB
8	Reserved.
9–11 LAS[0:2]	Low address space. Corresponds to the configuration of the low address space. All possible values of LAS and the configuration to which each value corresponds are shown below. LAS is read only. 110 The LAS value of 110 provides two 16-KB blocks, two 48-KB blocks, and two 64-KB blocks.
12–14	Reserved.
15 MAS	Mid address space size. Corresponds to the configuration of the mid address space. MAS is read only. 0 Two 128-KB blocks are available

Table 13-6. FLASH_MCR Field Descriptions (continued)

Field	Description
16 EER	ECC event error. Provides information on previous reads; if a double bit detection occurred, the EER bit is set to 1. This bit must then be cleared, or a reset must occur before this bit returns to a 0 state. This bit cannot be set by the application. In the event of a single bit detection and correction, this bit is not set. If EER is not set, or remains 0, this indicates that all previous reads (from the last reset, or clearing of EER) were correct. Since this bit is an error flag, it must be cleared to a 0 by writing a 1 to the register location. A write of 0 has no effect. 0 Reads are occurring normally. 1 An ECC Error occurred during a previous read. **Note:** This bit can be set on speculative prefetches that cause double bit error detection. Therefore, use the ECSM[FNCE] flag for detecting non-correctable ECC errors in the flash instead of using FLASH_MCR[EER].
17 RWE	Read while write event error. Provides information on previous RWW reads. If a read while write error occurs, this bit is set to 1. This bit must then be cleared, or a reset must occur before this bit returns to a 0 state. This bit cannot be set to 1 by the user. If RWE is not set, or remains 0, this indicates that all previous RWW reads (from the last reset, or clearing of RWE) were correct. Since this bit is an error flag, it must be cleared to a 0 by writing a 1 to the register location. A write of 0 has no effect. 0 Reads are occurring normally. 1 A read while write error occurred during a previous read.
18–19	Reserved.
20 PEAS	Program/erase access space. Indicates which space is valid for program and erase operations, either main array space or shadow space. PEAS is read only. 0 Shadow address space is disabled for program/erase and main address space enabled 1 Shadow address space is enabled for program/erase and main address space disabled.
21 DONE	State machine status. Indicates if the flash module is performing a high voltage operation. DONE is set to a 1 on termination of the flash module reset and at the end of program and erase high voltage sequences. 0 Flash is executing a high voltage operation. 1 Flash is not executing a high voltage operation.
22 PEG	Program/erase good. Indicates the completion status of the last flash program or erase sequence for which high voltage operations were initiated. The value of PEG is updated automatically during the program and erase high voltage operations. Aborting a program/erase high voltage operation causes PEG to be cleared, indicating the sequence failed. PEG is set to a 1 when the module is reset. PEG is read only. The value of PEG is valid only when PGM = 1 and/or ERS = 1 and after DONE has transitioned from 0 to 1 due to an abort or the completion of a program/erase operation. PEG is valid until PGM/ERS makes a 1 to 0 transition or EHV makes a 0 to 1 transition. The value in PEG is not valid after a 0 to 1 transition of DONE caused by PSUS or ESUS being set to logic 1. A diagram presenting PEG valid times is presented in Figure 13-5. If PGM and ERS are both 1 when DONE makes a qualifying 0 to 1 transition the value of PEG indicates the completion status of the PGM sequence. This happens in an erase-suspended program operation. 0 Program or erase operation failed. 1 Program or erase operation successful.
23–24	Reserved.
25 STOP	Stop mode enabled. Puts the flash into stop mode. Changing the value in STOP from a 0 to a 1 places the flash module in stop mode. A 1 to 0 transition of STOP returns the flash module to normal operation. STOP can be written only when PGM and ERS are low. When STOP = 1, only the STOP bit in the MCR can be written. In STOP mode all address spaces, registers, and register bits are deactivated except for the FLASH_MCR[STOP] bit. 0 Flash is not in stop mode; the read state is active. 1 Flash is in stop mode.

Table 13-6. FLASH_MCR Field Descriptions (continued)

Field	Description
26	Reserved.
27 PGM	Program. Used to set up flash for a program operation. A 0 to 1 transition of PGM initiates an flash program sequence. A 1 to 0 transition of PGM ends the program sequence. PGM can be set only under one of the following conditions: • User mode read (STOP and ERS are low). • Erase suspend[1] (ERS and ESUS are 1) with EHV low. PGM can be cleared by the user only when EHV are low and DONE is high. PGM is cleared on reset. 0 Flash is not executing a program sequence. 1 Flash is executing a program sequence.
28 PSUS	Program suspend. Indicates the flash module is in program suspend or in the process of entering a suspend state. The flash module is in program suspend when PSUS = 1 and DONE = 1. PSUS can be set high only when PGM and EHV are high. A 0 to 1 transition of PSUS starts the sequence which sets DONE and places the flash in program suspend. PSUS can be cleared only when DONE and EHV are high. A 1 to 0 transition of PSUS with EHV = 1 starts the sequence which clears DONE and returns the flash module to program. The flash module cannot exit program suspend and clear DONE while EHV is low. PSUS is cleared on reset. 0 Program sequence is not suspended. 1 Program sequence is suspended.
29 ERS	Erase. Used to set up flash for an erase operation. A 0 to 1 transition of ERS initiates an flash erase sequence. A 1 to 0 transition of ERS ends the erase sequence. ERS can be set only in a normal operating mode read (STOP and PGM are low). ERS can be cleared by the user only when ESUS and EHV are low and DONE is high. ERS is cleared on reset. 0 Flash is not executing an erase sequence. 1 Flash is executing an erase sequence.
30 ESUS	Erase suspend. Indicates that the flash module is in erase suspend or in the process of entering a suspend state. The flash module is in erase suspend when ESUS = 1 and DONE = 1. ESUS can be set high only when ERS and EHV are high and PGM is low. A 0 to 1 transition of ESUS starts the sequence which sets DONE and places the flash in erase suspend. ESUS can be cleared only when DONE and EHV are high and PGM is low. A 1 to 0 transition of ESUS with EHV = 1 starts the sequence which clears DONE and returns the flash module to erase mode. The flash module cannot exit erase suspend and clear DONE while EHV is low. ESUS is cleared on reset. 0 Erase sequence is not suspended. 1 Erase sequence is suspended.

Table 13-6. FLASH_MCR Field Descriptions (continued)

Field	Description
31 EHV	Enable high voltage. Enables the flash module for a high voltage program/erase operation. EHV is cleared on reset. EHV must be set after an interlock write to start a program/erase sequence. EHV can be set, initiating a program/erase, after an interlock write under one of the following conditions: • Erase (ERS = 1, ESUS = 0). • Program (ERS = 0, ESUS = 0, PGM = 1, PSUS = 0). • Erase-suspended program (ERS = 1, ESUS = 1, PGM = 1, PSUS = 0). If a program operation is to be initiated while an erase is suspended the user must clear EHV while in erase suspend before setting PGM. In normal operation, a 1 to 0 transition of EHV with DONE high, PSUS and ESUS low terminates the current program/erase high voltage operation. When an operation is aborted[2], there is a 1 to 0 transition of EHV with DONE low and the suspend bit for the current program/erase sequence low. An abort causes the value of PEG to be cleared, indicating a failed program/erase; address locations being operated on by the aborted operation contain indeterminate data after an abort. A suspended operation cannot be aborted. EHV can be written during suspend. EHV must be high for the flash to exit suspend. Do not writer the EHV bit after a suspend bit is set high and before DONE has transitioned high. Do not set the EHV bit low after the current suspend bit is set low and before DONE has transitioned low. 0 Flash is not enabled to perform a high voltage operation. 1 Flash is enabled to perform a high voltage operation.

1 In an erase-suspended program, programming flash locations in blocks which were being operated on in the erase can corrupt flash core data. Avoid this case due to reliability implications.

2 Aborting a high voltage operation leaves the flash core addresses in an indeterminate data state. This can be recovered by executing an erase on the affected blocks.

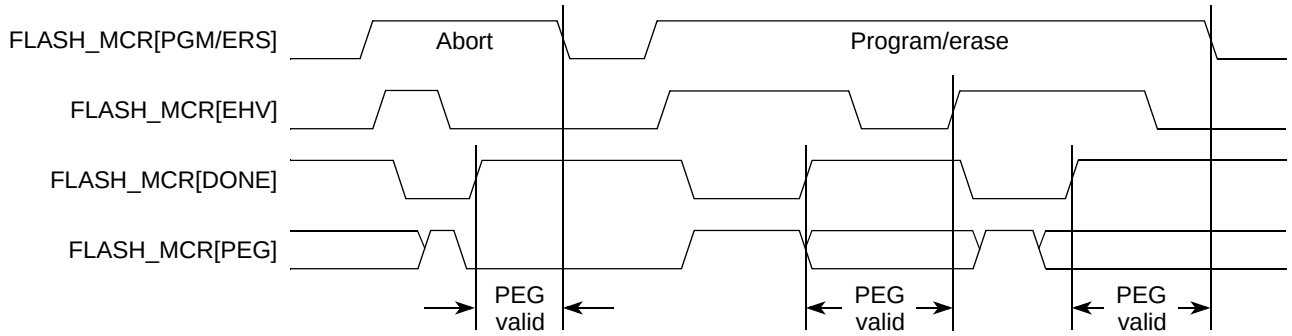


Figure 13-5. PEG Valid Times

13.3.2.1.1 MCR Simultaneous Register Writes

A number of MCR bits are protected against write when another bit or set of bits is in a specific state. These write locks are covered on a bit by bit basis in Section 13.3.2.1, "Module Configuration Register (FLASH_MCR)." The write locks detailed in that section do not consider the effects of trying to write two or more bits simultaneously. The effects of writing bits simultaneously that put the flash module in an illegal state are detailed here.

The flash does not allow you to write bits simultaneously that put the device into an illegal state. This is implemented through a priority mechanism among the bits. The bit changing priorities are detailed in Table 13-7.

Table 13-7. MCR Bit Set/Clear Priority Levels

Priority Level	MCR Bits
1	STOP
2	ERS
3	PGM
4	EHV
5	ESUS, PSUS

If the user attempts to write two or more MCR bits simultaneously then only the bit with the highest priority level is written. Setting two bits with the same priority level is prevented by existing write locks and does not put the flash in an illegal state.

For example, setting FLASH_MCR[STOP] and FLASH_MCR[PGM] simultaneously results in only FLASH_MCR[STOP] being set. Attempting to clear FLASH_MCR[EHV] while setting FLASH_MCR[PSUS] results in FLASH_MCR[EHV] being cleared, while FLASH_MCR[PSUS] remains unaffected.

13.3.2.2 Low/Mid Address Space Block Locking Register (FLASH_LMLR)

The low and mid address block locking register provides a means to protect blocks from being modified. These bits along with bits in the secondary LMLOCK field (FLASH_SLMLR), determine if the block is locked from program or erase. An “OR”’ of FLASH_LMLR and FLASH_SLMLR determine the final lock status. Refer to Section 13.3.2.4, “Secondary Low/Mid Address Space Block Locking Register (FLASH_SLMLR)” for more information on FLASH_SLMLR.

NOTE

In the event that blocks are not present (due to configuration or total memory size), the LOCK bits defaults to locked, and are not writable. The reset value is always 1 (independent of the shadow block), and register writes have no effect.

Address: Base (0xC3F8_8000) + 0x0004 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	LME	0	0	0	0	0	0	0	0	0	0	SLOCK	1	1	MLOCK		1	1	1	1	1	1	1	1	1	1	LLOCK					
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]

[1] The reset value of these bits is determined by flash values in the shadow row. Erasing the array sets the reset value to 1.

Figure 13-6. Low/Mid Address Space Block Locking Register (FLASH_LMLR)

Table 13-8. FLASH_LMLR Field Descriptions

Field	Description
0 LME	Low and mid address lock enable. Enables the locking register fields (SLOCK, MLOCK and LLOCK) to be set or cleared by register writes. This bit is a status bit only, and can not be written or cleared, and the reset value is 0. The method to set this bit is to write a password, and if the password matches, the LME bit is set to reflect the status of enabled, and is enabled until a reset operation occurs. For LME, the password 0xA1A1_1111 must be written to the FLASH_LMLR. 0 Low and mid address locks are disabled, and cannot be modified. 1 Low and mid address locks are enabled and can be written.
1–10	Reserved.
11 SLOCK	Shadow lock. Locks the shadow row from programs and erases. The SLOCK bit is not writable if a high voltage operation is suspended. Upon reset, information from the shadow row is loaded into the SLOCK bit. The SLOCK bit can be written as a register. Reset causes the bits to go back to their shadow row value. The default value of the SLOCK bit (assuming the corresponding shadow row bit is erased) is locked. SLOCK is not writable unless LME is high. 0 Shadow row is available to receive program and erase pulses. 1 Shadow row is locked for program and erase.
12–13	Reserved.
14–15 MLOCK[1:0]	Mid address block lock. A value of 1 in a bit of the lock register signifies that the corresponding block is locked for program and erase. A value of 0 in the lock register signifies that the corresponding block is available to receive program and erase pulses. Likewise the lock register is not writable if a high voltage operation is suspended. Upon reset, information from the shadow row is loaded into the block registers. The LOCK bits can be written as a register. Reset causes the bits to return to their shadow row value. The default value of the LOCK bits (assuming erased fuses) is locked. In the event that blocks are not present (due to configuration or total memory size), the LOCK bits default to locked, and are not writable. The reset value always is 1 (independent of the shadow row), and register writes have no effect. MLOCK is not writable unless LME is high.
16–25	Reserved
26–31 LLOCK[5:0]	Low address block lock. These bits have the same description and attributes as MLOCK. As an example of how the LLOCK bits are used, if a configuration has six 16-KB blocks in the low address space, the block residing at address array base + 0, corresponds to LLOCK0. The next 16-KB block corresponds to LLOCK1, and so on up to LLOCK5.

13.3.2.3 High Address Space Block Locking Register (FLASH_HLR)

The high address space block locking register provides a means to protect blocks from being modified.

Address: Base (0xC3F8_8000) + 0x0008 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	HBE	0	0	0	1	1	1	1	1	1	1	1	HLOCK																			
W																																
Reset	0	0	0	0	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]

[1] The reset value of these bits is determined by flash values in the shadow row. An erased array causes the reset value to be 1.

Figure 13-7. High Address Space Block Locking Register (FLASH_HLR)

Table 13-9. FLASH_HLR Field Descriptions

Field	Description
0 HBE	High address lock enable. Enables the locking field (HLOCK) to be set or cleared by register writes. This bit is a status bit only, and cannot be written to or cleared, and the reset value is 0. The method to set this bit is to provide a password, and if the password matches, the HBE bit is set to reflect the status of enabled, and is enabled until a reset operation occurs. For HBE, the password 0xB2B2_2222 must be written to FLASH_HLR. 0 High address locks are disabled, and cannot be modified. 1 High address locks are enabled to be written.
1–11	Reserved.
12–31 HLOCK[19:0]	High address space block lock. Has the same characteristics as MLOCK. Refer to Section 13.3.2.2, “Low/Mid Address Space Block Locking Register (FLASH_LMLR)” for more information. The block numbering for High Address space starts with HLOCK[0] and continues until all blocks are accounted. HLOCK is not writable unless HBE is set. In the event that blocks are not present (due to configuration or total memory size), the HLOCK bits are default to locked, and are not writable.

13.3.2.4 Secondary Low/Mid Address Space Block Locking Register (FLASH_SLMLR)

The FLASH_SLMLR provides an alternative means to protect blocks from being modified. These bits along with bits in the LMLOCK field (FLASH_LMLR), determine if the block is locked from program or erase. An “OR” of FLASH_LMLR and FLASH_SLMLR determine the final lock status. Refer to Section 13.3.2.2, “Low/Mid Address Space Block Locking Register (FLASH_LMLR)” for more information on FLASH_LMLR.

Address: Base (0xC3F8_8000) + 0x000C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	SLE	0	0	0	0	0	0	0	0	0	0	SS LOCK	1	1	SM LOCK		1	1	1	1	1	1	1	1	1	1	SLLOCK					
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	1[1]	1	1	1[1]	1[1]	1	1	1	1	1	1	1	1	1	1	1[1]	1[1]	1[1]	1[1]	1[1]	1[1]

[1] The reset value of these bits is determined by flash values in the shadow row. An erased array sets the reset value to 1.

Figure 13-8. Secondary Low/Mid Address Space Block Locking Register (FLASH_SLMLR)

Table 13-10. FLASH_SLMLR Field Descriptions

Field	Description
0 SLE	Secondary low and mid address lock enable. Enables the secondary lock fields (SSLOCK, SMLOCK, and SLLOCK) to be set or cleared by register writes. This bit is a status bit only, and cannot be written to or cleared, and the reset value is 0. The method to set this bit is to provide a password, and if the password matches, the SLE bit is set to reflect the status of enabled, and is enabled until a reset operation occurs. For SLE, the password 0xC3C3_3333 must be written to the FLASH_SLMLR. 0 Secondary low and mid address locks are disabled, and cannot be modified. 1 Secondary low and mid address locks are enabled to be written.
1–10	Reserved.
11 SSLOCK	Secondary shadow lock. An alternative method to use to lock the shadow row from programs and erases. SSLOCK has the same description as SLOCK in Section 13.3.2.2, “Low/Mid Address Space Block Locking Register (FLASH_LMLR).” SSLOCK is not writable unless SLE is high.
12–13	Reserved.
14–15 SMLOCK[1:0]	Secondary mid address block lock. Alternative method to use to lock the mid address space blocks from programs and erases. SMLOCK has the same description as MLOCK in section Section 13.3.2.2, “Low/Mid Address Space Block Locking Register (FLASH_LMLR).” SMLOCK is not writable unless SLE is set. In the event that blocks are not present (due to configuration or total memory size), the SMLOCK bits default to locked, and not writable.
16–25	Reserved.
26–31 SLLOCK[5:0]	Secondary low address block lock. These bits are an alternative method that to use to lock the low address space blocks from programs and erases. SLLOCK has the same description as LLOCK in Section 13.3.2.2, “Low/Mid Address Space Block Locking Register (FLASH_LMLR). SLLOCK is not writable unless SLE is high. In the event that blocks are not present (due to configuration or total memory size), the SLLOCK bits default to locked, and are not writable.

13.3.2.5 Low/Mid Address Space Block Select Register (FLASH_LMSR)

The FLASH_LMSR provides a means to select blocks to be operated on during erase.

Address: Base (0xC3F8_8000) + 0x0010 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MSEL		0	0	0	0	0	0	0	0	0	0	LSEL					
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 13-9. Low/Mid Address Space Block Select Register (FLASH_LMSR)

Table 13-11. FLASH_LMSR Field Descriptions

Field	Description
0–13	Reserved.
14–15 MSEL[1:0]	Mid address space block select. Values in the selected register signify that a block(s) is or is not selected for erase. The reset value for the select registers is 0. The blocks must be selected (or unselected) before doing an erase interlock write as part of the erase sequence. The select register is not writable after an interlock write is completed or if a high voltage operation is suspended. In the event that blocks are not present (due to configuration or total memory size), the corresponding SELECT bits default to unselected, and are not writable. The reset value is always 0, and register writes have no effect. A description of how blocks are numbered is detailed in Section 13.3.2.2, “Low/Mid Address Space Block Locking Register (FLASH_LMLR).” 0b0000 Mid address space blocks are *not* selected for erase 0b0001 One mid address space block is selected for erase 0b0011 Two mid address space blocks are selected for erase
16–25	Reserved.
26–31 LSEL[5:0]	Low address space block select. Used to select blocks in the low address space; these have the same description and attributes as the MSEL bits 0b0000 Low address space blocks are *not* selected for erase 0b0001 One low address space block is selected for erase 0b0011 Two low address space blocks are selected for erase 0b0111 Three low address space blocks are selected for erase 0b1111 Four low address space blocks are selected for erase 0b0001_1111 Five low address space blocks are selected for erase 0b0011_1111 Six low address space blocks are selected for erase

13.3.2.6 High Address Space Block Select Register (FLASH_HSR)

The FLASH_HSR allows the application to select the high address flash blocks on which to operate.

Address: Base (0xC3F8_8000) + 0x0014 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	1	1	1	1	1	1	1	1	HBSEL																			
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 13-10. High Address Space Block Select Register (FLASH_HSR)

Table 13-12. FLASH_HSR Field Descriptions

Field	Description
0–11	Reserved.
12–31 HBSEL[19:0]	High address space block select. Has the same characteristics as MSEL. For more information refer to Section 13.3.2.5, “Low/Mid Address Space Block Select Register (FLASH_LMSR).” 0b0000 High address space blocks are *not* selected for erase 0b0001 One high address space block is selected for erase 0b0011 Two high address space blocks are selected for erase 0b0111 Three high address space blocks are selected for erase 0b1111 Four high address space blocks are selected for erase 0b0001_1111 Five high address space blocks are selected for erase 0b0011_1111 Six high address space blocks are selected for erase 0b0111_1111 Seven high address space blocks are selected for erase 0b1111_1111 Eight high address space blocks are selected for erase 0b0001_1111_1111 Nine high address space blocks are selected for erase 0b0011_1111_1111 Ten high address space blocks are selected for erase 0b0111_1111_1111 Eleven high address space blocks are selected for erase 0b1111_1111_1111 Twelve high address space blocks are selected for erase 0b0001_1111_1111_1111_1111 17 high address space blocks are selected for erase 0b0011_1111_1111_1111_1111 18 high address space blocks are selected for erase 0b0111_1111_1111_1111_1111 19 high address space blocks are selected for erase 0b1111_1111_1111_1111_1111 20 high address space blocks are selected for erase

13.3.2.7 Address Register (FLASH_AR)

The FLASH_AR provides the first failing address in the event of ECC event error (FLASH_MCR[EER] set), as well as providing the address of a failure that occurs in a state machine operation (FLASH_MCR[PEG] cleared). ECC event errors take priority over state machine errors. This is especially valuable in the event of a RWW operation, where the read senses an ECC error and the state machine fails simultaneously. This address is always a doubleword address that selects 64 bits.

In normal operating mode, the FLASH_AR is not writable.

Address: Base (0xC3F8_8000) + 0x0018 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	ADDR																			0	0	0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 13-11. Address Register (FLASH_AR)

Table 13-13. FLASH_AR Field Descriptions

Field	Description
0–9	Reserved.
10–28 ADDR[3:21]	Doubleword address of first failing address in the event of an ECC error, or the address of a failure occurring during state machine operation.
29–31 ADDR[0:2]	Always read as 0.

13.3.2.8 Flash Bus Interface Unit Control Register (FLASH_BIUCR)

The FLASH_BIUCR is the control register for the set up and control of the flash interface. This register must not be written while executing from flash. Only use a 32-bit write operation to write to this register.

Address: Base (0xC3F8_8000) + 0x001C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	M4 PFE	M3 PFE	M2 PFE	M1 PFE	M0 PFE
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	238	24	25	26	27	28	29	30	31
R	APC			WWSC		RWSC			DPFEN		IPFEN		PFLIM			BFEN
W																
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Figure 13-12. Flash Bus Interface Unit Control Register (FLASH_BIUCR)

Table 13-14. FLASH_BIUCR Field Descriptions

Bits	Description
0-10	Reserved
11-15	Master *n* prefetch enable. Used to control whether prefetching can be triggered based on the master ID of a requesting master. These bits are cleared by hardware reset. Refer to 1. 0 No prefetching can be triggered by this master 1 Prefetching can be triggered by this master These fields are identified as follows: M4PFE = FEC M3PFE= EBI M2PFE= eDMA M1PFE= Nexus M0PFE= MCU core
16–18 APC[1]	Address pipelining control. Used to control the number of cycles between pipelined access requests. This field must be set to a value corresponding to the operating frequency of the system clock. The required settings are documented in Table 13-15. 000 Reserved 001 Access requests require one hold cycle 010 Access requests require two hold cycles ... 110 Access requests require 6 hold cycles 111 No address pipelining
19–20 WWSC [1]	Write wait state control. Used to control the timing for array writes. This field must be set to a value corresponding to the operating frequency of the system clock. The required settings are documented in Table 13-15. 00 Reserved 01 One wait state 10 Two wait states 11 Three wait states
21–23 RWSC [1]	Read wait state control**.** Used to control the flash array access time for array reads. This field must be set to a value corresponding to the operating frequency of the system clock. The required settings are documented in Table 13-15. 000 Zero wait states 001 One wait state ... 111 Seven wait states
24–25 DPFEN	Data prefetch enable. Enables or disables prefetching initiated by a data read access. This field is cleared by hardware reset. 00 No prefetching is triggered by a data read access 01 Prefetching can be triggered only by a data burst read access 10 Reserved 11 Prefetching can be triggered by any data read access
26–27 IPFEN	Instruction prefetch enable. Enables or disables prefetching initiated by an instruction read access. This field is cleared by hardware reset. 00 No prefetching is triggered by an instruction read access 01 Prefetching can be triggered only by an instruction burst read access 10 Reserved 11 Prefetching can be triggered by any instruction read access

Table 13-14. FLASH_BIUCR Field Descriptions (continued)

Bits	Description
28–30 PFLIM	Prefetch limit. Controls the prefetch algorithm used by the FBIU prefetch controller. This field defines a limit on the maximum number of sequential prefetches which are attempted between buffer misses. This field is cleared by hardware reset. 000 No prefetching is performed 001 A single additional line (next sequential) is prefetched on a buffer miss 010 Up to two additional lines can be prefetched following each buffer miss before prefetching is halted. A single additional line (next sequential) is prefetched on a buffer miss, and the next sequential line is prefetched on a buffer hit (if not already present). 011 Up to three additional lines can be prefetched following each buffer miss before prefetching is halted. Only a single additional prefetch is initiated after each buffer hit or miss. 100 Up to four additional lines can be prefetched following each buffer miss before prefetching is halted. Only a single additional prefetch is initiated after each buffer hit or miss. 101 Up to five additional lines can be prefetched following each buffer miss before prefetching is halted. Only a single additional prefetch is initiated after each buffer hit or miss. 110 An unlimited number of additional lines can be prefetched following each buffer miss. Only a single additional prefetch is initiated on each buffer hit or miss. 111 Reserved
31 BFEN	FBIU line read buffers enable. Enables or disables line read buffer hits. It is also used to invalidate the buffers. These bits are cleared by hardware reset. 0 The line read buffers are disabled from satisfying read requests, and all buffer valid bits are cleared. 1 The line read buffers are enabled to satisfy read requests on hits. Buffer valid bits can be set when the buffers are successfully filled. **Note:** Disable prefetching before invalidating the buffers. This includes starting a program or erase operation, or turning on and off the buffers.

[1] APC, WWSC, and RWSC values are determined by the maximum frequency of operation. Refer to Table 13-15.

Table 13-15. FLASH_BIU Settings vs. Frequency of Operation

Maximum Frequency (MHz)	APC	RWSC	WWSC	DPFEN	IPFEN	PFLIM	BFEN
up to and including 82 MHz[1]	0b001	0b001	0b01	0b00, 0b01, or 0b11[2]	0b00, 0b01, or 0b11[2]	0b000-0b110[3]	0b0, 0b1[4]
up to and including 102 MHz[5]	0b001	0b010	0b01	0b00, 0b01, or 0b11[2]	0b00, 0b01, or 0b11[2]	0b000-0b110[3]	0b0, 0b1[4]
up to and including132 MHz[6]	0b010	0b011	0b01	0b00, 0b01, or 0b11[2]	0b00, 0b01, or 0b11[2]	0b000-0b110[3]	0b0, 0b1[4]
Default Setting after Reset	0b111	0b111	0b11	0b00	0b00	0b000	0b0

[1] This setting allows for 80 MHz system clock with 2% frequency modulation.

[2] For maximum flash performance, set to 0b11.

[3] For maximum flash performance, set to 0b110.

[4] For maximum flash performance, set to 0b1.

[5] This setting allows for 100 MHz system clock with 2% frequency modulation.

[6] This setting allows for 130 MHz system clock with 2% frequency modulation.

13.3.2.9 Flash Bus Interface Unit Access Protection Register (FLASH_BIUAPR)

The FLASH_BIUAPR controls access protection for the flash from masters on the crossbar switch. Use a 32-bit write operation only to this register.

Address: Base (0xC3F8_8000) + 0x0020 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	1	1	1	1	1	1	M4AP		M3AP		M2AP		M1AP		M0AP	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 13-13. Flash Bus Interface Unit Access Protection Register (FLASH_BIUAPR)

Table 13-16. FLASH_BIUAPR Field Descriptions

Field	Description
0–21	Reserved. Reads/Writes have no effect.
22–31 M*n*AP [0:1]	Master *n* access protection. Controls whether read and write accesses to the flash are allowed based on the master ID of a requesting master. These fields are initialized by hardware reset. Refer to Table 7-3. 00 No accesses can be performed by this master 01 Only read accesses can be performed by this master 10 Only write accesses can be performed by this master 11 Both read and write accesses can be performed by this master These fields are identified as follows: M0AP= MCU core M1AP= Nexus M2AP= eDMA M3AP= EBI M4AP= FEC

13.4 Functional Description

13.4.1 Flash Bus Interface Unit (FBIU)

The Flash BIU interfaces between the system bus and the flash memory interface unit and generates read and write enables, the flash array address, write size, and write data as inputs to the flash memory interface unit (MI). The Flash BIU captures read data from the MI and drives it on the system bus. Up to two lines (1 line is a 256-bit width) of data or instructions are buffered by the Flash BIU. Lines can be prefetched in advance of being requested by the system bus interface, allowing single-cycle read data responses on buffer hits.

Several prefetch control algorithms are available for controlling line read buffer fills. Prefetch triggering can be restricted to instruction accesses only, data accesses only, or can be unrestricted. Prefetch triggering can also be controlled on a per-master basis.

Access protections can be applied on a per-master basis for both reads and writes to support security and privilege mechanisms.

13.4.1.1 FBIU Basic Interface Protocol

The Flash BIU interfaces to the flash array by driving addresses and read or write enable signals to the flash memory interface unit. The access time of the flash is determined by the settings of the wait state control bits in the FLASH_BIUCR, as well as the pipelining of addresses.

The Flash BIU also has the capability of extending the normal system bus access timing by inserting additional primary (initial access) wait states for reads and burst reads. This capability is provided to allow emulation of other memories which have different access time characteristics.

13.4.1.2 FBIU Access Protections

The Flash BIU provides hardware configurable access protections for both read and write cycles from masters. It allows restriction of read and write requests on a per-master basis. The FBIU also supports software configurable access protections. Detection of a protection violation results in an error response from the Flash BIU to the system bus.

13.4.1.3 Flash Read Cycles—Buffer Miss

Read data is normally stored in the least-recently updated line read buffer in parallel with the requested data being forwarded to the system bus.

13.4.1.4 Flash Read Cycles—Buffer Hit

Single clock read responses to the system bus are possible with the Flash BIU when the requested read access is buffered.

13.4.1.5 Flash Access Pipelining

Accesses to the flash array can be pipelined by driving a subsequent access address and control signals while waiting for the current access to complete. Pipelined access requests are always run to completion and are not aborted by the Flash BIU. Request pipelining allows for improved performance by reducing the access latency seen by the system bus master. Access pipelining can be applied to both read and write cycles by the flash array.

13.4.1.6 Flash Error Response Operation

The flash array can terminate a requested access with an error. This can occur due to an uncorrectable ECC error, an access control violation, or because of improper access sequencing during program/erase operations. When an error response is received, the Flash BIU marks a line read buffer as invalid. An error response can be signaled on read or write operations.

13.4.1.7 FBIU Line Read Buffers and Prefetch Operation

The Flash BIU contains a pair of 256-bit line read buffers which are used to hold data read from the flash array. Each buffer operates independently and is filled using a single array access. The buffers are used for both prefetch and normal demand fetches.

Prefetch triggering is controllable on a per-master and access-type basis. Bus masters can be enabled or disabled from triggering prefetches, and triggering can be further restricted based on whether a read access is for instruction or data and whether or not it is a burst access. A read access to the Flash BIU can trigger a prefetch to the next sequential line of array data on the cycle following the request. The access address is incremented to the next-higher 32-byte boundary, and a flash array prefetch is initiated if the data is not already resident in a line read buffer. Prefetched data is loaded into the buffer which is not being used to satisfy the original request.

Buffers can be in one of six states, listed here in prioritized order:

- Invalid—the buffer contains no valid data.
- Used—the buffer contains valid data which has been provided to satisfy a burst type read.
- Valid—the buffer contains valid data which has been provided to satisfy a single type read.
- Prefetched—the buffer contains valid data which has been prefetched to satisfy a potential future access.
- Busy—the buffer is currently being used to satisfy a burst read.
- Busy fill—the buffer has been allocated to receive data from the flash array, and the array access is still in progress.

Selection of a buffer to fill on a buffer miss is based on this prioritized order beginning with the first item (invalid). Selection of a buffer to fill on a triggered prefetch is based on the buffer which is not being used to satisfy the triggering access.

The consequences of this replacement policy are that buffers are selected for filling on a ‘least recently updated’ basis when prefetching, and on a ‘most recently emptied’ basis for demand fetches (that is, a fetch which is actually satisfying a current system bus access). This policy allows for prefetched data to remain valid when non-prefetch enabled bus masters are granted flash access.

Several algorithms are available for prefetch control which trade off performance for power. They are described in Section 13.3.2.8, “Flash Bus Interface Unit Control Register (FLASH_BIUCR).” More aggressive prefetching increases power due to the number of wasted (discarded) prefetches, but can increase performance by lowering average read latency.

13.4.1.8 FBIU Instruction/Data Prefetch Triggering

Prefetch triggering can be enabled for instruction reads. Triggering can be enabled for all instruction reads or only for instruction burst reads. Prefetch triggering can be enabled for data reads. Triggering can be enabled for all data reads or only for data burst reads. Prefetches are not triggered by write cycles.

13.4.1.9 FBIU Per-Master Prefetch Triggering

Prefetch triggering can be controlled for individual bus masters. System bus accesses indicate the requesting master.

13.4.1.10 FBIU Buffer Invalidation

The line read buffers can be invalidated under hardware and software control. Buffers are automatically invalidated whenever the buffers are turned on or off, or at the beginning of a program or erase operation.

NOTE

Disable prefetching before invalidating the buffers. This includes starting a program or erase operation, or turning on and off the buffers.

13.4.1.11 Flash Wait-state Emulation

Emulation of other memory array timings are supported by the Flash BIU. This functionality can be useful to maintain the access timing for blocks of memory which were used to overlay flash blocks for the purpose of system calibration or tuning during code development.

The Flash BIU inserts additional primary wait states according to user-programmable values for primary wait states. When these inputs are non-zero, additional cycles are added to system bus transfers. Normal system bus termination is extended. In addition, no line read buffer prefetches are initiated, and buffer hits are ignored.

13.4.2 Flash Memory Array: User Mode

In user (normal) operating mode the flash module can be read, written (register writes and interlock writes), programmed, or erased. The following subsections define all actions that can be performed in normal operating mode. The registers mentioned in these sections are detailed in Section 13.3.2, “Register Descriptions.”

13.4.2.1 Flash Read and Write

The default state of the flash module is read. The main and shadow address space can be read only in the read state. The module configuration register (FLASH_MCR) is always available for read. The flash module enters the read state on reset. The flash module is in the read state under four sets of conditions:

- The read state is active when FLASH_MCR[STOP] = 0 (user mode read).
- The read state is active when FLASH_MCR[PGM] = 1 and/or FLASH_MCR[ERS] = 1 and high voltage operation is ongoing (read while write).

NOTE

Reads done to the partitions being operated on (either erased or programmed) result in an errors and the FLASH_MCR[RWE] bit is set.

- The read state is active when FLASH_MCR[PGM] = 1 and FLASH_MCR[PSUS] = 1 in the MCR. (Program suspend).
- The read state is active when FLASH_MCR[ERS] = 1 and FLASH_MCR[ESUS] = 1 and FLASH_MCR[PGM] = 0 in the MCR (erase suspend).

NOTE

Flash core reads are done through the BIU. In many cases the BIU does page buffering to allow sequential reads to be done with higher performance. This can create a data coherency issue that must be handled with software. Data coherency can be an issue after a program or erase operation, as well as shadow row operations.

In flash normal operating mode, registers can be written and the flash array can be written to do interlock writes.

Reads attempted to invalid locations result in indeterminate data. Invalid locations occur when addressing is done to blocks that do not exist in non 2^n array sizes.

Interlock writes attempted to invalid locations (due to blocks that do not exist in non 2^n array sizes), result in an interlock occurring, but attempts to program or erase these blocks do not occur since they are forced to be locked.

Refer to Section 13.3.2.2, “Low/Mid Address Space Block Locking Register (FLASH_LMLR), Section 13.3.2.3, “High Address Space Block Locking Register (FLASH_HLR)” and Section 13.3.2.4, “Secondary Low/Mid Address Space Block Locking Register (FLASH_SLMLR)” for more information.

13.4.2.2 Read While Write (RWW)

The flash core is divided into partitions. Partitions are always comprised of two or more blocks. Partitions are used to determine read while write (RWW) groupings. While a write (program or erase) is being done within a given partition, a read can be simultaneously executed to any other partition. Partitions are listed in Table 13-4. Each partition in high address space comprises of two 128-KB blocks. The shadow block has unique RWW restrictions described in Section 13.4.2.5, “Flash Shadow Block.”

The flash core is also divided into blocks to implement independent erase or program protection. The shadow block exists outside the normal address space and is programmed, erased and read independently of the other blocks. The shadow block is included to support systems that require NVM for security or system initialization information.

A software mechanism is provided to independently lock or unlock each block in high-, mid-, and low-address space against program and erase.

13.4.2.3 Flash Programming

Programming changes the value stored in an array bit from logic 1 to logic 0 only. Programming cannot change a stored logic 0 to a logic 1. Addresses in locked/disabled blocks cannot be programmed. The user can program the values in any or all of eight words within a page in a single program sequence. Word addresses are selected using bits 4:2 of the page-bound word.

Whenever a program operation occurs, ECC bits are programmed. ECC is handled on a 64-bit boundary. Thus, if only 1 word in any given 64-bit ECC segment is programmed, do not program the adjoining word (in that segment) because the ECC calculation has already completed for that 64-bit segment. Attempts to program the adjoining word results in an operation failure. All programming operations must be from 64 bits to 256 bits, and be 64-bit aligned. The programming operation must completely fill the selected ECC segments within the page.

The program operation consists of the following sequence of events:

1. Change the value in the FLASH_MCR[PGM] bit from a 0 to a 1.

NOTE

Ensure the block that contains the address to be programmed is unlocked. Refer to Section 13.3.2.2, “Low/Mid Address Space Block Locking Register (FLASH_LMLR), Section 13.3.2.3, “High Address Space Block Locking Register (FLASH_HLR)” and Section 13.3.2.4, “Secondary Low/Mid Address Space Block Locking Register (FLASH_SLMLR)” for more information.

2. Write the first address to be programmed in the flash module with the program data. This write is referred to as a program data interlock write. An interlock write can either be an aligned-word or doubleword.
3. If more than 1 word or doubleword is to be programmed, write each additional address in the page with data to be programmed. This is referred to as a program data write. All unwritten data words default to 0xFFFF FFFF.
4. Write a logic 1 to the FLASH_MCR[EHV] bit to start the internal program sequence or skip to step 9 to terminate.
5. Wait until the FLASH_MCR[DONE] bit goes high.
6. Confirm FLASH_MCR[PEG] = 1.
7. Write a logic 0 to the FLASH_MCR[EHV] bit.
8. If more addresses are to be programmed, return to step 2.
9. Write a logic 0 to the FLASH_MCR[PGM] bit to terminate the program sequence.

The program sequence is presented graphically in Figure 13-14. The program suspend operation detailed in Figure 13-14 is discussed in Section 13.4.2.3.2, “Flash Program Suspend/Resume.”

The first write after a program is initiated determines the page address to be programmed. The program can be initiated with the 0 to 1 transition of the FLASH_MCR[PGM] bit or by clearing the FLASH_MCR[EHV] bit at the end of a previous program. This first write is referred to as an interlock write. If the program is not an erase-suspended program, the interlock write determines if the shadow or normal array space is programmed and causes FLASH_MCR[PEAS] to be set/cleared.

In the case of an erase-suspended program, the value in FLASH_MCR[PEAS], is retained from the erase.

An interlock write must be performed before setting FLASH_MCR[EHV]. The user can terminate a program sequence by clearing FLASH_MCR[PGM] prior to setting FLASH_MCR[EHV].

If multiple writes are done to the same location the data for the last write is used in programming.

While FLASH_MCR[DONE] is low, FLASH_MCR[EHV] is high and FLASH_MCR[PSUS] is low the user can clear FLASH_MCR[EHV], resulting in a program abort. A program abort forces the module to step 8 of the program sequence. An aborted program results in FLASH_MCR[PEG] being set low, indicating a failed operation. The data space being operated on before the abort contains indeterminate data. The user cannot abort a program sequence while in program suspend.

WARNING

Aborting a program operation leaves the flash core addresses being programmed in an indeterminate data state. This can be recovered by executing an erase on the affected blocks.

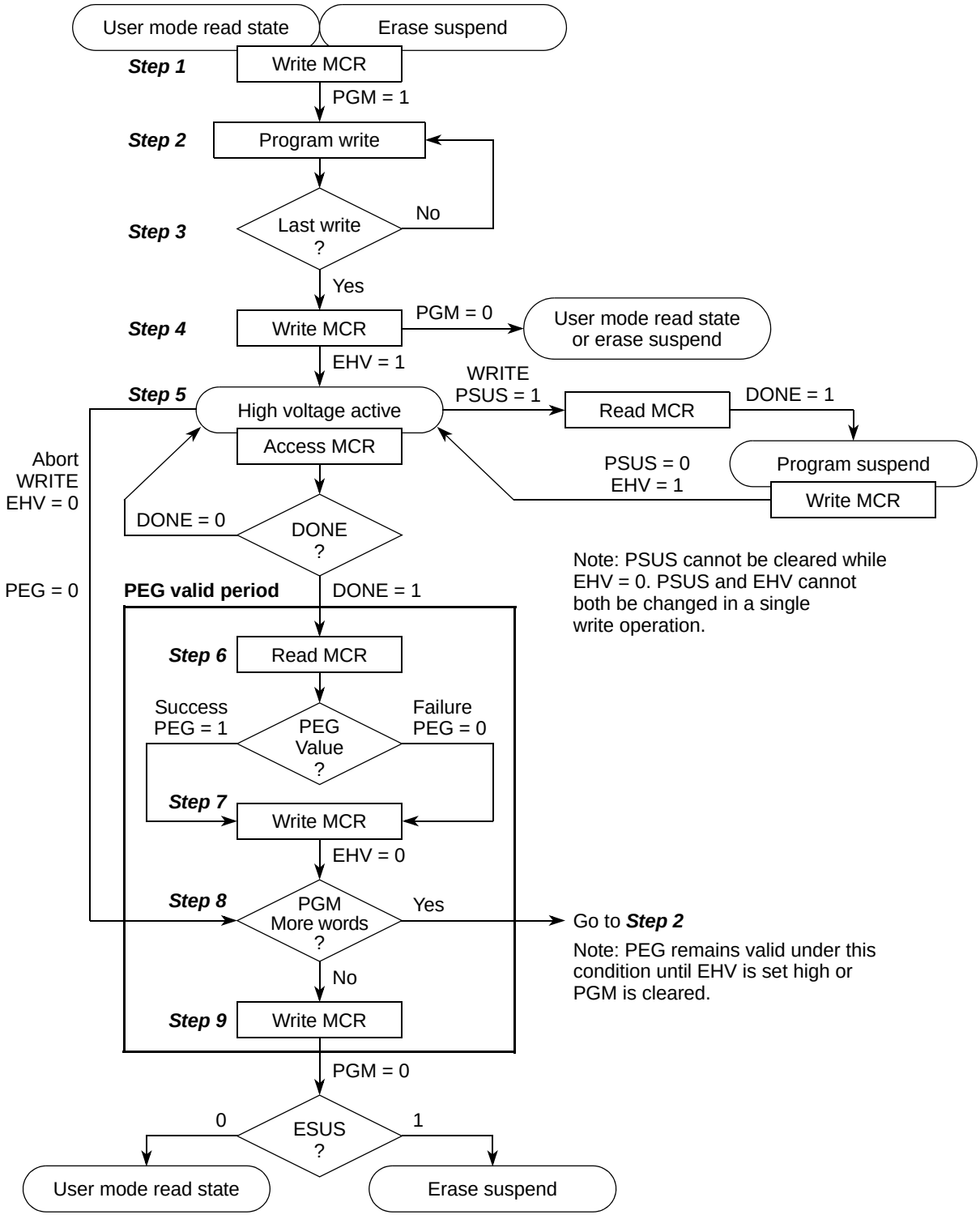


Figure 13-14. Program Sequence

13.4.2.3.1 Software Locking

A software mechanism is provided to independently lock/unlock each high, mid, and low address space against program and erase.

Software Locking is done through the FLASH_LMLR (low/mid address space block locking register), FLASH_SLMLR (secondary low/mid address space block locking register), or FLASH_HLR (high address space block locking register). These can be written through register writes, and can be read through register reads.

When the program/erase operations are enabled through hardware, software locks are enforced through doing register writes.

13.4.2.3.2 Flash Program Suspend/Resume

The program sequence can be suspended to allow read access to the flash core. It is not possible to erase or program during a program suspend. Do not attempt interlock writes during program suspend.

A program suspend can be initiated by changing the value of the FLASH_MCR[PSUS] bit from a 0 to a 1. FLASH_MCR[PSUS] can be set high at any time when FLASH_MCR[PGM] and FLASH_MCR[EHV] are high. A 0 to 1 transition of FLASH_MCR[PSUS] causes the flash module to start the sequence to enter program suspend, which is a read state. The module is not suspended until FLASH_MCR[DONE] = 1. At this time, flash core reads can be attempted. After it is suspended, the flash core can only be read. Reads to the blocks being programmed/erased return indeterminate data.

The program sequence is resumed by writing a logic 0 to FLASH_MCR[PSUS]. FLASH_MCR[EHV] must be set to a 1 before clearing FLASH_MCR[PSUS] to resume operation. When the operation resumes, the flash module continues the program sequence from one of a set of predefined points. This can extend the time required for the program operation.

13.4.2.4 Flash Erase

Erase changes the value stored in all bits of the selected blocks to logic 1. Locked or disabled blocks cannot be erased. If multiple blocks are selected for erase during an erase sequence, the blocks are erased sequentially starting with the lowest numbered block and terminating with the highest. Aborting an erase operation leaves the flash core blocks being erased in an indeterminate data state. This can be recovered by executing an erase on the affected blocks.

The erase sequence consists of the following sequence of events:

1. Change the value in the FLASH_MCR[ERS] bit from 0 to a 1.
2. Select the block, or blocks to be erased by writing ones to the appropriate registers in FLASH_LMSR or FLASH_HSR. If the shadow row is to be erased, this step can be skipped, and FLASH_LMSR and FLASH_HSR are ignored. For shadow row erase, refer to section Section 13.4.2.5, “Flash Shadow Block” for more information.

NOTE

Lock and Select are independent. If a block is selected and locked, no erase occurs. Refer to Section 13.3.2.2, "Low/Mid Address Space Block Locking Register (FLASH_LMLR), Section 13.3.2.3, "High Address Space Block Locking Register (FLASH_HLR)" and Section 13.3.2.4, "Secondary Low/Mid Address Space Block Locking Register (FLASH_SLMLR)" for more information.

3. Write to any address in flash. This is referred to as an erase interlock write.
4. Write a logic 1 to the FLASH_MCR[EHV] bit to start an internal erase sequence or skip to step 9 to terminate.
5. Wait until the FLASH_MCR[DONE] bit goes high.
6. Confirm FLASH_MCR[PEG] = 1.
7. Write a logic 0 to the FLASH_MCR[EHV] bit.
8. If more blocks are to be erased, return to step 2.
9. Write a logic 0 to the FLASH_MCR[ERS] bit to terminate the erase.

The erase sequence is presented graphically in Figure 13-15. The erase suspend operation detailed in Figure 13-15 is discussed in section Section 13.4.2.4.1, "Flash Erase Suspend/Resume."

After settingFLASH_MCR[ERS], one write, referred to as an interlock write, must be performed before FLASH_MCR[EHV] can be set to a 1. Data words written during erase sequence interlock writes are ignored. The user can terminate the erase sequence by clearing FLASH_MCR[ERS] before setting FLASH_MCR[EHV].

An erase operation can be aborted by clearing FLASH_MCR[EHV] assuming FLASH_MCR[DONE] is low, FLASH_MCR[EHV] is high and FLASH_MCR[ESUS] is low. An erase abort forces the module to step 8 of the erase sequence. An aborted erase results in FLASH_MCR[PEG] being set low, indicating a failed operation. The blocks being operated on before the abort contain indeterminate data. The user cannot abort an erase sequence while in erase suspend.

WARNING

Aborting an erase operation leaves the flash core blocks being erased in an indeterminate data state. This can be recovered by executing an erase on the affected blocks.

13.4.2.4.1 Flash Erase Suspend/Resume

The erase sequence can be suspended to allow read access to the flash core. The erase sequence can also be suspended to program (erase-suspended program) the flash core. A program started during erase suspend can in turn be suspended. Only one erase suspend and one program suspend are allowed at a time during an operation. It is not possible to erase during an erase suspend, or program during a program suspend. During suspend, all reads to flash core locations targeted for program and blocks targeted for erase return indeterminate data. Programming locations in blocks targeted for erase during erase-suspended program can result in corrupted data.

An erase suspend operation is initiated by setting the FLASH_MCR[ESUS] bit. FLASH_MCR[ESUS] can be set to a 1 at any time when FLASH_MCR[ERS] and FLASH_MCR[EHV] are high and FLASH_MCR[PGM] is low. A 0 to 1 transition of FLASH_MCR[ESUS] causes the flash module to start the sequence which places it in erase suspend. The user must wait until FLASH_MCR[DONE] = 1 before the module is suspended and further actions are attempted. After it is suspended, the array can be read or a program sequence can be initiated (erase-suspended program). Before initiating a program sequence the user must first clear FLASH_MCR[EHV]. If a program sequence is initiated the value of the FLASH_MCR[PEAS] is not reset. These values are fixed at the time of the first interlock of the erase. Flash core reads while FLASH_MCR[ESUS] = 1 from the blocks being erased return indeterminate data.

The erase operation is resumed by clearing the FLASH_MCR[ESUS] bit. The flash continues the erase sequence from one of a set of predefined points. This can extend the time required for the erase operation.

WARNING

In an erase-suspended program, programming flash locations in blocks which were being operated on in the erase can corrupt flash core data.

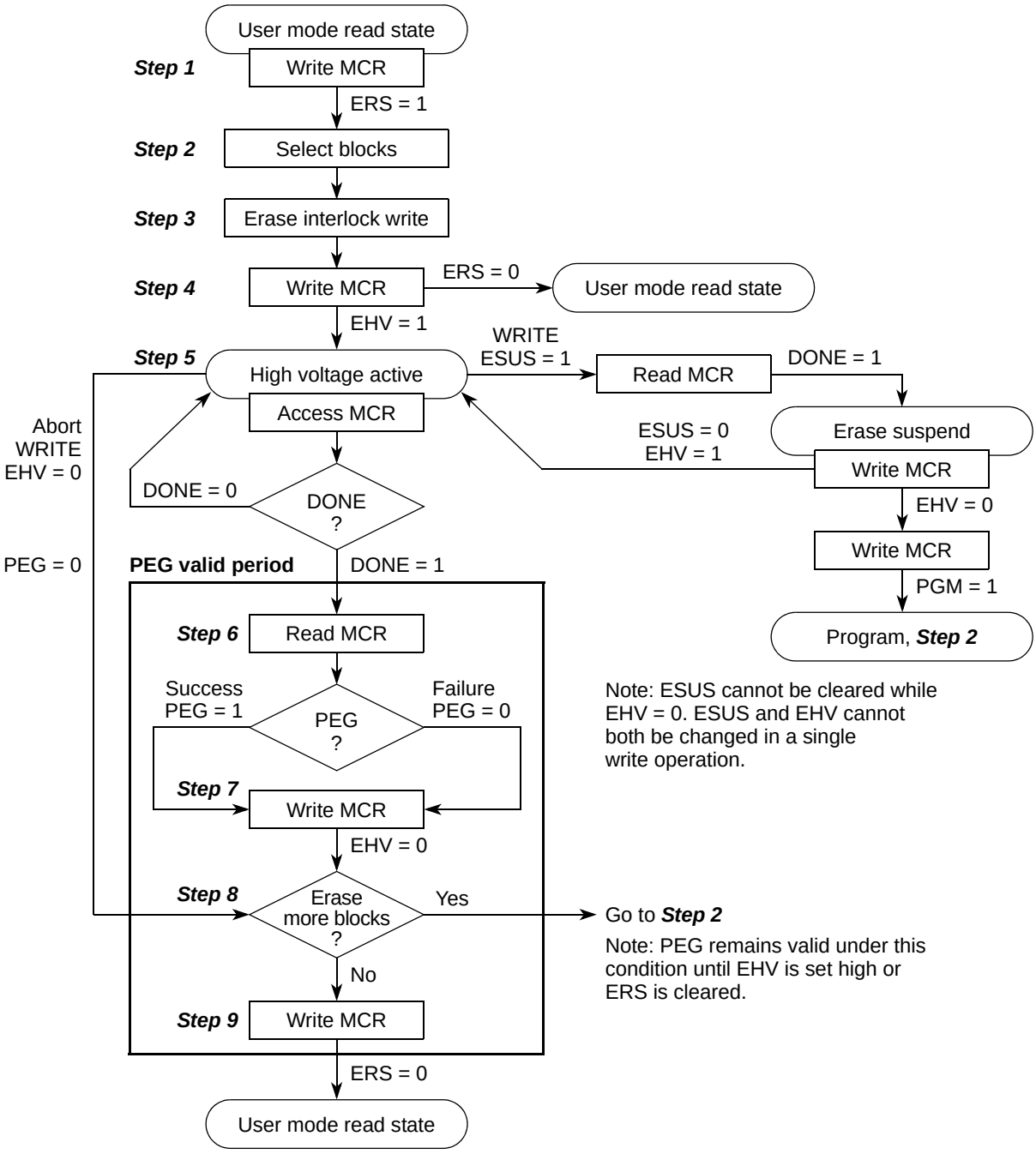


Figure 13-15. Erase Sequence

13.4.2.5 Flash Shadow Block

The flash shadow block is a memory-mapped block in the flash memory map. Program and erase of the shadow block are enabled only when FLASH_MCR[PEAS] = 1. After the user has begun an erase operation on the shadow block, the operation cannot be suspended to program the main address space and vice-versa. The user must terminate the shadow erase operation to program or erase the main address space.

NOTE

If an erase of user space is requested, and a suspend is done with attempts to erase suspend program shadow space, this attempted program is directed to user space as dictated by the state of FLASH_MCR[PEAS]. Likewise an attempted erase suspended program of user space, while the shadow space is being erased, is directed to shadow space as dictated by the state of FLASH_MCR[PEAS].

The shadow block cannot utilize the RWW feature. After an operation is started in the shadow block, a read cannot be done to the shadow block, or any other block. Likewise, after an operation is started in a block in low/mid/high address space, a read cannot be done in the shadow block.

The shadow block contains information on how the lock registers are reset. The first and second words can be used for reset configuration words. All other words can be used for user defined functions or other configuration words.

The shadow block can be locked/unlocked against program or erase by using the FLASH_LMLR or FLASH_SLMLR discussed in Section 13.3.2, “Register Descriptions.”

Programming of the shadow row has similar restrictions to programming the array in terms of how ECC is calculated. Refer to Section 13.4.2.3, “Flash Programming” for more information. Only one program is allowed per 64 bit ECC segment between erases. Erase of the shadow row is done similarly as an array erase. Refer to Section 13.4.2.4, “Flash Erase” for more information.

13.4.2.6 Censorship

Censorship logic disables access to internal flash based on the censorship control word value and the BOOTCFG[0:1] bits in the SIU_RSR. This prevents modification of the FLASH_BIUAPR bitfields associated with all masters except the core based on the censorship control word value, the BOOTCFG[0:1] bits in the SIU_RSR, and the EXTM bit in the EBI_MCR. Also, censorship logic sets the boot default value to external-with-external-master access disabled based on the value of the censorship control word and a TCU input signal.

13.4.2.6.1 Censorship Control Word

The censorship control word is a 32-bit value located at the base address of the shadow row plus 0x1E0. The flash module latches the value of the control word prior to the negation of system reset. Censorship logic uses the value latched in the flash module to disable access to internal flash, disable the NDI, prevent modification of the FLASH_BIUAPR bitfields, and/or set the boot default value.

13.4.2.6.2 Flash Disable

Censorship logic disables read and write access to internal flash according to the logic presented in Table 13-17.

Table 13-17 shows the encoding of the BOOTCFG signals in conjunction with the value stored in the censorship word in the shadow row of internal flash memory. The table also shows: the name of the boot mode; whether the internal flash memory is enabled or disabled; whether the Nexus port is enabled or disabled; whether the password downloaded in serial boot mode is compared with a fixed ‘public’ password or compared to a user programmable flash password.

Table 13-17. Flash Access Disable Logic

BOOTCFG[1] [0:1]	Censorship Control 0x00FF_FDE0 (Upper Half)	Serial Boot Control 0x00FF_FDE2 (Lower Half)	Boot Mode Name	Internal Flash State	Nexus State[2]	Serial Password
00	!0x55AA	Don't care	Internal–Censored	Enabled	Disabled	Flash
	0x55AA		Internal–Public	Enabled	Enabled	Public
01	Don't care	0x55AA	Serial–Flash password	Enabled	Disabled	Flash
		!0x55AA	Serial–Public password	Disabled	Enabled	Public
10	!0x55AA	Don't care	External–No Arbitration–Censored	Disabled	Enabled	Public
	0x55AA		External–No Arbitration–Public	Enabled	Enabled	Public
11	!0x55AA	Don't care	External–External Arbitration–Censored	Disabled	Enabled	Public
	0x55AA		External–External Arbitration–Public	Enabled	Enabled	Public
’!’ =’NOT’ means any value other than the value specified						

1 BOOTCFG[0:1] bits are located in the SIU_RSR.

2 The Nexus port controller is held in reset when in censored mode.

The FBIU returns a bus error if an access is attempted while flash access is disabled. Flash access is any read, write or execute access.

13.4.2.6.3 FLASH_BIUAPR Modification

Censorship logic prevents modification of the access protection register (FLASH_BIUAPR) bit fields associated with all masters except the core according to the logic presented in Table 13-18.

Table 13-18. PFBAPR Modification Logic

BOOTCFG[1]		Censorship Control Word		EXTM[2]	PFBAPR Bitfields Writable
[0]	[1]	Upper Half	Lower Half		
0	0	0x55AA	0xXXXX	0	Yes
0	0	!0x55AA	0xXXXX	0	Yes
1	0	0x55AA	0xXXXX	0	Yes
1	0	!0x55AA	0xXXXX	0	Yes
1	1	0x55AA	0xXXXX	0	Yes
1	1	!0x55AA	0xXXXX	0	Yes
0	1	0xXXXX	0x55AA	0	Yes
0	1	0xXXXX	!0x55AA	0	Yes
0	0	0x55AA	0xXXXX	1	Yes
0	0	!0x55AA	0xXXXX	1	No
1	0	0x55AA	0xXXXX	1	Yes
1	0	!0x55AA	0xXXXX	1	No
1	1	0x55AA	0xXXXX	1	Yes
1	1	!0x55AA	0xXXXX	1	No
0	1	0xXXXX	0x55AA	1	No
0	1	0xXXXX	!0x55AA	1	No

1 BOOTCFG[0:1] bits are located in the SIU_RSR.

2 EXTM bit is located in the EBI_MCR.

13.4.2.6.4 External Boot Default

The SIU latches the boot default value in the SIU_RSR BOOTCFG[0:1] bits if and only if $\overline{\text{RSTCFG}}$ is negated. Censorship logic sets the boot default value before the SIU latches the value to external-with-external-master access disabled (EXTM = 0) if the lower half of the censorship control word equals 0xFFFF or 0x0000. Otherwise, censorship logic sets the boot default value to internal flash.

13.4.3 Flash Memory Array: Stop Mode

Stop mode is entered by setting the FLASH_MCR[STOP] bit. The FLASH_MCR[STOP] bit cannot be written when FLASH_MCR[PGM] = 1 or FLASH_MCR[ERS] = 1. In stop mode all DC current sources in the flash module are disabled. Stop mode is exited by clearing the FLASH_MCR[STOP] bit.

Accessing the flash memory array when STOP is asserted results in an error response from the flash BIU to the system bus. Memory array accesses must not be attempted until the flash transitions out of stop mode.

13.4.4 Flash Memory Array: Reset

A reset is the highest priority operation for the flash and terminates all other operations.

The flash uses reset to initialize register and status bits to their default reset values. If the flash is executing a program or erase operation and a reset is issued, the operation is aborted and the flash disables the high voltage logic without damage to the high voltage circuits. Reset aborts all operations and forces the flash into normal operating mode ready to receive accesses. FLASH_MCR[DONE] is set to 1 at the exit of reset.

After reset is negated, register accesses can be performed, although registers that require updating from shadow information, or other inputs, cannot read updated values until flash exits reset. FLASH_MCR[DONE] can be polled to determine if reset has been exited.

Chapter 14
Internal Static RAM (SRAM)

14.1 Introduction

The SRAM provides KB of general-purpose system SRAM. The first 32-KB of SRAM is powered by a separate power supply pin for standby operation. Figure 14-1 shows the internal SRAM block diagram.

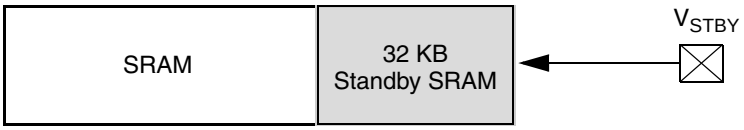


Figure 14-1. Internal SRAM Block Diagram

The SRAM controller has these features:

- Read/write accesses can map to SRAM from any master
- 32 KB with a separate power source for standby operation
- Byte, halfword, word, and doubleword addressable
- Single-bit correction and double-bit error detection

14.2 SRAM Operating Modes

Table 14-1 lists and describes the SRAM operating modes.

Table 14-1. SRAM Operating Modes

Mode	Description
Normal (functional)	Allows reads and writes of SRAM.
Standby	Preserves the 32 KB of standby memory when the 1.5 V power drops below the level of V_{STBY}. Updates to standby SRAM are inhibited during system reset or during standby mode.

14.3 External Signal Description

The external signal for SRAM is the V_{STBY} RAM power supply. If the standby feature of the SRAM is not used, tie the V_{STBY} pin to V_{SS}.

14.4 Register Memory Map

The SRAM occupies 128 KB of memory starting at the base address as shown in Table 14-2.

Table 14-2. SRAM Memory Map

Address	Register Name	Register Description	Size
Base (0x4000_0000)	—	SRAM powered by V_{STBY}	32 KB
Base + 0x8000	—	96-KB RAM	96 KB

The internal SRAM has no registers. Registers for the SRAM ECC are located in the ECSM. Refer to Chapter 8, "Error Correction Status Module (ECSM)," for more information.

14.5 Functional Description

ECC checks are performed during the read portion of an SRAM ECC read/write (R/W) operation, and ECC calculations are performed during the write portion of a read/write (R/W) operation. Because the ECC bits can contain random data after the device is powered on, you must initialize the SRAM by executing 64-bit write instructions to the entire SRAM. For more information, refer to Section 14.7, "Initialization and Application Information."

14.6 SRAM ECC Mechanism

The SRAM ECC detects the following conditions and produces the following results:

- Detects and corrects all 1-bit errors
- Detects and flags all 2-bit errors as non-correctable errors
- Detects 72-bit reads (64-bit data bus plus the 8-bit ECC) that return all zeros or all ones, asserts an error indicator on the bus cycle, and sets the error flag

SRAM does not detect all errors greater than 2 bits.

Internal SRAM write operations are performed on the following byte boundaries:

- 1 byte (0:7 bits)
- 2 bytes (0:15 bits)
- 4 bytes or 1 word (0:31 bits)
- 8 bytes or 2 words (0:63 bits)

If the entire 64 data bits are written to SRAM, no read operation is performed and the ECC is calculated across the 64-bit data bus. The 8-bit ECC is appended to the data segment and written to SRAM.

If the write operation is less than the entire 64-bit data width (1-, 2-, or 4-byte segment), the following occurs:

1. The ECC mechanism checks the entire 64-bit data bus for errors, detecting and either correcting or flagging errors.
2. The write data bytes (1-, 2-, or 4-byte segment) are merged with the corrected 64 bits on the data bus.

3. The ECC is then calculated on the resulting 64 bits formed in the previous step.
4. The 8-bit ECC result is appended to the 64 bits from the data bus, and the 72-bit value is then written to SRAM.

14.6.1 Access Timing

The system bus is a two-stage pipelined bus, which makes the timing of any access dependent on the access during the previous clock. Table 14-3 lists the various combinations of read and write operations to SRAM and the number of wait states used for the each operation. The table columns contain the following information:

Current operation	Lists the type of SRAM operation executing currently
Previous operation	Lists the valid types of SRAM operations that can precede the current SRAM operation (valid operation during the preceding clock)
Wait states	Lists the number of wait states (bus clocks) the operation requires which depends on the combination of the current and previous operation

Table 14-3. Number of Wait States Required for SRAM Operations

	Current Operation	Previous Operation	Number of Wait States Required
Read Operation	Read	Idle	1
		Pipelined read	
		Burst read	
		64-bit write	2
		8-, 16-, or 32-bit write	0 (read from the same address)
			1 (read from a different address)
	Pipelined read	Read	0
	Burst read	Idle	1,0,0,0
		Pipelined read	
		Burst read	
		64-bit write	2,0,0,0
		8-, 16-, or 32-bit write	0,0,0,0 (read from the same address)
			1,0,0,0 (read from a different address)

Table 14-3. Number of Wait States Required for SRAM Operations (continued)

	Current Operation	Previous Operation	Number of Wait States Required
Write Operation	8-, 16-, or 32-bit write	Idle	1
		Read	
		Pipelined 8-, 16-, or 32-bit write	2
		64-bit write	
		8-, 16-, or 32-bit write	0 (write to the same address)
	Pipelined 8-, 16-, or 32-bit write	8-, 16-, or 32-bit write	0
	64-bit write	Idle	0
		64-bit write	
		Read	
	64-bit burst write	Idle	0,0,0,0
		64-bit write	
		Read	

14.6.2 Reset Effects on SRAM Accesses

If a reset event asserts during a read or write operation to SRAM, the completion of that access depends on the cycle at which the reset occurs. Data read from or written to SRAM before the reset event occurred is retained, and no other address locations are accessed or changed.

NOTE

Standby memory can contain the previous data values if a reset occurs while cache is running in copy back mode.

14.7 Initialization and Application Information

To use the SRAM, the ECC must check all bits that require initialization after power on. Use a 64-bit cache-inhibited write to each SRAM location in the application initialization code to initialize the SRAM array. All writes must specify an even number of registers performed on 64-bit word-aligned boundaries. If the write is not the entire 64-bits (8-, 16-, or 32-bits), a read / modify / write operation is generated that checks the ECC value upon the read. Refer to Section 14.6, “SRAM ECC Mechanism.”

NOTE

You *must* initialize SRAM, even if the application does not use ECC reporting.

14.7.1 Example Code

To initialize SRAM correctly, use the store multiple word (**stmw)** instruction to implement 64-bit writes to all SRAM locations. The **stmw** instruction concatenates two 32-bit registers to implement a single 64-bit write.

The following example code illustrates the use of the **stmw** instruction to initialize the SRAM ECC bits.

```
init_RAM:
lis      r11,0x4000       # base address of the SRAM, 64-bit word aligned
ori      r11,r11,0        # not needed for this address but can be for others
li       r12,1024         # loop counter to get all of SRAM;
                          # 128k/4 bytes/32 GPRs = 1024
mtctr    r12
init_ram_loop:
stmw     r0,0(r11)        # write all 32 GPRs to SRAM
addi     r11,r11,128      # inc the ram ptr; 32 GPRs * 4 bytes = 128
bdnz     init_ram_loop    # loop for 128k of SRAM
blr                       # done
```

Chapter 15
Fast Ethernet Controller (FEC)

15.1 Introduction

The fast Ethernet control (FEC) chapter provides a feature-set overview, a functional block diagram, and transceiver connection information for both the 10 and 100 Mbps MII (media independent interface), as well as the 7-wire serial interface. Additionally, detailed descriptions of operation and the programming model are included.

15.1.1 Block Diagram

Figure 15-1 shows the block diagram of the FEC. The FEC is implemented with a combination of hardware and microcode. The off-chip (Ethernet) interfaces are compliant with industry and IEEE® 802.3 standards.

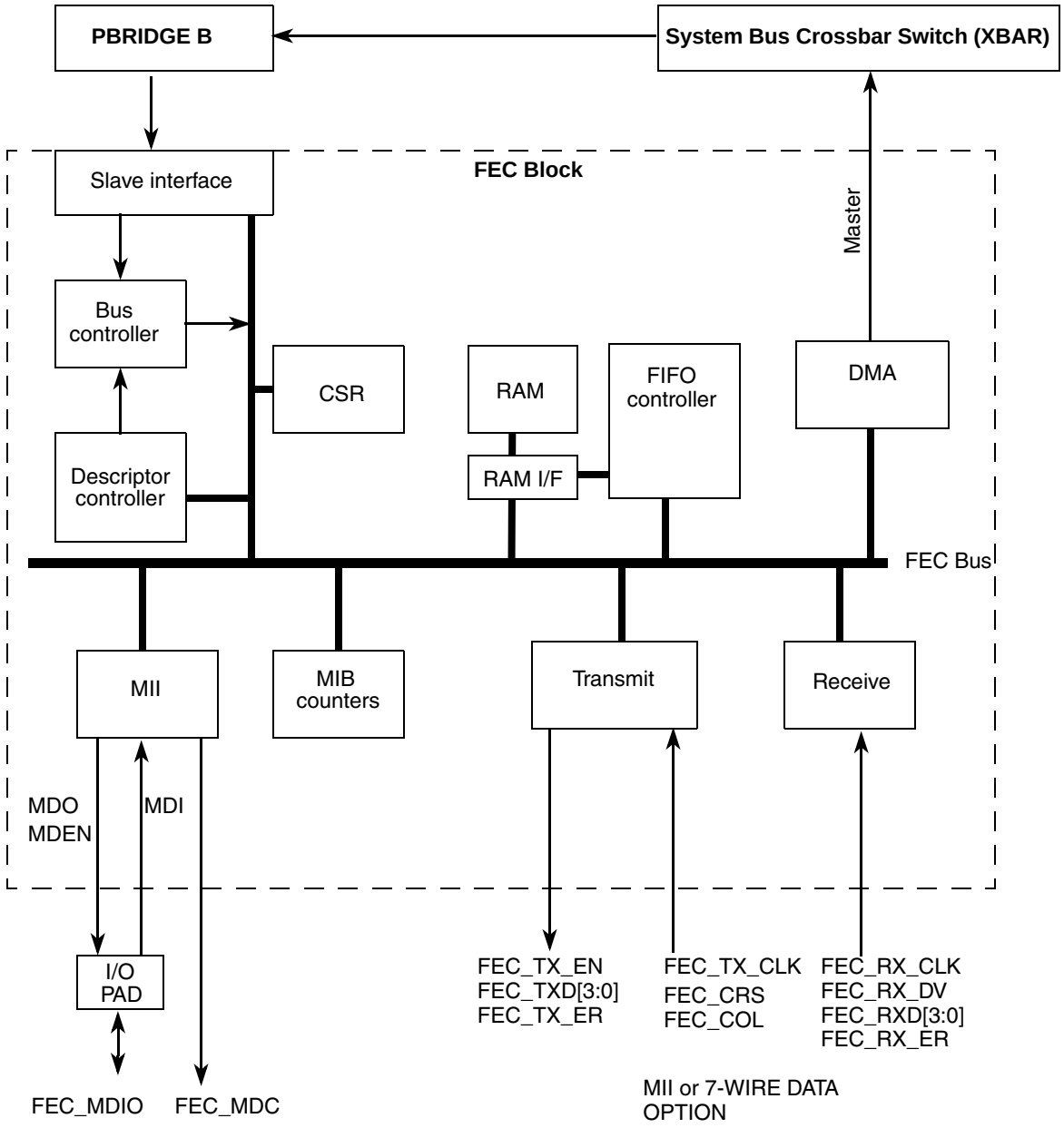


Figure 15-1. FEC Block Diagram

15.1.2 Overview

The Ethernet media access controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE® 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports three different standard MAC-PHY (physical) interfaces for connection to an external Ethernet transceiver. The FEC supports the 10/100 Mbps MII and the 10 Mbps-only 7-wire interface, which uses a subset of the MII signals.

The descriptor controller is RISC-based and provides the following FEC functions:

- Initialization (the internal registers not initialized by the application or hardware)
- High-level control of the DMA channels (initiating DMA transfers)
- Interpreting buffer descriptors
- Address recognition for receive frames
- Random number generation for transmit collision backoff timer

NOTE

DMA references in this section refer to the FEC DMA engine used to transfer FEC data only. It is not related to the DMA controller described in Chapter 9, “Enhanced Direct Memory Access (eDMA).”

The RAM is the focal point of all data flow in the fast Ethernet controller and is divided into transmit and receive FIFOs. The FIFO boundaries are programmable using the FRSR register. Application data flows to/from the DMA block from/to the receive/transmit FIFOs. Transmit data flows from the transmit FIFO into the transmit block and receive data flows from the receive block into the receive FIFO.

You control the FEC by writing, through the slave interface module, to control registers located in each block. The CSR (control and status register) block provides global control (such as Ethernet reset and enable) and interrupt handling registers.

The MII block provides a serial channel for control/status communication with the external physical layer device (transceiver). This serial channel consists of the MDC (management data clock) and MDIO (management data input/output) lines of the MII interface.

The DMA block provides multiple channels allowing transmit data, transmit descriptor, receive data, and receive descriptor accesses to run independently.

The transmit and receive blocks provide the Ethernet MAC functionality (with some assist from microcode).

The message information block (MIB) maintains counters for a variety of network events and statistics. It is not necessary for operation of the FEC but provides valuable counters for network management. The counters supported are the RMON (RFC 1757) Ethernet Statistics group and some of the IEEE® 802.3 counters.

15.1.3 Features

The FEC incorporates the following features:

- Support for three different Ethernet physical interfaces:
  - 100-Mbps IEEE® 802.3 MII
  - 10-Mbps IEEE® 802.3 MII
  - 10-Mbps 7-wire interface (industry standard)
- Built-in FIFO and DMA controller
- IEEE® 802.3 MAC (compliant with IEEE® 802.3 1998 edition)
- Programmable max frame length supports IEEE® 802.1 VLAN tags and priority
- IEEE® 802.3 full duplex flow control
- Support for full-duplex operation (200 Mbps throughput) with a system clock rate of 100 MHz using the external FEC_TX_CLK or FEC_RX_CLK
- Support for half-duplex operation (100 Mbps throughput) with a system clock rate of 50 MHz using the external FEC_TX_CLK or FEC_RX_CLK
- Retransmission from transmit FIFO following a collision (no system bus utilization)
- Automatic internal flushing of the receive FIFO for runts (collision fragments) and address recognition rejects (no system bus utilization)
- Address recognition
  - Frames with a broadcast address can be unconditionally accepted or rejected
  - Exact match for single 48-bit individual (unicast) address
  - Hash (64-bit) check of individual (unicast) addresses
  - Hash (64-bit) check of group (multicast) addresses
  - Promiscuous mode
- RMON and IEEE® statistics
- Interrupts for network activity and error conditions

15.2 Modes of Operation

The primary operational modes are described in this section.

15.2.1 Full and Half Duplex Operation

Use full duplex mode for point-to-point links between switches, or between an end node and a switch. Use half duplex mode for connections between an end node and a repeater, or between repeaters. Select the duplex mode using the TCR[FDEN] bit.

When configured for full duplex mode, flow control can be enabled. See the TCR[RFC_PAUSE] and TCR[TFC_PAUSE] bits, the RCR[FCE] bit, and Section 15.4.10, “Full Duplex Flow Control,” for more details.

Throughputs of 200 Mbps in full duplex operations and 100 Mbps in half-duplex operations can be attained.

15.2.2 Interface Options

The following interface options are supported. A detailed discussion of the interface configurations is provided in Section 15.4.5, “Network Interface Options”.

15.2.2.1 10 Mbps and 100 Mbps MII Interface

MII is the media independent interface defined by the IEEE® 802.3 standard for 10/100 Mbps operation. Configure the MAC-PHY interface to operate in MII mode by asserting RCR[MII_MODE].

The speed of operation is determined by the FEC_TX_CLK and FEC_RX_CLK signals which are driven by the external transceiver. The transceiver auto-negotiates the speed or it is controlled by software via the serial management interface (FEC_MDC and FEC_MDIO signals) to the transceiver. See the MMFR and MSCR register descriptions, as well as the section on the MII, for a description of how to read and write registers in the transceiver using this interface.

15.2.2.2 10 Mpbs 7-Wire Interface Operation

The FEC supports a 7-wire interface as used by many 10 Mbps Ethernet transceivers. The RCR[MII_MODE] bit controls this functionality. If this bit is deasserted, the MII mode is disabled and the 10 Mbps, 7-wire mode is enabled.

15.2.3 Address Recognition Options

The address options supported are promiscuous, broadcast reject, individual address (hash or exact match), and multicast hash match. Address recognition options are discussed in detail in Section 15.4.8, “Ethernet Address Recognition.”

15.2.4 Internal Loopback

Internal loopback mode is selected via RCR[LOOP]. Loopback mode is discussed in detail in Section 15.4.13, “Internal and External Loopback.”

15.3 Programming Model

This section gives an overview of the registers, followed by a description of the buffers.

The FEC is programmed by a combination of control/status registers (CSRs) and buffer descriptors. The CSRs are used for mode control and to extract global status information. The descriptors are used to pass data buffers and related buffer information between the hardware and software.

15.3.1 Top Level Module Memory Map

The FEC implementation requires 1 KB of memory. This is divided into two sections of 512 bytes each:

- Section one contains the control and status registers
- Section two contains event and statistic counters held in the MIB block.

Table 15-1 defines the top level memory map. All accesses to and from the FEC memory map must be via 32-bit accesses. There is no support for accesses other than 32-bit.

Table 15-1. FEC Module Memory Map

Address	Function
Base address FFF4_C000–FFF4_C1FF	Control and status registers
FFF4_C200–FFF4_C3FF	MIB block counters

15.3.2 Detailed Memory Map (Control and Status Registers)

Table 15-2 shows the FEC register memory map with each register address, name, and a brief description. The base address of the FEC registers is 0xFFF4_C000.

NOTE

Some FEC memory locations and bits are not documented. The FEC memory map is from 0xFFF4_C000–0xFFF4_C5FF. The memory and bits are not required for the FEC software driver. They are used mainly by the FEC subblocks for the FEC operation and are visible through the slave interface.

Errant writes to these locations can corrupt FEC operation. Because the FEC is a system bus master, errant writes can corrupt any part of the system memory map. Errant writes to documented FEC memory locations can also result is data corruption.

15.3.3 MIB Block Counters Memory Map

Table 15-2 defines the MIB Counters memory map which defines the locations in the MIB RAM space where hardware-maintained counters reside. These fall in the 0xFFF4_C200–0xFFF4_C3FF address offset range. The counters are divided into two groups.

- RMON counters are included which cover the Ethernet Statistics counters defined in RFC 1757. In addition to the counters defined in the Ethernet Statistics group, a counter is included to count truncated frames as the FEC only supports frame lengths up to 2047 bytes. The RMON counters are implemented independently for transmit and receive to insure accurate network statistics when operating in full duplex mode.
- IEEE® counters are included which support the Mandatory and Recommended counter packages defined in section 5 of ANSI/IEEE® Std. 802.3 (1998 edition). The IEEE® Basic Package objects are supported by the FEC but do not require counters in the MIB block. In addition, some of the

recommended package objects which are supported do not require MIB counters. Counters for transmit and receive full duplex flow control frames are included as well.

Table 15-2. MIB Counter Memory Map Locations

Base Address + Offset [1]	Mnemonic	Description
0x0200	RMON_T_DROP	Count of frames not counted correctly
0x0204	RMON_T_PACKETS	RMON TX packet count
0x0208	RMON_T_BC_PKT	RMON TX broadcast packets
0x020C	RMON_T_MC_PKT	RMON TX multicast packets
0x0210	RMON_T_CRC_ALIGN	RMON TX packets w CRC/align error
0x0214	RMON_T_UNDERSIZE	RMON TX packets < 64 bytes, valid CRC
0x0218	RMON_T_OVERSIZE	RMON TX packets > MAX_FL bytes, valid CRC
0x021C	RMON_T_FRAG	RMON TX packets < 64 bytes, invalid CRC
0x0220	RMON_T_JAB	RMON TX packets > MAX_FL bytes, invalid CRC
0x0224	RMON_T_COL	RMON TX collision count
0x0228	RMON_T_P64	RMON TX 64 byte packets
0x022C	RMON_T_P65TO127	RMON TX 65 to 127 byte packets
0x0230	RMON_T_P128TO255	RMON TX 128 to 255 byte packets
0x0234	RMON_T_P256TO511	RMON TX 256 to 511 byte packets
0x0238	RMON_T_P512TO1023	RMON TX 512 to 1023 byte packets
0x023C	RMON_T_P1024TO2047	RMON TX 1024 to 2047 byte packets
0x0240	RMON_T_P_GTE2048	RMON TX packets with more than 2048 bytes
0x0244	RMON_T_OCTETS	RMON TX octets
0x0248	IEEE_T_DROP	Count of frames not counted correctly
0x024C	IEEE_T_FRAME_OK	Frames transmitted OK
0x0250	IEEE_T_1COL	Frames transmitted with single collision
0x0254	IEEE_T_MCOL	Frames transmitted with multiple collisions
0x0258	IEEE_T_DEF	Frames transmitted after deferral delay
0x025C	IEEE_T_LCOL	Frames transmitted with late collision
0x0260	IEEE_T_EXCOL	Frames transmitted with excessive collisions
0x0264	IEEE_T_MACERR	Frames transmitted with Tx FIFO underrun
0x0268	IEEE_T_CSERR	Frames transmitted with carrier sense error
0x026C	IEEE_T_SQE	Frames transmitted with SQE error
0x0270	IEEE_T_FDXFC	Flow control pause frames transmitted
0x0274	IEEE_T_OCTETS_OK	Octet count for frames transmitted without error

Table 15-2. MIB Counter Memory Map Locations (continued)

Base Address + Offset [1]	Mnemonic	Description
0x0280	RMON_R_DROP	Count of frames not counted correctly
0x0284	RMON_R_PACKETS	RMON RX packet count
0x0288	RMON_R_BC_PKT	RMON RX broadcast packets
0x028C	RMON_R_MC_PKT	RMON RX multicast packets
0x0290	RMON_R_CRC_ALIGN	RMON RX packets with CRC/align error
0x0294	RMON_R_UNDERSIZE	RMON RX packets < 64 bytes, valid CRC
0x0298	RMON_R_OVERSIZE	RMON RX packets > MAX_FL bytes, valid CRC
0x029C	RMON_R_FRAG	RMON RX packets < 64 bytes, invalid CRC
0x02A0	RMON_R_JAB	RMON RX packets > MAX_FL bytes, invalid CRC
0x02A4	—	Reserved
0x02A8	RMON_R_P64	RMON RX 64 byte packets
0x02AC	RMON_R_P65TO127	RMON RX 65 to 127 byte packets
0x02B0	RMON_R_P128TO255	RMON RX 128 to 255 byte packets
0x02B4	RMON_R_P256TO511	RMON RX 256 to 511 byte packets
0x02B8	RMON_R_P512TO1023	RMON RX 512 to 1023 byte packets
0x02BC	RMON_R_P1024TO2047	RMON RX 1024 to 2047 byte packets
0x02C0	RMON_R_P_GTE2048	RMON RX packets with more than 2048 bytes
0x02C4	RMON_R_OCTETS	RMON RX octets
0x02C8	IEEE_R_DROP	Count of frames not counted correctly
0x02CC	IEEE_R_FRAME_OK	Frames received OK
0x02D0	IEEE_R_CRC	Frames received with CRC error
0x02D4	IEEE_R_ALIGN	Frames received with alignment error
0x02D8	IEEE_R_MACERR	Receive FIFO overflow count
0x02DC	IEEE_R_FDXFC	Flow control pause frames received
0x02E0	IEEE_R_OCTETS_OK	Octet count for frames received without error

[1] All accesses to and from the FEC memory map must be 32-bit accesses. There is no support for accesses other than 32-bit.

15.3.4 Registers

15.3.4.1 FEC Burst Optimization Master Control Register (FBOMCR)

Although *not* an FEC register, the FEC burst optimization master control register (FBOMCR) controls FEC burst optimization behavior on the system bus, hence it is described in this section.

FEC registers are described in Section 15.3.4.2.1, "Ethernet Interrupt Event Register (EIR)" through Section 15.3.4.3.4, "Receive Buffer Size Register (EMRBR)."

To increase throughput, the FEC interface to the system bus can accumulate read requests or writes to burst those transfers on the system bus. The FBOMCR determines the XBAR ports for which this bursting is enabled, as well as whether the bursting is for reads, writes, or both. FBOMCR also controls how errors for writes are handled. The FBOMCR address is 0xFFF4_0024, which is the ECSM base address 0xFFF4_0000 plus the offset of 0x0024.

Address: Base + 0x0024 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	FXS BE0	FXS BE1	0	FXS BE3	0	0	FXS BE6	FXS BE7	RBEN	WBEN	ACC ERR	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-2. FEC Burst Optimization Master Control Register (FBOMCR)

Table 15-3 describes the fields and functions of the FEC burst optimization register:

Table 15-3. FBOMCR Field Descriptions

Bits	Name	Description
0–7	FXSBE*n* [0:7]	FXSBE – FEC XBAR slave burst enable. FXSBE*n* enables bursting by the FEC interface to the XBAR slave port controlled by that respective FXSBE*n* bit. If FXSBE*n* is asserted, then that XBAR slave port enabled by the bit can accept the bursts allowed by RBEN and WBEN. Otherwise, the FEC interface does not burst to the XBAR slave port controlled by that respective FXSBE*n* bit. Read bursts from that XBAR slave port are enabled by RBEN. Write bursts to that XBAR slave port are enabled by WBEN. FXSBE*n* assignments to XBAR slave ports: FXSBE0 = Flash FXSBE1 = EBI FXSBE3 = Internal SRAM FXSBE6 = Peripheral bridge A FXSBE7 = Peripheral bridge B
8	RBEN	Global read burst enable from XBAR slave port designated by FXSBE*n* 0 = Read bursting from all XBAR slave ports is disabled. 1 = Read bursting is enabled from any XBAR slave port whose FXSBE*n* bit is asserted.

Table 15-3. FBOMCR Field Descriptions (continued)

Bits	Name	Description
9	WBEN	Global write burst enable to XBAR slave port designated by FXSBE*n* 0 = Write bursting to all XBAR slave ports is disabled. 1 = Write bursting is enabled to any XBAR slave port whose FXSBE*n* bit is asserted.
10	ACCERR	Accumulate error - This bit determines whether an error response for the first half of the write burst is accumulated to the second half of the write burst or discarded. In order to complete the burst, the FEC interface to the system bus responds by indicating that the first half of the burst completed without error before it actually writes the data so that it can fetch the second half of the write data from the FIFO. When actually written onto the system bus, the first half of the write burst can have an error. Because this half initially responded without an error to the FIFO, the error is discarded or accumulated with the error response for the second half of the burst. 0 Any error to the first half of the write burst is discarded. 1 Any actual error response to the first half of the write burst is accumulated in the second half's response. In other words, an error response to the first half is seen in the response to the second half, even if the second half does not error.
11–31	—	Reserved, must be cleared.

15.3.4.2 FEC Registers

The following sections describe each FEC register in detail. The base address of these registers is 0xFFF4_C000.

15.3.4.2.1 Ethernet Interrupt Event Register (EIR)

When an event occurs that sets a bit in the Ethernet Interrupt Event register (EIR), an interrupt is generated if the corresponding bit in the interrupt mask register (EIMR) is also set. The bit in the EIR is cleared if a one is written to that bit position; writing zero has no effect. This register is cleared upon hardware reset.

These interrupts can be divided into operational interrupts, transceiver or network error interrupts, and internal error interrupts. Interrupts which can occur in normal operation are GRA, TXF, TXB, RXF, RXB, and MII. Interrupts resulting from errors/problems detected in the network or transceiver are HBERR, BABR, BABT, LC, and RL. Interrupts resulting from internal errors are HBERR and UN.

Some of the error interrupts are independently counted in the MIB block counters. Software can mask the following interrupts since the errors are visible to network management using the following MIB counters:

HBERR	IEEE_T_SQE
BABR	RMON_R_OVERSIZE (valid CRC), RMON_R_JAB (invalid CRC)
BABT	RMON_T_OVERSIZE (valid CRC), RMON_T_JAB (invalid CRC)
LATE_COL	IEEE_T_LCOL
COL_RETRY_LIM	IEEE_T_EXCOL
XFIFO_UN	IEEET_MACERR

Table 15-2 shows the Ethernet interrupt event register (EIR):

Address: Base + 0x0004 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	HB ERR	BABR	BABT	GRA	TXF	TXB	RXF	RXB	MII	EB ERR	LC	RL	UN	0	0	0
W	w1c[1]	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-3. Ethernet Interrupt Event Register (EIR)

[1] "w1c" signifies the bit is cleared by writing 1 to it.

Table 15-4 describes the fields and functions of the Ethernet interrupt event register:

Table 15-4. EIR Field Descriptions

Field	Description
0 HBERR	Heartbeat error. This interrupt indicates that HBC is set in the TCR register and that the COL input was not asserted within the Heartbeat window following a transmission.
1 BABR	Babbling receive error. This bit indicates a frame was received with length in excess of RCR[MAX_FL] bytes.
2 BABT	Babbling transmit error. This bit indicates that the transmitted frame length has exceeded RCR[MAX_FL] bytes. This condition is usually caused by a frame that is too long being placed into the transmit data buffers. Truncation does not occur.
3 GRA	Graceful stop complete. This interrupt is asserted for one of three reasons. Graceful stop means that the transmitter is put into a pause state after completion of the frame currently being transmitted. 1) A graceful stop, which was initiated by the setting of the TCR[GTS] bit is now complete. 2) A graceful stop, which was initiated by the setting of the TCR[TFC_PAUSE] bit is now complete. 3) A graceful stop, which was initiated by the reception of a valid full duplex flow control “pause” frame is now complete. See Section 15.4.10, “Full Duplex Flow Control.”
4 TXF	Transmit frame interrupt. This bit indicates that a frame has been transmitted and that the last corresponding buffer descriptor has been updated.
5 TXB	Transmit buffer interrupt. This bit indicates that a transmit buffer descriptor has been updated.
6 RXF	Receive frame interrupt. This bit indicates that a frame has been received and that the last corresponding buffer descriptor has been updated.
7 RXB	Receive buffer interrupt. This bit indicates that a receive buffer descriptor has been updated that was not the last in the frame.
8 MII	MII interrupt. This bit indicates that the MII has completed the data transfer requested.
9 EBERR	Ethernet bus error. This bit indicates that a system bus error occurred when a DMA transaction was underway. When the EBERR bit is set, ECR[ETHER_EN] is cleared, halting frame processing by the FEC. When this occurs software needs to ensure that the FIFO controller and DMA are also soft reset.
10 LC	Late collision. This bit indicates that a collision occurred beyond the collision window (slot time) in half duplex mode. The frame is truncated with a bad CRC and the remainder of the frame is discarded.
11 RL	Collision retry limit. This bit indicates that a collision occurred on each of 16 successive attempts to transmit the frame. The frame is discarded without being transmitted and transmission of the next frame commences. Can only occur in half duplex mode.
12 UN	Transmit FIFO underrun. This bit indicates that the transmit FIFO became empty before the complete frame was transmitted. A bad CRC is appended to the frame fragment and the remainder of the frame is discarded.
13–31	Reserved, must be cleared.

15.3.4.2.2 Ethernet Interrupt Mask Register (EIMR)

The EIMR register controls which interrupt events are allowed to generate actual interrupts. All implemented bits in this CSR are read/write. This register is cleared upon a hardware reset. If the corresponding bits in both the EIR and EIMR registers are set, the interrupt is signaled to the CPU. The interrupt signal remains asserted until a 1 is written to the EIR bit (write 1 to clear) or a 0 is written to the EIMR bit.

Address: Base + 0x0008 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	HB ERR	BABR	BABT	GRA	TXF	TXB	RXF	RXB	MII	EB ERR	LC	RL	UN	0	0	0
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-4. Interrupt Mask Register (EIMR)

Table 15-5 describes the fields and functions of the Ethernet interrupt event register:

Table 15-5. EIMR Field Descriptions

Field	Description
0–12 See Figure 15-4 and Table 15-4.	Interrupt mask. Each bit corresponds to an interrupt source defined by the EIR register. The corresponding EIMR bit determines whether an interrupt condition can generate an interrupt. 0 The corresponding interrupt source is masked. 1 The corresponding interrupt source is not masked. Write 1 to clear.
13–31	Reserved, must be cleared.

15.3.4.2.3 Receive Descriptor Active Register (RDAR)

RDAR is a command register, written by the application, that indicates that the receive descriptor ring has been updated (empty receive buffers were produced by the driver with the empty bit set).

Whenever the register is written, the R_DES_ACTIVE bit is set. This is independent of the data actually written by the application. When set, the FEC polls the receive descriptor ring and process receive frames (provided ECR[ETHER_EN] is also set). Once the FEC polls a receive descriptor with an empty bit that is cleared to 0, the FEC clears R_DES_ACTIVE and stops receive descriptor ring polling until the bit is set again, signifying that additional descriptors were placed into the receive descriptor ring.

The RDAR register is cleared at reset and when ECR[ETHER_EN] is cleared.

Address: Base + 0x0010 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	R_DES_ ACTIVE	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-5. Receive Descriptor Active Register (RDAR)

Table 15-6 describes the receive descriptor active register (RDAR):

Table 15-6. RDAR Field Descriptions

Field	Description
0–6	Reserved, must be cleared.
7 R_DES_ACTIVE	Set to one when this register is written, regardless of the value written. Cleared by the FEC device whenever no additional “empty” descriptors remain in the receive ring. Also cleared when ECR[ETHER_EN] is cleared.
8–31	Reserved, must be cleared.

15.3.4.2.4 Transmit Descriptor Active Register (TDAR)

The TDAR is a command register that must be written by the application to indicate that the transmit descriptor ring has been updated (transmit buffers have been produced by the driver with the ready bit set in the buffer descriptor).

Whenever the register is written, the X_DES_ACTIVE bit is set. This value is independent of the data actually written by the application. When set, the FEC polls the transmit descriptor ring and processes transmit frames (provided ECR[ETHER_EN] is also set). Once the FEC polls a transmit descriptor and the ready bit is not set, the FEC clears X_DES_ACTIVE and stops polling the transmit descriptor ring until you set the bit again, signifying additional descriptors were placed in the transmit descriptor ring.

The TDAR register is cleared at reset, when ECR[ETHER_EN] is cleared, or when ECR[RESET] is set.

Address: Base + 0x0014 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	X_DES_ ACTIVE	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-6. Transmit Descriptor Active Register (TDAR)

Table 15-7 describes the transmit descriptor active register (TDAR):

Table 15-7. TDAR Field Descriptions

Field	Description
0–6	Reserved, must be cleared.
7 X_DES_ACTIVE	Set to one when this register is written, regardless of the value written. Cleared by the FEC device whenever no additional “ready” descriptors remain in the transmit ring. Also cleared when ECR[ETHER_EN] is cleared.
8–31	Reserved, must be cleared.

15.3.4.2.5 Ethernet Control Register (ECR)

ECR is a read/write application register, though both fields in this register can be altered by hardware as well. The ECR is used to enable and disable the FEC.

Address: Base + 0x0024 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ETHER EN	RESET
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-7. Ethernet Control Register (ECR)

Table 15-8 describes the fields and functions in the Ethernet control register:

Table 15-8. ECR Field Descriptions

Bits	Description
0–29	Reserved
30 ETHER_EN	When this bit is set, the FEC is enabled, and reception and transmission are possible. When this bit is cleared, reception is immediately stopped and transmission is stopped after a bad CRC is appended to any currently transmitted frame. The buffer descriptors for an aborted transmit frame are not updated after clearing this bit. When ETHER_EN is deasserted, the DMA, buffer descriptor, and FIFO control logic are reset, including the buffer descriptor and FIFO pointers. The ETHER_EN bit is altered by hardware under the following conditions: • ECR[RESET] is set by software, in which case ETHER_EN is cleared • An error condition causes the EIR[EBERR] bit to set, in which case ETHER_EN is cleared
31 RESET	When this bit is set, the equivalent of a hardware reset is performed but it is local to the FEC. ETHER_EN is cleared and all other FEC registers take their reset values. Also, any transmission/reception currently in progress is abruptly aborted. This bit is automatically cleared by hardware during the reset sequence. The reset sequence takes approximately 8 system clock cycles after RESET is written with a 1.

15.3.4.2.6 MII Management Frame Register (MMFR)

The MMFR is accessed by the application and does not reset to a defined value. The MMFR register is used to communicate with the attached MII compatible PHY devices, providing read/write access to their MII registers. Performing a write to the MMFR generates a management frame unless the MSCR is cleared to 0. If you write to MMFR when MSCR = 0, and then set the MSCR register to a non-zero value, an MII frame is generated with the data previously written to the MMFR. This allows you to program MMFR and MSCR in either order if MSCR is currently zero.

Address: Base + 0x0040 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	ST		OP		PA					RA					TA	
Reset	U[1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	DATA															
Reset	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

[1] "U" signifies a bit that is uninitialized.

Figure 15-8. MII Management Frame Register (MMFR)

Table 15-9 describes the fields and functions for the MII management frame register:

Table 15-9. MMFR Field Descriptions

Field	Description
0–1 ST	Start of frame delimiter. These bits must be programmed to 01 for a valid MII management frame.
2–3 OP	Operation code. This field must be programmed to 10 (read) or 01 (write) to generate a valid MII management frame. A value of 11 produces "read" frame operation while a value of 00 produces "write" frame operation, but these frames are not MII compliant.
4–8 PA	PHY address. This field specifies one of up to 32 attached PHY devices.
9–13 RA	Register address. This field specifies one of up to 32 registers within the specified PHY device.
14–15 TA	Turn around. This field must be programmed to 10 to generate a valid MII management frame.
16–31 DATA	Management frame data. This is the field for data to be written to or read from the PHY register.

To perform a read or write operation on the MII management interface, the MMFR register must be written by the application. To generate a valid read or write management frame, the ST field must be written with a 01 pattern, and the TA field must be written with a 10. If other patterns are written to these fields, a frame is generated but does not comply with the IEEE® 802.3 MII definition.

To generate an IEEE® 802.3-compliant MII management interface write frame (write to a PHY register), the application must write {01 01 PHYAD REGAD 10 DATA} to the MMFR register. Writing this pattern

causes the control logic to shift the data in the MMFR register out following a preamble generated by the control state machine. Do not read the MMFR register during this time, because the contents is altered and serially shifted, therefore this data can be invalid. Once the write management frame operation is complete, the MII interrupt is generated. At this time the contents of the MMFR register matches the original value written.

To generate an MII management interface read frame (read a PHY register) you must write {01 10 PHYAD REGAD 10 XXXX} to the MMFR register (the content of the DATA field is ignored). Writing this pattern causes the control logic to shift the data in the MMFR register out following a preamble generated by the control state machine. Do not read the MMFR register during this time, because the contents are altered and serially shifted, and can contain invalid data. Once the read management frame operation is complete, the MII interrupt is generated. At this time the contents of the MMFR register matches the original value written except for the DATA field contents that are replaced by the value read from the PHY register.

If the MMFR register is written while frame generation is in progress, the frame contents is altered. Software must poll the EIR[MII] bit or use the EIR[MII] bit to generate an interrupt to avoid writing to the MMFR register while frame generation is in progress.

15.3.4.2.7 MII Speed Control Register (MSCR)

The MSCR provides control of the MII clock (FEC_MDC signal) frequency, allows a preamble drop on the MII management frame, and provides observability (intended for manufacturing test) of an internal counter used in generating the FEC_MDC clock signal.

Address: Base + 0x0044 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	DIS_PREAMBLE	MII_SPEED						0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-9. MII Speed Control Register (MSCR)

Table 15-10 describes the fields and functions of the MII speed control register (MSCR):

Table 15-10. MSCR Field Descriptions

Field	Description
0–23	Reserved, must be cleared.
24 DIS_PREAMBLE	Asserting this bit causes preamble (32 1's) not to be prepended to the MII management frame. The MII standard allows the preamble to be dropped if the attached PHY devices does not require it.

Table 15-10. MSCR Field Descriptions

Field	Description
25–30 MII_SPEED	MII_SPEED controls the frequency of the MII management interface clock (FEC_MDC) relative to the system clock. A value of 0 in this field “turns off” the MDC and leaves it in a low voltage state. Any non-zero value results in the MDC frequency of 1÷ (MII_SPEED × 4) of the system clock frequency.
31	Reserved, must be cleared.

The MII_SPEED field must be programmed with a value to provide an MDC frequency of less than or equal to 2.5 MHz to be compliant with the IEEE® 802.3 MII specification. The MII_SPEED must be set to a non-zero value in order to source a read or write management frame. After the management frame is complete, the MSCR register can be optionally cleared to zero to turn off the MDC. The MDC generated has a 50% duty cycle except when MII_SPEED is changed during operation (the change takes effect following a rising- or falling-edge of MDC).

If the system clock is 50 MHz, programming this register to 0x0000_0005 results in an MDC frequency of 50 MHz x 1/20 = 2.5 MHz. A table showing optimum values for MII_SPEED as a function of system clock frequency is provided in Table 15-11.

Table 15-11. Programming Examples for MSCR

System Clock Frequency	MII_SPEED (field in reg)	MDC frequency
50 MHz	0x0005	2.5 MHz
66 MHz	0x0007	2.36 MHz
80 MHz	0x0008	2.5 MHz
100 MHz	0x000A	2.5 MHz
132 MHz	0x000D	2.5 MHz

15.3.4.2.8 MIB Control Register (MIBC)

The MIBC is a read/write register used to provide control of and to observe the state of the MIB block. This register is accessed by the application if there is a need to disable the MIB block operation. For example, in order to clear all MIB counters in RAM the application must disable the MIB block, then clear all the MIB RAM locations, then enable the MIB block. The MIB_DISABLE bit is reset to 1. See Table 15-2 for the locations of the MIB counters.

Address: Base + 0x0064 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	MIB_DISABLE	MIB_IDLE	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-10. MIB Control Register (MIBC)

Table 15-12 describes the fields and functions in the MIB block control register (MIBC):

Table 15-12. MIBC Field Descriptions

Field	Description
0 MIB_DISABLE	A read/write control bit. If set, the MIB logic halts and does not update any MIB counters.
1 MIB_IDLE	A read-only status bit. If set the MIB block is not currently updating any MIB counters.
2–31	Reserved

15.3.4.2.9 Receive Control Register (RCR)

The RCR is programmed by the application. The RCR controls the operational mode of the receive block and must be written only when ECR[ETHER_EN] = 0 (initialization time).

Address: Base + 0x0084 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	MAX_FL										
W																
Reset	0	0	0	0	0	1	0	1	1	1	1	0	1	1	1	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	FCE	BC_REJ	PROM	MII_MODE	DRT	LOOP
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 15-11. Receive Control Register (RCR)

Table 15-13 describes the fields and functions in the receive control register (RCR):

Table 15-13. RCR Descriptions

Bits	Name	Description
0–4	—	Reserved, must be cleared.
5–15 MAX_FL	MAX_FL	Maximum frame length. Resets to decimal 1518. Length is measured starting at DA and includes the CRC at the end of the frame. Transmit frames longer than MAX_FL cause the BABT interrupt to occur. Receive frames longer than MAX_FL cause a BABR interrupt and sets the LG bit in the end-of-frame receive buffer descriptor. You can program the default value to 1518 or 1522 (if VLAN tags are supported).
16–25	—	Reserved, must be cleared.
26 FCE	FCE	Flow control enable. If asserted, the receiver detects PAUSE frames. Upon PAUSE frame detection, the transmitter stops transmitting data frames for a given duration.
27 BC_REJ	BC_REJ	Broadcast frame reject. If asserted, frames with DA (destination address) = FF_FF_FF_FF_FF_FF is rejected unless the PROM bit is set. If both BC_REJ and PROM = 1, then frames with broadcast DA is accepted and the M (MISS) bit is set in the receive buffer descriptor.
28 PROM	PROM	Promiscuous mode. All frames are accepted regardless of address matching.
29 MII_MODE	MII_MODE	Media independent interface mode. Selects external interface mode. Setting this bit to one selects MII mode, setting this bit equal to zero selects 7-wire mode (used only for serial 10 Mbps). This bit controls the interface mode for both transmit and receive blocks.
30 DRT	DRT	Disable receive on transmit. 0 Receive path operates independently of transmit (use for full duplex or to monitor transmit activity in half duplex mode). 1 Disable reception of frames while transmitting (normally used for half duplex mode).
31 LOOP	LOOP	Internal loopback. If set, transmitted frames are looped back internal to the device and the transmit output signals are not asserted. The system clock is substituted for the FEC_TX_CLK when LOOP is asserted. DRT must be set to zero when asserting LOOP.

15.3.4.2.10 Transmit Control Register (TCR)

The transmit control register is read/write and is used to configure the transmit block. This register is cleared at system reset. Modify bits 29 and 30 only when ECR[ETHER_EN] = 0.

Address: Base + 0x00C4 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	RFC_ PAUSE	TFC_ PAUSE	FDEN	HBC	GTS
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-12. Transmit Control Register (TCR)

Table 15-14 describes the fields and functions in the transmit control register:

Table 15-14. Transmit Control Register Field Descriptions

Field	Description
0–26	Reserved, must be cleared.
27 RFC_PAUSE	Receive frame control pause. This read-only status bit is asserted when a full duplex flow control pause frame has been received and the transmitter is paused for the duration defined in this pause frame. This bit automatically clears when the pause duration is complete.
28 TFC_PAUSE	Transmit frame control pause. Transmits a PAUSE frame when asserted. When this bit is set, the MAC stops transmitting data frames after the current transmission completes. At this time, the GRA interrupt in the EIR register is asserted. With transmission of data frames stopped, the MAC transmits a MAC Control PAUSE frame. Next, the MAC clears the TFC_PAUSE bit and resumes transmitting data frames. If you pause the transmitter by asserting GTS or receiving another PAUSE frame, the MAC can still transmit a MAC control PAUSE frame.
29 FDEN	Full duplex enable. If set, frames are transmitted independent of carrier sense and collision inputs. This bit must only be modified when ETHER_EN is deasserted.
30 HBC	Heartbeat control. If set, the heartbeat check is performed following end of transmission and the HB bit in the status register is set if the collision input does not assert within the heartbeat window. This bit must only be modified when ETHER_EN is deasserted.
31 GTS	Graceful transmit stop. When this bit is set, the MAC stops transmitting after any frame that is currently being transmitted is complete and the GRA interrupt in the EIR register is asserted. If frame transmission is not currently underway, the GRA interrupt is asserted immediately. Once transmission has completed, a “restart” can be accomplished by clearing the GTS bit. The next frame in the transmit FIFO is then transmitted. If an early collision occurs during transmission when GTS = 1, transmission stops after the collision. The frame is transmitted again once GTS is cleared. Previous frames can reside in the transmit FIFO that are transmitted when GTS is reasserted. To avoid this condition, deassert ECR[ETHER_EN] following the GRA interrupt.

15.3.4.2.11 Physical Address Low Register (PALR)

The PALR is written by the application. This register contains the lower 32 bits (bytes 0,1,2,3) of the 48-bit MAC address used in the address recognition process to compare with the DA (destination address) field of receive frames with an individual DA. In addition, this register is used in bytes 0 through 3 of the 6-byte source address field when transmitting PAUSE frames. This register is not reset and must be initialized by the application.

Address: Base + 0x00E4 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	PADDR1															
Reset	U [1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	PADDR1															
Reset	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

[1] “U” signifies a bit that is uninitialized.

Figure 15-13. Physical Address Low Register (PALR)

Table 15-15 describes the field and function in the physical address low register (PALR):

Table 15-15. PALR Field Descriptions

Field	Description
0–31 PADDR1	Bytes 0 (bits 0:7), 1 (bits 8:15), 2 (bits 16:23) and 3 (bits 24:31) of the 6-byte individual address to be used for exact match, and the Source Address field in PAUSE frames.

15.3.4.2.12 Physical Address Upper Register (PAUR)

The application program writes the PAUR. This register contains the upper 16 bits (bytes 4 and 5) of the 48-bit MAC address used in the address recognition process to compare with the DA (destination address) field of receive frames with an individual DA. In addition, this register is used in bytes 4 and 5 of the 6-byte source address field when transmitting PAUSE frames. Bits 16:31 of the PAUR contain a constant TYPE field (0x8808) used to transmit PAUSE frames. This register is not reset, and bits 0:15 must be initialized by the application program. See Section 15.4.10, "Full Duplex Flow Control" for information on using the TYPE field.

Address: Base + 0x00E8 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	PADDR2															
W																
Reset	U [1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	TYPE															
W																
Reset	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

[1] "U" signifies a bit that is uninitialized.

Figure 15-14. Physical Address Upper Register (PAUR)

Table 15-16 describes the fields and functions in the physical address upper register (PAUR):

Table 15-16. PAUR Field Descriptions

Field	Description
0–15 PADDR2	Bytes 4 (bits 0:7) and 5 (bits 8:15) of the 6-byte individual address to be used for exact match, and the Source Address field in PAUSE frames.
16–31 TYPE	The type field is used in PAUSE frames. These bits are a constant, 0x8808.

15.3.4.2.13 Opcode and Pause Duration Register (OPD)

The OPD is read/write accessible. This register contains the 16-bit OPCODE and 16-bit pause duration (PAUSE_DUR) fields used in transmission of a PAUSE frame. The OPCODE field is a constant value, 0x0001. When another node detects a PAUSE frame, that node pauses the transmission for the duration specified in the pause duration field. This register is not reset and must be initialized by the application. See Section 15.4.10, "Full Duplex Flow Control" for information on using the OPD register.

Address: Base + 0x00EC Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	OPCODE															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	PAUSE_DUR															
W																
Reset	U [1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

[1] "U" signifies a bit that is uninitialized.

Figure 15-15. Opcode/Pause Duration Register (OPD)

Table 15-17 describes the fields and functions of the opcode and pause duration register (OPD):

Table 15-17. OPD Field Descriptions

Field	Description
0–15 OPCODE	Opcode field used in PAUSE frames. These bits are a constant, 0x0001.
16–31 PAUSE_DUR	Pause duration field used in PAUSE frames.

15.3.4.2.14 Descriptor Individual Upper Address Register (IAUR)

The IAUR is written by the application. This register contains the upper 32 bits of the 64-bit individual address hash table used in the address recognition process to check for possible match with the DA field of receive frames with an individual DA. This register is not reset and must be initialized by the application.

Address: Base + 0x0118 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	IADDR1															
Reset	U[1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	IADDR1															
Reset	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

[1] "U" signifies a bit that is uninitialized. See the Preface of the book.

Figure 15-18. Descriptor Individual Upper Address Register (IAUR)

Table 15-18. IAUR Field Descriptions

Field	Descriptions
0–31 IADDR1	The upper 32 bits of the 64-bit hash table used in the address recognition process for receive frames with a unicast address. Bit 31 of IADDR1 contains hash index bit 63. Bit 0 of IADDR1 contains hash index bit 32.

15.3.4.2.15 Descriptor Individual Lower Address (IALR)

The IALR register is written by the application. This register contains the lower 32 bits of the 64-bit individual address hash table used in the address recognition process to check for possible match with the DA field of receive frames with an individual DA. This register is not reset and must be initialized by the application.

Address: Base + 0x011C Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	IADDR2															
Reset	U[1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	IADDR2															
Reset	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

[1] "U" signifies a bit that is uninitialized. See the Preface of the book.

Figure 15-19. Descriptor Individual Lower Address Register (IALR)

Table 15-19. IALR Field Descriptions

Field	Description
0–31 IADDR2	The lower 32 bits of the 64-bit hash table used in the address recognition process for receive frames with a unicast address. Bit 31 of IADDR2 contains hash index bit 31. Bit 0 of IADDR2 contains hash index bit 0.

15.3.4.2.16 Descriptor Group Upper Address (GAUR)

The GAUR is written by the application. This register contains the upper 32 bits of the 64-bit hash table used in the address recognition process for receive frames with a multicast address. This register must be initialized by the application.

Address: Base + 0x0120 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	GADDR1															
Reset	U[1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	GADDR1															
Reset	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

[1] "U" signifies a bit that is uninitialized. See the Preface of the book.

Figure 15-20. Descriptor Group Upper Address Register (GAUR)

Table 15-20. GAUR Field Descriptions

Field	Description
0–31 GADDR1	The GADDR1 register contains the upper 32 bits of the 64-bit hash table used in the address recognition process for receive frames with a multicast address. Bit 31 of GADDR1 contains hash index bit 63. Bit 0 of GADDR1 contains hash index bit 32.

15.3.4.2.17 Descriptor Group Lower Address (GALR)

The GALR register is written by the application. This register contains the lower 32 bits of the 64-bit hash table used in the address recognition process for receive frames with a multicast address. This register must be initialized by the application.

Address: Base + 0x0124 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	GADDR2															
W																
Reset	U[1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	GADDR2															
W																
Reset	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

1 "U" signifies a bit that is uninitialized. See the Preface of the book.

Figure 15-21. Descriptor Group Lower Address Register (GALR)

Table 15-21. GALR Field Descriptions

Field	Description
0–31 GADDR2	The GADDR2 register contains the lower 32 bits of the 64-bit hash table used in the address recognition process for receive frames with a multicast address. Bit 31 of GADDR2 contains hash index bit 31. Bit 0 of GADDR2 contains hash index bit 0.

15.3.4.2.18 FIFO Transmit FIFO Watermark Register (TFWR)

The TFWR is a 32-bit read/write register with one 2-bit field programmed by the application to control the amount of data required in the transmit FIFO before transmission of a frame can begin. This allows the application to minimize transmit latency (TFWR = 0x) or allow for larger bus access latency (TFWR = 11) due to contention for the system bus. Setting the watermark to a high value minimizes the risk of a transmit FIFO underrun due to contention for the system bus. The byte counts of the TFWR field can require modification to match a given system requirement.

Address: Base + 0x0144 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X_WMRK	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 15-22. FIFO Transmit FIFO Watermark Register (TFWR)

Table 15-22. TFWR Field Descriptions

Field	Descriptions
0–29	Reserved, must be cleared.
30–31 X_WMRK	Number of bytes written to transmit FIFO before transmission of a frame begins 0x 64 bytes written 10 128 bytes written 11 192 bytes written

15.3.4.3 FIFO Receive Bound Register (FRBR)

The FRBR is a 32-bit register with one 8-bit field that the application can read to determine the upper address bound of the FIFO RAM. Drivers can use this value, along with the FRSR register, to divide the available FIFO RAM between the transmit and receive data paths.

Address Base + 0x014C Access: RO

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	R_BOUND								0	0
W																
Reset	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

Figure 15-23. FIFO Receive Bound Register (FRBR)

Table 15-23. FRBR Field Descriptions

Field	Descriptions
0–21	Reserved, read as 0 (except bit 10, which is read as 1).
22–29 R_BOUND	Read-only. Highest valid FIFO RAM address.
30–31	Reserved, must be cleared.

15.3.4.3.1 FIFO Receive Start Register (FRSR)

The FRSR is a 32-bit register with one 8-bit field programmed by the application to indicate the starting address of the receive FIFO. FRSR marks the boundary between the transmit and receive FIFOs. The transmit FIFO uses addresses from the start of the FIFO to the location four bytes before the address programmed into the FRSR. The receive FIFO uses addresses from FRSR to FRBR inclusive.

The FRSR register is initialized by hardware at reset. FRSR only needs to be written to change the default value.

Address Base + 0x0150 Access: RO

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	R_FSTART								0	0
W																
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Figure 15-24. FIFO Receive Start Register (FRSR)

Table 15-24. FRSR Field Descriptions

Field	Descriptions
0–21	Reserved, read as 0 (except bit 21, which is read as 1).
22–29 R_FSTART	Address of first receive FIFO location. Acts as delimiter between receive and transmit FIFOs.
30–31	Reserved, read as 0.

15.3.4.3.2 Receive Descriptor Ring Start (ERDSR)

The ERDSR is written by the application. It provides a pointer to the start of the circular receive buffer descriptor queue in external memory. This pointer must be 32-bit aligned; however, it is recommended it be made 128-bit aligned (evenly divisible by 16).

This register is not reset and must be initialized by the application prior to operation.

Address Base + 0x0180 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	R_DES_START															
Reset	U[1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	R_DES_START														0	0
W																
Reset	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

1 “U” signifies a bit that is uninitialized.

Figure 15-25. Receive Descriptor Ring Start Register (ERDSR)

Table 15-25. ERDSR Field Descriptions

Field	Descriptions
0–29 R_DES_START	Pointer to start of receive buffer descriptor queue.
30–31	Reserved, must be cleared.

15.3.4.3.3 Transmit Buffer Descriptor Ring Start (ETDSR)

The ETDSR is written by the application. It provides a pointer to the start of the circular transmit buffer descriptor queue in external memory. This pointer must be 32-bit aligned; however, it is recommended it be made 128-bit aligned (evenly divisible by 16). Bits 30 and 31 must be written to 0 by the application. Non-zero values in these two bit positions are ignored by the hardware.

This register is not reset and must be initialized by the application prior to operation.

Address Base + 0x0184 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	X_DES_START															
Reset	U[1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	X_DES_START														0	0
W																
Reset	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

[1] "U" signifies a bit that is uninitialized.

Figure 15-26. Transmit Buffer Descriptor Ring Start Register (ETDSR)

Table 15-26. ETDSR Field Descriptions

Field	Descriptions
0–29 X_DES_START	Pointer to start of transmit buffer descriptor queue.
30–31	Reserved, must be cleared.

15.3.4.3.4 Receive Buffer Size Register (EMRBR)

The EMRBR is a 32-bit register with one 7-bit field programmed by the application. The EMRBR register dictates the maximum size of all receive buffers. Note that because receive frames are truncated at 2K–1 byte, only bits 21–27 are used. This value must take into consideration that the receive CRC is always written into the last receive buffer. To allow one maximum size frame per buffer, EMRBR must be set to RCR[MAX_FL] or larger. The EMRBR must be evenly divisible by 16. To insure this, bits 28-31 are

forced low. To minimize bus utilization (descriptor fetches) it is recommended that EMRBR be greater than or equal to 256 bytes.

The EMRBR register does not reset, and must be initialized by the application.

Address: Base + 0x0188 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	U[1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	R_BUF_SIZE							0	0	0	0
W																
Reset	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

1 "U" signifies a bit that is uninitialized.

Figure 15-27. Receive Buffer Size Register (EMRBR)

Table 15-27. EMRBR Field Descriptions

Field	Descriptions
0–20	Reserved, must be written to 0 by the host processor.
21–27 R_BUF_SIZE	Receive buffer size.
28–31	Reserved, must be written to 0 by the host processor.

15.4 Functional Description

This section describes the operation of the FEC, beginning with the hardware and software initialization sequence, then the software (Ethernet driver) interface for transmitting and receiving frames.

Following the software initialization and operation sections are sections providing a detailed description of the functions of the FEC.

15.4.1 Initialization Sequence

This section describes which registers are reset due to hardware reset, which are reset by the FEC RISC, and what locations the application must initialize prior to enabling the FEC.

15.4.1.1 Hardware Controlled Initialization

In the FEC, registers and control logic that generate interrupts are reset by hardware. A hardware reset deasserts output signals and resets general configuration bits.

Other registers reset when the ECR[ETHER_EN] bit is cleared. ECR[ETHER_EN] is deasserted by a hard reset or can be deasserted by software to halt operation. By deasserting ECR[ETHER_EN], the configuration control registers such as the TCR and RCR are not reset, but the entire data path is reset.

Table 15-28. ECR[ETHER_EN] De-Assertion Effect on FEC

Register/Machine	Reset Value
XMIT block	Transmission is aborted (bad CRC appended)
RECV block	Receive activity is aborted
DMA block	All DMA activity is terminated
RDAR	Cleared
TDAR	Cleared
Descriptor Controller block	Halt operation

15.4.2 Application Initialization (Prior to Asserting ECR[ETHER_EN])

The application must initialize portions of the FEC prior to setting the ECR[ETHER_EN] bit. The exact values depend on the application. The sequence is not important.

Ethernet MAC registers requiring initialization are defined in Table 15-29.

Table 15-29. Application Initialization (Before ECR[ETHER_EN])

Description
Initialize EIMR
Clear EIR (write 0xFFFF_FFFF)
TFWR (optional)
IALR and IAUR
GAUR and GALR
PALR and PAUR (only needed for full duplex flow control)
OPD (only needed for full duplex flow control)
RCR
TCR
MSCR (optional)
Clear MIB_RAM (locations Base + 0x0200–0x02FC)

FEC FIFO/DMA registers that require initialization are defined in Table 15-30.

Table 15-30. FEC Application Initialization (Before ECR[ETHER_EN])

Description
Initialize FRSR (optional)
Initialize EMRBR
Initialize ERDSR

Table 15-30. FEC Application Initialization (Before ECR[ETHER_EN]) (continued)

Description
Initialize ETDSR
Initialize (Empty) Transmit Descriptor ring
Initialize (Empty) Receive Descriptor ring

15.4.3 Microcontroller Initialization

In the FEC, the descriptor control RISC initializes some registers after ECR[ETHER_EN] is asserted. After the microcontroller initialization sequence is complete, the hardware is ready for operation.

Table 15-31 shows microcontroller initialization operations.

Table 15-31. Microcontroller Initialization

Description
Initialize Backoff Random Number Seed
Activate Receiver
Activate Transmitter
Clear Transmit FIFO
Clear Receive FIFO
Initialize Transmit Ring Pointer
Initialize Receive Ring Pointer
Initialize FIFO Count Registers

15.4.4 Application Initialization (After Asserting ECR[ETHER_EN])

After asserting ECR[ETHER_EN], the application can set up the buffer/frame descriptors and write to the TDAR and RDAR. See Section 15.5, “Buffer Descriptors” for more details.

15.4.5 Network Interface Options

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a 7-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by the RCR[MII_MODE] bit. In MII mode (RCR[MII_MODE] = 1), there are 18 signals defined by the IEEE® 802.3 standard and supported by the EMAC. These signals are shown in Table 15-32 below.

Table 15-32. MII Mode

Signal Description	EMAC Signal
Transmit Clock	FEC_TX_CLK
Transmit Enable	FEC_TX_EN
Transmit Data	FEC_TXD[3:0]

Table 15-32. MII Mode (continued)

Signal Description	EMAC Signal
Transmit Error	FEC_TX_ER
Collision	FEC_COL
Carrier Sense	FEC_CRS
Receive Clock	FEC_RX_CLK
Receive Data Valid	FEC_RX_DV
Receive Data	FEC_RXD[3:0]
Receive Error	FEC_RX_ER
Management Data Clock	FEC_MDC
Management Data Input/Output	FEC_MDIO

The 7-wire serial mode interface (RCR[MII_MODE] = 0) operates in what is generally referred to as the "AMD" mode. 7-wire mode connections to the external transceiver are shown in Table 15-33.

Table 15-33. 7-Wire Mode Configuration

Signal Description	FEC Signal
Transmit Clock	FEC_TX_CLK
Transmit Enable	FEC_TX_EN
Transmit Data	FEC_TXD0
Collision	FEC_COL
Receive Clock	FEC_RX_CLK
Receive Data Valid	FEC_RX_DV
Receive Data	FEC_RXD0

15.4.6 FEC Frame Transmission

The Ethernet transmitter is designed to work with almost no intervention from software. Once ECR[ETHER_EN] is asserted and data appears in the transmit FIFO, the Ethernet MAC is able to transmit onto the network.

When the transmit FIFO fills to the watermark (defined by the TFWR), the MAC transmit logic asserts FEC_TX_EN and start transmitting the preamble (PA) sequence, the start frame delimiter (SFD), and then the frame information from the FIFO. However, the controller defers the transmission if the network is busy (FEC_CRS asserts). Before transmitting, the controller waits for carrier sense to become inactive, then determines if carrier sense stays inactive for 60 bit times. If so, the transmission begins after waiting an additional 36 bit times (96 bit times after carrier sense originally became inactive). See Section 15.4.14.1, "Transmission Errors" for more details.

If a collision occurs during transmission of the frame (half duplex mode), the Ethernet controller follows the specified backoff procedures and attempts to retransmit the frame until the retry limit is reached. The transmit FIFO stores at least the first 64 bytes of the transmit frame, so that they do not have to be retrieved from system memory in case of a collision. This improves bus utilization and latency in case immediate retransmission is necessary.

When all the frame data has been transmitted, the FCS (frame check sequence or 32-bit cyclic redundancy check, CRC) bytes are appended if the TC bit is set in the transmit frame control word. If the ABC bit is set in the transmit frame control word, an invalid CRC is appended to the frame data regardless of the TC bit value. Following the transmission of the CRC, the Ethernet controller writes the frame status information to the MIB block. Short frames are automatically padded by the transmit logic (if the TC bit in the transmit buffer descriptor for the end of frame buffer = 1).

Both buffer (TXB) and frame (TFINT) interrupts can be generated as determined by the settings in the EIMR.

The transmit error interrupts are HBERR, BABT, LATE_COL, COL_RETRY_LIM, and XFIFO_UN. If the transmit frame length exceeds MAX_FL bytes, the BABT interrupt is asserted but the entire frame is transmitted (no truncation).

To pause transmission, set the GTS (graceful transmit stop) bit in the TCR register. When the TCR[GTS] is set, the FEC transmitter stops immediately if transmission is not in progress; otherwise, it continues transmission until the current frame either finishes or terminates with a collision. After the transmitter has stopped, the GRA (graceful stop complete) interrupt is asserted. If TCR[GTS] is cleared, the FEC resumes transmission with the next frame.

The Ethernet controller transmits bytes least significant bit first.

15.4.7 FEC Frame Reception

The FEC receiver is designed to work with almost no intervention from the host and can perform address recognition, CRC checking, short frame checking, and maximum frame length checking.

When the driver enables the FEC receiver by asserting ECR[ETHER_EN], the FEC starts processing receive frames immediately. When FEC_RX_DV asserts, the receiver first checks for a valid PA/SFD header. If the PA/SFD is valid, it is stripped and the frame is processed by the receiver. If no valid PA/SFD is found, the frame is ignored.

In serial mode, the first 16 bit times of FEC_RXD0 following assertion of FEC_RX_DV are ignored. Following the first 16 bit times the data sequence is checked for alternating 1 and 0. If a 11 or 00 data sequence is detected during bit times 17 to 21, the remainder of the frame is ignored. After bit time 21, the data sequence is monitored for a valid SFD (11). If a 00 is detected, the frame is rejected. When a 11 is detected, the PA/SFD sequence is complete.

In MII mode, the receiver checks for at least one byte matching the SFD. Zero or more PA bytes can occur, but if a 00 bit sequence is detected prior to the SFD byte, the frame is ignored.

After the first 6 bytes of the frame have been received, the FEC performs address recognition on the frame.

Once a collision window (64 bytes) of data has been received and if address recognition has not rejected the frame, the receive FIFO is signalled that the frame is “accepted” and can be passed on to the DMA. If the frame is a runt (due to collision) or is rejected by address recognition, the receive FIFO is notified to “reject” the frame. Thus, no collision fragments are presented to the application except late collisions, which indicate serious LAN problems.

During reception, the Ethernet controller checks for various error conditions and once the entire frame is written into the FIFO, a 32-bit frame status word is written into the FIFO. This status word contains the M, BC, MC, LG, NO, CR, OV and TR status bits, and the frame length. See Section 15.4.14.2, “Reception Errors” for more details.

Receive buffer (RXB) and frame interrupts (RFINT) can be generated if enabled by the EIMR register. A receive error interrupt is babbling receiver error (BABR). Receive frames are not truncated if they exceed the max frame length (MAX_FL); however, the BABR interrupt occurs and the LG bit in the receive buffer descriptor (RxBD) is set. See Section 15.5.2, “Ethernet Receive Buffer Descriptor (RxBD)” for more details.

When the receive frame is complete, the FEC sets the L-bit in the RxBD, writes the other frame status bits into the RxBD, and clears the E-bit. The Ethernet controller next generates a maskable interrupt (RFINT bit in EIR, maskable by RFIEN bit in EIMR), indicating that a frame has been received and is in memory. The Ethernet controller then waits for a new frame.

The Ethernet controller receives serial data LSB first.

15.4.8 Ethernet Address Recognition

The FEC filters the received frames based on the type of destination address (DA) — individual (unicast), group (multicast), or broadcast (all-ones group address). The difference between an individual address and a group address is determined by the I/G bit in the destination address field. A flowchart for address recognition on received frames is illustrated in the figures below.

Address recognition is accomplished through the use of the receive block and microcode running on the microcontroller. The flowchart shown in Figure 15-28 illustrates the address recognition decisions made by the receive block, while Figure 15-29 illustrates the decisions made by the microcontroller.

If the DA is a broadcast address and broadcast reject (RCR[BC_REJ]) is deasserted, then the frame is accepted unconditionally, as shown in Figure 15-28. Otherwise, if the DA is not a broadcast address, then the microcontroller runs the address recognition subroutine, as shown in Figure 15-29.

If the DA is a group (multicast) address and flow control is disabled, then the microcontroller performs a group hash table lookup using the 64-entry hash table programmed in GAUR and GALR. If a hash match occurs, the receiver accepts the frame.

If flow control is enabled, the microcontroller does an exact address match check between the DA and the designated PAUSE DA (01:80:C2:00:00:01). If the receive block determines that the received frame is a valid PAUSE frame, then the frame is rejected. The receiver detects a PAUSE frame with the DA field set to the designated PAUSE DA or the unicast physical address.

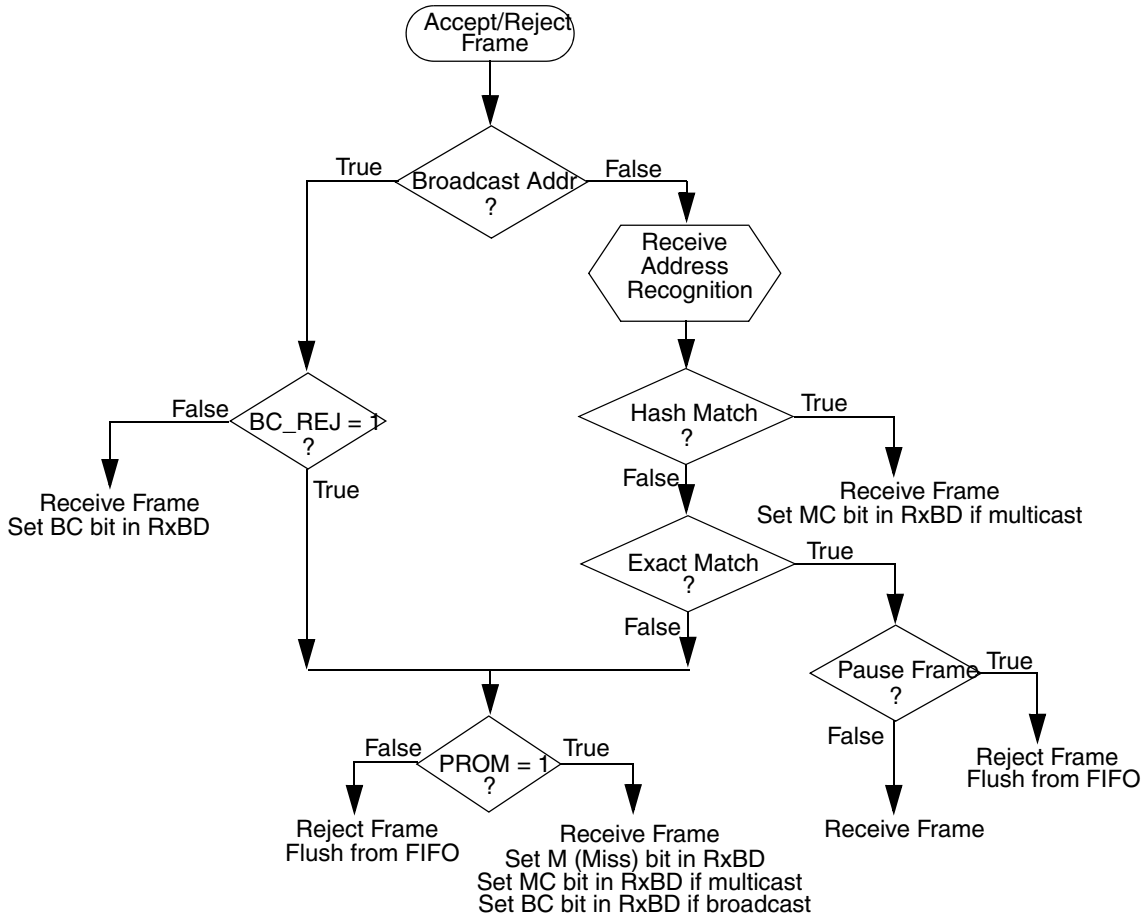
If the DA is the individual (unicast) address, the microcontroller performs an individual exact match comparison between the DA and 48-bit physical address that the application programs in the PALR and

PAUR registers. If an exact match occurs, the frame is accepted; otherwise, the microcontroller does an individual hash table lookup using the 64-entry hash table programmed in registers, IAUR and IALR. In the case of an individual hash match, the frame is accepted. Again, the receiver accepts or reject the frame based on PAUSE frame detection, shown in Figure 15-28.

If neither a hash match (group or individual), nor an exact match (group or individual) occur, then If promiscuous mode is enabled (RCR[PROM] = 1), then the frame is accepted and the MISS bit in the receive buffer descriptor is set; otherwise, the frame is rejected.

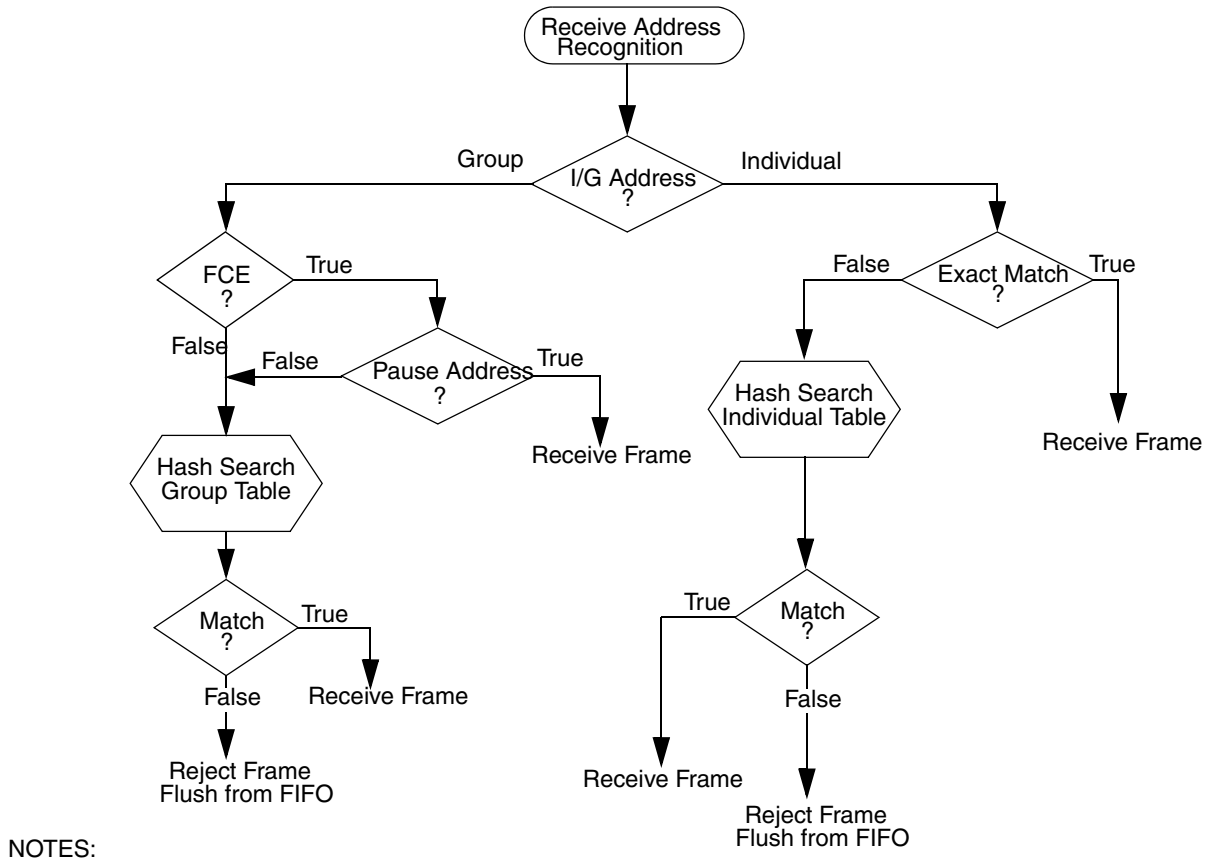
Similarly, if the DA is a broadcast address, broadcast reject (RCR[BC_REJ]) is asserted, and promiscuous mode is enabled, then the frame is accepted and the MISS bit in the receive buffer descriptor is set; otherwise, the frame is rejected.

In general, when a frame is rejected, it is flushed from the FIFO.



NOTES:
BC_REJ - field in RCR register (BroadCast REJect)
PROM - field in RCR register (PROMiscous mode)
Pause Frame - valid Pause frame received

Figure 15-28. Ethernet Address Recognition—Receive Block Decisions



NOTES:
FCE - field in RCR register (Flow Control Enable)
I/G - Individual/Group bit in Destination Address (least significant bit in first byte received in MAC frame)

Figure 15-29. Ethernet Address Recognition—Microcode Decisions

15.4.9 Hash Algorithm

The hash table algorithm used in the group and individual hash filtering operates as follows. The 48-bit destination address is mapped into one of 64 bits, which are represented by 64 bits stored in GAUR, GALR (group address hash match) or IAUR, IALR (individual address hash match). This mapping is performed by passing the 48-bit address through the on-chip 32-bit CRC generator and selecting the 6 most significant bits of the CRC-encoded result to generate a number between 0 and 63. The MSB of the CRC result selects GAUR (MSB = 1) or GALR (MSB = 0). The least significant 5 bits of the hash result select the bit within the selected register. If the CRC generator selects a bit that is set in the hash table, the frame is accepted; otherwise, it is rejected.

For example, if eight group addresses are stored in the hash table and random group addresses are received, the hash table prevents roughly 56/64 (or 87.5%) of the group address frames from reaching memory. Those that do reach memory must be further filtered by the processor to determine if they truly contain one of the eight desired addresses.

The effectiveness of the hash table declines as the number of addresses increases.

The hash table registers must be initialized by the application. The CRC32 polynomial to use in computing the hash is:

$$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$$

A table of example Destination Addresses and corresponding hash values is included below for reference.

Table 15-34. Destination Address to 6-Bit Hash

48-bit DA	6-bit Hash (in hex)	Hash Decimal Value
65:ff:ff:ff:ff:ff	0x0	0
55:ff:ff:ff:ff:ff	0x1	1
15:ff:ff:ff:ff:ff	0x2	2
35:ff:ff:ff:ff:ff	0x3	3
B5:ff:ff:ff:ff:ff	0x4	4
95:ff:ff:ff:ff:ff	0x5	5
D5:ff:ff:ff:ff:ff	0x6	6
F5:ff:ff:ff:ff:ff	0x7	7
DB:ff:ff:ff:ff:ff	0x8	8
FB:ff:ff:ff:ff:ff	0x9	9
BB:ff:ff:ff:ff:ff	0xA	10
8B:ff:ff:ff:ff:ff	0xB	11
0B:ff:ff:ff:ff:ff	0xC	12
3B:ff:ff:ff:ff:ff	0xD	13
7B:ff:ff:ff:ff:ff	0xE	14
5B:ff:ff:ff:ff:ff	0xF	15
27:ff:ff:ff:ff:ff	0x10	16
07:ff:ff:ff:ff:ff	0x11	17
57:ff:ff:ff:ff:ff	0x12	18
77:ff:ff:ff:ff:ff	0x13	19
F7:ff:ff:ff:ff:ff	0x14	20
C7:ff:ff:ff:ff:ff	0x15	21
97:ff:ff:ff:ff:ff	0x16	22
A7:ff:ff:ff:ff:ff	0x17	23
99:ff:ff:ff:ff:ff	0x18	24
B9:ff:ff:ff:ff:ff	0x19	25
F9:ff:ff:ff:ff:ff	0x1A	26

Table 15-34. Destination Address to 6-Bit Hash (continued)

48-bit DA	6-bit Hash (in hex)	Hash Decimal Value
C9:ff:ff:ff:ff:ff	0x1B	27
59:ff:ff:ff:ff:ff	0x1C	28
79:ff:ff:ff:ff:ff	0x1D	29
29:ff:ff:ff:ff:ff	0x1E	30
19:ff:ff:ff:ff:ff	0x1F	31
D1:ff:ff:ff:ff:ff	0x20	32
F1:ff:ff:ff:ff:ff	0x21	33
B1:ff:ff:ff:ff:ff	0x22	34
91:ff:ff:ff:ff:ff	0x23	35
11:ff:ff:ff:ff:ff	0x24	36
31:ff:ff:ff:ff:ff	0x25	37
71:ff:ff:ff:ff:ff	0x26	38
51:ff:ff:ff:ff:ff	0x27	39
7F:ff:ff:ff:ff:ff	0x28	40
4F:ff:ff:ff:ff:ff	0x29	41
1F:ff:ff:ff:ff:ff	0x2A	42
3F:ff:ff:ff:ff:ff	0x2B	43
BF:ff:ff:ff:ff:ff	0x2C	44
9F:ff:ff:ff:ff:ff	0x2D	45
DF:ff:ff:ff:ff:ff	0x2E	46
EF:ff:ff:ff:ff:ff	0x2F	47
93:ff:ff:ff:ff:ff	0x30	48
B3:ff:ff:ff:ff:ff	0x31	49
F3:ff:ff:ff:ff:ff	0x32	50
D3:ff:ff:ff:ff:ff	0x33	51
53:ff:ff:ff:ff:ff	0x34	52
73:ff:ff:ff:ff:ff	0x35	53
23:ff:ff:ff:ff:ff	0x36	54
13:ff:ff:ff:ff:ff	0x37	55
3D:ff:ff:ff:ff:ff	0x38	56
0D:ff:ff:ff:ff:ff	0x39	57
5D:ff:ff:ff:ff:ff	0x3A	58

Table 15-34. Destination Address to 6-Bit Hash (continued)

48-bit DA	6-bit Hash (in hex)	Hash Decimal Value
7D:ff:ff:ff:ff:ff	0x3B	59
FD:ff:ff:ff:ff:ff	0x3C	60
DD:ff:ff:ff:ff:ff	0x3D	61
9D:ff:ff:ff:ff:ff	0x3E	62
BD:ff:ff:ff:ff:ff	0x3F	63

15.4.10 Full Duplex Flow Control

Full-duplex flow control allows the application to transmit pause frames and to detect received pause frames. Upon detection of a pause frame, MAC data frame transmission stops for a given pause duration.

To enable pause frame detection, the FEC must operate in full-duplex mode (TCR[FDEN] asserted) and flow control enable (RCR[FCE]) must be asserted. The FEC detects a pause frame when the fields of the incoming frame match the pause frame specifications, as shown in the table below. In addition, the receive status associated with the frame must indicate that the frame is valid.

Table 15-35. PAUSE Frame Field Specification

48-bit Destination Address	0x0180_C200_0001 or Physical Address
48-bit Source Address	Any
16-bit TYPE	0x8808
16-bit OPCODE	0x0001
16-bit PAUSE_DUR	0x0000–0xFFFF

Pause frame detection is performed by the receiver and microcontroller modules. The microcontroller runs an address recognition subroutine to detect the specified pause frame destination address, while the receiver detects the TYPE and OPCODE pause frame fields. On detection of a pause frame, TCR[GTS] is asserted by the FEC internally. When transmission has paused, the EIR[GRA] interrupt is asserted and the pause timer begins to increment. Note that the pause timer makes use of the transmit backoff timer hardware, which is used for tracking the appropriate collision backoff time in half-duplex mode. The pause timer increments once every slot time, until OPD[PAUSE_DUR] slot times have expired. On OPD[PAUSE_DUR] expiration, TCR[GTS] is deasserted allowing MAC data frame transmission to resume. Note that the receive flow control pause (TCR[RFC_PAUSE]) status bit is asserted while the transmitter is paused due to reception of a pause frame.

To transmit a pause frame, the FEC must operate in full-duplex mode and the application must assert flow control pause (TCR[TFC_PAUSE]). On assertion of transmit flow control pause (TCR[TFC_PAUSE]), the transmitter asserts TCR[GTS] internally. When the transmission of data frames stops, the EIR[GRA] (graceful stop complete) interrupt asserts. Following EIR[GRA] assertion, the pause frame is transmitted. On completion of pause frame transmission, flow control pause (TCR[TFC_PAUSE]) and TCR[GTS] are deasserted internally.

The application must specify the desired pause duration in the OPD register.

Note that when the transmitter is paused due to receiver/microcontroller pause frame detection, transmit flow control pause (TCR[TFC_PAUSE]) still can be asserted and causes the transmission of a single pause frame. In this case, the EIR[GRA] interrupt is not asserted.

15.4.11 Inter-Packet Gap (IPG) Time

The minimum inter-packet gap time for back-to-back transmission is 96 bit times. After completing a transmission or after the backoff algorithm completes, the transmitter waits for carrier sense to be negated before starting its 96 bit time IPG counter. Frame transmission can begin 96 bit times after carrier sense is negated if it stays negated for at least 60 bit times. If carrier sense asserts during the last 36 bit times, it is ignored and a collision occurs.

The receiver receives back-to-back frames with a minimum spacing of at least 28 bit times. If an inter-packet gap between receive frames is less than 28 bit times, the following frame can be discarded by the receiver.

15.4.12 Collision Handling

If a collision occurs during frame transmission, the Ethernet controller continues the transmission for at least 32 bit times, transmitting a JAM pattern consisting of 32 ones. If the collision occurs during the preamble sequence, the JAM pattern is sent after the end of the preamble sequence.

If a collision occurs within 512 bit times, the retry process is initiated. The transmitter waits a random number of slot times. A slot time is 512 bit times. If a collision occurs after 512 bit times, then no retransmission is performed and the end of frame buffer is closed with a late collision (LC) error indication.

15.4.13 Internal and External Loopback

Both internal and external loopback are supported by the Ethernet controller. In loopback mode, both of the FIFOs are used and the FEC actually operates in a full-duplex fashion. Both internal and external loopback are configured using combinations of the LOOP and DRT bits in the RCR register and the FDEN bit in the TCR register.

For both internal and external loopback set FDEN = 1.

For internal loopback set RCR[LOOP] = 1 and RCR[DRT] = 0. FEC_TX_EN and FEC_TX_ER do not assert during internal loopback. During internal loopback, the transmit/receive data rate is higher than in normal operation because the internal system clock is used by the transmit and receive blocks instead of the clocks from the external transceiver. This causes an increase in the required system bus bandwidth for transmission and the DMA must move data to and from external memory. Pace the frames on the transmit side or limit the size of the frames to prevent transmit FIFO underrun and receive FIFO overflow.

For external loopback set RCR[LOOP] = 0, RCR[DRT] = 0 and configure the external transceiver for loopback.

15.4.14 Ethernet Error-Handling Procedure

The Ethernet controller reports frame reception and transmission error conditions using the FEC RxBDs, the EIR register, and the MIB block counters.

15.4.14.1 Transmission Errors

15.4.14.1.1 Transmitter Underrun

If this error occurs, the FEC sends 32 bits that ensure a CRC error and stops transmitting. All remaining buffers for that frame are then flushed and closed. The UN bit is set in the EIR. The FEC then continues to the next transmit buffer descriptor and begin transmitting the next frame.

The “UN” interrupt is asserted if enabled in the EIMR register.

15.4.14.1.2 Retransmission Attempts Limit Expired

When this error occurs, the FEC terminates transmission. All remaining buffers for that frame are flushed and closed, and the RL bit is set in the EIR. The FEC then continues to the next transmit buffer descriptor and begin transmitting the next frame.

The “RL” interrupt is asserted if enabled in the EIMR register.

15.4.14.1.3 Late Collision

When a collision occurs after the slot time (512 bits starting at the preamble), the FEC terminates transmission. All remaining buffers for that frame are flushed and closed, and the LC bit is set in the EIR register. The FEC then continues to the next transmit buffer descriptor and begin transmitting the next frame.

The “LC” interrupt is asserted if enabled in the EIMR register.

15.4.14.1.4 Heartbeat

Some transceivers have a self-test feature called ‘heartbeat’ or ‘signal quality error.’ To signify a good self-test, the transceiver indicates a collision to the FEC within 4 microseconds after completion of a frame transmitted by the Ethernet controller. This indication of a collision does not imply a real collision error on the network, but is rather an indication that the transceiver still seems to be functioning properly. This is called the heartbeat condition.

If the HBC bit is set in the TCR register and the heartbeat condition is not detected by the FEC after a frame transmission, then a heartbeat error occurs. When this error occurs, the FEC closes the buffer, sets the HB bit in the EIR register, and generates the HBERR interrupt if it is enabled.

15.4.14.2 Reception Errors

15.4.14.2.1 Overrun Error

If the receive block has data to put into the receive FIFO and the receive FIFO is full, the FEC sets the OV bit in the RxBD. All subsequent data in the frame is discarded and subsequent frames can also be discarded until the receive FIFO is serviced by the DMA and space is made available. At this point the receive frame/status word is written into the FIFO with the OV bit set. This frame must be discarded by the driver.

15.4.14.2.2 Non-Octet Error (Dribbling Bits)

The Ethernet controller handles up to seven dribbling bits when the receive frame terminates past an non-octet aligned boundary. Dribbling bits are not used in the CRC calculation. If there is a CRC error, then the frame non-octet aligned (NO) error is reported in the RxBD. If there is no CRC error, then no error is reported.

15.4.14.2.3 CRC Error

When a CRC error occurs with no dribble bits, the FEC closes the buffer and sets the CR bit in the RxBD. CRC checking cannot be disabled, but the CRC error can be ignored if checking is not required.

15.4.14.2.4 Frame Length Violation

When the receive frame length exceeds MAX_FL bytes, the BABR interrupt is generated, and the LG bit in the end of frame RxBD is set. The frame is not truncated unless the frame length exceeds 2047 bytes).

15.4.14.2.5 Truncation

When the receive frame length exceeds 2047 bytes the frame is truncated, and the TR bit is set in the RxBD.

15.5 Buffer Descriptors

This section provides a description of the operation of the driver/DMA via the buffer descriptors. It is followed by a detailed description of the receive and transmit descriptor fields.

15.5.1 Driver/DMA Operation with Buffer Descriptors

The data for the FEC frames must reside in memory external to the FEC. The data for a frame is placed in one or more buffers. Associated with each buffer is a buffer descriptor (BD) which contains a starting address (pointer), data length, and status/control information (which contains the current state for the buffer). To permit maximum flexibility, the BDs are also located in external memory and are read in by the FEC DMA engine.

Software “produces” buffers by allocating/initializing memory and initializing buffer descriptors. Setting the RxBD[E] or TxBD[R] bit “produces” the buffer. Software writing to either the TDAR or RDAR tells the FEC that a buffer has been placed in external memory for the transmit or receive data traffic, respectively. The hardware reads the BDs and “consumes” the buffers after they have been produced. After

the data DMA is complete and the buffer descriptor status bits have been written by the DMA engine, the RxBD[E] or TxBD[R] bit is cleared by hardware to signal that the buffer has been “consumed.” Software can poll the BDs to detect when the buffers were consumed or can rely on the buffer/frame interrupts. These buffers can then be processed by the driver and returned to the free list.

The ECR[ETHER_EN] signal operates as a reset to the BD/DMA logic. When ECR[ETHER_EN] is deasserted the DMA engine BD pointers are reset to point to the starting transmit and receive BDs. The buffer descriptors are not initialized by hardware during reset. At least one transmit and receive buffer descriptor must be initialized by software before the ECR[ETHER_EN] bit is set.

The buffer descriptors operate as two separate rings. ERDSR defines the starting address for receive BDs and ETDSR defines the starting address for transmit BDs. The last buffer descriptor in each ring is defined by the wrap (W) bit. When set, W indicates that the next descriptor in the ring is at the location pointed to by ERDSR and ETDSR for the receive and transmit rings, respectively. Buffer descriptor rings must start on a 32-bit boundary; however, it is recommended they are made 128-bit aligned.

15.5.1.1 Driver/DMA Operation with Transmit BDs

Typically a transmit frame is divided between multiple buffers. An example is to have an application payload in one buffer, TCP header in a second buffer, IP header in a third buffer, Ethernet/IEEE® 802.3 header in a fourth buffer. The Ethernet MAC does not prepend the Ethernet header (destination address, source address, length/type fields), so this must be provided by the driver in one of the transmit buffers. The Ethernet MAC can append the Ethernet CRC to the frame. Whether the CRC is appended by the MAC or by the driver is determined by the TC bit in the transmit BD which must be set by the driver.

The driver (TxBD software producer) must set up Tx BDs in such a way that a complete transmit frame is given to the hardware at once. If a transmit frame consists of three buffers, the BDs must be initialized with pointer, length and control (W, L, TC, ABC) and then the TxBD[R] bits must be set = 1 in reverse order (3rd, 2nd, 1st BD) to insure that the complete frame is ready in memory before the DMA begins. If the TxBDs are set up in order, the DMA Controller can DMA the first BD before the second becomes available, potentially causing a transmit FIFO underrun.

In the FEC, the DMA is notified by the driver that new transmit frames are available by writing to the TDAR register. When this register is written to (data value is not significant) the FEC sends a DMA request to read the next transmit BD in the ring. Once started, the FEC and DMA continue to read and interpret transmit BDs in order, and DMA the associated buffers, until a transmit BD is encountered with the R bit = 0. At this point the FEC polls this BD one more time. If the R bit = 0 the second time, then the FEC stops the transmit descriptor read process until software sets up another transmit frame and writes to TDAR.

When the DMA of each transmit buffer is complete, the DMA writes back to the BD to clear the R bit, indicating that the hardware consumer is finished with the buffer.

15.5.1.2 Driver and DMA Operations with Receive BDs

Unlike transmit, the length of the receive frame is unknown by the driver ahead of time. Therefore the driver must set a variable to define the length of all receive buffers. In the FEC, this variable is written to the EMRBR register.

The driver (RxBD software producer) must set up some number of “empty” buffers for the Ethernet by initializing the address field and the E and W bits of the receive BDs. The receive DMA consumes the buffers by:

- Filling them with data as frames are received
- Clearing the E bit to 0
- Setting the L bit to 1 to indicate the last buffer in the frame,
- Setting the frame status bits (if L = 1) and the length field.

If a receive frame spans multiple receive buffers, the L bit is only set for the last buffer in the frame. For non-last buffers, the length field in the receive BD is written by the DMA (at the same time the E bit is cleared) with the default receive buffer length value. For end-of-frame buffers, the receive BD is written with L = 1 and information is written to the status bits (M, BC, MC, LG, NO, CR, OV, TR). Some of the status bits are error indicators which, if set, indicate the receive frame must be discarded and not given to higher layers. The frame status/length information is written into the receive FIFO following the end of the frame (as a single 32-bit word) by the receive logic. The length field for the end-of-frame buffer is written with the length of the entire frame, not just the length of the last buffer.

For simplicity, the driver can assign a default receive buffer length large enough to contain an entire frame, keeping in mind that a malfunction on the network or an implementation that is not within the specification can result in giant frames. Frames of 2K (2048) bytes or larger are truncated by the FEC at 2047 bytes to guarantee the application never receives frame larger than 2047 bytes.

Similar to transmit, the FEC polls the receive descriptor ring after the driver sets up receive BDs and writes to the RDAR register. As frames are received, the FEC fills the receive buffers and updates the associated BDs, then reads the next BD in the receive descriptor ring. If the FEC reads a receive BD and finds the E bit = 0, it polls the BD again. If BD = 0 a second time, the FEC stops reading the receive BDs until the driver writes to RDAR.

15.5.2 Ethernet Receive Buffer Descriptor (RxBD)

In the RxBD, the application initializes the E and W bits in the first word and the pointer in second word. When the buffer has been DMA’d, the Ethernet controller modifies the E, L, M, BC, MC, LG, NO, CR, OV, and TR bits and writes the length of the used portion of the buffer in the first word. The M, BC, MC, LG, NO, CR, OV and TR bits in the first word of the buffer descriptor are only modified by the Ethernet controller when the L bit is set to 1.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Offset + 0	E	RO1	W	RO2	L	—	—	M	BC	MC	LG	NO	—	CR	OV	TR
Offset + 2	Data Length															
Offset + 4	Rx Data Buffer Pointer - A [0:15]															
Offset + 6	Rx Data Buffer Pointer - A [16:31]															

Figure 15-30. Receive Buffer Descriptor (RxBD)

Table 15-36. Receive Buffer Descriptor Field Definitions

Halfword	Location	Field Name	Description
Offset + 0	Bit 0	E	Empty. Written by the FEC (=0) and application (=1). 0 The data buffer associated with this BD has been filled with received data, or data reception has been aborted due to an error condition. The status and length fields have been updated as required. 1 The data buffer associated with this BD is empty, or reception is currently in progress.
Offset + 0	Bit 1	RO1	Receive software ownership. This field is reserved for use by software. This read/write bit is not modified by hardware, nor does its value affect hardware.
Offset + 0	Bit 2	W	Wrap. Written by the application. 0 The next buffer descriptor is found in the consecutive location 1 The next buffer descriptor is found at the location defined in ERDSR.
Offset + 0	Bit 3	RO2	Receive software ownership. This field is reserved for use by software. This read/write bit is not modified by hardware, nor does its value affect hardware.
Offset + 0	Bit 4	L	Last in frame. Written by the FEC. 0 The buffer is not the last in a frame. 1 The buffer is the last in a frame.
Offset + 0	Bits 5–6	—	Reserved.
Offset + 0	Bit 7	M	Miss. Written by the FEC. This bit is set by the FEC for frames that were accepted in promiscuous mode, but were flagged as a “miss” by the internal address recognition. Thus, while in promiscuous mode, the application can use the M-bit to quickly determine whether the frame was destined to this station. This bit is valid only if the L-bit is set and the PROM bit is set. 0 The frame was received because of an address recognition hit. 1 The frame was received because of promiscuous mode.
Offset + 0	Bit 8	BC	Is set if the DA is broadcast (FF-FF-FF-FF-FF-FF).
Offset + 0	Bit 9	MC	Is set if the DA is multicast and not BC.
Offset + 0	Bit 10	LG	Rx frame length violation. Written by the FEC. A frame length greater than RCR[MAX_FL] was recognized. This bit is valid only if the L-bit is set. The receive data is not altered in any way unless the length exceeds 2047 bytes.
Offset + 0	Bit 11	NO	Receive non-octet aligned frame. Written by the FEC. A frame that contained a number of bits not divisible by 8 was received, and the CRC check that occurred at the preceding byte boundary generated an error. This bit is valid only if the L-bit is set. If this bit is set the CR bit is not set.
Offset + 0	Bit 12	—	Reserved.

Table 15-36. Receive Buffer Descriptor Field Definitions (continued)

Halfword	Location	Field Name	Description
Offset + 0	Bit 13	CR	Receive CRC error. Written by the FEC. This frame contains a CRC error and is an integral number of octets in length. This bit is valid only if the L-bit is set.
Offset + 0	Bit 14	OV	Overrun. Written by the FEC. A receive FIFO overrun occurred during frame reception. If this bit is set, the other status bits, M, LG, NO, CR, and CL lose their normal meaning and are cleared to zero. This bit is valid only if the L-bit is set.
Offset + 0	Bit 15	TR	Is set if the receive frame is truncated (frame length > 2047 bytes). If the TR bit is set, the frame must be discarded and the other error bits must be ignored because their validity cannot be verified.
Offset + 2	Bits [0:15]	Data Length	Data length. Written by the FEC. Data length is the number of 8-bit data groups (octets) written by the FEC into this BD's data buffer if L = 0 (the value is equal to EMRBR), or the length of the frame including CRC if L = 1. It is written by the FEC once as the BD is closed.
Offset + 4	Bits [0:15]	A[0:15]	RX data buffer pointer, bits [0:15][1]
Offset + 6	Bits [0:15]	A[16:31]	RX data buffer pointer, bits [16:31]

[1] The receive buffer pointer, which contains the address of the associated data buffer, must always be evenly divisible by 16. The buffer must reside in memory external to the FEC. This value is never modified by the Ethernet controller.

NOTE

Whenever the software driver sets an E bit in one or more receive descriptors, the driver must follow that with a write to RDAR.

15.5.3 Ethernet Transmit Buffer Descriptor (TxBD)

Data is presented to the FEC for transmission by arranging it in buffers referenced by the channel's TxBDs. The Ethernet controller confirms transmission by clearing the ready bit (R bit) when DMA of the buffer is complete. In the TxBD the application initializes the R, W, L, and TC bits and the length (in bytes) in the first word, and the buffer pointer in the second word.

The FEC sets the R bit = 0 in the first word of the BD when the buffer has been DMA'd. Status bits for the buffer/frame are not included in the transmit buffer descriptors. Transmit frame status is indicated via individual interrupt bits (error conditions) and in statistic counters in the MIB block. See Section 15.3.3, "MIB Block Counters Memory Map" for more details.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Offset + 0	R	TO1	W	TO2	L	TC	ABC	—	—	—	—	—	—	—	—	—
Offset + 2	Data Length															
Offset + 4	Tx Data Buffer Pointer - A [0:15]															
Offset + 6	Tx Data Buffer Pointer - A [16:31]															

Figure 15-31. Transmit Buffer Descriptor (TxBD)

Table 15-37. Transmit Buffer Descriptor Field Definitions

Halfword	Location	Field Name	Description
Offset + 0	Bit 0	R	Ready. Written by the FEC and the application. 0 The data buffer associated with this BD is not ready for transmission. the application can manipulate this BD or its associated data buffer. The FEC clears this bit after the buffer has been transmitted or after an error condition is encountered. 1 The data buffer, which has been prepared for transmission by the application, has not been transmitted or is currently being transmitted. No fields of this BD can be written by the application once this bit is set.
Offset + 0	Bit 1	TO1	Transmit software ownership. This field is reserved for software use. This read/write bit is not modified by hardware, nor does its value affect hardware.
Offset + 0	Bit 2	W	Wrap. Written by the application. 0 The next buffer descriptor is found in the consecutive location 1 The next buffer descriptor is found at the location defined in ETDSR.
Offset + 0	Bit 3	TO2	Transmit software ownership. This field is reserved for use by software. This read/write bit is not modified by hardware, nor does its value affect hardware.
Offset + 0	Bit 4	L	Last in frame. Written by the application. 0 The buffer is not the last in the transmit frame. 1 The buffer is the last in the transmit frame.
Offset + 0	Bit 5	TC	Tx CRC. Written by the application (only valid if L = 1). 0 End transmission immediately after the last data byte. 1 Transmit the CRC sequence after the last data byte.
Offset + 0	Bit 6	ABC	Append invalid CRC. Written by the application (only valid if L = 1). 0 No effect 1 Transmit the CRC sequence inverted after the last data byte (regardless of TC value).
Offset + 0	Bits [7:15]	—	Reserved.

Table 15-37. Transmit Buffer Descriptor Field Definitions (continued)

Halfword	Location	Field Name	Description
Offset + 2	Bits [0:15]	Data Length	Data length, written by the application. Data length is the number of octets the FEC must transmit from this BD's data buffer. It is never modified by the FEC. Bits [0:10] are used by the DMA engine, bits[11:15] are ignored.
Offset + 4	Bits [0:15]	A[0:15]	Tx data buffer pointer, bits [0:15][1]
Offset + 6	Bits [0:15]	A[16:31]	Tx data buffer pointer, bits [16:31].

[1] The transmit buffer pointer, which contains the address of the associated data buffer, must always be evenly divisible by 4. The buffer must reside in memory external to the FEC. This value is never modified by the Ethernet controller.

NOTE

Once the software driver has set up the buffers for a frame, it must set up the corresponding BDs. The last step in setting up the BDs for a transmit frame must be to set the R bit in the first BD for the frame. The driver must follow that with a write to TDAR which triggers the FEC to poll the next BD in the ring.

Chapter 16
Boot Assist Module (BAM)

16.1 Introduction

This chapter describes the boot assist module (BAM).

16.1.1 Overview

The BAM contains the MCU boot program code. The BAM control block is connected to peripheral bridge B and occupies the last 16 KB of the MCU memory space. The BAM program supports several booting modes:

- Internal flash
- External memory without bus arbitration
- External memory with bus arbitration
- Serial boot using an eSCI interface
- Serial boot using a FlexCAN interface

The BAM program is executed by the e200z6 core just after the MCU reset. Depending on the boot mode, the program initializes the minimum MCU resources to start application code execution.

Figure 16-1 is a block diagram of the BAM.

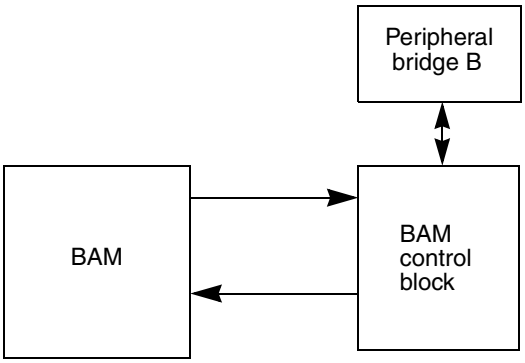


Figure 16-1. BAM Block Diagram

16.1.2 Features

The BAM program provides the following features:

- Initial e200z6 core MMU setup with minimum address translation for all internal MCU resources and external memory address space
- Locate and detect application boot code
- Automatic switch to serial boot mode if internal or external flash is not initialized or invalid
- Programmable 64-bit password protection for serial boot mode
- Boot application code from:
  - Internal flash module
  - external memory without arbitration
  - external memory with arbitration
- Serial boot loads the application boot code from a FlexCAN or eSCI bus into internal SRAM
- Censorship protection for internal flash module
- Enable the e200z6 core watchdog timer
- Configurable memory map for use with the classic PowerPC Book E code or Freescale VLE code
- Configurable external data bus for 16- or 32-bit wide (416 and 496 PBGA packages only)

16.1.3 Modes of Operation

16.1.3.1 Normal Mode

In normal operation, the BAM responds to all read requests within its address space. The BAM program is executed following the negation of reset.

16.1.3.2 Debug Mode

The BAM program is not executed when the MCU comes out of reset in OnCE debug mode. Use the development tool to configure and initialize the MCU before accessing the MCU resources.

16.1.3.3 Internal Boot Mode

Use internal boot mode to boot from internal flash memory. Configuration information, initialization, and boot code are kept in internal flash. The BAM program must complete the boot process before application code can enable the external bus interface.

16.1.3.4 External Boot Modes

Use external boot mode when the boot code and configuration information are located in external memory that is connected to the EBI. Enable bus arbitration for multiprocessor systems to allow a boot option. Do not select external boot mode for devices without an external bus.

16.1.3.5 Serial Boot Mode

This mode of operation can load a user program into internal SRAM using either the eSCI or FlexCAN serial interface, then execute the downloaded program. The program can then control the downloading of data, as well as erasing and programming the internal or external flash memory.

Serial boot mode downloads:

- 64-bit password
- 32-bit start address
- 32-bit download consisting of 1-bit VLE flag (most significant bit)
  followed by a 31-bit length field containing the number of bytes to receive (download length)

Set the VLE flag to 1 for devices that support variable length encoding and must run in VLE mode. When the VLE flag is set, the BAM programs the external bus interface (EBI), RAM, and the flash memory map unit (MMU) TLB entries 1, 2, and 3 with the VLE attribute.

Clear the VLE bit to 0 for devices that use the PowerPC Book E or Power Architecture instruction set mode.

16.2 Memory Map

The BAM has 16 KB of memory, from 0xFFFF_C000 through 0xFFFF_FFFF, which is divided into four 4-KB segments, each containing a copy of the BAM program code. The BAM code resides in the 4-KB memory segment beginning at 0xFFFF_F000. A copy of the BAM code resides in the three preceding 4-KB segment, as shown in Table 16-1. The BAM program executes from the reset vector at address 0xFFFF_FFFC.

Table 16-1 shows the addresses for the BAM code in the memory map.

Table 16-1. BAM Memory Map

Address	Description
0xFFFF_C000–0xFFFF_CFFF	BAM program mirrored
0xFFFF_D000–0xFFFF_DFFF	BAM program mirrored
0xFFFF_E000–0xFFFF_EFFF	BAM program mirrored
0xFFFF_F000–0xFFFF_FFFF	BAM program

16.3 Functional Description

16.3.1 BAM Program Resources

The BAM program initializes and uses the following MCU resources:

- BOOTCFG field in the reset status register (SIU_RSR) to determine the boot option
- Address and contents of the reset configuration halfword (RCHW), which contains the address and configuration options for the boot code. Refer to Chapter 4, “Reset,” for information about the RCHW.

- DISNEX bit in the SIU_CCR register to determine if the Nexus port is enabled
- MMU allows core access to MCU internal resources and the EBI
- EBI registers and external bus pads, when using external boot modes
- FlexCAN A, eSCI A and their pads, when using serial boot mode
- eDMA during serial boot mode

16.3.2 BAM Program Operation

The MCU core accesses the BAM after $\overline{\text{RSTOUT}}$ negates and before the application program executes.

The BAM program configures the e200z6 core MMU access for all MCU internal resources and external memory, as shown in Table 16-2. The memory map configuration is the same for internal flash boot mode.

Table 16-2. MMU Configuration for Internal Flash Boot

TLB Entry	Region	Attributes	Logical Base Address	Physical Base Address	Size
0	Peripheral bridge B and BAM	• Cache inhibited • Guarded • Big endian • Global PID	0xFFF0_0000	0xFFF0_0000	1 MB
1	Internal flash	• Cache enabled • Not guarded • Big endian • Global PID	0x0000_0000	0x0000_0000	16 MB
2	EBI	• Cache enabled • Not guarded • Big endian • Global PID	0x2000_0000	0x0000_0000	16 MB
3	Internal SRAM	• Cache inhibited • Not guarded • Big endian • Global PID	0x4000_0000	0x4000_0000	256 KB
4	Peripheral bridge A	• Cache inhibited • Guarded • Big endian • Global PID	0xC3F0_0000	0xC3F0_0000	1 MB

MMU maps the logical addresses to the same physical addresses for all modules except for the external bus interface (EBI). The logical EBI addresses are mapped to physical addresses in internal flash memory. This allows code developed to run from external memory to run from internal flash memory.

The BAM program reads the following data and determines the boot mode for the boot sequence:

- BOOTCFG[0:1] located in the reset status register (SIU_RSR)
- Censorship control field located at 0x00FF_FDE0 in the shadow row of internal flash
- Serial boot control field located at 0x00FF_FDE2 in the shadow row of internal flash

The boot mode determines the following:

- Enables or disables internal flash memory
- Enables or disables the Nexus port
- Compares the password received in serial boot mode to a preset public password or a programmable password located in internal flash

Table 16-3 summarizes the different boot modes.

Table 16-3. Boot Modes

BOOTCFG [0:1]	Censorship Control 0x00FF_FDE0	Serial Boot Control 0x00FF_FDE2	Boot Mode Name	Internal Flash State	Nexus State	Serial Password
00	!0x55AA[1]	Any value	Internal—Censored	Enabled	Disabled	Flash
	0x55AA		Internal—Public	Enabled	Enabled	Public
01	Any value	0x55AA	Serial—Flash password	Enabled	Disabled	Flash
		!0x55AA	Serial—Public password	Disabled	Enabled	Public
10	!0x55AA	Any value	External—No arbitration—Censored	Disabled	Enabled	Public
	0x55AA		External—No arbitration—Public	Enabled	Enabled	Public
11	!0x55AA	Any value	External—External arbitration —Censored	Disabled	Enabled	Public
	0x55AA		External—External arbitration —Public	Enabled	Enabled	Public

1 '!' = 'NOT,' as in !0x55AA, which means all values except 0x55AA. Do not use 0x0000 or 0xFFFF for the value of the censorship control or serial boot control words.

The 32-bit censorship word, which contains the censorship control and serial boot control fields, is read and interpreted during the boot process. Its value is used in conjunction with the BOOTCFG[0:1] values to enable or disable the internal flash memory and the Nexus interface. The censorship word is programmed at the factory to contain 0x55AA_55AA, which uses a password in internal flash to activate serial boot mode for an uncensored (public) device.

The censorship word starts at address 0x00FF_FDE0 and contains a 16-bit censorship control field [0:15] and a 16-bit serial boot control field [16:31]. The factory default settings are shown in Figure 16-2:

Address: 0x00FF_FDE0 Value: 0x55AA

MSB	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Binary value	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0
Hex value	5				5				A				A			

Censorship control field–default value configures the device as uncensored.

Address: 0x00FF_FDE2 Value: 0x55AA

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Binary value	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0
Hex value	5				5				A				A			

Serial boot control field–default value reads a password from internal flash.

Figure 16-2. Censorship Word

The BAM program reads the DISNEX bit to determine which of the following passwords to compare with the serial password received in serial boot mode:

- Public password (64-bit constant value of 0xFEED_FACE_CAFE_BEEF); or
- Flash password (64-bit value in the shadow row of internal flash at address 0x00FF_FDD8).

Serial boot flash password starts at address 0x00FF_FDD8:

Address: 0x00FF_FDD8 Value: 0xFEED

MSB	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Binary value	1	1	1	1	1	1	1	0	1	1	1	0	1	1	0	1
Hex value	F				E				E				D			

Address: 0x00FF_FDDA Value: 0xFACE

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Binary value	1	1	1	1	1	0	1	0	1	1	0	0	1	1	1	0
Hex value	F				A				C				E			

Address: 0x00FF_FDDC Value: 0xCAFE

MSB	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
Binary value	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	0
Hex value	C				A				F				E			

Address: 0x00FF_FDDE Value: 0xBEEF

	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
Binary value	1	0	1	1	1	1	1	0	1	1	1	0	1	1	1	1
Hex value	B				E				E				F			

Figure 16-3. Serial Boot Flash Password

The BAM program continues to make specific initialization in one of the four boot modes.

16.3.2.1 Internal Boot Mode

When the BAM detects internal flash boot mode, a bus error exception handler is invoked to handle corrupt data from internal flash memory and avoid a bus error. The BAM program reads up to six addresses in internal flash to find a valid 16-bit reset configuration halfword (RCHW). If a valid RCHW is read, the BAM program sets the e200z6 watchdog timer enable bit RCHW[WTE]. If a valid RCHW is not read, the BAM program proceeds to serial boot mode.

16.3.2.1.1 Finding the Reset Configuration Halfword

A valid RCHW is a 16-bit value that contains a constant 8-bit boot identifier and configuration bits (refer to Section 4.4.3.5.1, “Reset Configuration Halfword Definition”). The RCHW is the first halfword in one of the six low address flash blocks as shown in Table 16-4.

Table 16-4. Low Address Space (LAS) Block Memory Addresses

Block	Address
0	0x0000_0000
1	0x0000_4000
2	0x0001_0000
3	0x0001_C000
4	0x0002_0000
5	0x0003_0000

If the BAM fails to find a valid RCHW, it assumes the flash is erased or corrupt and switches to serial boot operating mode.

If the value in RCHW is valid, the watchdog timer is enabled by setting the RCHW[WTE] bit, the BAM program fetches the reset vector from BOOT_BLOCK_ADDRESS + 0x0004, and branches to the reset boot vector. The application must have a valid instruction at the reset boot vector address.

BOOT_BLOCK_ADDRESS + 0x0000_0004

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31

Figure 16-4. Reset Boot Vector

If the watchdog timer is enabled for internal boot mode, the watchdog timeout is set to 2.5×2^{17} system clock cycles.

16.3.2.2 External Boot Modes

Use external boot mode to boot an application from an external asynchronous memory device that is connected to the EBI. External boot mode is controlled by $\overline{CS}$[0].

16.3.2.2.1 External Boot MMU Configuration

As shown in Table 16-5, the BAM program sets up two MMU regions differently than in internal flash boot mode (refer to Table 16-2). The internal flash logical addresses are mapped to the physical addresses of the EBI.

Table 16-5. MMU Configuration for External Boot Mode

TLB Entry	Region	Attributes	Logical Base Address	Physical Base Address	Size
1	Internal flash memory	• Cache enabled • Not guarded • Big endian • Global PID	0x0000_0000	0x2000_0000	16 MB
2	EBI	• Cache enabled • Not guarded • Big endian • Global PID	0x2000_0000	0x2000_0000	16 MB

This allows code written to run from internal flash memory to execute from external memory.

16.3.2.2.2 Single Bus Master or Multiple Bus Masters

External boot mode has two options for booting:

- External boot with no arbitration — Use this mode for single-master systems where the MCU is the only bus master, therefore no arbitration of the external bus is necessary. Refer to Section 16.3.2.2.3, "Configure the EBI for External Boot—Single Master with no Arbitration."
- External boot with external arbitration — Use this mode for multi-master systems where more than one bus master uses the external bus and bus arbitration is handled external to the MCU. Refer to Section 16.3.2.2.4, "Configure the EBI for External Boot with External Arbitration Mode."

In a multi-master system where both masters boot from the same external bus memory, configure one master to use external boot with no arbitration mode, and configure all other masters to boot using external boot with external arbitration mode. The EBI configuration differs for these modes.

The boot modes are specified by the BOOTCFG[0:1] value. Refer to the following section for more information:

Section 12.4.2.10, "Bus Operation in External Master Mode"

16.3.2.2.3 Configure the EBI for External Boot—Single Master with no Arbitration

The BAM program configures:

- Chip select $\overline{CS}$[0] as a 16-bit port starting at base address 0x2000_0000 with:
  - no burst
  - 15 wait states
  - 8 MB
- EBI for no external master (clears EXTM bit)
- Enables the EBI for normal operation
- Configures the following EBI signals:
  - ADDR[8:31]
  - DATA[0:15]
  - $\overline{WE}$[0]
  - $\overline{OE}$
  - $\overline{TS}$
  - $\overline{CS}$[0]

16.3.2.2.4 Configure the EBI for External Boot with External Arbitration Mode

NOTE

Some signals listed in this section are not implemented on all device packages. Refer to Chapter 12, "External Bus Interface (EBI)," for more information.

To use external boot mode with external arbitration, the BAM program must also configure the following bits in addition to the bits set for External Boot with no Arbitration mode:

- Sets the EXTM bit that enables the EBI for external master operation
- Configures the EBI for external arbitration by setting the EARB bit.
- Configures the EBI signals $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ for bus arbitration. Refer to Table 16-6.

Table 16-6. External Bus Interface Configuration

Pins [1]	Function After Device Reset	Function and Value After BAM Execution				
		Serial Boot Mode [2] or Internal Boot Mode	External Boot with no Arbitration [3] (Single-master Mode)		External Boot with External Arbitration [3] (Multi-master Mode)	
	Function	Function	Function	PCR Value	Function	PCR Value
ADDR[8:31]	GPIO	GPIO	ADDR[8:31]	0x0440	ADDR[8:31]	0x0440
DATA[16:31]	GPIO	GPIO	GPIO or DATA[16:31] [4]	Default or 0x1440 [4]	GPIO or DATA[16:31] [4]	Default or 0x1440 [4]
DATA[0:15]	GPIO	GPIO	DATA[0:15]	0x0440	DATA[0:15]	0x0440
$\overline{TEA}$	GPIO	GPIO	GPIO	Default [5]	GPIO	Default [5]
$\overline{CS}$[0]	GPIO	GPIO	CS[0]	0x0443	$\overline{CS}$[0]	0x0443
$\overline{CS}$[1:3]	GPIO	GPIO	GPIO	Default [5]	GPIO	Default [5]
$\overline{WE}/\overline{BE}$[0]	GPIO	GPIO	$\overline{WE}$[0]	0x0443	$\overline{WE}/\overline{BE}$[0]	0x0443
$\overline{WE}/\overline{BE}$[1:3]	GPIO	GPIO	GPIO	Default [5]	GPIO	Default [5]
$\overline{OE}$	GPIO	GPIO	$\overline{OE}$	0x0443	$\overline{OE}$	0x0443
$\overline{TS}$	GPIO	GPIO	$\overline{TS}$	0x0443	$\overline{TS}$	0x0443
$\overline{TA}$	GPIO	GPIO	GPIO	Default [5]	GPIO	Default [5]
RD_$\overline{WR}$	GPIO	GPIO	GPIO	Default [5]	GPIO	Default [5]
BDIP	GPIO	GPIO	GPIO	Default [5]	GPIO	Default [5]
$\overline{BB}$	GPIO	GPIO	GPIO	Default [5]	$\overline{BB}$	0X0443
$\overline{BG}$	GPIO	GPIO	GPIO	Default [5]	$\overline{BG}$	0X0443
$\overline{BR}$	GPIO	GPIO	GPIO	Default [5]	$\overline{BR}$	0X0443
TSIZ[0:1]	GPIO	GPIO	GPIO	Default [5]	GPIO	Default [5]

1 Refer to Chapter 12, “External Bus Interface (EBI),” since some signals are not implemented on all devices.

2 These values are for serial boot mode only when entered directly using the BOOTCFG signals.

3 If serial boot is entered indirectly from external boot mode because a valid RCHW was not found, the EBI remains configured according to these columns.

4 If the BAM reads a valid RCHW with the PS0 bit clear, DATA[16:31] are reconfigured from GPIO to data bus signals by writing 0x0440 to the pad configuration registers (PCRs).

5 The BAM does not write to the PCR for this signal; the value is the PCR default value. Refer to Chapter 6, “System Integration Unit (SIU)” for the signal PCR default values.

16.3.2.2.5 Read the Reset Configuration Halfword

The BAM program reads the first location in external memory, i.e address 0x2000_0000, for a valid reset configuration halfword (RCHW, refer to Figure 16-4). If the BAM program finds a valid RCHW, the following occurs:

- The $\overline{CS}$[0] port size and data pins are configured according to the RCHW[PS0] bit
- The e200z6 core watchdog timeout is enabled or disabled using the RCHW[WTE] bit. The watchdog timeout interval is 2.5×2^{17} system clock periods when using the RCHW.
- MMU boots using PowerPC Book E code or Freescale VLE code according to the RCHW[VLE] setting.

Then the BAM program reads the reset vector shown in Figure 16-4 from the address 0x2000_0004 and branches to that reset vector address, starting application program execution.

16.3.2.3 Serial Boot Mode Operation

Serial boot operating mode configures:

- FlexCAN A and the eSCI A GPIO signals
- Unused message buffers in FlexCAN A are designated as scratch pad SRAM
- Flash memory map unit (MMU) TLB entries
- Watchdog timer is enabled and set to 2.5×2^{27} system clock cycles

Serial boot mode downloads:

- 64-bit password
- 32-bit start address
- 32-bit download consisting of a 1-bit VLE flag followed by a 31-bit length field

Set the VLE flag to 1 for devices that support variable length encoding and must run in VLE mode. When the VLE flag is set, the BAM configures these components:

- External bus interface (EBI) signals and port size
- SRAM structure
- VLE attribute is set in flash memory map unit (MMU) TLB entries 1, 2, and 3

Clear the VLE bit to 0 for devices that use the PowerPC Book E or Power Architecture instruction set mode.

16.3.2.3.1 Serial Boot Mode MMU and EBI Configuration

The BAM program sets up the MMU for all peripheral and memory regions in one of two different modes and sets up the EBI in one of three different modes; depending on how serial boot mode was entered.

If serial boot mode is entered directly by choosing the mode with the BOOTCFG signals, or was entered indirectly from internal boot mode because no valid RCHW was found, then the MMU is configured the same way as for internal boot mode. The EBI is disabled and all bus pins function as GPIO.

If serial boot mode is entered indirectly from external boot/single-master or external boot/multi-master/external arbitration because no valid RCHW was found, then the MMU and EBI are configured the for an external boot mode with a 16-bit data bus.

Refer to Table 16-3 and Table 16-5 for more information.

16.3.2.3.2 Serial Boot Mode FlexCAN and eSCI Configuration

In serial boot mode, the BAM program configures FlexCAN A and eSCI A to receive messages. The CNRXA and RXDA signals are configured as inputs to the FlexCAN and eSCI modules. The CNTXA signal is configured as an output from the FlexCAN module. The TXDA signal of the eSCI A remains configured as GPIO input. The BAM program writes 0x0000_0000_0000_0000 to the e200z6 core timebase registers (TB), enables the e200z6 core setting the watchdog timer to use 2.5×2^{27} system clock cycles before a reset occurs.

Refer to for examples of time out periods.

In serial boot mode the FlexCAN controller is configured to operate at a baud (bit) rate equal to the system clock frequency divided by 60 with one message buffer (MB) using the standard 11-bit identifier format detailed in the CAN 2.0A specification.

Refer to Section 22.4.5.4, “Protocol Timing,” for information on FlexCAN bit rate generation.

Coming out of reset, the default system clock is 1.5 times the crystal frequency. The baud rate with PLL enabled is equal to the crystal frequency divided by 40.

Refer to Chapter 11, “Frequency Modulated Phase Locked Loop and System Clocks (FMPLL),” for more information. Table 16-7 shows FlexCAN operation at reset.

Table 16-7. BAM FlexCAN Frequency at Reset (FMPLL Enabled out of Reset)

FMPLL Clock Mode	System Clock Frequency (f_{sys}) after Reset	Serial Boot Mode Frequency[1] (FlexCAN Baud Rate)
Crystal reference mode or External reference mode	1.5 x crystal reference frequency ($f_{ref\_crystal}$) [2]	Crystal reference frequency ÷ 40
Dual controller mode	2 x EXTCLK	EXTCLK ÷ 30

1 Serial boot mode frequency is set in software as the system clock frequency divided by 60.

2 Crystal reference frequency is set at 8–20 MHz.

The BAM ignores the following errors:

- Bit 1 errors
- Bit 0 errors
- Acknowledge errors
- Cyclic redundancy code errors
- Form errors
- Stuffing errors
- TX error counter errors

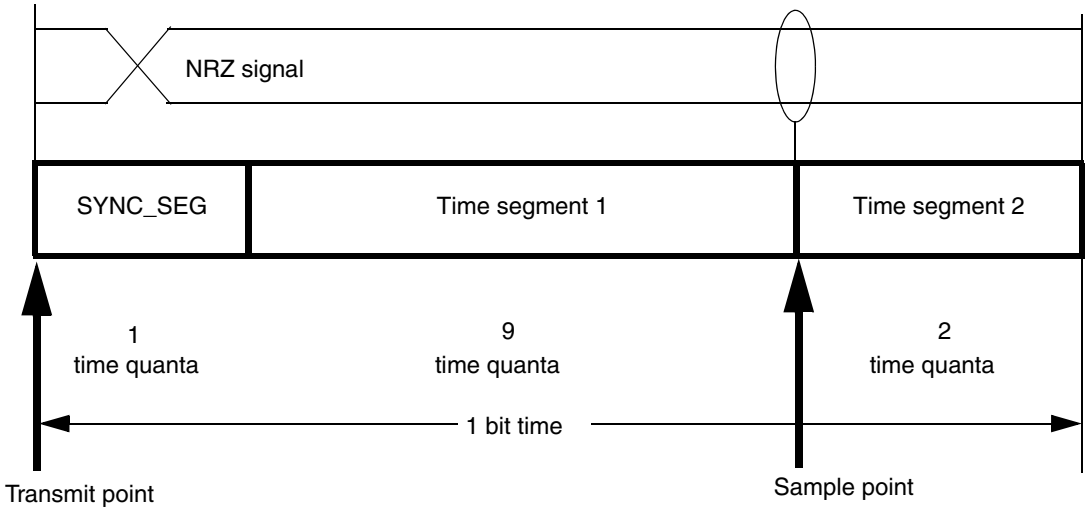
- Rx error counter errors

All data received, regardless of errors, is echoed out on the CNTXA signal.

NOTE

The host computer must compare the ‘echoed data’ to the sent data and restart the process if an error is detected.

Refer to Figure 16-5 for details of FlexCAN bit timing.



1 time quanta = 5 system clock periods = 3 1/3 crystal clock periods (with PLL enabled)

Figure 16-5. FlexCAN Bit Timing

The eSCI is configured for one start bit, eight data bits, no parity and one stop bit and to operate at a baud rate equal to the system clock divided by 1250. Refer to Table 16-9 for examples of baud rates.

The BAM ignores the following eSCI errors:

- Overrun errors
- Noise errors
- Framing errors
- Parity errors

All data received is assumed to be good and is echoed out on the TXD signal. It is the responsibility of the host computer to compare the echoes with the sent data and restart the process if an error is detected.

Table 16-8. Serial Boot Mode—Baud Rate and Watchdog Summary

Crystal Frequency (MHz)	System Clock Frequency (MHz)	SCI Baud Rate	FlexCAN Baud Rate	Watchdog Timeout Period (seconds)
$f_{ref\_crystal}$	$f_{sys} = 1.5 \times f_{ref\_crystal}$	$f_{sys} \div 1250$	$f_{sys} \div 60$	$(2.5 \times 2^{27}) \div f_{sys}$
8	12	9600	200 K	28.0

Table 16-8. Serial Boot Mode—Baud Rate and Watchdog Summary (continued)

Crystal Frequency (MHz)	System Clock Frequency (MHz)	SCI Baud Rate	FlexCAN Baud Rate	Watchdog Timeout Period (seconds)
12	18	14400	300 K	18.6
16	24	19200	400 K	14.0
20	30	24000	500 K	11.2

Upon receiving a valid FlexCAN message with an ID equal to 0x0011 that contains eight data bytes, or a valid eSCI message, the BAM uses a serial boot submode: FlexCAN serial boot mode, or eSCI serial boot mode.

In FlexCAN serial boot mode, the eSCI A signal RXDA reverts to GPIO input. All data is downloaded on the FlexCAN bus and eSCI messages are ignored.

In eSCI serial boot mode, the FlexCAN A signals CNRXA and CNTXA revert to GPIO inputs and the TXDA signal is configured as an output. All data is downloaded on the eSCI bus and FlexCAN messages are ignored.

Table 16-9. FlexCAN and eSCI Reset Configuration for FlexCAN and eSCI Boot

Pin Label	Reset Function	Initial Serial Boot Mode	Serial Boot Mode after Receiving a Valid	
			FlexCAN Message	eSCI Message
CNTXA	GPIO	CNTXA	CNTXA	GPIO
CNRXA	GPIO	CNRXA	CNRXA	GPIO
TXDA	GPIO	GPIO	GPIO	TXDA
RXDA	GPIO	RXDA	GPIO	RXDA

Table 16-10. FlexCAN and eSCI Reset Pin Configuration

Pins	I/O	Weak Pullup State	Hysteresis	Driver Configuration	Slew Rate	Input Buffer Enable
CNTXA_TXDA	Output	Enabled Up	—	Push/pull	Medium	N
CNRXA_RXDA	Input	Enabled Up	Y	—	—	—
GPIO	Input	Enabled Up	Y	—	—	—

16.3.2.3.3 Download Process for FlexCAN Serial Boot Mode

The download process contains the following steps:

1. Download the 64-bit password.
2. Download the start address, VLE flag, and the number of data bytes to download.
3. Download the data.
4. Execute the boot code from the start address.

Each step of the process must complete before the next step starts.

1. Download the 64-bit password.

   The host computer must send a FlexCAN message with ID = 0x011 that contains the 64-bit serial download password. FlexCAN messages with other IDs or fewer bytes of data are ignored. When a valid message is received, the BAM transmits a FlexCAN message with ID = 0x001 that contains the data received. The host must not send a second FlexCAN message until it receives the echo of the first message. A FlexCAN message sent before the echo is received is ignored.

   The 64-bit password is validated to ensure that none of the four 16-bit halfwords have a value of 0x0000 or 0xFFFF, which are invalid passwords. A valid password must have at least one 0 and one 1 in each halfword lane.

   The BAM program then reads the disable Nexus bit [DISNEX] in the SIU_CCR register to determine the censorship status of the MCU. If Nexus is disabled, the MCU is censored and the password is compared to a password stored in the shadow row in internal flash memory.

   If Nexus is enabled, the MCU is not censored or booting from external flash and the password is compared to the constant value = 0xFEED_FACE_CAFE_BEEF.

   If the password fails any validity tests, the MCU stops responding to all stimulus. To repeat boot operation, the MCU needs to be reset by external reset or by watchdog. If the password is valid, the BAM program refreshes the e200z6 watchdog timer and the next step in the protocol can be performed.

2. Download the start address, VLE bit, and the download size.

   The host computer must send a FlexCAN message with an ID = 0x012 that contains:

   — 32-bit start address in internal SRAM indicating where to store the succeeding data in memory;

   — 32-bit number containing a 1-bit variable length encoded (VLE) flag followed by a 31-bit length field that contains the number of data bytes to receive and store in memory before switching to execute the code just loaded.

   The start address is expected on a 32-bit word boundary, therefore the least significant 2 bits of the address are ignored. FlexCAN messages with other IDs or fewer data bytes are ignored.

   Set the VLE bit in the serial download data (most significant bit in the LENGTH word) if the code to download uses VLE instructions.

   When a valid message is received, the BAM transmits a FlexCAN message with an ID = 0x002 that contains the received data. The host computer must not send another FlexCAN message until it receives the echo from the previous message. A FlexCAN message sent before the echo is received is ignored.

3. Download the data.

   The host computer must send a succession of FlexCAN messages with ID = 0x013 that contains raw binary data (the data length is variable). Each data byte received is stored in MCU memory, starting at the address specified in the previous step and incrementing through memory until the number of data bytes received and stored in memory matches the number specified in the previous step. FlexCAN messages with ID values other than 0x013 are ignored.

   When a valid message is received, the BAM transmits a FlexCAN message with an ID = 0x003 that contains the data received. The host computer must not send another FlexCAN message until

it receives the echo from the previous message. A FlexCAN message sent before the echo is received is ignored.

NOTE

Internal SRAM is protected by 64-bit error correction (ECC) hardware. All writes to uninitialized internal SRAM must be 64-bits wide, or an ECC error occurs. The BAM buffers 8 bytes of downloaded data before executing a single 64-bit write. Only internal SRAM supports 64-bit writes. Downloading data to other RAM causes errors.

If the start address of the downloaded data is not at an 8-byte boundary, the BAM writes 0x00 to the memory locations from the preceding 8-byte boundary to the start address (maximum 4 bytes). The BAM also writes 0x00 to all memory locations from the last byte of data downloaded to the following 8-byte boundary (maximum 7 bytes).

4. Execute code.

   The BAM waits for the last FlexCAN message transmission to complete. Then the FlexCAN controller is disabled. CNTXA and CNRXA become GPIO inputs. The BAM branches to the starting address of the downloaded code, as specified in step 2.

NOTE

The code that downloads and executes must:

- Periodically refresh the e200z6 watchdog timer; or
- Change the timeout period to a value that does not cause resets during normal operation.

Table 16-11. FlexCAN Serial Boot Mode Download Process

Step	Host Message Sent	MCU Response Message	Action
1	FlexCAN ID = 0x011 + 64-bit password	FlexCAN ID = 0x001 + 64-bit password	Password checked for validity and compared against stored password. e200z6 watchdog timer is refreshed if the password check is successful.
2	FlexCAN ID = 0x012 + 32-bit store address + 32-bit number of bytes	FlexCAN ID = 0x002 + 32-bit store address + 32-bit number of bytes	The load address and the number of bytes to download are stored for future use.
3	FlexCAN ID = 0x013 + 8 to 64 bits of raw binary data	FlexCAN ID = 0x003 + 8 to 64 bits of raw binary data	Each data byte received is written to MCU memory, starting at the address specified in the previous step and incrementing until the number of data bytes received and stored matches the number of bytes to download and store (specified in step 2).
4	None	None	The BAM program returns I/O pins and the FlexCAN module to their reset state, then branches to the start address of the stored data (specified in step 2).

16.3.2.3.4 eSCI Serial Boot Mode Download Process

The eSCI serial boot mode download process contains the following steps:

1. Download the 64-bit password.
2. Download the start address, VLE flag, and the number of data bytes to download.
3. Download the data.
4. Execute the code from start address.

Each step in the following process must complete before the next step starts. The eSCI operates in half duplex mode where the host sends a byte of data, then waits for the echo back from the MCU before proceeding with the next byte. Bytes sent from the host before the previous echo from the MCU is received are ignored.

1. Download the 64-bit password.

   The first 8 bytes of eSCI data the host computer sends must contain the 64-bit serial download password. For each valid eSCI message received, the BAM transmits the same data on the eSCI A TXDA signal.

   The received 64-bit password is checked for validity. It is checked to ensure that none of the 4 x 16-bit halfwords are illegal passwords (0x0000 or 0xFFFF). A password must have at least one 0 and one 1 in each halfword to qualify as legal.

   The BAM program then checks the censorship status of the MCU by checking the DISNEX bit in the SIU_CCR. If Nexus is disabled, the MCU is considered censored and the password is compared with a password stored in the shadow row of internal flash memory.

   If Nexus is enabled, the MCU is not censored or is booting from external flash and the password is compared to the constant value of 0xFEED_FACE_CAFE_BEEF.

   If the password fails a validity test, the MCU stops responding to all stimulus. To repeat the boot operation, assert the $\overline{\text{RESET}}$ signal or wait for the watchdog timer to reset the MCU. If the password is valid, the BAM refreshes the e200z6 watchdog timer and proceeds to step 2.
2. Download the start address, VLE bit, and the download size.

   The host computer must send the next eight bytes of eSCI data that contains:

   — 32-bit start address in internal SRAM indicating where to store the succeeding data in memory;

   — 32-bit number containing a 1-bit variable length encoded (VLE) flag followed by a 31-bit length field that contains the number of data bytes to receive and store in memory before switching to execute the code just loaded.

   The start address is normally located on a word boundary (4-bytes), therefore the least significant 2 bits of the address are ignored. For each valid eSCI message received, the BAM transmits the same data on the eSCI A TXDA signal.

   Set the VLE bit in the serial download data (most significant bit in the LENGTH word) if the code to download uses VLE instructions.
3. Download the data.

   The host computer must then send a succession of eSCI messages, each containing raw binary data. Each byte of data received is stored in the MCU's memory, starting at the address specified in the previous step and incrementing through memory until the number of data bytes received and stored

in memory matches the number specified in the previous step. For each valid eSCI message received, the BAM transmits the same data on the TXDA signal.

NOTE

Internal SRAM is protected by 64-bit wide error correction coding hardware (ECC). All writes to uninitialized internal SRAM must be 64 bits wide, or an ECC error occurs. The BAM buffers download data until 8-bytes are received, and then executes a single 64-bit wide write. Only internal SRAM supports 64-bit writes. Downloading data to RAM other than internal SRAM causes errors.

If the start address of the downloaded data is not on an 8-byte boundary, the BAM writes 0x00 beginning at the preceding 8-byte boundary memory location to the start address (4 byte maximum). The BAM also writes 0x00 to all memory locations from the last data byte downloaded to the following 8-byte boundary (7 byte maximum).

4. Execute the code.

   The BAM waits for the last eSCI message transmission to complete and then disables the eSCI. TXDA and RXDA revert to general-purpose inputs. The BAM branches to the starting address where the downloaded code is stored (specified in step 2) and executes the code.

NOTE

The code that downloads and executes must periodically refresh the e200z6 watchdog timer or change the timeout period to a value that does not cause resets during normal operation.

Table 16-12. eSCI Serial Boot Mode Download Process

Step	Host Sent Message	BAM Response Message	Action
1	64-bit password MSB first	64-bit password	Password checked for validity and compared against stored password. e200z6 watchdog timer is refreshed if the password check is successful
2	32-bit store address + 32-bit number of bytes MSB first	32-bit store address + 32-bit number of bytes	Load address and size of download are stored for future use
3	8 bits of raw binary data	8 bits of raw binary data	Each byte of data received is stored in MCU memory, starting at the address specified in the previous step and incrementing until the number of data bytes received and stored matches the number of data bytes specified in the preceding step.
4	None	None	The BAM returns I/O pins and the eSCI module to their reset state, except it asserts ESCI_A_CR2[MDIS] instead of negates. Then the BAM branches to the starting address of the stored data specified in step 2.

16.3.3 Interrupts

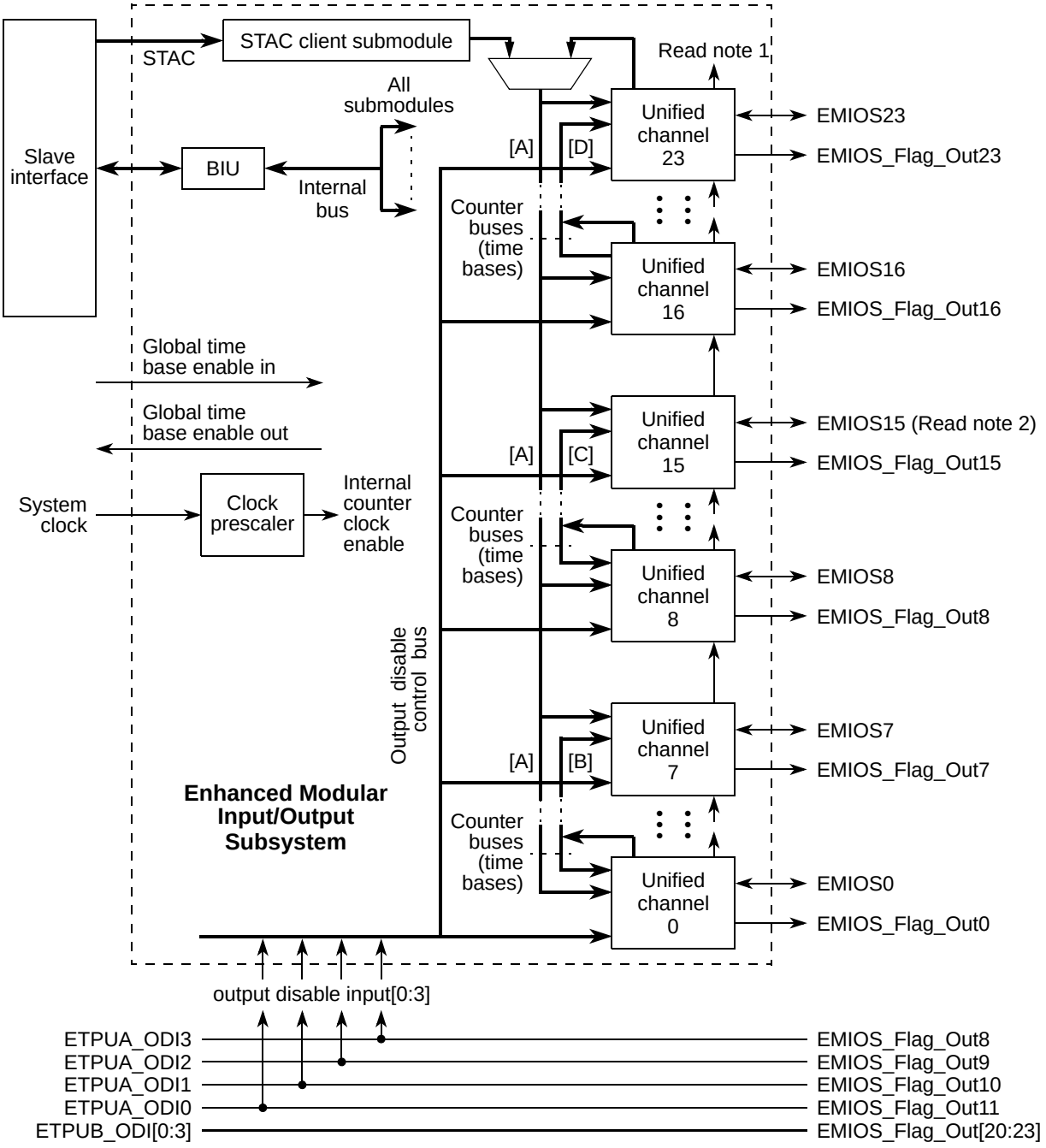
No interrupts are generated or enabled by the BAM.

Chapter 17
Enhanced Modular Input/Output Subsystem (eMIOS)

17.1 Introduction

This chapter describes the enhanced modular input/output subsystem (eMIOS) which can generate or measure timed events.

Figure 17-1 shows the block diagram of the eMIOS.



Note 1: Connection between UC[n-1] and UC*n* necessary to implement QDEC mode.

Note 2: On channels 12–15, there is no input from EMIOS[12:15], only from the DSPI module.

Figure 17-1. eMIOS Block Diagram

17.1.1 Overview

The eMIOS builds on the MIOS concept by using a unified channel module that provides a superset of the functionality of all the individual MIOS channels, while providing a consistent user interface. This allows more flexibility as each unified channel can be programmed for different functions.

17.1.2 Features

- 24 unified channels
- Unified channels features
  - 24-bit registers for captured/match values
  - 24-bit internal counter
  - Internal prescaler
  - Dedicated output pin for buffer direction control
  - Selectable time base
  - Can generate its own time base
- Four 24-bit wide counter buses
  - Counter bus A can be driven by unified channel 23 or by the STAC bus.
  - Counter bus B, C, and D are driven by unified channels 0, 8, and 16, respectively.
  - Counter bus A can be shared among all unified channels. UCs 0 to 7 can share counter bus A and B, UCs 8 to 15 can share counter bus A and C, and UCs 16 to 23 can share counter buses A and D.
- One global prescaler
- Shared time bases through the counter buses
- Synchronization among internal and external time bases
- Shadow FLAG register
- State of module can be frozen for debug purposes
- DMA request capability for some channels
- Motor control capability

17.1.3 eMIOS Operating Modes

The eMIOS has the following operating modes:

Table 17-1. eMIOS Operating Modes

Mode	Description
User	User mode is the normal operating mode. When EMIOS_MCR[FRZ] = 0, and EMIOS_CCR[FREN] = 0, the eMIOS is in user mode.
Debug	Debug mode is individually programmed for each channel. When entering this mode, the UC registers' contents are frozen, but remain available for read and write access through the slave interface. After leaving debug mode, all counters that were frozen upon debug mode entry resume at the point where they were frozen. In debug mode, all clocks are running and all registers are accessible; thus, this mode is not intended for power saving, but for use during software debugging.
Freeze	Freeze mode enables the eMIOS to freeze the registers of the unified channels when debug mode is requested at the MCU level. While in freeze mode, the eMIOS continues to operate to allow the MCU access to the unified channels' registers. The unified channel remains frozen until the EMIOS_MCR[FRZ] bit is cleared to zero, the MCU exits debug mode, or a unified channel's EMIOS_CCR[FREN] bit is cleared.

17.1.3.1 Unified Channel Modes

The unified channels can be configured to operate in the following modes:

- General purpose input/output
- Single action input capture
- Single action output compare
- Input pulse-width measurement
- Input period measurement
- Double action output compare
- Pulse/edge accumulation
- Pulse/edge counting
- Quadrature decode
- Windowed programmable time accumulation
- Modulus counter, normal
- Modulus counter, buffered
- Output pulse-width and frequency modulation, normal
- Output pulse-width and frequency modulation, buffered
- Center-aligned output pulse-width modulation with dead time insertion, normal
- Center-aligned output pulse-width modulation with dead time insertion, buffered
- Output pulse-width modulation, normal
- Output pulse-width modulation, buffered

These modes are described in Section 17.4.4.4, "Unified Channel Operating Modes."

17.2 External Signal Description

Each unified channel has one input and one output signal connected to the channel's I/O pin. Refer to the SIU and DSPI sections for details about the connection to pads and other modules.

The internal *output disable input* signals 0-3 (refer to Table 17-3) are provided to implement the output disable feature needed for motor control. They are connected to EMIOS_Flag_Out signals according to Section 17.2.1.1, "Output Disable Input—eMIOS Output Disable Input Signals."

17.2.1 External Signals

When configured as an input, EMIOS*n* is synchronized and filtered by the programmable input filter (PIF). The output of the PIF is then used by the channel logic and is available to be read by the MCU through the UCIN bit of the EMIOS_CSR*n*.

When configured as an output, EMIOS*n* is a registered output and is available for reading by the MCU through the UCOUT bit of the EMIOS_CSR*n*.

Table 17-2. External Signals

Signal	Direction	Function	Reset State
EMIOS[0:11, 16:23]	Input	eMIOS Unified Channel *n* input	—
EMIOS[0:23]	Output	eMIOS Unified Channel *n* output	0 / Hi-Z[1]

[1] A value of 0 refers to the reset value of the signal. Hi-Z refers to the state of the external pin if a tri-state output buffer is controlled by the corresponding eMIOS signal.

17.2.1.1 Output Disable Input—eMIOS Output Disable Input Signals

Output disable inputs to both the eMIOS and the eTPU modules are connected to EMIOS_Flag_Out*n* signals according to Table 17-3.

Table 17-3. eMIOS Output Disable Input Signals

eMIOS Channel[1]	eMIOS Output Disable Input Signal[2]	eTPU Output Disable Input Signal[3]
EMIOS_Flag_Out8	Output disable input 3	ETPUA_ODI3
EMIOS_Flag_Out9	Output disable input 2	ETPUA_ODI2
EMIOS_Flag_Out10	Output disable input 1	ETPUA_ODI1
EMIOS_Flag_Out11	Output disable input 0	ETPUA_ODI0
EMIOS_Flag_Out20	—	ETPUB_ODI0
EMIOS_Flag_Out21	—	ETPUB_ODI1
EMIOS_Flag_Out22	—	ETPUB_ODI2
EMIOS_Flag_Out23	—	ETPUB_ODI3

1 All other EMIOS_Flag_Out*n* output signals are not connected.

2 Each of the four internal eMIOS *output disable input* signals can be programmed to disable the output of any eMIOS channel if that channel has selected output disable capability by the setting of its EMIOS_CCR*n*[ODIS] bit, and by specifying the output disable input in its EMIOS_CCRn[ODISSL] field.

3 ETPU*x*_ODI*y* input signals disable outputs for eTPU engine *x*, channels (*y**8) through (*y**8+7). Refer to the ETPU chapter for more details.

17.3 Memory Map/Register Definition

Addresses of unified channel (UC) registers are specified as offsets from the channel's base address, otherwise the eMIOS base address is used as reference.

The overall address map organization is shown in Table 17-4.

Table 17-4. eMIOS Memory Map

Address	Register Name	Register Description	Bits
Base (0xC3FA_0000)	EMIOS_MCR	Module configuration register	32
Base + 0x0004	EMIOS_GFR	Global flag register	32
Base + 0x0008	EMIOS_OUDR	Output update disable register	32
Base + 0x000C–0x001F	—	Reserved	—
Base + 0x0020	UC0	Unified channel 0 registers	256
Base + 0x0040	UC1	Unified channel 1 registers	256
Base + 0x0060	UC2	Unified channel 2 registers	256

Table 17-4. eMIOS Memory Map (continued)

Address	Register Name	Register Description	Bits
Base + 0x0080	UC3	Unified channel 3 registers	256
Base + 0x00A0	UC4	Unified channel 4 registers	256
Base + 0x00C0	UC5	Unified channel 5 registers	256
Base + 0x00E0	UC6	Unified channel 6 registers	256
Base + 0x0100	UC7	Unified channel 7 registers	256
Base + 0x0120	UC8	Unified channel 8 registers	256
Base + 0x0140	UC9	Unified channel 9 registers	256
Base + 0x0160	UC10	Unified channel 10 registers	256
Base + 0x0180	UC11	Unified channel 11 registers	256
Base + 0x01A0	UC12	Unified channel 12 registers	256
Base + 0x01C0	UC13	Unified channel 13 registers	256
Base + 0x01E0	UC14	Unified channel 14 registers	256
Base + 0x0200	UC15	Unified channel 15 registers	256
Base + 0x0220	UC16	Unified channel 16 registers	256
Base + 0x0240	UC17	Unified channel 17 registers	256
Base + 0x0260	UC18	Unified channel 18 registers	256
Base + 0x0280	UC19	Unified channel 19 registers	256
Base + 0x02A0	UC20	Unified channel 20 registers	256
Base + 0x02C0	UC21	Unified channel 21 registers	256
Base + 0x02E0	UC22	Unified channel 22 registers	256
Base + 0x0300	UC23	Unified channel 23 registers	256

Table 17-5 lists the memory map address for the unified channel registers. All registers are cleared on reset.

Table 17-5. Unified Channel Memory Map

Address	Register Name	Register Description	Bits
UC*n* Base + 0x0000	EMIOS_CADR*n*	Channel A data register	32
UC*n* Base + 0x0004	EMIOS_CBDR*n*	Channel B data register	32
UC*n* Base + 0x0008	EMIOS_CCNTR*n*	Channel counter register	32
UC*n* Base + 0x000C	EMIOS_CCR*n*	Channel control register	32
UC*n* Base + 0x0010	EMIOS_CSR*n*	Channel status register	32
UC*n* Base + 0x0014	EMIOS_ALTA*n*	Channel alternate address register	32
UC*n* Base + (0x0018–0x001F)	—	Reserved	—

17.3.1 Register Description

All registers are 32-bit wide. This section describes the eMIOS with 24 unified channels supporting 24-bit wide data.

17.3.1.1 eMIOS Module Configuration Register (EMIOS_MCR)

EMIOS_MCR contains global control bits for the eMIOS module.

Address: Base + 0x0000 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	MDIS	FRZ	GTBE	ETB	GPREN	0	0	0	0	0	0	SRV			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	GPRE								0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 17-2. eMIOS Module Configuration Register (EMIOS_MCR)

The following table describes the fields in the eMIOS module configuration register:

Table 17-6. EMIOS_MCR Field Descriptions

Field	Description
0	Reserved. This bit is readable and writable, but has no effect.
1 MDIS	Module disable. Puts the eMIOS in low power mode. The MDIS bit is used to stop the clock of the module, except the access to registers EMIOS_MCR and EMIOS_OUDR. 0 Clock is running 1 Enter low power mode
2 FRZ	Freeze. Enables the eMIOS to freeze the registers in the unified channels when debug mode is requested at the MCU level. Set the FREN bit in each unified channel to enter freeze mode. While in freeze mode, the eMIOS continues to operate to allow the MCU access to the unified channels registers. The unified channel remains frozen until: • FRZ bit is cleared to zero; or, • MCU exits debug mode; or, • Unified channel FREN bit is cleared 0 Allows unified channels to continue to operate when device enters debug mode and the EMIOS_CCR*n*[FREN] bit is set 1 Stops unified channels operation when in debug mode and the EMIOS_CCR*n*[FREN] bit is set
3 GTBE[1]	Global time base enable. Used to export a global time base enable from the module and provide a method to start time bases of several modules simultaneously. 0 Global time base enable out signal negated 1 Global time base enable out signal asserted **Note:** The global time base enable input signal controls the internal counters. When asserted, internal counters are enabled. When negated, internal counters disabled.

Table 17-6. EMIOS_MCR Field Descriptions (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>4
ETB</td><td>External time base. Selects the time base source that drives counter bus [A].
0 Unified channel 23 drives counter bus [A]
1 STAC drives counter bus [A]
Note: If ETB is set to select STAC as the counter bus[A] source, the GTBE must be set to enable the STAC to counter bus[A]. See Section 17.4.2, “STAC Client Submodule” and the shared time and angle clock (STAC) bus interface section and the STAC bus configuration register (ETPU_REDCR) section of the eTPU chapter for more information about the STAC.</td></tr>
<tr><td>5
GPREN</td><td>Global prescaler enable. Enables the prescaler counter.
0 Prescaler disabled (no clock) and prescaler counter is cleared
1 Prescaler enabled</td></tr>
<tr><td>6–11</td><td>Reserved.</td></tr>
<tr><td>12–15
SRV[0:3]</td><td>Server time slot. Selects the address of a specific STAC server to which the STAC client submodule is assigned (refer to Section 17.4.2, “STAC Client Submodule,” for details)
0000 eTPU engine A, TCR1
0001 eTPU engine B, TCR1
0010 eTPU engine A, TCR2
0011 eTPU engine B, TCR2
0100–1111 reserved</td></tr>
<tr><td>16–23
GPRE[0:7]</td><td>Global prescaler. Selects the clock divider value for the global prescaler, as shown here:
<table>
<tr><th>GPRE[0:7]</th><th>Divide Ratio</th></tr>
<tr><td>00000000</td><td>1</td></tr>
<tr><td>00000001</td><td>2</td></tr>
<tr><td>.
.
.
.</td><td>.
.
.
.</td></tr>
<tr><td>11111111</td><td>256</td></tr>
</table></td></tr>
<tr><td>24–31</td><td>Reserved.</td></tr>
</table>

[1] The GTBE signal is an inter-module signal, not an external pin on the device.

17.3.1.2 eMIOS Global Flag Register (EMIOS_GFR)

The EMIOS_GFR is a read-only register that groups the FLAG bits from all channels. This organization improves interrupt handling on simpler devices. These bits are mirrors of the FLAG bits of each channel register (EMIOS_CSR) and flag bits in those channel registers cannot be cleared by accessing this ‘mirror’ register.

Address: Base + 0x0004 Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	F23	F22	F21	F20	F19	F18	F17	F16
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 17-3. eMIOS Global Flag Register (EMIOS_GFR)

17.3.1.3 eMIOS Output Update Disable Register (EMIOS_OUDR)

The EMIOS_OUDR serves to disable transfers from the A2 to the A1 channel registers and from the B2 to the B1 channel registers when values are written to these registers, and the channel is running in modulus counter (MC) mode or an output mode.

Address: Base + 0x0008 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	OU23	OU22	OU21	OU20	OU19	OU18	OU17	OU16
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	OU15	OU14	OU13	OU12	OU11	OU10	OU9	OU8	OU7	OU6	OU5	OU4	OU3	OU2	OU1	OU0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 17-4. eMIOS Output Update Disable Register (EMIOS_OUDR)

The following table describes the fields in the eMIOS output update disable register:

Table 17-7. EMIOS_OUDR Field Descriptions

Field	Description
0–7	Reserved.
8–31 OU*n*	Channel *n* output update disable. When running in MC mode or an output mode, values are written to registers A2 and B2. OU*n* bits are used to disable transfers from registers A2 to A1 and B2 to B1. Each bit controls one channel. 0 Transfer enabled. Depending on the operating mode, transfer occurs immediately or in the next period. Unless stated otherwise, transfer occurs immediately. 1 Transfers disabled

17.3.1.4 eMIOS Channel A Data Register (EMIOS_CADR*n*)

Depending on the mode of operation, internal registers A1 or A2, used for matches and captures, can be assigned to address EMIOS_CADR*n*. Both A1 and A2 are cleared by reset. Table 17-8 summarizes the EMIOS_CADR*n* writing and reading accesses for all operating modes.

Refer to Section 17.4.4.4, “Unified Channel Operating Modes” for more information.

Address: UC*n* Base + 0x0000 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	A							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	A															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 17-5. eMIOS Channel A Data Register (EMIOS_CADR*n*)

17.3.1.5 eMIOS Channel B Data Register (EMIOS_CBDR*n*)

Depending on the mode of operation, internal registers B1 or B2 can be assigned to address EMIOS_CBDR*n*. Both B1 and B2 are cleared by reset. Table 17-8 summarizes the EMIOS_CBDR*n* writing and reading accesses for all operating modes.

Refer to Section 17.4.4.4, “Unified Channel Operating Modes” for more information.

NOTE

The EMIOS_CBDR*n* must not be read speculatively. For future compatibility, the TLB entry covering the EMIOS_CBDR*n* must be configured to be guarded.

Address: UC*n* Base + 0x0004 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	B							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	B															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 17-6. eMIOS Channel B Data Register (EMIOS_CBDR*n*)

The following table describes the fields in the eMIOS channel B data register:

Table 17-8. EMIOS_CADR*n*, EMIOS_CBDR*n*, and EMIOS_ALTA*n* Value Assignments

Operating Mode	Register Access				
	Write	Read	Write	Read	Alternate Read
GPIO	A1, A2	A1	B1,B2	B1	—
SAIC[1]	—	A2	B2	B2	—
SAOC[1]	A2	A1	B2	B2	—
IPWM	—	A2	—	B1	—
IPM	—	A2	—	B1	—
DAOC	A2	A1	B2	B1	—
PEA	A1	A2	—	B1	—
PEC[1]	A1	A1	B1	B1	A2
QDEC[1]	A1	A1	B2	B2	—
WPTA	A1	A1	B1	B1	A2
MC – normal[1]	A2	A1	B2	B2	—
MC – buffered	A2	A1	B2	B2	—
OPWFM – normal	A2	A1	B2	B1	—
OPWFM – buffered	A2	A1	B2	B1	—
OPWMC – normal	A2	A1	B2	B1	—
OPWMC – buffered	A2	A1	B2	B1	—
OPWM – normal	A2	A1	B2	B1	—
OPWM – buffered	A2	A1	B2	B1	—

[1] In these modes, the register EMIOS_CBDR*n* is not used, but B2 can be accessed.

17.3.1.6 eMIOS Channel Counter Register (EMIOS_CCNTR*n*)

The EMIOS_CCNTR*n* contains the value of the internal counter. When GPIO mode is selected or the channel is frozen, the EMIOS_CCNTR*n* is readable and writable. For all others modes, the EMIOS_CCNTR*n* is a read-only register. When entering some operating modes, this register is automatically cleared.

Refer to Section 17.4.4.4, "Unified Channel Operating Modes," for details.

Address: UC*n* Base + 0x0008 Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	C							
W[1]																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	C															
W[1]																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[1] In GPIO mode or freeze action, this register is writable.

Figure 17-7. eMIOS Channel Counter Register (EMIOS_CCNTR*n*)

17.3.1.7 eMIOS Channel Control Register (EMIOS_CCR*n*)

The eMIOS_CCR*n* enables the setting of several control parameters for a unified channel. Among these controls are the setting of a channel prescaler, channel mode selection, input trigger sensitivity and filtering, interrupt and DMA request enabling, and output mode control.

Address: UC*n* Base + 0x000C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	FREN	ODIS	ODISSL		UCPRE		UCP REN	DMA	0	IF				FCK	FEN	0
W[1]																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	BSL		EDSEL	EDPOL	MODE						
W[1]			FORCMA	FORCMB												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 17-8. eMIOS Channel Control Register (EMIOS_CCR*n*)

The following table describes the fields in the eMIOS channel control register:

Table 17-9. EMIOS_CCR*n* Field Description

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>0
FREN</td><td>Freeze enable. If set and validated by FRZ bit in EMIOS_MCR, freezes all registers values when in debug mode, allowing the MCU to perform debug functions.
0 Normal operation
1 Freeze UC registers values</td></tr>
<tr><td>1
ODIS</td><td>Output disable. Allows output disable in any output mode except GPIO.
0 The output pin operates normally
1 If the selected output disable input signal is asserted, the output pin goes to the complement of EDPOL for OPWFM, OPWFMB, and OPWMB modes, but the unified channel continues to operate normally; that is, it continues to produce FLAG and matches. When the selected output disable input signal is negated, the output pin operates normally.</td></tr>
<tr><td>2–3
ODISSL[0:1]</td><td>Output disable select. Selects one of the four output disable input signals.
00 output disable input 0
01 output disable input 1
10 output disable input 2
11 output disable input 3</td></tr>
<tr><td>4–5
UCPRE[0:1]</td><td>Prescaler. Selects the clock divider value for the unified channel internal prescaler, as shown in the following table:
<table>
<tr><th>UCPRE[0:1]</th><th>Divide Ratio</th></tr>
<tr><td>00</td><td>1</td></tr>
<tr><td>01</td><td>2</td></tr>
<tr><td>10</td><td>3</td></tr>
<tr><td>11</td><td>4</td></tr>
</table></td></tr>
<tr><td>6
UCPREN</td><td>Prescaler enable. Enables the prescaler counter.
0 Prescaler disabled (no clock) and prescaler counter is loaded with UCPRE value
1 Prescaler enabled</td></tr>
</table>

Table 17-9. EMIOS_CCR*n* Field Description (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>7
DMA</td><td>Direct memory access. Set the DMA bit according to whether generating a FLAG or an interrupt is used as a DMA request.
0 FLAG assigned to Interrupt request
1 FLAG assigned to DMA request
eMIOS channels that don’t support DMA are indicated in the following table. Do not change the DMA bit default value of 0 for any channel that does not support DMA.
<table>
<tr><th>eMIOS Channel</th><th>DMA = 0</th><th>DMA = 1</th></tr>
<tr><td>0</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>1</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>2</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>3</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>4</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>5</td><td>Interrupt</td><td>Reserved</td></tr>
<tr><td>6</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>7</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>8</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>9</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>10</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>11</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>12</td><td>Interrupt</td><td>Reserved</td></tr>
<tr><td>13</td><td>Interrupt</td><td>Reserved</td></tr>
<tr><td>14</td><td>Interrupt</td><td>Reserved</td></tr>
<tr><td>15</td><td>Interrupt</td><td>Reserved</td></tr>
<tr><td>16</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>17</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>18</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>19</td><td>Interrupt</td><td>DMA request</td></tr>
<tr><td>20</td><td>Interrupt</td><td>Reserved</td></tr>
<tr><td>21</td><td>Interrupt</td><td>Reserved</td></tr>
<tr><td>22</td><td>Interrupt</td><td>Reserved</td></tr>
<tr><td>23</td><td>Interrupt</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>8</td><td>Reserved.</td></tr>
</table>

Table 17-9. EMIOS_CCR*n* Field Description (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>9–12
IF[0:3]</td><td>Input filter. Controls the programmable input filter, selecting the minimum input pulse-width that can pass through the filter, as shown below. For output modes, these bits have no meaning.
<table>
<tr><th>IF[0:3][1]</th><th>Minimum Input Pulse Width [filter clock periods]</th></tr>
<tr><td>0000</td><td>Bypassed[2]</td></tr>
<tr><td>0001</td><td>2 filter clock periods</td></tr>
<tr><td>0010</td><td>4 filter clock periods</td></tr>
<tr><td>0100</td><td>8 filter clock periods</td></tr>
<tr><td>1000</td><td>16 filter clock periods</td></tr>
<tr><td>all others</td><td>Invalid values</td></tr>
</table>
1 Filter latency is three clock cycles.
2 The input signal is synchronized before arriving at the digital filter.</td></tr>
<tr><td>13
FCK</td><td>Filter clock select. Selects the clock source for the programmable input filter.
0 Prescaled clock
1 Main clock</td></tr>
<tr><td>14
FEN</td><td>FLAG enable. Allows the unified channel FLAG bit to generate an interrupt signal or a DMA request signal (The type of signal to be generated is defined by the DMA bit).
0 Disable (FLAG does not generate an interrupt or DMA request)
1 Enable (FLAG generates an interrupt or DMA request)</td></tr>
<tr><td>15–17</td><td>Reserved.</td></tr>
<tr><td>18
FORCMA</td><td>Force match A. For output modes, the FORCMA bit is equivalent to a successful comparison on comparator A (except that the FLAG bit is not set). This bit is cleared by reset and is always read as zero. This bit is valid for every output operating mode which uses comparator A, otherwise it has no effect.
0 Has no effect
1 Force a match at comparator A
For input modes, the FORCMA bit is not used and writing to it has no effect.</td></tr>
<tr><td>19
FORCMB</td><td>Force match B. For output modes, the FORCMB bit is equivalent to a successful comparison on comparator B (except that the FLAG bit is not set). This bit is cleared by reset and is always read as zero. This bit is valid for every output operating mode which uses comparator B, otherwise it has no effect.
0 Has no effect
1 Force a match at comparator B
For input modes, the FORCMB bit is not used and writing to it has no effect.</td></tr>
<tr><td>20</td><td>Reserved.</td></tr>
</table>

Table 17-9. EMIOS_CCR*n* Field Description (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>21–22
BSL[0:1]</td><td>Bus select. Used to select either one of the counter buses or the internal counter to be used by the unified channel.

<table><tr><th>BSL[0:1]</th><th>Selected Bus</th></tr><tr><td>00</td><td>All channels: counter bus [A]</td></tr><tr><td>01</td><td>Channels 0–7: counter bus [B]
Channels 8–5: counter bus [C]
Channels 16–23: counter bus [D]</td></tr><tr><td>10</td><td>Invalid value</td></tr><tr><td>11</td><td>All channels: internal counter (read following note)</td></tr></table>
Note: In certain modes the internal counter is used internally and therefore cannot be used as the channel time base.</td></tr>
<tr><td>23
EDSEL</td><td>Edge selection bit. For input modes, the EDSEL bit selects whether the internal counter is triggered by both edges of a pulse or just by a single edge as defined by the EDPOL bit. When not shown in the mode of operation description, this bit has no effect.
0 Single-edge triggering defined by the EDPOL bit
1 Both edges triggering

For GPIO input mode, the EDSEL bit selects if a FLAG can be generated.
0 A FLAG is generated as defined by the EDPOL bit
1 No FLAG is generated

For SAOC mode, the EDSEL bit selects the behavior of the output flip-flop at each match.
0 The EDPOL value is transferred to the output flip-flop
1 The output flip-flop is toggled</td></tr>
</table>

Table 17-9. EMIOS_CCR*n* Field Description (continued)

Field	Description
24 EDPOL	Edge polarity. For input modes (except QDEC and WPTA mode), the EDPOL bit asserts which edge triggers either the internal counter or an input capture or a FLAG. When not shown in the mode of operation description, this bit has no affect. 0 Trigger on a falling edge 1 Trigger on a rising edge For WPTA mode, the internal counter is used as a time accumulator and counts up when the input gating signal has the same polarity of EDPOL bit. 0 Counting occurs when the input gating signal is low 1 Counting occurs when the input gating signal is high For QDEC (MODE[6] cleared), the EDPOL bit selects the count direction according to *direction* signal (UC*n* input). 0 Counts down when UC*n* is asserted 1 Counts up when UC*n* is asserted NOTE: UC[n-1] EDPOL bit selects which edge clocks the internal counter of UC*n* 0 Trigger on a falling edge 1 Trigger on a rising edge For QDEC (MODE[6] set), the EDPOL bit selects the count direction according to the phase difference. 0 Internal counter decrements if phase_A is ahead phase_B signal 1 Internal counter increments if phase_A is ahead phase_B signal NOTE: To operate properly, EDPOL bit must contain the same value in UC*n* and UC[n-1] For output modes, the EDPOL bit is used to select the logic level on the output pin. When software selects any output mode except GPIO, the initial state of the output flip-flop is the complement of EDPOL. 0 A match on comparator A clears the output flip-flop, while a match on comparator B sets it 1 A match on comparator A sets the output flip-flop, while a match on comparator B clears it
25–31 MODE	Mode selection. Selects the mode of operation of the unified channel, as shown in Table 17-10.

The following table lists the binary values for the unified channel operating modes used in the eMIOS channel control register:

Table 17-10. Binary Values for Unified Channel Operating Modes

MODE[0:6]	Unified Channel Operating Modes
0000000	General purpose input/output mode (input)
0000001	General purpose input/output mode (output)
0000010	Single action input capture
0000011	Single action output compare
0000100	Input pulse-width measurement
0000101	Input period measurement
0000110	Double-action output compare (with FLAG set on the second match)
0000111	Double-action output compare (with FLAG set on both match)
0001000	Pulse and edge accumulation (continuous)

Table 17-10. Binary Values for Unified Channel Operating Modes (continued)

MODE[0:6]	Unified Channel Operating Modes
0001001	Pulse and edge accumulation (single shot)
0001010	Pulse and edge counting (continuous)
0001011	Pulse and edge counting (single shot)
0001100	Quadrature decode (for count and direction encoders type)
0001101	Quadrature decode (for phase_A and phase_B encoders type)
0001110	Windowed programmable time accumulation
0001111	Reserved
0010000	Modulus counter. Up counter, internal clock source.
0010001	Modulus counter. Up counter, external clock source.
0010010–0010011	Reserved
0010100	Modulus counter. Up/down counter, no change in counter direction upon match of input counter and register B1, internal clock source.
0010101	Modulus counter. Up/down counter, no change in counter direction upon match of input counter and register B1, external clock source.
0010110	Modulus counter. Up/down counter, change in counter direction upon match of input counter and register B1 and sets the FLAG, internal clock source.
0010111	Modulus counter. Up/down counter, change in counter direction upon match of input counter and register B1 and sets the FLAG, external clock source.
0011000	Output pulse-width and frequency modulation. FLAG set at match of internal counter and comparator B, immediate update.
0011001	Output pulse-width and frequency modulation. FLAG set at match of internal counter and comparator B, next period update.
0011010	Output pulse-width and frequency modulation. FLAG set at match of internal counter and comparator A or comparator B, immediate update.
0011011	Output pulse-width and frequency modulation. FLAG set at match of internal counter and comparator A or comparator B, next period update.
0011100	Center-aligned output pulse-width modulation. FLAG set in trailing edge, trailing edge dead-time.
0011101	Center-aligned output pulse-width modulation. FLAG set in trailing edge, leading edge dead-time.
0011110	Center-aligned output pulse-width modulation. FLAG set in both edges, trailing edge dead-time.
0011111	Center-aligned output pulse-width modulation. FLAG set in both edges, leading edge dead-time.
0100000	Output pulse-width modulation. FLAG set at match of internal counter and comparator B, immediate update.
0100001	Output pulse-width modulation. FLAG set at match of internal counter and comparator B, next period update.
0100010	Output pulse-width modulation. FLAG set at match of internal counter and comparator A or comparator B, immediate update.

Table 17-10. Binary Values for Unified Channel Operating Modes (continued)

MODE[0:6]	Unified Channel Operating Modes
0100011	Output pulse-width modulation. FLAG set at match of internal counter and comparator A or comparator B, next period update.
0100100–1001111	Reserved
1010000	Modulus up counter, buffered, internal clock
1010001	Modulus up counter, buffered, external clock
1010010–1010011	Reserved
1010100	Modulus up/down counter, buffered. FLAG set on one event, internal clock.
1010101	Modulus up/down counter, buffered. FLAG set on one event, external clock.
1010110	Modulus up/down counter, buffered. FLAG set on both events, internal clock.
1010111	Modulus up/down counter, buffered. FLAG set on both events, external clock.
1011000	Output pulse-width and frequency modulation, buffered. FLAG set at match of internal counter and comparator B.
1011001	Reserved
1011010	Output pulse-width and frequency modulation, buffered. FLAG set at match of internal counter and comparator A or comparator B.
1011011	Reserved
1011100	Center-aligned output pulse-width modulation, buffered. FLAG set on trailing edge, trailing edge dead-time.
1011101	Center-aligned output pulse-width modulation, buffered. FLAG set on trailing edge, leading edge dead-time.
1011110	Center-aligned output pulse-width modulation, buffered. FLAG set on both edges, trailing edge dead-time.
1011111	Center-aligned output pulse-width modulation, buffered. FLAG set on both edges, leading edge dead-time.
1100000	Output pulse-width modulation, buffered. FLAG set on second match.
1100001	Reserved
1100010	Output pulse-width modulation, buffered. FLAG set on both matches.

17.3.1.8 eMIOS Channel Status Register (EMIOS_CSR*n*)

EMIOS_CSR*n* reflects the status of the UC input/output signals and the overflow condition of the internal counter, as well as the occurrence of a trigger event.

Address: UC*n* Base + 0x0010 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	OVR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	w1c															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	OVFL	0	0	0	0	0	0	0	0	0	0	0	0	UCIN	UCOUT	FLAG
W	w1c															w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 17-9. eMIOS Channel Status Register (EMIOS_CSR*n*)

The following table describes the fields in the eMIOS channel status register:

Table 17-11. EMIOS_CSR*n* Field Descriptions

Field	Description
0 OVR	Overrun. Indicates a FLAG was generated when the FLAG bit was set to 1. To clear the OVR bit: write 1 to clear the bit to 0, or clear the FLAG bit to 0, which also clears the OVR bit. 0 Overrun has not occurred 1 Overrun has occurred
1–15	Reserved.
16 OVFL	Overflow. Indicates that an overflow occurred in the internal counter. OVFL is cleared by writing a 1 to it. 0 No overflow 1 An overflow had occurred
17–28	Reserved.
29 UCIN	Unified channel input pin. Reflects the input pin state after being filtered and synchronized.
30 UCOUT	Unified channel output pin. The UCOUT bit reflects the output pin state.
31 FLAG	FLAG. Set when an input capture or a match event in the comparators occurs. Write a 1 to clear this bit to 0. 0 FLAG cleared 1 FLAG set event has occurred **Note:** When EMIOS_CCR[DMA] bit is set, the FLAG bit is cleared by the eDMA controller.

17.3.1.9 eMIOS Alternate Address Register (EMIOS_ALTA*n*)

The EMIOS_ALTA*n* register provides an alternate read-only address to access channel registers in PEC and WPTA modes. If EMIOS_ALTA*n* is used it is possible to access the A2 register in the PEC and WPTA modes. The EMIOS_ALTA*n* address register does not implement coherency mechanisms such as the blocking of B register updates after the A register is read.

Table 17-8, "EMIOS_CADR*n*, EMIOS_CBDR*n*, and EMIOS_ALTA*n* Value Assignments," shows the internal registers accessed by address EMIOS_ALTA*n* in each one of the channel operation modes.

Address: UC*n* Base + 0x0014 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	ALTA[8:15]							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	ALTA[16:31]															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 17-10. eMIOS Alternate Address Register (EMIOS_ALTA*n*)

The following table describes the field in the eMOIS alternate address register:

Table 17-12. EMIOS_ALTA*n* Field Descriptions

Field	Description
0–7	Reserved.
8–31 ALTA	Alternate address. Set when an alternate address is provided for accessing both the A1 and A2 channel registers. 0 Access only A1 register 1 Access both A1 and A2 registers

17.4 Functional Description

The eMIOS provides independent channels (UC) that can be configured and accessed by the MCU. Four time bases can be shared by the channels through four counter buses and each unified channel can generate its own time base. Optionally, the counter A bus can be driven by an external time base from the eTPU imported through the STAC interface.

NOTE

Counter bus A can be driven by unified channel 23 or by the STAC bus. Counter bus B, C, and D are driven by unified channels 0, 8, and 16, respectively. Counter bus A can be shared among all unified channels. UCs 0 to 7 can share counter bus A and B, UCs 8 to 15 can share counter bus A and C, and UCs 16 to 23 can share counter buses A and D.

The four components of the eMIOS module are:

- Bus interface unit
- STAC client submodule
- Global clock prescaler
- Unified channels and their modes of operation

17.4.1 Bus Interface Unit (BIU)

The bus interface unit provides the interface between the internal bus and the slave interface, allowing communication among all submodules and the slave interface. The BIU allows 8-, 16-, and 32-bit accesses. They are performed over a 32-bit data bus in a single cycle clock.

17.4.1.1 Effect of Freeze on the BIU

When the FRZ bit in the EMIOS_MCR is set and the module is in debug mode, the operation of the BIU is not affected.

17.4.2 STAC Client Submodule

The shared time and angle count (STAC) bus provides access to one external time base, imported from the STAC bus to the eMIOS unified channels. The eTPU module's time bases and angle count can be exported and/or imported through the STAC client submodule interface. Time bases and/or angle information of either eTPU engine can be exported to the other eTPU engine and to the eMIOS module, which is only a STAC client. There are restrictions on engine export/import targets: one engine cannot export from or import to itself, nor can it import time base and/or angle count if in angle mode.

The device’s STAC server identification assignment is shown in Table 17-13. The time slot assignment is fixed, so only time bases running at system clock divided by four or slower can be integrally exported. The STAC client submodule runs with the system clock, and its time slot timing is synchronized with the eTPU timing on reset. The time slot sequence is 0-1-2-3, such that they alternate between engines one and two.

Table 17-13. STAC Client Submodule Server Slot Assignment

Engine	Time Base	Server ID
1	TCR1	0
1	TCR2	2
2	TCR1	1
2	TCR2	3

Figure 17-11 provides a block diagram for the STAC client submodule.

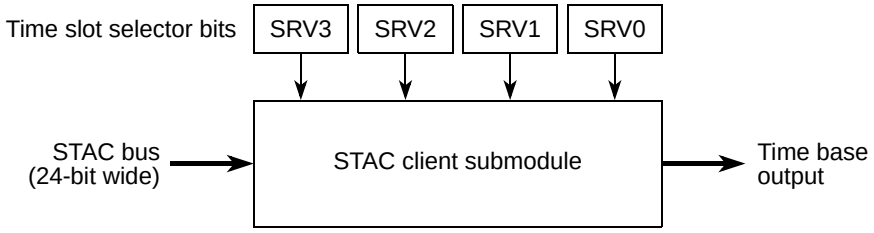
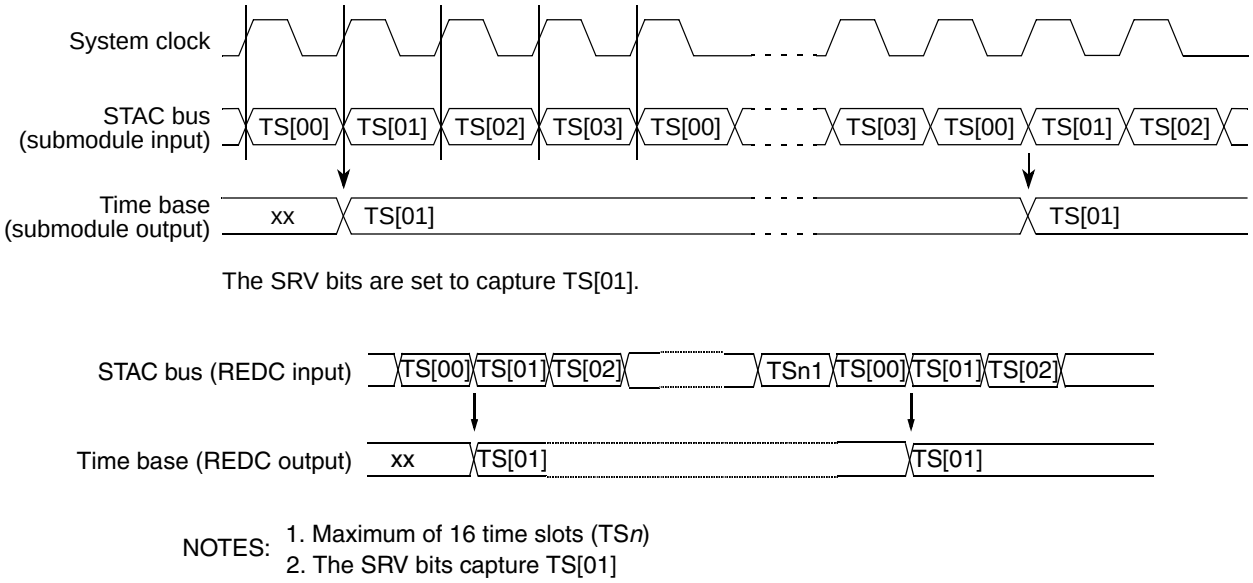


Figure 17-11. STAC Client Submodule Block Diagram

Bits SRV[0:3] in register EMIOS_MCR, selects the time slot of the STAC output bus. Figure 17-12 shows a timing diagram for the STAC client submodule.



NOTES:
1. Maximum of 16 time slots (TS*n*)
2. The SRV bits capture TS[01]

Figure 17-12. Timing Diagram for the STAC Bus and STAC Client Submodule Output

Every time the selected time slot changes, the STAC client submodule output is updated.

17.4.2.1 Effect of Freeze on the STAC Client Submodule

When the FRZ bit in the EMIOS_MCR is set and the module is in debug mode, the operation of the STAC client submodule is not affected; that is, there is no freeze function in this submodule.

17.4.3 Global Clock Prescaler Submodule (GCP)

The global trace prescaler divides the system clock to generate a clock for the unified channels. The system clock is prescaled by the value defined according to the GPRE[0:7] bits in the EMIOS_MCR. The output is clocked every time the counter overflows. Counting is enabled by setting EMIOS_MCR[GPREN]. The counter can be stopped at any time by clearing this bit, thereby stopping the internal counter in all the unified channels.

NOTE

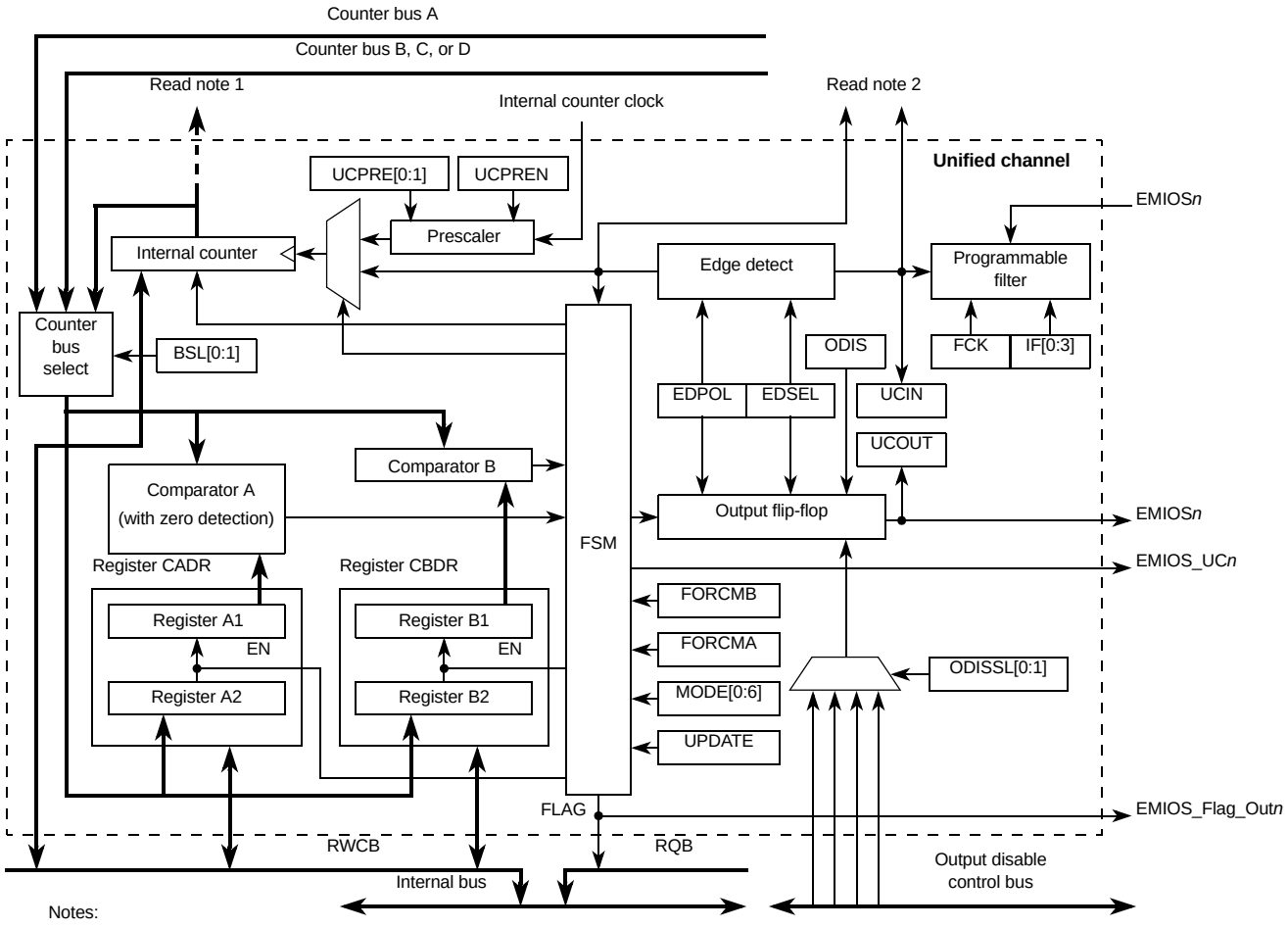
When the FRZ bit in the EMIOS_MCR is set and the module is in debug mode, the operation of the GCP submodule is not affected; there is no freeze function in this submodule.

17.4.4 Unified Channel (UC)

Figure 17-13 shows the unified channel block diagram. Each unified channel consists of the following:

- Counter bus select that sets the time base used for all timing functions by the channel
- Programmable clock prescaler
- Two double buffered data registers A and B that allow up to two input capture and/or output compare events to occur before software intervention is needed.
- Two comparators (equal only) A and B that compare the selected counter bus with the value in the data registers
- Internal counter for use as a local time base or to count input events
- Programmable input filter that ensures that only valid pin transitions are received by a channel
- Programmable input edge-detector that detects rising, falling, or both edges
- Output flip-flop that holds the logic level applied to the output pin
- eMIOS status and control registers
- Output disable input selector that assigns an output-disabled input signal for use as the unified channel output disable
- Control state machine (FSM)

The major components and functions of the unified channels are discussed in Section 17.4.4.1, “Programmable Input Filter (PIF)” through Section 17.4.4.4, “Unified Channel Operating Modes.”



Notes:

1. Counter bus A can be driven by either the STAC bus or channel 23. Refer to EMIOS_MCR[ETB]. Channel 0 drives counter bus B, channel 8 drives counter bus C and channel 16 drives counter bus D. Counter bus B can be selected as the counter for channels 0-7, counter bus C for channels 8-15, and counter bus D for channels 16-23. Refer to Figure 1-1 and EMIOS_CCR*n*[BS].
2. Goes to the finite state machine of the UC[n-1]. These signals are used for QDEC mode.

Figure 17-13. Unified Channel Block Diagram

17.4.4.1 Programmable Input Filter (PIF)

The PIF ensures that only valid input pin transitions are received by the unified channel edge detector. A block diagram of the PIF is shown in Figure 17-14.

The PIF is a 5-bit programmable up counter that is incremented by the selected clock source, according to bits IF[0:3] in EMIOS_CCR*n*. The clock source is selected by the EMIOS_CCR*n*[FCK] bit.

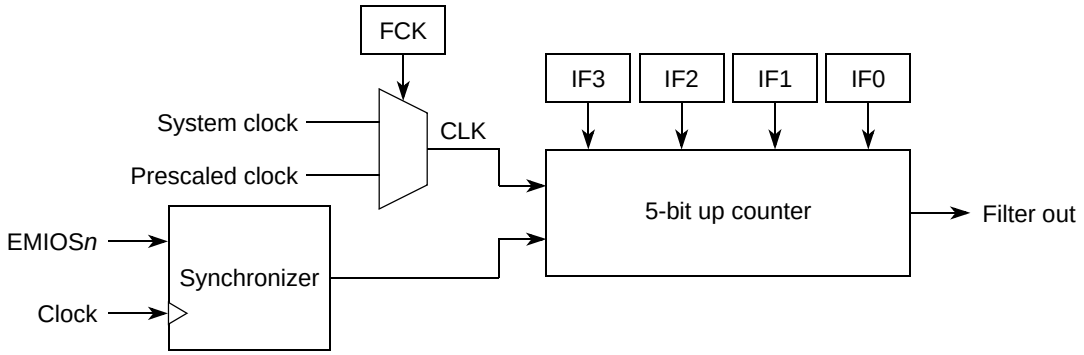


Figure 17-14. Programmable Input Filter Submodule Diagram

The input signal is synchronized by the system clock. When a state change occurs in this signal, the 5-bit counter starts counting up. As long as the new state is stable on the pin, the counter continues incrementing. If a counter overflows occurs, the new pin value is validated. In this case, it is transmitted as a pulse edge to the edge detector. If the opposite edge appears on the pin before validation (overflow), the counter is reset. At the next synchronized pin transition, the counter starts counting again. Any pulse that is shorter than a full range of the masked counter is regarded as a glitch, and it is not passed on to the edge detector. A timing diagram of the input filter is shown in Figure 17-15.

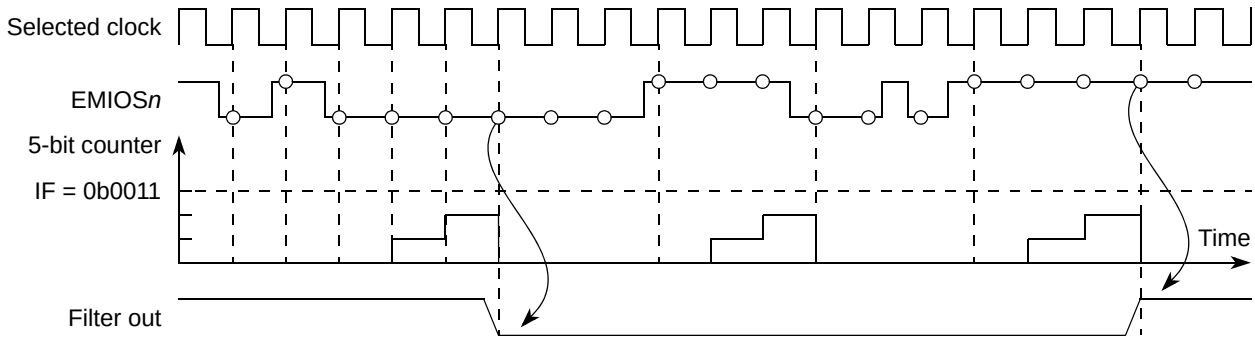


Figure 17-15. Programmable Input Filter Example

17.4.4.2 Clock Prescaler (CP)

A unified channel has a clock prescaler (CP) that divides the global clock prescaler (refer to Section 17.4.3, “Global Clock Prescaler Submodule (GCP)”) output signal to generate a clock enable for the internal counter of the unified channel. It is a programmable 2-bit down counter. The global clock prescaler submodule (GCP) output signal is prescaled by the value defined in Table 17-9 according to the UCPRE[0:1] bits in the EMIOS_CCR*n*. The output is clocked every time the counter reaches zero. Counting is enabled by setting the UCPREN bit in the EMIOS_CCR*n*. The counter can be stopped at any time by clearing this bit, thereby stopping the internal counter in the unified channel.

17.4.4.3 Effect of Freeze on a Unified Channel

When in debug mode and the EMIOS_MCR[FRZ] bit and the EMIOS_CCR*n*[FREN] bit are both set, the internal counter and the unified channel’s capture and compare functions are halted. The UC is frozen in its current state.

During freeze, all registers are accessible. When the unified channel is operating in an output mode, the force match functions remain available, allowing the software to force the output to the desired level.

For input modes, any input events that occurs while the channel is frozen are ignored.

When exiting debug mode or freeze enable bit is cleared (FRZ in the EMIOS_MCR or FREN in the EMIOS_CCR*n*) the channel actions resume.

17.4.4.4 Unified Channel Operating Modes

The mode of operation of a unified channel is determined by the mode select bits MODE[0:6] in the EMIOS_CCR*n*. See Table 17-10 for details.

When entering an output mode (except for GPIO mode), the output flip-flop is set to the complement of the EDPOL bit in the EMIOS_CCR*n*.

Because the internal counter EMIOS_CCNTR*n* continues to run in all modes (except for GPIO mode), it is possible to use this counter as the UC time base unless it (the internal counter) is a required resource in the operation of the selected mode.

To provide smooth waveform generation while allowing A and B registers to be asynchronously updated during UC operation, the double-buffered modes MCB, OPWFMB, OPWMB, and OPWMCB are provided (beginning at Section 17.4.4.4.15, “Modulus Counter Buffered Mode (MCB)”). In these modes the A and B registers are double buffered. Descriptions of the double-buffered modes are presented separately, because there are several basic differences from the single-buffered MC, OPWFM, OPWM, and OPWMC modes.

In the following pages, Section 17.4.4.4.1, “General Purpose Input/Output Mode (GPIO)” through Section 17.4.4.4.14, “Output Pulse-Width Modulation Mode (OPWM) and Section 17.4.4.4.18, “Output Pulse-Width Modulation, Buffered Mode (OPWMB)” explain in detail the unified channels’ modes of operation.

17.4.4.4.1 General Purpose Input/Output Mode (GPIO)

The following table lists the general purpose input/output mode settings:

Table 17-14. GPIO Operating Mode

MODE[0:6]	Unified Channel GPIO Operating Mode
0b0000000	General purpose input/output mode (input)
0b0000001	General purpose input/output mode (output)

In GPIO mode, all input capture and output compare functions of the UC are disabled, the internal counter (EMIOS_CCNTRn register) is cleared and disabled. All control bits remain accessible. To prepare the UC for a new operating mode, writing to registers EMIOS_CADR*n* or EMIOS_CBDR*n* stores the same value in registers A1/A2 or B1/B2, respectively.

MODE[6] bit selects between input (MODE[6] = 0) and output (MODE[6] = 1) modes.

It is required that when changing MODE[0:6], the application software goes to GPIO mode first to reset the UC's internal functions properly. Failure to do this can lead to invalid and unexpected output compares and input capture results, or can cause the FLAGs to be set incorrectly.

In GPIO input mode, the FLAG generation is determined according to EDPOL and EDSEL bits and the input pin status can be determined by reading the UCIN bit.

In GPIO output mode, the unified channel is used as a single output port pin and the value of the EDPOL bit is permanently transferred to the output flip-flop.

NOTE

The GPIO modes provided in the eMIOS are particularly useful as interim modes when certain other eMIOS modes are being dynamically configured and enabled or disabled during the execution of the application. For normal GPIO function on the eMIOS pins, it is recommended that the SIU be used to configure those pins as system GPIO. See Section 6.2.1.3, "General-Purpose I/O (GPIO[0:213])" pins.

17.4.4.4.2 Single-Action Input Capture Mode (SAIC)

The following table lists the single action input capture mode settings:

Table 17-15. SAIC Operating Mode

MODE[0:6]	Unified Channel SAIC Operating Mode
0b0000010	Single action input capture mode

In SAIC mode, when a triggering event occurs on the input pin, the value on the selected time base is captured into register A2. At the same time, the FLAG bit is set to indicate that an input capture has occurred. Register EMIOS_CADR*n* returns the value of register A2.

The input capture is triggered by a rising, falling or either edges in the input pin, as configured by EDPOL and EDSEL bits in EMIOS_CCR*n*.

Figure 17-16 shows how the unified channel can be used for input capture.

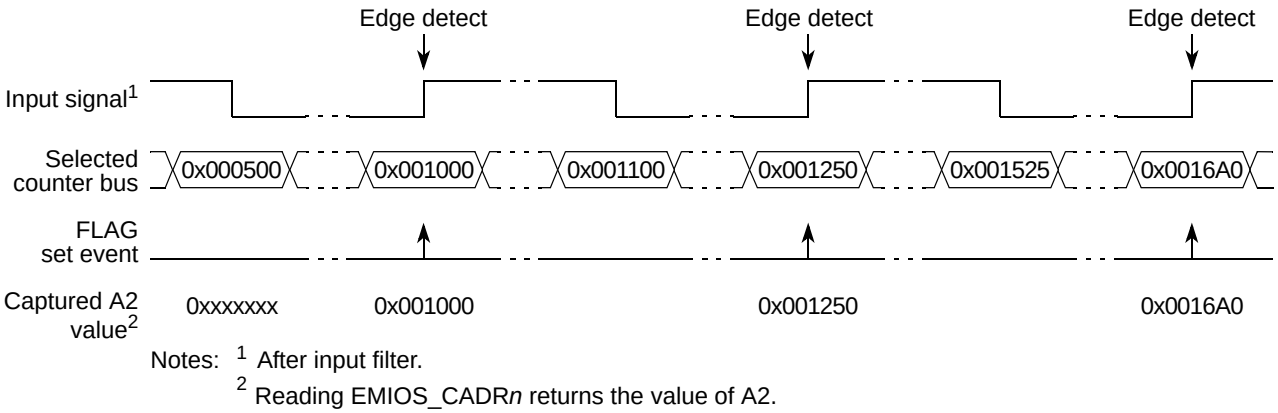


Figure 17-16. Single-action Input Capture Example

17.4.4.4.3 Single-action Output Compare Mode (SAOC)

The following table lists the single action output compare mode setting:

Table 17-16. SAOC Operating Mode

MODE[0:6]	Unified Channel SAOC Operating Mode
0b0000011	Single-action output compare mode

In SAOC mode, a match value is loaded in register A2 and then transferred to register A1 to be compared with the selected time base. When a match occurs, the EDSEL bit selects if the output flip-flop is toggled or if the value in EDPOL is transferred to it. At the same time, the FLAG bit is set to indicate that the output compare match has occurred. Writing to register EMIOS_CADR*n* stores the value in register A2 and reading to register EMIOS_CADR*n* returns the value of register A1.

An output compare match can be simulated in software by setting the FORCMA bit in EMIOS_CCR*n*. In this case, the FLAG bit is not set.

Figure 17-17 shows how to use the unified channel perform a single output compare while transferring EDPOL to the output flip-flop. This figure toggles the output flip-flop with Figure 17-18 at each match.

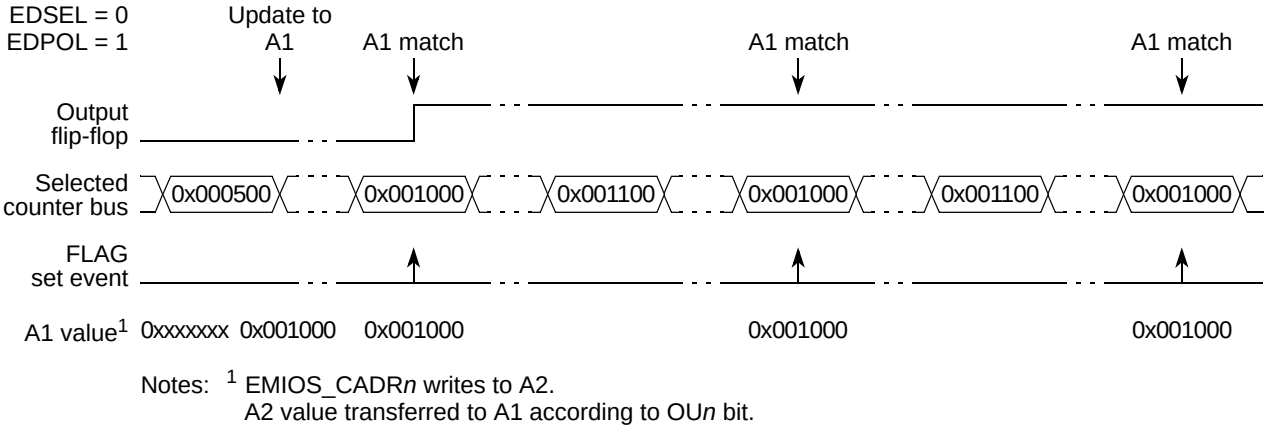


Figure 17-17. SAOC Example with EDPOL Value Transferred to the Output Flip-flop

Figure 17-18 shows how to use the unified channel perform a single output compare while transferring EDPOL to the output flip-flop. This figure toggles the output flip-flop with Figure 17-17 at each match.

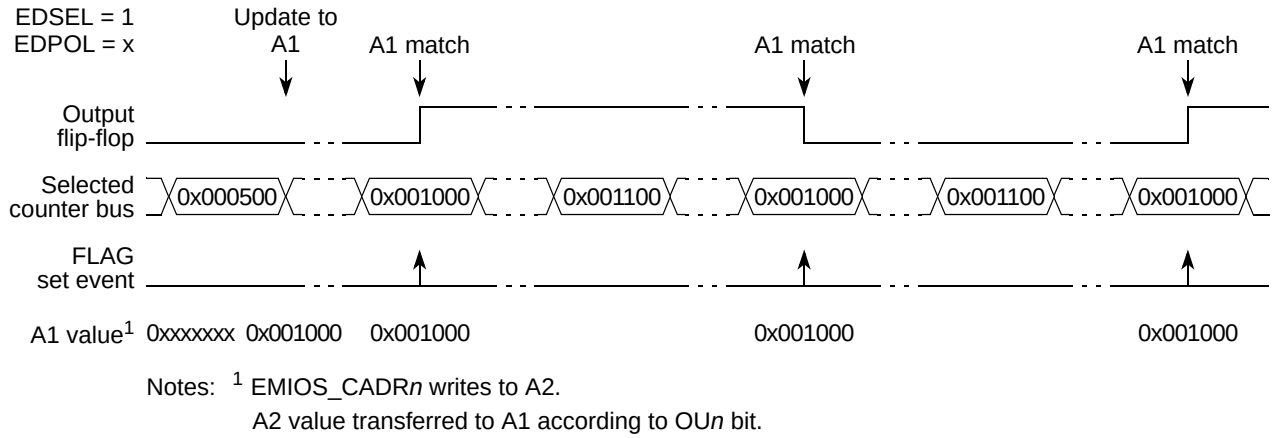


Figure 17-18. SAOC Example Toggling the Output Flip-flop

17.4.4.4.4 Input Pulse-Width Measurement Mode (IPWM)

The following table lists the input pulse-width measurement mode setting:

Table 17-17. IPWM Operating Mode

MODE[0:6]	Unified Channel IPWM Operating Mode
0b0000100	Input pulse-width measurement mode

The IPWM mode measures the width of a positive or negative pulse by capturing the leading edge on register B1 and the trailing edge on register A2. Successive captures are done on consecutive edges of opposite polarity. The leading edge sensitivity (pulse polarity) is selected by EDPOL bit in the

EMIOS_CCR*n*. Registers EMIOS_CADR*n* and EMIOS_CBDR*n* return the values in register A2 and B1, respectively.

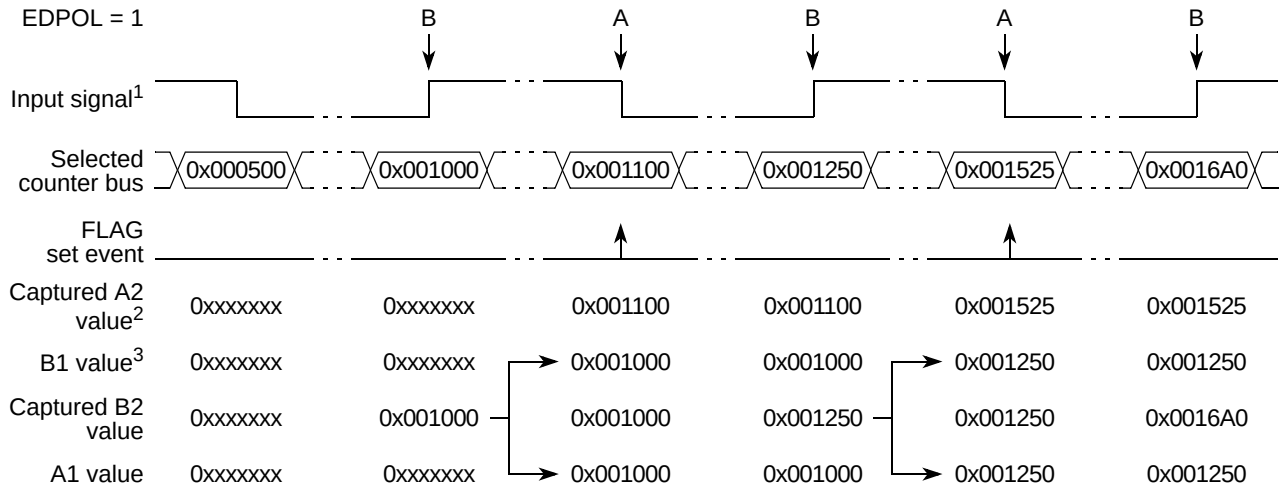
The capture function of register A2 remains disabled until the first leading edge triggers the first input capture on register B2. When this leading edge is detected, the count value of the selected time base is latched into register B2; the FLAG bit is not set. When the trailing edge is detected, the count value of the selected time base is latched into register A2 and, at the same time, the FLAG bit is set and the content of register B2 is transferred to register B1.

If subsequent input capture events occur while the corresponding FLAG bit is set, registers A2, B1, and A1 are updated with the latest captured values and the FLAG remains set. Registers EMIOS_CADR*n* and EMIOS_CBDR*n* return the value in registers A2 and B1, respectively.

To guarantee coherent access, reading EMIOS_CADR*n* forces B1 to be updated with the content of register A1. At the same time transfers between B2 and B1 are disabled until the next read of the EMIOS_CBDR*n* register. Reading EMIOS_CBDR*n* forces B1 to be updated with A1 register content and re-enables transfers from B2 to B1, to take effect at the next trailing edge capture. Transfers from B2 to A1 are not blocked at any time.

The input pulse width is calculated by subtracting the value in B1 from A2.

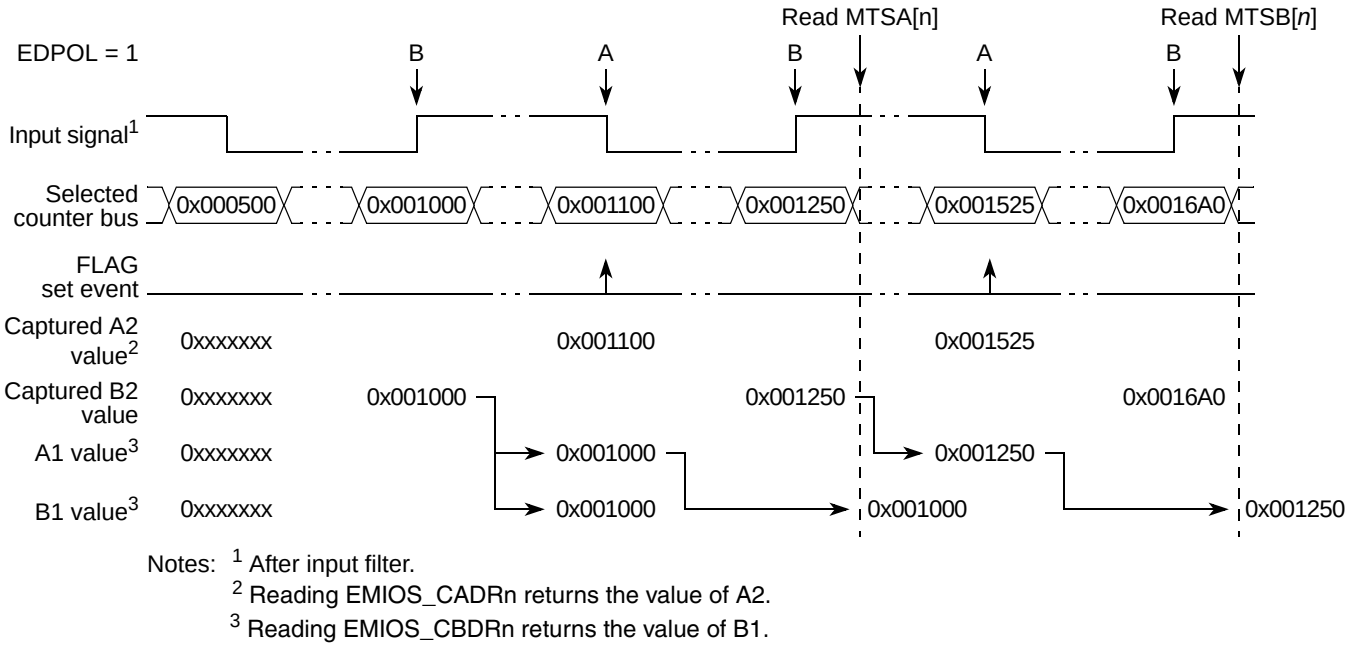
Figure 17-19 shows how the unified channel can be used for input pulse-width measurement.



Notes: 1 After input filter.
2 Reading EMIOS_CADRn returns the value of A2, writing EMIOS_CADRn writes to A2.
3 Reading EMIOS_CBDRn returns the value of B1, writing EMIOS_CBDRn writes to B1.

Figure 17-19. Input pulse-width Measurement Example

Figure 17-20 shows the A1 and B1 updates when EMIOS_CADR*n* and EMIOS_CBDR*n* register reads occur. The A1 register always has coherent data related to the A2 register. Note also that when an EMIOS_CADR*n* read is performed, the B1 register is loaded with A1 register content. This guarantee that the data in register B1 always has the coherent data related to the last EMIOS_CADR*n* read. The B1 register updates remains locked until an EMIOS_CBDR*n* read occurs. If an EMIOS_CADR*n* read is performed, the B1 register is updated with A1 register content even if the B1 update is locked by a previous EMIOS_CADR*n* read operation.



Notes: [1] After input filter.
[2] Reading EMIOS_CADRn returns the value of A2.
[3] Reading EMIOS_CBDRn returns the value of B1.

Figure 17-20. B1 and A1 Updates at EMIOS_CADR*n* and EMIOS_CBDR*n* Reads

Reading EMIOS_CADR*n* followed by EMIOS_CBDR*n* always provides coherent data. If coherent data is not required, invert the sequence of reads; read EMIOS_CBDR*n* before reading EMIOS_CADR*n*. If B1 register updates are blocked after an EMIOS_CADR*n* read, a second EMIOS_CBDR*n* read is required to release B1 register updates.

17.4.4.4.5 Input Period Measurement Mode (IPM)

The following table lists the input period measurement mode setting:

Table 17-18. IPM Operating Mode

MODE[0:6]	Unified Channel IPM Operating Mode
0b0000101	Input period measurement mode

The IPM mode allows the measurement of the period of an input signal by capturing two consecutive rising edges or two consecutive falling edges. Successive input captures are done on consecutive edges of the same polarity. The edge polarity is defined by the EDPOL bit in the EMIOS_CCR*n*.

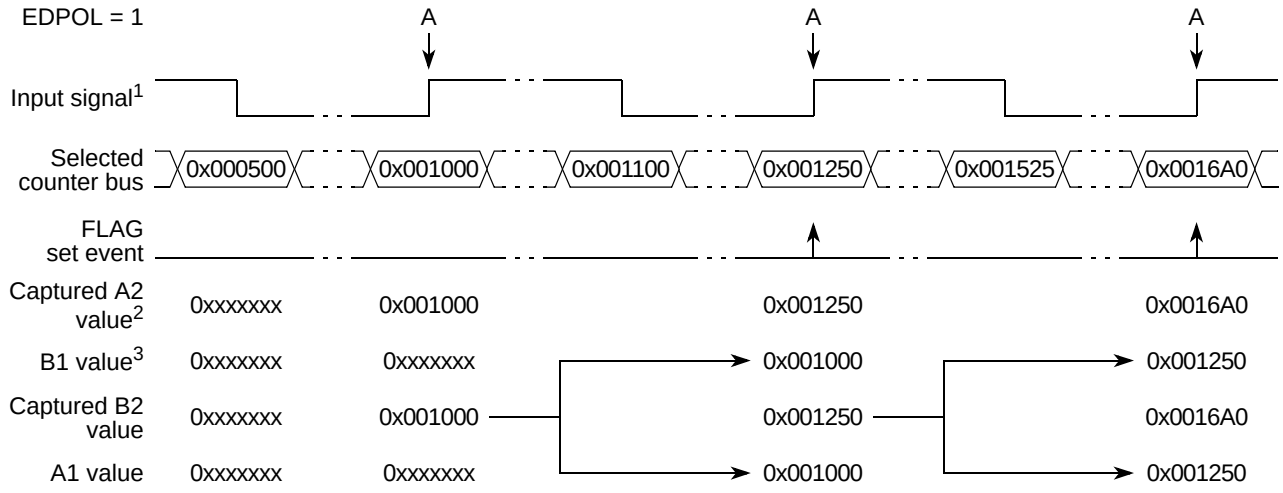
When the first edge of selected polarity is detected, the selected time base is latched into the registers A2 and B2, and the data previously held in register B2 is transferred to register B1. On this first capture the FLAG line is not set, and the values in registers B1 is meaningless. On the second and subsequent captures, the FLAG line is set and data in register B2 is transferred to register B1.

When the second edge of the same polarity is detected, the counter bus value is latched into registers A2 and B2, the data previously held in register B2 is transferred to data register B1 and to register A1. The FLAG bit is set to indicate that the start and end points of a complete period have been captured. This sequence of events is repeated for each subsequent capture. Registers EMIOS_CADR*n* and EMIOS_CBDR*n* return the values in register A2 and B1, respectively.

To allow coherent data, reading EMIOS_CADR*n* forces A1 content to be transferred to the B1 register and disables transfers between B2 and B1. These transfers are disabled until the next read of the EMIOS_CBDR*n* register. Reading EMIOS_CBDR*n* forces A1 content to be transferred to B1 and re-enables transfers from B2 to B1, to take effect at the next edge capture.

The input pulse period is calculated by subtracting the value in B1 from A2.

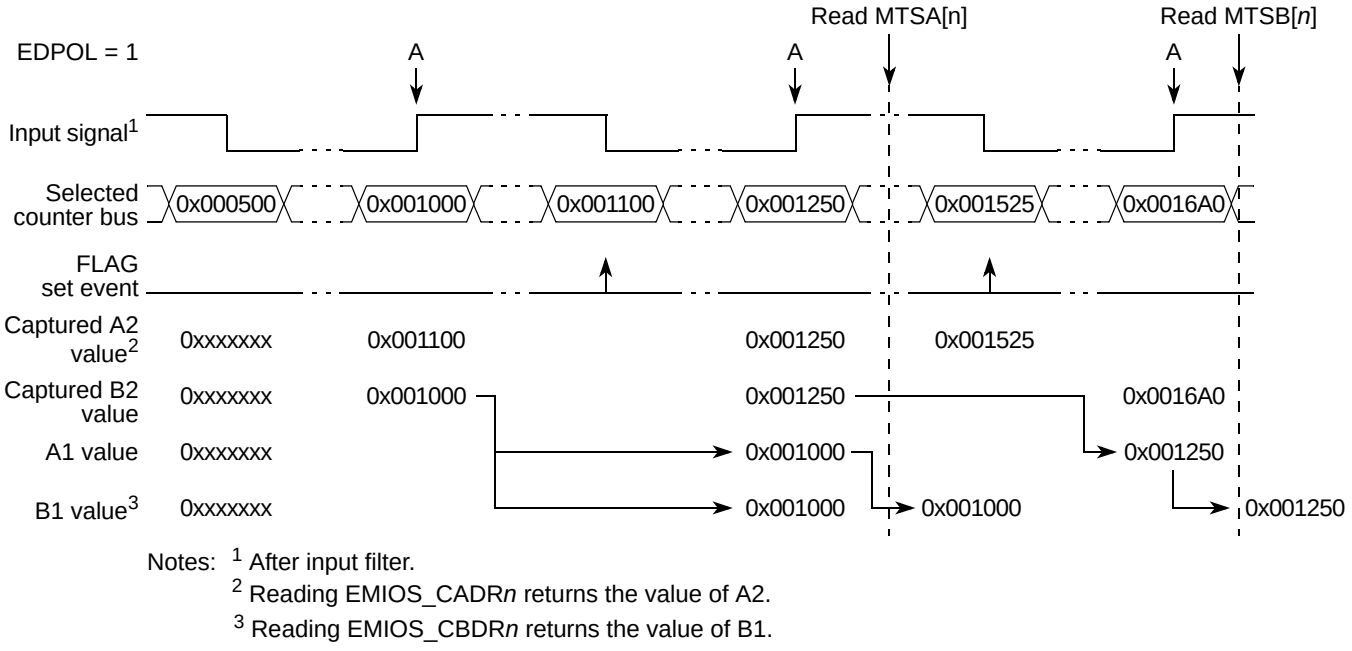
Figure 17-21 shows how the unified channel can be used for input period measurement.



Notes: 1 After input filter.
2 Reading EMIOS_CADRn returns the value of A2.
3 Reading EMIOS_CBDRn returns the value of B1.

Figure 17-21. Input Period Measurement Example

Figure 17-22 describes the A1 and B1 register updates when EMIOS_CADR*n* and EMIOS_CBDR*n* read operations are performed. When an EMIOS_CADR*n* read occurs the content of A1 is transferred to B1 thus providing coherent data in the A2 and B1 registers. Transfers from B2 to B1 are then blocked until EMIOS_CBDR*n* is read. After EMIOS_CBDR*n* is read, register A1 content is transferred to register B1 and the transfers from B2 to B1 are re-enabled to occur at the transfer edges, which is the leading edge in the Figure 17-22 example.



Notes: [1] After input filter.
[2] Reading EMIOS_CADR*n* returns the value of A2.
[3] Reading EMIOS_CBDR*n* returns the value of B1.

Figure 17-22. A1 and B1 Updates at EMIOS_CADR and EMIOS_CBDR Reads

17.4.4.4.6 Double-action Output Compare Mode (DAOC)

The following table lists the double-action output compare mode settings:

Table 17-19. DAOC Operating Modes

MODE[0:6]	Unified Channel DAOC Operating Mode
0b0000110	Double-action output compare (with FLAG set on the second match)
0b0000111	Double-action output compare (with FLAG set on both matches)

In the DAOC mode the leading and trailing edges of the variable pulse-width output are generated by matches occurring on comparators A and B, respectively.

When the DAOC mode is first selected (coming from GPIO mode) both comparators are disabled. Comparators A and B are enabled by updating registers A1 and B1 respectively and remain enabled until a match occurs on that comparator, when it is disabled again. To update registers A1 and B1, a write to A2 and B2 must occur and the EMIOS_CCR*n*[ODIS] bit must be cleared.

The output flip-flop is set to the value of EMIOS_CCR*n*[EDPOL] when a match occurs on comparator A and to the complement of EDPOL when a match occurs on comparator B.

MODE[6] controls if the EMIOS_CSR*n*[FLAG] is set on both matches or just on the second match (see Table 17-10 for details).

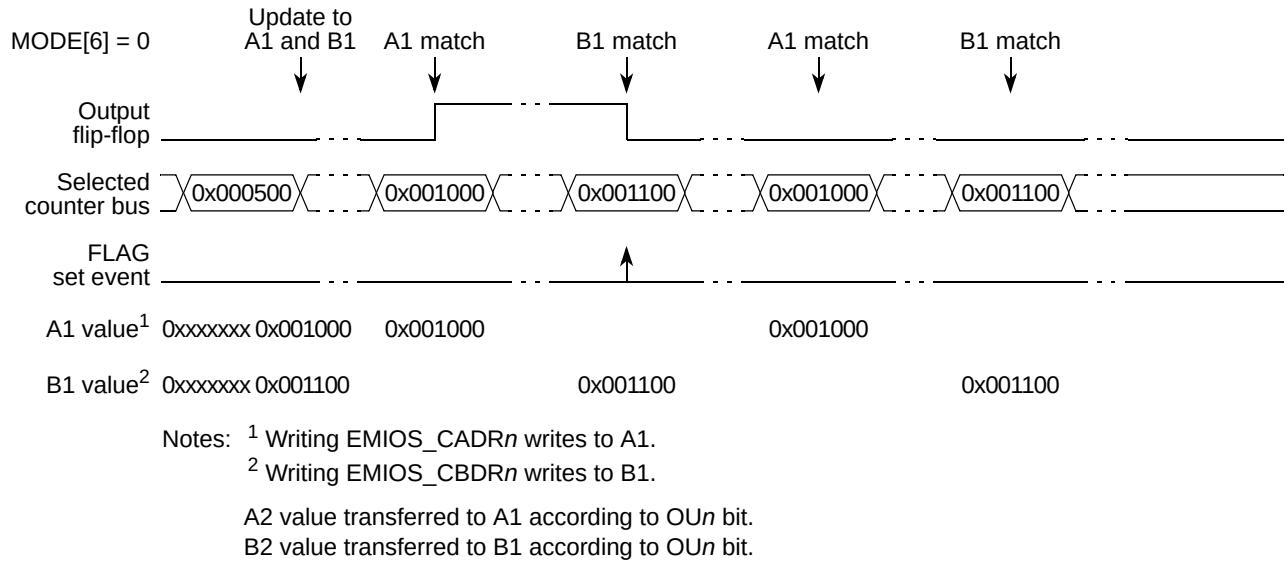
If subsequent enabled output compares occur on registers A1 and B1, pulses continue to generate, regardless of the state of the FLAG bit.

At any time, the EMIOS_CCR*n*[FORCMA] and EMIOS_CCR*n*[FORCMB] bits allow the software to force the output flip-flop to the level corresponding to a comparison event in comparator A or B, respectively. The FLAG bit is not affected by these forced operations.

NOTE

If both registers (A1 and B1) are loaded with the same value, the unified channel behaves as if a single match on comparator B had occurred; that is, the output flip-flop is set to the complement of EDPOL bit and the FLAG bit is set.

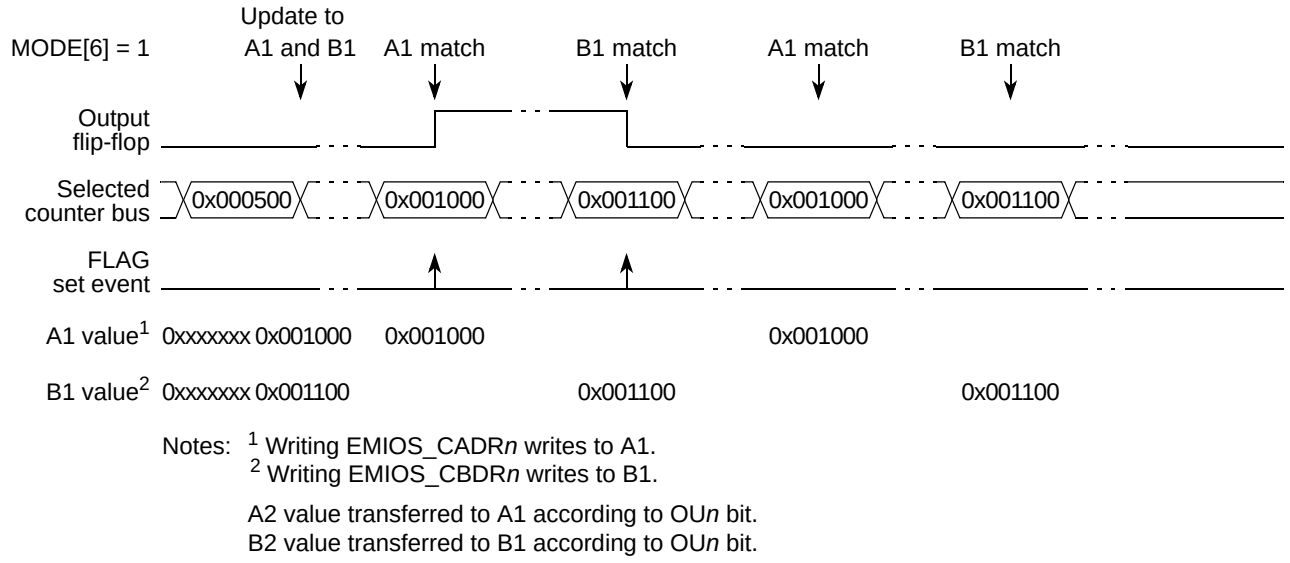
Figure 17-23 and Figure 17-24 show how the unified channel can be used to generate a single output pulse with FLAG bit being set on the second match or on both matches, respectively.



Notes: [1] Writing EMIOS_CADR*n* writes to A1.
[2] Writing EMIOS_CBDR*n* writes to B1.

A2 value transferred to A1 according to OU*n* bit.
B2 value transferred to B1 according to OU*n* bit.

Figure 17-23. Double Action Output Compare with FLAG Set on the Second Match



Notes: [1] Writing EMIOS_CADR*n* writes to A1.
[2] Writing EMIOS_CBDR*n* writes to B1.

A2 value transferred to A1 according to OU*n* bit.
B2 value transferred to B1 according to OU*n* bit.

Figure 17-24. Double-action Output Compare with FLAG Set on Both Matches

17.4.4.4.7 Pulse/Edge Accumulation Mode (PEA)

The following table lists the pulse/edge accumulation mode settings:

Table 17-20. PEA Operating Mode

MODE[0:6]	Unified Channel PEA Operating Mode
0b0001000	Pulse/edge accumulation (continuous)
0b0001001	Pulse/edge accumulation (single shot)

The PEA mode returns the time taken to detect a desired number of input events. MODE[6] bit selects between continuous or single shot operation.

After writing to register A1, the internal counter is cleared on the first input event, ready to start counting input events and the selected timebase is latched into register B2. On the match between the internal counter and register A1, a counter bus capture is triggered to register A2 and B2. The data previously held in register B2 is transferred to register B1 and the FLAG bit is set to indicate that an event has occurred. The desired time interval can be determined by subtracting register B1 from A2. Registers EMIOS_CADR*n* and EMIOS_CBDR*n* return the values in register A2 and B1, respectively.

To guarantee coherent access, reading EMIOS_CADR*n* disables transfers between B2 and B1. These transfers are disabled until the next read of the EMIOS_CBDR*n* register. Reading the EMIOS_CBDR*n* register re-enables transfers from B2 to B1, to take effect at the next transfer event, as described above.[1]

1. If B1 was not updated due to B2 to B1 transfer being disabled after reading register EMIOS_CADR*n*, further EMIOS_CADR*n* and EMIOS_CBDR*n* reads do not return coherent data until a new bus capture is triggered to registers A2 and B2. The capture event is indicated when the channel FLAG asserts. If enabled, the FLAG also generates an interrupt.

The counter clock (an input event) is triggered by a rising or falling edge, or by both the rising and falling edges on the input pin. The polarity of the triggering edge is selected by the EDSEL and EDPOL bits in EMIOS_CCR*n*.

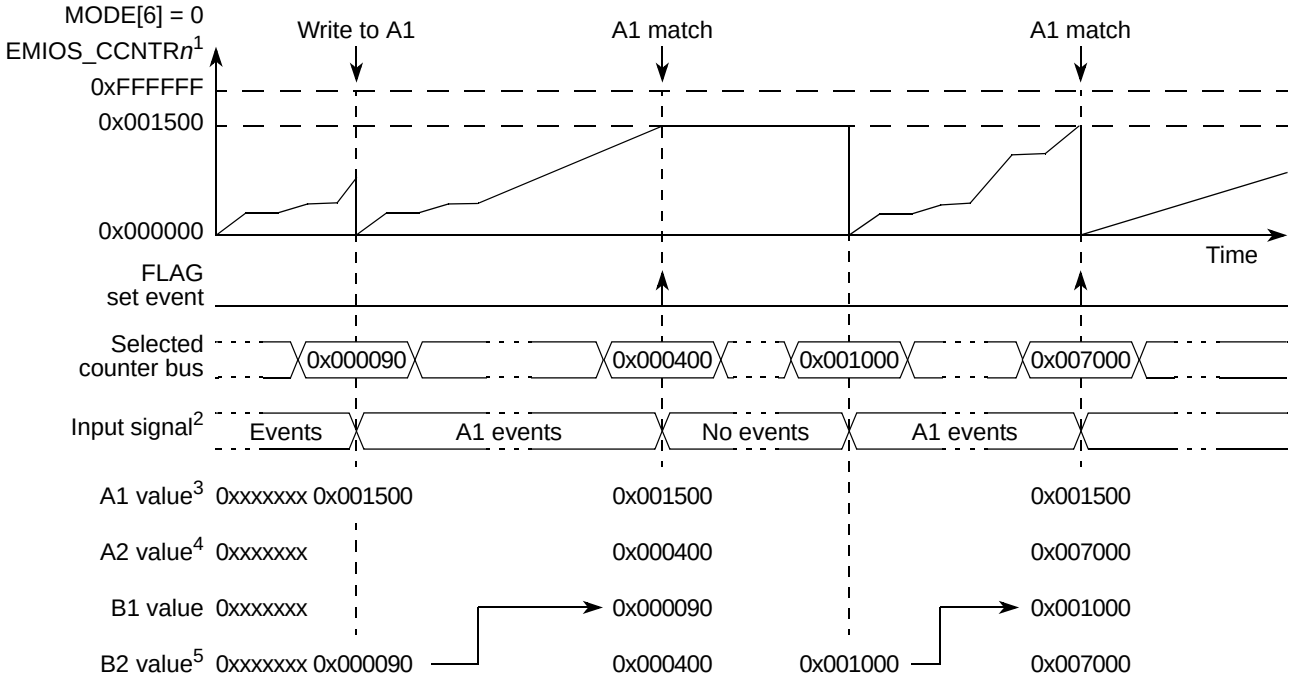
For continuous operating mode (MODE[6] cleared), the counter is cleared on the next input event after a FLAG generation and continues to operate as described above.

For single shot operation (MODE[6] set), the counter is not cleared or incremented after a FLAG generation, until a new writing operation to register A is performed.

NOTE

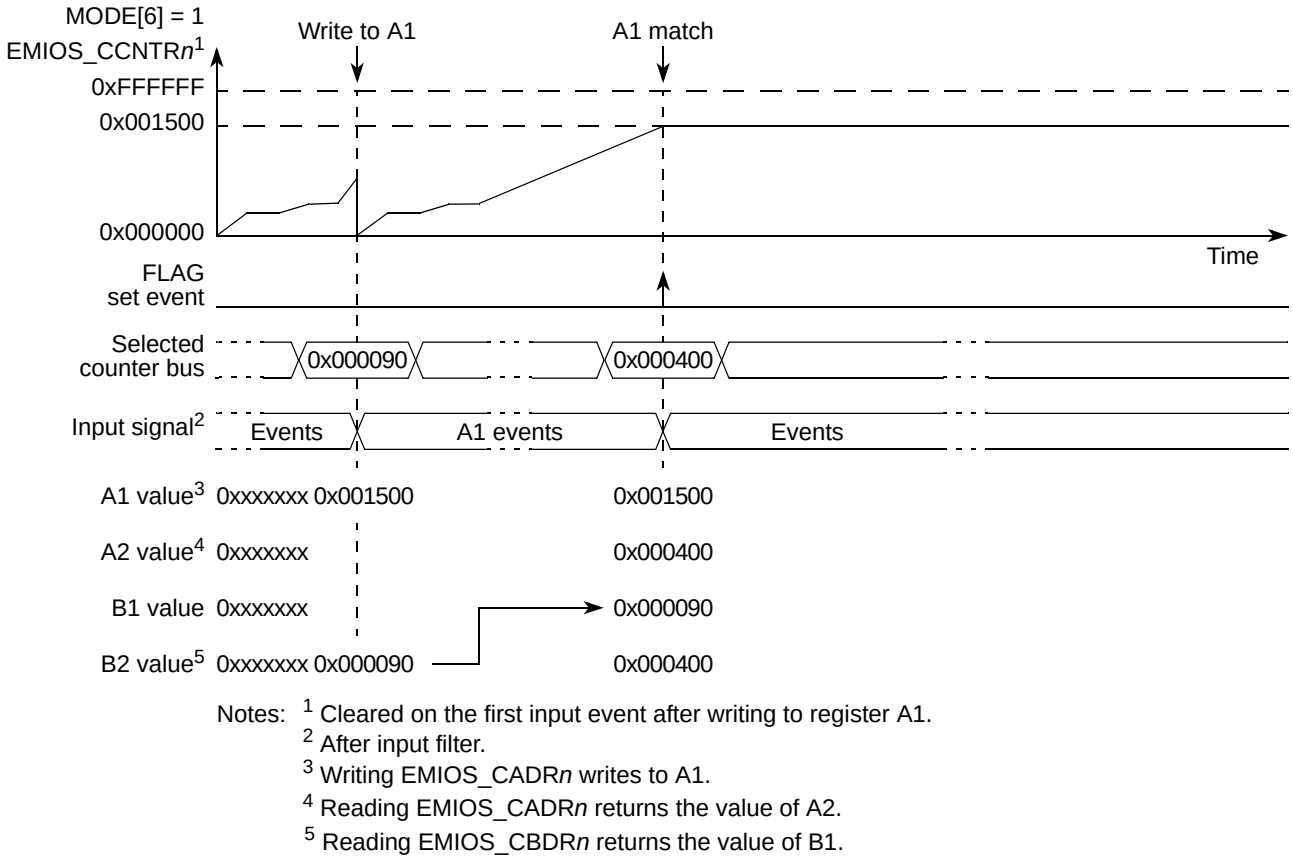
The FORCMA and FORCMB bits have no effect when the unified channel is configured for PEA mode.

Figure 17-25 and Figure 17-26 show how the unified channel can be used for continuous and single shot pulse/edge accumulation mode.



Notes: [1] Cleared on the first input event after writing to register A1.
[2] After input filter.
[3] Writing EMIOS_CADR*n* writes to A1.
[4] Reading EMIOS_CADR*n* returns the value of A2.
[5] Reading EMIOS_CBDR*n* returns the value of B1.

Figure 17-25. Pulse/Edge Accumulation Continuous Mode Example



Notes: [1] Cleared on the first input event after writing to register A1.
[2] After input filter.
[3] Writing EMIOS_CADR*n* writes to A1.
[4] Reading EMIOS_CADR*n* returns the value of A2.
[5] Reading EMIOS_CBDR*n* returns the value of B1.

Figure 17-26. Pulse/Edge Accumulation Single-shot Mode Example

17.4.4.4.8 Pulse and Edge Counting Mode (PEC)

The following table lists the pulse and edge counting mode settings:

Table 17-21. PEC Operating Mode

MODE[0:6]	Unified Channel PEC Operating Mode
0b0001010	Pulse and edge counting (continuous)
0b0001011	Pulse and edge counting (single shot)

The PEC mode returns the amount of pulses or edges detected on the input for a desired time window. MODE[6] bit selects between continuous or single shot operation.

Triggering of the internal counter is done by a rising- or falling-edge or both edges on the input signal. The polarity and the triggering edge is selected by EDSEL and EDPOL bits in EMIOS_CCR*n*.

Register A1 holds the start time and register B1 holds the stop time for the time window. After writing to register A1, when a match occur between comparator A and the selected timebase, the internal counter is cleared and it is ready to start counting input events. When the time base matches comparator B1, the

internal counter is disabled and its content is transferred to register A2. At the same time the FLAG bit is set. Reading registers EMIOS_ALTA*n* or A2 returns the amount of detected pulses.

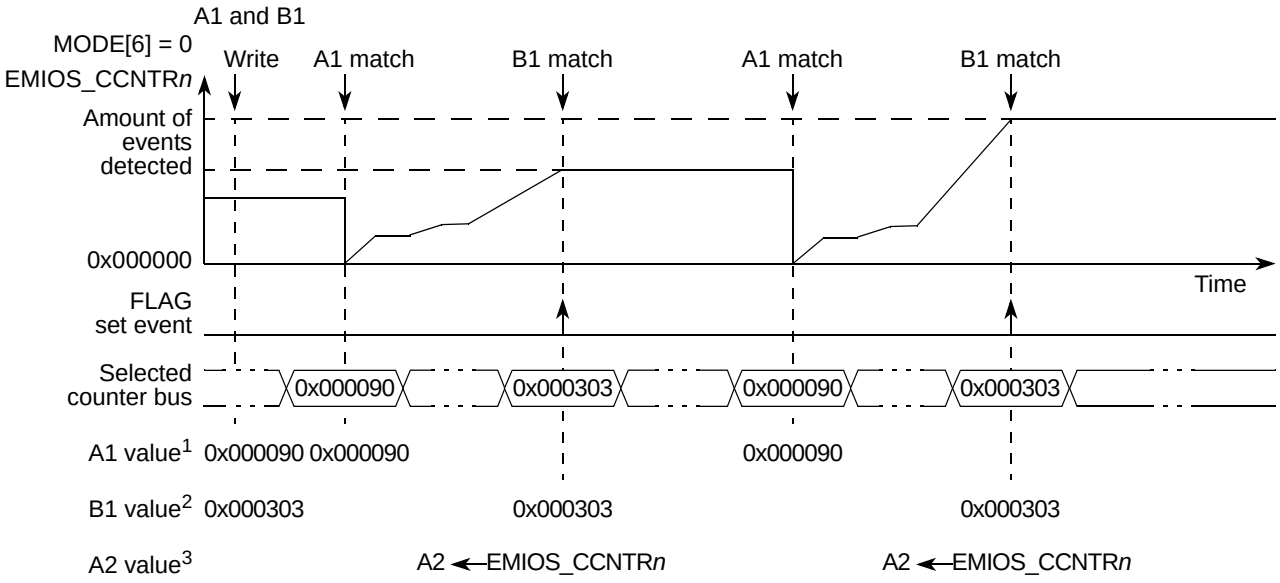
For continuous operation (MODE[6] cleared), the next match between comparator A and the selected time base clears the internal counter and counting is enabled again. To guarantee the accuracy when reading EMIOS_CCNTR*n* after the flag is set, the software must check if the time base value is out of the time interval defined by registers A1 and B1. Alternatively register A2 always holds the latest available measurement providing coherent data at any time after the first FLAG occurs. This register is addressed by the alternate address EMIOS_ALTA*n*.

For single shot operation (MODE[6] set), the next match between comparator A and the selected time base has no effect, until a new write to register A is performed. The EMIOS_CCNTR*n* content is also transferred to register A2 when a match in the B comparator occurs.

NOTE

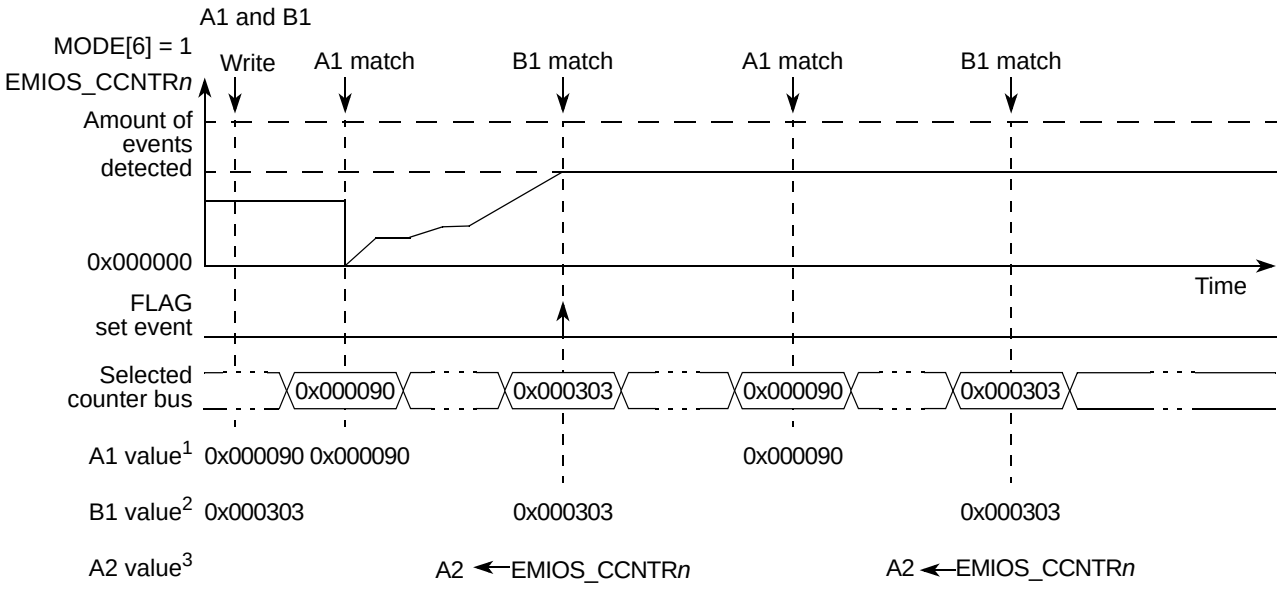
The FORCMA and FORCMB bits have no effect when the unified channel is configured for PEC mode.

Figure 17-27 and Figure 17-28 show how the unified channel can be used for continuous or single shot pulse/edge counting mode.



Notes: [1] Writing EMIOS_CADR*n* writes to A1.
[2] Writing EMIOS_CBDR*n* writes to B1.
[3] Reading EMIOS_ALTA*n* returns the value of A2.

Figure 17-27. Pulse/Edge Counting Continuous Mode Example



Notes: [1] Reading EMIOS_CADR*n* returns the value of A1.
[2] Reading EMIOS_CBDR*n* returns the value of B1.
[3] Reading EMIOS_ALTA*n* returns the value of A2. (EMIOS_ALTA only used in PEC and WPTA modes)

Figure 17-28. Pulse/Edge Counting Single-Shot Mode Example

17.4.4.4.9 Quadrature Decode Mode (QDEC)

The following table lists the quadrature decode mode settings:

Table 17-22. QDEC Operating Mode

MODE[0:6]	Unified Channel QDEC Operating Mode
0b0001100	Quadrature decode (for count and direction encoders type)
0b0001101	Quadrature decode (for phase_A and phase_B encoders type)

Quadrature decode mode uses UC*n* operating in QDEC mode and the programmable input filter (PIF) from UC[n-1]. UC[n-1] can be configured, at the same time, to an operation mode that does not use I/O pins, such as MC mode (modulus counter). The connection among the UCs is circular; that is, when UC0 is running in QDEC mode, the programmable input filter from UC23 is being used.

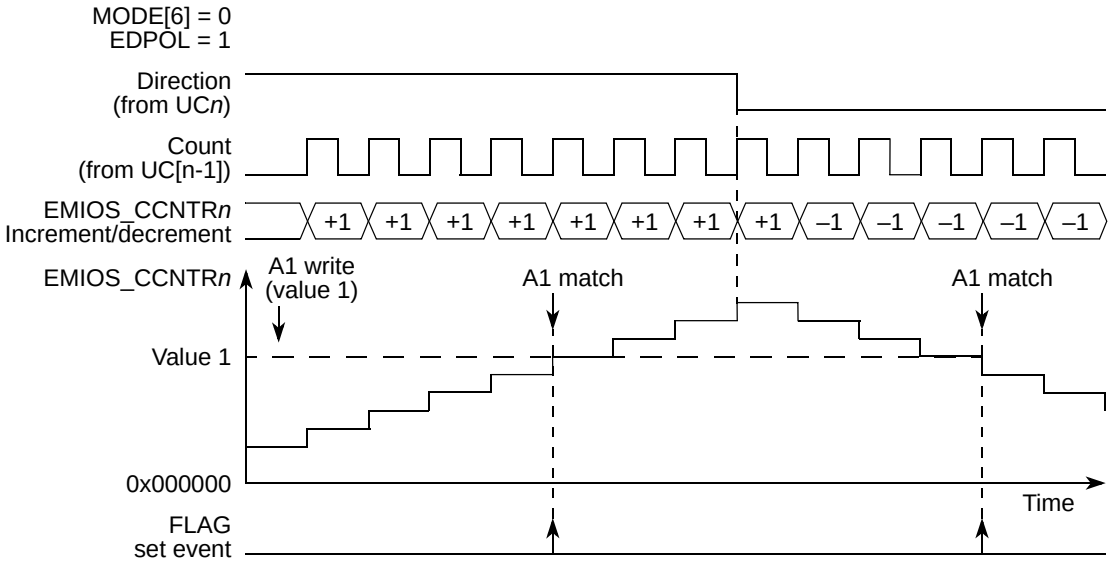
This mode generates a FLAG every time the internal counter matches A1 register. The internal counter is automatically selected and is not cleared when entering this mode.

MODE[6] bit selects which type of encoder is used: count and direction encoder or phase_A and phase_B encoders.

When operating with count and direction encoder (MODE[6] cleared), UC*n* input pin must be connected to the direction signal and UC[n-1] input pin must be connected to the count signal of the quadrature encoder. UC*n* EDPOL bit selects count direction according to direction signal and UC[n-1] EDPOL bit selects if the internal counter is clocked by the rising or falling edge of the count signal.

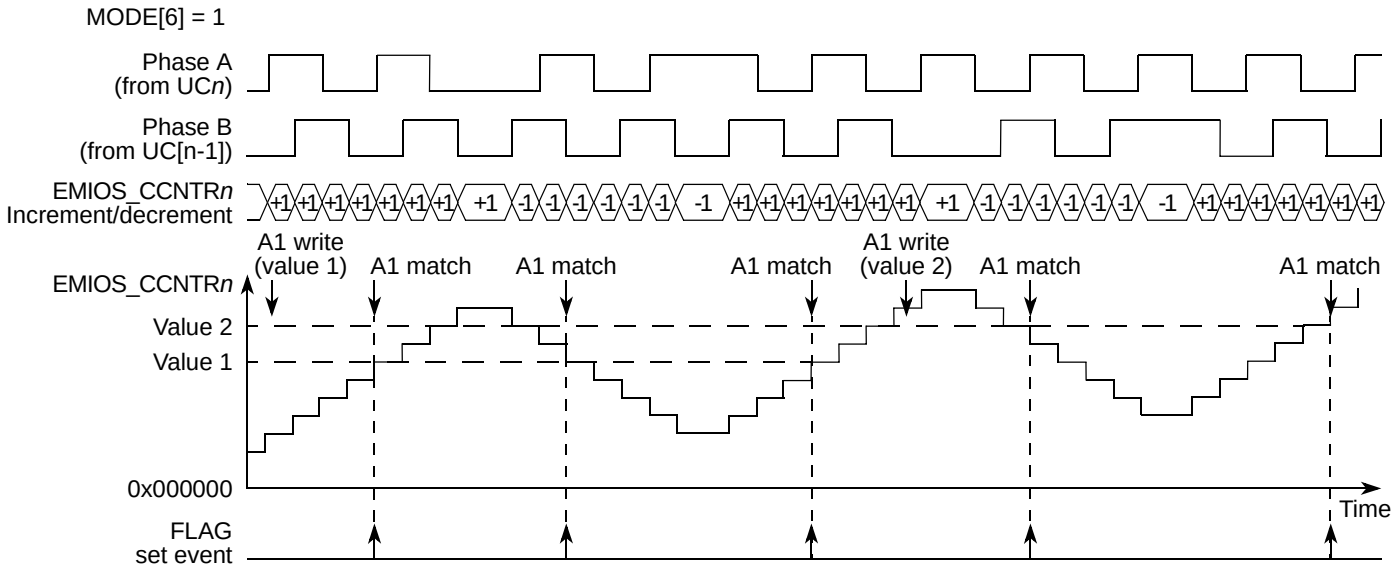
When operating with phase_A and phase_B encoder (MODE[6] set), UC*n* input pin must be connected to the phase_A signal and UC[n-1] input pin must be connected to the phase_B signal of the quadrature encoder. EDPOL bit selects the count direction according to the phase difference between phase_A and phase_B signals.

Figure 17-29 and Figure 17-30 show two unified channels configured to quadrature decode mode for count and direction encoder and phase_A and phase_B encoders, respectively.



Note: Writing EMIOS_CADR*n* writes to A1.

Figure 17-29. Quadrature Decode Mode Example with Count and Direction Encoder



Note: Writing EMIOS_CADR*n* writes to A1.

Figure 17-30. Quadrature Decode Mode Example with Phase_A and Phase_B Encoder

17.4.4.4.10 Windowed Programmable Time Accumulation Mode (WPTA)

The WPTA mode accumulates the sum of the total high time or low time of an input signal over a programmable interval (time window).

The prescaler bits UCPRE[0:1] in EMIOS_CCR*n* define the increment rate of the internal counter.

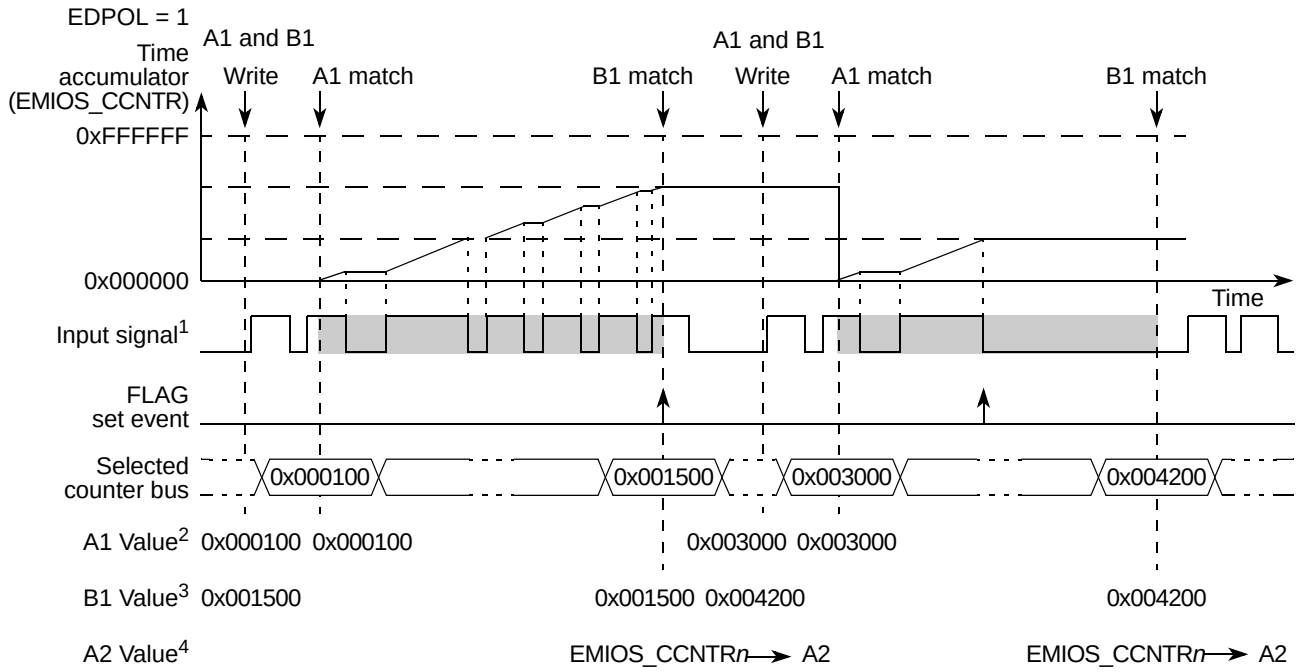
Register A1 holds the start time and register B1 holds the stop time of the programmable time interval. When a match occurs between register A and the selected timebase, the internal counter is cleared and it is ready to start counting. The internal counter is used as a time accumulator; that is, it counts up when the input signal has the same polarity of EDPOL bit in EMIOS_CCR*n* and does not count otherwise. When a match occurs in comparator B, the internal counter is disabled regardless of the input signal polarity and the FLAG bit is set. At the same time the content of EMIOS_CCNTR*n* is transferred to register A2. Reading EMIOS_CCNTR*n* or A2 returns the high or low time of the input signal.

EMIOS_CCNTR*n* is stable only outside the time window defined from A1 to B1 matches, otherwise its contents reflects a count in progress and not the final value. Alternatively to EMIOS_CCNTR*n*, register A2 returns the latest available measurement. Because this register is updated only at comparator B matches, it always contains stable and up-to-date data. In WPTA mode this register is accessible through the alternate register address EMIOS_ALTA*n*.

NOTE

The FORCMA and FORCMB bits have no effect when the unified channel is configured for WPTA mode.

Figure 17-31 shows how the unified channel can be used to accumulate high time.



Notes: [1] After input filter.
[2] Writing EMIOS_CADR*n* writes to A1.
[3] Writing EMIOS_CBDR*n* writes to B1.
[4] Reading EMIOS_ALTA*n* returns the value of A2. (EMIOS_ALTA only used in PEC and WPTA modes)

Figure 17-31. Windowed Programmable Time Accumulation Example

17.4.4.4.11 Modulus Counter Mode (MC)

The following table lists the modulus counter settings:

Table 17-23. Modulus Counter Operating Modes

MODE[0:6]	Unified Channel MC Operating Mode
0b0010000	Modulus counter. Up counter, internal clock source.
0b0010001	Modulus counter. Up counter, external clock source.
0b0010010–0b0010011	Reserved
0b0010100	Modulus counter. Up/down counter, no change in counter direction upon match of input counter and register B1, internal clock source.
0b0010101	Modulus counter. Up/down counter, no change in counter direction upon match of input counter and register B1, external clock source.

Table 17-23. Modulus Counter Operating Modes (continued)

MODE[0:6]	Unified Channel MC Operating Mode
0b0010110	Modulus counter. Up/down counter, change in counter direction upon match of input counter and register B1 and sets the FLAG, internal clock source.
0b0010111	Modulus counter. Up/down counter, change in counter direction upon match of input counter and register B1 and sets the FLAG, external clock source.

The MC mode can provide a time base for a counter bus or a general purpose timer.

MODE[6] bit selects internal or external clock source when cleared or set, respectively. When external clock is selected, the input signal pin is used as the source and the triggering polarity edge is selected by the EDPOL and EDSEL in the EMIOS_CCR*n*.

When software selects the modulus counter mode, the internal counter is initially reset to 0. The internal counter counts up from the current value until it matches the value in register A1. Register B1 is cleared and is not accessible to the MCU. MODE[4] bit selects up mode or up/down mode, when cleared or set, respectively.

When in up count mode, a match between the internal counter and register A1 sets the FLAG and clears the internal counter.

When in up/down count mode, a match between the internal counter and register A1 sets the FLAG and changes the counter direction from increment to decrement. A match between register B1 and the internal counter changes the counter direction from decrement to increment and sets the FLAG only if MODE[5] bit is set.

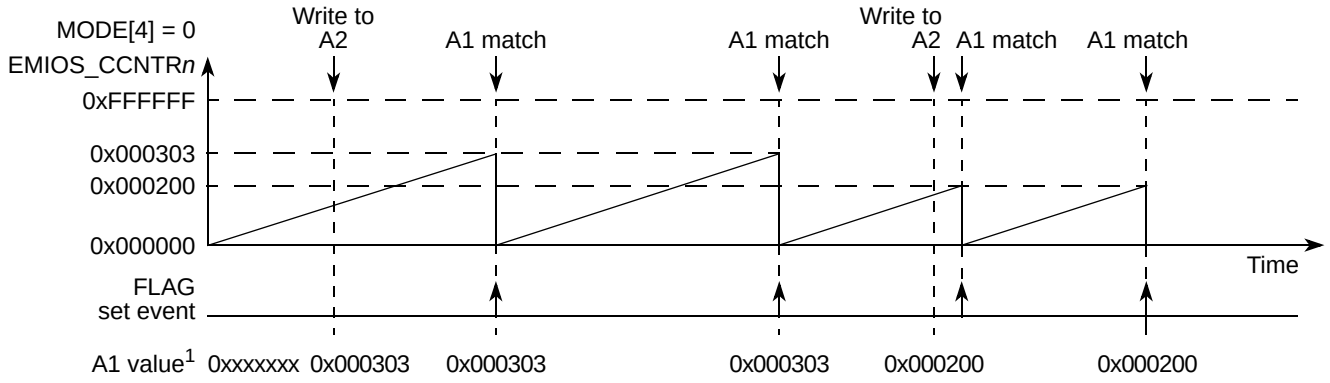
NOTE

The FORCMA and FORCMB bits have no effect when the unified channel is configured for MC mode.

NOTE

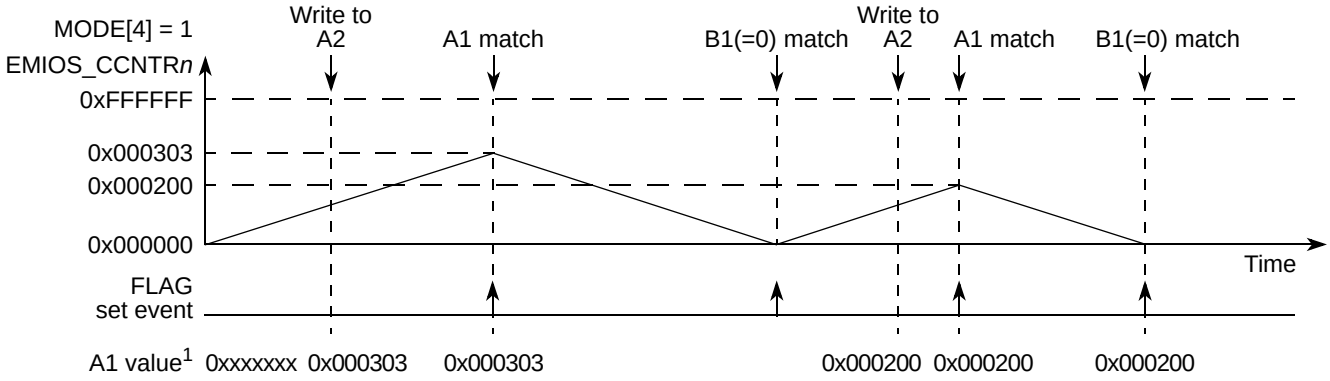
Any update to the A register takes place immediately, regardless of the current state of the counter and whether the counter is in up mode, or up/down mode.

Figure 17-32 and Figure 17-33 shows how to use the unified channel as a modulus counter in up mode and up/down mode, respectively.



Notes: [1] Writing EMIOS_A*n* writes to A2.
A2 value transferred to A1 according to OU*n* bit.

Figure 17-32. Modulus Counter Up Mode Example



Notes: [1] Writing EMIOS_A*n* writes to A2.
A2 value transferred to A1 according to OU*n* bit.

Figure 17-33. Modulus Counter Up/Down Mode Example

17.4.4.4.12 Output Pulse-Width and Frequency Modulation Mode (OPWFM)

The following table lists the output pulse-width and frequency modulation mode settings:

Table 17-24. OPWFM Operating Mode

MODE[0:6]	Unified Channel OPWFM Operating Mode
0b0011000	Output pulse-width and frequency modulation. FLAG set at match of internal counter and comparator B, immediate update.
0b0011001	Output pulse-width and frequency modulation. FLAG set at match of internal counter and comparator B, next period update.
0b0011010	Output pulse-width and frequency modulation. FLAG set at match of internal counter and comparator A or comparator B, immediate update.
0b0011011	Output pulse-width and frequency modulation. FLAG set at match of internal counter and comparator A or comparator B, next period update.

In this mode, the duty cycle is (register A1 + 1) and the period is (register B1 + 1). The MODE[6] bit controls the transfer from register B2 to B1, which can be done either immediately (MODE[6] cleared), providing the fastest change in the duty cycle, or at every match of register A1 (MODE[6] set).

The internal counter is automatically selected as a time base, therefore the BSL[0:1] bits in register EMIOS_CCR*n* have no meaning. The output flip-flop's active state is the complement of EDPOL bit. The output flip-flop is active during the duty cycle (from the start of the cycle until a match occurs in comparator A). After the match in comparator A the output flip-flop is in the inactive state (the value of EDPOL) until the next cycle starts. When a match on comparator A occurs, the output flip-flop is set to the value of the EDPOL bit. When a match occurs on comparator B, the output flip-flop is set to the complement of the EDPOL bit and the internal counter is cleared.

FLAG can be generated at match B, when MODE[5] is cleared, or in both matches, when MODE[5] is set.

At any time, the FORCMA and FORCMB bits allow the software to force the output flip-flop to the level corresponding to a match on A or B respectively. Also, FORCMB clears the internal counter. The FLAG bit is not set by the FORCMA or FORCMB operations.

If subsequent comparisons occur on comparators A and B, the PWFM pulses continue to be output, regardless of the state of the FLAG bit.

To achieve 0% duty cycle, both registers A1 and B1 must be set to the same value. When a simultaneous match occurs on comparators A and B, the output flip-flop is set at every period to the value of EDPOL bit.

To temporarily change from the current duty cycle to 0% and then return to the current duty cycle, the sequence is the following:

1. If not currently stored, store value of register A.
2. Set A=B.
3. If immediate 0% duty cycle is desired, set FORCA=1.
4. To return to the previous duty cycle, restore register A with its former value.

100% duty cycle is possible by writing 0x000000 to register A. When a match occurs, the output flip-flop is set at every period to the complement of EDPOL bit. The transfer from register B2 to B1 is still controlled by MODE[6] bit.

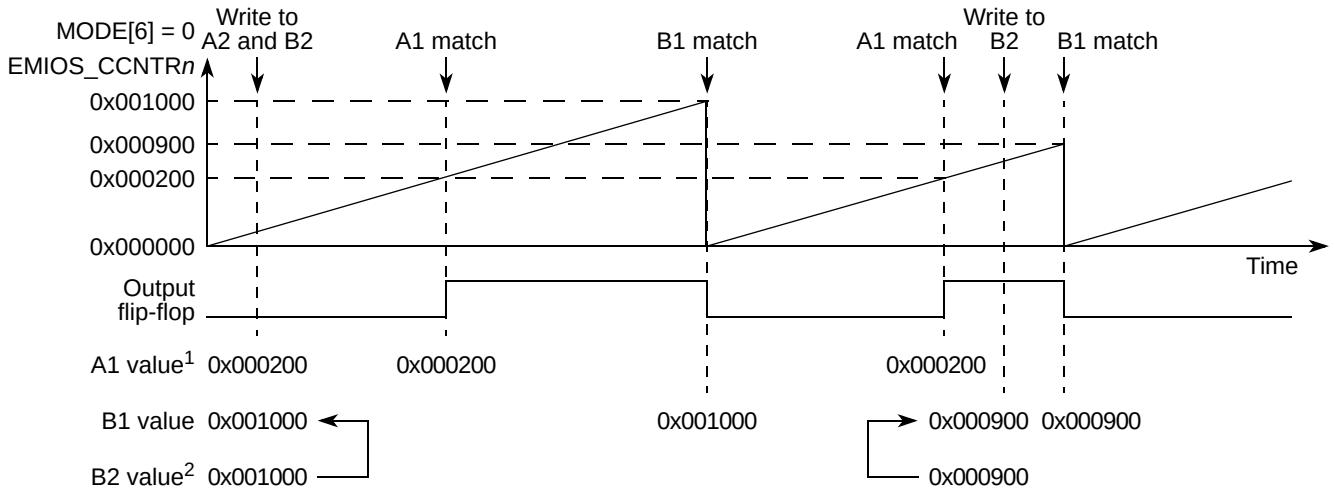
To temporarily change from the current duty cycle to 100% and then return to the current duty cycle, the sequence is the following:

1. If not currently stored, store value of register A.
2. Set A=0.
3. If immediate 100% duty cycle is desired, set FORCB=1.
4. To return to the previous duty cycle, restore register A with its former value.

NOTE

Updates to the A register always occur immediately. If next period update is selected via the mode[6] bit, only the B register update is delayed until the next period.

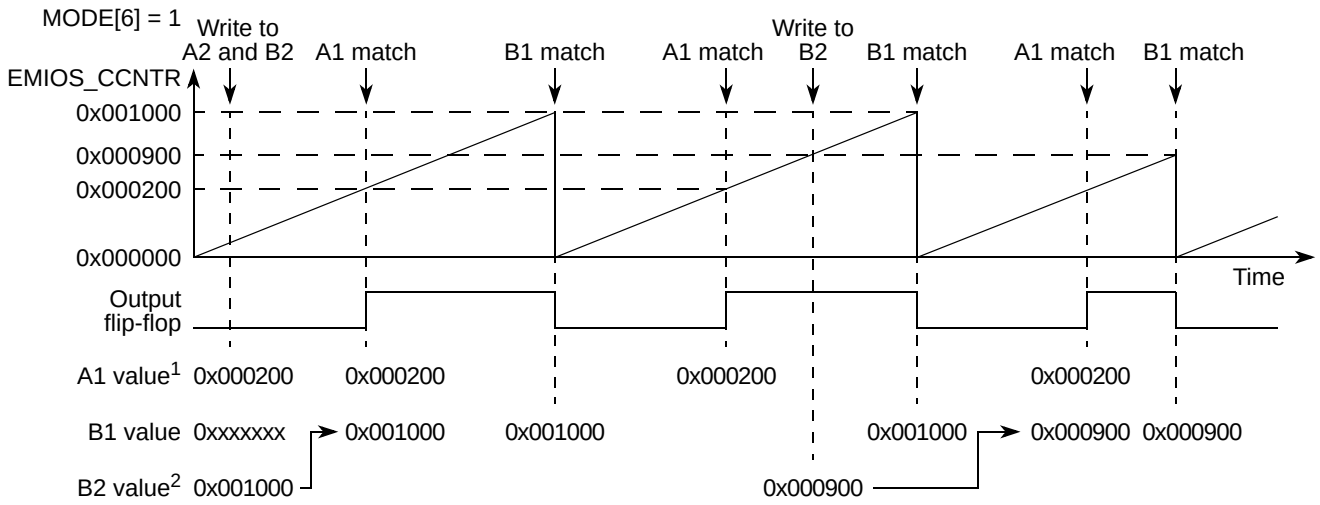
Figure 17-34 shows the unified channel running in OPFWM mode with immediate register update.



Notes: [1] Writing EMIOS_A*n* writes to A2.
[2] Writing EMIOS_B*n* writes to B2.
A2 value transferred to A1 according to OU*n* bit.
B2 value transferred to B1 according to OU*n* bit.

Figure 17-34. OPWFM with Immediate Update

Figure 17-35 shows the unified channel running in OPFWM mode with next period update PFWM mode. In both figures EDPOL = 1, so the output is low during the duty cycle.



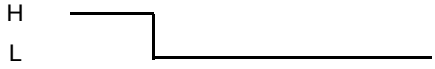
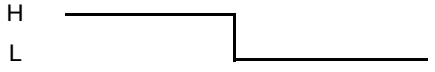
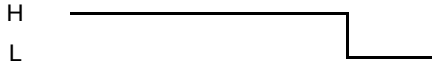
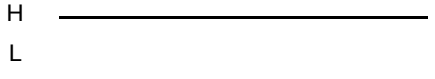
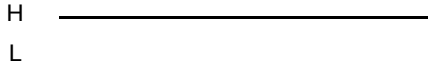
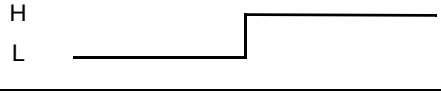
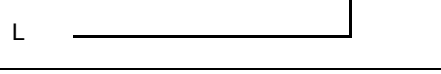
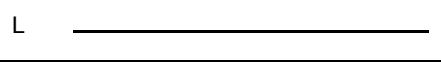
Notes: [1] Writing EMIOS_A*n* writes to A2.
[2] Writing EMIOS_B*n* writes to B2.

A2 value transferred to A1 according to OU*n* bit.
B2 value transferred to B1 according to OU*n* bit.

Figure 17-35. OPWFM with Next Period Update

Table 17-25 has additional illustrative examples.

Table 17-25. Examples of Output Waveforms

EDPOL	Duty Cycle	A (decimal)	B (decimal)	Waveform
0 Active high output	0%	1000	1000	
	25%	250	1000	
	50%	500	1000	
	75%	750	1000	
	100%	0	1000	
1 Active low output	0%	1000	1000	
	25%	250	1000	
	50%	500	1000	
	75%	750	1000	
	100%	0	1000	

17.4.4.4.13 Center-Aligned Output Pulse-Width Modulation with Dead-time Mode (OPWMC)

The following table lists the center-aligned output pulse-width modulation with dead-time mode settings:

Table 17-26. OPWMC Operating Mode

MODE[0:6]	Unified Channel OPWMC Operating Mode
0b0011100	Center-aligned output pulse-width modulation. FLAG set in trailing edge, trailing edge dead-time.
0b0011101	Center-aligned output pulse-width modulation. FLAG set in trailing edge, leading-edge dead-time.
0b0011110	Center-aligned output pulse-width modulation. FLAG set in both edges, trailing edge dead-time.
0b0011111	Center-aligned output pulse-width modulation. FLAG set in both edges, leading edge dead-time.

This operating mode generates a center-aligned PWM with dead-time insertion in the leading- or trailing-edge.

The selected counter bus must be running an up/down time base, as shown in Figure 17-33. BSL[0:1] bits select the time base. Register A1 contains the ideal duty cycle for the PWM signal and is compared with the selected time base. Register B1 contains the dead time value and is compared with the internal counter. For a leading edge dead time insertion, the output PWM duty cycle is equal to the difference between register A1 and register B1, and for a trailing edge dead time insertion, the output PWM duty cycle is equal to the sum of register A1 and register B1. MODE[6] bit selects between trailing and leading dead time insertion, respectively.

NOTE

Synchronize the internal prescaler of the OPWMCB channel with the MCB channel prescaler and set them to the same value. This allows the A1 and B1 registers to represent the same time scale for duty cycle and dead time insertion.

When operating with leading edge dead time insertion, the first match between A1 and the selected time base clears the internal counter and switches the selected time base to the internal counter. When a match occurs between register B1 and the selected time base, the output flip-flop is set to the value of the EDPOL bit and the time base is switched to the selected counter bus. In the next match between register A1 and the selected time base, the output flip-flop is set to the complement of the EDPOL bit. This sequence repeats continuously.

When operating with trailing edge dead time insertion, the first match between A1 and the selected time base sets the output flip-flop to the value of the EDPOL bit. In the next match between register A1 and the selected time base, the internal counter is cleared and the selected time base is switched to the internal counter. When a match occurs between register B1 and the selected time base, the output flip-flop is set to the complement of the EDPOL bit and the time base is switched to the selected counter bus. This sequence repeats continuously.

FLAG can be generated in the trailing edge of the output PWM signal when MODE[5] is cleared, or in both edges, when MODE[5] is set.

At any time, the FORCMA or FORCMB bits are equivalent to a successful comparison on comparator A or B with the exception that the FLAG bit is not set.

NOTE

When in freeze mode, the FORCMA or FORCMB bits only allow the software to force the output flip-flop to the level corresponding of a match on A or B respectively.

If subsequent matches occur on comparators A and B, the PWM pulses continue to be generated, regardless of the state of the FLAG bit.

To achieve a duty cycle of 100%, both registers A1 and B1 must be set to the same value. When a simultaneous match occurs between the selected time base and registers A1 and B1, the output flip-flop is set at every period to the value of EDPOL bit and the selected time base switches to the selected counter bus, allowing a new cycle to begin at any time, as previously described. 0% duty cycle is possible by writing 0x000000 to register A. When a match occurs, the output flip-flop is set at every period to the complement of EDPOL bit and the selected time base switches to the selected counter bus, allowing a new cycle to begin at any time, as previously described. In both cases, FLAG is generated regardless of MODE[5] bit.

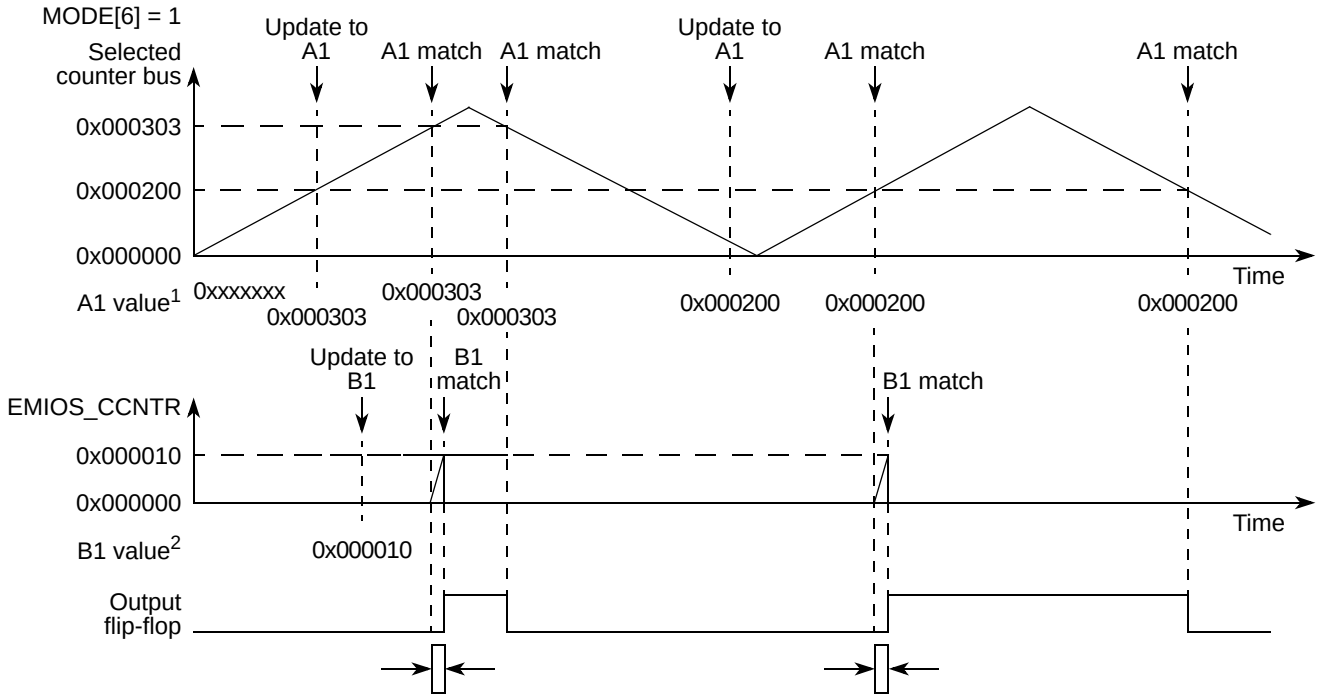
NOTE

If A1 and B1 are set to the 0x000000, a 0% duty cycle waveform is produced.

NOTE

Any updates to the A or B register takes place immediately.

Figure 17-36 and Figure 17-37 show the unified channel running in OPWMC with leading and trailing dead-time, respectively.

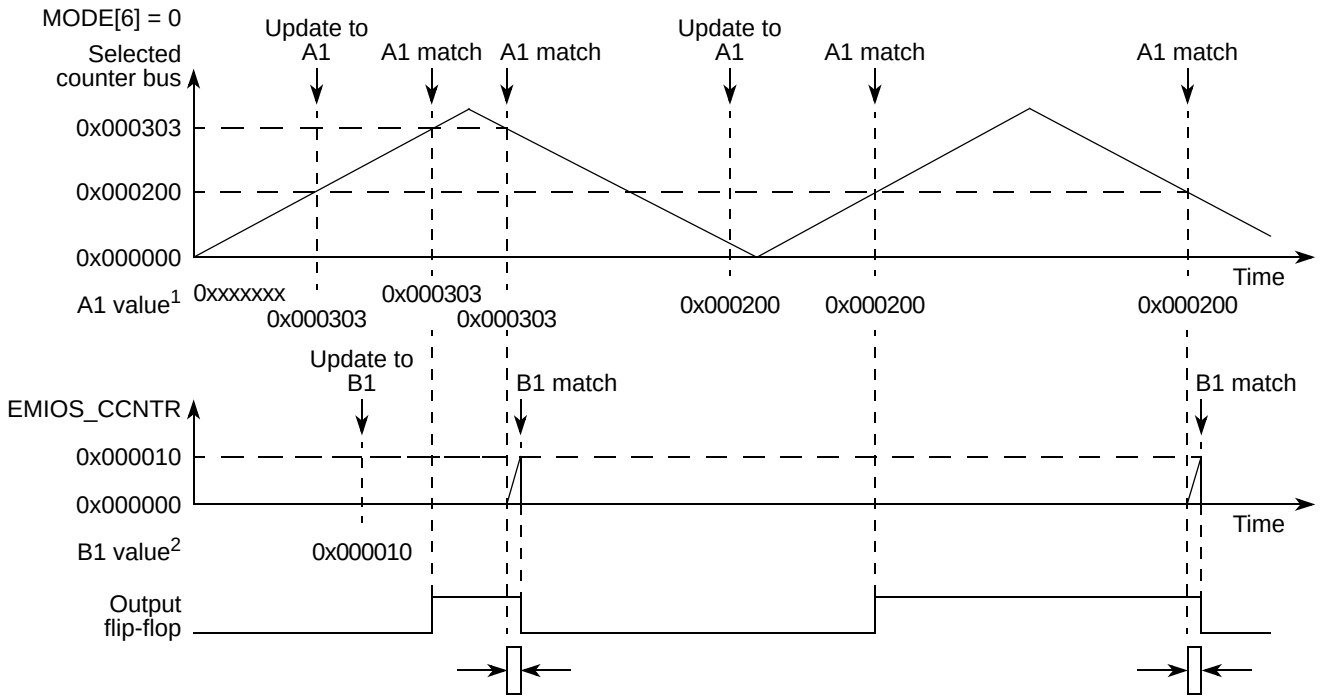


Notes: [1] Writing EMIOS_A*n* writes to A1.
[2] Writing EMIOS_B*n* writes to B1.

A2 value transferred to A1 according to OU*n* bit.
B2 value transferred to B1 according to OU*n* bit.

Figure 17-36. Output PWMC with Leading Dead-time Insertion

Figure 17-37 shows the unified channel in OPWMC with trailing dead-time.



Notes: [1] Writing EMIOS_A*n* writes to A2.
[2] Writing EMIOS_B*n* writes to B1.

A2 value transferred to A1 according to OU*n* bit.
B2 value transferred to B1 according to OU*n* bit.

Figure 17-37. Output PWMC with Trailing Dead-time Insertion

17.4.4.4.14 Output Pulse-Width Modulation Mode (OPWM)

The following table lists the output width modulation mode settings:

Table 17-27. OPWM Operating Modes

MODE[0:6]	Unified Channel OPWM Operating Mode
0b0100000	Output pulse-width modulation. FLAG set at match of internal counter and comparator B, immediate update.
0b0100001	Output pulse-width modulation. FLAG set at match of internal counter and comparator B, next period update.
0b0100010	Output pulse-width modulation. FLAG set at match of internal counter and comparator A or comparator B, immediate update.
0b0100011	Output pulse-width modulation. FLAG set at match of internal counter and comparator A or comparator B, next period update.

Registers A1 and B1 define the leading and trailing edges of the PWM output pulse, respectively. MODE[6] bit controls the transfer from register B2 to B1, which can be done either immediately (MODE[6] cleared), providing the fastest change in the duty cycle, or at every match of register A1 (MODE[6] set).

The value loaded in register A1 is compared with the value on the selected time base. When a match on comparator A occurs, the output flip-flop is set to the value of the EDPOL bit. When a match occurs on comparator B, the output flip-flop is set to the complement of the EDPOL bit.

FLAG can be generated at match B, when MODE[5] is cleared, or in both matches, when MODE[5] is set.

At any time, the FORCMA and FORCMB bits allow the software to force the output flip-flop to the level corresponding to a match on A or B respectively. The FLAG bit is not set by the FORCMA and FORCMB operations.

If subsequent matches occur on comparators A and B, the PWM pulses continue to be generated, regardless of the state of the FLAG bit.

To achieve 0% duty cycle, both registers A1 and B1 must be set to the same value. When a simultaneous match on comparators A and B occur, the output flip-flop is set at every period to the value of EDPOL bit. 0% duty cycle is possible by writing 0x000000 to register A. When a match occurs, the output flip-flop is set at every period to the complement of EDPOL bit. The transfer from register B2 to B1 is still controlled by MODE[6] bit.

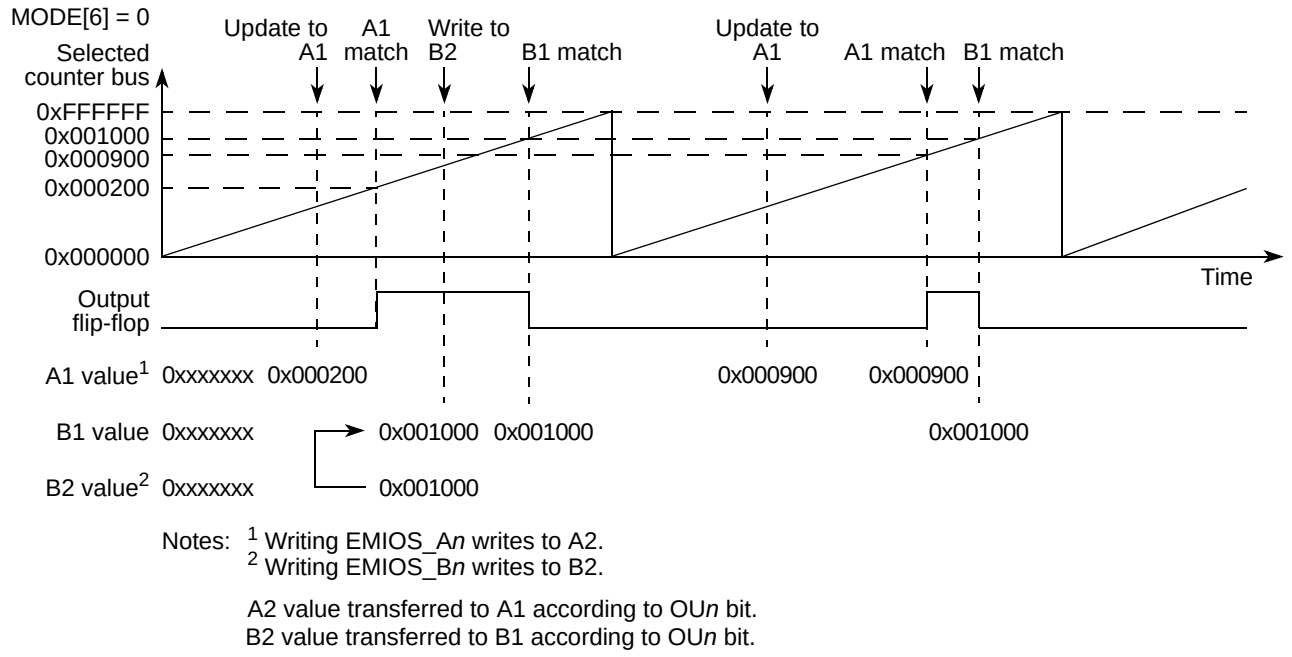
NOTE

If A1 and B1 are set to the 0x000000, a 100% duty cycle waveform is produced.

NOTE

Updates to the A register always occur immediately. If next period update is selected via the mode[6] bit, only the B register update is delayed until the next period.

Figure 17-38 and Figure 17-39 show the unified channel running in OPWM with immediate update and next period update, respectively.

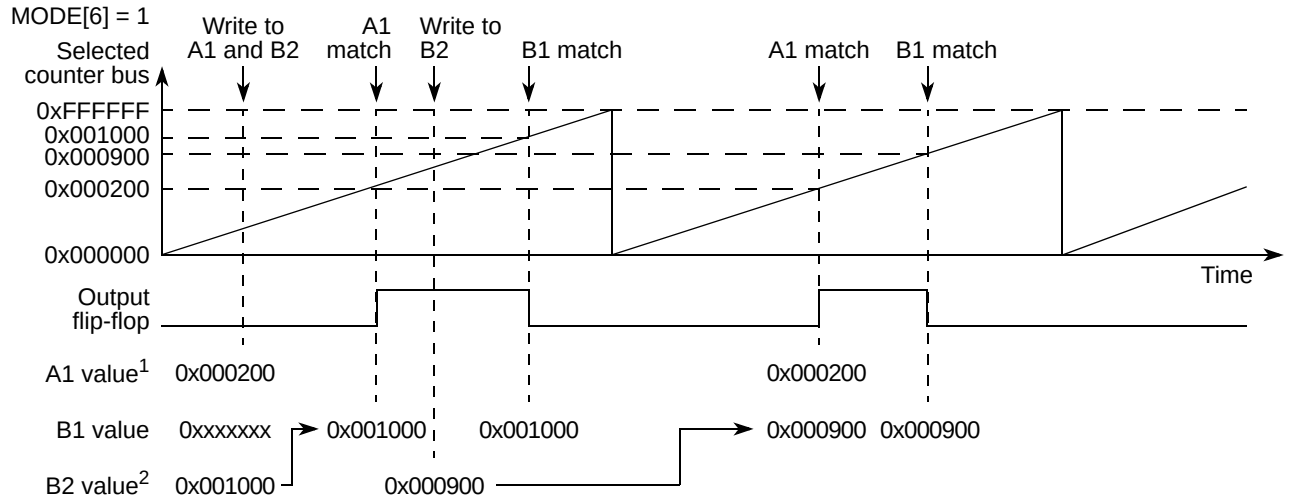


Notes: [1] Writing EMIOS_A*n* writes to A2.
[2] Writing EMIOS_B*n* writes to B2.

A2 value transferred to A1 according to OU*n* bit.
B2 value transferred to B1 according to OU*n* bit.

Figure 17-38. Output PWM with Immediate Update

Figure 17-39 show the unified channel running in OPWM with immediate update and next period update, respectively.



Notes: [1] Writing EMIOS_A*n* writes to A2.
[2] Writing EMIOS_B*n* writes to B2.

A2 value transferred to A1 according to OU*n* bit.
B2 value transferred to B1 according to OU*n* bit.

Figure 17-39. Output PWM with Next Period Update

17.4.4.4.15 Modulus Counter Buffered Mode (MCB)

The following table lists the modulus counter buffered mode settings:

Table 17-28. MCB Operating Modes

MODE[0:6]	Unified Channel MCB Operating Mode
0b1010000	Modulus up counter, buffered, internal clock
0b1010001	Modulus up counter, buffered, external clock
0b1010010–0b1010001	Reserved
0b1010100	Modulus up/down counter, buffered. FLAG set on one event, internal clock.
0b1010101	Modulus up/down counter, buffered. FLAG set on one event, external clock.
0b1010110	Modulus up/down counter, buffered. FLAG set on both events, internal clock.
0b1010111	Modulus up/down counter, buffered. FLAG set on both events, external clock.

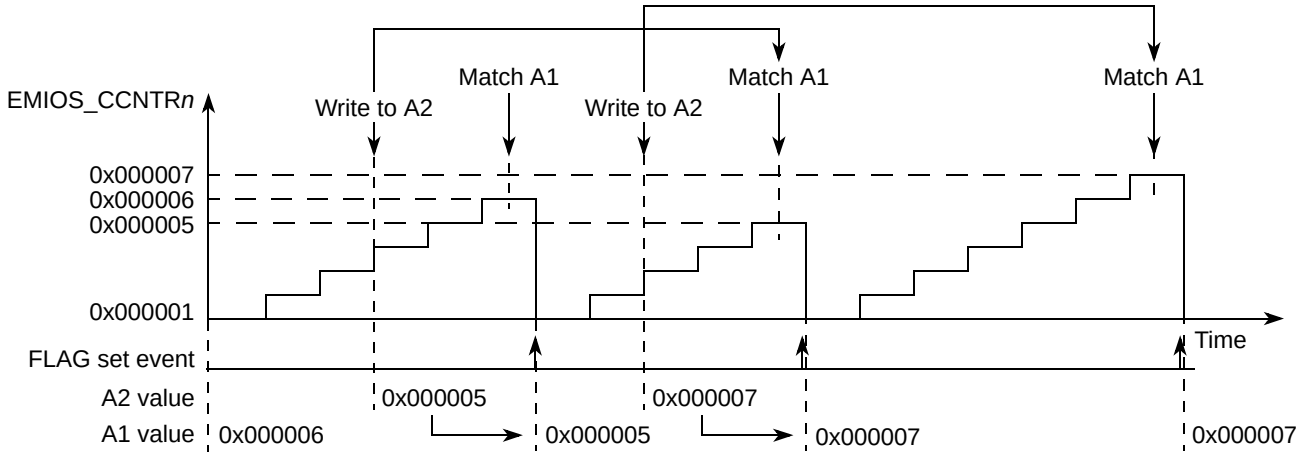
The MCB mode provides a time base which can be shared with other channels through the internal counter buses. Register A1 is double buffered, thus allowing smooth transitions between cycles when changing the A2 register value asynchronously. The A1 register is updated at the cycle boundary, which is defined as when the internal counter reaches the value one. The internal counter values are within a range from one up to register A1 value in MCB mode.

The MODE[6] bit selects the internal clock source if clear or external if set. When an external clock is selected, the channel input pin is used as the channel clock source. The active edge of this clock is defined by EDPOL and EDSEL bits in the EMIOS_CCR channel register.

When entering the MCB mode, if up counter is selected (MODE[4] = 0), the internal counter starts counting up from its current value to until an A1 match occurs. On the next system clock cycle after an A1 match occurs, the internal counter is set to one and the counter continues counting up. If up/down mode is selected (MODE[4] = 1), the counter changes direction at the A1 match and counts down until it reaches one and is then set to count up again. In this mode B1 is set to one and cannot be changed, as it is used to generate a match to switch from down count to up count.

The MCB mode counts between one and the A1 register value. The counter cycle period in up count mode is equal to the A1 value. In up/down counter mode the period is defined by the formula: $(2 \times A1) - 2$.

Figure 17-40 illustrates the counter cycle for several A1 values. Register A1 is loaded with the A2 value at the cycle boundary. Thus any value written to A2 within cycle (*n*) is updated to A1 at the next cycle boundary, and therefore is used on cycle (*n*+1). The cycle boundary between cycle (*n*) and cycle (*n*+1) is defined as the first clock cycle of cycle (*n*+1). Flags are set when A1 matches occur.

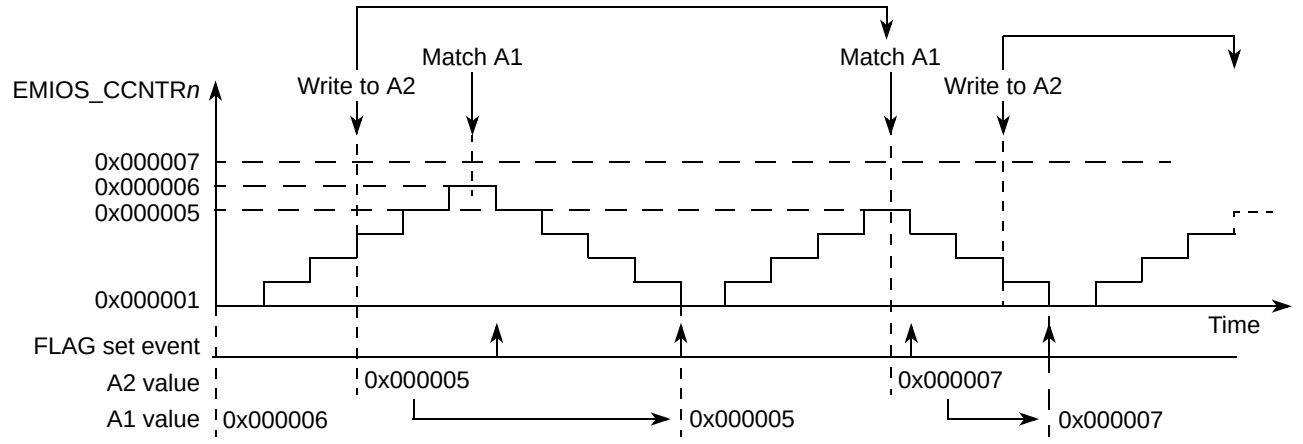


Note: A2 value transferred to A1 according to OU*n* bit.

Figure 17-40. eMIOS MCB Mode Example — Up Operation

Figure 17-41 illustrates the MCB up/down counter mode. The A1 register is updated at the cycle boundary. If A2 is written in cycle (*n*), this new value is used in cycle (*n*+1) for the next A1 match.

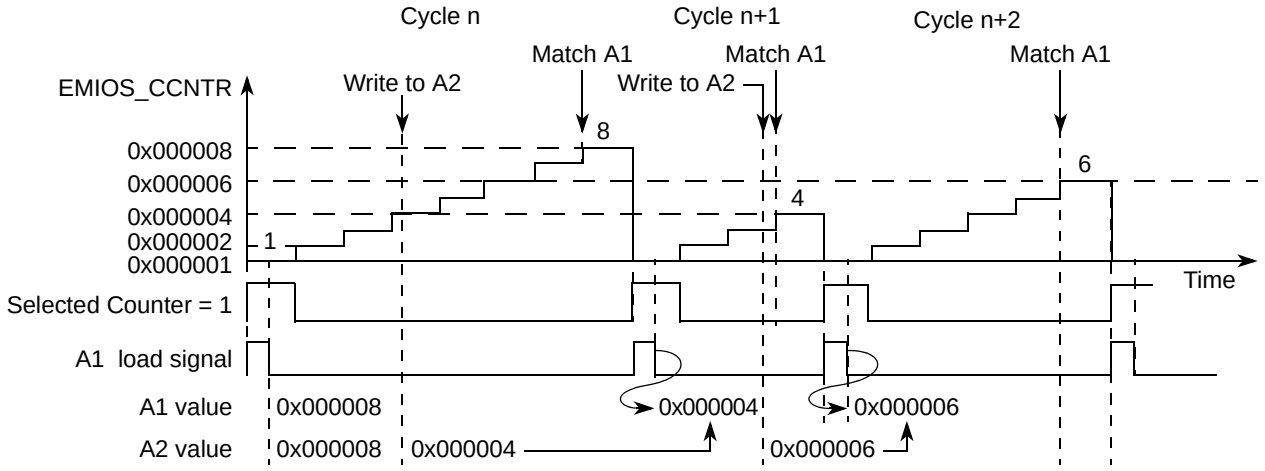
Flags are generated only at an A1 match if MODE[5] is 0. If MODE[5] is 1, flags are also generated at the cycle boundary.



Note: A2 value transferred to A1 according to OU*n* bit.

Figure 17-41. eMIOS MCB Mode Example — Up/Down Operation

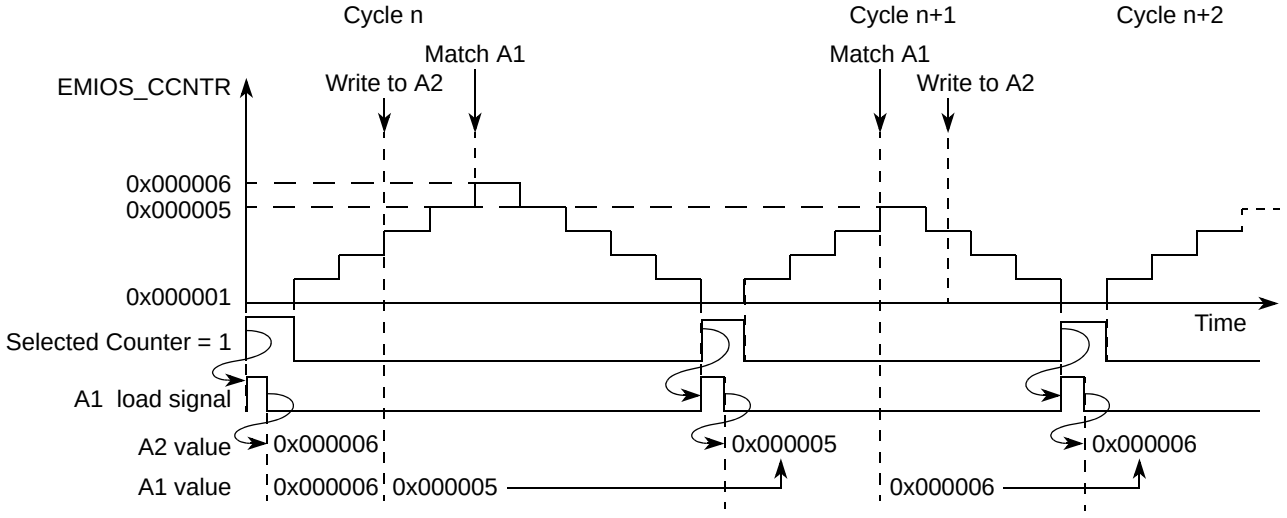
Figure 17-42 provides a more detailed illustration of the A1 update process in up counter mode. The A1 load signal is generated based on the detection of the internal counter reaching one, and has the duration of one system clock cycle. During the load pulse A1 still holds its previous value. It is actually updated at the second system clock cycle.



Note: A2 value transferred to A1 according to OU*n* bit.

Figure 17-42. eMIOS MCB Mode Example — Up Operation A1 Register Update

Figure 17-43 illustrates the A1 register update process in up/down counter mode. A2 can be written at any time within cycle (*n*) to be used in cycle (*n*+1). Thus, A1 receives the new value at the next cycle boundary. The EMIOS_OUDR[n] bits can be used to disable the update of A1 register.



Note: A2 value transferred to A1 according to OU*n* bit (the transfer is triggered by the A1 load signal).

Figure 17-43. eMIOS MCB Mode Example — Up/Down Operation A1 Register Update

17.4.4.4.16 Output Pulse-Width and Frequency Modulation Buffered Mode (OPWFMB)

The following table lists the output pulse-width and frequency modulation buffered mode settings:

Table 17-29. OPWFMB Operating Modes

MODE[0:6]	Unified Channel OPWFM Operating Mode
0b1011000	Output pulse-width and frequency modulation, buffered. FLAG set at match of internal counter and comparator B.
0b1011001	Reserved
0b1011010	Output pulse-width and frequency modulation, buffered. FLAG set at match of internal counter and comparator A or comparator B.

This mode generates waveforms with variable duty cycle and frequency. The internal channel counter is automatically selected as the time base, A1 sets the duty cycle and B1 determines the frequency. Both A1 and B1 are double buffered to allow smooth signal generation when changing the register values asynchronously. Both 0% and 100% duty cycles are supported.

To provide smooth and consistent channel operation, this mode differs substantially from the OPWFM mode. The main differences are in how A1 and B1 are updated, the delay from the A1 match to the output flip-flop transition, and the range of the internal counter which ranges from 1 up to B1 value.

When a match on comparator A occurs, the output register is set to the value of EDPOL. When a match on comparator B occurs, the output register is set to the complement of EDPOL. A B1 match also causes the internal counter to transition to 1, thus re-starting the counter cycle.

Figure 17-44 shows an example of OPWFMB mode operation. The output flip-flop transition occurs when the A1 or B1 match signal is negated, as detected by the negative edge of the A1 and B1 match signals. For example, if register A1 is set to 0x000004, the output flip-flop transitions 4 counter periods after the cycle starts, plus one system clock cycle. In the example shown in Figure 17-44 the prescaler ratio is set to two (refer to Section 17.5.3, “Time Base Generation).

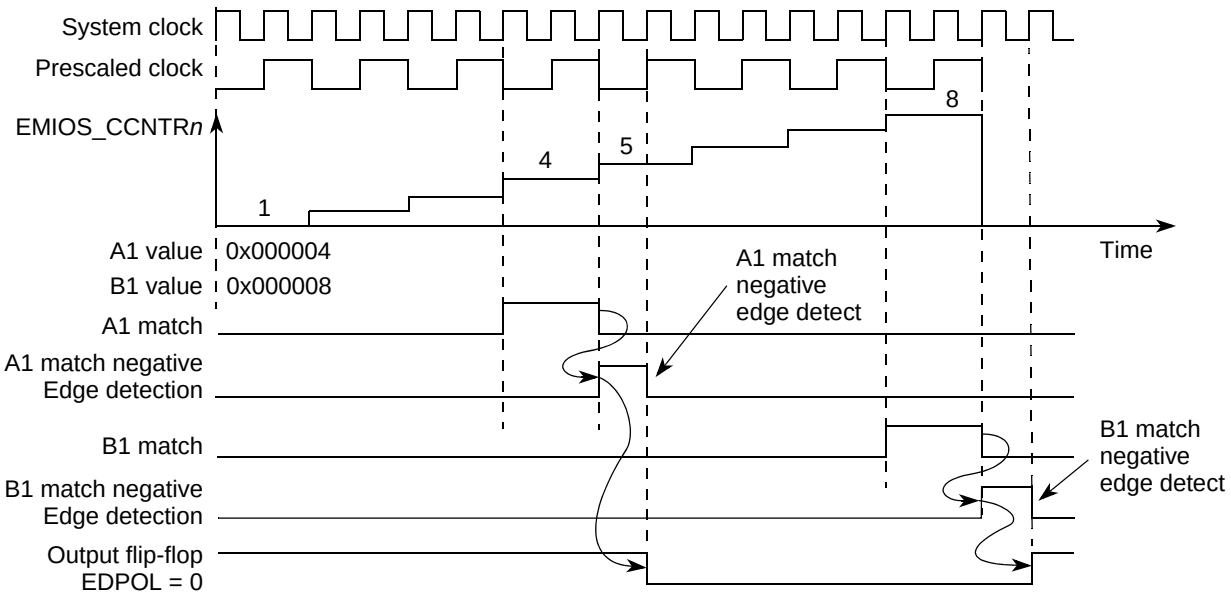


Figure 17-44. eMIOS OPWFMB Mode Example — A1/B1 Match to Output Register Delay

Figure 17-45 shows the generated output signal if A1 is 0. Since the counter does not reach zero in this mode, the channel internal logic infers a match as if A1 = 1, with the difference that in this case the positive edge of the match signal is used to trigger the output flip-flop transition instead of the positive edge that is used when A1 = 1. The A1 positive edge match signal from cycle (*n*+1) occurs at the same time as the B1 match negative edge from cycle (*n*). This allows the use of the A1 match positive edge to mask the B1 match negative edge when they occur at the same time. The result is that no transition occurs on the output flip-flop, and a 0% duty cycle is generated.

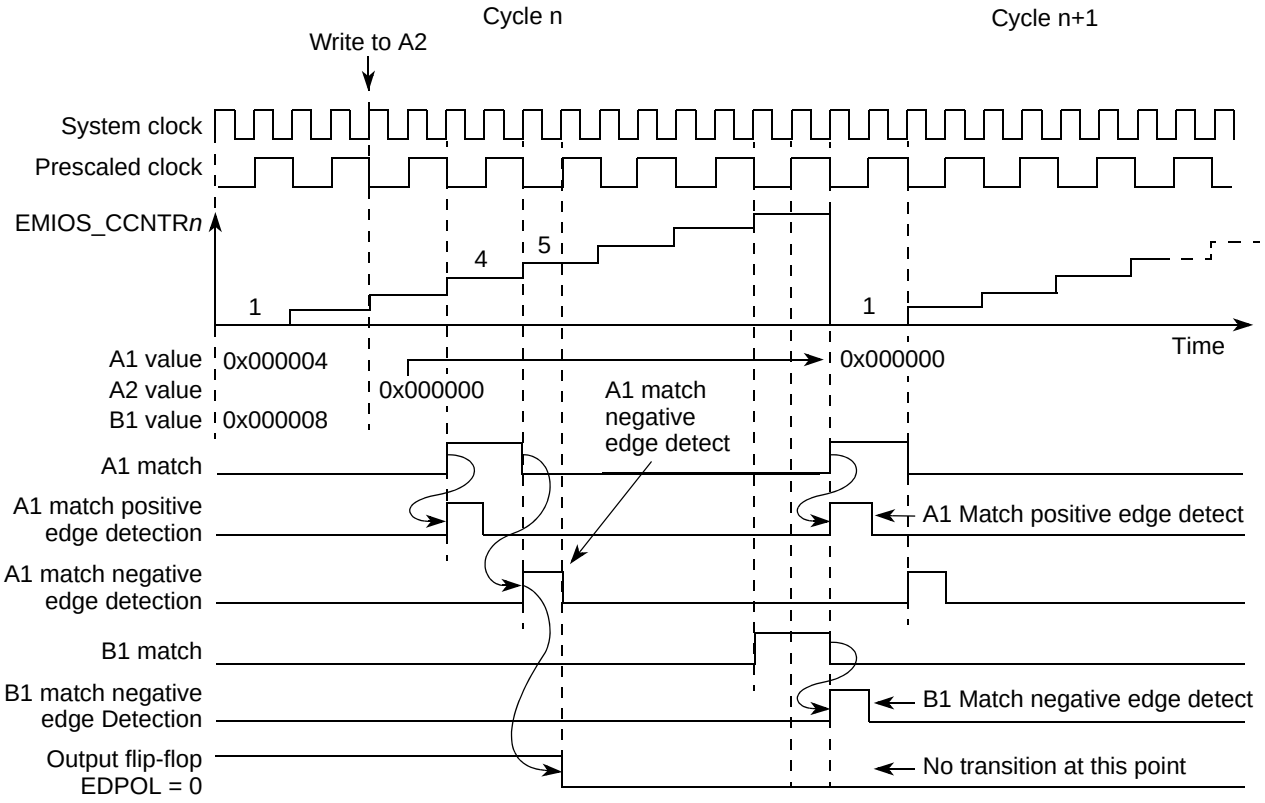


Figure 17-45. eMIOS OPWFMB Mode Example — A1 = 0 (0% Duty Cycle)

Figure 17-46 shows the timing for the A1 and B1 loading. A1 and B1 use the same signal to trigger a load, which is generated based on the selected counter reaching one. This event is defined as the cycle boundary. The load signal pulse has the duration of one system clock cycle and occurs at the first system clock period of every cycle of the counter. If A2 and B2 are written within cycle (*n*), their values are loaded into A1 and B1, respectively, at the first clock of cycle (*n*+1). The update disable bits, EMIOS_OUDR, can be used to control the update of these registers, thus allowing the delay of A1 and B1 update for synchronization purposes.

During the load pulse A1 still holds its old value, which is updated on the following system clock cycle. During the A1 load pulse, an internal by-pass allows the use of A2 instead of A1 for matches if A2 is either 0 or 1, thus allowing matches to be generated even when A1 is being loaded. This approach allows a uniform channel operation for any A2 value, including 1 and 0.

In Figure 17-46 it is assumed that the channel and global prescalers are set to one, meaning that the channel internal counter transition at every system clock cycle. FLAGs can be generated only on B1 matches when MODE[5] is cleared, or on both A1 and B1 matches when MODE[5] is set. Since B1 FLAG occurs at the cycle boundary, this flag can be used to indicate that A2 or B2 data written on cycle (*n*) were loaded to A1 or B1, respectively, thus generating matches in cycle (*n*+1).

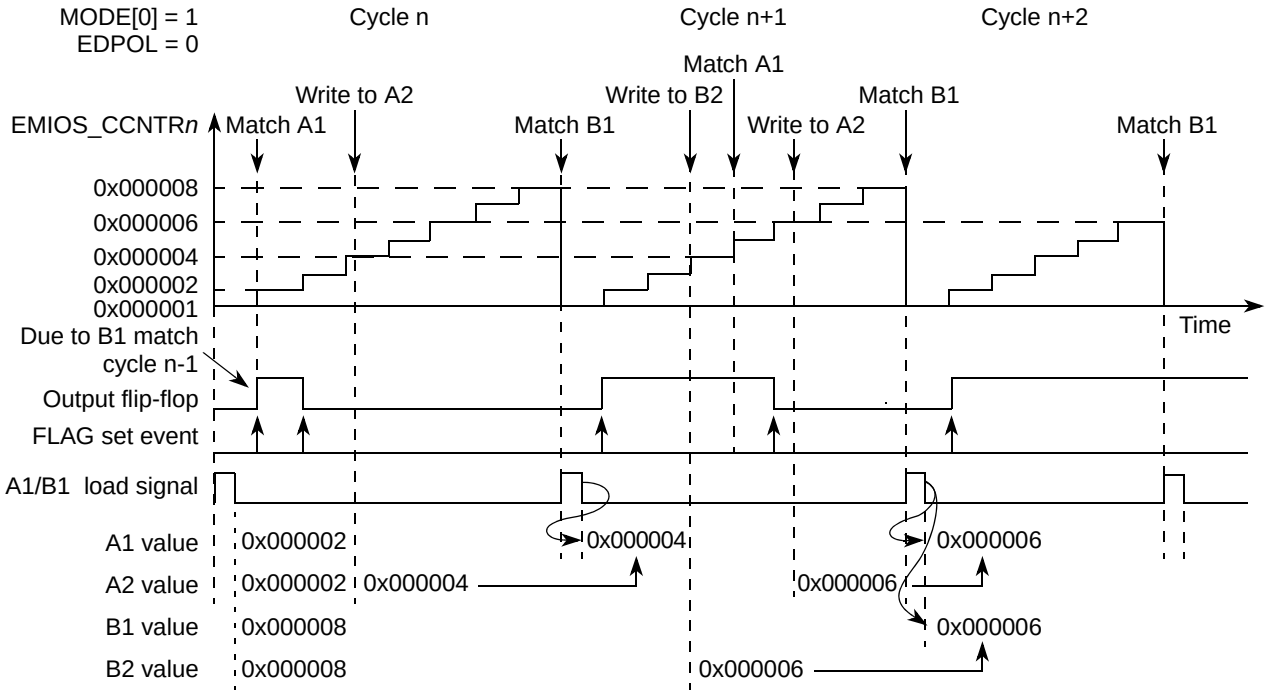


Figure 17-46. eMIOS OPWFMB Mode Example — A1/B1 Updates and Flags

Figure 17-47 shows the operation of the output disable feature in OPWFMB mode. Unlike OPWFM mode, the output disable forces the channel output flip-flop to the EDPOL bit value. This functionality targets applications that use active high signals and a high to low transition at A1 match. For such cases, clear EDPOL to 0.

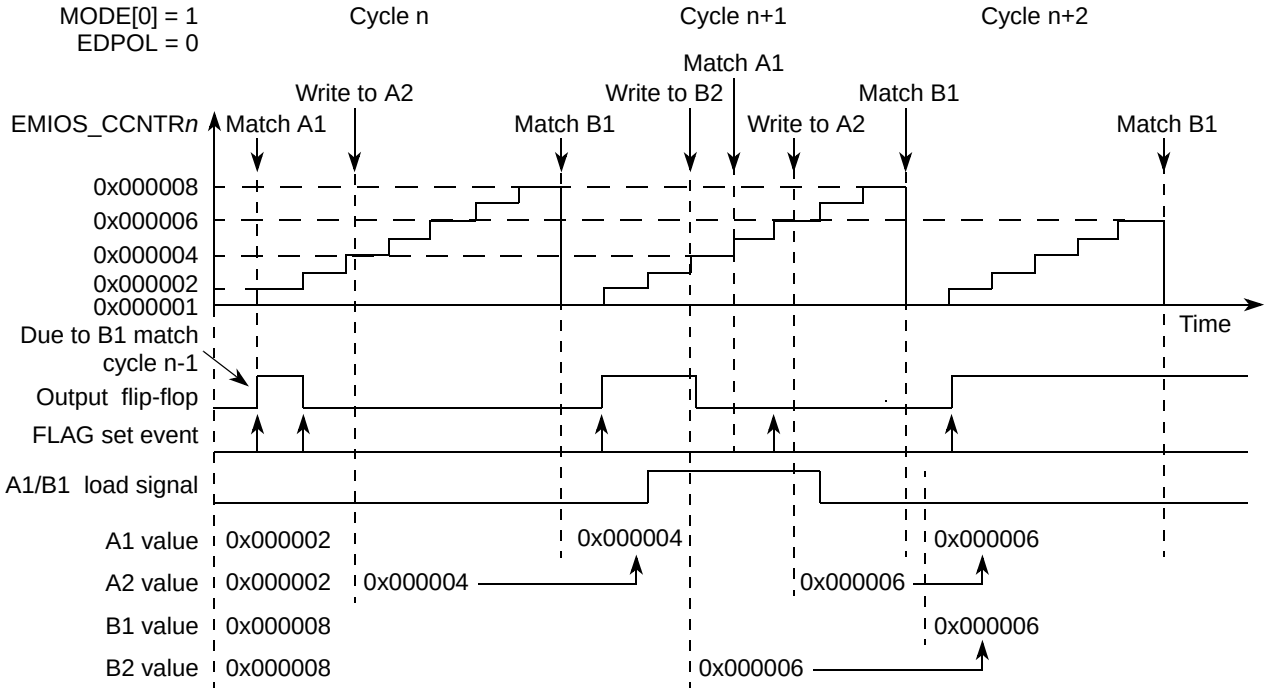


Figure 17-47. eMIOS OPWFMB Mode Example — Active Output Disable

The output disable has a synchronous operation, meaning that the assertion of the output disable input signal causes the channel output flip-flop to transition to EDPOL at the next system clock cycle. If the output disable input is negated, the output flip-flop transitions at the following A1 or B1 match.

In Figure 17-47 it is assumed that the output disable input is enabled and selected for the channel (refer to Section 17.3.1.7, “eMIOS Channel Control Register (EMIOS_CCRn),” for a detailed description of the ODIS and ODISSL bits and selection of the output disable inputs).

The FORCMA and FORCMB bits allow the software to force the output flip-flop to the level corresponding to a match on comparators A or B respectively. Similar to a B1 match, FORCMB clears the internal counter. The FLAG bit is not set when the FORCMA or FORCMB bits are set.

Figure 17-48 illustrates the generation of 100% and 0% duty cycle signals. It is assumed that EDPOL = 0 and the prescaler ratio is 1. Initially A1 = 0x000008 and B1 = 0x000008. In this case, a B1 match has precedence over an A1 match, thus the output flip-flop is set to the complement of EDPOL. This cycle corresponds to a 100% duty cycle signal. The same output signal can be generated for any A1 value greater than or equal to B1.

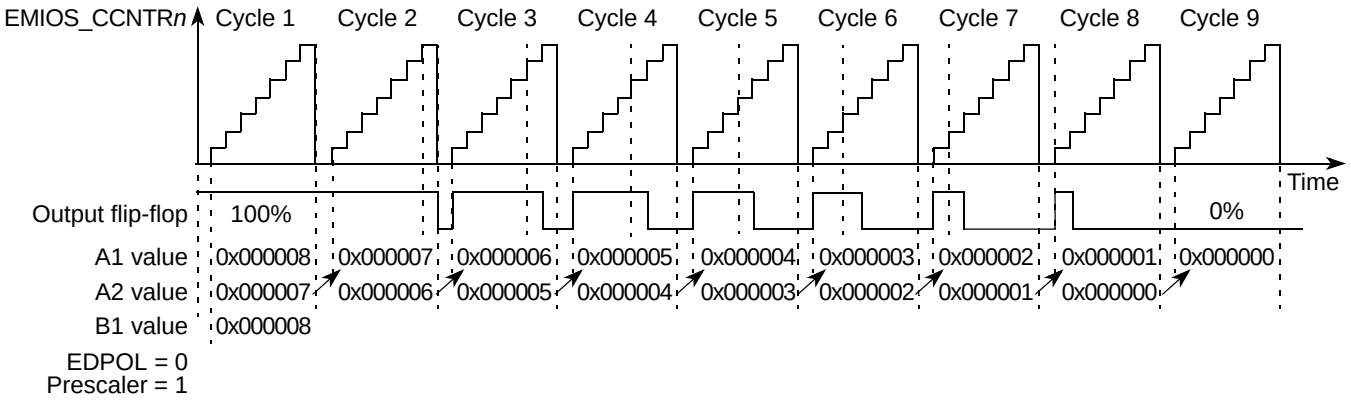


Figure 17-48. eMIOS OPWFMB Mode Example — 100% to 0% Duty Cycle

A 0% duty cycle signal is generated if A1 = 0 as shown in Figure 17-48 cycle 9. In this case the B1 = 0x000008 match from cycle 8 occurs at the same time as the A1 = 0x000000 match from cycle 9. Refer to Figure 17-45 for a description of A1 and B1 match generation for a case where A1 match has precedence over B1 match and the output signal transitions to EDPOL.

17.4.4.4.17 Center-Aligned Output Pulse-Width Modulation Buffered Mode (OPWMCB)

The following table lists the center-aligned output pulse-width modulation buffered mode settings:

Table 17-30. OPWMCB Operating Modes

MODE[0:6]	Unified Channel OPWMCB Operating Mode
0b1011100	Center-aligned output pulse-width modulation, buffered. FLAG set on trailing edge, trailing edge dead-time.
0b1011101	Center-aligned output pulse-width modulation, buffered. FLAG set on trailing edge, leading edge dead-time.
0b1011110	Center-aligned output pulse-width modulation, buffered. FLAG set on both edges, trailing edge dead-time.
0b1011111	Center-aligned output pulse-width modulation, buffered. FLAG set on both edges, leading edge dead-time.

This mode generates a center-aligned PWM with dead time insertion on the leading or trailing edge. A1 and B1 registers are double buffered to allow smooth output signal generation when changing A2 or B2 values asynchronously.

The selected counter bus for a channel configured to OPWMCB mode must be another channel running in MCB up/down counter mode (refer to Section 17.4.4.4.15, “Modulus Counter Buffered Mode (MCB)”). Register A1 contains the ideal duty cycle for the PWM signal and is compared with the selected time base. Register B1 contains the dead time value and is compared against the internal counter. For a leading edge

dead time insertion, the output PWM duty cycle is equal to the difference between register A1 and register B1, and for a trailing edge dead time insertion, the output PWM duty cycle is equal to the sum of register A1 and register B1. The MODE[6] bit selects between trailing and leading dead time insertion, respectively.

NOTE

Synchronize the internal prescaler of the OPWMCB channel with the MCB channel prescaler and set them to the same value. This allows the A1 and B1 registers to represent the same time scale for duty cycle and dead time insertion.

Figure 17-49 illustrates loading of the A1 and B1 registers, which occurs when the selected counter bus reaches the value one. This counter value defines the cycle boundary. Values written to A2 or B2 within cycle (*n*) are loaded into A1 or B1 registers and are used to generate matches in cycle (n+1).

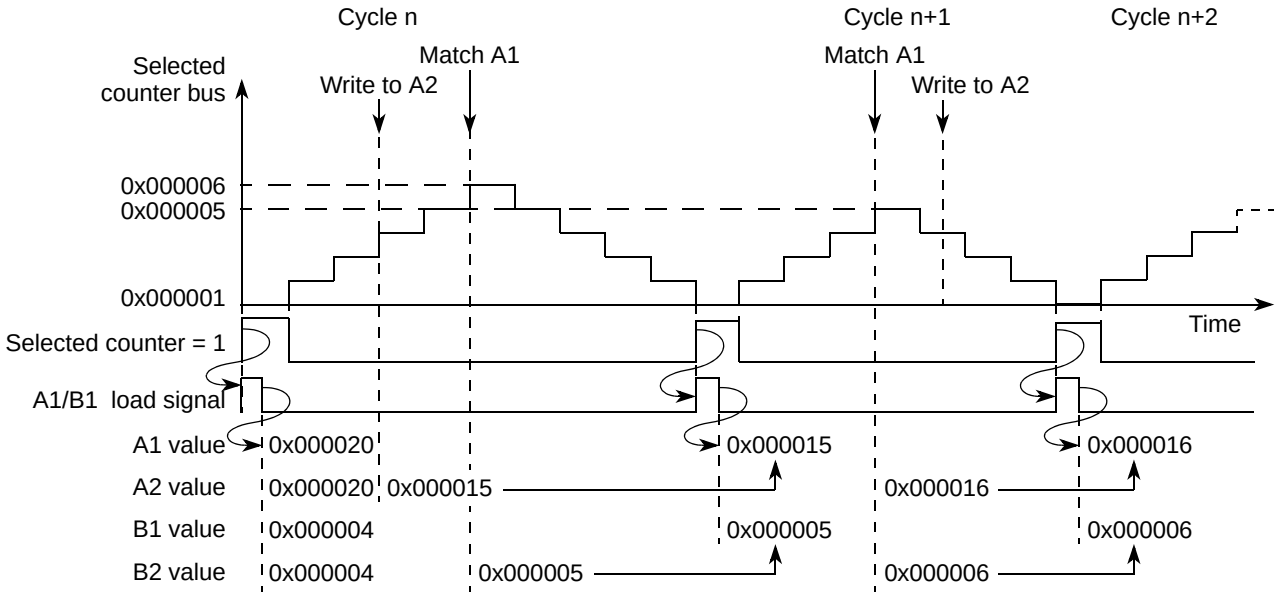


Figure 17-49. eMIOS OPWMCB Mode Example — A1/B1 Register Loading

The EMIOS_OUDR[n] bit can be used to disable the A1 and B1 updates, thus allowing the loading of these registers to be synchronized with the load of A1 or B1 registers in others channels. By using the update disable bit, the A1 and B1 registers can be updated in the same counter cycle.

In this mode A1 matches set the internal counter to one. When operating with leading edge dead time insertion, the first A1 match resets the internal counter to 0x000001. When a match occurs between register B1 and the internal time base, the output flip-flop is set to the value of the EDPOL bit. In the following match between A1 and the selected time base, the output flip-flop is set to the complement of the EDPOL bit. This sequence repeats continuously.

Figure 17-50 shows two cycles of a center-aligned PWM signal. Both A1 and B1 register values are changing within the same cycle, which allows the duty cycle and dead time values to be changed at simultaneously.

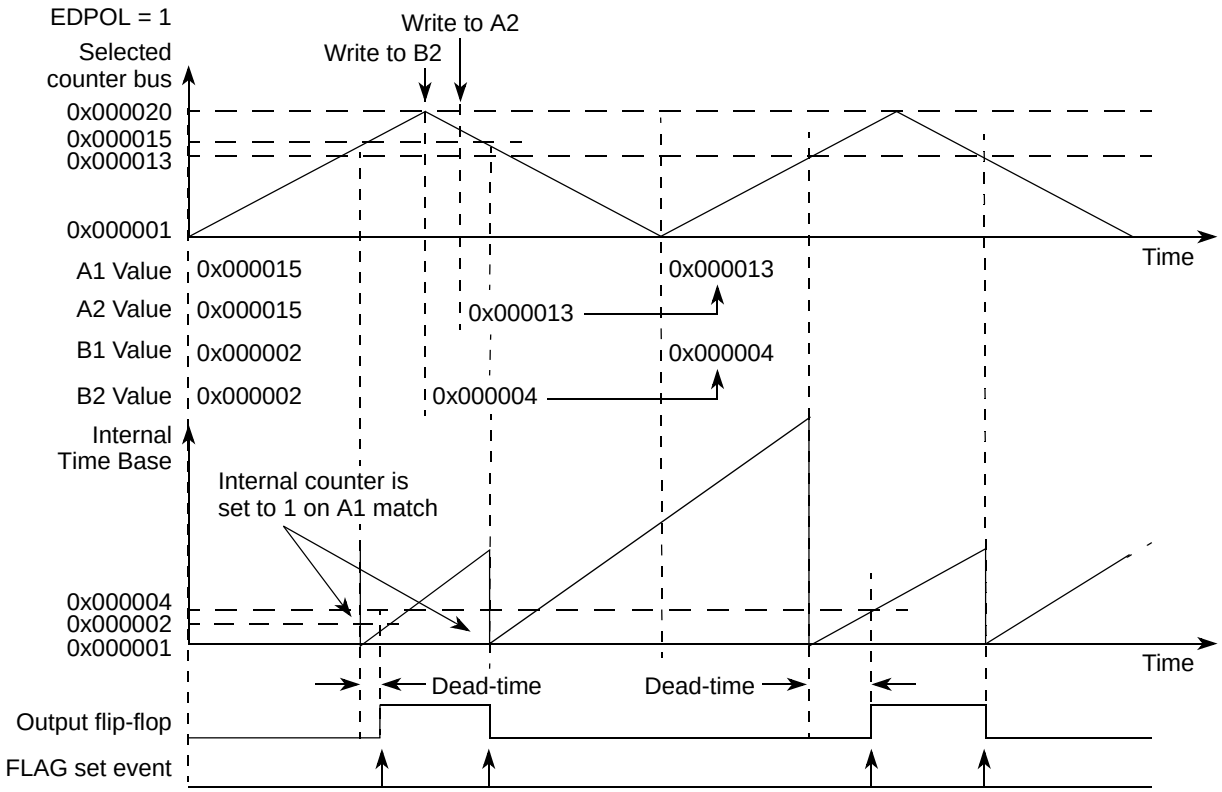


Figure 17-50. eMIOS PWMCB Mode Example — Lead Dead Time Insertion

As shown in Figure 17-51, when operating with trailing edge dead time insertion the first match between A1 and the selected time base sets the output flip-flop to the value of the EDPOL bit and resets the internal counter to 0x000001. In the second match between register A1 and the selected time base, the internal counter is reset to 0x000001 and B1 matches are enabled. When the match between register B1 and the selected time base occurs the output flip-flop is set to the complement of the EDPOL bit. This sequence repeats continuously.

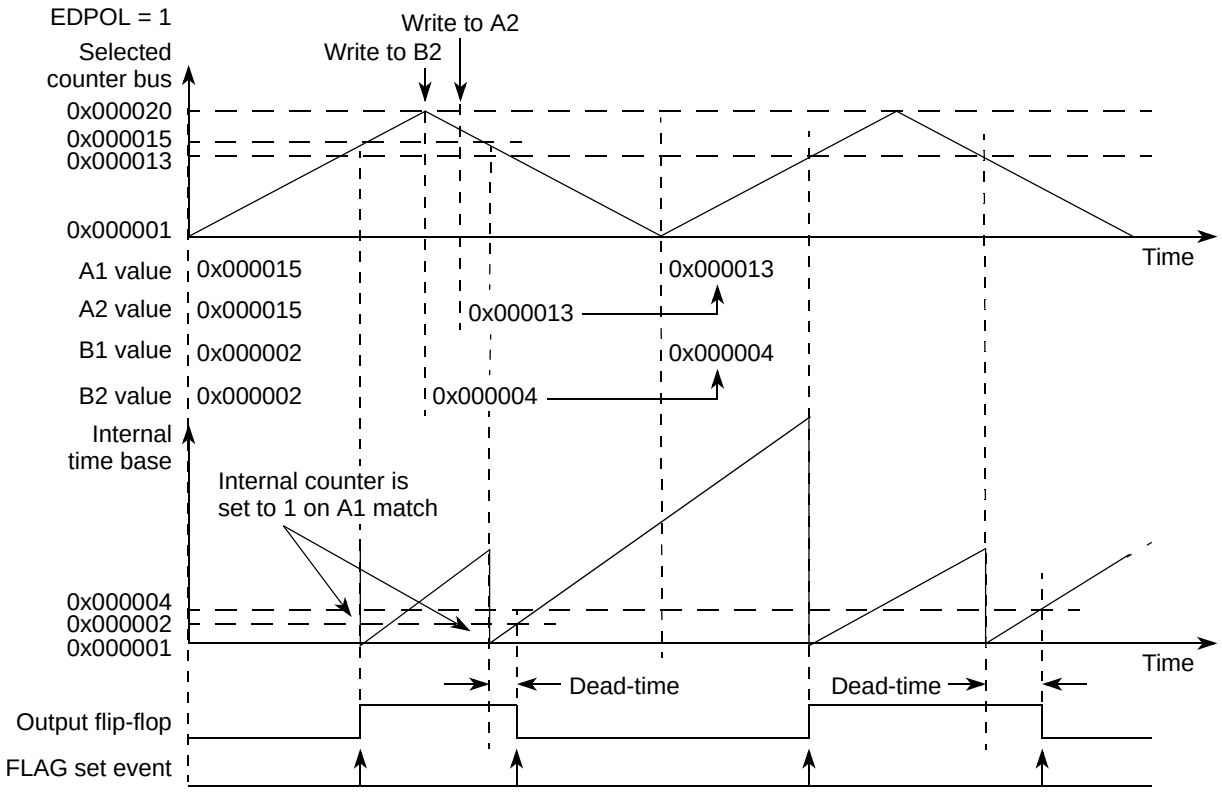


Figure 17-51. eMIOS PWMCB Mode Example — Trailing Dead Time Insertion

FLAG can be generated in the trailing edge of the output PWM signal when MODE[5] is cleared, or on both edges when MODE[5] is set. If subsequent matches occur on A and B, the PWM pulses continue to be generated, regardless of the state of the FLAG bit.

NOTE

In OPWMCB mode, FORCMA and FORCMB do not have the same behavior as a regular match. Instead they force the output flip-flop to a constant value which depends upon the selected dead time insertion mode, lead or trail and the value of the EDPOL bit.

FORCMA has different behaviors depending on the selected dead time insertion mode. In leading dead time insertion mode, writing one to FORCMA sets the output flip-flop to the compliment of EDPOL. In trailing dead time insertion mode, the output flip-flop is forced to the value of EDPOL.

If FORCMB is set, the output flip-flop value depends on the selected dead time insertion mode. In leading dead time insertion mode, FORCMB sets the output flip-flop to the value of EDPOL. In trailing dead time insertion mode, the output flip-flop is forced to the compliment of EDPOL.

NOTE

Setting the FORCMA bit does not reset the internal time base to 0x000001 as a regular A1 match does. FORCMA and FORCMB have the same behavior even in freeze or normal mode regarding the output flip-flop transition.

The FLAG bit is not set in the case of the FORCMA, FORCMB or both bits being set at the same time.

When FORCMA and FORCMB are both set, the output flip-flop is set to the compliment of the EDPOL bit. This is equivalent to FORCMA having precedence over FORCMB when lead dead time insertion is selected and FORCMB having precedence over FORCMA when trailing dead time insertion is selected.

Duty cycles from 0% to 100% can be generated by setting appropriate A1 and B1 values relative to the period of the external time base. Setting A1 = 1 or A1 = 0 generates a 100% duty cycle waveform. If A1 > period ÷ 2, where period refers to the selected counter bus period, then a 0% duty cycle is produced. Assuming EDPOL is one and OPWMCB mode with trailing dead time insertion mode is selected, 100% duty cycle signals can be generated if B1 occurs at or after the cycle boundary (external counter = 1).

NOTE

A special case occurs when A1 is set to the external counter bus period ÷ 2, which is the maximum value of the external counter. In this case the output flip-flop is constantly set to the EDPOL bit value.

Internal channel logic prevents matches from one cycle to propagate to the next cycle. In trailing dead time insertion mode, a B1 match from cycle (*n*) can eventually cross the cycle boundary and occur in cycle (n+1). In this case the B1 match is masked out and does not cause the output flip-flop to transition. Therefore matches in cycle (n+1) are not affected by the late B1 matches from cycle (*n*).

Figure 17-52 shows a 100% duty cycle output signal generated by setting A1 = 4 and B1 = 3. In this case the trailing edge is positioned at the boundary of cycle (n+1), which is actually considered to belong to cycle (n+2) and therefore does not cause the output flip-flip to transition.

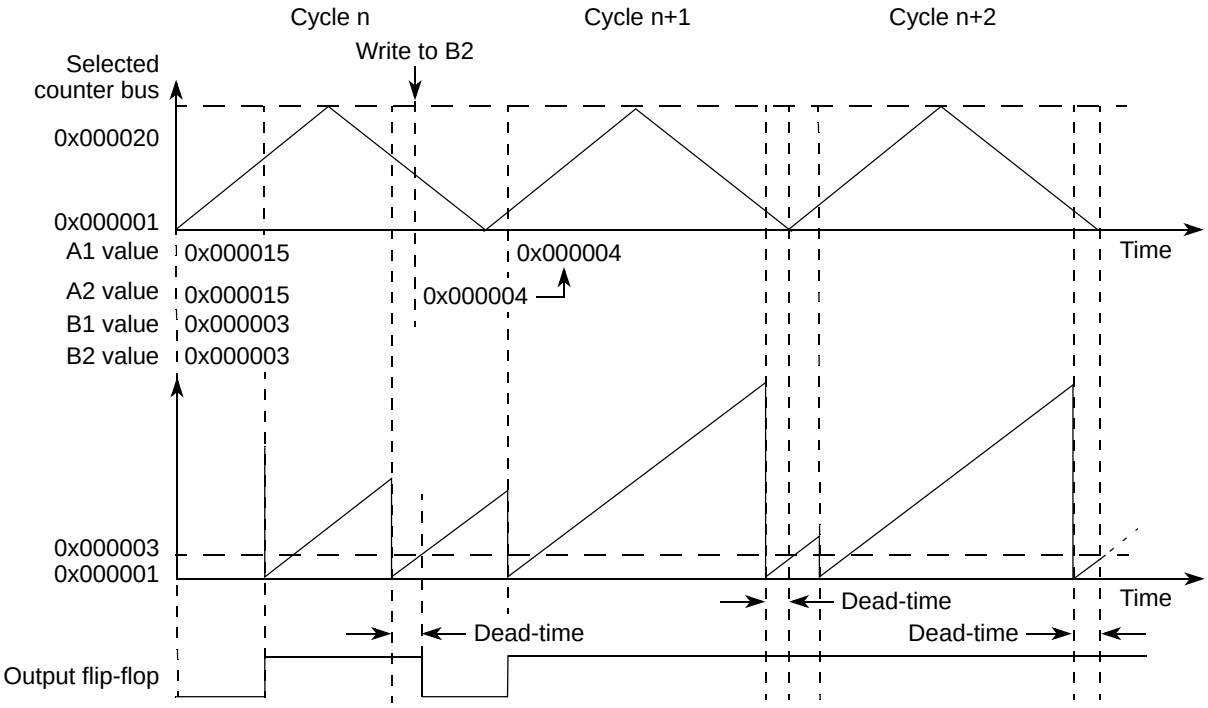


Figure 17-52. eMIOS PWMCB Mode Example — 100% Duty Cycle (A1 = 4, B1 = 3)

The output disable input, if enabled, causes the output flip-flop to transition to the compliment of EDPOL. This allows to the channel output flip-flop to be forced to a safety state. The internal channel matches continue to occur in this case, thus generating flags. When the output disable is negated, the channel output flip-flop is again controlled by A1 and B1 matches. This process is synchronous, meaning that the output channel pin transitions only occur on system clock edges.

Like in OPWMB and OPWFMB modes, the match signal used to set or clear the channel output flip-flop is generated on the negation of the channel comparator output signal which compares the selected time base with A1 or B1. Refer to Figure 17-44, which illustrates the delay from matches to output flip-flop transition in OPWFMB mode.

17.4.4.4.18 Output Pulse-Width Modulation, Buffered Mode (OPWMB)

The following table lists the output pulse-width modulation buffered mode settings:

Table 17-31. OPWMB Operating Modes

MODE[0:6]	Unified Channel OPWMB Operating Mode
0b1100000	Output pulse-width modulation, buffered. FLAG set on second match.
0b1100001	Reserved
0b1100010	Output pulse-width modulation, buffered. FLAG set on both matches.

OPWMB mode is used to generate pulses with programmable leading and trailing edge placement. An external counter is selected from one of the counter buses. The A1 register value defines the first edge and B1 defines the second edge. The output signal polarity is defined by the EDPOL bit. If EDPOL is zero, a negative edge occurs when A1 matches the selected counter bus and a positive edge occurs when B1 matches the selected counter bus.

The A1 and B1 registers are double buffered and updated from A2 and B2, respectively, at the cycle boundary. The load operation is similar to the OPWFMB mode.

Refer to Figure 17-46 for more information on A1 and B1 register updates.

Flags are generated at B1 matches when MODE[5] is cleared, or on both A1 and B1 matches when MODE[5] is set. If subsequent matches occur on comparators A and B, the PWM pulses continue to be generated regardless of the state of the FLAG bit.

The FORCMA and FORCMB bits allow software to force the output flip-flop to the level corresponding to a match on A1 or B1 respectively. FLAG is not set by the FORCMA and FORCMB operations.

The following rules apply to the OPWMB mode:

- B1 matches have precedence over A1 matches if they occur at the same time within the same counter cycle.
- A1 = 0 match from cycle (*n*) has precedence over a B1 match from cycle (n-1).
- A1 matches are masked if they occur after a B1 match within the same cycle.
- Values written to A2 or B2 on cycle (*n*) are loaded to A1 or B1 at the following cycle boundary (assuming EMIOS_OUDR[*n*] is not asserted). Thus the new values are used for A1 and B1 matches in cycle (*n*+1).

Figure 17-53 illustrates operation in OPWMB mode with A1/B1 matches and the transition of the channel output flip-flop. In this example EDPOL is zero.

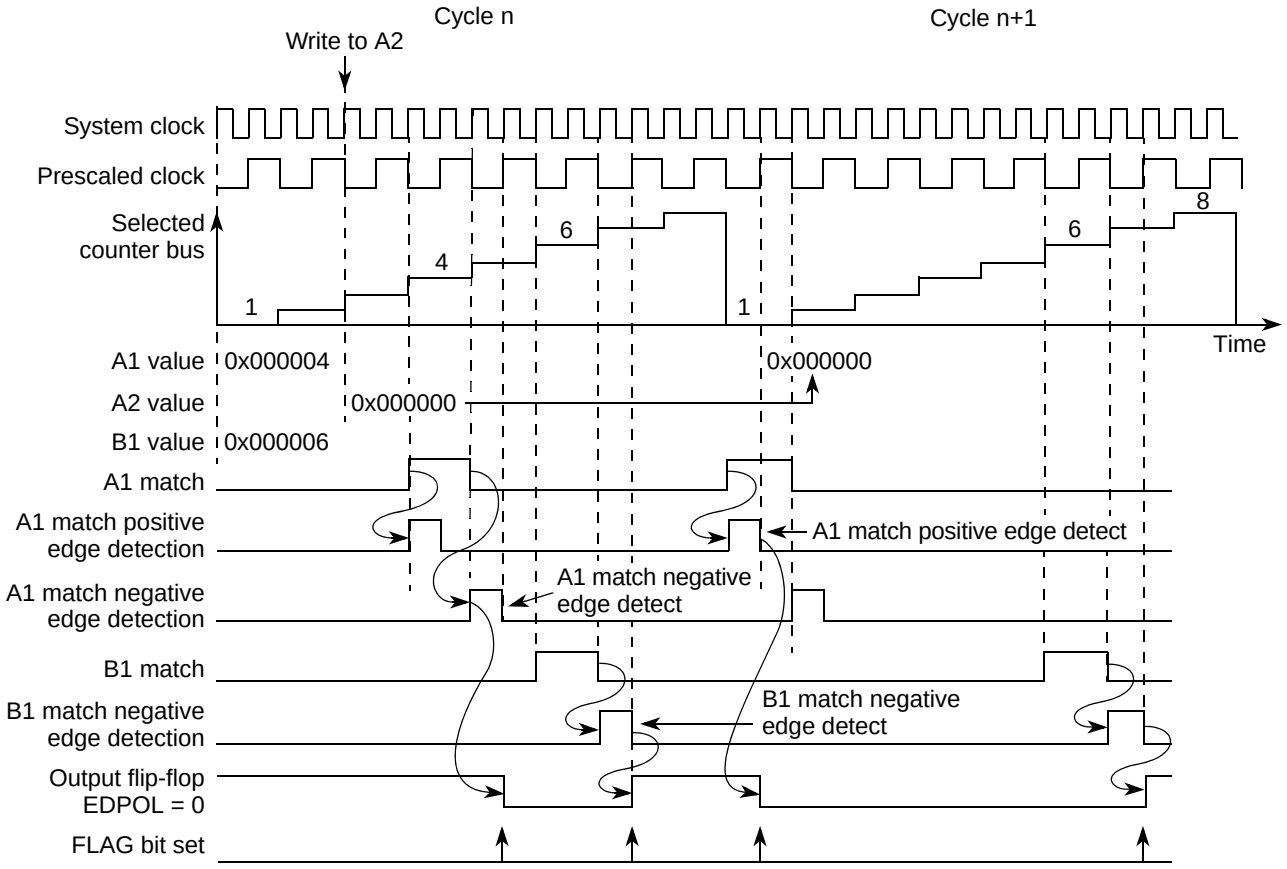


Figure 17-53. eMIOS OPWMB Mode Example — Matches and Flags

The output flip-flop transitions are based on the negative edges of the A1 and B1 match signals. Figure 17-53 shows the value of A1 being set to zero in cycle (n+1). In this case the match positive edge is used instead of the negative edge to transition the output flip-flop.

Figure 17-54 illustrates the channel operation for 0% duty cycle. The A1 match signal positive edge occurs at the same time as the B1 = 8 signal negative edge. In this case the A1 match has precedence over the B1 match, causing the output flip-flop to remain at the EDPOL value, thus generating a 0% duty cycle.

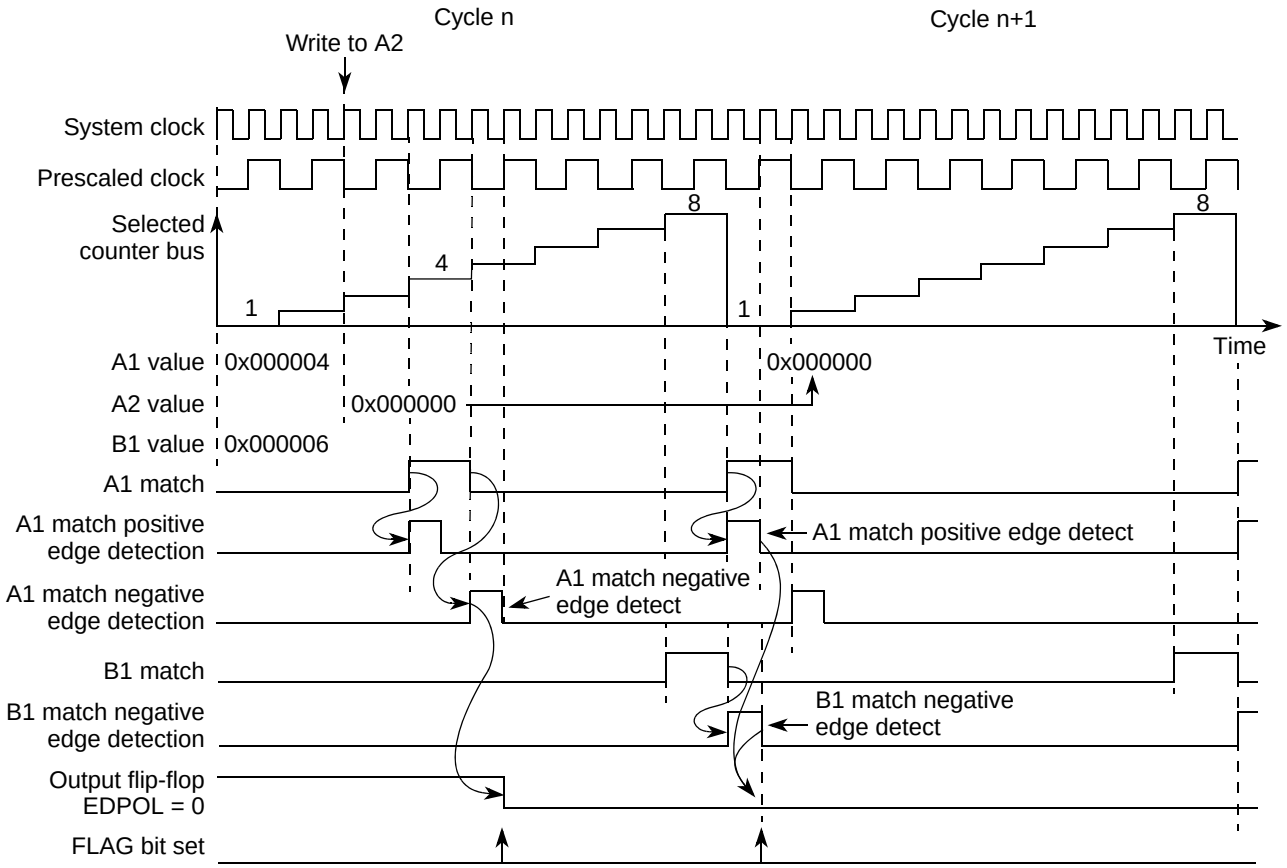


Figure 17-54. eMIOS OPWMB Mode Example — 0% Duty Cycle

Figure 17-55 shows the operation of the OPWMB mode with the output disable signal asserted. The output disable forces a transition in the output flip-flop to the EDPOL bit value. After the output disable is negated, the output flip-flop is allowed to transition at the next A1 or B1 match. The output disable does not modify the flag bit behavior. There is one system clock delay between the assertion of the output disable signal and the transition of the output flip-flop.

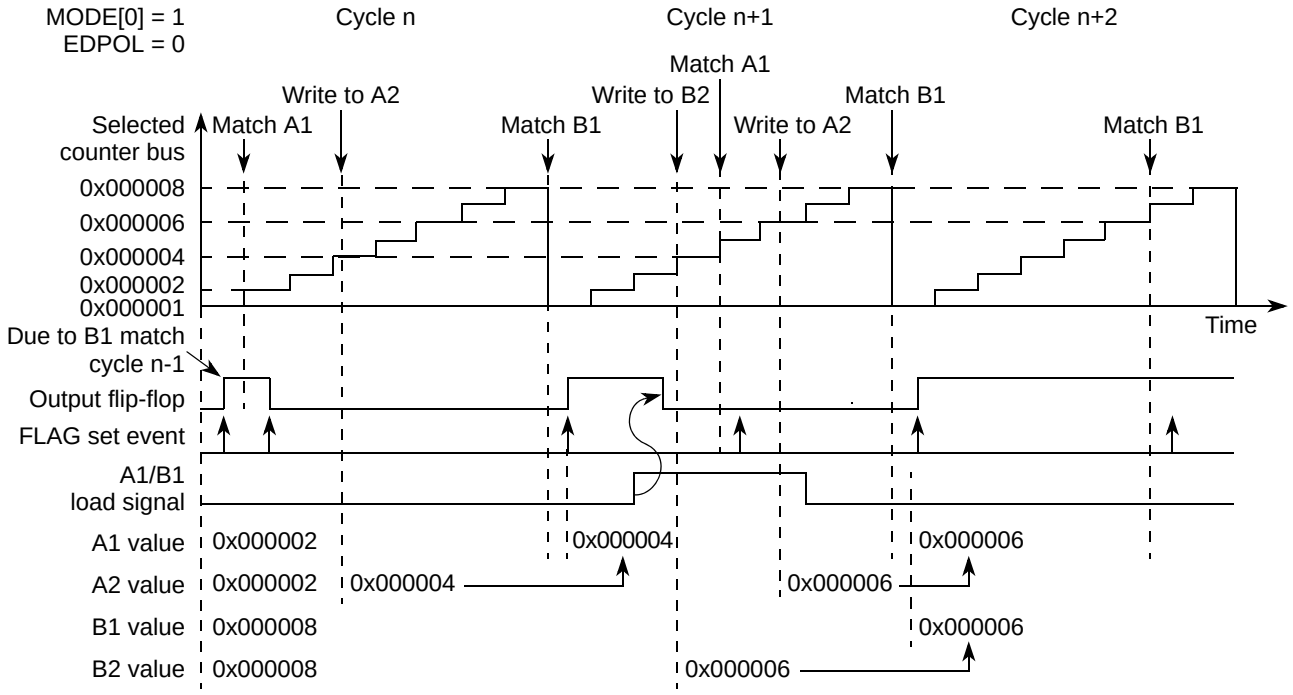


Figure 17-55. eMIOS OPWMB Mode Example — Active Output Disable

Figure 17-56 shows a waveform changing from 100% to 0% duty cycle. In this case EDPOL is zero and B1 is set to the same value as the period of the selected external time base.

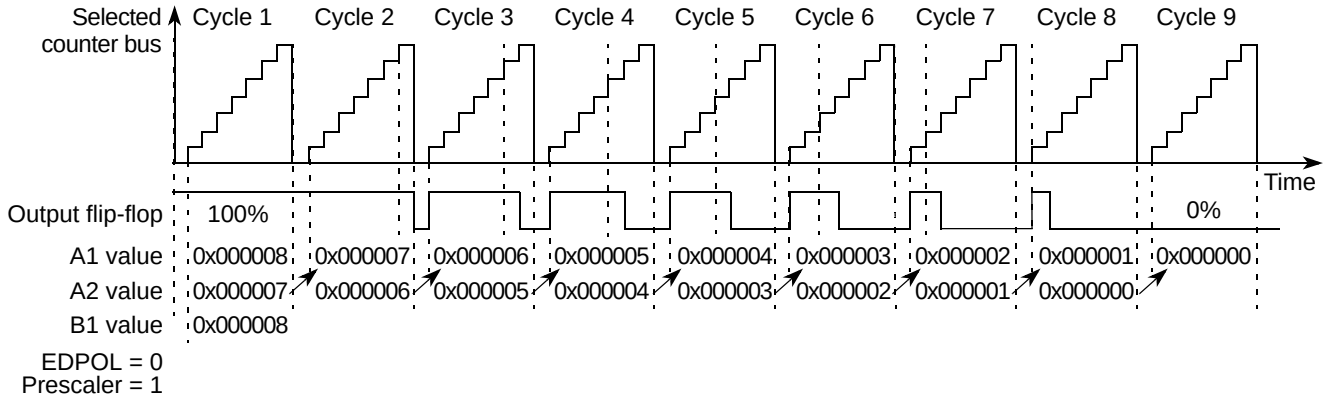


Figure 17-56. eMIOS OPWMB Mode Example — 100% to 0% Duty Cycle

In Figure 17-56 if B1 is set to a value lower than 0x000008 it is not possible to achieve 0% duty cycle by only changing A1 register value. Since B1 matches have precedence over A1 matches, the output flip-flop transitions to the compliment of EDPOL at B1 matches. In this example, if B1 = 0x000009, a B1 match does not occur, and thus a 0% duty cycle signal is generated.

17.5 Initialization/Application Information

Upon reset, all eMIOS unified channels default to general purpose inputs (GPIO input mode).

17.5.1 Considerations on Changing a UC Mode

Before changing an operating mode, program the UC to GPIO mode, and update EMIOS_CADR*n* and EMIOS_CBDR*n* with the values for the next operating mode. The EMIOS_CCR*n* can be written with the next operating mode. If a UC is changed from one mode to another without performing this procedure, the first operating cycle of the selected time base is unpredictable.

NOTE

When interrupts are enabled and an interrupt is generated, clear the FLAG bits before exiting the interrupt service routine.

17.5.2 Generating Correlated Output Signals

Correlated output signals can be generated by all output operating modes. Bits ODIS*n* can be used to control the update of these output signals.

To guarantee that the internal counters of correlated channels are incremented in the same clock cycle, the internal prescalers must be set up before enabling the global prescaler. If the internal prescalers are set after enabling the global prescaler, the internal counters can increment in the same ratio, but at a different clock cycle.

Drive output disable input signals with the EMIOS_Flag_Out signals of some UCs running in SAIC mode. When an output disable condition occurs, the software interrupt routine must service the output channels before servicing the channels running SAIC. This procedure avoid glitches in the output pins.

17.5.3 Time Base Generation

For all channel operation modes that generate a time base (MC, OPWFM, OPWM, MCB, OPWFMB and OPWMB), the internal counter rate can be modified by configuring the clock prescaler ratio. The clock prescaler can use several ratios calculated as:

$$\text{Ratio} = (\text{GPRE} + 1) \times (\text{UCPRE} + 1)$$

The prescaled clocks in Figure 17-58, Figure 17-59, and Figure 17-57 illustrate the time base generation mechanism. Figure 17-60 shows the time base generation when using the internal clock set and clear on match start.

If the prescaler ratio is 9, the prescaled clock pulses every nine clock cycles and the internal counter increments every nine clock cycles. The high pulse allows the EMIOS_CCNTR*n* to increment as long as no other conditions disable this counter. The match signal is generated by pulsing every time the internal counter matches the programmed match value. For a programmed match value, the time base-period becomes smaller as the prescaler ratio increases.

Figure 17-57 shows the prescaler ratio equal to 1, therefore the prescaled clock remains high and continuously enables the internal counter (EMIOS_CCNTR*n*):

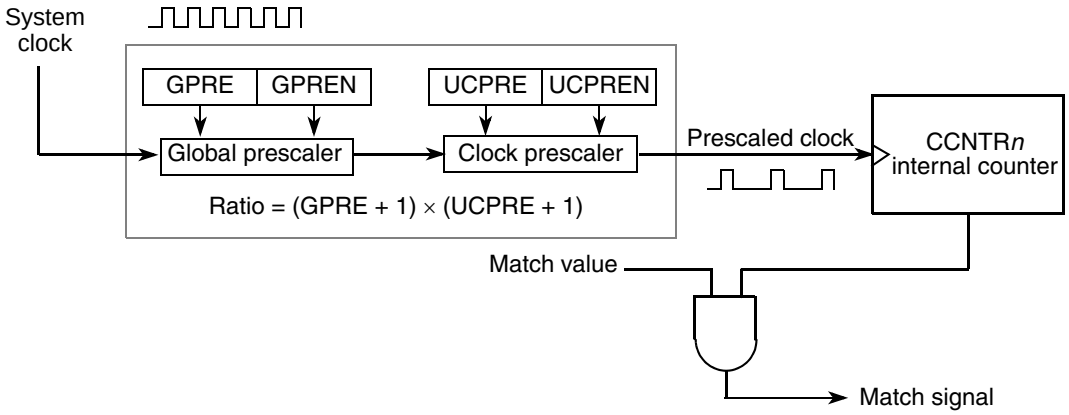


Figure 17-57. eMIOS Time Base Generation Block Diagram

Figure 17-58 shows the prescaler ratio equal to one, therefore the prescaled clock remains high and continuously enables the internal counter (EMIOS_CCNTR*n*):

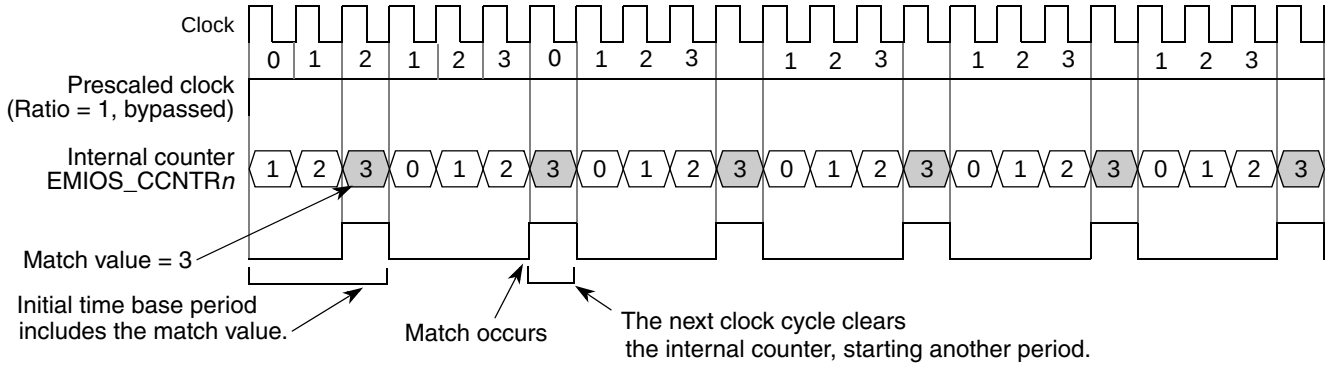


Figure 17-58. eMIOS Time Base Example — Fastest Prescaler Ratio = 1

Figure 17-59 shows the prescaler ratio equal to three, therefore, the prescaled clock pulses every three clock cycles and the internal counter increments every three clock cycles:

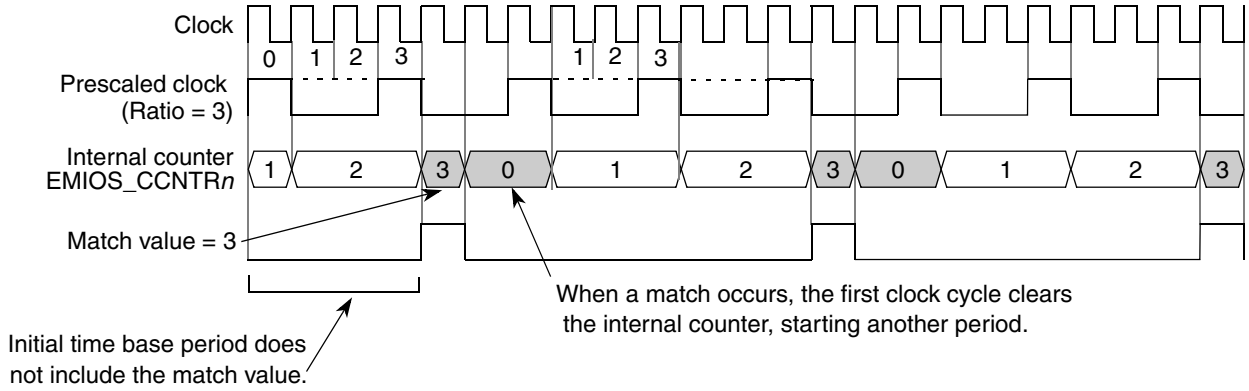
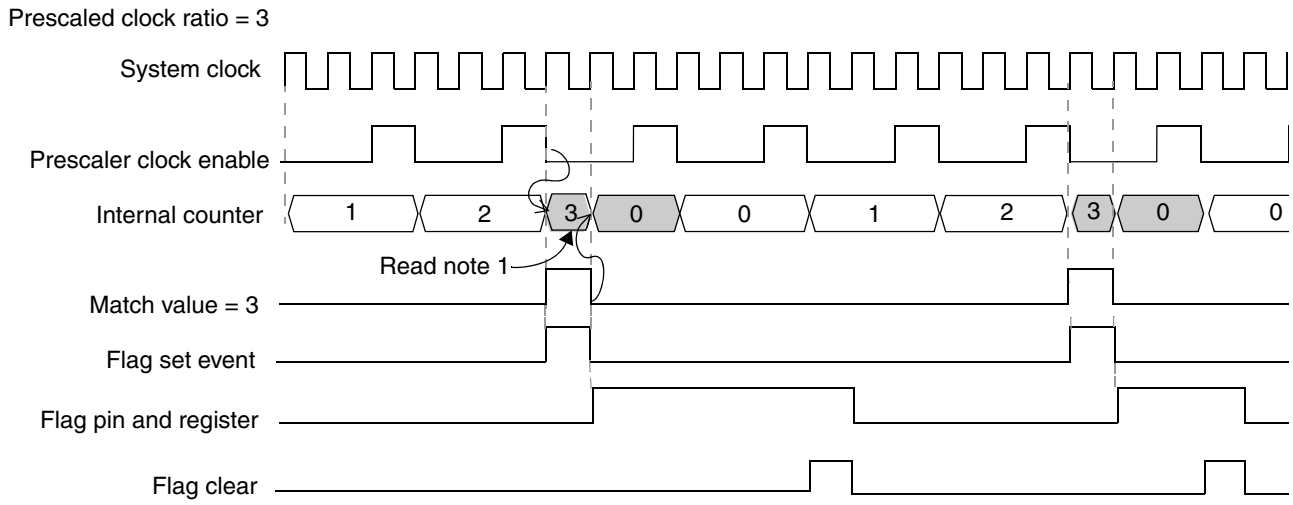


Figure 17-59. eMIOS Time Base Example — Prescale Ratio = 3, Match Value = 3

Figure 17-60 shows an example of time-base generation using the internal clock with clear on match start:



Note 1: When a match occurs, the first clock cycle is used to clear the internal counter. The internal counter starts counting after the second edge of the prescaled clock.

Figure 17-60. Time Base Generation Using the Internal Clock with Clear on Match Start

Chapter 18
Enhanced Time Processing Unit (eTPU)

18.1 Introduction

The enhanced time processing unit (eTPU) operates in parallel with the MPC5566 core (CPU) to:

- Execute programs independently from the host core
- Detect and precisely record the timing of input events
- Generate complex output waveforms
- Enhances the CPU with time processing without requiring real-time host processing

The host core setup and service times for each input and output event are greatly minimized. The MPC5566 contains two eTPUs.

The eTPU improves the performance of the device by providing high-resolution timing:

- eTPU dedicated channels include two match and two capture registers (TPUs had one).
- eTPU engines are optimized to service channel hardware
- Fast instruction execution rate of the eTPU engine reduces service time

Because responding to hardware service requests is primarily done by the eTPU engine, the host is free to handle higher level operations.

18.1.1 eTPU Implementation

For more detailed information regarding the eTPU module and compiler, refer to the *Enhanced Time Processing (eTPU) Reference Manual*. This chapter provides an overview of the eTPU module:

- 4 KB of shared data memory (SDM). This memory is also referred to as eTPU shared parameter (SP) RAM, or (SPRAM).
- 20 KB of shared code memory (SCM).
- MPC5566 has two eTPU engines: eTPU A and eTPU B
- The eTPU debug interface is built into the device's debug module. Refer to Section 10.2.1 of the *eTPU Reference Manual* for details on eTPU debug.
- Data transfer requests are implemented to each eTPU engine: eTPU A has five DMA requests; eTPU B has 12 DMA requests.
- I/O channel pairs can be shared on a common pin. The output buffer enable (OBE) is not used in the device. The outputs are enabled in the SIU; refer to Chapter 6, "System Integration Unit (SIU)."

Because of the differences between the MPC5566 implementation of the eTPU and the full eTPU, full register bit descriptions are included within this chapter as well as in the *Enhanced Time Processing (eTPU) Reference Manual.*

18.1.2 Block Diagram

Figure 18-1 shows a top-level block diagram of dual eTPU engines in the MPC5566.

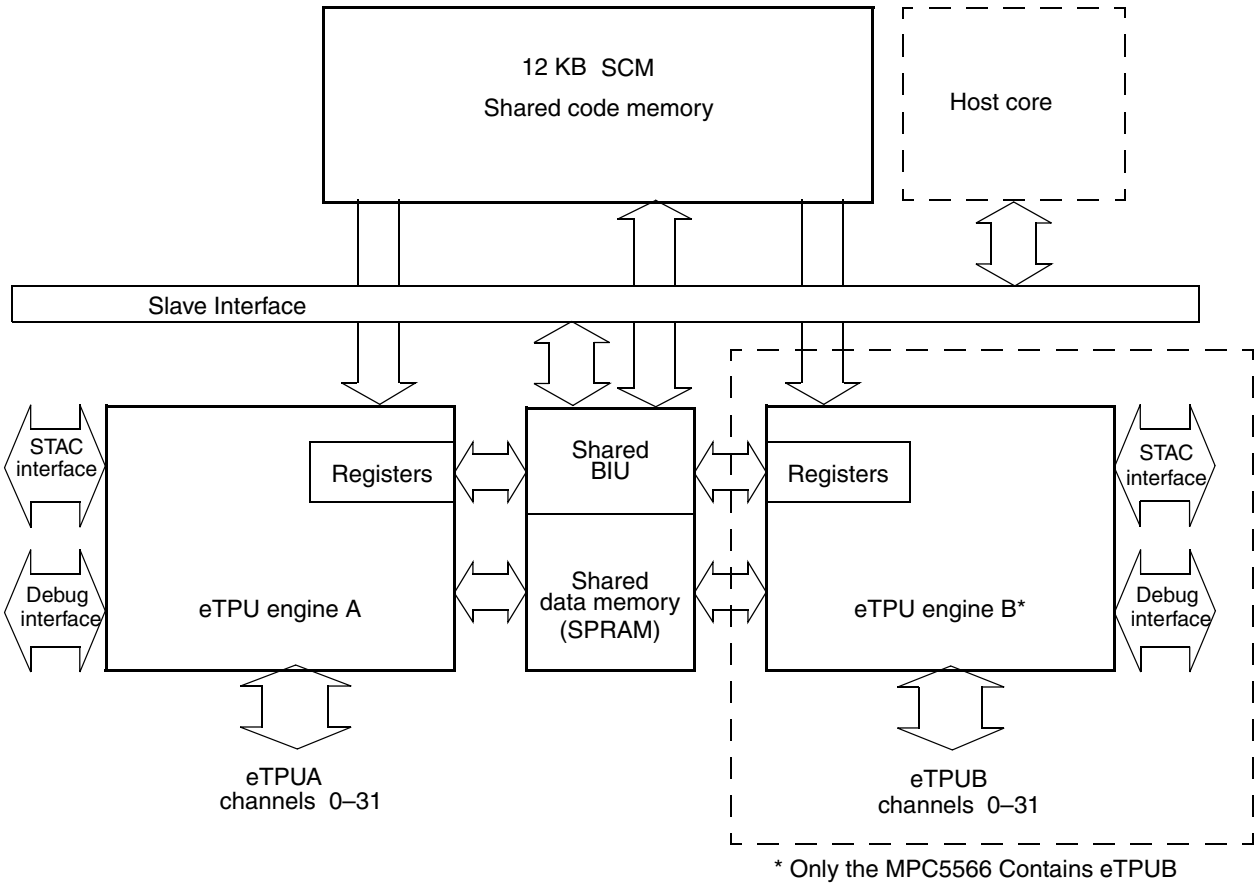


Figure 18-1. Dual eTPU Block Diagram

Figure 18-2 shows the block diagram for the eTPU engine.

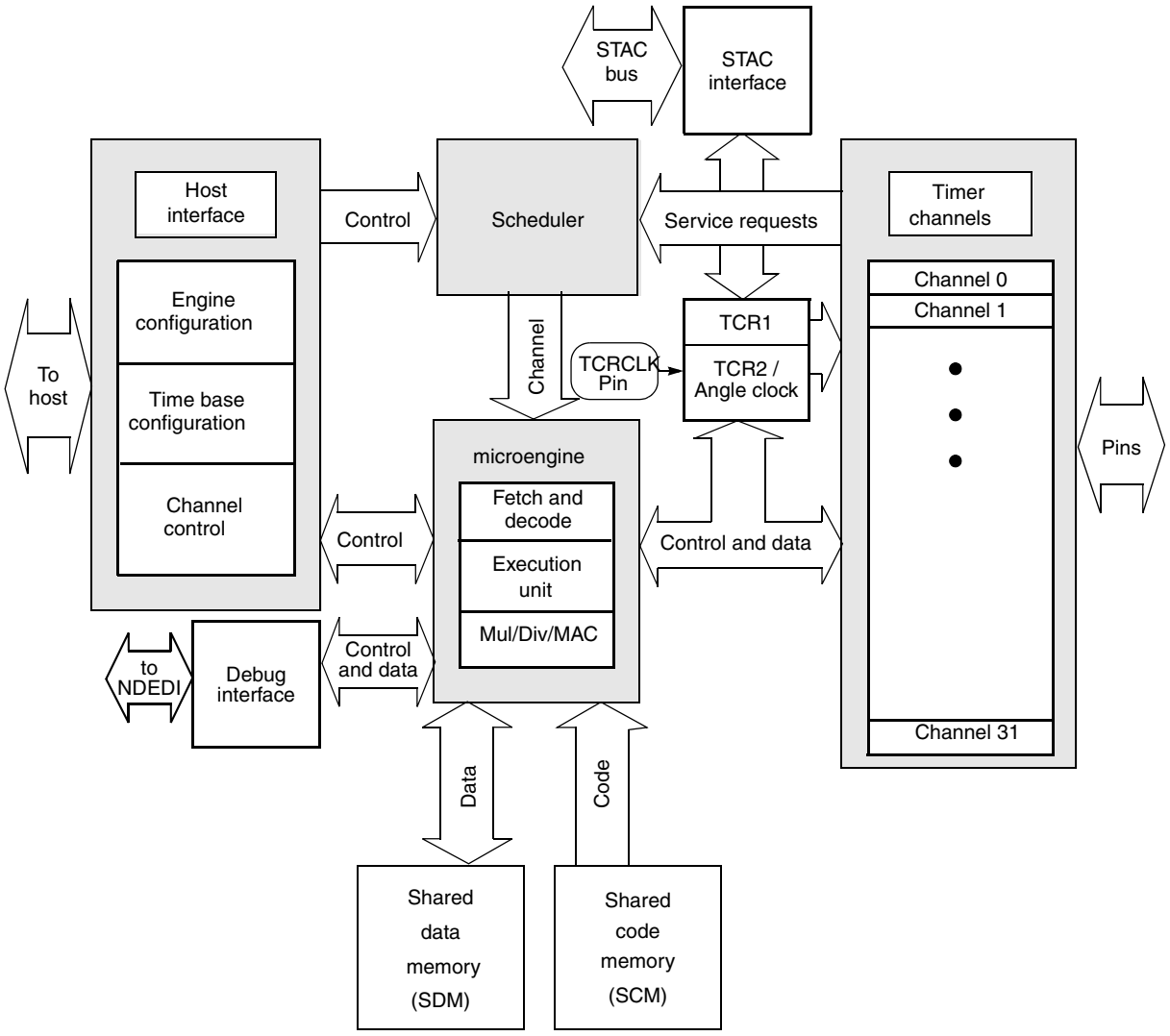


Figure 18-2. eTPU Engine Block Diagram

18.1.3 eTPU Operation Overview

The eTPU is a real-time microprocessed subsystem. Therefore, it runs microengine code from instruction memory (SCM) to handle specific events and accesses data memory (SDM) for parameters, work data, and application state information. Events can originate from I/O channels (due to pin transitions and/or time base matches), device core requests, or inter-channel requests. Events that call for local eTPU processing activate the microengine by issuing a service request. The service request microcode can send an interrupt to the device core, but cannot directly interrupt the core using I/O channel events.

Each channel has a function that consists of a set of microengine routines, called threads, that service eTPU requests which defines the channel's behavior. Function routines, which reside in the SCM, are also used to configure the channel. A function can be assigned to several channels, but a channel can only process

one function at a given moment. The eTPU can change the function assigned to a channel if the channel is reconfigured by the device core. The device core configures the function to channel assignments.

The following eTPU hardware supplies resource sharing features that support concurrency:

- A hardware scheduler dispatches the service request microengine routines based on a set of priorities defined by the device's core. Each channel has its own unique priority assignment that primarily depends on CPU assignment. The channel's number is an inherent property also used to determine priority.
- A service request routine cannot be interrupted by another service request until it ends, that is, until an end instruction is executed. This sequence of uninterrupted instruction execution is called a thread. The core can terminate the thread by writing 1 to the FEND bit in the ETPU_ECR register.
- Channel-specific contexts (registers and flags) are automatically switched between the end of a thread and the beginning of the next one.
- SDM arbitration, a dual-parameter coherency controller, and semaphores can be used to ensure coherent access to eTPU data shared by both eTPU engines and the device core.

18.1.4 eTPU Engine

The eTPU engine processes input pin transitions and generates output pin waveforms. These events are triggered by eTPU timers (time bases) that are driven by a system clock to give absolute time control or by an asyncronous counter, such as an angle clock that is tracking the angle of a rotating shaft.

Each eTPU engine consists of the following blocks: 32 independent timer channels, a task scheduler, a host interface, and a microprocessor (hereinafter called a microengine) that has dedicated hardware for input signal processing and output signal generation over the 32 I/O channels. Each channel can choose between two 24-bit counter registers for a time base.

The microengines fetch microinstructions from shared code memory (SCM). eTPU application parameters and global and local variables, referred to as work data, are held in 32-bit shared data memory (SDM), which is also used for passing information between the device's core and both microengines. The bus interface unit (BIU) allows the device's core to access eTPU registers, SDM, and SCM.

The blocks of an eTPU engine are duplicated in a dual eTPU configuration. eTPU engines A and B are often referred to as eTPU A and eTPU B in this document.

18.1.4.1 Time Bases

Each eTPU engine has two 24-bit count registers TCR1 and TCR2 that provide reference time bases for all match and input capture events. Prescalers for both time bases are controlled by the device core through bit fields in the eTPU engine configuration registers.

The values for each of TCR1 and TCR2 counter registers can be independently derived from the system clock or from an external input via the TCRCLK pin. In addition, the TCR2 time base can be derived from special angle-clock hardware that enables implementing angle-based functions. This feature is added to support advanced angle-based engine control applications.

The TCRs can also drive an eMIOS time base through the shared time and counter (STAC) bus, or they can be written by eTPU function software.

18.1.4.2 eTPU Timer Channels

Each eTPU engine has 32 identical, independent channels. Each channel corresponds to an input/output signal pair. Every channel has access to two 24-bit counter registers, TCR1 and TCR2.

Each channel consists of event logic which supports a total of four events, two capture and two match events. The event logic contains two 24-bit capture registers and two 24-bit match registers. The match registers are compared to a selected TCR by greater-than-or-equal-to and equal-only comparators. The match and compare register pairs enable many combinations of single and double-action functions.

The channel configuration can be changed by the microengine. Each channel can perform double capture, double match or a variety of other capture-match combinations. Service requests can be generated on one or both of the match events and/or on one of the capture events.

Digital filters that have different filtering modes are provided for the input signals.

Every channel can use any time base or angle counter for either match or capture operation. For example, a match on TCR1 can capture the value of TCR2. The channels can request service from the microengine due to recognized pin transitions (input events) or time base matches.

Every eTPU channel can be configured with the following combinations:

- Single input capture, no match (TPU3 functionality)
- Single input capture with single match time-out (TPU3 functionality)
- Single input capture with double match time-out with several double match submodes
- Double input capture with single or double match time-out with several double match submodes
- Single output match (TPU3 functionality)
- Double output match with several double match submodes
- Input-dependent output generation

The double match functionality has various combinations for generation of service request and determining pin actions.

18.1.4.3 Host Interface

Each engine’s host interface allows the device core to control the operation of the eTPU. In order for the eTPU to start operation, the device core must initialize the eTPU by writing to the appropriate host interface registers to assign a function and priority to each channel. In addition, the device core writes to the host service request and channel configuration registers to further define operation for each initialized channel.

NOTE

The host transfers the code image for the eTPU microcode to the SCM, then the host enables eTPU access to the SCM (which also disables host access).

18.1.4.4 Shared Data Memory (SDM)

The SDM works as data RAM that can be accessed by the device core and up to two eTPU engines. This memory is used for either:

- Information transfer between the device core and the eTPU
- Data storage for the eTPU microcode program
- Communication between the two eTPU engines

The SDM width is 32 bits, and is accessible by the host in any of the three formats: byte, 16-bit, or 32-bit. The eTPU can access the SDM's full 32 bits, lower 24 bits or upper byte (8-bit). The host can also access the SDM space mirrored in an alternate area with parameter sign extension (PSE). PSE allows accessing 24-bit data as 32-bit sign-extended data without using the device's bandwidth to extend the data.

Parameter sign extension accesses differ from the usual host accesses to the original SDM area:

Writes are effective only to the lower 3-bytes of a word: the word's most significant byte (byte address) is kept unaltered in SDM.

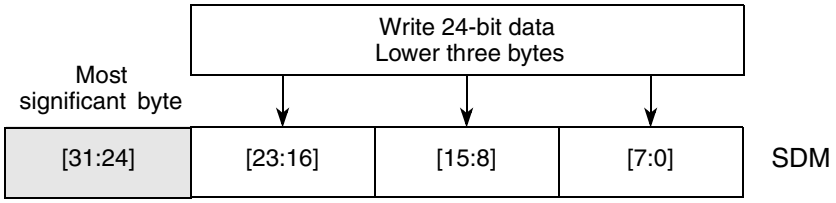


Figure 18-3. SDM PSE Area Write

NOTE

For the most significant byte, the word format is big endian.

Reads return the lower 3-bytes of a word sign-extended to 32 bits; the most significant bit of the word's second most significant byte (byte addresses) is copied in all 8 bits of the most significant read byte.

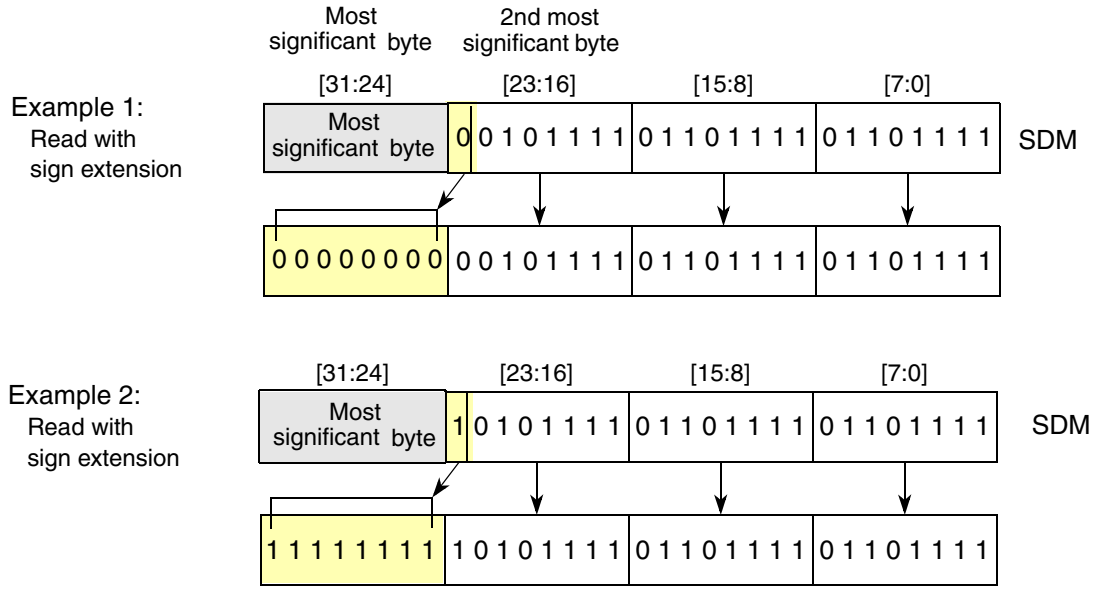


Figure 18-4. PSE Accesses

Each eTPU channel can be associated with a variable number of parameters located in the SDM, according to its selected function. In addition, the SDM can be fully shared between two eTPU engines, enabling communication between them. Each function can require a different number of parameters. During eTPU initialization the host has to program channel base addresses, allocating proper parameters for each channel according to its selected function.

In the host address space each parameter occupies four bytes (32 bits). eTPU usage of the upper byte is achieved by having a 32-bit preload (P) register that can access the upper byte, the lower 24 bits, or all the 32 bits. The microcode can switch between access sizes at any time.

18.1.4.5 Task Scheduler

As mentioned in Section 18.1.3, “eTPU Operation Overview,” every channel function is composed of one or more threads, and threads cannot be interrupted by host or channel events, such as channel servicing. The function of the task scheduler, therefore, is to recognize and prioritize the channels needing service and grant execution time to each channel. The time given to an individual thread for execution or service is called a time slot. The duration of a time slot is determined by the number of instructions executed in the thread plus SDM wait-states received, and varies in length. Although several channels can request service at the same time, the function threads must be executed serially.

At any time, an arbitrary number of channels can require service. The channel logic, eTPU microcode, or the host application notifies the scheduler by issuing a service request.

Out of reset, all channels are disabled. The device core makes a channel active by assigning it one of three priorities: high, middle, or low. The scheduler determines the order in which channels are serviced based on channel number and assigned priority. The priority mechanism, implemented in hardware, ensures that all requesting channels are serviced.

18.1.4.6 Microengine

The eTPU microengine is a simple RISC implementation that performs each instruction in a microcycle of two system clocks, while pre-fetching the next instruction through an instruction pipeline. Instruction execution time is constant for the arithmetic logic unit (ALU) unless it gets wait states from SDM arbitration.

Microcode is stored in shared code memory (SCM) that is 32 bits wide. The microengine instruction set provides basic arithmetic and logic operations, flow control (jumps and subroutine calls), SDM access, and channel configuration and control. The instruction formats are defined in such a way that allow particular combinations of two or three of these operations with unconflicting resources to be executed in parallel in the same microcycle, thus improving performance.

The microengine also has an independent multiply/divide/MAC unit that performs these complex operations in parallel with other microengine instructions.

Channel functionality is integrated into the instruction set through channel control operations and conditional branch operations, which support jumps/calls on channel-specific conditions. This allows quick and terse channel configuration and control code, contributing to reduced service time.

18.1.4.7 Dual eTPU Engine System

The MPC5566 eTPU implementation includes two eTPU engines sharing SDM and the same code in the SCM.

The two eTPU engines share the bus interface unit (BIU) and the shared data memory (SDM). This allows the MPC5566 core to communicate with the eTPU and also provides a means of communication between the eTPU engines. The shared BIU includes coherency logic which supports dual parameter (8 bytes) coherency in transfers between the host and eTPU, using a temporary parameter area within the SDM.

18.1.4.8 Debug Interface

Nexus level 3 debug support is available through the eTPU Nexus development interface (NDEDI). Refer to Chapter 25, “Nexus Development Interface.”

18.1.5 Features

The eTPU includes these distinctive features:

- Up to 32 channels for each eTPU engine: each channel is associated with an I/O signal pair
  - — Enhanced input digital filters on the input pins for improved noise immunity. The eTPU digital filter can use two samples, three samples, or work in continuous mode.
  - — Orthogonal channels, except for channel 0: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality. Channel 0 has the same capabilities of the others, but can also work with special angle counter logic.
  - — A link service request allows activation of a channel thread by request of another channel, even between eTPU engines.

  - A host service request allows activation of a channel thread by the device core request.
  - Each channel has an event mechanism that supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal or equal-only comparator.
- Two independent 24-bit time bases for channel synchronization
  - The first time base can be clocked by the system clock with programmable prescaler division from 2 to 512 (in steps of 2).
  - The first time base can also be clocked by an external signal with programmable prescaler divisions of 1 to 256.
  - The second time base can be clocked by an external signal with programmable prescaler divisions from 1 to 64 or by the system clock divided by 8.
  - The second time base has a programmable prescaler that applies to all TCR2 clock inputs except the angle counter.
  - The second time base counter can work as an angle counter, enabling angle-based applications to match angle instead of time.
  - The second time base can alternatively be used as a pulse accumulator gated by an external signal.
  - Either time base can be written or read by either eTPU engine at any time.
  - Either time base can be read, but not written, by the host.
  - Both time bases can be exported or imported from engine to engine through the STAC (shared time and counter) bus.

NOTE

An engine cannot export or import to or from itself. An engine cannot import a time base and/or angle count if it is in angle mode.

- Event-triggered RISC processor (microengine)
  - 2-stage pipeline implementation (fetch and execution), with separate instruction memory (SCM) and data memory (SDM).
  - Two-system-clock microcycle fixed-length instruction execution for the ALU.
  - 20 KB of shared code memory (SCM).
  - Interleaved SCM access in dual-engine eTPU (MPC5566) avoids contention in time for instruction memory.
  - 4 KB of shared data memory (SDM)
  - Interleaved SDM access in dual-engine eTPU (MPC5566) avoids contention in time for instruction memory.
  - Instruction set with embedded channel support, including specialized channel control subinstructions and conditional branching on channel-specific flags.
  - Channel-oriented addressing: channel-bound address mode with host configured channel base address allows the same function to operate independently on different channels.
  - Channel-bound data address space of up to 128 32-bit parameters (512 bytes).

  - — Global parameter address mode allows access to common channel data of up to 256 32-bit parameters (1024 bytes).
  - — Support for indirect and stacked data access schemes.
  - — Parallel execution of: data access, ALU, channel control and flow control subinstructions in selected combinations.
  - — 24-bit registers and ALU, plus one 32-bit register for full-width SDM access.
  - — Additional 24-bit multiply/MAC/divide unit which supports all signed/unsigned/ multiply/MAC combinations, and unsigned 24-bit divide. The MAC/divide unit works in parallel with the regular microcode commands.
- Resource sharing features resolve channel contention for common use of channel registers, memory and microengine time
  - — Hardware scheduler works as a ‘task management’ unit, dispatching event service routines by predefined, host-configured priority.
  - — Hardware breakpoints on data access, qualified by address and/or data values.
  - — Hardware breakpoints on instruction address.
  - — Automatic channel context switch when a ‘task switch’ occurs; that is, one function thread ends and another begins to service a request from another channel. Channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel.
  - — Individual channel priority setting in three levels: high, middle, and low.
  - — Scheduler priority scheme allows calculation of worst case latency for event servicing and ensures servicing of all channels by preventing permanent blockage.
  - — SDM shared between host core and both eTPU engines, supporting channel-channel or host-channel communication.
  - — Hardware implementation of four semaphores allows for resource arbitration between channels in both eTPU engines.
  - — Hardware semaphores are directly supported by the microengine instruction set.
  - — Dual-parameter coherency hardware support allows coherent (to host) access to two parameters by microengines in back-to-back accesses, or by Host CPU in 64-bit accesses.
  - — Coherent dual-parameter controller allows coherent (to microengines) accesses to two parameters by the host.
- Test and development support features
  - — Nexus level 3 debug support through the eTPU Nexus block (NDEDI)
  - — Software breakpoints
  - — SCM (code memory) continuous signature-check built-in code integrity test multiple input signature calculator (MISC): runs concurrently with eTPU normal operation

18.2 Modes of Operation

The eTPU is capable of working in the following modes.

18.2.1 User Configuration Mode

By having access to the shared code memory (SCM), the core has the ability to program the eTPU cores with time functions.

18.2.2 User Mode

In user mode the core does not access the eTPU shared code memory, and pre-defined eTPU functions are used.

18.2.3 Debug Mode

The core debugs eTPU code, accessing special trace/debug features via Nexus interface:

- Hardware breakpoint/watchpoint setting
- Access to internal registers
- Single-step execution
- Forced instruction execution
- Software breakpoint insertion and removal

18.2.4 Module Disable Mode

eTPU engine clocks are stopped through a register write to ETPU_ECR bit MDIS, saving power. Input sampling stops. eTPU engines can be in stop mode independently. Module disable mode stops only the engine clock, so that the shared BIU and global channel registers can be accessed, and interrupts and DMA requests can be cleared and enabled/disabled. An engine only enters module disable mode when any currently running thread is finished.

These modes are loosely selected: there is no unique register field or signals to choose between them. Some features of one mode can be used with features of other modes.

18.2.5 eTPU Mode Selection

User and user configuration are the production operating modes, and differ from each other only in access to SCM.

Module disable mode is entered by setting ETPU_ECR[MDIS]. eTPU engines can be individually stopped (there is one ETPU_ECR for each engine).

18.3 External Signal Description

18.3.1 Overview

There are a total 65 external signals in each eTPU engine:

- 32 channel input signals
- 32 channel output signals

- TCRCLK clock input

Therefore, a dual-engine system has a total of 130 external signals. There are four internal output disable signals for each eTPU engine that implement the output disable feature needed for motor control.

Refer to 17.2.1.1, "Output Disable Input—eMIOS Output Disable Input Signals," for more information.

18.3.2 Output and Input Channel Signals

Each eTPU channel has an input and output associated with it, and these can be connected to external pins or wired internally to other peripheral devices. As shown in Chapter 20, "Deserial Serial Peripheral Interface (DSPI)" and Table 20-20, eTPU output channel 0 (ETPUA[0]_ETPUA[12]_GPIO[114]) is serialized to DSPI C and then connected to input 2 on the IMUX for external $\overline{\text{IRQ}}$[3]. Most eTPU channels are serialized, but eTPU channels 22 and 23 are connected to their pin only.

Some channels are serialized through one DSPI to two different locations. The eTPU channel 29 (ETPUA[29]_PCSC[2]_GPIO[143]) is serialized to both eTPU_A input channel 29 and input 1 on IMUX for external $\overline{\text{IRQ}}$[8]. This serialization is performed by DSPI B. Finally, some channels are serialized through different DSPIs. The eTPU channel 17 is serialized through DSPI B to input 1 on IMUX for external $\overline{\text{IRQ}}$[6], but is also serialized by DSPI D to input 3 on IMUX for external $\overline{\text{IRQ}}$[2].

Figure 20-22, Figure 20-23, and Figure 20-24 along with Table 20-20, Table 20-21, and Table 20-22 explain the serial connectivities of the eTPU and eMIOS channels.

The following table lists the eTPU B channel connections:

Table 18-1. eTPU B Channel Connection Table

eTPU Channel Number	I/O	Pin Number	eTPU Channel Connections	DSPI Serial Channel Connections	eTPU B Signal	Signals with Which eTPU Signal is Shared:
0–7	I	M25, M24, L26, L25, L24, K26, L23, K25	0–7	not connected	eTPU_B[0:7]	eTPU_B[16:23] (output only) GPIO[147:154]
				DSPI A[15:8][1]		
	O	AE19, AD19, AF20, AE20, AF21, AC19, AD20, AF21	0–7			eMIOS[16:23] GPIO[195:202]
8–15	I	K24, J26, K23, J25, J24, H26, H25, G26	8–15	not connected	eTPU_B[8:15]	eTPU_B[24:31] (output only) GPIO[155:162]
	O			DSPI A[7:0][1]		
16–31	I	D16, D17, A17, C16, A18, B17, C17, D18, A19, B18, C18, A20, B19, D19, C19, B20	16–31	not connected	eTPU_B[16:31]	GPIO[163:178]
	O					

[1] The channel numbers for some of the DSPI channels connections are reversed, for example if eTPU_B[0:7] is mapped to DSPI_A[15:8], then eTPU_B[0] is connected to DSPI_A[15], eTPU_B[1] is connected to DSPI_A[14],..., eTPU_B[7] is connected to DSPI_A[8].

18.3.2.1 Time Base Clock Signal (TCRCLKA and TCRCLKB)

The TCRCLKA and TCRCLKB input signals are used to control the TCR1 and TCR2 time bases for eTPU A and eTPU B.

NOTE

Throughout this document, TCRCLKA and TCRCLKB are referred to generically as TCRCLK.

There is an independent TCRCLK input for each eTPU engine. Table 18-2 shows the TCRCLK pin connections.

- For pulse accumulator operations, TCRCLK can be used as a gate for a counter based on the system clock divided by eight.
- For angle operations TCRCLK can be used to get the tooth transition indications in angle mode. Refer to the *eTPU Reference Manual's* Sections 5.9 and 5.10.

Table 18-2. MPC5566 TCRCLK Signals

Signal Name	Pin Assignment	I/O	Pin Connection	
			496 BGA	416 BGA
TCRCLKA_ $\overline{\text{IRQ}}$[7]_ GPIO[113]	Primary Alternate General-purpose I/O	I I I/O	N5	N4
TCRCLKB_ $\overline{\text{IRQ}}$[6]_ GPIO[146]	Primary Alternate General-purpose I/O	I I I/O	K21	M23

18.3.2.2 Channel Output Disable Signals

Each eTPU engine has four input signals that are used to force the outputs of a group of eight channels to an inactive level. These signals originate from the eMIOS. When an output disable signal is active, all eight channels assigned to the disable signal that have their ODIS bits set to one in the ETPU_C*n*CR register have their outputs forced to the opposite of the value specified in the ETPU_C*n*CR[OPOL] bit. Therefore, individual channels can be selected to be affected by the output disable signals, as well as their disabling forced polarity.

Refer to Section 17.2.1.1, "Output Disable Input—eMIOS Output Disable Input Signals," for more information on the output disable signals.

The output disable channel groups are defined in Table 18-3.

Table 18-3. Output Disable Channel Groups

eMIOS Channel	Engine	eTPU Channels Disabled
11	A	0–7
10		8–15
9		16–23
8		24–31
20	B	0–7
21		8–15
22		16–23
23		24–31

18.4 Memory Map and Register Definition

18.4.1 eTPU Memory Map Overview

The eTPU system simplified memory map is shown in Table 18-4. The base address for the eTPU module is listed as BASE. Each of the register areas shown can have their own reserved address areas.

Table 18-4. eTPU High-Level Memory Map

Address	Register Description
Base (C3FC_0000)– Base + 0x0000_001F	eTPU system module configuration registers
Base + (0x0000_0020–0x0000_002F)	eTPU A time base registers
Base + (0x0000_0030–0x0000_003F)	Reserved
Base + (0x0000_0040–0x0000_004F)	eTPU B time base registers
Base + (0x0000_0050–0x0000_01FF)	Reserved
Base + (0x0000_0200–0x0000_02FF)	eTPU A and B global channel registers
Base + (0x0000_0300–0x0000_03FF)	Reserved
Base + (0x0000_0400–0x0000_07FF)	eTPU A channel registers
Base + (0x0000_0800–0x0000_0BFF)	eTPU B channel registers
Base + (0x0000_0C00–0x0000_7FFF)	Reserved
Base + (0x0000_8000–0x0000_8FFF)	Shared data memory (4 KB)
Base + (0x0000_9000–0x0000_BFFF)	Reserved
Base + (0x0000_C000–0x0000_CFFF)	Shared data memory PSE mirror[1] (4 KB)
Base + (0x0000_CD00–0x0000_FFFF)	Reserved

Table 18-4. eTPU High-Level Memory Map (continued)

Address	Register Description
Base + (0x0001_0000–0x0001_4FFF)	Shared code memory (20 KB)
Base + (0x0001_5000–0x0001_FFFF)	Not writable. Reads the return value of ETPU_SCMOFFDATAR register.

[1] Parameter Sign Extension access area. Refer to the *eTPU Reference Manual*.

18.4.2 eTPU Register Addresses

Table 18-5 shows the eTPU registers and their locations, without examples or explanation of how the fields are used. For a complete description of these registers, refer to the *Enhanced Time Processing Unit (eTPU) Reference Manual*. The features are explained in detail there.

Table 18-5. Detailed Memory Map

Address	Register Name	Register Description	Bits
Base = 0xC3FC_0000	ETPU_MCR	eTPU module configuration register	32
Base + 0x0000_0004	ETPU_CDCR	eTPU coherent dual-parameter controller register	32
Base + 0x0000_0008	—	Reserved	—
Base + 0x0000_000C	ETPU_MISCCMPR	eTPU MISC compare register	32
Base + 0x0000_0010	ETPU_SCMOFFDATAR	eTPU SCM off-range data register	32
Base + 0x0000_0014	ETPU_ECR_A	eTPU A engine configuration register	32
Base + 0x0000_0018	ETPU_ECR_B[1]	eTPU B engine configuration register	32
Base + 0x0000_001C	—	Reserved	—
Base + 0x0000_0020	ETPU_TBCR_A	eTPU A time base configuration register	32
Base + 0x0000_0024	ETPU_TB1R_A	eTPU A time base 1	32
Base + 0x0000_0028	ETPU_TB2R_A	eTPU A time base 2	32
Base + 0x0000_002C	ETPU_REDCR_A	eTPU A STAC bus interface configuration register	32
Base + (0x0000_0030–0x0000_003F)	—	Reserved	—
Base + 0x0000_0040	ETPU_TBCR_B[1]	eTPU B time base configuration register	32
Base + 0x0000_0044	ETPU_TB1R_B[1]	eTPU B time base 1	32
Base + 0x0000_0048	ETPU_TB2R_B[1]	eTPU B time base 2	32
Base + 0x0000_004C	ETPU_REDCR_B[1]	eTPU B STAC bus interface configuration register	32
Base + (0x0000_0050–0x0000_01FF)	—	Reserved	—
Base + 0x0000_0200	ETPU_CISR_A	eTPU A channel interrupt status register	32
Base + 0x0000_0204	ETPU_CISR_B[1]	eTPU B channel interrupt status register	32
Base + 0x0000_0208	—	Reserved	—

Table 18-5. Detailed Memory Map (continued)

Address	Register Name	Register Description	Bits
Base + 0x0000_020C	—	Reserved	—
Base + 0x0000_0210	ETPU_CDTRSR_A	eTPU A channel data transfer request status register	32
Base + 0x0000_0214	ETPU_CDTRSR_B[1]	eTPU B channel data transfer request status register	32
Base + 0x0000_0218	—	Reserved	—
Base + 0x0000_021C	—	Reserved	—
Base + 0x0000_0220	ETPU_CIOSR_A	eTPU A channel interrupt overflow status register	32
Base + 0x0000_0224	ETPU_CIOSR_B[1]	eTPU B channel interrupt overflow status register	32
Base + 0x0000_0228	—	Reserved	—
Base + 0x0000_022C	—	Reserved	—
Base + 0x0000_0230	ETPU_CDTROSR_A	eTPU A channel data transfer request overflow status register	32
Base + 0x0000_0234	ETPU_CDTROSR_B[1]	eTPU B channel data transfer request overflow status register	32
Base + 0x0000_0238	—	Reserved	—
Base + 0x0000_023C	—	Reserved	—
Base + 0x0000_0240	ETPU_CIER_A	eTPU A channel interrupt enable register	32
Base + 0x0000_0244	ETPU_CIER_B[1]	eTPU B channel interrupt enable register	32
Base + 0x0000_0248	—	Reserved	—
Base + 0x0000_024C	—	Reserved	—
Base + 0x0000_0250	ETPU_CDTRER_A	eTPU A channel data transfer request enable register	32
Base + 0x0000_0254	ETPU_CDTRER_B[1]	eTPU B channel data transfer request enable register	32
Base + (0x0000_0258–0x0000_027F)	—	Reserved	—
Base + 0x0000_0280	ETPU_CPSSR_A	eTPU A channel pending service status register	32
Base + 0x0000_0284	ETPU_CPSSR_B[1]	eTPU B channel pending service status register	32
Base + 0x0000_0288	—	Reserved	—
Base + 0x0000_028C	—	Reserved	—
Base + 0x0000_0290	ETPU_CSSR_A	eTPU A channel service status register	32
Base + 0x0000_0294	ETPU_CSSR_B[1]	eTPU B channel service status register	32
Base + (0x0000_0298–0x0000_03FF)	—	Reserved	—

Table 18-5. Detailed Memory Map (continued)

Address	Register Name	Register Description	Bits
Base + 0x0000_0400	ETPU_C0CR_A	eTPU A channel 0 configuration register	32
Base + 0x0000_0404	ETPU_C0SCR_A	eTPU A channel 0 status and control register	32
Base + 0x0000_0408	ETPU_C0HSRR_A	eTPU A channel 0 host service request register	32
Base + 0x0000_040C	—	Reserved	—
Base + 0x0000_0410	ETPU_C1CR_A	eTPU A channel 1 configuration register	32
Base + 0x0000_0414	ETPU_C1SCR_A	eTPU A channel 1 status and control register	32
Base + 0x0000_0418	ETPU_C1HSRR_A	eTPU A channel 1 host service request register	32
Base + (0x0000_041C–0x0000_05EF)	—	Reserved	—
Base + 0x0000_05F0	ETPU_C31CR_A	eTPU A channel 31 configuration register	32
Base + 0x0000_05F4	ETPU_C31SCR_A	eTPU A channel 31 status and control register	32
Base + 0x0000_05F8	ETPU_C31HSRR_A	eTPU A channel 31 host service request register	32
Base + (0x0000_05FC–0x0000_07FF)	—	Reserved	—
Base + 0x0000_0800	ETPU_C0CR_B[1]	eTPU B channel 0 configuration register	32
Base + 0x0000_0804	ETPU_C0SCR_B[1]	eTPU B channel 0 status and control register	32
Base + 0x0000_0808	ETPU_C0HSRR_B[1]	eTPU B channel 0 host service request register	32
Base + 0x0000_080C	—	Reserved	—
Base + 0x0000_0810	ETPU_C1CR_B[1]	eTPU B channel 1 configuration register	32
Base + 0x0000_0814	ETPU_C1SCR_B[1]	eTPU B channel 1 status and control register	32
Base + 0x0000_0818	ETPU_C1HSRR_B[1]	eTPU B channel 1 host service request register	32
Base + (0x0000_081C–0x0000_09EC)	—	Reserved	—
Base + 0x0000_09F0	ETPU_C31CR_B[1]	eTPU B channel 31 configuration register	32
Base + 0x0000_09F4	ETPU_C31SCR_B[1]	eTPU B channel 31 status and control register	32
Base + 0x0000_09F8	ETPU_C31HSRR_B[1]	eTPU B Channel 31 host service request register	32
Base + (0x0000_09FC–0x0000_7FFF)	—	Reserved	—
Base + (0x0000_8000–0x0000_8BFF)	SDM	Shared Data Memory (parameter RAM)	4 KB
Base + (0x0000_8C00–0x0000_BFFF)	—	Reserved	—
Base + (0x0000_C000–0x0000_CBFF)	—	SDM PSE mirror[2]	4 KB
Base + (0x0000_CC00–0x0000_FFFF)	—	Reserved	—

Table 18-5. Detailed Memory Map (continued)

Address	Register Name	Register Description	Bits
Base + (0x0001_0000–0x0001_4FFF)	SCM	Shared Code Memory[3]	20 KB
Base + (0x0001_5000–0x0001_FFFF)	—	Reserved	—

1 The register at this address is available only on the MPC5554 and the MPC5566.

2 Parameter sign extension access area. Refer to the *eTPU Reference Manual*.

3 SCM access is only available under certain conditions when ETPU_MCR[VIS] = 1. The SCM can only be written in 32-bit accesses.

18.4.3 System Configuration Registers

18.4.3.1 eTPU Module Configuration Register (ETPU_MCR)

This register is global to both eTPU engines, and resides in the shared BIU. ETPU_MCR gathers global configuration and status in the eTPU system, including global exception. It is also used for configuring the SCM (shared code memory) operation and test.

Address: Base + 0x0000_0000 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	MGEA	MGEB	ILFA	ILFB	0	0	0	SCMSIZE				
W	GEC															
Reset	0	0	0	0	0	0	0	0	0	0	0	SCMSIZE				

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	SCMMISF	SCMMISEN	0	0	VIS	0	0	0	0	0	GTBE
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-5. eTPU Module Configuration Register (ETPU_MCR)

Table 18-6. ETPU_MCR Field Descriptions

Field	Description
0 GEC	Global exception clear. Negates global exception request and clears global exception status bits MGEA, MGEB, ILFA, ILFB and SCMMISF. A read always returns 0. Writes have the following effect: 0 Keep global exception request and status bits ILFA, ILFB, MGEA, MGEB, and SCMMISF as is. 1 Negate global exception, clear status bits ILFA, ILFB, MGEA, MGEB, and SCMMISF. GEC works the same way with either one or both engines in stop mode.
1–3	Reserved

Table 18-6. ETPU_MCR Field Descriptions (continued)

Field	Description
4 MGEA	Microcode global exception engine A. Indicates that a global exception was asserted by microcode executed on the respective engine. The determination of the reason why the global exception was asserted is application dependent: it can be coded in an SDM status parameter, for instance. This bit is cleared by writing 1 to GEC. 0 No microcode-requested global exception pending. 1 Global exception requested by microcode is pending.
5 MGEB	Microcode global exception engine B. Indicates that a global exception was asserted by microcode executed on the respective engine. The determination of the reason why the global exception was asserted is application dependent: it can be coded in an SDM status parameter, for instance. This bit is cleared by writing 1 to GEC. 0 No microcode requested global exception pending. 1 Global exception requested by microcode is pending.
6 ILFA	Illegal instruction flag eTPU A. Set by the microengine to indicate that an illegal instruction was decoded in engine A. This bit is cleared by host writing 1 to GEC. For more information about illegal instructions, refer to Section 9.6 in the *eTPU Reference Manual*. 0 Illegal Instruction not detected. 1 Illegal Instruction detected by eTPU A.
7 ILFB	Illegal instruction flag eTPU B. Set by the microengine to indicate that an illegal instruction was decoded in engine B. This bit is cleared by host writing 1 to GEC. For more details, refer to the *eTPU Reference Manual*. 0 Illegal Instruction not detected. 1 Illegal Instruction detected by eTPU B.
8–10	Reserved
11–15 SCMSIZE [0:4]	SCM size. Holds the number of 2 KB SCM Blocks minus 1. This value is MCU-dependent.
16–20	Reserved
21 SCMMISF	SCM MISC Flag. Set by the SCM MISC (multiple input signature calculator) logic to indicate that the calculated signature does not match the expected value, at the end of a MISC iteration. For more details, refer to the *eTPU Reference Manual* for more details. 0 Signature mismatch not detected. 1 MISC has read entire SCM array and the expected signature in ETPU_MISCCMPR does not match the value calculated. This bit is cleared by writing 1 to GEC.
22 SCM MISEN	SCM MISC enable. Used for enabling/disabling the operation of the MISC logic. SCMMISEN is readable and writable at any time. The MISC logic only operates when this bit is set to 1. When the bit is reset the MISC address counter is set to the initial SCM address. When enabled, the MISC continuously cycles through the SCM addresses, reading each and calculating a CRC. To save power, the MISC can be disabled by clearing the SCMMISEN bit. For more details, refer to the *eTPU Reference Manual*. 0 MISC operation disabled. The MISC logic is reset to its initial state. 1 MISC operation enabled. (Toggling to 1 clears the SCMMISF bit) SCMMISEN is cleared automatically when MISC logic detects an error; that is, when SCMMISF transitions from 0 to 1, disabling the MISC operation.
23–24	Reserved

Table 18-6. ETPU_MCR Field Descriptions (continued)

Field	Description
25 VIS	SCM visibility. Determines SCM visibility to the slave bus interface and resets the MISC state (but SCMMISEN keeps its value). 0 SCM is not visible to the slave bus. Accessing SCM address space issues a bus error. 1 SCM is visible to the slave bus. The MISC state is reset. This bit is write protected when any of the engines are not in halt or stop states. When VIS=1, the ETPU_ECR MDIS bits are write protected, and only 32-bit aligned SCM writes are supported. The value written to SCM is unpredictable if other transfer sizes are used.
26 – 30	Reserved
31 GTBE	Global time base enable. Enables time bases in both engines, allowing them to be started synchronously. An assertion of GTBE also starts the eMIOS time base[1]. This enables the eTPU time bases and the eMIOS time base to all start synchronously. 1 time bases in both eTPU engines and eMIOS are enabled to run. 0 time bases in both engines are disabled to run. **Note:** When GTBE is turned off with Angle Mode enabled, the EAC must be reinitialized before GTBE is turned on again.

1 The eMIOS also has a GTBE bit. Assertion of either the eMIOS or eTPU GTBE bit starts time bases for the eMIOS and eTPU, refer to the *eTPU Reference Manual.*

18.4.3.2 eTPU Coherent Dual-Parameter Controller Register (ETPU_CDCR)

ETPU_CDCR configures and controls dual-parameter coherent transfers. For more information, refer to the *eTPU Reference Manual*.

Address: Base + 0x0000_0004 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	STS			CTBASE					PBBASE							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	PWIDTH			PARM0					WR	PARM1						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 18-6. eTPU Coherent Dual-Parameter Controller Register (ETPU_CDCR)

Table 18-7. ETPU_CDCR Field Descriptions

Field	Description
0 STS	Start. Set by the host to start the data transfer between the parameter buffer pointed by PBBASE and the target addresses selected by the concatenation of fields CTBASE and PARM0/1. The host receives wait-states until the data transfer is complete. Coherency logic resets STS after the data transfer is complete. For more information, refer to the *eTPU Reference Manual*. 0 (Write) does not start a coherent transfer. 1 (Write) starts a coherent transfer.
1–5 CTBASE [0:4]	Channel transfer base. This field concatenates with fields PARM0/PARM1 to determine the absolute offset (from the SDM base) of the parameters to be transferred: Parameter 0 address = {CTBASE, PARM0} × 4 + SDM base Parameter 1 address = {CTBASE, PARM1} × 4 + SDM base
6–15 PBBASE [0:9]	Parameter buffer base address. Points to the base address of the parameter buffer location, with granularity of 2 parameters (8 bytes). The host (byte) address of the first parameter in the buffer is PBBASE × 8 + SDM Base Address.
16 PWIDTH	Parameter width selection. Selects the width of the parameters to be transferred between the PB and the target address. 0 Transfer 24-bit parameters. The upper byte remains unchanged in the destination address. 1 Transfer 32-bit parameters. All 32 bits of the parameters are written in the destination address.
17–23 PARM0 [0:6]	Channel parameter number 0. This field in concatenation with CTBASE[3:0] determine the address offset (from the SDM base address) of the parameter which is the destination or source (defined by WR) of the coherent transfer. The SDM address offset of the parameter is {CTBASE, PARM0}*4. PARM0 allows non-contiguous parameters to be transferred coherently[1].
24 WR	Read/Write selection. This bit selects the direction of the coherent data transfer. 0 Read operation. Data transfer is from the selected parameter RAM address to the PB. 1 Write operation. Data transfer is from the PB to the selected parameter RAM address.
25–31 PARM1 [0:6]	Channel parameter number 1. This field in concatenation with CTBASE[3:0] determines the address offset (from the SDM base) of the parameter which is the destination or source (defined by WR) of the coherent transfer. The SDM address offset of the parameter is {CTBASE, PARM1}*4. PARM1 allows non-contiguous parameters to be transferred coherently[1].

[1] The parameter pointed by {CTBASE, PARM0} is the first transferred.

18.4.3.3 eTPU MISC Compare Register (ETPU_MISCCMPR)

The multiple input signature calculator compare register (ETPU_MISCCMPR) holds the 32-bit signature expected from the whole shared code memory (SCM) array. This register must be written by the host with the 32-bit word to be compared against the calculated signature at the end of the MISC cycle. This register is global to both eTPU engines. For more details, refer to the *eTPU Reference Manual*.

Address: Base + 0x0000_000C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	EMISCCMP															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	EMISCCMP															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-7. eTPU MISC Compare Register (ETPU_MISCCMPR)

Table 18-8. ETPU_MISCCMPR Field Descriptions

Field	Description
0–31 EMISCCMP [0:31]	Expected multiple input signature calculator compare register value. For more information, refer to the *eTPU Reference Manual*.

18.4.3.4 eTPU SCM Off-Range Data Register (ETPU_SCMOFFDATAR)

ETPU_SCMOFFDATAR holds the 32-bit value returned when the SCM array is accessed at non implemented addresses, either by the host or by the microengine. This register can be written by the host with the 32-bit instruction to be executed by the microengine to recover from runaway code. This register is global to both ETPU engines.

NOTE

The ETPU_SCMOFFDATAR reset value is the opcode of an instruction that disables matches, clears the TDLs and the MRLs; the opcode also issues an illegal instruction Global Exception, and ends the thread.

Address: Base + 0x0000_0010 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	ETPUSCMOFFDATAR[0:15]															
Reset	1	1	1	1	0	0	1	1	0	1	1	1	0	1	1	1

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	ETPUSCMOFFDATAR[16:31]															
Reset	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1

Figure 18-8. eTPU SCM Off-Range Data Register (ETPU_SCMOFFDATAR)

Table 18-9. ETPU_SCMOFFDATAR Field Descriptions

Field	Description
0–31 ETPU SCMOFF DATA	SCM Off-range read data value.

18.4.3.5 eTPU Engine Configuration Register (ETPU_ECR)

Each engine has its own ETPU_ECR. The ETPU_ECR holds configuration and status fields that are programmed independently in each engine.

Address: Base + 0x0000_0014 (eTPU A)
Address: Base + 0x0000_0018 (eTPU B) Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	FEND	MDIS	0	STF	0	0	0	0	HLTF	0	0	0	0	FPSCK		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	CDFC		0	0	0	0	0	0	0	0	0	ETB				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-9. eTPU Engine Configuration Register (ETPU_ECR)

Table 18-10. ETPU_ECR Field Descriptions

Field	Description
0 FEND	Force end. Assertion terminates any current running thread as if an END instruction have been executed. For more information, refer to the *eTPU Reference Manual*. 0 Normal operation. 1 Terminates current thread. This bit is self-negating.
1 MDIS	Module disable internal stop. This is the low power stop bit. When MDIS is set, the engine shuts down its internal clocks. TCR1 and TCR2 cease to increment, and input sampling stops. The engine asserts the stop flag (STF) bit to indicate that it has stopped. However, the BIU continues to run, and the host can access all registers except for the channel registers[1] and writes to time base registers. For more information on channel registers, refer to Section 18.4.6, "Channel Configuration and Control Registers." After MDIS is set, even before STF asserts, data read from the channel registers is not meaningful, a Bus Error is issued, and writes are unpredictable. When the MDIS bit is asserted while the microcode is executing, the eTPU stops when the thread is complete. 0 eTPU engine runs. 1 Commands engine to stop its clocks. Stop completes on the next system clock after the stop condition is valid. The MDIS bit is write-protected when ETPU_MCR[VIS]=1. **Note:** After the MDIS has been switched from 1 to 0 or vice-versa, do not switch its value again until STF switches to the same value.
2	Reserved
3 STF	Stop flag bit. Each engine asserts its stop flag (STF) to indicate that it has stopped. Only then the host can assume that the engine has actually stopped. The eTPU system is fully stopped when the STF bits of both eTPU engines are asserted. The engine only stops when any ongoing thread is complete in this case. 0 The engine is operating. 1 The engine has stopped (after the local MDIS bit has been asserted). Summarizing engine stop conditions, which STF reflects: STF_A:= (after stop completed) MDIS_A STF_B:= (after stop completed) MDIS_B STF_A and STF_B mean STF bit from engine A and STF bit from engine B respectively.
4–7	Reserved
8 HLTF	Halt mode flag. If eTPU engine entered halt state, this flag is asserted. The flag remains asserted while the microengine is in halt state, even during a single-step or forced instruction execution. Refer to the *eTPU Reference Manual* for further details about entering halt mode. 0 eTPU engine is not halted. 1 eTPU engine is halted
9–12	Reserved

Table 18-10. ETPU_ECR Field Descriptions (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>13–15
FPSCK
[0:2]</td><td>Filter prescaler clock control. Controls the prescaling of the clocks used in digital filters for the channel input signals and TCRCLK input. The following table illustrates filter prescaler clock control.
<table>
<tr><th>Filter Control</th><th>Sample on System Clock Divided by:</th></tr>
<tr><td>000</td><td>2</td></tr>
<tr><td>001</td><td>4</td></tr>
<tr><td>010</td><td>8</td></tr>
<tr><td>011</td><td>16</td></tr>
<tr><td>100</td><td>32</td></tr>
<tr><td>101</td><td>64</td></tr>
<tr><td>110</td><td>128</td></tr>
<tr><td>111</td><td>256</td></tr>
</table>
Filtering can be controlled independently by the engine, but all input digital filters in the same engine have same clock prescaling. For more details, refer to the eTPU Reference Manual</td></tr>
<tr><td>16–17
CDFC
[0:1]</td><td>Channel digital filter control. Select a digital filtering mode for the channels when configured as inputs for improved noise immunity. Channel digital filter control is illustrated in the following table.
<table>
<tr><th>CDFC</th><th>Selected Digital Filter</th></tr>
<tr><td>00</td><td>TPU2/3 two sample mode: Using the filter clock which is the system clock divided by (2, 4, 8,..., 256) as a sampling clock (selected by FPSCK field in ETPU_ECR), comparing two consecutive samples which agree with each other sets the input signal state. This is the default reset state.</td></tr>
<tr><td>01</td><td>Invalid value.</td></tr>
<tr><td>10</td><td>eTPU three sample mode: Similar to the TPU2/3 two sample mode, but comparing three consecutive samples which agree with each other sets the input signal state.</td></tr>
<tr><td>11</td><td>eTPU continuous mode: Signal needs to be stable for the whole filter clock period. This mode compares all the values at the rate of system clock divided by two, between two consecutive filter clock pulses. If all the values agree with each other, input signal state is updated.</td></tr>
</table>
The eTPU has three digital filtering modes for the channels which provide programmable trade-off between signal latency and noise immunity. For more information on filtering, refer to the eTPU Reference Manual. Changing CDFC during eTPU normal input channel operation is not recommended since it changes the behavior of the transition detection logic while executing its operation.</td></tr>
</table>

Table 18-10. ETPU_ECR Field Descriptions (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>18–26</td><td>Reserved</td></tr>
<tr><td>27–31
ETB
[0:4]</td><td>Entry table base. Determines the location of the microcode entry table for the eTPU functions in SCM. More information about entry points is located in the eTPU Reference Manual. The following table shows the entry table base address options.
<table>
<tr><th>ETB</th><th>Entry Table Base Address for CPU Host Address (byte format)</th><th>Entry Table Base Address for Microcode Address (word format)</th></tr>
<tr><td>00000</td><td>0x0000_0000</td><td>0x0000_0000</td></tr>
<tr><td>00001</td><td>0x0000_0800</td><td>0x0000_0200</td></tr>
<tr><td>00010</td><td>0x0000_1000</td><td>0x0000_0400</td></tr>
<tr><td>.
.
.
.</td><td>.
.
.
.</td><td>.
.
.
.</td></tr>
<tr><td>11110</td><td>0x0000_F000</td><td>0x0000_3C00</td></tr>
<tr><td>11111</td><td>0x0000_F800</td><td>0x0000_3E00</td></tr>
</table></td></tr>
</table>

[1] The time base registers can still be read in stop mode, but writes are ineffective and a bus error is issued. Global channel registers and SDM can be accessed normally.

18.4.4 Time Base Registers

Time base registers allow the configuration and visibility of internally-generated time bases TCR1 and TCR2. There is one of each of these registers for each eTPU engine.

NOTE

Writes to this register generate a bus error and are ineffective when MDIS = 1. Reads are always permitted.

18.4.4.1 eTPU Time Base Configuration Register (ETPU_TBCR)

This register configures several time base options.

Address: Base + 0x0000_0020 (eTPU A)
Address: Base + 0x0000_0040 (eTPU B)

Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	TCR2CTL			TCRCF		0	AM	0	0	0	TCR2P					
W																
Reset	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	TCR1CTL		0	0	0	0	0	0	TCR1P							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-10. eTPU Time Base Configuration Register (ETPU_TBCR)

NOTE

The MPC5566 has two eTPU engines, each with a dedicated TCRCLK signal: TCRCLKA and TCRCLKB.

Table 18-11. ETPU_TBCR Field Descriptions

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>0–2
TCR2CTL</td><td>TCR2 clock and gate control are part of the TCR2 clocking system. These bits determine the clock source for TCR2 before the prescaler. TCR2 can count on any detected edge of the TCRCLK signal or use it for gating the system clock divided by 8. After reset, the TCRCLK signal rising edge is selected. TCR2 can also be clocked by the system clock divided by 8. TCR2CTL also determines the TCRCLK edge selected for angle tooth detection in angle mode. Refer to the eTPU Reference Manual for more information. TCR2 clock sources are listed in the following table.
<table>
<tr><th>TCR2CTL</th><th>AM = 0
(TCR2 Clock)</th><th>AM = 1
(Angle Tooth Detection)</th></tr>
<tr><td>000</td><td>Gated DIV8 clock (system clock / 8). When the external TCRCLK signal is low, the DIV8 clock is blocked, preventing it from incrementing the TCR2 prescaler. When the external TCRCLK signal is high, TCR2 prescaler is incremented at the frequency of the system clock divided by 8.</td><td>Do not use with angle mode (AM = 1).</td></tr>
<tr><td>001</td><td>Rise transition on TCRCLK signal increments TCR2 prescaler.</td><td>Rising edge</td></tr>
<tr><td>010</td><td>Fall transition on TCRCLK signal increments TCR2 prescaler.</td><td>Falling edge</td></tr>
<tr><td>011</td><td>Rise or fall transition on TCRCLK signal increments TCR2 prescaler.</td><td>Rising or falling edge</td></tr>
<tr><td>100</td><td>DIV8 clock (system clock / 8).</td><td>Do not use with angle mode (AM = 1).</td></tr>
<tr><td>101</td><td>Peripheral timebase clock source.</td><td>Do not use with angle mode (AM = 1).</td></tr>
<tr><td>110</td><td>Do not use with angle mode (AM = 0).</td><td>No edge</td></tr>
<tr><td>111</td><td>TCR2CTL shuts down TCR2 clocking, except as a STAC client.</td><td>Do not use with angle mode (AM = 1).</td></tr>
</table></td></tr>
<tr><td>3–4
TCRCF</td><td>TCRCLK signal filter control. Controls the TCRCLK digital filter determining whether the TCRCLK signal input (after a synchronizer) is filtered with the same filter clock as the channel input signals or uses the system clock divided by 2, and also whether the TCRCLK digital filter works in integrator mode or two sample mode. The following table describes TCRCLK filter clock/mode.
<table>
<tr><th>TCRCF</th><th>Filter Input</th><th>Filter Mode</th></tr>
<tr><td>00</td><td>System clock divided by 2</td><td>Two sample</td></tr>
<tr><td>01</td><td>Filter clock of the channels</td><td>Two sample</td></tr>
<tr><td>10</td><td>System clock divided by 2</td><td>Integration</td></tr>
<tr><td>11</td><td>Filter clock of the channels</td><td>Integration</td></tr>
</table>
For more information, refer to the eTPU Reference Manual.</td></tr>
<tr><td>5</td><td>Reserved</td></tr>
</table>

Table 18-11. ETPU_TBCR Field Descriptions (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>6
AM</td><td>Angle mode selection. When the AM bit is set and neither TCR1 nor TCR2 are STAC interface clients, the EAC (eTPU Angle Clock) hardware provides angle information to the channels using the TCR2 bus. When the AM bit is cleared (non-angle mode), EAC operation is disabled, and its internal registers can be used as general purpose registers.
0 EAC operation is disabled.
1 TCR2 works in angle mode;
• if TCR2 is not a STAC client, the EAC works and stores tooth counter and angle tick counter data in TCR2.
• If TCR1 or TCR2 is a STAC bus client, EAC operation is forbidden. Therefore, if AM is set, the angle logic does not work properly.
Note: AM must not be changed when ETPU_MCR[GTBE] = 1.
Note: Changing AM can cause expurious transition detections on channel 0, depending on the channel mode and state.
For more information, refer to the eTPU Reference Manual.</td></tr>
<tr><td>7–9</td><td>Reserved</td></tr>
<tr><td>10–15
TCR2P</td><td>Timer count register 2 prescaler control. Part of the TCR2 clocking system. TCR2 is clocked from the output of a prescaler. The prescaler divides its input by (TCR2P+1) allowing frequency divisions from 1 to 64. The prescaler input is the system clock divided by 8 (in gated or non-gated clock mode) or Internal Timebase input, or TCRCLK filtered input. This field has no effect on TCCR2 in Angle Mode. For more information on TCR2, refer to the eTPU Reference Manual.</td></tr>
<tr><td>16–17
TCR1CTL</td><td>TCR1 clock/gate control. Part of the TCR1 clocking system. It determines the clock source for TCR1. TCR1 can count on detected rising edge of the TCRCLK signal or the system clock divided by 2. After reset TCRCLK signal is selected. The following table shows the selection of the TCR1 clock source.
<table>
<tr><th>TCR1CTL</th><th>TCR1 Clock</th></tr>
<tr><td>00</td><td>selects TCRCLK as clock source for the TCR1 prescaler (must not be use in Angle Mode)</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>10</td><td>selects system clock divided by 2 as clock source for the TCR1 prescaler</td></tr>
<tr><td>11</td><td>TCR1CTL shuts down TCR1 clock. TCR1 can still change if STAC client.</td></tr>
</table>
For more information on the TCR1 clocking system, refer to the eTPU Reference Manual.</td></tr>
<tr><td>18–23</td><td>Reserved.</td></tr>
<tr><td>24–31
TCR1P</td><td>Timer count register 1 prescaler control. Clocked from the output of a prescaler. The input to the prescaler is the internal eTPU system clock divided by 2 or the output of TCRCLK filter, or Peripheral Timebase input. The prescaler divides this input by (TCR1P+1) allowing frequency divisions from 1 up to 256.</td></tr>
</table>

18.4.4.2 eTPU Time Base 1 (TCR1) Visibility Register (ETPU_TB1R)

This register provides visibility of the TCR1 time base for core host read access. This register is read-only. The value of the TCR1 time base shown can be driven by the TCR1 counter or imported, depending on the configuration set in ETPU_REDCR. For more information, refer to the *eTPU Reference Manual*.

Address: Base + 0x0000_0024 (eTPU A)
Address: Base + 0x0000_0044 (eTPU B)

Access: R/O

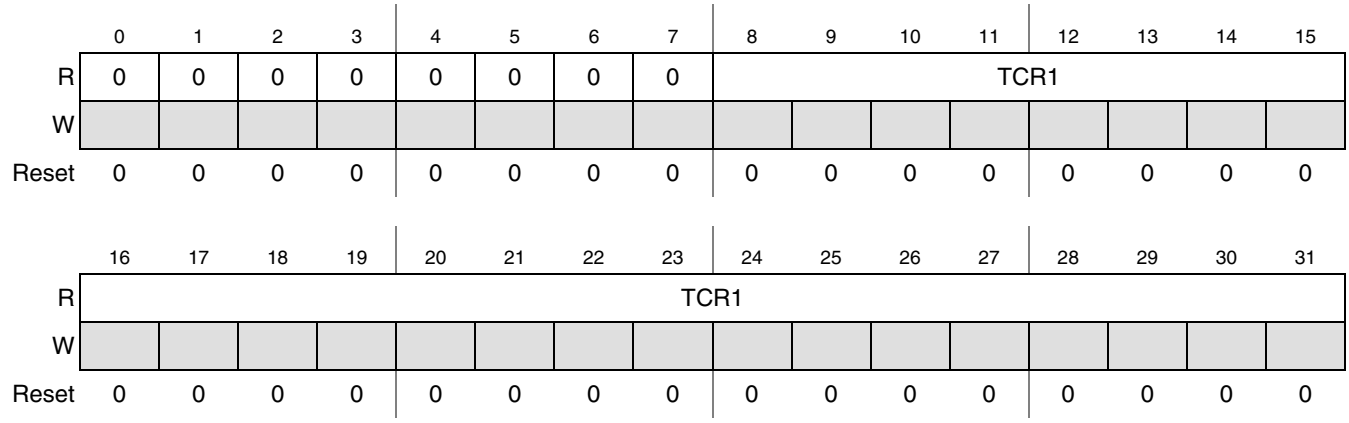


Figure 18-11. eTPU Time Base 1 (TCR1) Visibility Register (ETPU_TB1R)

Table 18-12. ETPU_TB1R Field Descriptions

Field	Description
0–7	Reserved
8–31 TCR1 [0:23]	TCR1 value. Used on matches and captures. For more information, refer to the *eTPU Reference Manual*.

18.4.4.3 eTPU Time Base 2 (TCR2) Visibility Register (ETPU_TB2R)

This register provides visibility of the TCR2 time base for core host read access. This register is read-only. The value of the TCR2 time base shown can be driven by the TCR2 counter, the angle mode logic, or imported from the STAC interface, depending on angle mode (an engine cannot import when in angle mode) and STAC interface configurations set in registers ETPU_TBCR and ETPU_REDCR. For more information on time bases, refer to the *eTPU Reference Manual*.

Address: Base + 0x0000_0028 (eTPU A)
Address: Base + 0x0000_0048 (eTPU B)

Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	TCR2							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	TCR2															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-12. eTPU Time Base 2 (TCR2) Visibility Register (ETPU_TB2R)

Table 18-13. ETPU_TB2R Bit Field Descriptions

Field	Description
0–7	Reserved
8–31 TCR2 [0:23]	TCR2 value. Used on matches and captures. For information on TCR2, refer to the *eTPU Reference Manual*.

18.4.4.4 STAC Bus Configuration Register (ETPU_REDCR)

This register configures the eTPU STAC bus interface module and operation. For more information on the STAC interface, refer to the *eTPU Reference Manual*.

Address: Base + 0x0000_002C (eTPU A)
Address: Base + 0x0000_004C (eTPU B)

Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	REN1	RSC1	0	0	SERVER_ID1				0	0	0	0	SRV1			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	REN2	RSC2	0	0	SERVER_ID2				0	0	0	0	SRV2			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-13. STAC Bus Configuration Register (ETPU_REDCR)

Table 18-14. ETPU_REDCR Field Descriptions

Field	Description
0 REN1	TCR1 resource[1] client/server operation enable. Enables or disables client/server operation for the eTPU STAC interface. REN1 enables TCR1. 0 Server/client operation for resource 1 is disabled. 1 Server/client operation for resource 1 is enabled.
1 RSC1	TCR1 resource server/client assignment. Selects the eTPU data resource assignment to be used as a server or client. RSC1 selects the functionality of TCR1. For server mode, external plugging determines the unique server address assigned to each TCR. For a client mode, the SRV1 field determines the server address to which the client listens. 0 Resource client operation. 1 Resource server operation.
2–3	Reserved
4–7 SERVER_ID1	STAC bus address for TCR1 as a server. For more information on the STAC interface, refer to the *eTPU Reference Manual*.
8–11	Reserved
12–15 SRV1 [0:3]	TCR1 resource server. Selects the address of the specific STAC Server the local TCR1 listens to when configured as a STAC client. For more information on the STAC interface, refer to the *eTPU Reference Manual*.
16 REN2	TCR2 resource[1] client/server operation enable. Enables or disables client/server operation for eTPU slave resources. REN2 enables TCR2 slave bus operations. 1 Server/client operation for resource 2 is enabled. 0 Server/client operation for resource 2 is disabled.

Table 18-14. ETPU_REDCR Field Descriptions (continued)

Field	Description
17 RSC2	TCR2[2] resource server/client assignment. Selects the eTPU data resource assignment to be used as a server or client. RSC2 selects the functionality of TCR2. For server mode, external plugging determines the unique server address assigned to each TCR. For a client mode, the SRV2 field determines the Server address to which the client listens. 0 Resource Client operation. 1 Resource Server operation.
18–19	Reserved
20–23 SERVER_ID2	STAC bus address for TCR2 as a server.
24–27	Reserved
28–31 SRV2 [0:3]	TCR2 resource server. Selects the address of the specific STAC server the local TCR2 listens to when configured as a STAC Client. For more information on the STAC interface, refer to the *eTPU Reference Manual*.

[1] Resource identifies any parameter that changes in time and can be exported / imported from other device. For the eTPU, a resource can be TCR1 or TCR2 (either time or angle values).

[2] When TCR2 is configured as a STAC bus client (REN2 = 1, RSC2 = 0) the angle clock hardware must be disabled (ETPU_TBCR[AM] = 0).

18.4.5 Global Channel Registers

The registers in this section group, by type, the interrupt status and enable bits from all the channels. This organization eases management of all channels or groups of channels by a single interrupt handler routine. These bits are mirrored by the individual channel registers.

18.4.5.1 eTPU Channel Interrupt Status Register (ETPU_CISR)

Host interrupt status from all channels are grouped in ETPU_CISR. The bits are mirrored by the channels' status/control registers. For more information, refer to Section 18.4.6.3, "eTPU Channel n Status Control Register (ETPU_CnSCR)," and the *eTPU Reference Manual*.

NOTE

The host core must write 1 to clear (w1c) an interrupt status bit.

Address: Base + 0x0000_0200 (eTPU A)
Address: Base + 0x0000_0204 (eTPU B)

Access: R/W1c

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	CIS31	CIS30	CIS29	CIS28	CIS27	CIS26	CIS25	CIS24	CIS23	CIS22	CIS21	CIS20	CIS19	CIS18	CIS17	CIS16
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	CIS15	CIS14	CIS13	CIS12	CIS11	CIS10	CIS9	CIS8	CIS7	CIS6	CIS5	CIS4	CIS3	CIS2	CIS1	CIS0
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-14. eTPU Channel Interrupt Status Register (ETPU_CISR)

Table 18-15. ETPU_CISR Field Descriptions

Field	Description
0–31 CIS*n*	Channel *n* interrupt status. 0 indicates that channel *n* has no pending interrupt to the host core. 1 indicates that channel *n* has a pending interrupt to the host core. To clear a status bit, the host must write 1 to it. For details about interrupts refer to the *eTPU Reference Manual*.

18.4.5.2 eTPU Channel Data Transfer Request Status Register (ETPU_CDTRSR)

Data transfer request status from all channels are grouped in ETPU_CDTRSR. The bits are mirrored by the channels' status/control registers. For more information on data transfers and channel control registers, refer to the *eTPU Reference Manual*.

In the MPC5566, eTPU A channels [0:2,12:15,28:29] and eTPU B channels [0:3,12:15,28:31] are connected to the DMA. The data transfer request lines that are not connected to the DMA controller are not connected and do not generate transfer requests, even if their request status bits are asserted in registers ETPU_CDTRSR and ETPU_C*n*SCR. Channels that are not connected can still have their status bits (DTRS*n*) cleared by writing a 1 to the appropriate field.

Address: Base + 0x0000_0210 (eTPU A)
Address: Base + 0x0000_0214 (eTPU B)

Access: R/W1c

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	DTRS 31	DTRS 30	DTRS 29	DTRS 28	DTRS 27	DTRS 26	DTRS 25	DTRS 24	DTRS 23	DTRS 22	DTRS 21	DTRS 20	DTRS 19	DTRS 18	DTRS 17	DTRS 16
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	DTRS 15	DTRS 14	DTRS 13	DTRS 12	DTRS 11	DTRS 10	DTRS 9	DTRS 8	DTRS 7	DTRS 6	DTRS 5	DTRS 4	DTRS 3	DTRS 2	DTRS 1	DTRS 0
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-15. eTPU Channel Data Transfer Request Status Register (ETPU_CDTRSR)

Table 18-16. ETPU_CDTRSR Field Descriptions

Field	Description
0–31 DTRS*n*	Channel *n* data transfer request status. 0 Indicates that channel *n* has no pending data transfer request. 1 Indicates that channel *n* has a pending data transfer request. To clear a status bit, the host must write 1 to it. For details about data transfer requests refer to the *eTPU Reference Manual*.

18.4.5.3 eTPU Channel Interrupt Overflow Status Register (ETPU_CIOSR)

An interrupt overflow occurs when an interrupt is issued for a channel when the previous interrupt status bit for the same channel has not been cleared. Interrupt overflow status from all channels are grouped in ETPU_CIOSR. The bits are mirrored by the channels' status/control registers. For information about channel status registers and overflow, refer to Section 18.4.6.3, "eTPU Channel n Status Control Register (ETPU_CnSCR)," and the *eTPU Reference Manual*.

NOTE

The host must write 1 to clear an interrupt overflow status bit.

Address: Base + 0x0000_0220 (eTPU A)
Address: Base + 0x0000_0224 (eTPU B)

Access: R/W1c

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	CIOS 31	CIOS 30	CIOS 29	CIOS 28	CIOS 27	CIOS 26	CIOS 25	CIOS 24	CIOS 23	CIOS 22	CIOS 21	CIOS 20	CIOS 19	CIOS 18	CIOS 17	CIOS 16
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	CIOS 15	CIOS 14	CIOS 13	CIOS 12	CIOS 11	CIOS 10	CIOS 9	CIOS 8	CIOS 7	CIOS 6	CIOS 5	CIOS 4	CIOS 3	CIOS 2	CIOS 1	CIOS 0
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-16. eTPU Channel Interrupt Overflow Status Register (ETPU_CIOSR)

Table 18-17. ETPU_CIOSR Field Descriptions

Field	Description
0–31 CIOS*n*	Channel *n* interrupt overflow status. 0 indicates that no interrupt overflow occurred in the channel. 1 indicates that an interrupt overflow occurred in the channel. To clear a status bit, the host must write 1 to it. For details about interrupts refer to the *eTPU Reference Manual*.

18.4.5.4 eTPU Channel Data Transfer Request Overflow Status Register (ETPU_CDTROSR)

Data transfer request overflow status from all channels are grouped in ETPU_CDTROSR. The bits are mirrored by the channels' status/control registers. For more information on channel status registers and data transfer request overflow, refer to Section 18.4.6.3, "eTPU Channel n Status Control Register (ETPU_CnSCR)," and the *eTPU Reference Manual*.

NOTE

The host must write 1 to clear a data transfer request overflow status bit.

Address: Base + 0x0000_0230 (eTPU A)
Address: Base + 0x0000_0234 (eTPU B)

Access: R/W1c

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	DTR OS31	DTR OS30	DTR OS29	DTR OS28	DTR OS27	DTR OS26	DTR OS25	DTR OS24	DTR OS23	DTR OS22	DTR OS21	DTR OS20	DTR OS19	DTR OS18	DTR OS17	DTR OS16
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	DTR OS15	DTR OS14	DTR OS13	DTR OS12	DTR OS11	DTR OS10	DTR OS9	DTR OS8	DTR OS7	DTR OS6	DTR OS5	DTR OS4	DTR OS3	DTR OS2	DTR OS1	DTR OS0
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-17. eTPU Channel Data Transfer Request Overflow Status Register (ETPU_CDTROSR)

Table 18-18. ETPU_CDTROSR Field Descriptions

Field	Description
0–31 DTROS*n*	Channel *n* data transfer request overflow status. 0 indicates that no data transfer request overflow occurred in the channel 1 indicates that a data transfer request overflow occurred in the channel. To clear a status bit, the host must write 1 to it. For details about data transfer request overflow, refer to the *eTPU Reference Manual*.

18.4.5.5 eTPU Channel Interrupt Enable Register (ETPU_CIER)

The host interrupt enable bits for all 32 channels are grouped in ETPU_CIER. The bits are mirrored by the channel configuration registers. For more information on channel configuration registers and interrupt enable, refer to Section 18.4.6.2, “eTPU Channel n Configuration Register (ETPU_CnCR),” and the *eTPU Reference Manual*.

Address: Base + 0x0000_0240 (eTPU A)
Address: Base + 0x0000_0244 (eTPU B)

Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	CIE 31	CIE 30	CIE 29	CIE 28	CIE 27	CIE 26	CIE 25	CIE 24	CIE 23	CIE 22	CIE 21	CIE 20	CIE 19	CIE 18	CIE 17	CIE 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	CIE 15	CIE 14	CIE 13	CIE 12	CIE 11	CIE 10	CIE 9	CIE 8	CIE 7	CIE 6	CIE 5	CIE 4	CIE 3	CIE 2	CIE 1	CIE 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-18. eTPU Channel Interrupt Enable Register (ETPU_CIER)

Table 18-19. ETPU_CIER Field Descriptions

Field	Description
0–31 CIE*n*	Channel *n* interrupt enable. Enable the eTPU channels to interrupt the MPC5566 core. 0 Interrupt disabled for channel *n*. 1 Interrupt enabled for channel *n* For details about interrupts refer to the *eTPU Reference Manual*.

18.4.5.6 eTPU Channel Data Transfer Request Enable Register (ETPU_CDTRER)

Data transfer request enable status bits from all channels are grouped in ETPU_CDTRER. The bits are mirrored in the channels' configuration registers. For more on configuration registers and data transfer request enable, refer to Section 18.4.6.2, "eTPU Channel n Configuration Register (ETPU_CnCR)," and the *eTPU Reference Manual*.

Address: Base + 0x0000_0250 (eTPU A)
Address: Base + 0x0000_0254 (eTPU B)

Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	DTRE 31	DTRE 30	DTRE 29	DTRE 28	DTRE 27	DTRE 26	DTRE 25	DTRE 24	DTRE 23	DTRE 22	DTRE 21	DTRE 20	DTRE 19	DTRE 18	DTRE 17	DTRE 16
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	DTRE 15	DTRE 14	DTRE 13	DTRE 12	DTRE 11	DTRE 10	DTRE 9	DTRE 8	DTRE 7	DTRE 6	DTRE 5	DTRE 4	DTRE 3	DTRE 2	DTRE 1	DTRE 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-19. eTPU Channel Data Transfer Request Enable Register (ETPU_CDTRER)

Table 18-20. ETPU_CDTRER Field Descriptions

Field	Description
0–31 DTRE*n*	Channel *n* data transfer request enable. Enable data transfer requests for their respective channels. 0 Data transfer request disabled for channel *n*. 1 Data transfer request enabled for channel *n*. For details about interrupts refer to the *eTPU Reference Manual*.

18.4.5.7 eTPU Channel Pending Service Status Register (ETPU_CPSSR)

ETPU_CPSSR is a read-only register that holds the status of the pending channel service requests. For information on channel service requests, refer to the *eTPU Reference Manual*.

NOTE

More than one source can request service when a channel's service request bit is set.

Address: Base + 0x0000_0280 (eTPU A)
Address: Base + 0x0000_0284 (eTPU B)

Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	SR31	SR30	SR29	SR28	SR27	SR26	SR25	SR24	SR23	SR22	SR21	SR20	SR19	SR18	SR17	SR16
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-20. eTPU Channel Pending Service Status Register (ETPU_CPSSR)

Table 18-21. ETPU_CPSSR Bit Field Descriptions

Field	Description
0–31 SR*n*	Pending service request *n*. Indicates a pending service request for channel *n*. The SR status for the pending request is negated at the time slot transition for the respective service thread. 0 no service request pending for channel *n* 1 pending service request for channel *n*

NOTE

The pending service status bit for a channel is set when a service request is pending, even if the Channel is disabled (CPR*n* = 0).

18.4.5.8 eTPU Channel Service Status Register (ETPU_CSSR)

ETPU_CSSR holds the current channel service status on whether it is being serviced or not. Only one bit can be asserted in this register at a given time. When no channel is being serviced, the register read value is 0x0000_0000. ETPU_CSSR is a read-only register. This register can be read during normal eTPU operation for monitoring the scheduler activity. For more information on channels being serviced, refer to the *eTPU Reference Manual*.

NOTE

The ETPU_CSSR is not an absolute indication of channel status. If more than one source is requesting service, the asserted status bit only indicates that one of the requests has been granted.

NOTE

Channel service status does not always reflect decoding of the CHAN register, since the CHAN register can be changed by the service thread microcode.

Address: Base + 0x0000_0290 (eTPU A)
Address: Base + 0x0000_0294 (eTPU B)

Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	SS31	SS30	SS29	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20	SS19	SS18	SS17	SS16
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	SS15	SS14	SS13	SS12	SS11	SS10	SS9	SS8	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-21. ETPU_CSSR Register

Table 18-22. ETPU_CSSR Field Descriptions

Field	Description
0–31 SS*n*	Service status *n*. Indicates that channel *n* is currently being serviced. It is updated at the 1st microcycle of a time slot transition. 0 channel *n* is not currently being serviced 1 channel *n* is currently being serviced Refer to the *eTPU Reference Manual* for more information on time slot transitions.

18.4.6 Channel Configuration and Control Registers

Each channel, for both eTPU engines, has a group of three registers used to control, configure and check status of that channel as shown in Table 18-23.

Table 18-23. Channel Registers Structure

Channel Offset	Register Name
0x0000	eTPU channel configuration register (ETPU_C*n*CR)
0x0004	eTPU channel status/control register[1] (ETPU_C*n*SCR)
0x0008	eTPU channel host service request register (ETPU_C*n*HSRR)
0x000C	Reserved

[1] In the MPC5566, eTPU A channels [0:2,12:15,28:29] and eTPU B channels [0:3,12:15,28:31] are connected to the DMA. The data transfer request lines that are not connected to the DMA controller are left disconnected and do not generate interrupt requests, even if their request status bits assert in registers ETPU_CDTRSR and ETPU_C*n*SCR.

18.4.6.1 Channel Registers Layout

One contiguous area is used to map all channel registers of each eTPU engine as shown in Table 18-24.

Table 18-24. eTPU Channel Register Map

Address	Registers Structure
Base + 0x0000_0400	eTPU A channel 0 register structure
Base + 0x0000_0410	eTPU A channel 1 register structure
Base + 0x0000_0420	eTPU A channel 2 register structure
Base + (0x0000_0430–0x0000_05D0)	. . .
Base + 0x0000_05E0	eTPU A channel 30 register structure
Base + 0x0000_05F0	eTPU A channel 31 register structure
Base + (0x0000_0600–0x0000_07FF)	Reserved
Base + 0x0000_0800	eTPU B channel 0 register structure
Base + 0x0000_0810	eTPU B channel 1 register structure
Base + 0x0000_0820	eTPU B channel 2 register structure
Base + (0x0000_0830–0x0000_09D0)	. . .
Base + 0x0000_09E0	eTPU B channel 30 register structure
Base + 0x0000_09F0	eTPU B channel 31 register structure
Base + (0x0000_00A0–0x0000_0BFF)	Reserved

There are 64 structures defined, one for each available channel in the eTPU System (32 for each engine). The base address for the structure presented can be calculated by using the following equation:

$$Channel\_Register\_Structure\_Base\_Address = ETPU\_Engine\_Channel\_Base + (channel\_number \times 0x0000\_0010)$$

where:

$$ETPU\_Engine\_Channel\_Base = ETPU\_Base + ((0x0000\_0400 = ETPU\ A) \text{ or } (0x0000\_0800 = ETPU\ B))$$

18.4.6.2 eTPU Channel *n* Configuration Register (ETPU_C*n*CR)

The ETPU_C*n*CR is a collection of the configuration bits related to an individual channel. Some of these bits are mirrored from the global channel registers.

Address: Channel_Register_Base + 0x0000 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	CIE	DTRE	CPR		0	0	ETPD[1]	ETCS	0	0	0	CFS				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	ODIS	OPOL	0	0	0	CPBA										
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[1] ETPD is not available on the MPC5566.

Figure 18-22. ETPU Channel *n* Configuration Register (ETPU_C*n*CR)

Table 18-25. ETPU_C*n*CR Field Descriptions

Field	Description
0 CIE	Channel interrupt enable. This bit is mirrored from the ETPU_CIER 0 Disable interrupt for this channel.For more information, refer to the *eTPU Reference Manual*. 1 Enable interrupt for this channel.
1 DTRE	Channel data transfer request enable. This bit is mirrored from the ETPU_CDTRER. 0 Disable data transfer request for this channel.Refer to the *eTPU Reference Manual* for more information. 1 Enable data transfer request for this channel.

Table 18-25. ETPU_C*n*CR Field Descriptions (continued)

Field	Description
2–3 CPR [0:1]	Channel priority. Defines the priority level for the channel. The priority level is used by the hardware scheduler. The values for CPR[1:0] and corresponding levels are shown in the table below. **CPR** / **Priority** 00 Disabled 01 Low 10 Middle 11 High For more information on the hardware scheduler, refer to the *eTPU Reference Manual*.
4–6	Reserved
7 ETCS	Entry table condition select. Determines the channel condition encoding scheme that selects the entry point to be taken in an entry table. The ETCS value has to be compatible with the function chosen for the channel, selected in ETPU_C*n*CR[CFS]. Two condition encoding schemes are available. 1 Select alternate entry table condition encoding scheme. 0 Select standard entry table condition encoding scheme.For details about entry table and condition encoding schemes, refer to the *eTPU Reference Manual*.
8–10	Reserved
11–15 CFS [0:4]	Channel function select. Defines the function to be performed by the channel. The function assigned to the channel has to be compatible with the channel condition encoding scheme, selected by ETPU_C*n*CR[ETCS]. For more information about functions, refer to the *eTPU Reference Manual*.
16 ODIS	Output disable. Enables the channel to have its output forced to the value opposite to OPOL when the output disable input signal corresponding to the channel group that it belongs is active. 0 Turns off the output disable feature for the channel.For more information on output disable, refer to the *eTPU Reference Manual*. 1 Turns on the output disable feature for the channel
17 OPOL	Output polarity. Determines the output signal polarity. The activation of the output disable signal forces, when enabled by ETPU_C*n*CR[ODIS], the channel output signal to the opposite of this polarity. 0 Output active low (output disable drives output to high) 1 Output active high (output disable drives output to low)
18–20	Reserved
21–31 CPBA [0:10]	Channel *n* parameter base address. The value of this field multiplied by 8 specifies the SDM parameter base host (byte) address for channel *n* (2-parameter granularity). The formula for calculating the absolute channel parameter base (byte) address, as seen by the host, is eTPU_Base + 0x8000 + CPBA*8. The SDM is mirrored in the parameter sign extension (PSE) area. The formula to calculate the absolute channel parameter base (byte) address in the PSE area is eTPU_Base + 0xC000 + CPBA*8. For more information on SDM addresses, refer to the *eTPU Reference Manual*.

18.4.6.3 eTPU Channel *n* Status Control Register (ETPU_C*n*SCR)

ETPU_C*n*SCR is a collection of the interrupt status bits of the channel, and also the function mode definition (read-write). Bits CIS, CIOS, DTRS, and DTROS for each channel can also be accessed from ETPU_CISR, ETPU_CIOSR, ETPU_CDTRSR, and ETPU_CDTROSR respectively. For more information on the three previously mentioned registers, refer to the *eTPU Reference Manual*.

NOTE

The device core must write 1 to clear a status bit.

NOTE

In this device, eTPU A channels [0:2,12:15,28:29] and eTPU B channels [0:3,12:15,28:31] are connected to the DMA. The data transfer request lines that are not connected to the DMA controller are left disconnected and do not generate transfer requests, even if their request status bits assert in registers ETPU_CDTRSR and ETPU_C*n*SCR

Address: Channel_Register_Base + 0x0004 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	CIS	CIOS	0	0	0	0	0	0	DTRS	DTROS	0	0	0	0	0	0
W	w1c	w1c							w1c	w1c						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	IPS	OPS	0	0	0	0	0	0	0	0	0	0	0	0	FM	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-23. eTPU Channel *n* Status Control Register (ETPU_C*n*SCR)

Table 18-26. ETPU_C*n*SCR Field Descriptions

Field	Description
0 CIS	Channel interrupt status. 0 Channel has no pending interrupt to the device core. 1 Channel has a pending interrupt to the device core. CIS is mirrored in the ETPU_CISR. For more information on ETPU_CISR and interrupts, refer to Section 18.4.5.1, “eTPU Channel Interrupt Status Register (ETPU_CISR),” and the *eTPU Reference Manual*. The core must write 1 to clear CIS.
1 CIOS	Channel interrupt overflow status. 0 Interrupt overflow negated for this channel 1 Interrupt overflow asserted for this channel CIOS is mirrored in the ETPU_CIOSR. For more information on the ETPU_CIOSR and interrupt overflow, refer to Section 18.4.5.3, “eTPU Channel Interrupt Overflow Status Register (ETPU_CIOSR)” and the *eTPU Reference Manual*. The core must write 1 to clear CIOS.
2–7	Reserved
8 DTRS	Data transfer request status. 0 Channel has no pending data transfer request. 1 Channel has a pending data transfer request. DTRS is mirrored in the ETPU_CDTRSR. For more information on the ETPU_CDTRSR and data transfer, refer to Section 18.4.5.2, “eTPU Channel Data Transfer Request Status Register (ETPU_CDTRSR)” and the *eTPU Reference Manual*. The core must write 1 to clear DTRS.

Table 18-26. ETPU_C*n*SCR Field Descriptions (continued)

Field	Description
9 DTROS	Data transfer request overflow status. 0 Data transfer request overflow negated for this channel. 1 Data transfer request overflow asserted for this channel. DTROS is mirrored in the ETPU_CDTROSR. Refer to Section 18.4.5.4, "eTPU Channel Data Transfer Request Overflow Status Register (ETPU_CDTROSR)" and the *eTPU Reference Manual* for more information on ETPU_CDTROSR and data transfer overflows. The core must write 1 to clear DTROS.
10–15	Reserved
16 IPS	Channel input pin state. Shows the current value of the filtered channel input signal state
17 OPS	Channel output pin state. Shows the current value driven in the channel output signal, including the effect of the external output disable feature. If the channel input and output signals are connected to the same pad, OPS reflects the value driven to the pad. This is not necessarily the actual pad value, which drives the value in the IPS bit.
18–29	Reserved
30–31 FM [0:1]	Channel function mode.[1] Each function can use this field for specific configuration. These bits can be tested by microengine code.

[1] These bits are equivalent to the TPU/TPU2/TPU3 host sequence (HSQ) bits.

18.4.6.4 eTPU Channel *n* Host Service Request Register (ETPU_C*n*HSRR)

ETPU_C*n*HSRR is used by the device core to issue service requests to the channel.

Address: Channel_Register_Base + 0x0008 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	HSR		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 18-24. eTPU Channel *n* Host Service Request Register (ETPU_CnHSRR)

Table 18-27. ETPU_C*n*HSRR Field Descriptions

Field	Description
0–28	Reserved
29–31 HSR [0:2]	Host service request. Used by the host core to request service to the channel • HSR = 000: no host service request pending • HSR > 000: function-dependent host service request pending. The HSR value turns to 000 automatically at the end of microengine service for that channel. The host must write HSR > 0 only when HSR = 0. Writing HSR = 000 withdraws a pending request if the scheduler has not started to resolve the entry point, however after the scheduler starts resolving, do not abort the service thread.

18.5 Functional Description

Refer to the *eTPU Reference Manual* for information regarding the functional description of the eTPU module.

18.6 Initialization/Application Information

After initial power-on reset, the eTPU remains in an idle state (except when debug is asserted on power-on reset—in this case, the microengines awaken in the halt state). In addition, initialize the SCM with the eTPU application prior to configuring the eTPU.

Chapter 19
Enhanced Queued Analog-to-Digital Converter (eQADC)

19.1 Introduction

The enhanced queued analog-to-digital converter (eQADC) provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog-to-digital converters (ADCs), and a single master to single slave serial interface to an off-chip external device. The two on-chip ADCs are architected to allow access to all the analog channels.

19.1.1 Block Diagram

Figure 19-1 shows the primary components inside the eQADC.

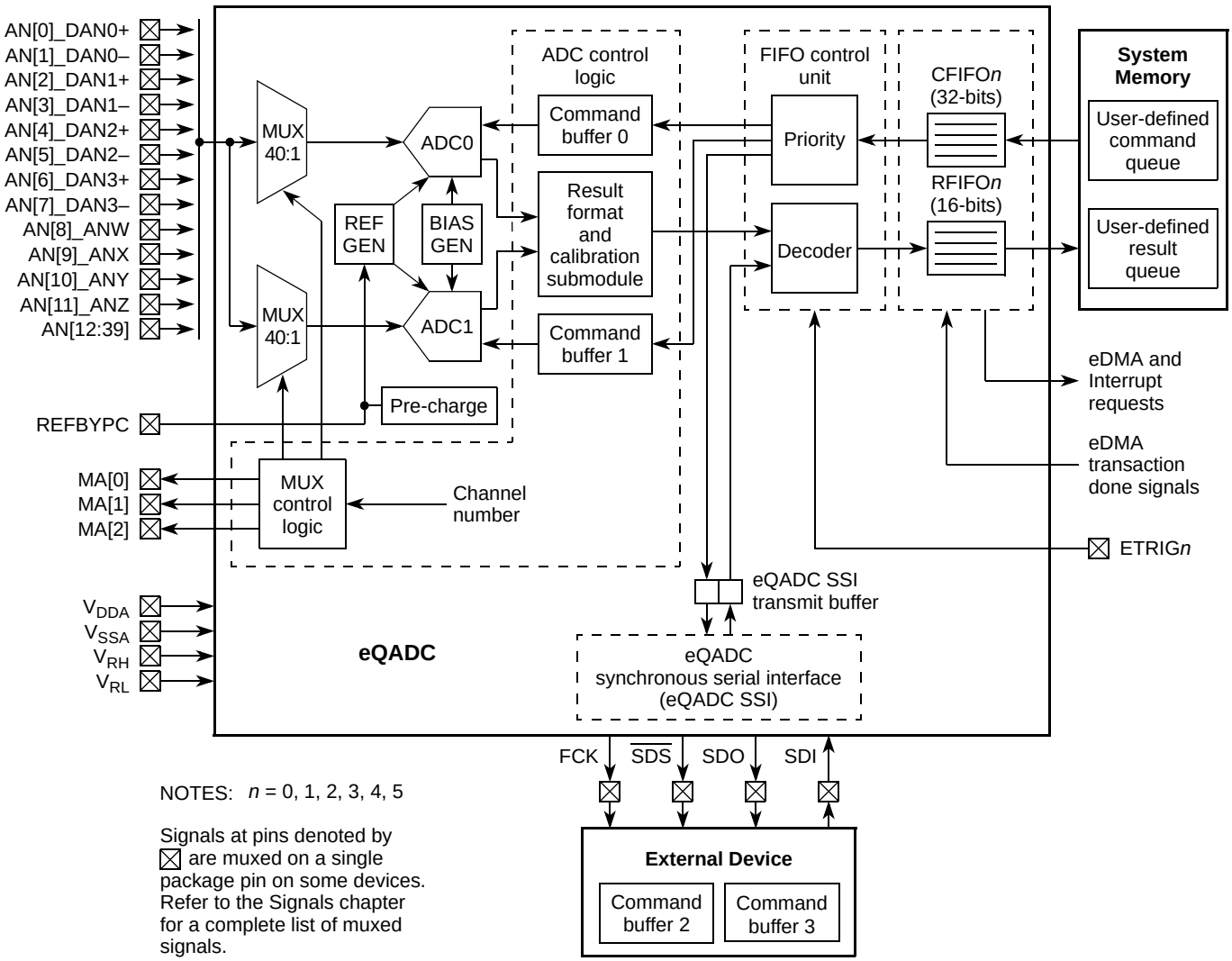


Figure 19-1. Simplified eQADC Block Diagram

19.1.2 Overview

The eQADC transfers commands from multiple command FIFOs (CFIFOs) to the on-chip ADCs or to the external device. The module can also in parallel (independently of the CFIFOs) receive data from the on-chip ADCs or from an off-chip external device into multiple result FIFOs (RFIFOs). The eQADC supports software and external hardware triggers from other modules to initiate transfers of commands from the CFIFOs to the on-chip ADCs or to the external device. (Refer to Section 6.4.5.1, “eQADC External Trigger Input Multiplexing.”) It also monitors the amount of memory currently in use by each the CFIFO and RFIFO to detect underflow and overflow conditions.

A CFIFO underflow occurs when a CFIFO:

- Is in the TRIGGERED state; and
- Becomes empty.

An RFIFO overflow occurs when an RFIFO:

- Becomes full; and
- Host CPU or eDMA data is waiting to transmit to the RFIFO.

The eQADC generates eDMA or interrupt requests to control data movement between the FIFOs and the system memory, which is external to the eQADC.

The eQADC consists of the FIFO control unit which controls the CFIFOs and the RFIFOs, two ADCs with control logic, and the eQADC synchronous serial interface (eQADC SSI) which allows communication with an external device. There are six CFIFOs and six RFIFOs, each with four entries.

The FIFO control unit performs the following functions:

- Prioritizes the CFIFOs to determine which CFIFOs transfer commands
- Supports software and hardware triggers to start command transfers from a particular CFIFO
- Decodes command data from the CFIFOs and sends the commands to one of the two on-chip ADCs or to the external device
- Decodes result data from on-chip ADCs or from the external device, and transfers data to the RFIFO

The ADC control logic manages the execution of commands bound for on-chip ADCs from the CFIFOs and with the RFIFOs via the result format and calibration submodule. The ADC control logic performs the following functions:

- Buffers command data for execution
- Decodes command data and accordingly generates control signals for the two on-chip ADCs
- Formats and calibrates conversion result data coming from the on-chip ADCs
- Generates the internal multiplexer control signals and the select signals used by the external multiplexers

The eQADC SSI allows for a full duplex, synchronous, serial communication between the eQADC and an external device.

Figure 19-1 also depicts data flow through the eQADC. Commands are contained in system memory in a user-defined queue data structure. Command data is moved from the user-defined command queue to the CFIFOs by either the host CPU or by the eDMA. After a CFIFO is triggered and becomes the highest priority, CFIFO command data is transferred from the CFIFO to the on chip ADCs, or to the external device. The ADC executes the command, and the result is moved through the result format and calibration submodule and to the RFIFO. The RFIFO target is specified by a field in the command that initiated the conversion. Data from the external device bypasses the result format and calibration submodule and is moved directly to its specified RFIFO. When data is stored in an RFIFO, data is moved from the RFIFO by the host CPU or by the eDMA to a data structure in system memory depicted in Figure 19-1 as a user-defined result queue.

For users familiar with the QADC, the eQADC system upgrades the functionality provided by that module. Refer to Section 19.5.7, “eQADC versus QADC,” for a comparison between the eQADC and QADC.

19.1.3 Features

The eQADC includes these distinctive features:

- Two independent on-chip RSD cyclic ADCs
  - 12 bit AD resolution.
  - Targets up to 10 bit accuracy at 400 kilosamples per second (ADC_CLK = 6 MHz) and eight bit accuracy at 800 kilosamples per second (ADC_CLK = 12 MHz) for differential conversions.
  - Differential conversions (range -2.5 V to +2.5 V).
  - Single-ended signal range from 0–5 V.
  - Sample times of two (default), 8, 64, or 128 ADC clock cycles.
  - Sample time stamp information when requested.
  - Parallel interface to eQADC CFIFOs and RFIFOs.
  - Supports right-justified unsigned and signed formats for conversion results.
- Optional automatic application of ADC calibration constants: provision of reference voltages (25% V_{REF}[1] and 75% V_{REF}) for ADC calibration purposes
- 40 input channels available to the two on-chip ADCs
- Four pairs of differential analog input channels
- Full duplex synchronous serial interface to an external device
  - A free-running clock is provided for use by the external device
  - Supports a 26-bit message length
  - Transmits a null message when there are no triggered CFIFOs with commands bound for external command buffers, or when there are triggered CFIFOs with commands bound for external command buffers but the external command buffers are full
- Priority-based CFIFOs
  - Supports six CFIFOs with fixed priority. The lower the CFIFO number, the higher its priority. Supports software and several hardware trigger modes to arm a particular CFIFO.
  - Generates interrupt when command coherency is not achieved.
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter
- Upgrades the functionality of the QADC

1. $V_{REF} = V_{RH} - V_{RL}$.

19.1.4 Modes of Operation

This section describes the operating modes of the eQADC.

19.1.4.1 Normal Mode

This is the default operational mode when the eQADC is not in background debug or stop mode.

19.1.4.2 Debug Mode

Upon a debug mode entry request, eQADC behavior varies according to the status of the DBG field in Section 19.3.2.1, “eQADC Module Configuration Register (EQADC_MCR).” If DBG is programmed to 0b00, the debug mode entry request is ignored. If DBG is programmed to 0b10 or to 0b11, the eQADC enters debug mode. In case the eQADC SSI is enabled, the free running clock (FCK) output to external device does not stop when DBG is programmed to 0b11, but FCK stops in low phase, when DBG is programmed to 0b10.

During debug mode, the eQADC does not transfer commands from any CFIFOs, no null messages are transmitted to the external device, no data is returned to any RFIFO, no hardware trigger event is captured, and all eQADC registers can be accessed as in normal mode. Access to eQADC registers implies that CFIFOs can still be triggered using software triggers, because no scheme is implemented to write-protect registers during debug mode. eDMA and interrupt requests continue to be generated as in normal mode.

If at the time the debug mode entry request is detected, there are commands in the ADC that were already under execution, these commands are completed but the generated results, if any, are not sent to the RFIFOs until debug mode is exited. Commands that have not begun to execute are not executed until after exiting debug mode. The clock with an on-chip ADC stops, during its low phase, after the ADC stops executing commands. The time base counter only stops after all on-chip ADCs stop executing commands.

When exiting debug mode, the eQADC relies on the FIFO control unit and on the CFIFO status to determine the next command entry to transfer.

The eQADC internal behavior after the debug mode entry request is detected differs depending on the status of command transfers.

- No command transfer is in progress.

  The eQADC immediately halts future command transfers from any CFIFO.

  If a null message is being transmitted, eQADC completes the serial transmission before halting future command transfers. If valid data (conversion result or data read from an ADC register) is received by the result format and calibration submodule at the end of transmission, this data is not sent to an RFIFO until debug mode is exited.

  If the null message transmission is aborted, the eQADC completes the abort procedure before halting future command transfers from any CFIFO. The message of the CFIFO that caused the abort of the previous serial transmission is transmitted only after exiting debug mode.
- Command transfer is in progress.

  eQADC completes the transfer and updates CFIFO status before halting future command transfers from any CFIFO.

Command transfers to the external device are considered completed when the serial transmission of the command is completed. If valid data (conversion result or data read from an ADC register) is received at the end of a serial transmission, it is not sent to an RFIFO until debug mode is exited. The CFIFO status bits are still updated after the completion of the serial transmission, therefore, after debug mode entry request is detected, the eQADC status bits stop changing several system clock cycles after the on-going serial transmission completes.

If the command message transmission aborts, the eQADC completes the abort procedure before halting future command transfers from any CFIFO. The message of the CFIFO that caused the abort of the previous serial transmission is transmitted only after debug mode exits.

- Command/null message transfer through serial interface was aborted but next serial transmission did not start.

  If the debug mode entry request is detected between the time a previous serial transmission was aborted and the start of the next transmission, the eQADC completes the abort procedure before halting future command transfers from any CFIFO. The message of the CFIFO that caused the abort of the previous serial transmission is transmitted only after debug mode exits.

19.1.4.3 Stop Mode

Upon a stop mode entry request detection, the eQADC progressively halts its operations until it reaches a static, stable state from which it can recover when returning to normal mode. The eQADC then asserts an acknowledge signal, indicating that it is static and that the clock input can be stopped. In stop mode, the free running clock (FCK) output to external device stops during its low phase if the eQADC SSI is enabled, and no hardware trigger events is captured. No capturing of hardware trigger events means that — as long as the system clock is running — CFIFOs can still be triggered using software triggers because no scheme is implemented to write-protect registers during stop mode.

If at the time the stop mode entry request is detected, there are commands in the ADC that were already under execution, these commands are completed but the generated results, if any, are not sent to the RFIFOs until stop mode is exited. Commands whose execution has not started do not execute until stop mode exits.

After these remaining commands are executed, the clock input to the ADCs is stopped. The time base counter stops after all on-chip ADCs cease executing commands and then the stop acknowledge signal is asserted. When exiting stop mode, the eQADC relies on the CFIFO operation modes and on the CFIFO status to determine the next command entry to transfer.

The eQADC internal behavior after the stop mode entry request is detected differs depending on the status of the command transfer.

- No command transfer is in progress

  The eQADC immediately halts future command transfers from any CFIFO.

  If a null message is being transmitted, eQADC completes the transmission before halting future command transfers. If valid data (conversion result or data read from an ADC register) is received at the end of the transmission, it is not sent to an RFIFO until stop mode exits.

If the null message transmission is aborted, the eQADC completes the abort procedure before halting future command transfers from any CFIFO. The message of the CFIFO that caused the abort of the previous serial transmission is only transmitted after stop mode exits.

- Command transfer is in progress.

  The eQADC completes the transfer and update CFIFO status before halting future command transfers from any CFIFO.

  Command transfers to the external device are considered completed when the serial transmission of the command is completed. If valid data (conversion result or data read from an ADC register) is received at the end of a serial transmission, it is not sent to an RFIFO until stop mode exits. The CFIFO status bits are still updated after the completion of the serial transmission, therefore, after stop mode entry request is detected, the eQADC status bits stop changing several system clock cycles after the on-going serial transmission completes.

  If the command message transmission is aborted, the eQADC completes the abort procedure before halting future command transfers from any CFIFO. The message of the CFIFO that caused the abort of the previous serial transmission are transmitted only after stop mode exits.

- Command/null message transfer through serial interface was aborted but next serial transmission did not start.

  If the stop mode entry request is detected between the time a previous serial transmission was aborted and the start of the next transmission, the eQADC completes the abort procedure before halting future command transfers from any CFIFO. The message of the CFIFO that caused the abort of the previous serial transmission is transferred only after stop mode is exited.

19.2 External Signal Description

These signals are external to the eQADC module, but may or may not be physical pins. Refer to Chapter 2, “Signal Description” for a complete list of all physical pins and signals.

Table 19-1. eQADC External Signals

Function	Description	I/O Type	Status During Reset[1]	Status After Reset[2]	Type	Package
AN[0]_ DAN0+	Single-ended analog input 0 Positive terminal differential input	I	I / —	AN[0] / —	Analog	496 416
AN[1]_ DAN0-	Single-ended analog input 1 Negative terminal differential input	I	I / —	AN[1] / —	Analog	496 416
AN[2]_ DAN1+	Single-ended analog input 2 Positive terminal differential input	I	I / —	AN[2] / —	Analog	496 416
AN[3]_ DAN1-	Single-ended analog input 3 Negative terminal differential input	I	I / —	AN[3] / —	Analog	496 416
AN[4]_ DAN2+	Single-ended analog input 4 Positive terminal differential input	I	I / —	AN[4] / —	Analog	496 416
AN[5]_ DAN2-	Single-ended analog input 5 Negative terminal differential input	I	I / —	AN[5] / —	Analog	496 416

Table 19-1. eQADC External Signals (continued)

Function	Description	I/O Type	Status During Reset[1]	Status After Reset[2]	Type	Package
AN[6]_ DAN3+	Single-ended analog input 6 Positive terminal differential input	I	I / —	AN[6] / —	Analog	496 416
AN[7]_ DAN3-	Single-ended analog input 7 Negative terminal differential input	I	I / —	AN[7] / —	Analog	496 416
AN[8]_ ANW	Single-ended analog input 8 External multiplexed analog input W	I	I / —	AN[8] / —	Analog	496 416
AN[9]_ ANX	Single-ended analog input 9 External multiplexed analog input X	I	I / —	AN[9] / —	Analog	496 416
AN[10]_ ANY	Single-ended analog input 10 External multiplexed analog input Y	I	I / —	AN[10] / —	Analog	496 416
AN[11]_ ANZ	Single-ended analog input 11 External multiplexed analog input Z	I	I / —	AN[11] / —	Analog	496 416
AN[12]_ MA[0]_ $\overline{\text{SDS}}$	Single-ended analog input 12 Mux address 0 eQADC SSI serial data select	I O O	I / —	AN[12] / —	Analog/ Digital/ Digital	496 416
AN[13]_ MA[1]_ SDO	Single-ended analog input 13 Mux address 1 eQADC SSI serial data out	I O O	I / —	AN[13] / —	Analog/ Digital/ Digital	496 416
AN[14]_ MA[2]_ SDI	Single-ended analog input 14 Mux address 2 eQADC SSI serial data in	I O I	I / —	AN[14] / —	Analog/ Digital/ Digital	496 416
AN[15]_ FCK	Single-ended analog input 15 eQADC free running clock	I O	I / —	AN[15] / —	Analog/ Digital	496 416
AN[16]	Single-ended analog input 16	I	I / —	AN[16] / —	Analog	496 416
AN[17:18]	Single-ended analog input 17–18	I	I / —	AN[17:19] / —	Analog	496 416
AN[19:20]	Single-ended analog input 19–20	I	I / —	AN[19:20] / —	Analog	496 416
AN[21]	Single-ended analog input	I	I / —	AN[21] / —	Analog	496 416
AN[22:25]	Single-ended analog input	I	I / —	AN[22:25] / —	Analog	496 416
AN[26]	Single-ended analog input	I	I / —	AN[26] / —	Analog	496 416
AN[27:28]	Single-ended analog input	I	I / —	AN[27:28] / —	Analog	496 416
AN[29]	Single-ended analog input	I	I / —	AN[29] / —	Analog	496 416

Table 19-1. eQADC External Signals (continued)

Function	Description	I/O Type	Status During Reset[1]	Status After Reset[2]	Type	Package
AN[30:32]	Single-ended analog input	I	I / —	AN[30:32] / —	Analog	496 416
AN[33]	Single-ended analog input	I	I / —	AN[33] / —	Analog	496 416
AN[34:35]	Single-ended analog input	I	I / —	AN[34:35] / —	Analog	496 416
AN[36]	Single-ended analog input	I	I / —	AN[36] / —	Analog	496 416
AN[37:39]	Single-ended analog input 37–39	I	I / —	AN[37:39] / —	Analog	496 416
ETRIG[0]_ GPIO[111]	External trigger for CFIFO0, CFIFO2, and CFIFO4, as well as the muxed GPIO	I I/O	— / Up	— / Up	Digital	496 416
ETRIG[1]_ GPIO[112]	External trigger for CFIFO1, CFIFO3, and CFIFO5, as well as the muxed GPIO	I I/O	— / Up	— / Up	Digital	496 416
Power Supplies						
V_{RH}	Voltage reference high	I	— / —	V_{RH}	Power	496 416
V_{RL}	Voltage reference low	I	— / —	V_{RL}	Power	496 416
REFBYPC	Reference bypass capacitor input	I	— / —	REFBYPC	Power	496 416
V_{DDA}	Analog positive power supply	I	N/A	V_{DDA}	Power	496 416
V_{SSA}	Analog negative power supply	I	N/A	V_{SSA}	Power	496 416

1 Terminology is O — output, I — input, Up — weak pullup enabled, Down — weak pulldown enabled, Low — output driven low, High — output driven high. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pullup/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

2 Function after reset of GPI is general-purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pullup/down enabled on the pin.

19.3 Memory Map and Register Definition

This section provides memory maps and detailed descriptions of all registers. Data written to or read from reserved areas of the memory map is undefined.

19.3.1 eQADC Memory Map

This section provides memory maps for the eQADC.

Table 19-2. eQADC Memory Map

Address	Register Name	Register Description	Bits
Base (0xFFF8_0000)	EQADC_MCR	EQADC module configuration register	32
Base + 0x0004	—	Reserved	—
Base + 0x0008	EQADC_NMSFR	eQADC null message send format register	32
Base + 0x000C	EQADC_ETDFR	eQADC external trigger digital filter register	32
Base + 0x0010	EQADC_CFPR0	eQADC command FIFO push register 0	32
Base + 0x0014	EQADC_CFPR1	eQADC command FIFO push register 1	32
Base + 0x0018	EQADC_CFPR2	eQADC command FIFO push register 2	32
Base + 0x001C	EQADC_CFPR3	eQADC command FIFO push register 3	32
Base + 0x0020	EQADC_CFPR4	eQADC command FIFO push register 4	32
Base + 0x0024	EQADC_CFPR5	eQADC command FIFO push register 5	32
Base + 0x0028	—	Reserved	—
Base + 0x002C	—	Reserved	—
Base + 0x0030	EQADC_RFPR0	eQADC result FIFO pop register 0	32 [1]
Base + 0x0034	EQADC_RFPR1	eQADC result FIFO pop register 1	32 [1]
Base + 0x0038	EQADC_RFPR2	eQADC result FIFO pop register 2	32 [1]
Base + 0x003C	EQADC_RFPR3	eQADC result FIFO pop register 3	32 [1]
Base + 0x0040	EQADC_RFPR4	eQADC result FIFO pop register 4	32 [1]
Base + 0x0044	EQADC_RFPR5	eQADC result FIFO pop register 5	32 [1]
Base + 0x0048	—	Reserved	—
Base + 0x004C	—	Reserved	—
Base + 0x0050	EQADC_CFCR0	eQADC command FIFO control register 0	16
Base + 0x0052	EQADC_CFCR1	eQADC command FIFO control register 1	16
Base + 0x0054	EQADC_CFCR2	eQADC command FIFO control register 2	16
Base + 0x0056	EQADC_CFCR3	eQADC command FIFO control register 3	16
Base + 0x0058	EQADC_CFCR4	eQADC command FIFO control register 4	16
Base + 0x005A	EQADC_CFCR5	eQADC command FIFO control register 5	16
Base + 0x005C	—	Reserved	—
Base + 0x0060	EQADC_IDCR0	eQADC interrupt and eDMA control register 0	16
Base + 0x0062	EQADC_IDCR1	eQADC interrupt and eDMA control register 1	16
Base + 0x0064	EQADC_IDCR2	eQADC interrupt and eDMA control register 2	16
Base + 0x0066	EQADC_IDCR3	eQADC interrupt and eDMA control register 3	16
Base + 0x0068	EQADC_IDCR4	eQADC interrupt and eDMA control register 4	16
Base + 0x006A	EQADC_IDCR5	eQADC interrupt and eDMA control register 5	16

Table 19-2. eQADC Memory Map (continued)

Address	Register Name	Register Description	Bits
Base + 0x006C	—	Reserved	—
Base + 0x0070	EQADC_FISR0	eQADC FIFO and interrupt status register 0	32
Base + 0x0074	EQADC_FISR1	eQADC FIFO and interrupt status register 1	32
Base + 0x0078	EQADC_FISR2	eQADC FIFO and interrupt status register 2	32
Base + 0x007C	EQADC_FISR3	eQADC FIFO and interrupt status register 3	32
Base + 0x0080	EQADC_FISR4	eQADC FIFO and interrupt status register 4	32
Base + 0x0084	EQADC_FISR5	eQADC FIFO and interrupt status register 5	32
Base + 0x0088	—	Reserved	—
Base + 0x008C	—	Reserved	—
Base + 0x0090	EQADC_CFTCR0	eQADC command FIFO transfer counter register 0	16
Base + 0x0092	EQADC_CFTCR1	eQADC command FIFO transfer counter register 1	16
Base + 0x0094	EQADC_CFTCR2	eQADC command FIFO transfer counter register 2	16
Base + 0x0096	EQADC_CFTCR3	eQADC command FIFO transfer counter register 3	16
Base + 0x0098	EQADC_CFTCR4	eQADC command FIFO transfer counter register 4	16
Base + 0x009A	EQADC_CFTCR5	eQADC command FIFO transfer counter register 5	16
Base + 0x009C	—	Reserved	—
Base + 0x00A0	EQADC_CFSSR0	eQADC command FIFO status snapshot register 0	32
Base + 0x00A4	EQADC_CFSSR1	eQADC command FIFO status snapshot register 1	32
Base + 0x00A8	EQADC_CFSSR2	eQADC command FIFO status snapshot register 2	32
Base + 0x00AC	EQADC_CFSR	eQADC command FIFO status register	32
Base + 0x00B0	—	Reserved	—
Base + 0x00B4	EQADC_SSICR	eQADC synchronous serial interface control register	32
Base + 0x00B8	EQADC_SSIRDR	eQADC synchronous serial interface receive data register	32
Base + (0x00BC–0x00FC)	—	Reserved	—
Base + (0x0100–0x010C)	EQADC_CF0R*n*	eQADC CFIFO0 registers 0–3	32
Base + (0x0110–0x013C)	—	Reserved	—
Base + (0x0140–0x014C)	EQADC_CF1R*n*	eQADC CFIFO1 registers 0–3	32
Base + (0x0150–0x017C)	—	Reserved	—
Base + (0x0180–0x018C)	EQADC_CF2R*n*	eQADC CFIFO2 registers 0–3	32
Base + (0x0190–0x01BC)	—	Reserved	—
Base + (0x01C0–0x01CC)	EQADC_CF3R*n*	eQADC CFIFO3 registers 0–3	32
Base + (0x01D0–0x01FC)	—	Reserved	—

Table 19-2. eQADC Memory Map (continued)

Address	Register Name	Register Description	Bits
Base + (0x0200–0x020C)	EQADC_CF4R*n*	eQADC CFIFO4 registers 0–3	32
Base + (0x0210–0x023C)	—	Reserved	—
Base + (0x0240–0x024C)	EQADC_CF5R*n*	eQADC CFIFO5 registers 0–3	32
Base + (0x0250–0x02FC)	—	Reserved	—
Base + (0x0300–0x030C)	EQADC_RF0R*n*	eQADC RFIFO0 registers 0–3	32
Base + (0x0310–0x033C)	—	Reserved	—
Base + (0x0340–0x034C)	EQADC_RF1R*n*	eQADC RFIFO1 registers 0–3	32
Base + (0x0350–0x037C)	—	Reserved	—
Base + (0x0380–0x038C)	EQADC_RF2R*n*	eQADC RFIFO2 registers 0–3	32
Base + (0x0390–0x03BC)	—	Reserved	—
Base + (0x03C0–0x03CC)	EQADC_RF3R*n*	eQADC RFIFO3 registers 0–3	32
Base + (0x03D0–0x03FC)	—	Reserved	—
Base + (0x0400–0x040C)	EQADC_RF4R*n*	eQADC RFIFO4 registers 0–3	32
Base + (0x0410–0x043C)	—	Reserved	—
Base + (0x0440–0x044C)	EQADC_RF5R*n*	eQADC RFIFO5 registers 0–3	32
Base + (0x0450–0x07FC)	—	Reserved	—

[1] Result FIFOs are 16-bits wide [0:15]; bits [16:31] are filled with zeros to allow for 32-bit read access.

19.3.2 eQADC Register Descriptions

19.3.2.1 eQADC Module Configuration Register (EQADC_MCR)

The EQADC_MCR contains bits used to control how the eQADC responds to a debug mode entry request, and to enable the eQADC SSI interface.

Address: Base+ 0x0000 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	ESSIE		0	DBG	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-2. eQADC Module Configuration Register (EQADC_MCR)

Table 19-3. EQADC_MCR Field Descriptions

Field	Description
0–26	Reserved.
27–28 ESSIE [0:1]	eQADC synchronous serial interface enable. Defines the eQADC synchronous serial interface operation. 00 eQADC SSI is disabled 01 Invalid value 10 eQADC SSI is enabled, FCK is free running, and serial transmissions are disabled 11 eQADC SSI is enabled, FCK is free running, and serial transmissions are enabled
29	Reserved.
30–31 DBG [0:1]	Debug enable. Defines the eQADC response to a debug mode entry request. 00 Do not enter debug mode 01 Invalid value 10 Enter debug mode. If the eQADC SSI is enabled, FCK stops while the eQADC is in debug mode. 11 Enter debug mode. If the eQADC SSI is enabled, FCK is free running while the eQADC is in debug mode

NOTE

Disabling the eQADC SSI (0b00 write to ESSIE) or serial transmissions from the eQADC SSI (0b10 write to ESSIE) while a serial transmission is in progress results in the abort of that transmission.

NOTE

When disabling the eQADC SSI, the FCK does not stop until it reaches its low phase.

19.3.2.2 eQADC Null Message Send Format Register (EQADC_NMSFR)

The EQADC_NMSFR defines the format of the null message sent to the external device.

Address: Base + 0x0008 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	NMF									
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	NMF															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-3. eQADC Null Message Send Format Register (EQADC_NMSFR)

Table 19-4. EQADC_NMSFR Field Descriptions

Field	Description
0–5	Reserved.
6–31 NMF [0:25]	Null message format. Contains the programmable null message send value for the eQADC. The value written to this register is sent as a null message when serial transmissions from the eQADC SSI are enabled (ESSIE field is configured to 0b11 in EQADC_MCR (Section 19.3.2.1, “eQADC Module Configuration Register (EQADC_MCR)) and either • there are no triggered CFIFOs with commands bound for external command buffers, or; • there are triggered CFIFOs with commands bound for external command buffers but the external command buffers are full. Refer to Section , “Null Message Format for External Device Operation” for more information on the format of a null message.

NOTE

The eQADC null message send format register (eQADC_NMSFR) only defines the format of the null message that eQADC sends. The null message register does not control how the eQADC detects a null message from the input source. The eQADC detects a null message by decoding the MESSAGE_TAG field on the receive data. Refer to Table 19-34 for more information on the MESSAGE_TAG field.

NOTE

Writing to the eQADC null message send format register while serial transmissions are enabled is not recommended. Refer to EQADC_MCR[ESSIE] field in Section 19.3.2.1, “eQADC Module Configuration Register (EQADC_MCR).”

19.3.2.3 eQADC External Trigger Digital Filter Register (EQADC_ETDFR)

The EQADC_ETDFR is used to set the minimum time a signal must be held in a logic state on the CFIFO triggers inputs to be recognized as an edge or level gated trigger. The digital filter length field specifies the

minimum number of system clocks that must be counted by the digital filter counter to recognize a logic state change.

Address: Base + 0x000C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	DFL			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-4. eQADC External Trigger Digital Filter Register (EQADC_ETDFR)

Table 19-5. EQADC_ETDFR Field Description Table

Field	Description
0–27	Reserved.
28–31 DFL[0:3]	Digital filter length. Specifies the minimum number of system clocks that must be counted by the digital filter counter to recognize a logic state change. The count specifies the sample period of the digital filter which is calculated according to the following equation: $FilterPeriod = (SystemClockPeriod \times 2^{DFL}) + 1(SystemClockPeriod)$ Minimum clock counts for which an ETRIG signal needs to be stable to be passed through the filter are shown in Table 19-6. Refer to Section 19.4.3.4, "External Trigger Event Detection," for more information on the digital filter. **Note:** The DFL field must only be written when the MODE*n* of all CFIFOs are configured to disabled.

Table 19-6. Minimum Required Time to Valid ETRIG

DFL[0:3]	Minimum Clock Count	Minimum Time (ns) (System Clock = 120MHz)
0b0000	2	16.67
0b0001	3	25.00
0b0010	5	41.67
0b0011	9	75.00
0b0100	17	141.67
0b0101	33	275.00
0b0110	65	541.67
0b0111	129	1075.00
0b1000	257	2141.67
0b1001	513	4275.00
0b1010	1025	8541.67

Table 19-6. Minimum Required Time to Valid ETRIG (continued)

DFL[0:3]	Minimum Clock Count	Minimum Time (ns) (System Clock = 120MHz)
0b1011	2049	17075.00
0b1100	4097	34141.67
0b1101	8193	68275.00
0b1110	16385	136541.67
0b1111	32769	273075.00

19.3.2.4 eQADC CFIFO Push Registers 0–5 (EQADC_CFPR*n*)

The EQADC_CFPRs provide a mechanism to fill the CFIFOs with command messages from the command queues. Refer to Section 19.4.3, "eQADC Command FIFOs," for more information on the CFIFOs and to Section 19.4.1.2, "Message Format in eQADC," for a description on command message formats.

Address: Base + 0x0010 (EQADC_CFPR0) Access: WO
Base + 0x0014 (EQADC_CFPR1);
Base + 0x0018 (EQADC_CFPR2)
Base + 0x001C (EQADC_CFPR3)
Base + 0x0020 (EQADC_CFPR4)
Base + 0x0024 (EQADC_CFPR5)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	CF_PUSH*n*															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	CF_PUSH*n*															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-5. eQADC CFIFO Push Registers 0–5 (EQADC_CFPR*n*)

Table 19-7. EQADC_CFPR*n* Field Descriptions

Field	Description
0–31 CF_PUSH*n* [0:31]	CFIFO push data *n*. When CFIFO*n* is not full, writing to the whole word or any bytes of EQADC_CFPR*n* pushes the 32-bit CF_PUSH*n* value into CFIFO*n*. Writing to the CF_PUSH*n* field also increments the corresponding CFCTR*n* value by one in Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)." When the CFIFO*n* is full, the eQADC ignores any write to the CF_PUSH*n*. Reading the EQADC_CFPR*n* always returns 0. **Note:** Write only whole words to the EQADC_CFPR*n* registers. Writing halfwords or bytes to EQADC_CFPR pushes the entire 32-bit CF_PUSH field into the CFIFO, but undefined data fills the areas of CF_PUSH that were not specifically designated as target locations for the write.

19.3.2.5 eQADC Result FIFO Pop Registers 0–5 (EQADC_RFPR*n*)

The eQADC_RFPRs allow you to retrieve data from RFIFOs.

NOTE

Do not read the EQADC_RFPR*n* unless absolutely necessary, since the data is lost when the read occurs. For compatibility, configure the TLB entry for the EQADC_RFPR*n* registers as guarded.

Address: Base + 0x0030 (EQADC_RFPR0) Access: RO
Base + 0x0034 (EQADC_RFPR1)
Base + 0x0038 (EQADC_RFPR2)
Base + 0x003C (EQADC_RFPR3)
Base + 0x0040 (EQADC_RFPR4)
Base + 0x0044 (EQADC_RFPR5)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	RF_POP*n*															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-6. eQADC RFIFO Pop Registers 0–5 (EQADC_RFPR*n*)

Table 19-8. EQADC_RFPR*n* Field Descriptions

Field	Description
0–15	Reserved.
16–31 RF_POP*n* [0:15]	Result FIFO pop data *n*. When RFIFO*n* is not empty, the RF_POP*n* contains the next unread entry value of RFIFO*n*. Reading the whole word, a halfword, or any bytes of EQADC_RFPR*n* pops one entry from RFIFO*n*, and the RFCTR*n* value is decremented by 1. Refer to Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)." When the RFIFO*n* is empty, any read on EQADC_RFPR*n* returns undefined data value and does not decrement the RFCTR*n* value. Writing to EQADC_RFPR*n* has no effect.

19.3.2.6 eQADC CFIFO Control Registers 0–5 (EQADC_CFCR*n*)

The eQADC_CFCRs contain bits that affect CFIFOs. These bits specify the CFIFO operation mode and can invalidate all of the CFIFO contents.

Address: EQADC_BASE + 0x0050 (EQADC_CFCR0) Access: R/W
EQADC_BASE + 0x0052 (EQADC_CFCR1)
EQADC_BASE + 0x0054 (EQADC_CFCR2)
EQADC_BASE + 0x0056 (EQADC_CFCR3)
EQADC_BASE + 0x0058 (EQADC_CFCR4);
EQADC_BASE + 0x005A (EQADC_CFCR5)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	MODE*n*				0	0	0	0
W						SSE*n*	CFINV*n*									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-7. eQADC CFIFO Control Registers (EQADC_CFCR*n*)

Table 19-9. EQADC_CFCR*n* Field Descriptions

Field	Description
0–4	Reserved.
5 SSE*n*	CFIFO single-scan enable bit *n*. Used to set the SSS*n* bit, as described in Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)." Writing a 1 to SSE*n* sets the SSS*n* if the CFIFO is in single-scan mode. When SSS*n* is already asserted, writing a 1 to SSE*n* has no effect. If the CFIFO is in continuous-scan mode or is disabled, writing a 1 to SSE*n* does not set SSS*n*. Writing a 0 to SSE*n* has no effect. SSE*n* always is read as 0. 0 No effect. 1 Set the SSS*n* bit.
6 CFINV*n*	CFIFO invalidate bit *n*. Causes the eQADC to invalidate all entries of CFIFO*n*. Writing a 1 to CFINV*n* resets the value of CFCTR*n* in the EQADC_FISR register (refer to Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)." Writing a 1 to CFINV*n* also resets the push next data pointer, transfer next data pointer to the first entry of CFIFO*n* in Figure 19-35. Reading CFINV*n* always returns a 0. Writing a 0 has no effect. 0 No effect. 1 Invalidate all of the entries in the corresponding CFIFO. **Note:** Writing CFINV*n* only invalidates commands stored in CFIFO*n*; previously transferred commands that are waiting for execution (commands stored in the ADC command buffers) are executed, and the results are stored in the RFIFO. **Note:** Do not write to CFINV*n* unless MODE*n* is disabled, and CFIFO status is IDLE.
7	Reserved.
8–11 MODE*n* [0:3]	CFIFO operation mode *n*. Selects the CFIFO operation mode for CFIFO*n*. Refer to Section 19.4.3.5, "CFIFO Scan Trigger Modes," for more information on CFIFO trigger mode. **Note:** If MODE*n* is not disabled, it must not be changed to any other mode besides disabled. If MODE*n* is disabled and the CFIFO status is IDLE, MODE*n* can be changed to any other mode.
12–15	Reserved.

Table 19-10. CFIFO Operation Mode Table

MODE*n*[0:3]	CFIFO Operation Mode
0b0000	Disabled
0b0001	Software trigger, single scan
0b0010	Low level gated external trigger, single scan
0b0011	High level gated external trigger, single scan

Table 19-10. CFIFO Operation Mode Table (continued)

MODE*n*[0:3]	CFIFO Operation Mode
0b0100	Falling edge external trigger, single scan
0b0101	Rising edge external trigger, single scan
0b0110	Falling or rising edge external trigger, single scan
0b0111–0b1000	Reserved
0b1001	Software trigger, continuous scan
0b1010	Low level gated external trigger, continuous scan
0b1011	High level gated external trigger, continuous scan
0b1100	Falling edge external trigger, continuous scan
0b1101	Rising edge external trigger, continuous scan
0b1110	Falling or rising edge external trigger, continuous scan
0b1111	Reserved

19.3.2.7 eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCR*n*)

The eQADC_IDCRs contain bits to enable the generation of interrupt or eDMA requests when the corresponding flag bits are set in EQADC_FISRn. Refer to Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn).”

Address: EQADC_BASE + 0x0060 (EQADC_IDCR0) Access: R/W
EQADC_BASE + 0x0062 (EQADC_IDCR1)
EQADC_BASE + 0x0064 (EQADC_IDCR2)
EQADC_BASE + 0x0066 (EQADC_IDCR3)
EQADC_BASE + 0x0068 (EQADC_IDCR4)
EQADC_BASE + 0x006A (EQADC_IDCR5)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	NCIE*n*	TORIE*n*	PIE*n*	EOQIE*n*	CFUIE*n*	0	CFFE*n*	CFFS*n*	0	0	0	0	RFOIE*n*	0	RFDE*n*	RFDS*n*
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-8. eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCR*n*)

Table 19-11. EQADC_IDCR*n* Field Descriptions

Field	Description
0 NCIE*n*	Non-coherency interrupt enable *n*. Enables the eQADC to generate an interrupt request when the corresponding NCF*n*, described in Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)," is asserted. 0 Disable non-coherency interrupt request 1 Enable non-coherency interrupt request
1 TORIE*n*	Trigger overrun interrupt enable *n*. Enables the eQADC to generate an interrupt request when the corresponding TORF*n* (described in Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)") is asserted. Apart from generating an independent interrupt request for a CFIFO*n* trigger overrun event, the eQADC also provides a combined interrupt at which the result FIFO overflow interrupt, the command FIFO underflow interrupt, and the command FIFO trigger overrun interrupt requests of all CFIFOs are ORed. When RFOIE*n*, CFUIE*n*, and TORIE*n* are all asserted, this combined interrupt request is asserted whenever one of the following 18 flags becomes asserted: RFOF*n*, CFUF*n*, and TORF*n* (assuming that all interrupts are enabled). Refer to Section 19.4.7, "eQADC eDMA/Interrupt Request," for details. 0 Disable trigger overrun interrupt request 1 Enable trigger overrun interrupt request
2 PIE*n*	Pause interrupt enable *n*. Enables the eQADC to generate an interrupt request when the corresponding PFx in EQADC_FISRn is asserted. Refer to Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)." 0 Disable pause interrupt request 1 Enable pause interrupt request
3 EOQIE*n*	End-of-queue interrupt enable *n*. Enables the eQADC to generate an interrupt request when the corresponding EOQF*n* in EQADC_FISRn is asserted. Refer to Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)." 0 Disable end of queue interrupt request. 1 Enable end of queue interrupt request.
4 CFUIE*n*	CFIFO underflow interrupt enable *n*. Enables the eQADC to generate an interrupt request when the corresponding CFUF*n* in EQADC_FISRn is asserted. Apart from generating an independent interrupt request for a CFIFO*n* underflow event, the eQADC also provides a combined interrupt at which the result FIFO overflow interrupt, the command FIFO underflow interrupt, and the command FIFO trigger overrun interrupt requests of all CFIFOs are ORed. When RFOIE*n*, CFUIE*n*, and TORIE*n* are all asserted, this combined interrupt request is asserted whenever one of the following 18 flags becomes asserted: RFOF*n*, CFUF*n*, and TORF*n* (assuming that all interrupts are enabled). Refer to Section 19.4.7, "eQADC eDMA/Interrupt Request," for details. 0 Disable underflow interrupt request 1 Enable underflow interrupt request
5	Reserved.
6 CFFE*n*	CFIFO fill enable *n*. Enables the eQADC to generate an interrupt request (CFFS*n* is asserted) or eDMA request (CFFS*n* is negated) when CFFF*n* in EQADC_FISRn is asserted. Refer to Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)." 0 Disable CFIFO fill eDMA or interrupt request 1 Enable CFIFO fill eDMA or interrupt request **Note:** CFFE*n* must not be negated while an eDMA transaction is in progress.
7 CFFS*n*	CFIFO fill select *n*. Selects if an eDMA or interrupt request is generated when CFFF*n* in EQADC_FISRn (Refer to Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)") is asserted. If CFFE*n* is asserted, the eQADC generates an interrupt request when CFFS*n* is negated, or it generates an eDMA request if CFFS*n* is asserted. 0 Generate interrupt request to move data from the system memory to CFIFO*n*. 1 Generate eDMA request to move data from the system memory to CFIFO*n*. **Note:** CFFS*n* must not be negated while an eDMA transaction is in progress.

Table 19-11. EQADC_IDCR*n* Field Descriptions (continued)

Field	Description
8–11	Reserved.
12 RFOIE*n*	RFIFO overflow interrupt enable *n*. Enables the eQADC to generate an interrupt request when the corresponding RFOF*n* in EQADC_FISRn is asserted. Refer to Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)." Apart from generating an independent interrupt request for an RFIFO*n* overflow event, the eQADC also provides a combined interrupt at which the result FIFO overflow Interrupt, the command FIFO underflow interrupt, and the command FIFO trigger overrun interrupt requests of all CFIFOs are ORed. When RFOIE*n*, CFUIE*n,* and TORIE*n* are all asserted, this combined interrupt request is asserted whenever one of the following 18 flags becomes asserted: RFOF*n,* CFUF*n*, and TORF*n* (assuming that all interrupts are enabled). Refer to Section 19.4.7, "eQADC eDMA/Interrupt Request," for details. 0 Disable overflow interrupt request 1 Enable overflow Interrupt request
13	Reserved.
14 RFDE*n*	RFIFO drain enable *n*. Enables the eQADC to generate an interrupt request (RFDS*n* is asserted) or eDMA request (RFDS*n* is negated) when RFDF*n* in EQADC_FISRn (Refer to Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)") is asserted. 0 Disable RFIFO drain eDMA or interrupt request 1 Enable RFIFO drain eDMA or interrupt request **Note:** RFDE*n* must not be negated while an eDMA transaction is in progress.
15 RFDS*n*	RFIFO drain select *n*. Selects if an eDMA or interrupt request is generated when RFDF*n* in EQADC_FISRn (Refer to Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)") is asserted. If RFDE*n* is asserted, the eQADC generates an interrupt request when RFDS*n* is negated, or it generates an eDMA request when RFDS*n* is asserted. 0 Generate interrupt request to move data from RFIF*n* to the system memory 1 Generate eDMA request to move data from RFIFO*n* to the system memory **Note:** RFDS*n* must not be negated while an eDMA transaction is in progress.

19.3.2.8 eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISR*n*)

The EQADC_FISRs contain flag and status bits for each CFIFO and RFIFO pair. Writing 1 to a flag bit clears it. Writing 0 has no effect. Status bits are read only. These bits indicate the status of the FIFO itself.

Address: Base + 0x0070 (EQADC_FISR0) Access: R/W1c
Base + 0x0074 (EQADC_FISR1)
Base + 0x0078 (EQADC_FISR2)
Base + 0x007C (EQADC_FISR3)
Base + 0x0080 (EQADC_FISR4)
Base + 0x0084 (EQADC_FISR5)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	NCF*n*	TORF*n*	PF*n*	EOQF*n*	CFUF*n*	SSS*n*	CFFF*n*	0	0	0	0	0	RFOF*n*	0	RFDF*n*	0
W	w1c	w1c	w1c	w1c	w1c		w1c						w1c		w1c	
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	CFCTR*n*				TNXTPTR*n*				RFCTR*n*				POPNXTPTR*n*			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-9. eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISR*n*)

Table 19-12. EQADC_FISR*n* Field Descriptions

Field	Description
0 NCF*n*	Non-coherency flag *n*. NCF*n* is set whenever a command sequence being transferred through CFIFO*n* becomes non-coherent. If NCIE*n* in EQADC_IDCRn (Refer to Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn)”) and NCF*n* are asserted, an interrupt request is generated. Writing a 1 clears NCF*n*. Writing a 0 has no effect. More for information on non-coherency refer to Section 19.4.3.6.5, “Command Sequence Non-Coherency Detection.” 0 Command sequence being transferred by CFIFO*n* is coherent 1 Command sequence being transferred by CFIFO*n* became non-coherent **Note:** Non-coherency means that a command in the command FIFO was not immediately executed, but delayed. This may occur if the command is pre-empted, where a higher priority queue is triggered and has a competing conversion command for the same converter.
1 TORF*n*	Trigger overrun flag for CFIFO *n*. TORF*n* is set when trigger overrun occurs for the specified CFIFO in edge or level trigger mode. Trigger overrun occurs when an already triggered CFIFO receives an additional trigger. When EQADC_IDCRn[TORIE*n]* is set (Refer to Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn)”) and TORF*n* are asserted, an interrupt request is generated. Apart from generating an independent interrupt request for a CFIFO*n* trigger overrun event, the eQADC also provides a combined interrupt at which the result FIFO overflow interrupt, the command FIFO underflow interrupt, and the command FIFO trigger overrun Interrupt requests of all CFIFOs are ORed. When RFOIE*n*, CFUIE*n*, and TORIE*n* are all asserted, this combined interrupt request is asserted whenever one of the following 18 flags becomes asserted: RFOF*n*, CFUF*n*, and TORF*n* (assuming that all interrupts are enabled). Refer to Section 19.4.7, “eQADC eDMA/Interrupt Request,” for details. Write 1 to clear the TORF*n* bit. Writing 0 has no effect. 0 No trigger overrun occurred 1 Trigger overrun occurred **Note:** The trigger overrun flag is not set for CFIFOs configured for software trigger mode.

Table 19-12. EQADC_FISR*n* Field Descriptions (continued)

Field	Description
2 PF*n*	Pause flag *n*. PF behavior changes according to the CFIFO trigger mode. • In edge trigger mode, PF*n* is set when the eQADC completes the transfer of an entry with an asserted pause bit from CFIFO*n*. • In level trigger mode, when CFIFO*n* is in the TRIGGERED state, PF*n* is set when CFIFO status changes from TRIGGERED due to the detection of a closed gate. An interrupt routine, generated due to the asserted PF, can be used to verify if a complete scan of the user-defined command queue was performed. If a closed gate is detected while no command transfers are taking place, it has an immediate effect on the CFIFO status. If a closed gate is detected while a command transfer to an on-chip ADC is taking place, it only affects the CFIFO status when the transfer completes. If a closed gate is detected during the serial transmission of a command to the external device, it has no effect on the CFIFO status until the transmission completes. The transfer of entries bound for the on-chip ADCs is considered completed when they are stored in the appropriate ADC command buffer. The transfer of entries bound for the external device is considered completed when the serial transmission of the entry is completed. In software trigger mode, PF*n* is never asserted. If PIE*n* (Refer to Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn)”) and PF*n* are asserted, an interrupt is generated. Writing a 1 clears the PF*n*. Writing a 0 has no effect. Refer to Section 19.4.3.6.3, “Pause Status,” for more information on pause flag. 0 Entry with asserted pause bit was not transferred from CFIFO*n* (CFIFO in edge trigger mode), or CFIFO status did not change from the TRIGGERED state due to detection of a closed gate (CFIFO in level trigger mode). 1 Entry with asserted pause bit was transferred from CFIFO*n* (CFIFO in edge trigger mode), or CFIFO status changes from the TRIGGERED state due to detection of a closed gate (CFIFO in level trigger mode). **Note:** In edge trigger mode, an asserted PF*n* only implies that the eQADC has finished transferring a command with an asserted pause bit from CFIFO*n*. It does not imply that result data for the current command and for all previously transferred commands has been returned to the appropriate RFIFO. **Note:** In software or level trigger mode, when the eQADC completes the transfer of an entry from CFIFO*n* with an asserted pause bit, PF*n* is not set and commands continue to transfer without pausing.
3 EOQF*n*	End-of-queue flag *n*. Indicates that an entry with an asserted EOQ bit was transferred from CFIFO*n* to the on-chip ADCs or to the external device. Refer to Section 19.4.1.2, “Message Format in eQADC,” for details about command message formats. When the eQADC completes the transfer of an entry with an asserted EOQ bit from CFIFO*n*, EOQF*n* is set. The transfer of entries bound for the on-chip ADCs is considered completed when they are stored in the appropriate command buffer. The transfer of entries bound for the external device is considered completed when the serial transmission of the entry is completed. If the EOQIE*n* bit (Refer to Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn)”) and EOQF*n* are asserted, an interrupt is generated. Writing a 1 clears the EOQF*n* bit. Writing a 0 has no effect. Refer to Section 19.4.3.6.2, “Command Queue Completion Status,” for more information on end-of-queue flag. 0 Entry with asserted EOQ bit was not transferred from CFIFO*n* 1 Entry with asserted EOQ bit was transferred from CFIFO*n* **Note:** An asserted EOQF*n* only implies that the eQADC has finished transferring a command with an asserted EOQ bit from CFIFO*n*. It does not imply that result data for the current command and for all previously transferred commands has been returned to the appropriate RFIFO.

Table 19-12. EQADC_FISR*n* Field Descriptions (continued)

Field	Description
4 CFUF*n*	CFIFO underflow flag *n*. Indicates an underflow event on CFIFO*n*. CFUF*n* is set when CFIFO*n* is in the TRIGGERED state and it becomes empty. No commands are transferred from an underflowing CFIFO, and command transfers from lower priority CFIFOs are not blocked. When CFUIE*n* (see Section Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn)”) and CFUF*n* are both asserted, the eQADC generates an interrupt request. Apart from generating an independent interrupt request for a CFIFO*n* underflow event, the eQADC also provides a combined interrupt at which the result FIFO overflow interrupt, the command FIFO underflow interrupt, and the command FIFO trigger overrun interrupt requests of all CFIFOs are ORed. When RFOIE*n*, CFUIE*n*, and TORIE*n* are all asserted, this combined interrupt request is asserted whenever one of the following 18 flags becomes asserted: RFOF*n*, CFUF*n*, and TORF*n* (assuming that all interrupts are enabled). Refer to Section 19.4.7, “eQADC eDMA/Interrupt Request,” for details. Writing a 1 clears CFUF*n*. Writing a 0 has no effect. 0 No CFIFO underflow event occurred 1 A CFIFO underflow event occurred
5 SSS*n*	CFIFO single-scan status bit *n*. When asserted, enables the detection of trigger events for CFIFOs programmed into single-scan level- or edge-trigger mode, and works as trigger for CFIFOs programmed into single-scan software-trigger mode. Refer to Section 19.4.3.5.2, “Single-Scan Mode,” for further details. The SSS*n* bit is set by writing a 1 to the SSE*n* bit (see Section Section 19.3.2.6, “eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)”). The eQADC clears the SSS*n* bit when a command with an asserted EOQ bit is transferred from a CFIFO in single-scan mode, when a CFIFO is in single-scan level trigger mode and its status changes from the TRIGGERED state due to the detection of a closed gate, or when the value of the CFIFO operation mode MODE*n* (see Section 19.3.2.6, “eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)”) is changed to disabled. Writing to SSS*n* has no effect. SSS*n* has no effect in continuous-scan or in disabled mode. 0 CFIFO in single-scan, level-, or edge-trigger mode ignores trigger events, or CFIFO in single-scan software-trigger mode is not triggered. 1 CFIFO in single-scan level- or edge-trigger mode detects a trigger event, or CFIFO in single-scan software-trigger mode is triggered.
6 CFFF*n*	CFIFO fill flag *n*. CFFF*n* is set when the CFIFO*n* is not full. When CFFE*n* (see Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn)”) and CFFF*n* are both asserted, an interrupt or an eDMA request is generated depending on the status of the CFFS*n* bit. When CFFS*n* is negated (interrupt requests selected), software clears CFFF*n* by writing a 1 to it. Writing a 0 has no effect. When CFFS*n* is asserted (eDMA requests selected), CFFF*n* is automatically cleared by the eQADC when the CFIFO becomes full. 0 CFIFO*n* is full. 1 CFIFO*n* is not full. **Note:** When generation of interrupt requests is selected (CFFS*n*=0), CFFF*n* must only be cleared in the ISR after the CFIFO*n* push register is accessed. **Note:** CFFF*n* should not be cleared when CFFSn is asserted (eDMA requests selected).
7–11	Reserved.

Table 19-12. EQADC_FISR*n* Field Descriptions (continued)

Field	Description
12 RFOF*n*	RFIFO overflow flag *n*. Indicates an overflow event on RFIFO*n*. RFOF*n* is set when RFIFO*n* is already full, and a new data is received from the on-chip ADCs or from the external device. The RFIFO*n* does not overwrite older data in the RFIFO, and the new data is ignored. When RFOIE*n* (see Section 19.3.2.7, "eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn)") and RFOF*n* are both asserted, the eQADC generates an interrupt request. Apart from generating an independent interrupt request for an RFIFO*n* overflow event, the eQADC also provides a combined interrupt at which the result FIFO overflow interrupt, the command FIFO underflow interrupt, and the command FIFO trigger overrun interrupt requests of all CFIFOs are ORed. When RFOIE*n*, CFUIE*n*, and TORIE*n* are all asserted, this combined interrupt request is asserted whenever one of the following 18 flags becomes asserted: RFOF*n*, CFUF*n*, and TORF*n* (assuming that all interrupts are enabled). Refer to Section 19.4.7, "eQADC eDMA/Interrupt Request," for details. Write 1 to clear RFOF*n*. Writing a 0 has no effect. 0 No RFIFO overflow event occurred. 1 An RFIFO overflow event occurred.
13	Reserved.
14 RFDF*n*	RFIFO drain flag *n*. Indicates if RFIFO*n* has valid entries that can be drained or not. RFDF*n* is set when the RFIFO*n* has at least one valid entry in it. When RFDE*n* (see Section 19.3.2.7, "eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn)") and RFDF*n* are both asserted, an interrupt or an eDMA request is generated depending on the status of the RFDS*n* bit. When RFDS*n* is negated (interrupt requests selected), software clears RFDF*n* by writing a 1 to it. Writing a 0 has no effect. When RFDS*n* is asserted (eDMA requests selected), RFDF*n* is automatically cleared by the eQADC when the RFIFO becomes empty. 0 RFIFO*n* is empty. 1 RFIFO*n* has at least one valid entry. **Note:** In the interrupt service routine, RFDF must be cleared only after the RFIFO*n* pop register is read. **Note:** RFDF*n* should not be cleared when RFDS*n* is asserted (eDMA requests selected).
15	Reserved.
16–19 CFCTR*n* [0:3]	CFIFO*n* entry counter. Indicates the number of commands stored in the CFIFO*n*. When the eQADC completes transferring a piece of new data from the CFIFO*n*, it decrements CFCTR*n* by 1. Writing a word or any bytes to the corresponding CFIFO Push Register (see Section 19.3.2.4, "eQADC CFIFO Push Registers 0–5 (EQADC_CFPRn)") increments CFCTR*n* by 1. Writing any value to CFCTR*n* has no effect.
20–23 TNX TPTR*n* [0:3]	CFIFO*n* transfer next pointer. Indicates the index of the next entry to be removed from CFIFO*n* when it completes a transfer. When TNXTPTR*n* is 0, it points to the entry with the smallest memory-mapped address inside CFIFO*n*. TNXTPTR*n* is only updated when a command transfer is completed. If the maximum index number (CFIFO depth minus 1) is reached, TNXTPTR*n* is wrapped to 0, else, it is incremented by 1. For details refer to Section 19.4.3.1, "CFIFO Basic Functionality." Writing any value to TNXTPTR*n* has no effect.
24–27 RFCTR*n* [0:3]	RFIFO*n* entry counter. Indicates the number of data items stored in the RFIFO*n*. When the eQADC stores a piece of new data into RFIFO*n,* it increments RFCTR*n* by 1. Reading the whole word, halfword or any bytes of the corresponding Result FIFO pop register (see Section 19.3.2.5, "eQADC Result FIFO Pop Registers 0–5 (EQADC_RFPRn)") decrements RFCTR*n* by 1. Writing any value to RFCTR*n* itself has no effect.
28–31 POPNX TPTR*n* [0:3]	RFIFO*n* pop next pointer. Indicates the index of the entry that is returned when EQADC_RFPR*n* is read. When POPNXTPTR*n* is 0, it points to the entry with the smallest memory-mapped address inside RFIFO*n*. POPNXTPTR*n* is updated when EQADC_RFPR*n* is read. If the maximum index number (RFIFO depth minus 1) is reached, POPNXTPTR*n* is wrapped to 0, else, it is incremented by 1. For details refer to Section 19.4.4.1, "RFIFO Basic Functionality." Writing any value to POPNXTPTR*n* has no effect.

19.3.2.9 eQADC CFIFO Transfer Counter Registers 0–5 (EQADC_CFTCR*n*)

The EQADC_CFTCRs record the number of commands transferred from a CFIFO. The EQADC_CFTCR supports the monitoring of command transfers from a CFIFO.

Address: EQADC_BASE + 0x0090 (EQADC_CFTCR0) Access: R/W
EQADC_BASE + 0x0092 (EQADC_CFTCR1)
EQADC_BASE + 0x0094 (EQADC_CFTCR2)
EQADC_BASE + 0x0096 (EQADC_CFTCR3)
EQADC_BASE + 0x0098 (EQADC_CFTCR4)
EQADC_BASE + 0x009A (EQADC_CFTCR5)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	TC_CF*n*										
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-10. eQADC CFIFO Transfer Counter Registers (EQADC_CFTCR*n*)

Table 19-13. EQADC_CFTCR*n* Field Descriptions

Field	Description
0–4	Reserved.
5–15 TC_CF*n* [0:10]	Transfer counter for CFIFO*n*. TC_CF*n* counts the number of commands that have been completely transferred from CFIFO*n*. TC_CF*n*=2, for example, signifies that two commands have been transferred. The transfer of entries bound for the on-chip ADCs is considered completed when they are stored in the appropriate command buffer. The transfer of entries bound for an external device is considered completed when the serial transmission of the entry is completed. The eQADC increments the TC_CF*n* value by 1 after a command is transferred. TC_CF*n* resets to 0 after eQADC completes transferring a command with an asserted EOQ bit. Writing any value to TC_CF*n* sets the counter to that written value. **Note:** If CFIFO*n* is in the TRIGGERED state when its MODE*n* field is programmed to disabled, the exact number of entries transferred from the CFIFO until that point (TC_CF*n*) is only known after the CFIFO status changes to IDLE, as indicated by CFS*n*. For details refer to Section 19.4.3.5.1, “Disabled Mode.”

19.3.2.10 eQADC CFIFO Status Snapshot Registers 0–2 (EQADC_CFSSR*n*)

The eQADC_CFSSRs contain status fields to track the operation status of each CFIFO and the transfer counter of the last CFIFO to initiate a command transfer to the internal ADCs and the external command buffers. EQADC_CFSSR0–1 are related to the on-chip ADC command buffers (buffers 0 and 1) while EQADC_CFSSR2 is related to the external command buffers (buffers 2 and 3). All fields of a particular EQADC_CFSSR are captured at the beginning of a command transfer to the buffer associated with that register.

Note that captured status register values are associated with a previous command transfer. This means that the eQADC_CFSSR registers capture the status registers before the status registers change, because of the transfer of the current command that is about to be popped from the CFIFO. The EQADC_CFSSRs are read only. Writing to the EQADC_CFSSRs has no effect.

Address: Base + 0x00A0 Access: RO

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	CFS0_T0		CFS1_T0		CFS2_T0		CFS3_T0		CFS4_T0		CFS5_T0		0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	LCFT0				TC_LCFT0										
W																
Reset	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Figure 19-11. eQADC CFIFO Status Snapshot Register 0 (EQADC_CFSSR0)

Table 19-14. EQADC_CFSSR0 Field Descriptions

Field	Description
0–11 CFS*n*_T0 [0:1]	CFIFO status at transfer to ADC*n* command buffer. Indicates the CFIFO*n* status at the time a command transfer to ADC*n* command buffer is initiated. CFS*n*_T0 is a copy of the corresponding CFS*n* in EQADC_CFSR (see Section 19.3.2.11, "eQADC CFIFO Status Register (EQADC_CFSR)") captured at the time a command transfer to buffer*n* is initiated.
12–16	Reserved.
17–20 LCFT0 [0:3]	Last CFIFO to transfer to ADC*n* command buffer. Holds the CFIFO number of last CFIFO to have initiated a command transfer to ADC*n* command buffer. LCFT0 has the following values: **LCFT0[0:3]** / **LCFT0 Meaning** 0b0000 – Last command was transferred from CFIFO0 0b0001 – Last command was transferred from CFIFO1 0b0010 – Last command was transferred from CFIFO2 0b0011 – Last command was transferred from CFIFO3 0b0100 – Last command was transferred from CFIFO4 0b0101 – Last command was transferred from CFIFO5 0b0110–0b1110 – Reserved 0b1111 – No command was transferred to ADC*n* command buffer
21–31 TC_LCFT0 [0:10]	Transfer counter for last CFIFO to transfer commands to ADC*n* command buffer. Indicates the number of commands which have been completely transferred from CFIFO*n* when a command transfer from CFIFO*n* to ADC*n* command buffer is initiated. TC_LCFT0 is a copy of the corresponding TC_CF*n* in EQADC_CFTCR*n* (see Section 19.3.2.9) captured at the time a command transfer from CFIFO*n* to ADC*n* command buffer is initiated. This field has no meaning when LCFT0 is 0b1111.

Address: Base + 0x00A4 Access: RO

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	CFS0_T1		CFS1_T1		CFS2_T1		CFS3_T1		CFS4_T1		CFS5_T1		0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	LCFT1				TC_LCFT1										
W																
Reset	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Figure 19-12. eQADC CFIFO Status Snapshot Register 1 (EQADC_CFSSR1)

Table 19-15. EQADC_CFSSR1 Field Descriptions

Field	Description
0–11 CFS*n*_T1 [0:1]	CFIFO status at transfer to ADC*n* command buffer. Indicates the CFIFO*n* status at the time a command transfer to ADC*n* command buffer is initiated. CFS*n*_T1 is a copy of the corresponding CFS*n* in EQADC_CFSR (see Section 19.3.2.11, “eQADC CFIFO Status Register (EQADC_CFSR)”) captured at the time a command transfer to buffer*n* is initiated.
12–16	Reserved.
17–20 LCFT1 [0:3]	Last CFIFO to transfer to ADC*n* command buffer. Holds the CFIFO number of last CFIFO to have initiated a command transfer to ADC*n* command buffer. LCFT1 has the following values: **LCFT1[0:3]** / **LCFT1 Meaning** 0b0000 – Last command was transferred from CFIFO0 0b0001 – Last command was transferred from CFIFO1 0b0010 – Last command was transferred from CFIFO2 0b0011 – Last command was transferred from CFIFO3 0b0100 – Last command was transferred from CFIFO4 0b0101 – Last command was transferred from CFIFO5 0b0110–0b1110 – Reserved 0b1111 – No command was transferred to ADC*n* command buffer
21–31 TC_LCFT1 [0:10]	Transfer counter for last CFIFO to transfer commands to ADC*n* command buffer. Indicates the number of commands which have been completely transferred from CFIFO*n* when a command transfer from CFIFO*n* to ADC*n* command buffer is initiated. TC_LCFT1 is a copy of the corresponding TC_CF*n* in EQADC_CFTCRn (see Section 19.3.2.9, “eQADC CFIFO Transfer Counter Registers 0–5 (EQADC_CFTCRn)”) captured at the time a command transfer from CFIFO*n* to ADC*n* command buffer is initiated. This field has no meaning when LCFT1 is 0b1111.

The third eQADC CFIFO status snapshot register is displayed in Figure 19-13.

Address: Base + 0x00A8 Access: RO

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	CFS0_TSSI		CFS1_TSSI		CFS2_TSSI		CFS3_TSSI		CFS4_TSSI		CFS5_TSSI		0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	ENI	LCFTSSI				TC_LCFTSSI										
W																
Reset	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Figure 19-13. eQADC CFIFO Status Snapshot Register 2 (EQADC_CFSSR2)

Table 19-16. EQADC_CFSSR2 Field Descriptions

Field	Description
0–11 CFS*n*_TSSI [0:1]	CFIFO Status at Transfer through the eQADC SSI. Indicates the CFIFO*n* status at the time a serial transmission through the eQADC SSI is initiated. CFS*n*_TSSI is a copy of the corresponding CFS*n* in EQADC_CFSR (see Section 19.3.2.11, “eQADC CFIFO Status Register (EQADC_CFSR)”) captured at the time a serial transmission through the eQADC SSI is initiated.
12–15	Reserved.
16 ENI	External command buffer number Indicator. Indicates to which external command buffer the last command was transmitted. 0 Last command was transferred to command buffer 2. 1 Last command was transferred to command buffer 3.

Table 19-16. EQADC_CFSSR2 Field Descriptions (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>17–20
LCFTSSI
[0:3]</td><td>Last CFIFO to transfer commands through the eQADC SSI. Holds the CFIFO number of last CFIFO to have initiated a command transfer to an external command buffer through the eQADC SSI. LCFTSSI does not indicate the transmission of null messages. LCFTSSI has the following values:
<table>
<tr><th>LCFTSSI[0:3]</th><th>LCFTSSI Meaning</th></tr>
<tr><td>0b0000</td><td>Last command was transferred from CFIFO0</td></tr>
<tr><td>0b0001</td><td>Last command was transferred from CFIFO1</td></tr>
<tr><td>0b0010</td><td>Last command was transferred from CFIFO2</td></tr>
<tr><td>0b0011</td><td>Last command was transferred from CFIFO3</td></tr>
<tr><td>0b0100</td><td>Last command was transferred from CFIFO4</td></tr>
<tr><td>0b0101</td><td>Last command was transferred from CFIFO5</td></tr>
<tr><td>0b0110 – 0b1110</td><td>Reserved</td></tr>
<tr><td>0b1111</td><td>No command was transferred to an external command buffer</td></tr>
</table></td></tr>
<tr><td>21–31
TC_LCFTSSI
[0:10]</td><td>Transfer counter for last CFIFO to transfer commands through eQADC SSI. Indicates the number of commands which have been completely transferred from a particular CFIFO at the time a command transfer from that CFIFO to an external command buffer is initiated. TC_LCFTSSI is a copy of the corresponding TC_CFn in EQADC_CFTCRn (see Section 19.3.2.9, “eQADC CFIFO Transfer Counter Registers 0–5 (EQADC_CFTCRn)”) captured at the time a command transfer to an external command buffer is initiated. This field has no meaning when LCFTSSI is 0b1111.</td></tr>
</table>

19.3.2.11 eQADC CFIFO Status Register (EQADC_CFSR)

The EQADC_CFSR contains the current CFIFO status. The EQADC_CFSRs are read only. Writing to the EQADC_CFSR has no effect.

Address: Base + 0x00AC Access: RO

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	CFS0		CFS1		CFS2		CFS3		CFS4		CFS5		0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-14. eQADC CFIFO Status Register (EQADC_CFSR)

Table 19-17. EQADC_CFSR Field Descriptions

Field	Description
0–11 CFS*n* [0:1]	CFIFO status. Indicates the current status of CFIFO*n*. Refer to Table 19-18 for more information on CFIFO status.
12–31	Reserved.

Table 19-18. Current CFIFO Status

CFIFO Status	Field Value	Explanation
IDLE	0b00	• CFIFO is disabled. • CFIFO is in single-scan edge or level trigger mode and does not have EQADC_FISRn[SSS] asserted. • eQADC completed the transfer of the last entry of the user defined command queue in single-scan mode.
Reserved	0b01	Not applicable.
WAITING FOR TRIGGER	0b10	• CFIFO mode is modified to continuous-scan edge or level trigger mode. • CFIFO mode is modified to single-scan edge or level trigger mode and EQADC_FISRn[SSS] is asserted. • CFIFO mode is modified to single-scan software trigger mode and EQADC_FISRn[SSS] is negated. • CFIFO is paused. • eQADC transferred the last entry of the queue in continuous-scan edge trigger mode.
TRIGGERED	0b11	CFIFO is triggered

19.3.2.12 eQADC SSI Control Register (EQADC_SSICR)

The EQADC_SSICR configures the SSI submodule.

Address: Base + 0x00B4 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	MDT			0	0	0	0	BR			
W																
Reset	0	0	0	0	0	1	1	1	0	0	0	0	1	1	1	1

Figure 19-15. eQADC SSI Control Register (EQADC_SSICR)

Table 19-19. EQADC_SSICR Field Descriptions

Field	Description
0–20	Reserved.
21–23 MDT [0:2]	Minimum delay after transmission. Defines the minimum delay after transmission time (t_{MDT}) expressed in serial clock (FCK) periods. t_{MDT} is the minimum time $\overline{SDS}$ should be kept negated between two consecutive serial transmissions. Table 19-20 lists the minimum delay after transfer time according to how MDT is set. The MDT field must only be written when the serial transmissions from the eQADC SSI are disabled - Refer to EQADC_MCR[ESSIE] field in Section 19.3.2.1, “eQADC Module Configuration Register (EQADC_MCR)”.
24–27	Reserved.
28–31 BR [0:3]	Baud rate. Selects system clock divide factor as shown in Table 19-21. The baud clock is calculated by dividing the system clock by the clock divide factor specified with the BR field. **Note:** The BR field must only be written when the eQADC SSI is disabled - Refer to EQADC_MCR[ESSIE] field in Section 19.3.2.1, “eQADC Module Configuration Register (EQADC_MCR).”

Table 19-20. Minimum Delay After Transmission (t_{MDT}) Time

MDT	t_{MDT} (FCK period)
0b000	1
0b001	2
0b010	3
0b011	4
0b100	5
0b101	6
0b110	7
0b111	8

Table 19-21. System Clock Divide Factor for Baud Clock

BR[0:3]	System Clock Divide Factor [1]
0b0000	2
0b0001	3
0b0010	4
0b0011	5
0b0100	6
0b0101	7
0b0110	8
0b0111	9
0b1000	10
0b1001	11

Table 19-21. System Clock Divide Factor for Baud Clock (continued)

BR[0:3]	System Clock Divide Factor [1]
0b1010	12
0b1011	13
0b1100	14
0b1101	15
0b1110	16
0b1111	17

1 If the system clock is divided by a odd number then the serial clock has a duty cycle different from 50%.

19.3.2.13 eQADC SSI Receive Data Register (EQADC_SSIRDR)

The eQADC SSI receive data register (EQADC_SSIRDR) records the last message received from the external device.

Address: Base + 0x00B8 Access: RO

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	RDV	0	0	0	0	0	R_DATA									
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	R_DATA															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-16. eQADC SSI Receive Data Register (EQADC_SSIRDR)

Table 19-22. EQADC_SSIRDR Field Descriptions

Field	Description
0 RDV	Receive data valid. Indicates if the last received data is valid. This bit is cleared automatically whenever the EQADC_SSIRDR is read. Writes have no effect. 0 Receive data is not valid. 1 Receive data is valid.
1–5	Reserved.
6–31 R_DATA [0:25]	eQADC receive DATA. Contains the last result message that was shifted in. Writes to the R_DATA have no effect. Messages that were not completely received due to a transmission abort is not copied into EQADC_SSIRDR.

19.3.2.14 eQADC CFIFO Registers (EQADC_CF[0–5]R*n*)

EQADC_CF[0–5]R*n* provide visibility of the contents of a CFIFO for debugging purposes. Each CFIFO has four registers that are uniquely mapped to its four 32-bit entries. Refer to Section 19.4.3, "eQADC Command FIFOs," for more information on CFIFOs. These registers are read only. Data written to these registers is ignored.

Address: CFIFO0: Base + 0x0100 (CF0R0) Access: RO
Base + 0x0104 (CF0R1)
Base + 0x0108 (CF0R2)
Base + 0x010C (CF0R3)
CFIFO1: Base + 0x0140 (CF1R0)
Base + 0x0144 (CF1R1)
Base + 0x0148 (CF1R2)
Base + 0x014C (CF1R3)
CFIFO2: Base + 0x0180 (CF2R0)
Base + 0x0184 (CF2R1)
Base + 0x0188 (CF2R2)
Base + 0x018C (CF2R3)

CFIFO3: Base + 0x01C0 (CF3R0)
Base + 0x01C4 (CF3R1)
Base + 0x01C8 (CF3R2)
Base + 0x01CC (CF3R3)
CFIFO4: Base + 0x0200 (CF4R0)
Base + 0x0204 (CF4R1)
Base + 0x0208 (CF4R2)
Base + 0x020C (CF4R3)
CFIFO5: Base + 0x0240 (CF5R0)
Base + 0x0244 (CF5R1)
Base + 0x0248 (CF5R2)
Base + 0x024C (CF5R3)

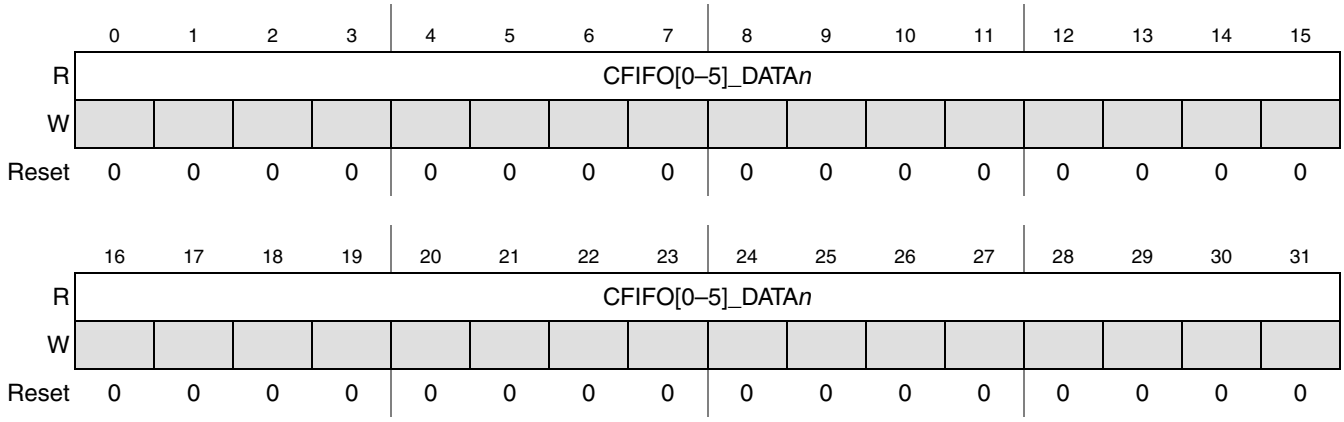


Figure 19-17. eQADC CFIF0[0–5] Registers (EQADC_CF[0–5]R*n*)

Table 19-23. EQADC_CF[0–5]R*n* Field Descriptions

Field	Description
0–31 CFIFO[0–5] _DATA*n* [0:31]	CFIFO[0–5]_data*n*. Returns the value stored within the entry of CFIFO[0–5]. Each CFIFO is composed of four 32-bit entries, with register 0 being mapped to the entry with the smallest memory mapped address.

19.3.2.15 eQADC RFIFO Registers (EQADC_RF[0–5]R*n*)

EQADC_RF[0–5]R*n* provide visibility of the contents of a RFIFO for debugging purposes. Each RFIFO has four registers which are uniquely mapped to its four 16-bit entries. Refer to Section 19.4.4, "Result FIFOs," for more information on RFIFOs. These registers are read only. Data written to these registers is ignored.

Address: RFIFO0: Base + 0x0300 (RF0R0) Access: RO
Base + 0x0304 (RF0R1)
Base + 0x0308 (RF0R2)
Base+0x030C (RF0R3)
RFIFO1: Base + 0x0340 (RF1R0)
Base + 0x0344 (RF1R1)
Base + 0x0348 (RF1R2)
Base + 0x034C (RF1R3)
RFIFO2: Base + 0x0380 (RF2R0)
Base + 0x0384 (RF2R1)
Base + 0x0388 (RF2R2)
Base + 0x038C (RF2R3)

RFIFO3: Base + 0x03C0 (RF3R0)
Base + 0x03C4 (RF3R1)
Base + 0x03C8 (RF3R2)
Base + 0x03CC (RF3R3)
RFIFO4: Base + 0x0400 (RF4R0)
Base + 0x0404 (RF4R1)
Base + 0x0408 (RF4R2
Base + 0x040C (RF4R3)
RFIFO5: Base + 0x0440 (RF5R0)
Base + 0x0444 (RF5R1)
Base + 0x0448 (RF5R2)
Base + 0x044C (RF5R3)

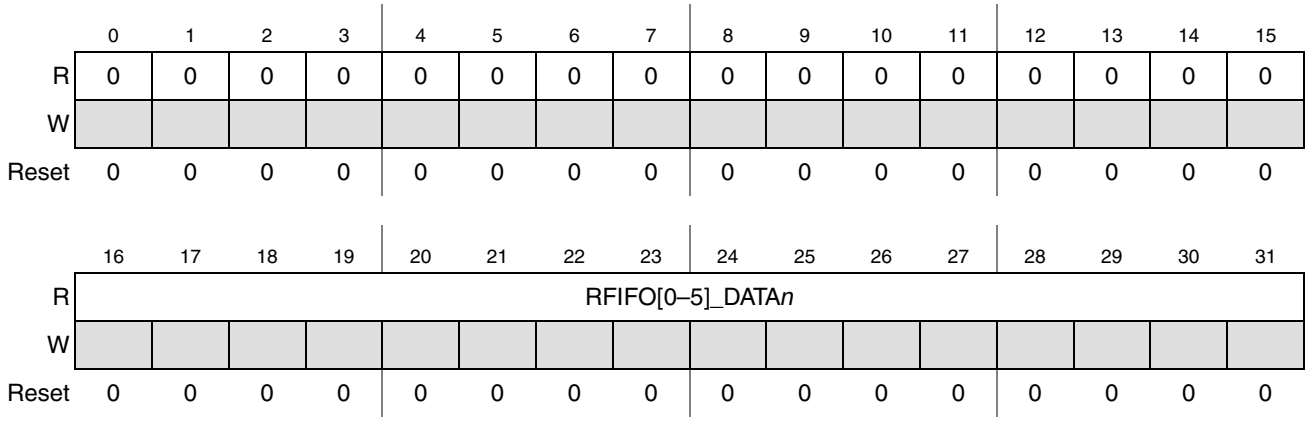


Figure 19-18. eQADC RFIFO*n* Registers (EQADC_RF[0–5]R*n*)

Table 19-24. EQADC_RF[0–5]R*n* Field Descriptions

FieIld	Description
0–31 RFIFO[0–5] _DATA*n* [0:15]	RFIFO[0–5] data *n*. Returns the value stored within the entry of RFIFO[0–5]. Each RFIFO is composed of four 16-bit entries, with register 0 being mapped to the entry with the smallest memory mapped address.

19.3.3 On-Chip ADC Registers

This section describes a list of registers that control on-chip ADC operation. The ADC registers are not part of the CPU accessible memory map. These registers can only be accessed indirectly through configuration commands. There are five non memory mapped registers per ADC, five for ADC0 and five for ADC1. The address, usage, and access privilege of each register is shown in Table 19-25 and Table 19-26. Data written to or read from reserved areas of the memory map is undefined.

Their assigned addresses are the values used to set the ADC_REG_ADDRESS field of the read/write configuration commands bound for the on-chip ADCs. These are halfword addresses. Further, the following restrictions apply when accessing these registers:

- Registers ADC0_CR, ADC0_GCCR, and ADC0_OCCR can only be accessed by configuration commands sent to the ADC0 command buffer.
- Registers ADC1_CR, ADC1_GCCR, and ADC1_OCCR can only be accessed by configuration commands sent to the ADC1 command buffer.
- Registers ADC_TSCR and ADC_TBCR can be accessed by configuration commands sent to the ADC0 command buffer or to the ADC1 command buffer. A data write to ADC_TSCR through a configuration command sent to the ADC0 command buffer writes the same memory location as when writing to it through a configuration command sent to the ADC1 command buffer. The same is valid for ADC_TBCR.

NOTE

Simultaneous write accesses from the ADC0 and ADC1 command buffers to ADC_TSCR or to ADC_TBCR are not allowed.

Table 19-25. ADC0 Registers

ADC0 Register Address	Use	Access
0x0000	ADC0 Address 0x00 is used for conversion command messages.	
0x0001	ADC0 Control Register (ADC0_CR)	Write/Read
0x0002	ADC Time Stamp Control Register (ADC_TSCR) [1]	Write/Read
0x0003	ADC Time Base Counter Register (ADC_TBCR) [1]	Write/Read
0x0004	ADC0 Gain Calibration Constant Register (ADC0_GCCR)	Write/Read
0x0005	ADC0 Offset Calibration Constant Register (ADC0_OCCR)	Write/Read
0x0006–0x00FF	Reserved	—

[1] This register is also accessible by configuration commands sent to the ADC1 command buffer.

Table 19-26. ADC1 Registers

ADC1 Register Address	Use	Access
0x0000	ADC1 Address 0x00 is used for conversion command messages.	
0x0001	ADC1 Control Register (ADC1_CR)	Write/Read

Table 19-26. ADC1 Registers (continued)

0x0002	ADC Time Stamp Control Register (ADC_TSCR) [1]	Write/Read
0x0003	ADC Time Base Counter Register (ADC_TBCR) [1]	Write/Read
0x0004	ADC1 Gain Calibration Constant Register (ADC1_GCCR)	Write/Read
0x0005	ADC1 Offset Calibration Constant Register (ADC1_OCCR)	Write/Read
0x0006–0x00FF	Reserved	—

[1] This register is also accessible by configuration commands sent to the ADC0 command buffer.

19.3.3.1 ADC*n* Control Registers (ADC0_CR and ADC1_CR)

The ADC*n* control registers (ADC*n*_CR) are used to configure the on-chip ADCs.

Address: 0x0001 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	ADC0_EN	0	0	0	ADC0_EMUX	0	0	0	0	0	0	ADC0_CLK_PS				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	ADC1_EN	0	0	0	ADC1_EMUX	0	0	0	0	0	0	ADC1_CLK_PS				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Figure 19-19. ADC*n* Control Registers (ADC0_CR and ADC1_CR)

Table 19-27. ADC*n*_CR Field Descriptions

Field	Description
0 ADC*n*_EN	ADC*n* enable. Enables ADC*n* to perform A/D conversions. Refer to Section 19.4.5.1, "Enabling and Disabling the on-chip ADCs," for details. 0 ADC is disabled. Clock supply to ADC0/1 is stopped. 1 ADC is enabled and ready to perform A/D conversions. **Note:** The bias generator circuit inside the ADC ceases functioning when both ADC0_EN and ADC1_EN bits are negated. **Note:** Conversion commands sent to a disabled ADC are ignored by the ADC control hardware. **Note:** When the ADC*n*_EN status is changed from asserted to negated, the ADC clock does not stop until it reaches its low phase.
1–3	Reserved.

Table 19-27. ADC*n*_CR Field Descriptions (continued)

Field	Description
4 ADC*n*_ EMUX	ADC*n* external multiplexer enable. When ADC*n*_EMUX is asserted, the MA pins output digital values to the external channel number selected to convert external multiplexer inputs. Refer to Section 19.4.6, "Internal/External Multiplexing," for a detailed description about how ADC*n*_EMUX affects channel number decoding. 0 External multiplexer disabled; no external multiplexer channels can be selected. 1 External multiplexer enabled; external multiplexer channels can be selected. **Note:** Both ADC*n*_EMUX bits must not be asserted at the same time. **Note:** The ADC*n*_EMUX bit must only be written when the ADC*n*_EN bit is negated. ADC*n*_EMUX can be set during the same write cycle used to set ADC*n*_EN.
5–10	Reserved.
11–15 ADC*n*_ CLK_PS [0:4]	ADC*n* clock prescaler. The ADC*n*_CLK_PS field controls the system clock divide factor for the ADC*n* clock as in Table 19-28. Refer to Section 19.4.5.2, "ADC Clock and Conversion Speed," for details about how to set ADC0/1_CLK_PS. The ADC*n*_CLK_PS field must only be written when the ADC*n*_EN bit is negated. This field can be configured during the same write cycle used to set ADC*n*_EN.

Table 19-28. System Clock Divide Factor for ADC Clock

ADC*n*_CLK_PS[0:4]	System Clock Divide Factor
0b00000	2
0b00001	4
0b00010	6
0b00011	8
0b00100	10
0b00101	12
0b00110	14
0b00111	16
0b01000	18
0b01001	20
0b01010	22
0b01011	24
0b01100	26
0b01101	28
0b01110	30
0b01111	32
0b10000	34
0b10001	36
0b10010	38

Table 19-28. System Clock Divide Factor for ADC Clock (continued)

ADC*n*_CLK_PS[0:4]	System Clock Divide Factor
0b10011	40
0b10100	42
0b10101	44
0b10110	46
0b10111	48
0b11000	50
0b11001	52
0b11010	54
0b11011	56
0b11100	58
0b11101	60
0b11110	62
0b11111	64

19.3.3.2 ADC Time Stamp Control Register (ADC_TSCR)

The ADC_TSCR contains a system clock divide factor used in the making of the time base counter clock. It determines at what frequency the time base counter runs. ADC_TSCR can be accessed by configuration commands sent to ADC0 or to ADC1. A data write to ADC_TSCR using a configuration command sent to ADC0 writes to the same memory location as a write using a configuration command sent to ADC1.

NOTE

Simultaneous write accesses from ADC0 and ADC1 to ADC_TSCR are not allowed.

Address: 0x0002 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	TBC_CLK_PS			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-20. ADC Time Stamp Control Register (ADC_TSCR)

Table 19-29. ADC_TSCR Field Descriptions

Field	Description
0–11	Reserved.
12–15 TBC_ CLK_PS [0:3]	Time base counter clock prescaler. Contains the system clock divide factor for the time base counter. It controls the accuracy of the time stamp. The prescaler is disabled when TBC_CLK_PS is set to 0b0000.

Table 19-30. Clock Divide Factor for Time Stamp

TBC_CLK_PS[0:3]	System Clock Divide Factor	Clock to Time Stamp Counter for a 120 MHz System Clock (MHz)
0b0000	Disabled	Disabled
0b0001	1	120
0b0010	2	60
0b0011	4	30
0b0100	6	20
0b0101	8	15
0b0110	10	12
0b0111	12	10
0b1000	16	7.5
0b1001	32	3.75
0b1010	64	1.88
0b1011	128	0.94
0b1100	256	0.47
0b1101	512	0.23
0b1110–0b1111	Reserved	—

NOTE

If TBC_CLK_PS is not set to disabled, it must not be changed to any other value besides disabled. If TBC_CLK_PS is set to disabled it can be changed to any other value.

19.3.3.3 ADC Time Base Counter Registers (ADC_TBCR)

The ADC_TBCR contains the current value of the time base counter. ADC_TBCR can be accessed by configuration commands sent to ADC0 or to ADC1. A data write to ADC_TBCR using a configuration command sent to ADC0 writes the same memory location as a write using a configuration command sent to ADC1.

NOTE

Simultaneous write accesses from ADC0 and ADC1 to ADC_TBCR are not allowed.

Address: 0x0003 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	TBC_VALUE															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-21. ADC Time Base Counter Register (ADC_TBCR)

Table 19-31. ADC_TBCR Field Descriptions

Field	Description
0–15 TBC_ VALUE [0:15]	Time base counter VALUE. Contains the current value of the time base counter. Reading TBC_VALUE returns the current value of time base counter. Writes to TBC_VALUE register load the written data to the counter. The time base counter counts from 0x0000 to 0xFFFF and wraps when reaching 0xFFFF.

19.3.3.4 ADC*n* Gain Calibration Constant Registers (ADC0_GCCR and ADC1_GCCR)

The ADC*n*_GCCR contains the gain calibration constant used to fine-tune the ADC*n* conversion results. Refer to Section 19.4.5.4, "ADC Calibration Feature," for details about the calibration scheme used in the eQADC.

Address: 0x0004 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	GCC0														
W																
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	GCC1														
W																
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-22. ADC*n* Gain Calibration Constant Registers (ADC*n*_GCCR)

Table 19-32. ADC*n*_GCCR Field Descriptions

Field	Description
0	Reserved.
1–15 GCC*n* [0:14]	ADC*n* gain calibration constant (GCC1) is an unsigned 15-bit fixed pointed number expressed in the *GCC_INT.GCC_FRAC* binary format. Use the gain calibration constant to fine-tune ADC*n* conversion results. The integer part of the gain constant (GCC_INT) contains a single binary digit while its fractional part (GCC_FRAC) contains 14 digits. For details about the GCC data format refer to Section 19.4.5.4.2, "MAC Unit and Operand Data Format."

19.3.3.5 ADC*n* Offset Calibration Constant Registers (ADC0_OCCR and ADC1_OCCR)

The ADC*n*_OCCR contains the offset calibration constant used to fine-tune of ADC0/1 conversion results. The offset constant is a signed 14-bit integer value. Refer to Section 19.4.5.4, "ADC Calibration Feature," for details about the calibration scheme used in the eQADC.

Address: 0x0005 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	OCC0													
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	OCC1													
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 19-23. ADC*n* Offset Calibration Constant Registers (ADC*n*_OCCR)

Table 19-33. ADC*n*_OCCR Field Descriptions

Field	Description
0–1	Reserved.
2–15 OCC*n* [0:13]	ADC*n* offset calibration constant. Contains the offset calibration constant used to fine-tune ADC*n* conversion results. Use the two's complement representation for expressing negative values.

19.4 Functional Description

The eQADC provides a parallel interface to two on-chip ADCs, and a single master to single slave serial interface to an off-chip external device. The two on-chip ADCs can access all the analog channels.

Initially, command data is contained in system memory in a user defined data queue structure. Command data is moved between the user-defined queues and CFIFOs by the host CPU or by the eDMA which responds to interrupt and eDMA requests generated by the eQADC. The eQADC supports software and

hardware triggers from other modules or external pins to initiate transfers of commands from the multiple CFIFOs to the on-chip ADCs or to the external device.

CFIFOs can be configured to be in single-scan or continuous-scan mode. When a CFIFO is configured to be in single-scan mode, the eQADC scans the user-defined command queue one time. The eQADC stops transferring commands from the triggered CFIFO after detecting the EOQ bit set in the last transfer. After an EOQ bit is detected, software involvement is required to rearm the CFIFO so that it can detect new trigger events.

When a CFIFO is configured for continuous-scan mode, the whole user command queue is scanned multiple times. After the detection of an asserted EOQ bit in the last command transfer, command transfers can continue or not depending on the mode of operation of the CFIFO.

The eQADC can also in parallel and independently of the CFIFOs receive data from the on-chip ADCs or from off-chip external device into multiple RFIFOs. Result data is moved from the RFIFOs to the user-defined result queues in system memory by the host CPU or by the eDMA.

19.4.1 Data Flow in the eQADC

Figure 19-24 shows how command data flows inside the eQADC system. A command message is the predefined format in which command data is stored in the user-defined command queues. A command message has 32 bits and is composed of two parts: a CFIFO header and an ADC command. Command messages are moved from the user command queues to the CFIFOs by the host CPU or by the eDMA as they respond to interrupt and eDMA requests generated by the eQADC. The eQADC generates these requests whenever a CFIFO is not full. The FIFO control unit transfers only the command part of the command message to the ADC. Information in the CFIFO header together with the upper bit of the ADC command is used by the FIFO control unit to arbitrate which triggered CFIFO transfers the next command. Because command transfer through the serial interface can take significantly more time than a parallel transfer to the on-chip ADCs, command transfers for on-chip ADCs occur concurrently with the transfers through the serial interface. Commands sent to the ADCs are executed in a first-in-first-out (FIFO) basis and three types of results can be expected: data read from an ADC register, a conversion result, or a time stamp. The order at which ADC commands sent to the external device are executed, and the type of results that can be expected depends on the architecture of that device with the exception of unsolicited data like null messages for example.

NOTE

While the eQADC pops commands out from a CFIFO, it also is checking the number of entries in the CFIFO and generating requests to fill it. The process of pushing and popping commands to and from a CFIFO can occur simultaneously.

The FIFO control unit expects all incoming results to be shaped in a pre-defined result message format. Figure 19-25 shows how result data flows inside the eQADC system. Results generated on the on-chip ADCs are formatted into result messages inside the result format and calibration submodule. Results returning from the external device are already formatted into result messages and therefore bypass the result format and calibration submodule located inside the eQADC. A result message is composed of an RFIFO header and an ADC Result. The FIFO control unit decodes the information contained in the RFIFO

header to determine the RFIFO to which the ADC result should be sent. After in an RFIFO, the ADC result is moved to the corresponding user result queue by the host CPU or by the eDMA as they respond to interrupt and eDMA requests generated by the eQADC. The eQADC generates these requests whenever an RFIFO has at least one entry.

NOTE

While conversion results are returned, the eQADC is checking the number of entries in the RFIFO and generating requests to empty it. The process of pushing and popping ADC results to and from an RFIFO can occur simultaneously.

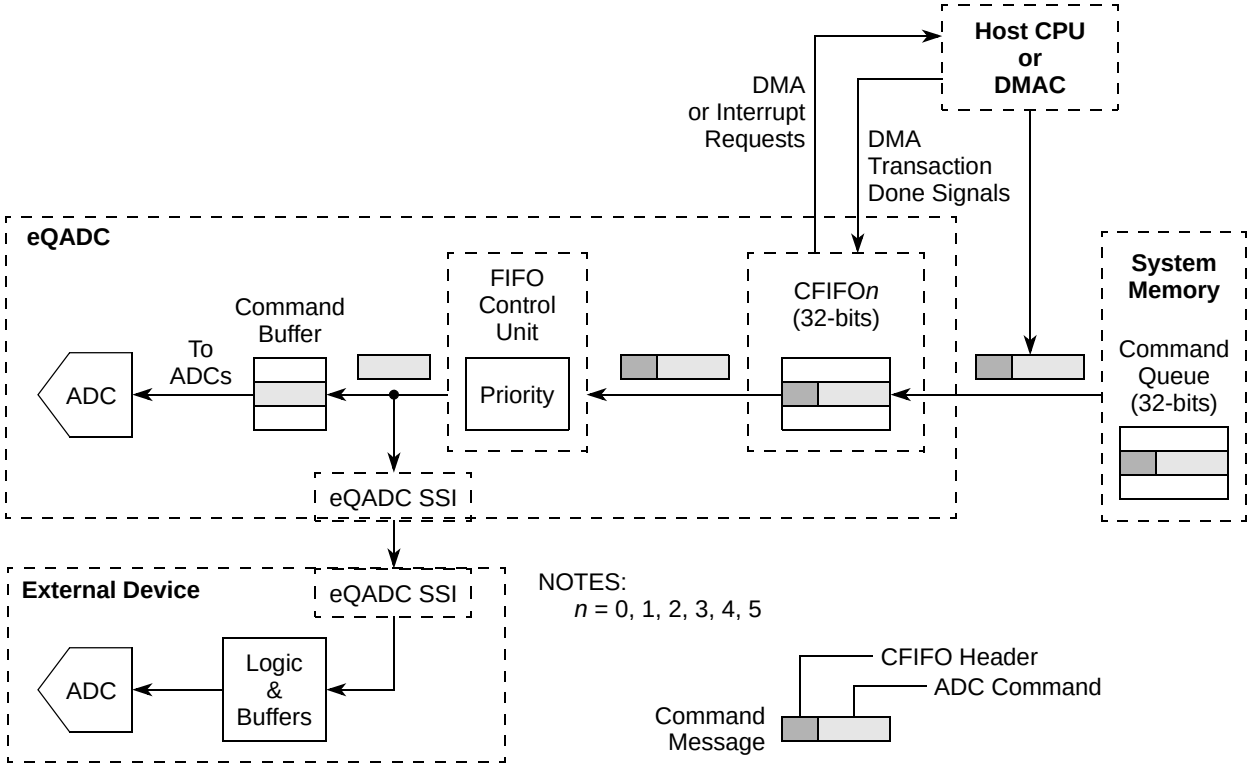


Figure 19-24. Command Flow During eQADC Operation

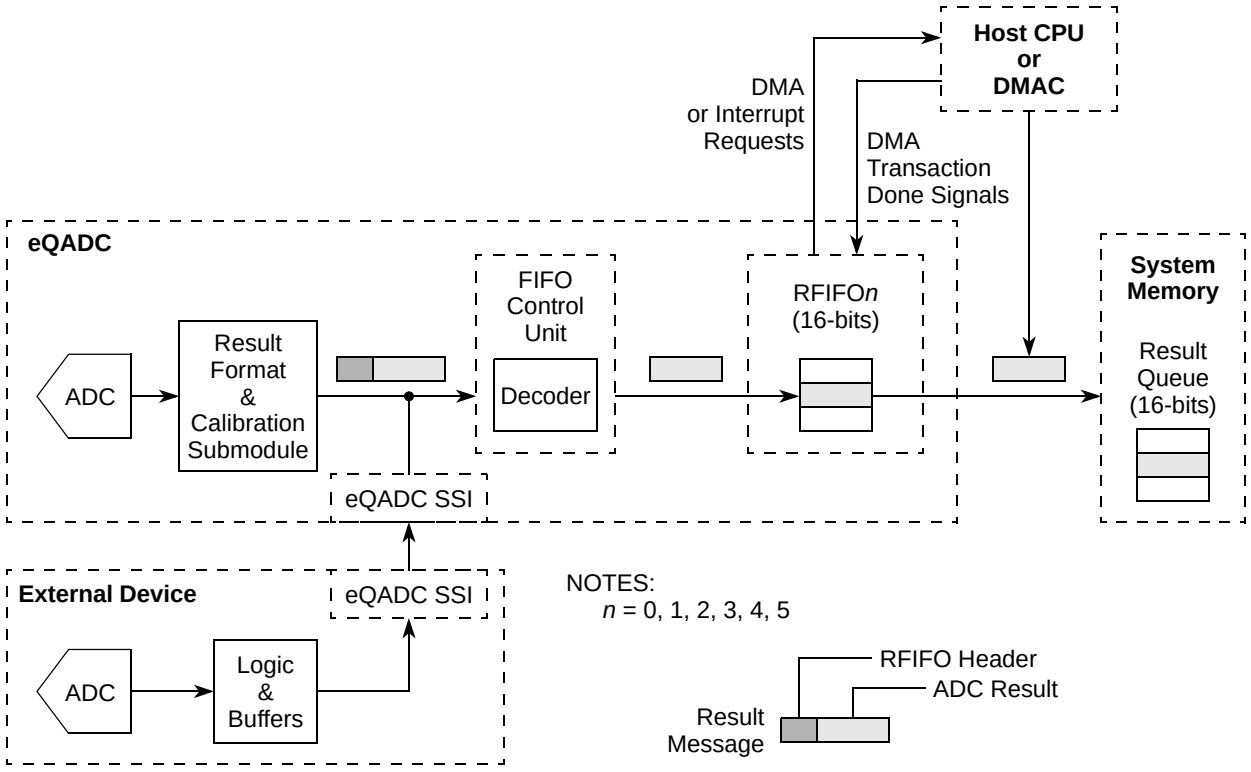


Figure 19-25. Result Flow During eQADC Operation

19.4.1.1 Assumptions/Requirements Regarding the External Device

The external device exchanges command and result data with the eQADC through the eQADC SSI interface. This section explains the minimum requirements an external device has to meet to properly interface with the eQADC. Some assumptions about the architecture of the external device are also described.

19.4.1.1.1 eQADC SSI Protocol Support

The external device must fully support the eQADC SSI protocol as specified in Section 19.4.8, “eQADC Synchronous Serial Interface (SSI) Submodule,” section of this document. Support for the abort feature is optional. When aborts are not supported, all command messages bound for an external command buffer must have the ABORT_ST bit negated - see Section , “ Command Message Format for External Device Operation.”

19.4.1.1.2 Number of Command Buffers and Result Buffers

The external device should have a minimum of one and a maximum of two command buffers to store command data sent from the eQADC. If more than two command buffers are implemented in the external device, they are not recognized by the eQADC as valid destinations for commands. In this document, the two valid external command buffers are referred to as command buffer 2 and command buffer 3 (the two on-chip ADCs being command buffer 0 and 1). The external device decides to which external command buffer a command should go by decoding the upper bit (BN bit) of the ADC command - see Section ,

" Command Message Format for External Device Operation." An external device that only implements one command buffer can ignore the BN bit.

The limit of two command buffers does not limit the number of result buffers in the slave device.

19.4.1.1.3 Command Execution and Result Return

Commands sent to a specific external command buffer should be executed in the order they were received.

Results generated by the execution of commands in an external command buffer should be returned in the order that the command buffer received these commands.

19.4.1.1.4 Null and Result Messages

The external device must be capable of correctly processing null messages as specified in the Section 19.3.2.2, "eQADC Null Message Send Format Register (EQADC_NMSFR)."

In case no valid result data is available to be sent to the eQADC, the external device must send data in the format specified in Section , "Null Message Format for External Device Operation."

In case valid result data is available to sent to the eQADC, the external device must send data in the format specified in Section , "Result Message Format for External Device Operation."

The BUSY0/1 fields of all messages sent from the external device to the eQADC must be correctly encoded according to the latest information on the fullness state of the command buffers. For example, if external command buffer 2 is empty before the end of the current serial transmission and if at the end of this transmission the external device receives a command to command buffer 2, then the BUSY0 field, that is to be sent to the eQADC on the next serial transmission, should be encoded assuming that the external command buffer has one entry.

19.4.1.2 Message Format in eQADC

This section explains the command and result message formats used for on-chip ADC operation and for external device operation.

A command message is the pre-defined format at which command data is stored in the user command queues. A command message has 32 bits and is composed of two parts: a CFIFO header and an ADC command. The size of the CFIFO header is fixed to 6 bits, and it works as inputs to the FIFO control unit. The header controls when a command queue ends, when it pauses, if commands are sent to internal or external buffers, and if it can abort a serial data transmission. Information contained in the CFIFO header, together with the upper bit of the ADC command, is used by the FIFO control unit to arbitrate which triggered CFIFO transfers the next command. ADC commands are encoded inside the least significant 26 bits of the command message.

A result message is composed of an RFIFO header and an ADC result. The FIFO control unit decodes the information contained in the RFIFO header to determine the RFIFO to which the ADC result is sent. The ADC result field is always 16 bits.

19.4.1.2.1 Message Formats for On-Chip ADC Operation

This section describes the command/result message formats used for on-chip ADC operation.

NOTE

Although this subsection describes how the command and result messages are formatted to communicate with the on-chip ADCs, nothing prevents the programmer from using a different format when communicating with an external device through the serial interface. Refer to Section 19.4.1.2.2, "Message Formats for External Device Operation." Apart from the BN bit, the ADC command of a command message can be formatted to communicate to an arbitrary external device provided that the device returns an RFIFO header in the format expected by the eQADC. When the FIFO control unit receives return data message, it decodes the message tag field and stores the 16-bit data into the corresponding RFIFO.

Conversion Command Message Format for On-Chip ADC Operation

Figure 19-26 describes the command message format for conversion commands when interfacing with the on-chip ADCs. A conversion result is always returned for conversion commands and time stamp information can be optionally requested. The lower byte of conversion commands is always cleared to 0 to distinguish it from configuration commands.

Address: 0x0005 Access: R/W

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
EOQ	PAUSE	Reserved			EB (0b0)	BN	CAL	MESSAGE_TAG				LST		TSR	FMT
CFIFO Header								ADC Command							

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CHANNEL_NUMBER								ADC_REG_ADDRESS							
Address Field															

Figure 19-26. Conversion Command Message Format for On-Chip ADC Operation

Table 19-34. On-Chip ADC Field Descriptions: Conversion Command Message Format

Field	Description
0 EOQ	End-of-queue. Asserted in the last command of a command queue to indicate to the eQADC that a scan of the queue is completed. EOQ instructs the eQADC to reset its current CFIFO transfer counter value (TC_CF) to 0. Depending on the CFIFO operating mode, the CFIFO status changes when it detects when the EOQ bit on the last transferred command is asserted. Refer to Section 19.4.3.5, "CFIFO Scan Trigger Modes," for details. 0 Not the last entry of the command queue. 1 Last entry of the command queue. **Note:** If both the pause and EOQ bits are asserted in the same command message the respective flags are set, but the CFIFO status changes as if only the EOQ bit were asserted.
1 PAUSE	Pause. Allows software to create sub-queues within a command queue. When the eQADC completes the transfer of a command with an asserted pause bit, the CFIFO enters the WAITING FOR TRIGGER state. Refer to Section 19.4.3.6.1, "CFIFO Operation Status," for a description of the state transitions. The pause bit is only valid when CFIFO operation mode is configured to single or continuous-scan edge trigger mode. 0 Do not enter WAITING FOR TRIGGER state after transfer of the current command message. 1 Enter WAITING FOR TRIGGER state after transfer of the current command message. **Note:** If both the pause and EOQ bits are asserted in the same command message the respective flags are set, but the CFIFO status changes as if only the EOQ bit were asserted.
2–4	Reserved.
5 EB	External buffer bit. A negated EB bit indicates that the command is sent to an on chip ADC. 0 Command is sent to an internal buffer. 1 Command is sent to an external buffer.
6 BN	Buffer number. For internal commands, ADCs 1 and 0 can be internal or external depending on the EBI bit setting. 0 Message ADC 0. 1 Message ADC 1.
7 CAL	Calibration. Indicates if the returning conversion result must be calibrated. 0 Do not calibrate conversion result. 1 Calibrate conversion result.

Table 19-34. On-Chip ADC Field Descriptions: Conversion Command Message Format (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>8–11
MESSAGE_
TAG
[0:3]</td><td>MESSAGE_TAG field. Allows the eQADC to separate returning results into different RFIFOs. When the eQADC transfers a command, the MESSAGE_TAG is included as part of the command. Eventually the external device/on-chip ADC returns the result with the same MESSAGE_TAG. The eQADC separates incoming messages into different RFIFOs by decoding the MESSAGE_TAG of the incoming data.
<table>
<tr><th>MESSAGE_TAG[0:3]</th><th>MESSAGE_TAG Meaning</th></tr>
<tr><td>0b0000</td><td>Result is sent to RFIFO 0</td></tr>
<tr><td>0b0001</td><td>Result is sent to RFIFO 1</td></tr>
<tr><td>0b0010</td><td>Result is sent to RFIFO 2</td></tr>
<tr><td>0b0011</td><td>Result is sent to RFIFO 3</td></tr>
<tr><td>0b0100</td><td>Result is sent to RFIFO 4</td></tr>
<tr><td>0b0101</td><td>Result is sent to RFIFO 5</td></tr>
<tr><td>0b0110–0b0111</td><td>Reserved</td></tr>
<tr><td>0b1000</td><td>Null message received</td></tr>
<tr><td>0b1001</td><td>Reserved for customer use. [1]</td></tr>
<tr><td>0b1010</td><td>Reserved for customer use. [1]</td></tr>
<tr><td>0b1011–0b1111</td><td>Reserved</td></tr>
</table>
[1] These messages are treated as null messages. Therefore, they must obey the format for incoming null messages and return valid BUSY0/1 fields. Refer to Section , “Null Message Format for External Device Operation.”</td></tr>
<tr><td>12–13
LST
[0:1]</td><td>Long sampling time. These two bits determine the duration of the sampling time in ADC clock cycles.
Note: For external mux mode, 64 or 128 sampling cycles is recommended.
<table>
<tr><th>LST[0:1]</th><th>Sampling cycles (ADC Clock Cycles)</th></tr>
<tr><td>0b00</td><td>2</td></tr>
<tr><td>0b01</td><td>8</td></tr>
<tr><td>0b10</td><td>64</td></tr>
<tr><td>0b11</td><td>128</td></tr>
</table></td></tr>
<tr><td>14
TSR</td><td>Time stamp request. TSR indicates the request for a time stamp. When TSR is asserted, the on-chip ADC control logic returns a time stamp for the current conversion command after the conversion result is sent to the RFIFOs. Refer to Section 19.4.5.3, “Time Stamp Feature,” for details.
0 Return conversion result only.
1 Return conversion time stamp after the conversion result.</td></tr>
<tr><td>15
FMT</td><td>Conversion data format. FMT specifies to the eQADC how to format the 12-bit conversion data returned by the ADCs into the 16-bit format which is sent to the RFIFOs. Refer to Section , “ADC Result Format for On-Chip ADC Operation,” for details.
0 Right justified unsigned.
1 Right justified signed.</td></tr>
</table>

Table 19-34. On-Chip ADC Field Descriptions: Conversion Command Message Format (continued)

Field	Description
16–23 CHANNEL_ NUMBER [0:7]	Channel number. Selects the analog input channel. The software programs this field with the channel number corresponding to the analog input pin to be sampled and converted. Refer to Section 19.4.6.1, "Channel Assignment," for details.
24–31 ADC_REG_ ADDRESS [0:7]	ADC register address. Identifies the address of the ADC register. Only use 16-bit (halfword) addresses. Refer to Table 19-25. Include $00 for conversion commands.

Write Configuration Command Message Format for On-Chip ADC Operation

Figure 19-27 describes the command message format for a write configuration command when interfacing with the on-chip ADCs. A write configuration command is used to set the control registers of the on-chip ADCs. No conversion data is returned for a write configuration command. Write configuration commands are differentiated from read configuration commands by a negated R/W bit.

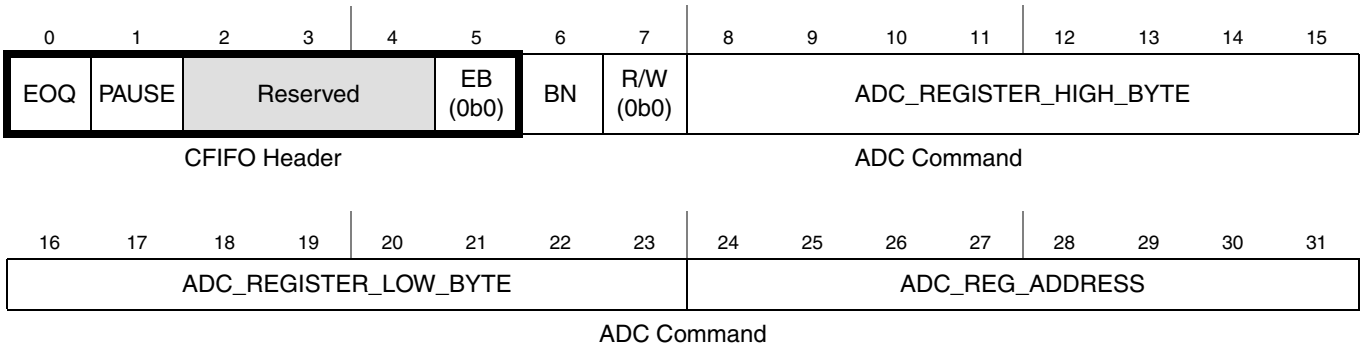


Figure 19-27. Write Configuration Command Message Format for On-chip ADC Operation

Table 19-35. On-Chip ADC Field Descriptions: Write Configuration

Field	Description
0 EOQ	End-of-queue. Asserted in the last command of a command queue to indicate to the eQADC that a scan of the queue is completed. EOQ instructs the eQADC to reset its current CFIFO transfer counter value (TC_CF) to 0. Depending on the CFIFO mode of operation, the CFIFO status also changes upon the detection of an asserted EOQ bit on the last transferred command. Refer to Section 19.4.3.5, "CFIFO Scan Trigger Modes," for details. 0 Not the last entry of the command queue. 1 Last entry of the command queue. **Note:** If both the pause and EOQ bits are asserted in the same command message the respective flags are set, but the CFIFO status changes as if only the EOQ bit were asserted.
1 PAUSE	Pause bit. Allows software to create sub-queues within a command queue. When the eQADC completes the transfer of a command with an asserted pause bit, the CFIFO enters the WAITING FOR TRIGGER state. Refer to Section 19.4.3.6.1, "CFIFO Operation Status," for a description of the state transitions. The pause bit is only valid when CFIFO operation mode is configured to single or continuous-scan edge trigger mode. 0 Do not enter WAITING FOR TRIGGER state after transfer of the current command message. 1 Enter WAITING FOR TRIGGER state after transfer of the current command message. **Note:** If both the pause and EOQ bits are asserted in the same command message, the respective flags are set, but the CFIFO status changes as if only the EOQ bit were asserted.

Table 19-35. On-Chip ADC Field Descriptions: Write Configuration

Field	Description
2–4	Reserved.
5 EB	External buffer bit. Always clear this bit for messages sent to an on-chip ADC. 0 Command is sent to an internal command buffer. 1 Command is sent to an external command buffer.
6 BN	Buffer number. Indicates to which buffer the message is sent.Buffers 1 and 0 can either be internal or external depending on the EBI bit setting. 0 Message buffer 0. 1 Message buffer 1.
7 R/W	Read/write. A negated R/W indicates a write configuration command. 0 Write 1 Read
8–15 ADC_ REGISTER _HIGH_ BYTE[0:7]	ADC register high byte. The value to be written into the most significant 8 bits of control/configuration register when the R/W bit is negated.
16–23 ADC_ REGISTER _LOW_ BYTE[0:7]	ADC register low byte. The value to be written into the least significant 8 bits of a control/configuration register when the R/W bit is negated.
24–31 ADC_REG_ ADDRESS [0:7]	ADC register address. Identifies to which ADC register the read or write is performed. Only use 16-bit (halfword) addresses. Refer to Table 19-25. Refer to Table 19-25.

Read Configuration Command Message Format for On-Chip ADC Operation

Figure 19-28 describes the command message format for a read configuration command when interfacing with the on-chip ADCs. A read configuration command is used to read the contents of the on-chip ADC registers which are only accessible via command messages. Read configuration commands are differentiated from write configuration commands by an asserted R/W bit.

Figure 19-28. Read Configuration Command Message Format for On-Chip ADC Operation

Table 19-36. On-Chip ADC Field Descriptions: Read Configuration

Field	Description
0 EOQ	End-of-queue. Asserted in the last command of a command queue to indicate to the eQADC that a scan of the queue is completed. EOQ instructs the eQADC to reset its current CFIFO transfer counter value (TC_CF) to 0. Depending on the CFIFO mode of operation, the CFIFO status changes upon the detection of an asserted EOQ bit on the last transferred command. Refer to Section 19.4.3.5, "CFIFO Scan Trigger Modes," for details. 0 Not the last entry of the command queue. 1 Last entry of the command queue. **Note:** If both the pause and EOQ bits are asserted in the same command message the respective flags are set, but the CFIFO status changes as if only the EOQ bit were asserted.
1 PAUSE	Pause bit. Allows software to create sub-queues within a command queue. When the eQADC completes the transfer of a command with an asserted pause bit, the CFIFO enters the WAITING FOR TRIGGER state. Refer to Section 19.4.3.6.1, "CFIFO Operation Status," for a description of the state transitions. The pause bit is only valid when CFIFO operation mode is configured to single or continuous-scan edge trigger mode. 0 Do not enter WAITING FOR TRIGGER state after transfer of the current command message. 1 Enter WAITING FOR TRIGGER state after transfer of the current command message. **Note:** If both the pause and EOQ bits are asserted in the same command message the respective flags are set, but the CFIFO status changes as if only the EOQ bit were asserted.
2–4	Reserved.
5 EB	External buffer bit. Always clear this bit for messages sent to an on-chip ADC. 0 Command is sent to an internal command buffer. 1 Command is sent to an external command buffer.
6 BN	Buffer number. Indicates to which buffer the message is sent. Buffers 1 and 0 can either be internal or external depending on the EBI bit setting. 0 Message buffer 0. 1 Message buffer 1.
7 R/W	Read/write. An asserted R/W bit indicates a read configuration command. 0 Write 1 Read

Table 19-36. On-Chip ADC Field Descriptions: Read Configuration (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>8–11
MESSAGE
_TAG[0:3]</td><td>MESSAGE_TAG field. Allows the eQADC to separate returning results into different RFIFOs. When the eQADC transfers a command, the MESSAGE_TAG is included as part of the command. Eventually the external device/on-chip ADC returns the result with the same MESSAGE_TAG. The eQADC separates incoming messages into different RFIFOs by decoding the MESSAGE_TAG of the incoming data.
<table>
<tr><th>MESSAGE_TAG[0:3]</th><th>MESSAGE_TAG Meaning</th></tr>
<tr><td>0b0000</td><td>Result is sent to RFIFO 0</td></tr>
<tr><td>0b0001</td><td>Result is sent to RFIFO 1</td></tr>
<tr><td>0b0010</td><td>Result is sent to RFIFO 2</td></tr>
<tr><td>0b0011</td><td>Result is sent to RFIFO 3</td></tr>
<tr><td>0b0100</td><td>Result is sent to RFIFO 4</td></tr>
<tr><td>0b0101</td><td>Result is sent to RFIFO 5</td></tr>
<tr><td>0b0110–0b0111</td><td>Reserved</td></tr>
<tr><td>0b1000</td><td>Null message received</td></tr>
<tr><td>0b1001</td><td>Reserved for customer use. [1]</td></tr>
<tr><td>0b1010</td><td>Reserved for customer use. [1]</td></tr>
<tr><td>0b1011–0b1111</td><td>Reserved</td></tr>
</table>
[1] These messages are treated as null messages. Therefore, they must obey the format for incoming null messages and return valid BUSY0/1 fields. Refer to Section , “Null Message Format for External Device Operation.”</td></tr>
<tr><td>12–23</td><td>Reserved.</td></tr>
<tr><td>24–31
ADC_REG_
ADDRESS
[0:7]</td><td>ADC register address. Identifies to which ADC register the read or write is performed. Only use 16-bit (halfword) addresses. Refer to Table 19-25. Refer to Table 19-25.</td></tr>
</table>

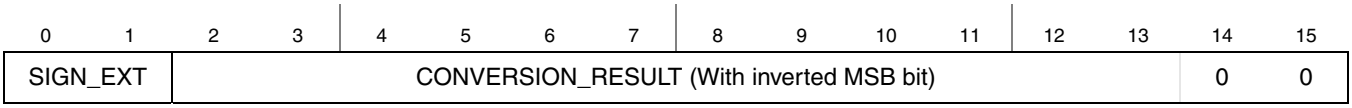
ADC Result Format for On-Chip ADC Operation

When the FIFO control unit receives a return data message, it decodes the MESSAGE_TAG field and stores the 16-bit data into the appropriate RFIFO. This section describes the ADC result portion of the result message returned by the on-chip ADCs.

The 16-bit data stored in the RFIFOs can be the following:

- Data read from an ADC register with a read configuration command. In this case, the stored 16-bit data corresponds to the contents of the ADC register that was read.
- A time stamp. In this case, the stored 16-bit data is the value of the time base counter latched when the eQADC detects the end of the analog input voltage sampling. For details see Section 19.4.5.3, “Time Stamp Feature.”
- A conversion result. In this case, the stored 16-bit data contains a right justified 14-bit result data. The conversion result can be calibrated or not depending on the status of CAL bit in the command that requested the conversion. When the CAL bit is negated, this 14-bit data is obtained by executing a 2-bit left-shift on the 12-bit data received from the ADC. When the CAL bit is asserted,

this 14-bit data is the result of the calculations performed in the EQADC MAC unit using the12-bit data received from the ADC and the calibration constants GCC and OCC (Refer to Section 19.4.5.4, “ADC Calibration Feature”). Then, this 14-bit data is further formatted into a 16-bit format according to the status of the FMT bit in the conversion command. When FMT is asserted, the 14-bit result data is reformatted to look as if it was measured against an imaginary ground at V_{REF} / 2 (the most significant bit (MSB) bit of the 14-bit result is inverted), and is sign-extended to a 16-bit format as in Figure 19-29. When FMT is negated, the eQADC zero-extends the 14-bit result data to a 16-bit format as in Figure 19-30. Correspondence between the analog voltage in a channel and the calculated digital values is shown in Table 19-39.

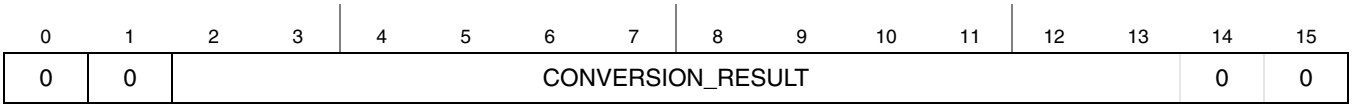


ADC Result

Figure 19-29. ADC Result Format when FMT = 1 (Right Justified Signed)—On-Chip ADC Operation

Table 19-37. ADC Result Format when FMT = 1 Field Descriptions

Field	Description
0–1 SIGN_ EXT[0:1]	Sign extension. Only has meaning when FMT is asserted. SIGN_EXT is 0b00 when CONVERSION_RESULT is positive, and 0b11 when CONVERSION_RESULT is negative.
2–15 CONVERSION _RESULT [0:13]	Conversion result. A digital value corresponding to the analog input voltage in a channel when the conversion command was initiated. The two’s complement representation is used to express negative values.



ADC Result

Figure 19-30. ADC Result Format when FMT = 0 (Right Justified Unsigned)—On-Chip ADC Operation

Table 19-38. ADC Result Format when FMT = 0 Field Descriptions

Field	Description
0–1 SIGN_ EXT[0:1]	Sign extension. These two bits are always zero for FMT=0 because unsigned results are positive.
2–15 CONVERSION _RESULT [0:13]	Conversion result. A digital value corresponding to the analog input voltage in a channel when the conversion command was initiated.

Table 19-39. Correspondence between Analog Voltages and Digital Values[1, 2]

	Voltage Level on Channel (V)	Corresponding 12-bit Conversion Result Returned by the ADC	16-bit Result Sent to RFIFOs (FMT=0) [3]	16-bit Result Sent to RFIFOs (FMT=1) [3]
Single-ended Conversions	5.12	0xFFF	0x3FFC	0x1FFC
	5.12 – LSB	0xFFF	0x3FFC	0x1FFC
	...	...	...	...
	2.56	0x800	0x2000	0x0000
	...	...	...	...
	1 LSB	0x001	0x0004	0xE004
	0	0x000	0x0000	0xE000
Differential Conversions	2.56	0xFFF	0x3FFC	0x1FFC
	2.56 – LSB	0xFFF	0x3FFC	0x1FFC
	...	...	...	...
	0	0x800	0x2000	0x0000
	...	...	...	...
	-2.56 + LSB	0x001	0x0004	0xE004
	-2.56	0x000	0x0000	0xE000

1 $V_{REF} = V_{RH} - V_{RL} = 5.12$ V. Resulting in one 12-bit count (LSB) =1.25 mV.

2 The two's complement representation is used to express negative values.

3 Assuming an accurately calibrated ADC with an ideal gain and a zero offset.

19.4.1.2.2 Message Formats for External Device Operation

This section describes the command messages, data messages, and null messages formats used for external device operation.

Command Message Format for External Device Operation

Figure 19-31 describes the command message format for external device operation. Command message formats for on-chip operation and for external device operation share the same CFIFO header format. However, there are no limitations regarding the format an ADC Command used to communicate to an arbitrary external device. Only the upper bit of an ADC Command has a fixed format (BN field) to indicate the FIFO control unit/external device to which the command and the external command buffer is sent. The remaining 25 bits can be anything decodable by the external device. Only the ADC command portion of a command message is transferred to the external device.

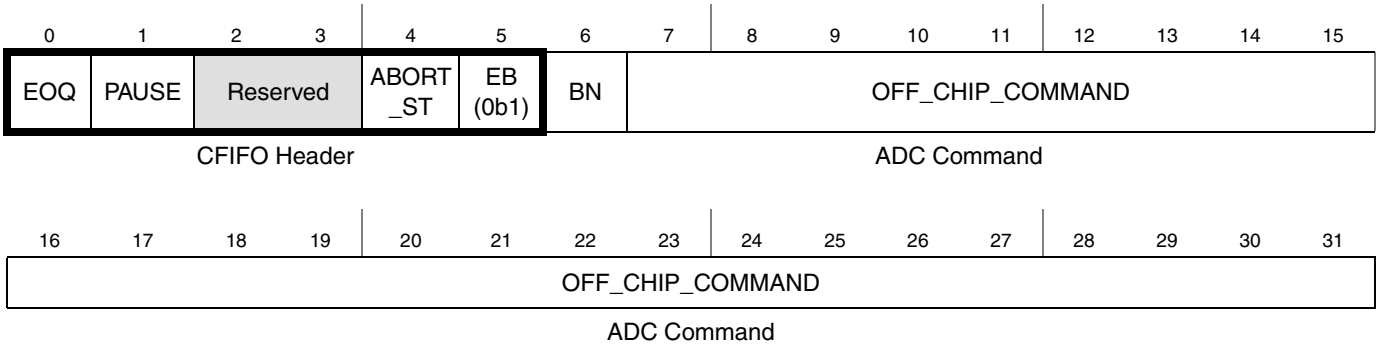


Figure 19-31. Command Message Format for External Device Operation

Table 19-40. On-Chip ADC Field Descriptions: External Device Operation

Field	Description
0 EOQ	End-of-queue. Asserted in the last command of a command queue to indicate to the eQADC that a scan of the queue is completed. EOQ instructs the eQADC to reset its current CFIFO transfer counter value (TC_CF) to 0. Depending on the CFIFO mode of operation, the CFIFO status changes upon the detection of an asserted EOQ bit on the last transferred command. Refer to Section 19.4.3.5, “CFIFO Scan Trigger Modes,” for details. 0 Not the last entry of the command queue. 1 Last entry of the command queue. **Note:** If both the pause and EOQ bits are asserted in the same command message the respective flags are set, but the CFIFO status changes as if only the EOQ bit were asserted.
1 PAUSE	Pause bit. Allows software to create sub-queues within a command queue. When the eQADC completes the transfer of a command with an asserted pause bit, the CFIFO enters the WAITING FOR TRIGGER state. Refer to Section 19.4.3.6.1, “CFIFO Operation Status,” for a description of the state transitions. The pause bit is only valid when CFIFO operation mode is configured to single or continuous-scan edge trigger mode. 0 Do not enter WAITING FOR TRIGGER state after transfer of the current command message. 1 Enter WAITING FOR TRIGGER state after transfer of the current command message. **Note:** If both the pause and EOQ bits are asserted in the same command message the respective flags are set, but the CFIFO status changes as if only the EOQ bit were asserted.
2–3	Reserved.
4 ABORT _ST	ABORT serial transmission. Indicates whether to abort an on-going serial transmission. All CFIFOs can abort null message transmissions when triggered but only CFIFO0 can abort command transmissions of lower priority CFIFOs. For more on serial transmission aborts, see Section 19.4.3.2, “CFIFO Prioritization and Command Transfer.” 0 Do not abort current serial transmission. 1 Abort current serial transmission.
5 EB	External buffer. Always set this bit for messages sent to an external ADC. 0 Command is sent to an internal command buffer. 1 Command is sent to an external command buffer.
6 BN	Refer to Section , “Conversion Command Message Format for On-Chip ADC Operation.”
7–31 OFF_CHIP_ COMMAND [0:24]	OFF-CHIP COMMAND Field. The OFF_CHIP_COMMAND field can be anything decodable by the external device. It is 25 bits long and it is transferred together with the BN bit to the external device when the CFIFO is triggered. Refer to Section , “Conversion Command Message Format for On-Chip ADC Operation,” for a description of the command message used when interfacing with the on-chip ADCs.

Result Message Format for External Device Operation

Data is returned from the ADCs in the form of result messages. A result message is composed of an RFIFO header and an ADC result. The FIFO control unit decodes the information contained in the RFIFO header and sends the contents of the ADC result to the appropriate RFIFO. Only data stored on the ADC_RESULT field is stored in the RFIFOs result queues. The ADC result of any received message with a null data message tag is ignored. The format of a result message returned from the external device is shown in Figure 19-32. It is 26 bits long, and is composed of a MESSAGE_TAG field, information about the status of the buffers (BUSY fields), and result data. The BUSY fields are needed to inform the eQADC about when it is appropriate to transfer commands to the external command buffers.

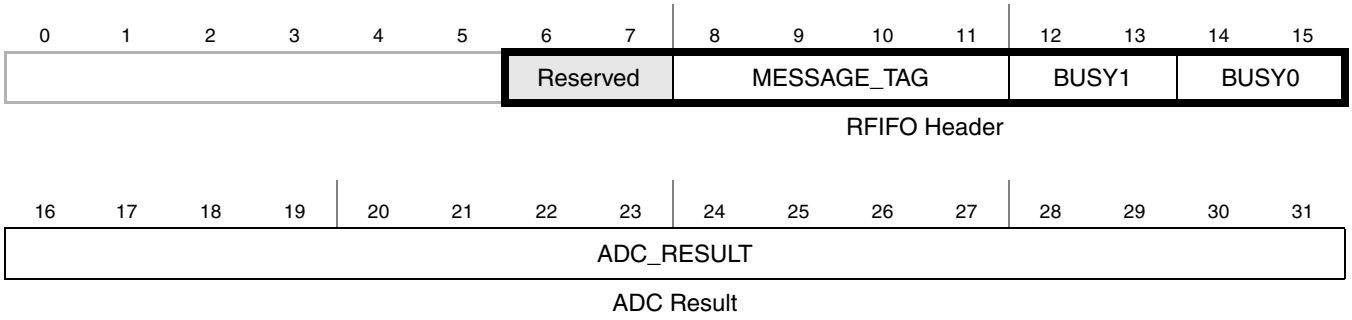


Figure 19-32. Result Message Format for External Device Operation

Table 19-41. Result Message Format for External Device Operation

Field	Description
6–7	Reserved.
8–11 MESSAGE_TAG[0:3]	MESSAGE_TAG Field. Refer to Section , “Conversion Command Message Format for On-Chip ADC Operation.”
12–15 BUSY*n* [0:1]	BUSY status. The BUSY fields indicate if the external device can receive more commands. Table 19-42 shows how these two bits are encoded. When an external device cannot accept any more new commands, it must set BUSY*n* to a value indicating “Do not send commands” in the returning message. The BUSY fields of values 0b10 and 0b10 can be freely encoded by the external device to allow visibility of the status of the external command buffers for debug. As an example, they could indicate the number of entries in an external command buffer.
16–31 ADC_ RESULT [0:15]	ADC RESULT Field. The result data received from the external device or on-chip ADC can be any value produced by the external device, such as the result of a conversion command, data requested via a read configuration command, or a time stamp value. The ADC_RESULT of any incoming message with a null message tag is ignored. When the MESSAGE_TAG is for an RFIFO, the eQADC extracts the 16-bit ADC_RESULT from the raw message and stores it into the appropriate RFIFO.

Table 19-42. Command BUFFER*n* BUSY Status[1]

BUSY*n*[0:1]	Meaning
0b00	Send available commands—command buffer is empty
0b01	Send available commands
0b10	Send available commands
0b11	Do not send commands

[1] After reset, the eQADC always assumes that the external command buffers are full and cannot receive commands.

Null Message Format for External Device Operation

Null messages are only transferred through the serial interface to allow results and unsolicited control data, like the status of the external command buffers, to return when there are no more commands pending to transfer. Null messages are only transmitted when serial transmissions from the eQADC SSI are enabled (see ESSIE field in Section 19.3.2.1, "eQADC Module Configuration Register (EQADC_MCR),"), and when one of the following conditions apply:

- There are no triggered CFIFOs with commands bound for external command buffers.
- There are triggered CFIFOs with commands bound for external command buffers but the external buffers are full. The eQADC detected returning BUSY*n* fields indicating "Do not send commands."

Figure 19-33 illustrates the null message send format. When the eQADC transfers a null message, it directly shifts out the 26-bit data content inside the Section 19.3.2.2, "eQADC Null Message Send Format Register (EQADC_NMSFR)." The register must be programmed with the null message send format of the external device.

Figure 19-34 illustrates the null message receive format. It has the same fields found in a result message with the exception that the ADC result is not used. Refer to section "Result Message Format for External Device Operation," for more information. The MESSAGE_TAG field must be set to the null message tag (0b1000). The eQADC does not store into an RFIFO any incoming message with a null message tag.

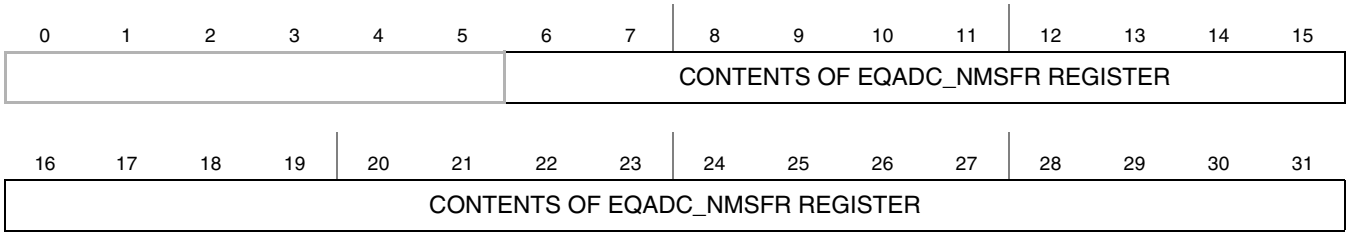


Figure 19-33. Null Message Send Format for External Device Operation

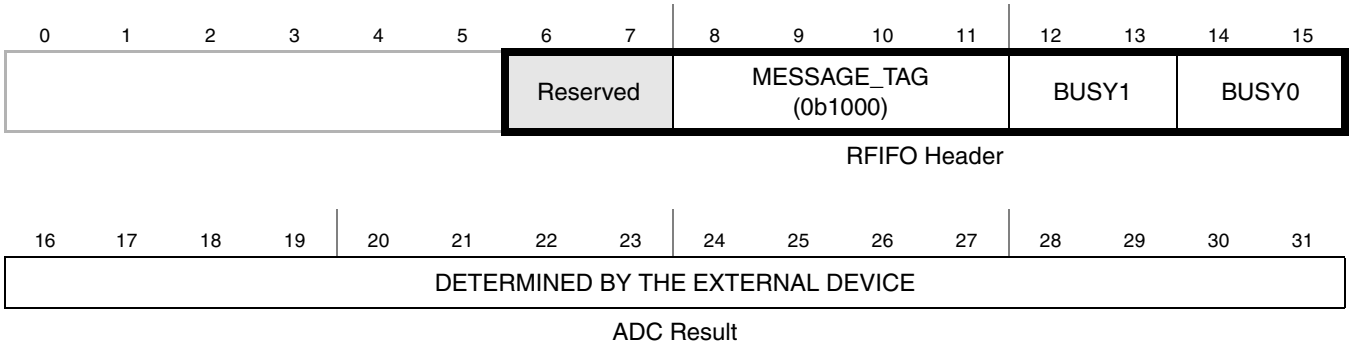


Figure 19-34. Null Message Receive Format for External Device Operation

Table 19-43. Null Message Receive Format for External Device Operation

Field	Description
6–7	Reserved.
8–11 MESSAGE_TAG[0:3]	MESSAGE_TAG field. Refer to Section , “Conversion Command Message Format for On-Chip ADC Operation.”
12–15 BUSY*n* [0:1]	BUSY status. Refer to Section , “Result Message Format for External Device Operation.”
16–31	Determined by the external device.

19.4.2 Command/Result Queues

The command and result queues are actually part of the eQADC system although they are not hardware implemented inside the eQADC. Instead command and result queues are user-defined queues located in system memory. Each command queue entry is a 32-bit command message.The last entry of a command queue has the EOQ bit asserted to indicate that it is the last entry of the queue. The result queue entry is a 16-bit data item.

Refer to Section 19.1.4, “Modes of Operation,” for a description of the message formats and their flow in eQADC.

Refer to Section 19.5.5, “Command Queue and Result Queue Usage,” for examples of how command queues and result queues can be used.

19.4.3 eQADC Command FIFOs

19.4.3.1 CFIFO Basic Functionality

There are six prioritized CFIFOs located in the eQADC. Each CFIFO is four entries deep, and each CFIFO entry is 32 bits long. A CFIFO serves as a temporary storage location for the command messages stored in the command queues in system memory. When a CFIFO is not full, the eQADC sets the corresponding CFFF bit in Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn).” If

CFFE is asserted as in Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn),” the eQADC generates requests for more commands from a command queue. An interrupt request, served by the host CPU, is generated when CFFS is negated, and a eDMA request, served by the eDMA, is generated when CFFS is asserted. The host CPU or the eDMA respond to these requests by writing to the Section 19.3.2.4, “eQADC CFIFO Push Registers 0–5 (EQADC_CFPRn),” to fill the CFIFO.

NOTE

Only whole words must be written to EQADC_CFPR. Writing halfwords or bytes to EQADC_CFPR pushes the entire 32-bit CF_PUSH field into the corresponding CFIFO, but undefined data fills the areas of CF_PUSH that were not specifically designated as target locations for writing.

Figure 19-35 describes the important components in the CFIFO. Each CFIFO is implemented as a circular set of registers to avoid the need to move all entries at each push/pop operation. The push next data pointer points to the next available CFIFO location for storing data written into the eQADC command FIFO push register. The transfer next data pointer points to the next entry to be removed from CFIFO*n* when it completes a transfer. The CFIFO transfer counter control logic counts the number of entries in the CFIFO and generates eDMA or interrupt requests to fill the CFIFO. TNXTPTR in Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn),” indicates the index of the entry that is currently being addressed by the transfer next data pointer, and CFCTR, in the same register, provides the number of entries stored in the CFIFO.

Using TNXTPTR and CFCTR, the absolute addresses for the entries indicated by the transfer next data pointer and by the push next data pointer can be calculated using the following formulas:

```
Transfer Next Data Pointer Address = CFIFOn_BASE_ADDRESS + TNXTPTRn x 4
Push Next Data Pointer Address = CFIFOn_BASE_ADDRESS +
[(TNXTPTRn+CFCTRn) mod CFIFO_DEPTH] x 4
```

where

- *a mod b* returns the remainder of the division of *a* by *b*.
- CFIFO*n*_BASE_ADDRESS is the smallest memory mapped address allocated to a CFIFO*n* entry.
- CFIFO_DEPTH is the number of entries contained in a CFIFO - four in this implementation.

When CFS*n* in Section 19.3.2.11, “eQADC CFIFO Status Register (EQADC_CFSR),” is in the TRIGGERED state, the eQADC generates the proper control signals for the transfer of the entry pointed by transfer next data pointer. CFUF*n* in Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn),” is set when a CFIFO*n* underflow event occurs. A CFIFO underflow occurs when the CFIFO is in the TRIGGERED state and it becomes empty. No commands are transferred from an underflowing CFIFO, and command transfers from lower priority CFIFOs are not blocked. CFIFO*n* is empty when the transfer next data pointer *n* equals the push next data pointer *n* and CFCTR*n* is 0. CFIFO*n* is full when the transfer next data pointer *n* equals the push next data pointer *n* and CFCTR*n* is not 0.

When the eQADC completes the transfer of an entry from CFIFO*n*: the transferred entry is popped from CFIFO*n*, the CFIFO counter CFCTR in the Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn),” is decremented by 1, and transfer next data pointer *n* is incremented by 1 (or wrapped around) to point to the next entry in the CFIFO. The transfer of entries bound for the on-chip

ADCs is considered completed when they are stored in the appropriate ADC command buffer. The transfer of entries bound for the external device is considered completed when the serial transmission of the entry is completed.

When the EQADC_CFPR*n* is written and CFIFO*n* is not full, the CFIFO counter CFCTR*n* is incremented by 1, and the push next data pointer *n* then is incremented by 1 (or wrapped around) to point to the next entry in the CFIFO.

When the EQADC_CFPR*n* is written but CFIFO*n* is full, the eQADC does not increment the counter value and does not overwrite any entry in CFIFO*n*.

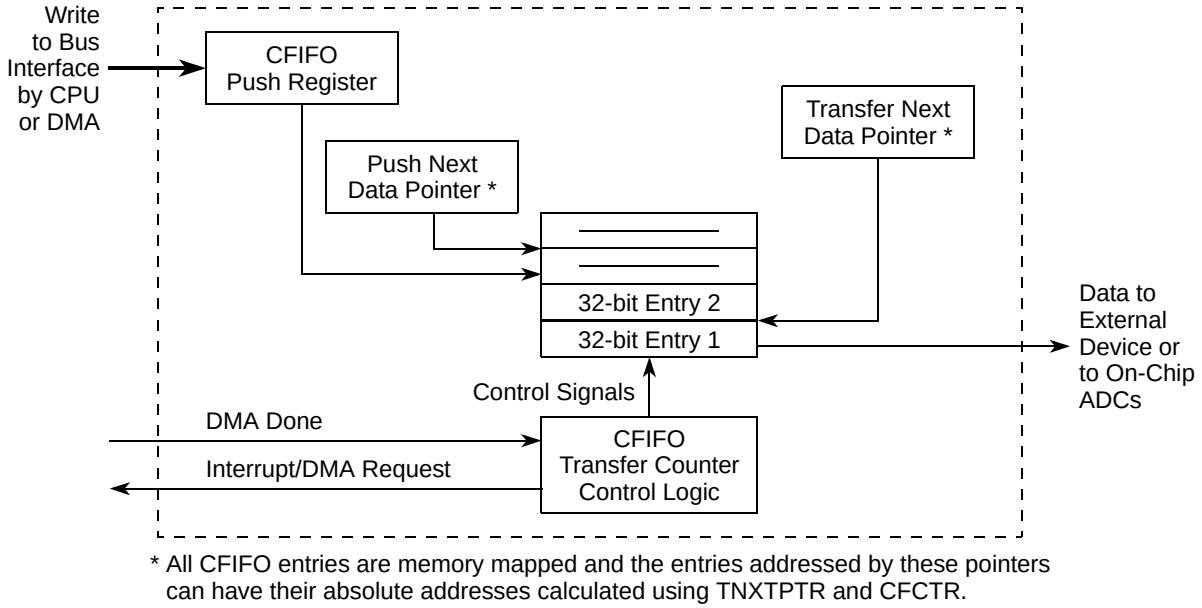


Figure 19-35. CFIFO Diagram

The detailed behavior of the push next data pointer and transfer next data pointer is described in the example shown in Figure 19-36 where a CFIFO with 16 entries is shown for clarity of explanation, the actual hardware implementation has only four entries. In this example, CFIFO*n* with 16 entries is shown in sequence after pushing and transferring entries.

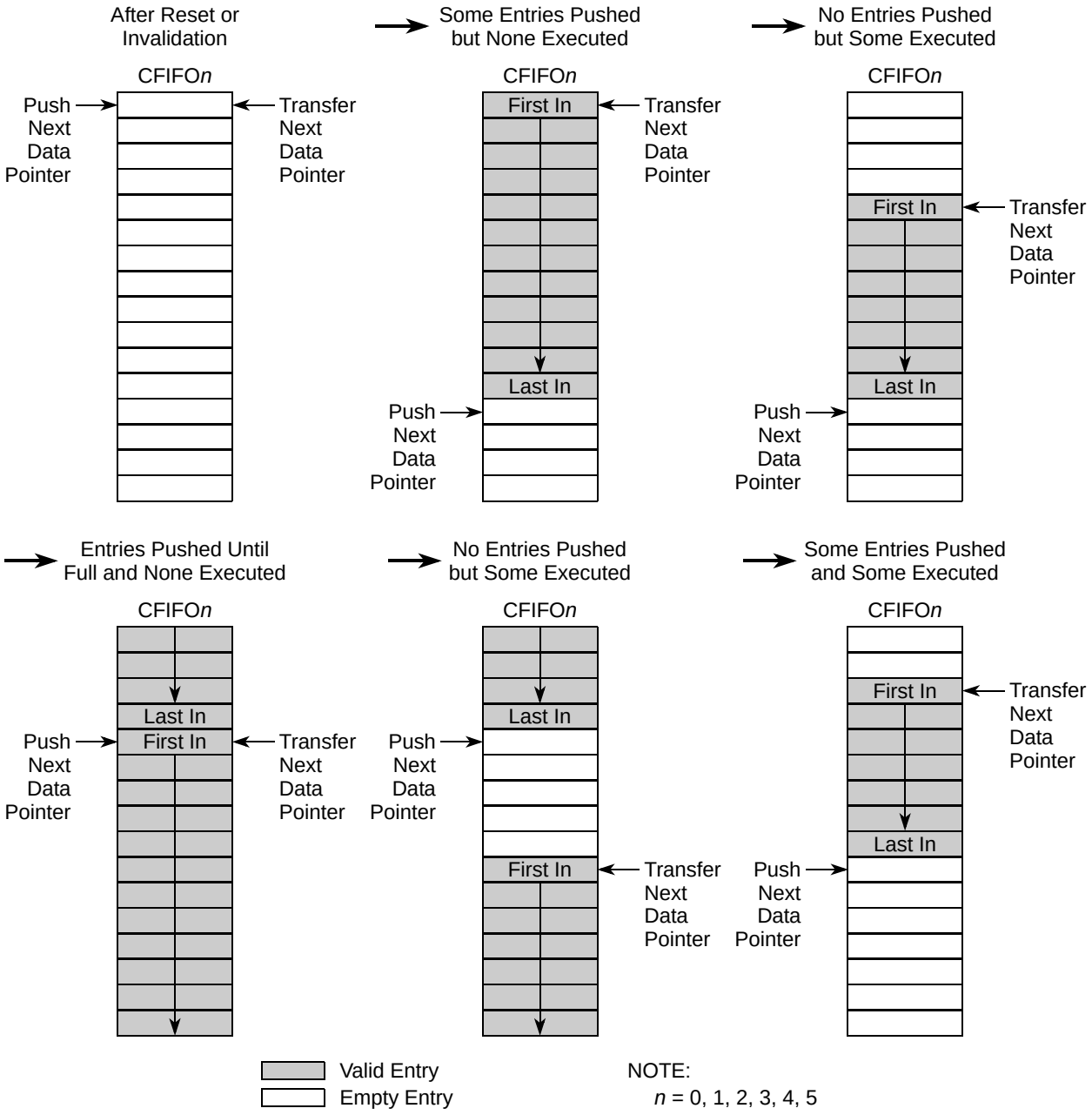


Figure 19-36. CFIFO Entry Pointer Example

19.4.3.2 CFIFO Prioritization and Command Transfer

The CFIFO priority is fixed according to the CFIFO number. A CFIFO with a smaller number has a higher priority. When commands from different CFIFOs are sent to the same destination (such as the same on-chip ADC), the higher priority CFIFO is always served first. A triggered, not-underflowing CFIFO starts to transfer commands when the following occur:

- Its commands are bound for an internal command buffer that is not full, and it is the highest priority triggered CFIFO sending commands to that buffer.

- Its commands are bound for an external command buffer that is not full, and it is the highest priority triggered CFIFO sending commands to an external buffer that is not full.

A triggered CFIFO with commands bound for a certain command buffer consecutively transfers its commands to the buffer until one of the following occurs:

- An asserted end of queue bit is reached.
- An asserted pause bit is encountered and the CFIFO is configured for edge trigger mode.
- CFIFO is configured for level trigger mode and a closed gate is detected.
- In case its commands are bound for an internal command buffer, a higher priority CFIFO that uses the same internal buffer is triggered.
- In case its commands are bound for an external command buffer, a higher priority CFIFO that uses an external buffer is triggered.

The prioritization logic of the eQADC, depicted in Figure 19-37, is composed of three independent submodules: one that prioritizes CFIFOs with commands bound for ADC0, another that prioritizes CFIFOs with commands for ADC1, and a last one that prioritizes CFIFOs with commands for external command buffer 2 and buffer 3. As these three submodules are independent, simultaneous commands to ADC0, to ADC1, and to eQADC SSI transmit buffer are allowed. The hardware identifies the destination of a command by decoding the EB and BN bits in the command message (see Section 19.4.1.2, “Message Format in eQADC,” for details).

NOTE

Triggered but empty CFIFOs, underflowing CFIFOs, are not considered for prioritization. No data from these CFIFOs is sent to the on-chip ADCs or the external command buffers, and lower priority CFIFOs are not stopped from transferring commands.

Whenever ADC0 is able to receive new commands, the prioritization submodule selects the highest-priority triggered CFIFO with a command bound for ADC0, and sends it to the ADC. In case ADC0 is able to receive new entries but there are no triggered CFIFOs with commands bound for it, nothing is sent. The submodule prioritizing ADC1 usage behaves in the same way.

When the eQADC SSI is enabled and ready to start serial transmissions, the submodule prioritizing eQADC SSI usage writes command or null messages into the eQADC SSI transmit buffer. Data written to the eQADC SSI transmit buffer is subsequently transmitted to the external device through the eQADC SSI link. The submodule writes commands to the eQADC SSI transmit buffer when there are triggered CFIFOs with commands bound for not-full external command buffers. The command written to the transmit buffer belongs to the highest priority CFIFO sending commands to an external buffer that is not full. This implies that a lower priority CFIFO can have its commands sent if a higher priority CFIFO cannot send its commands due to a full command buffer. The submodule writes null messages to the eQADC SSI transmit buffer when there are no triggered CFIFOs with commands bound for external command buffers, or when there are triggered CFIFOs with commands bound for external buffers but the external buffers are full. The eQADC monitors the status of the external buffers by decoding the BUSY fields of the incoming result messages from the external device (see Section , “Result Message Format for External Device Operation,” for details).

NOTE

When a higher priority CFIFO cannot send commands due to a full external command buffer, a lower priority CFIFO is served. When the higher priority CFIFO is ready to send commands, an interrupt to the command transfers from the lower priority CFIFO can result in CFIFO incoherence. Whether the lower priority CFIFO becomes non-coherent depends on the following:

- Rate at which commands on the external ADCs are executed
- Rate at which commands are transmitted to the external command buffers
- Depth of the buffers

After a serial transmission starts, the submodule monitors triggered CFIFOs and manages the abort of the serial transmissions. If a null message is transmitted, the serial transmission is aborted when all of the following conditions are met:

- A not-underflowing CFIFO in the TRIGGERED state has commands bound for an external command buffer that is not full, and it is the highest priority CFIFO sending commands to an external buffer that is not full.
- The ABORT_ST bit of the command to be transmitted is asserted.
- The 26th bit of the currently transmitting null message is not shifted out.

The command from the CFIFO is then written into eQADC SSI transmit buffer, allowing for a new serial transmission to initiate.

In case a command is being transmitted, the serial transmission is aborted when all following conditions are met:

- CFIFO0 is in the TRIGGERED state, is not underflowing, and its current command is bound for an external command buffer that is not full.
- The ABORT_ST bit of the command to be transmitted is asserted.
- The 26th bit of the currently transmitting command has not being shifted out.

The command from CFIFO0 is then written into eQADC SSI transmit buffer, allowing for a new serial transmission to initiate.

NOTE

The aborted command is not popped from the pre-empted CFIFO, but is retransmitted as soon as it’s the highest priority CFIFO sending commands to an unfilled external command buffer.

After a serial transmission is completed, the eQADC prioritizes the CFIFOs and schedules a command or a null message to be sent in the next serial transmission. After the data for the next transmission has been defined and scheduled, the eQADC can, under certain conditions, stretch the $\overline{\text{SDS}}$ negation time to allow the schedule of new data for that transmission. This occurs when the eQADC acknowledges that the status of a higher-priority CFIFO has changed to the TRIGGERED state and attempts to schedule that CFIFO

command before $\overline{SDS}$ is asserted. Only commands of CFIFOs that have the ABORT_ST bit asserted can be scheduled in this manner. Under such conditions:

1. A CFIFO0 command is scheduled for the next transmission independently of the type of data that was previously scheduled. The time during which $\overline{SDS}$ is negated is stretched to allow the eQADC to load the CFIFO0 command and start its transmission.
2. CFIFO1-5 commands are only scheduled for the next transmission if the previously scheduled data was a null message. The time during which $\overline{SDS}$ is negated is stretched to allow the eQADC to load that command and start its transmission. However, if the previously scheduled data was a command, no rescheduling occurs and the next transmission starts without delays.

If a CFIFO becomes triggered while $\overline{SDS}$ is negated, but the eQADC only attempts to reschedule that CFIFO command after $\overline{SDS}$ is asserted, then the current transmission is aborted depending on if the conditions for that are met or not.

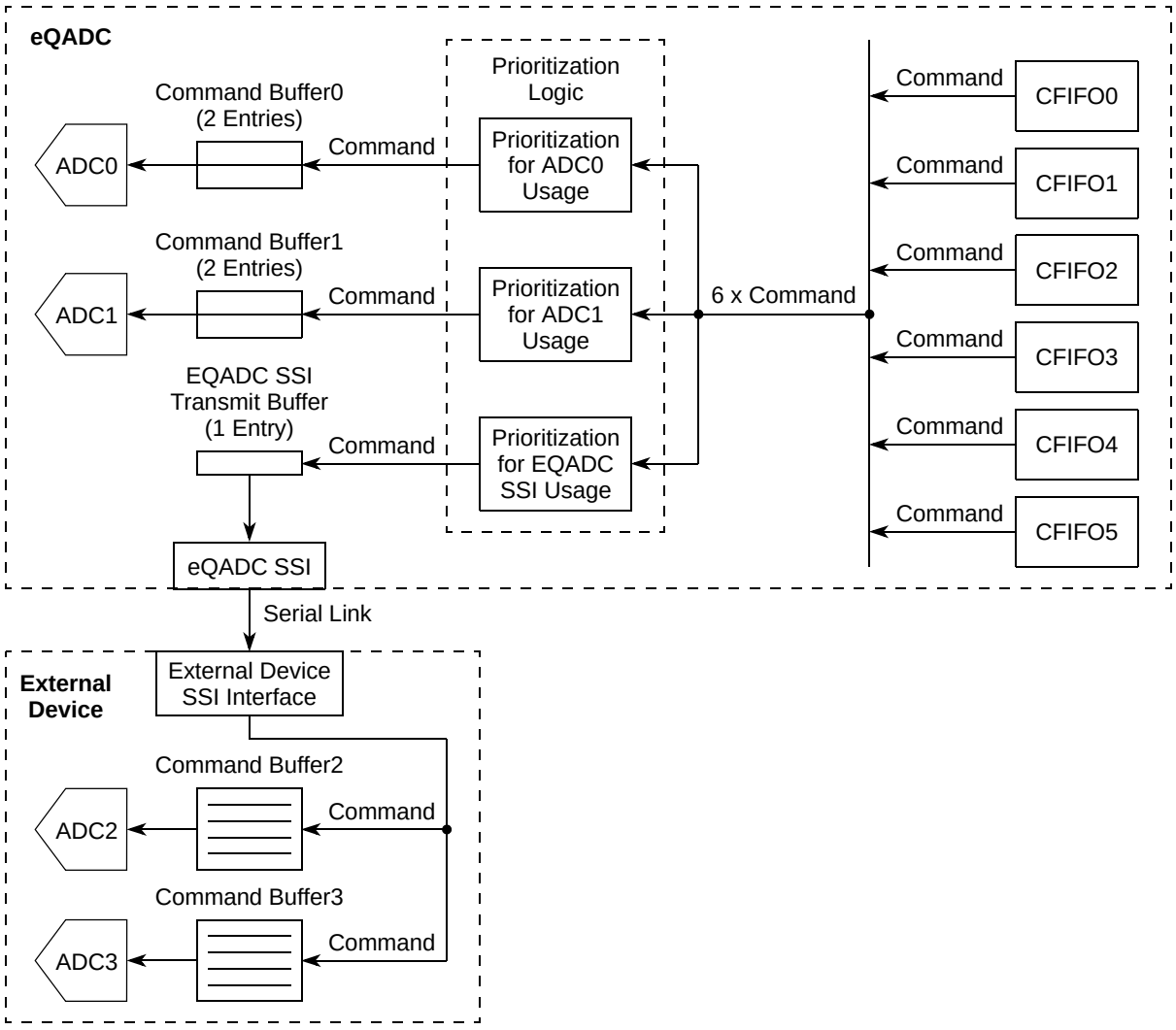


Figure 19-37. CFIFO Prioritization Logic

19.4.3.3 External Trigger from eTPU or eMIOS Channels

The six eQADC external trigger inputs can be connected to either an external pin (either ETRIG0, ETRIG1, GPIO206, or GPIO207), an eTPU channel, or an eMIOS channel. The input source for each eQADC external trigger is individually specified in the eQADC trigger input select register (SIU_ETISR) in the SIU block.

The eQADC trigger numbers specified by SIU_ETISR[TSEL(0–5)] correspond to CFIFO numbers 0–5. To calculate the CFIFO number that each trigger is connected to, divide the eDMA channel number by 2.

A complete description of the eTPU and eMIOS trigger function and configuration is found in Section 6.4.5.1, “eQADC External Trigger Input Multiplexing.”

19.4.3.4 External Trigger Event Detection

The digital filter length field in Section 19.3.2.3, “eQADC External Trigger Digital Filter Register (EQADC_ETDFR),” specifies the minimum number of system clocks that the external trigger signals 0 and 1 must be held at a logic level to be recognized as valid. All ETRIG signals are filtered. A counter for each queue trigger is implemented to detect a transition between logic levels. The counter counts at the system clock rate. The corresponding counter is cleared and restarted each time the signal transitions between logic levels. When the corresponding counter matches the value specified by the digital filter length field in Section 19.3.2.3, “eQADC External Trigger Digital Filter Register (EQADC_ETDFR),” the eQADC considers the ETRIG logic level to be valid and passes that new logic level to the rest of the eQADC.

The filter is only for filtering the ETRIG signal. Logic after the filter checks for transitions between filtered values, such as for detecting the transition from a filtered logic level zero to a filtered logic level one in rising edge external trigger mode. The eQADC can detect rising edge, falling edge, or level gated external triggers. The digital filter is always active independently of the status of the MODE*n* field in Section 19.3.2.6, “eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn),” but the edge, level detection logic is only active when MODE*n* is set to a value different from disabled, and in case MODE*n* is set to single scan mode, when the SSS bit is asserted. Note that the time necessary for a external trigger event to result into a CFIFO status change is not solely determined by the DFL field in the Section 19.3.2.3, “eQADC External Trigger Digital Filter Register (EQADC_ETDFR).” After being synchronized to the system clock and filtered, a trigger event is checked against the CFIFO trigger mode. Only then, after a valid trigger event is detected, the eQADC accordingly changes the CFIFO status. Refer to Figure 19-38 for an example.

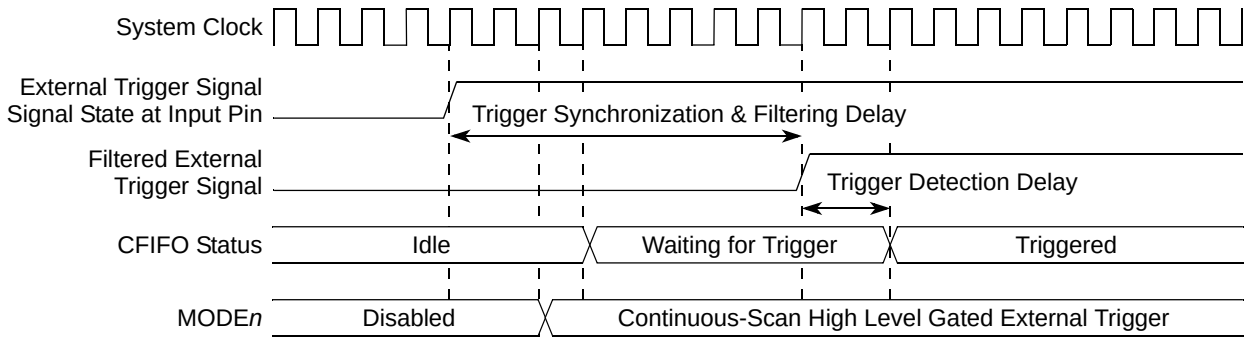


Figure 19-38. ETRIG Event Propagation Example

19.4.3.5 CFIFO Scan Trigger Modes

The eQADC supports two different scan modes, single-scan and continuous-scan. Refer to Table 19-44 for a summary of these two scan modes. When a CFIFO is triggered, the eQADC scan mode determines whether the eQADC stops command transfers from a CFIFO, and waits for software intervention to rearm the CFIFO to detect new trigger events, upon detection of an asserted EOQ bit in the last transfer. Refer to Section 19.4.1.2, "Message Format in eQADC," for details about command formats.

CFIFOs can be configured in single-scan or continuous-scan mode. When a CFIFO is configured in single-scan mode, the eQADC scans the command queue one time. The eQADC stops future command transfers from the triggered CFIFO after detecting the EOQ bit set in the last transfer. After a EOQ bit is detected, software involvement is required to rearm the CFIFO so that it can detect new trigger events.

When a CFIFO is configured for continuous-scan mode, no software involvement is necessary to rearm the CFIFO to detect new trigger events after an asserted EOQ is detected. In continuous-scan mode the whole command queue is scanned multiple times.

The eQADC also supports different triggering mechanisms for each scan mode. The eQADC does not transfer commands from a CFIFO until the CFIFO is triggered. The combination of scan modes and triggering mechanisms allows the support of different requirements for scanning input channels. The scan mode and trigger mechanism are configured by programming the MODE*n* field in Section 19.3.2.6, "eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)."

Enabled CFIFOs can be triggered by software or external trigger events. The elapsed time from detecting a trigger to transferring a command is a function of clock frequency, trigger synchronization, trigger filtering, programmable trigger events, command transfer, CFIFO prioritization, ADC availability, etc. Fast and predictable transfers can be achieved by ensuring that the CFIFO is not underflowing and that the target ADC can accept commands when the CFIFO is triggered.

19.4.3.5.1 Disabled Mode

The MODE*n* field in Section 19.3.2.6, "eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)," for all of the CFIFOs can be changed from any other mode to disabled at any time. No trigger event can initiate command transfers from a CFIFO which has its MODE field programmed to disabled.

NOTE

If MODE*n* is not disabled, it must not be changed to any other mode besides disabled. If MODE*n* is disabled and the CFIFO status is IDLE, MODE*n* can be changed to any other mode.

If MODE*n* is changed to disabled:

- The CFIFO execution status changes to IDLE. The timing of this change depends on whether a command is being transferred or not:
  - When no command transfer is in progress, the eQADC switches the CFIFO to IDLE status immediately.
  - When a command transfer to an on-chip ADC is in progress, the eQADC completes the transfer, updates TC_CF, and switches CFIFO status to IDLE. Command transfers to the internal ADCs are considered completed when a command is written to the relevant buffer.
  - When a command transfer to an external command buffer is in progress, the eQADC aborts the transfer and switches CFIFO status to IDLE. If the eQADC cannot abort the transfer, that is when the 26th bit of the serial message has being already shifted out, the eQADC completes the transfer, updates TC_CF and then switches CFIFO status to IDLE.
- The CFIFOs are not invalidated automatically. The CFIFO still can be invalidated by writing a 1 to the CFINV*n* bit (see Section 19.3.2.6, “eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)”). Certify that CFS has changed to IDLE before setting CFINV*n*.
- The TC_CF*n* value also is not reset automatically, but it can be reset by writing 0 to it.
- The EQADC_FISRn[SSS] bit (see Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)”) is negated. The SSS bit can be set even if a 1 is written to the EQADC_CFCR[SSE] bit (see Section 19.3.2.6, “eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)”) in the same write that the MODE*n* field is changed to a value other than disabled.
- The trigger detection hardware is reset. If MODE*n* is changed from disabled to an edge trigger mode, a new edge, matching that edge trigger mode, is needed to trigger the command transfers from the CFIFO.

NOTE

CFIFO fill requests, generated when the CFFF asserts, are not automatically halted when MODE*n* is changed to disabled. CFIFO fill requests are still generated until EQADC_IDCRn[CFFE] bit is cleared. Refer to Section Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn).”

19.4.3.5.2 Single-Scan Mode

In single-scan mode, a single pass through a sequence of command messages in the user-defined command queue is performed.

In single-scan software trigger mode, the CFIFO is triggered by an asserted single-scan status bit, EQADC_FISRn[SSS] (see Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5

(EQADC_FISRn)"). The SSS bit is set by writing 1 to the single-scan enable bit, EQADC_CFCRn[SSE] (see Section 19.3.2.6, "eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)").

In single-scan edge or level trigger mode, the respective triggers are only detected when the SSS bit is asserted. When the SSS bit is negated, all trigger events for that CFIFO are ignored. Writing a 1 to the SSE bit can be done during the same write cycle that the CFIFO operation mode is configured.

Only the eQADC can clear the SSS bit. After SSS is asserted, it remains asserted until the eQADC completes the command queue scan, or the CFIFO operation mode, EQADC_CFCRn[MODE*n*] (see Section 19.3.2.6) is changed to disabled. The SSS*n* bit is negated while MODE*n* is disabled.

Single-Scan Software Trigger

When single-scan software trigger mode is selected, the CFIFO is triggered by an asserted SSS bit. The SSS bit is asserted by writing 1 to the SSE bit. Writing to SSE while SSS is already asserted does not have any effect on the state of the SSS bit, nor does it cause a trigger overrun event.

The CFIFO commands start to be transferred when the CFIFO becomes the highest priority CFIFO using an available on-chip ADC or an external command buffer that is not full. When an asserted EOQ bit is encountered, the eQADC clears the SSS bit. Setting the SSS bit is required for the eQADC to start the next scan of the queue.

The pause bit has no effect in single-scan software trigger mode.

Single-Scan Edge Trigger

When SSS is asserted and an edge triggered mode is selected for a CFIFO, an appropriate edge on the associated trigger signal causes the CFIFO to become triggered. For example, if rising-edge trigger mode is selected, the CFIFO becomes triggered when a rising edge is sensed on the trigger signal. The CFIFO commands start to be transferred when the CFIFO becomes the highest priority CFIFO using an available on-chip ADC, or an external command buffer that is not full.

When an asserted EOQ bit is encountered, the eQADC clears SSS and stops command transfers from the CFIFO. An asserted SSS bit and a subsequent edge trigger event are required to start the next scan for the CFIFO. When an asserted pause bit is encountered, the eQADC stops command transfers from the CFIFO, but SSS remains set. Another edge trigger event is required for command transfers to continue. A trigger overrun happens when the CFIFO is in a TRIGGERED state and an edge trigger event is detected.

Single-Scan Level Trigger

When SSS is asserted and a level gated trigger mode is selected, the input level on the associated trigger signal puts the CFIFO in a TRIGGERED state. When the CFIFO is set to high-level gated trigger mode, a high level signal opens the gate, and a low level closes the gate. When the CFIFO is set to low-level gated trigger mode, a low level signal opens the gate, and a high level closes the gate. If the corresponding level is already present, setting the SSS bit triggers the CFIFO. The CFIFO commands start to be transferred when the CFIFO becomes the highest priority CFIFO using an available on-chip ADC or an external command buffer that is not full.

The eQADC clears the SSS bit and stops transferring commands from a triggered CFIFO when an asserted EOQ bit is encountered or when CFIFO status changes from triggered due to the detection of a closed gate.

If a closed gate is detected while no command transfers are taking place and the CFIFO status is triggered, the CFIFO status is immediately changed to IDLE, the SSS bit is negated, and the PF flag is asserted. If a closed gate is detected during the serial transmission of a command to the external device, it has no affect on the CFIFO status until the transmission completes. After the transmission is completed, the TC_CF counter is updated, the SSS bit is negated, the PF flag is asserted, and the CFIFO status is changed to IDLE. An asserted SSS bit and a level trigger are required to restart the CFIFO. Command transfers restart from the point they have stopped.

If the gate closes and opens during the same serial transmission of a command to the external device, it has no effect on the CFIFO status or on the PF flag, but the TORF flag asserts as shown in Figure 19-40. Therefore, closing the gate for a period less than a serial transmission time interval does not guarantee that the closure affects command transfers from a CFIFO.

The pause bit has no effect in single-scan level trigger mode.

19.4.3.5.3 Continuous-Scan Mode

In continuous-scan mode, multiple passes looping through a sequence of command messages in a command queue are executed. When a CFIFO is programmed for a continuous-scan mode, the EQADC_CFCRn[SSE] (see Section 19.3.2.6, “eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)”) does not have any effect.

Continuous-Scan Software Trigger

When a CFIFO is programmed to continuous-scan software trigger mode, the CFIFO is triggered immediately. The CFIFO commands start to be transferred when the CFIFO becomes the highest priority CFIFO using an available on-chip ADC or an external command buffer that is not full. When a CFIFO is programmed to run in continuous-scan software trigger mode, the eQADC does not halt transfers from the CFIFO until the CFIFO operation mode is modified to disabled or a higher priority CFIFO preempts it. Although command transfers do not stop upon detection of an asserted EOQ bit, the EOQF is set and, if enabled, an EOQ interrupt request is generated.

The pause bit has no effect in continuous-scan software trigger mode.

Continuous-Scan Edge Trigger

When rising, falling, or either edge trigger mode is selected for a CFIFO, a corresponding edge on the associated ETRIG signal places the CFIFO in a TRIGGERED state. The CFIFO commands start to be transferred when the CFIFO becomes the highest priority CFIFO using an available on-chip ADC or an external command buffer that is not full.

When an EOQ or a pause is encountered, the eQADC halts command transfers from the CFIFO and, if enabled, the appropriate interrupt requests are generated. Another edge trigger event is required to resume command transfers but no software involvement is required to rearm the CFIFO to detect such event.

A trigger overrun happens when the CFIFO is already in a TRIGGERED state and a new edge trigger event is detected.

Continuous-Scan Level Trigger

When high or low level gated trigger mode is selected, the input level on the associated trigger signal places the CFIFO in a TRIGGERED state. When high-level gated trigger is selected, a high-level signal opens the gate, and a low level closes the gate. The CFIFO commands start to be transferred when the CFIFO becomes the highest priority CFIFO using an available on-chip ADC or an external buffer that is not full. Although command transfers do not stop upon detection of an asserted EOQ bit at the end of a command transfer, the EOQF is asserted and, if enabled, an EOQ interrupt request is generated.

The eQADC stops transferring commands from a triggered CFIFO when CFIFO status changes from triggered due to the detection of a closed gate. If a closed gate is detected while no command transfers are taking place and the CFIFO status is TRIGGERED, the CFIFO status is immediately changed to waiting for trigger and the PF flag is asserted. If a closed gate is detected during the serial transmission of a command to the external device, it has no effect on the CFIFO status until the transmission completes. After the transmission is completed, the TC_CF counter is updated, the PF flag is asserted, and the CFIFO status is changed to waiting for trigger. Command transfers restart as the gate opens.

If the gate closes and opens during the same serial transmission of a command to the external device, it has no affect on the CFIFO status or on the PF flag, but the TORF flag asserts as shown in Figure 19-40. Therefore, closing the gate for a period less than a serial transmission time interval does not guarantee that command transfers from a CFIFO are closed.

The pause bit has no effect in continuous-scan level trigger mode.

19.4.3.5.4 CFIFO Scan Trigger Mode Start/Stop Summary

Table 19-44 summarizes the start and stop conditions of command transfers from CFIFOs for all of the single-scan and continuous-scan trigger modes.

Table 19-44. CFIFO Scan Trigger Mode—Command Transfer Start/Stop Summary

Trigger Mode	Requires Asserted SSS to Recognize Trigger Events?	Command Transfer Start/Restart Condition	Stop on asserted EOQ bit[1]?	Stop on asserted Pause bit[2]?	Other Command Transfer Stop Condition[3] [4]
Single Scan Software	Not Applicable	Asserted SSS bit.	Yes	No	None.
Single Scan Edge	Yes	A corresponding edge occurs when the SSS bit is asserted.	Yes	Yes	None.
Single Scan Level	Yes	Gate is opened when the SSS bit is asserted.	Yes	No	The eQADC also stops transfers from the CFIFO when CFIFO status changes from triggered due to the detection of a closed gate.[5]
Continuous Scan Software	No	CFIFO starts automatically after being configured into this mode.	No	No	None.

Table 19-44. CFIFO Scan Trigger Mode—Command Transfer Start/Stop Summary

Trigger Mode	Requires Asserted SSS to Recognize Trigger Events?	Command Transfer Start/Restart Condition	Stop on asserted EOQ bit[1]?	Stop on asserted Pause bit[2]?	Other Command Transfer Stop Condition[3] [4]
Continuous Scan Edge	No	A corresponding edge occurs.	Yes	Yes	None.
Continuous Scan Level	No	Gate is opened.	No	No	The eQADC also stops transfers from the CFIFO when CFIFO status changes from triggered due to the detection of a closed gate.[5]

1 Refer to Section 19.4.3.6.2, "Command Queue Completion Status," for more information on EOQ.

2 Refer to Section 19.4.3.6.3, "Pause Status," for more information on pause.

3 The eQADC always stops command transfers from a CFIFO when the CFIFO operation mode is disabled.

4 The eQADC always stops command transfers from a CFIFO when a higher priority CFIFO is triggered. Refer to Section 19.4.3.2, "CFIFO Prioritization and Command Transfer," for information on CFIFO priority.

5 If a closed gate is detected while no command transfers are taking place, it has an immediate effect on the CFIFO status. If a closed gate is detected during the serial transmission of a command to the external device, it has no effect on the CFIFO status until the transmission completes.

19.4.3.6 CFIFO and Trigger Status

19.4.3.6.1 CFIFO Operation Status

Each CFIFO has its own CFIFO status field. CFIFO status (CFS) can be read from EQADC_CFSSR (refer to Section 19.3.2.11, "eQADC CFIFO Status Register (EQADC_CFSR)." Figure 19-39 and Table 19-45 indicate the CFIFO status switching condition. Refer to Table 19-18 for the meaning of each CFIFO operation status. The last CFIFO to transfer a command to an on-chip ADC can be read from the LCFT*n* (*n*=0,1) fields (see Section 19.3.2.10, "eQADC CFIFO Status Snapshot Registers 0–2 (EQADC_CFSSRn)." The last CFIFO to transfer a command to a specific external command buffer can be identified by reading the EQADC_CFSSR*n*[LCFTSSI] and EQADC_CFSSR*n*[ENI] fields (see Section 19.3.2.10, "eQADC CFIFO Status Snapshot Registers 0–2 (EQADC_CFSSRn)."

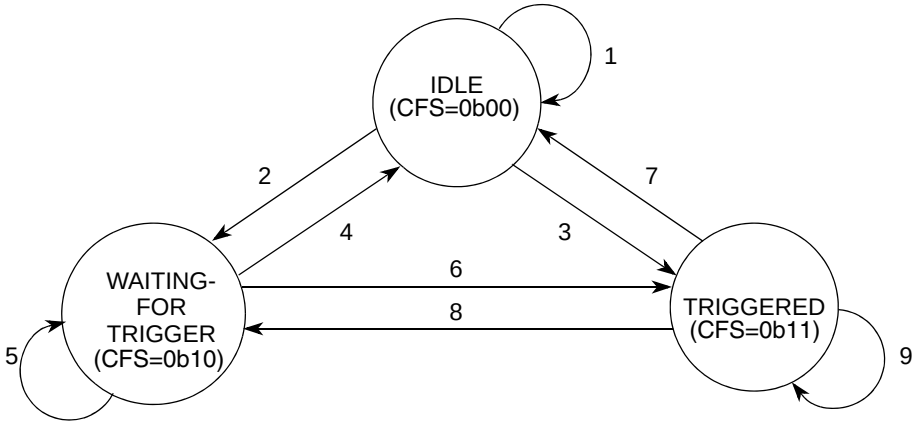


Figure 19-39. State Machine of CFIFO Status

Table 19-45. Command FIFO Status Switching Condition

No.	From Current CFIFO Status (CFS)	To New CFIFO Status (CFS)	Status Switching Condition
1	IDLE (00)	IDLE (0b00)	• CFIFO mode is programmed to disabled, OR • CFIFO mode is programmed to single-scan edge or level trigger mode and SSS is negated.
2		WAITING FOR TRIGGER (0b10)	• CFIFO mode is programmed to continuous-scan edge or level trigger mode, OR • CFIFO mode is programmed to single-scan edge or level trigger mode and SSS is asserted, OR • CFIFO mode is programmed to single-scan software trigger mode.
3		TRIGGERED (0b11)	• CFIFO mode is programmed to continuous-scan software trigger mode
4	WAITING FOR TRIGGER (10)	IDLE (0b00)	• CFIFO mode is modified to disabled mode.
5		WAITING FOR TRIGGER (0b10)	• No trigger occurred.
6		TRIGGERED (0b11)	• Appropriate edge or level trigger occurred, OR • CFIFO mode is programmed to single-scan software trigger mode and SSS bit is asserted.

Table 19-45. Command FIFO Status Switching Condition (continued)

No.	From Current CFIFO Status (CFS)	To New CFIFO Status (CFS)	Status Switching Condition
7	TRIGGERED (11)	IDLE (0b00)	• CFIFO in single-scan mode, eQADC detects the EOQ bit asserted at end of command transfer, and CFIFO mode is not modified to disabled, OR • CFIFO, in single-scan level trigger mode, and the gate closes while no commands are being transferred from the CFIFO, and CFIFO mode is not modified to disabled, OR • CFIFO, in single-scan level trigger mode, and eQADC detects a closed gated at end of command transfer, and CFIFO mode is not modified to disabled, OR • CFIFO mode is modified to disabled mode and CFIFO was not transferring commands. • CFIFO mode is modified to disabled mode while CFIFO was transferring commands, and CFIFO completes or aborts the transfer.
8		WAITING FOR TRIGGER (0b10)	• CFIFO in single or continuous-scan edge trigger mode, eQADC detects the pause bit asserted at the end of command transfer, the EOQ bit in the same command is negated, and CFIFO mode is not modified to disabled, OR • CFIFO in continuous-scan edge trigger mode, eQADC detects the EOQ bit asserted at the end of command transfer, and CFIFO mode is not modified to disabled, OR • CFIFO, in continuous-scan level trigger mode, and the gate closes while no commands are being transferred from the CFIFO, and CFIFO mode is not modified to disabled, OR • CFIFO, in continuous-scan level trigger mode, and eQADC detects a closed gated at end of command transfer, and CFIFO mode is not modified to disabled.
9		TRIGGERED (0b11)	• No event to switch to IDLE or WAITING FOR TRIGGER status has happened.

19.4.3.6.2 Command Queue Completion Status

The end of queue flag, EQADC_FISRn[EOQF] (see Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)”) is asserted when the eQADC completes the transfer of a CFIFO entry with an asserted EOQ bit. Software sets the EOQ bit in the last command message of a user-defined command queue to indicate that this entry is the end of the queue. Refer to Section 19.4.1.2, “Message Format in eQADC,” for information on command message formats. The transfer of entries bound for the on-chip ADCs is considered completed when they are stored in the appropriate command buffer. The transfer of entries bound for the external device is considered completed when the serial transmission of the entry is completed.

The command with a EOQ bit asserted is valid and is transferred. When EQADC_CFCRn[EOQIE] (refer to Section 19.3.2.6, “eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)”) and EQADC_FISRn[EOQF] are asserted, the eQADC generates an end of queue interrupt request.

In single-scan modes, command transfers from the corresponding CFIFO cease when the eQADC completes the transfer of a entry with an asserted EOQ. Software involvement is required to rearm the CFIFO so that it can detect new trigger events.

NOTE

An asserted EOQF*n* only implies that the eQADC has finished transferring a command with an asserted EOQ bit from CFIFO*n*. It does not imply that result data for the current command and for all previously transferred commands has been returned to the appropriate RFIFO.

19.4.3.6.3 Pause Status

In edge trigger mode, when the eQADC completes the transfer of a CFIFO entry with an asserted pause bit, the eQADC stops future command transfers from the CFIFO and sets EQADC_FISRn[PF]. The eQADC ignores the pause bit in command messages in any software level trigger mode. The eQADC sets the PF flag only in single or continuous-scan edge trigger mode when the pause bit set. When the PF flag is set for a CFIFO in single-scan edge trigger mode, the EQADC_FISRn[SSS] bit is not cleared.

Refer to the following sections for more information:

Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)”

Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)”

Section 19.4.1.2, “Message Format in eQADC,” for information on command message formats.

In level trigger mode, the PF flag designates that a CFIFO*n* is in the TRIGGERED status. The PF*n* bit is set when a closed gate is detected, triggering the CFIFO status change. The pause flag interrupt routine can be used to verify if a complete scan of the command queue was performed. If a closed gate is detected while no command transfers are taking place, it has an immediate effect on the CFIFO status. If a closed gate is detected during the serial transmission of a command to the external device, it has no effect on the CFIFO status until the transmission completes.

When EQADC_CFCR[PIE] and EQADC_FISRn[PF] are asserted, the eQADC generates a pause interrupt request. Refer to Section 19.3.2.6, “eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)” for more information.

NOTE

In edge-trigger mode, an asserted PF*n* only implies that the eQADC finished transferring a command with an asserted pause bit from CFIFO*n*. It does not imply that result data for the current command and for all previously transferred commands has been returned to the RFIFO.

NOTE

In software or level trigger mode, when the eQADC completes the transfer of an entry from CFIFO*n* with an asserted pause bit, PF*n* is not set and the command transfers continues without pausing.

19.4.3.6.4 Trigger Overrun Status

When a CFIFO is configured for edge or level trigger mode and is in a TRIGGERED state, an additional trigger event for the same CFIFO causes a trigger overrun:

1. The trigger overrun bit for the CFIFO is set (EQADC_FISRn[TORF*n*] = 1)
2. The EQADC_CFCRn[TORIE] and EQADC_FISRn[TORF] assert
3. The eQADC generates a trigger overrun interrupt request.

Refer to the following sections for more information:

Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)"

Section 19.3.2.6, "eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)"

For CFIFOs configured for level trigger mode, a trigger overrun event is detected only when the gate closes and reopens during a single serial command transmission as shown in Figure 19-40.

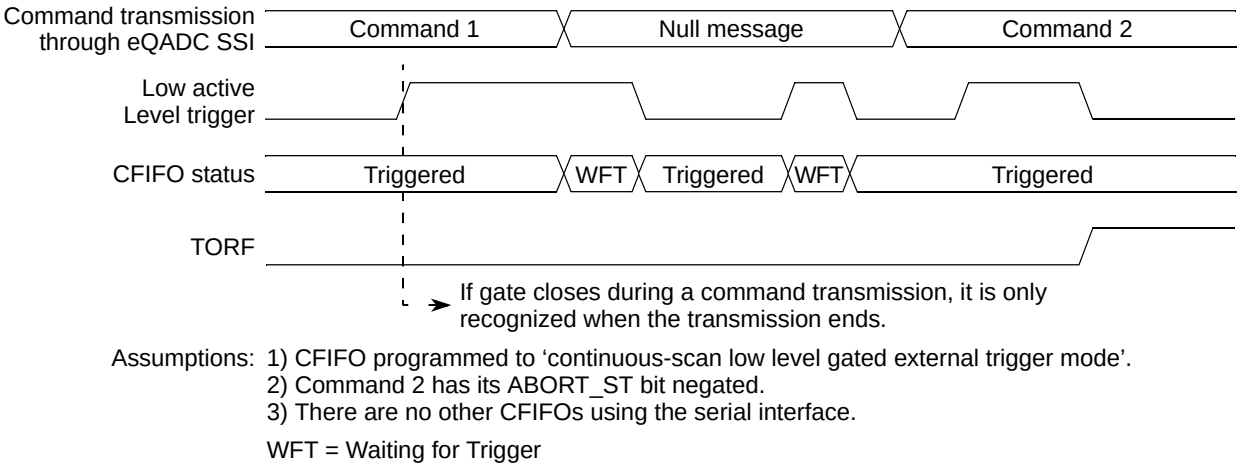


Figure 19-40. Trigger Overrun on Level Trigger Mode CFIFOs

NOTE

The trigger overrun flag is not set for CFIFOs configured for software trigger mode.

19.4.3.6.5 Command Sequence Non-Coherency Detection

The eQADC provides a mechanism to indicate if a command sequence has been completely executed without interruptions. A command sequence is defined as a group of consecutive commands bound for the same ADC and it is expected to be executed without interruptions. A command sequence is coherent if its commands are executed in order without interruptions. Because commands are stored in the ADC's command buffers before being executed in the eQADC, a command sequence is coherent if, while it is transferring commands to an on-chip ADC command buffer, the buffer is only fed with commands from that sequence without ever becoming empty.

A command sequence starts when:

- A CFIFO in TRIGGERED state transfers its first command to an on-chip ADC.

- The CFIFO is constantly transferring commands and the previous command sequence ended.
- The CFIFO resumes command transfers after being interrupted.

And a command sequence ended when:

- An asserted EOQ bit is detected on the last transferred command.
- CFIFO is in edge-trigger mode and asserted pause bit is detected on the last transferred command.
- The ADC to which the next command is sent is different from the ADC command last transferred.

Figure 19-41 shows examples of how the eQADC would detect command sequences when transferring commands from a CFIFO. The smallest possible command sequence can have a single command as shown in example 3 of Figure 19-41.

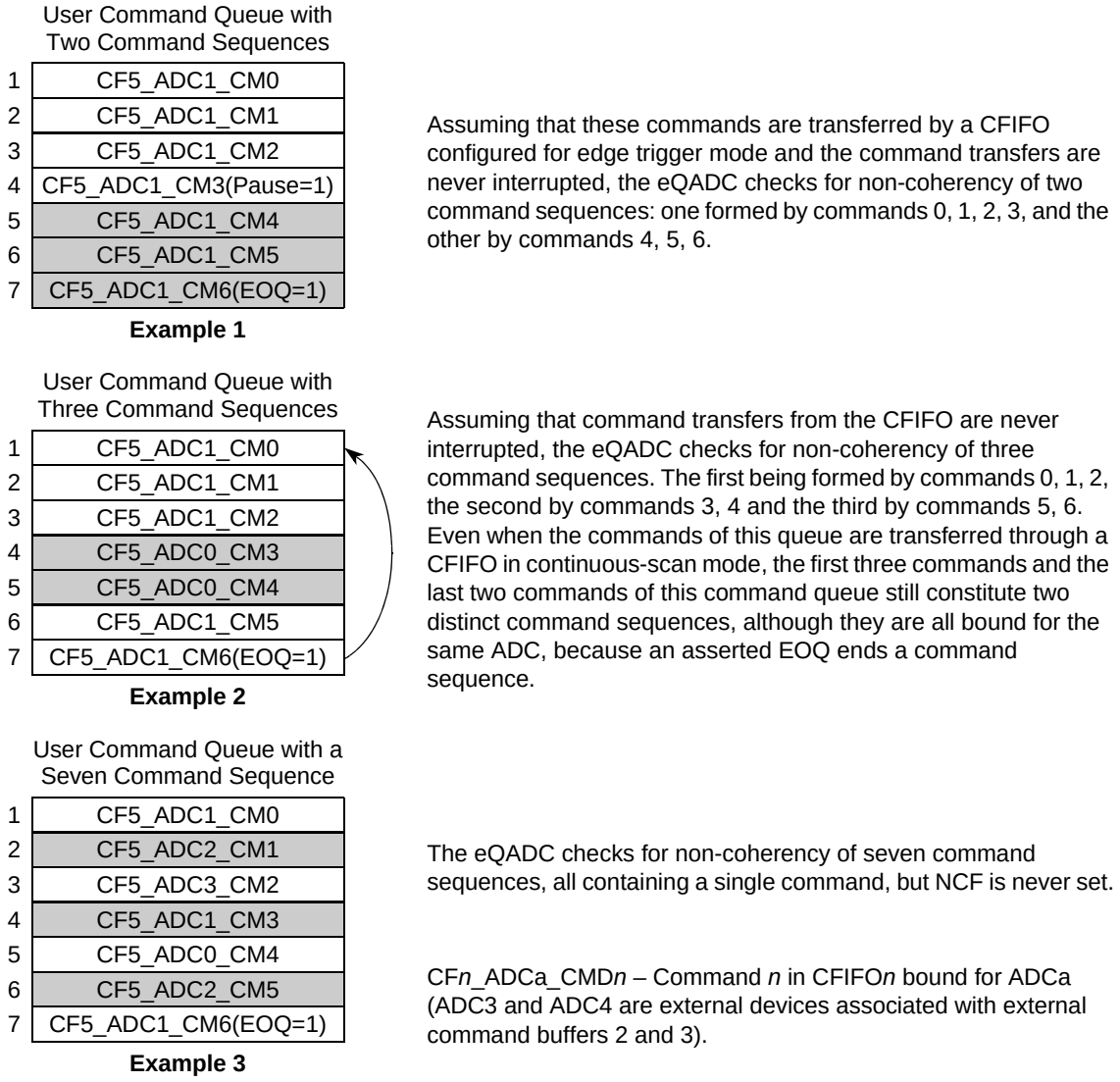


Figure 19-41. Command Sequence Examples

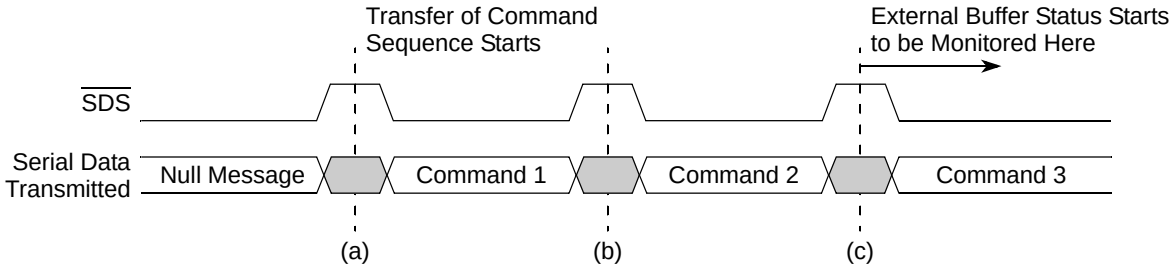
The NCF flag is used to indicate command sequence non-coherency. When the NCF*n* flag is asserted, it indicates that the command sequence being transferred through CFIFO*n* became non-coherent. The NCF flag only becomes asserted for CFIFOs in a TRIGGERED state.

A command sequence is non-coherent when, after transferring the first command of a sequence from a CFIFO to a buffer, it cannot successively send all the other commands of the sequence before any of the following conditions are true:

- The CFIFO through which commands are being transferred is pre-empted by a higher priority CFIFO which sends commands to the same ADC. The NCF flag becomes asserted immediately after the first command transfer from the pre-empting CFIFO, that is the higher priority CFIFO, to the ADC in use is completed. Refer to Figure 19-43.
- The external command buffer in use becomes empty. (Only the fullness of external buffers is monitored because the fill rate for internal ADC buffers is many times faster than the drain rate, and each has a dedicated priority engine.) This case happens when different CFIFOs attempt to use different external command buffers and the higher priority CFIFO bars the lower priority one from sending new commands to its buffer—see Figure 19-44. An external command buffer is considered empty when the corresponding BUSY field in the last result message received from external device is encoded as “Send available commands - buffer is empty”. Refer to Section , “Result Message Format for External Device Operation.” The NCF flag becomes asserted immediately after the eQADC detects that the external buffer in use becomes empty.

NOTE

After the transfer of a command sequence to an external command buffer starts, the eQADC ignores, for non-coherency detection purposes, the BUSY fields captured at the end of the first serial transmission. Thereafter, all BUSY fields captured at the end of consecutive serial transmissions are used to check the fullness of that external command buffer. This is done because the eQADC only updates its external ADC command buffer status record when it receives a serial message, resulting that the record kept by the eQADC is always outdated by, at least, the length of one serial transmission. This prevents a CFIFO from immediately becoming non-coherent when it starts transferring commands to an empty external command buffer. Refer to Figure 19-42 for an example.



Assumptions: 1) The CFIFO starts sending commands to an external command buffer when triggered.
2) Execution of a command on the external device takes longer than the time to complete two serial transmissions.

Figure 19-42. External Command Buffer Status Detection at Command Sequence Transfer Start

Table 19-46. External Buffer Status

Capture Point at eQADC	Buffer Status at External Device	Buffer Status as Captured by the eQADC	Used for NCF Detection on the eQADC?
(a)	EMPTY	EMPTY	No change
(b)	1 ENTRY	EMPTY	No
(c)	2 ENTRY	1 ENTRY	Yes

After the start of command sequence transfer, the eQADC checks for the command sequence coherency until the command sequence ends or one of the following conditions are true:

- Command sequence is non-coherent.
- CFIFO status changes from the TRIGGERED state
- CFIFO underflow occurs

NOTE

The NCF flag is asserted if an external command buffer empty event is detected at the same time the eQADC stops checking for the coherency of a command sequence.

After command transfers restart or continue, the non-coherency hardware operate as if the command sequence started from that point. Figure 19-45 depicts how the non-coherency hardware operates when a non-coherency event is detected.

NOTE

If MODE*n* is changed to disabled while a CFIFO is transferring commands, the NCF flag for that CFIFO is not asserted.

NOTE

When the eQADC enters debug or stop mode while a command sequence is executing, the NCF asserts if an empty external command buffer is detected after debug or stop mode exits.

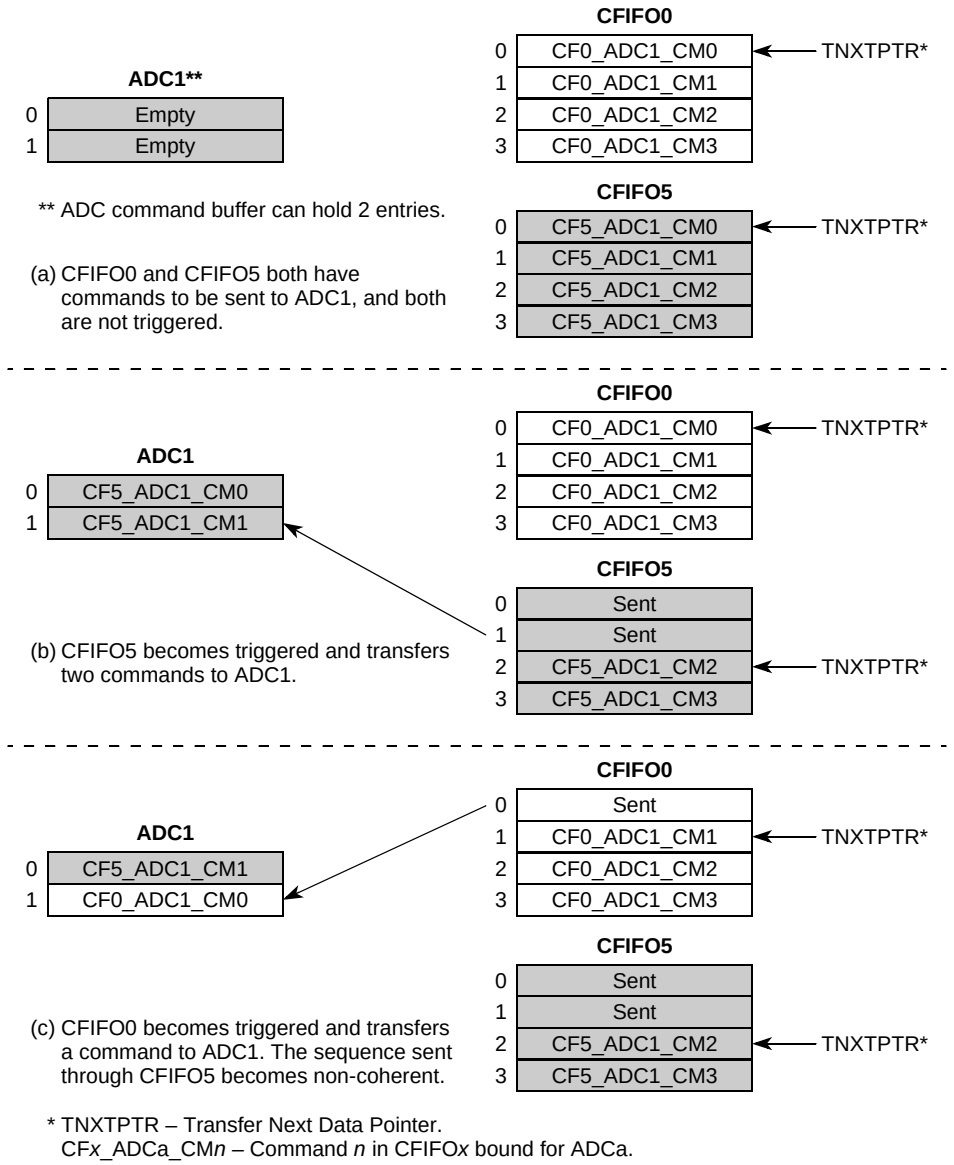


Figure 19-43. Non-Coherency Event When Different CFIFOs Use the Same Buffer

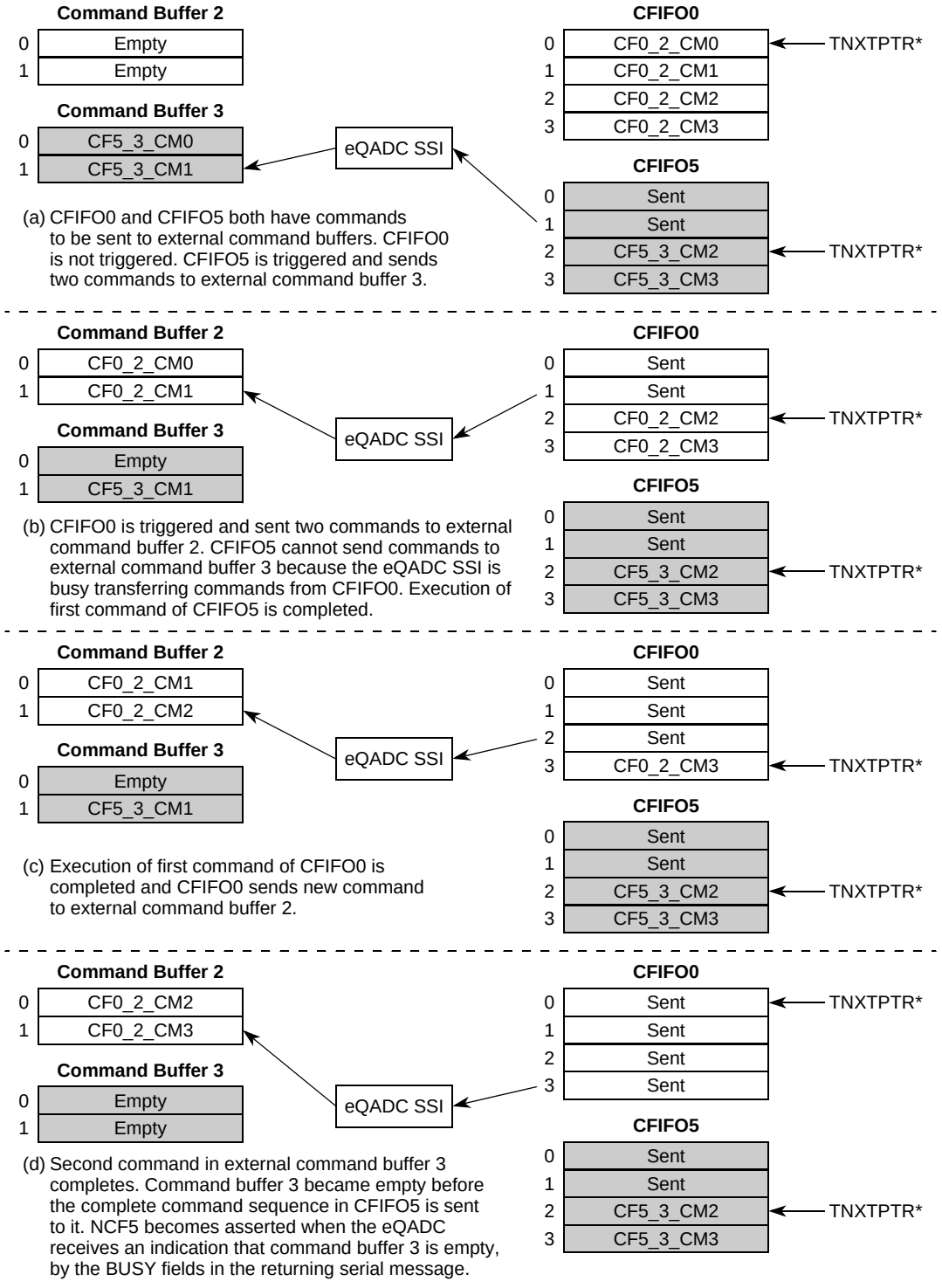


Figure 19-44. Non-Coherency Event When Different CFIFOs Are Using Different External Command Buffers

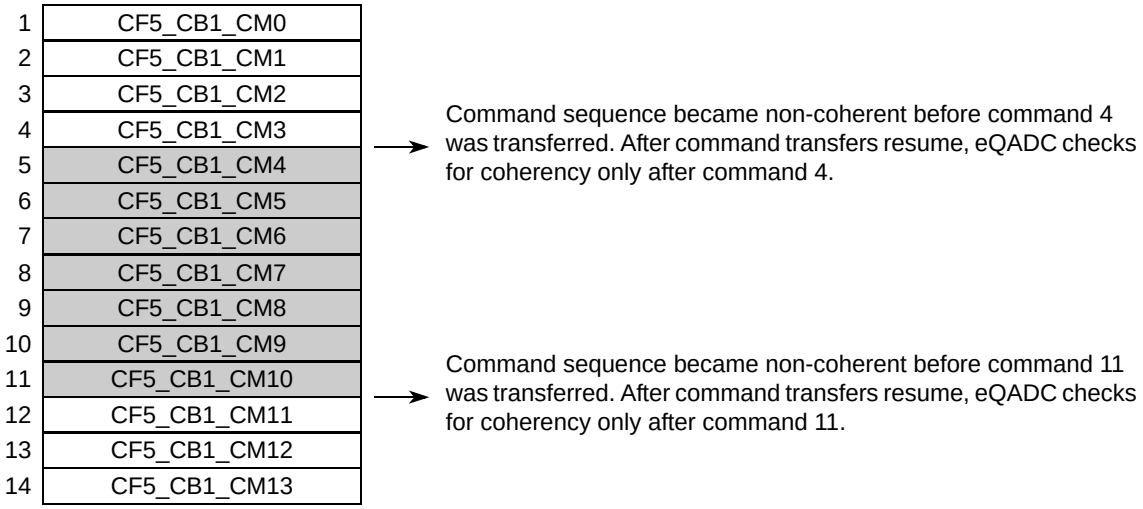


Figure 19-45. Non-coherency Detection When Transfers From a Command Sequence Are Interrupted

19.4.4 Result FIFOs

19.4.4.1 RFIFO Basic Functionality

There are six RFIFOs located in the eQADC. Each RFIFO is four entries deep, and each RFIFO entry is 16 bits long. Each RFIFO serves as a temporary storage location for the one of the result queues allocated in system memory. All result data is saved in the RFIFOs before being moved into the system result queues. When an RFIFO is not empty, the eQADC sets the corresponding EQADC_FISRn[RFDF] (see Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)”). If EQADC_IDCR*n*[RFDE] is asserted (see Section 19.3.2.7), the eQADC generates a request so that the RFIFO entry is moved to a result queue. An interrupt request, served by the host CPU, is generated when EQADC_IDCR*n*[RFDS] is negated, and an eDMA request, served by the eDMA, is generated when RFDS is asserted. The host CPU or the eDMA responds to these requests by reading EQADC_RFPRn (see Section 19.3.2.5, “eQADC Result FIFO Pop Registers 0–5 (EQADC_RFPRn)”) to retrieve data from the RFIFO.

NOTE

Reading a word, halfword, or any bytes from EQADC_RFPR*n* pops an entry from RFIFO*n*, and the RFCTR*n* field decrements by 1.

Configure the eDMA controller to read a single result (16-bit data) from the RFIFO pop registers for every asserted eDMA request it acknowledges. Refer to Section 19.5.2, “eQADC/eDMA Controller Interface” for eDMA controller configuration guidelines.

Figure 19-46 describes the important components in the RFIFO. Each RFIFO is implemented as a circular set of registers to avoid the need to move all entries at each push/pop operation. The pop next data pointer always points to the next RFIFO message to be retrieved from the RFIFO when reading eQADC_RFPR. The receive next data pointer points to the next available RFIFO location for storing the next incoming

message from the on-chip ADCs or from the external device. The RFIFO counter logic counts the number of entries in RFIFO and generates interrupt or eDMA requests to drain the RFIFO.

EQADC_FISRn[POPNXTPTR] (see Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)”) indicates which entry is currently being addressed by the pop next data pointer, and EQADC_FISRn[RFCTR] provides the number of entries stored in the RFIFO. Using POPNXTPTR and RFCTR, the absolute addresses for pop next data pointer and receive next data pointer can be calculated using the following formulas:

```
Pop Next Data Pointer Address= RFIFOn_BASE_ADDRESS + POPNXTPTRn x 4
Receive Next Data Pointer Address = RFIFOn_BASE_ADDRESS +
[(POPNXTPTRn + RFCTRn) mod RFIFO_DEPTH] x 4
```

where

- *a mod b* returns the remainder of the division of *a* by *b*.
- RFIFO*n*_BASE_ADDRESS is the smallest memory mapped address allocated to an RFIFO*n* entry.
- RFIFO_DEPTH is the number of entries contained in a RFIFO - four in this implementation.

When a new message arrives and RFIFO*n* is not full, the eQADC copies its contents into the entry pointed by receive next data pointer. The RFIFO counter EQADC_FISR*n*[RFCTR*n*] (see Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)”) is incremented by 1, and the receive next data pointer *n* is also incremented by 1 (or wrapped around) to point to the next empty entry in RFIFO*n*. However, if the RFIFO*n* is full, the eQADC sets the EQADC_FISR*n*[RFOF] (see Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)”). The RFIFO*n* does not overwrite the older data in the RFIFO, the new data is ignored, and the receive next data pointer *n* is not incremented or wrapped around. RFIFO*n* is full when the receive next data pointer *n* equals the pop next data pointer *n* and RFCTR*n* is not 0. RFIFO*n* is empty when the receive next data pointer *n* equals the pop next data pointer *n* and RFCTR*n* is 0.

When the eQADC RFIFO pop register *n* is read and the RFIFO*n* is not empty, the RFIFO counter RFCTR*n* is decremented by 1, and the pop next data pointer is incremented by 1 (or wrapped around) to point to the next RFIFO entry.

When the eQADC RFIFO pop register *n* is read and RFIFO*n* is empty, eQADC does not decrement the counter value and the pop next data pointer *n* is not updated. The read value is undefined.

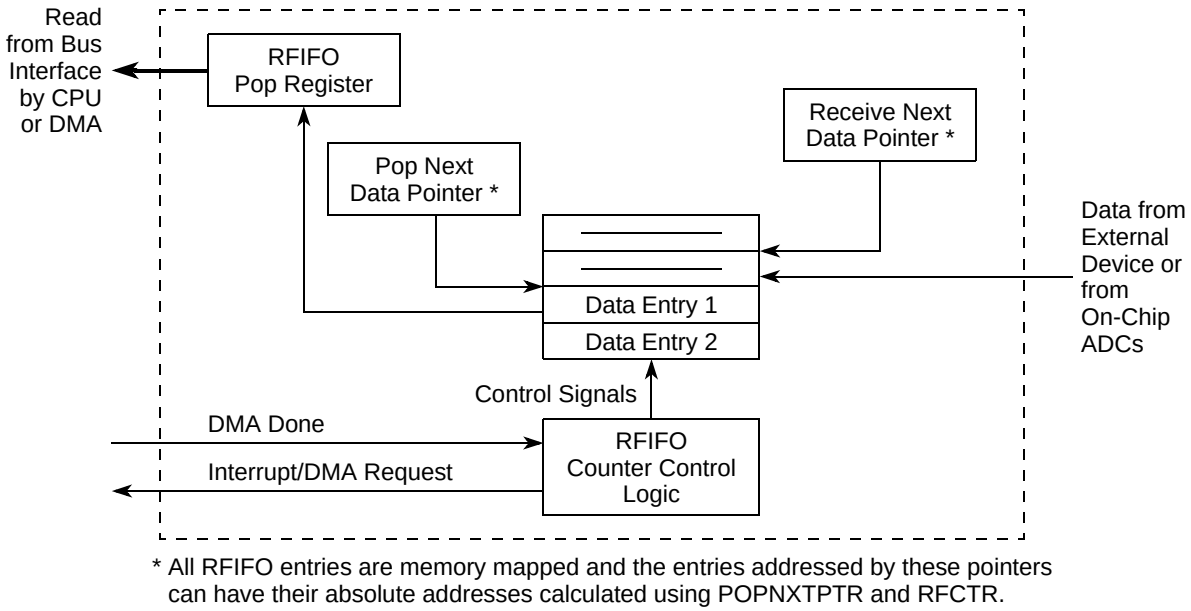


Figure 19-46. RFIFO Diagram

The detailed behavior of the pop next data pointer and receive next data pointer is described in the example shown in Figure 19-47 where an RFIFO with 16 entries is shown for clarity of explanation, the actual hardware implementation has only four entries. In this example, RFIFO*n* with 16 entries is shown in sequence after popping or receiving entries.

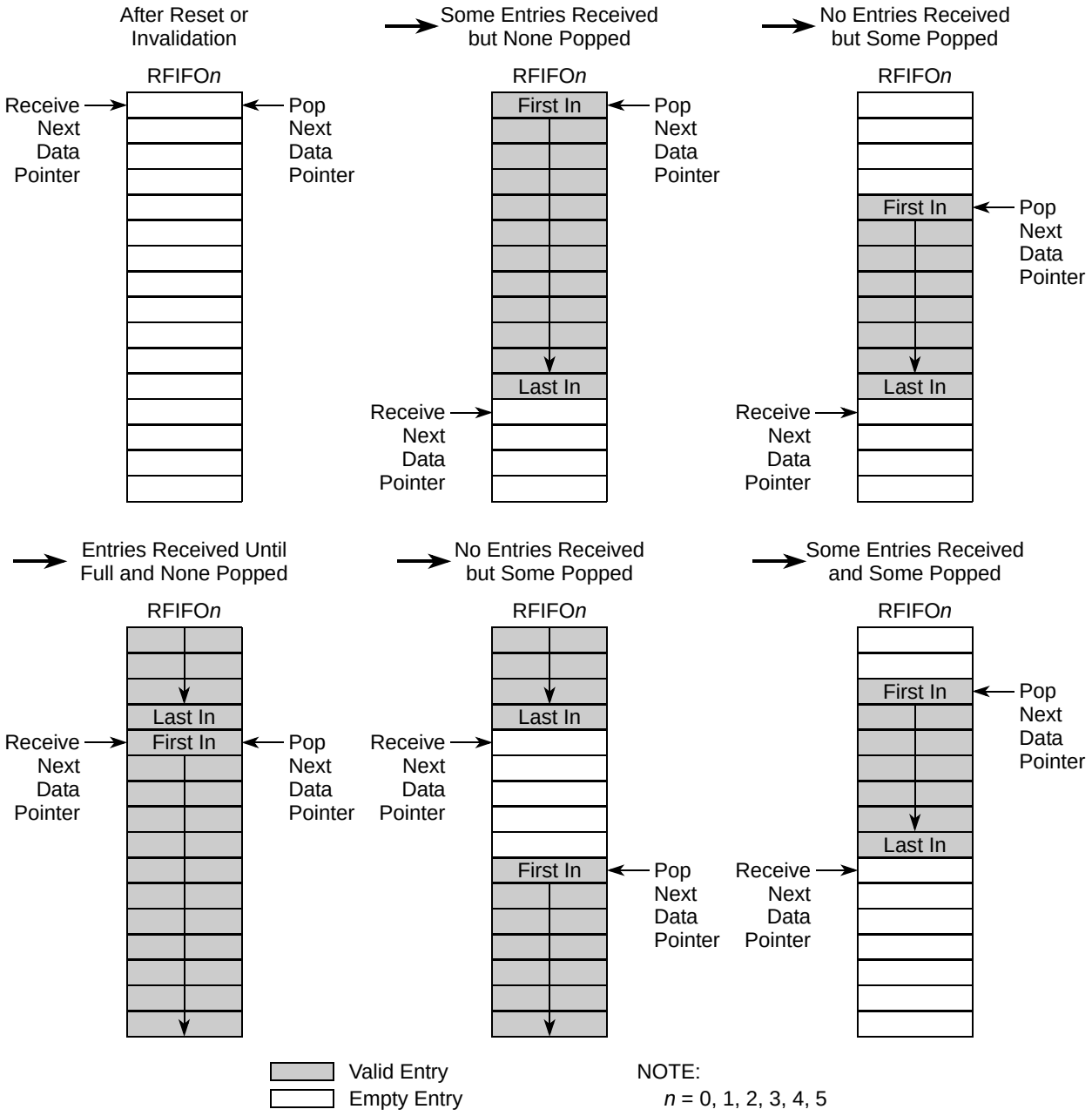


Figure 19-47. RFIFO Entry Pointer Example

19.4.4.2 Distributing Result Data into RFIFOs

Data to be moved into the RFIFOs can come from three sources: from ADC0, from ADC1, or from the external device. All result data comes with a MESSAGE_TAG field defining what to do with the received data. The FIFO control unit decodes the MESSAGE_TAG field and:

- Stores the 16-bit data into the appropriate RFIFO if the MESSAGE_TAG indicates a valid RFIFO number; or
- Ignores the data in case of a null or “reserved for customer use” MESSAGE_TAG

In general, received data is moved into RFIFOs as the data becomes available, while an exception happens when multiple results from different sources become available at the same time. In that case, result data from ADC0 is processed first, result data from ADC1 is only processed after all ADC0 data is processed, and result data from the external device is only processed after all data from ADC0/1 is processed.

When time-stamped results return from the on-chip ADCs, the conversion result and the time stamp are always moved to the RFIFOs in consecutive clock cycles to guarantee they are always stored in consecutive RFIFO entries.

19.4.5 On-Chip ADC Configuration and Control

19.4.5.1 Enabling and Disabling the on-chip ADCs

The on-chip ADCs have an enable bit (ADC0_CR[ADC0_EN] and ADC1_CR[ADC1_EN], see Section 19.3.3.1, “ADCn Control Registers (ADC0_CR and ADC1_CR)”) which allows the enabling of the ADCs only when necessary. When the enable bit for an ADC is negated, the clock input to that ADC is stopped. The ADCs are disabled out of reset - ADC0/1_EN bits are negated - to allow for their safe configuration. The ADC must only be configured when its enable bit is negated. After the enable bit of an ADC is asserted, clock input is started, and the bias generator circuit is turned on. When the enable bits of both ADCs are negated, the bias circuit generator is stopped.

NOTE

An 8ms wait time from V_{DDA} power up to enabling an ADC is required to pre-charge the external 100nf capacitor on REFBYPC. This time must be guaranteed by the crystal startup time plus the reset duration, or the host application. The ADC internal bias generator circuit starts up after 10υs upon VRH/VRL power up to stabilize the required bias current to the pre-charge circuit; the current to the other analog circuits are disabled until the ADCs are enabled. As soon as the ADCs are enabled, the bias currents to other analog circuits are ready.

NOTE

The eQADC is designed to wait 120 ADC clocks after an on-chip ADC enables or the eQADC exits stop mode before the first conversion command is issued. Two independent counters monitor the delay, one clocked by ADC0_CLK and another by ADC1_CLK. Conversion commands can begin executing when one of the counters reaches 120 ADC clocks. Conversion commands sent to a disabled ADC are ignored by the ADC control hardware.

19.4.5.2 ADC Clock and Conversion Speed

The clock input to the ADCs is defined by setting the ADC0_CR[ADC0_CLK_PS] and ADC1_CR[ADC1_CLK_PS] fields. Refer to Section 19.3.3.1, “ADCn Control Registers (ADC0_CR and ADC1_CR).” The ADC0/1_CLK_PS field selects the clock divide factor by which the system clock is

divided as showed in Table 19-28. The ADC clock frequency is calculated as below and it must not exceed 12 MHz.

$$ADCClockFrequency = \frac{SystemClockFrequency(MHz)}{SystemClockDivideFactor}; (ADCClockFrequency \leq 12MHz)$$

Figure 19-48 depicts how the ADC clocks for ADC0 and ADC1 are generated.

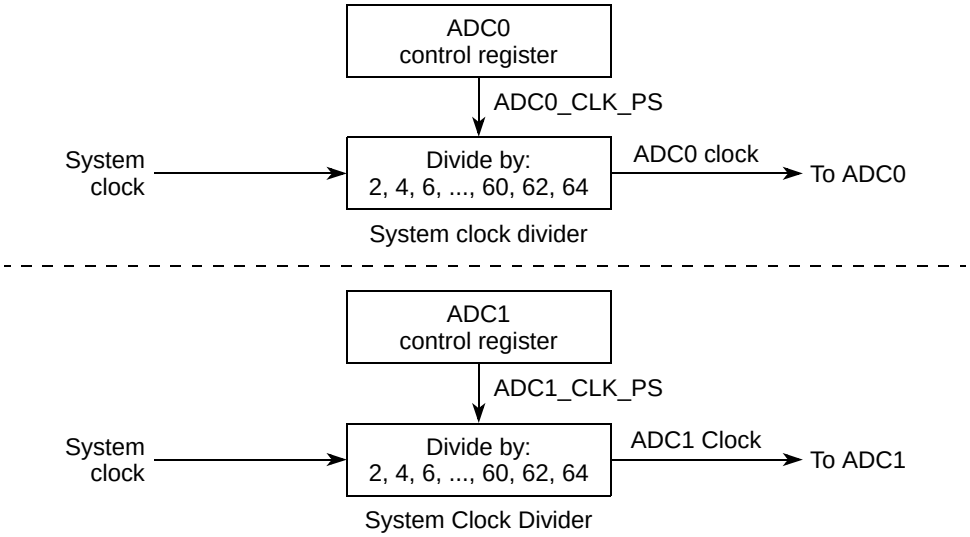


Figure 19-48. ADC0/1 Clock Generation

The ADC conversion speed (in kilosamples per second – ksamp/s) is calculated by the following formula. The number of sampling cycles is determined by the LST bits in the command message — see Section , "Conversion Command Message Format for On-Chip ADC Operation," — and it can take one of the following values: 2, 8, 64, or 128 ADC clock cycles. The number of AD conversion cycles is 13 for differential conversions and 14 for single-ended conversions. The maximum conversion speed is achieved when the ADC Clock frequency is set to its maximum (12Mhz) and the number of sampling cycles set to its minimum (2 cycles). The maximum conversion speed for differential and single-ended conversions are 800 k samples/sec and 750 k samples/sec, respectively.

$$ADCConversionSpeed = \frac{ADCClockFrequency(MHz)}{(NumberOfSamplingCycles + NumberOfADConversionCycles)}$$

Table 19-47 shows an example of how the ADC0/1_CLK_PS can be set when using a 120 MHz system clock and the corresponding conversion speeds for all possible ADC clock frequencies. The table also shows that according to the system clock frequency, certain clock divide factors are invalid (2, 4, 6, 8 clock divide factors in the example) since their use would result in a ADC clock frequency higher than the maximum one supported by the ADC. ADC clock frequency must not exceed 12 Mhz.

Table 19-47. ADC Clock Configuration Example (System Clock Frequency = 120 MHz)

ADC0/1_CLK_PS[0:4]	System Clock Divide Factor	ADC Clock in MHz (System Clock = 120MHz)	Differential Conversion Speed with Default Sampling Time (13 + 2 cycles) in ksamp/s	Single-Ended Conversion Speed with Default Sampling Time (14 + 2 cycles) in ksamp/s
0b00000	2	N/A	N/A	N/A
0b00001	4	N/A	N/A	N/A
0b00010	6	N/A	N/A	N/A
0b00011	8	N/A	N/A	N/A
0b00100	10	12.0	800	750
0b00101	12	10.0	667	625
0b00110	14	8.57	571	536
0b00111	16	7.5	500	469
0b01000	18	6.67	444	417
0b01001	20	6.0	400	375
0b01010	22	5.45	364	341
0b01011	24	5.0	333	313
0b01100	26	4.62	308	288
0b01101	28	4.29	286	268
0b01110	30	4.0	267	250
0b01111	32	3.75	250	234
0b10000	34	3.53	235	221
0b10001	36	3.33	222	208
0b10010	38	3.16	211	197
0b10011	40	3.0	200	188
0b10100	42	2.86	190	179
0b10101	44	2.73	182	170
0b10110	46	2.61	174	163
0b10111	48	2.5	167	156
0b11000	50	2.4	160	150
0b11001	52	2.31	154	144
0b11010	54	2.22	148	139
0b11011	56	2.14	143	134
0b11100	58	2.07	138	129
0b11101	60	2.0	133	125

Table 19-47. ADC Clock Configuration Example (System Clock Frequency = 120 MHz)

ADC0/1_CLK_PS[0:4]	System Clock Divide Factor	ADC Clock in MHz (System Clock = 120MHz)	Differential Conversion Speed with Default Sampling Time (13 + 2 cycles) in ksamp/s	Single-Ended Conversion Speed with Default Sampling Time (14 + 2 cycles) in ksamp/s
0b11110	62	1.94	129	121
0b11111	64	1.88	125	117

19.4.5.3 Time Stamp Feature

The on-chip ADCs can provide a time stamp for the conversions they execute. A time stamp is the value of the time base counter latched when the eQADC detects the end of the analog input voltage sampling. A time stamp for a conversion command is requested by setting the TSR bit in the corresponding command. When TSR is negated, that is a time stamp is not requested, the ADC returns a single result message containing the conversion result. When TSR is asserted, that is a time stamp is requested, the ADC returns two result messages; one containing the conversion result, and another containing the time stamp for that conversion. The result messages are sent in this order to the RFIFOs and both messages are sent to the same RFIFO as specified in the MESSAGE_TAG field of the executed conversion command.

The time base counter is a 16-bit up counter and wraps after reaching 0xFFFF. It is disabled after reset and it is enabled according to the setting of ADC_TSCR[TBC_CLK_PS] field (see Section 19.3.3.2, “ADC Time Stamp Control Register (ADC_TSCR)”). TBC_CLK_PS defines if the counter is enabled or disabled, and, if enabled, at what frequency it is incremented. The time stamps are returned regardless of whether the time base counter is enabled or disabled. The time base counter can be reset by writing 0x0000 to the ADC_TBCR (Section 19.3.3.3, “ADC Time Base Counter Registers (ADC_TBCR)”) with a write configuration command.

19.4.5.4 ADC Calibration Feature

19.4.5.4.1 Calibration Overview

The eQADC provides a calibration scheme to remove the effects of gain and offset errors from the results generated by the on-chip ADCs. Only results generated by the on-chip ADCs are calibrated. The results generated by ADCs on the external device are directly sent to RFIFOs unchanged. The main component of calibration hardware is a multiply-and-accumulate (MAC) unit, one per on-chip ADC, that is used to calculate the following transfer function which relates a calibrated result to a raw, uncalibrated one.

CAL_RES = GCC x (RAW_RES + OCC + 2);

where:

- CAL_RES is the calibrated result corresponding the input voltage V_i.
- GCC is the gain calibration constant.
- RAW_RES is the raw, uncalibrated result corresponding to an specific input voltage V_i.
- OCC is the offset calibration constant.

- The addition of two reduces the maximum quantization error of the ADC. Refer to Section 19.5.6.3, “Quantization Error Reduction During Calibration**.”**

Calibration constants GCC and OCC are determined by taking two samples of known reference voltages and using these samples to calculate their values. For details and example about how to calculate the calibration constants and use them in result calibration refer to Section 19.5.6, “ADC Result Calibration.” After it is calculated, the GCC coefficients are stored in ADC0_GCCR and ADC1_GCCR (see Section 19.3.3.4, “ADCn Gain Calibration Constant Registers (ADC0_GCCR and ADC1_GCCR)”) and the OCC coefficients in ADC0_OCCR and ADC1_OCCR (see Section 19.3.3.5, “ADCn Offset Calibration Constant Registers (ADC0_OCCR and ADC1_OCCR)”) from where their values are fed to the MAC unit. Since the analog characteristics of each on-chip ADC differs, each ADC has an independent pair of calibration constants.

A conversion result is calibrated according to the status of CAL bit in the command that initiated the conversion. If the CAL bit is asserted, the eQADC automatically calculates the calibrated result before sending the result to the appropriate RFIFO. If the CAL bit is negated, the result is not calibrated, it bypasses the calibration hardware, and is directly sent to the appropriate RFIFO.

19.4.5.4.2 MAC Unit and Operand Data Format

The MAC unit diagram is shown in Figure 19-49. Each on-chip ADC has a separate MAC unit to calibrate its conversion results.

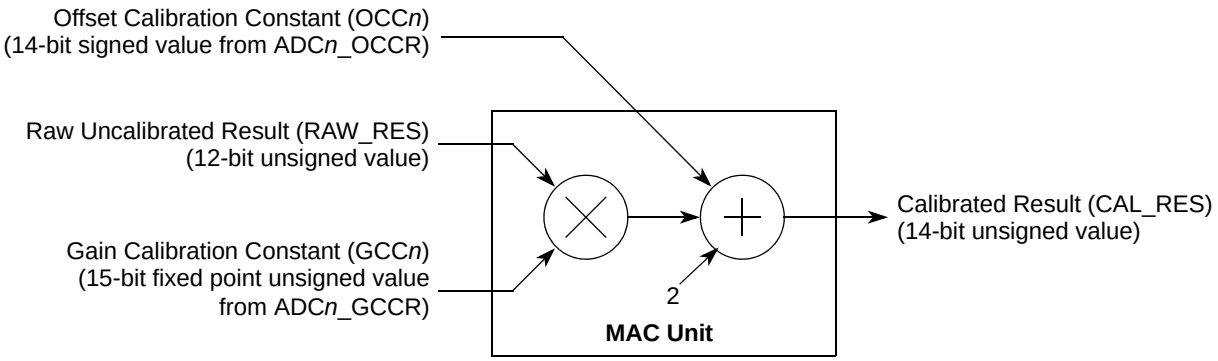


Figure 19-49. MAC Unit Diagram

The OCC*n* operand is a 14-bit signed value and it is the upper 14 bits of the value stored in ADC0_OCCR and ADC1_OCCR. The RAW_RES operand is the raw uncalibrated result, and it is a direct output from the on-chip ADCs.

The GCC*n* operand is a 15-bit fixed point unsigned value, and it is the upper 15 bits of the value stored in ADC0_GCCR and ADC1_GCCR. The GCC is expressed in the *GCC_INT.GCC_FRAC* binary format. The integer part of the GCC (GCC_INT = GCC[1]) contains a single binary digit while its fractional part (GCC_FRAC = GCC[2:15]) contains 14 bits. Refer to Figure 19-50 for more information. The gain constant equivalent decimal value ranges from 0 to 1.999938..., as shown in Table 19-49. Two is always added to the MAC output: see Section 19.5.6.3, “Quantization Error Reduction During Calibration. CAL_RES output is the calibrated result, and it is a 14-bit unsigned value. CAL_RES is truncated to 0x3FFF, in case of a overflow, and to 0x0000, in case of an underflow.

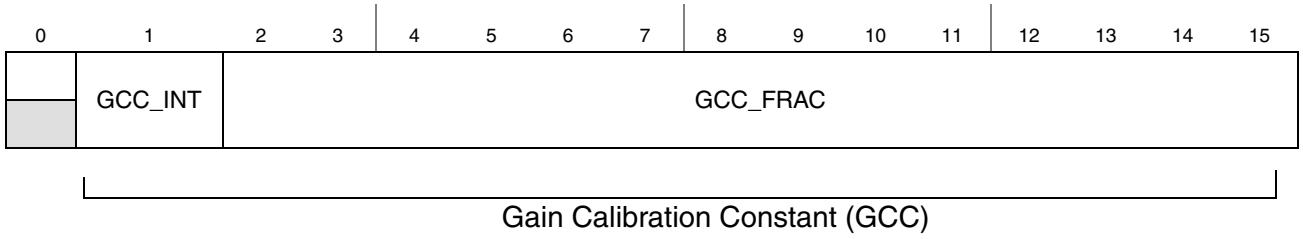


Figure 19-50. Gain Calibration Constant Format

Table 19-48. Gain Calibration Constant Format Field Descriptions

Field	Description
0	Reserved
1 GCC_INT	Integer part of the gain calibration constant for ADC*n*. GCC_INT is the integer part of the gain calibration constant (GCC) for ADC0/1. 0 = ADC0 1 = ADC1
2–15 GCC_FRAC [1:14]	Fractional part of the gain calibration constant for ADC*n*. GCC_FRAC is the fractional part of the gain calibration constant (GCC) for ADC*n*. GCC_FRAC can expresses decimal values ranging from 0 to 0.999938...

Table 19-49. Correspondence between Binary and Decimal Representations of the Gain Constant

Gain Constant (GCC_INT.GCC_FRAC binary format)	Corresponding Decimal Value
0.0000_0000_0000_00	0
...	...
0.1000_0000_0000_00	0.5
...	...
0.1111_1111_1111_11	0.999938...
1.0000_0000_0000_00	1
...	...
1.1100_0000_0000_00	1.75
...	...
1.1111_1111_1111_11	1.999938...

19.4.5.5 ADC Control Logic Overview and Command Execution

Figure 19-51 shows the basic logic blocks involved in the ADC control and how they interact. CFIFOs/RFIFOs interact with ADC command/result message return logic through the FIFO control unit. The EB and BN bits in the command message uniquely identify the ADC to which the command is sent. The FIFO control unit decodes these bits and sends the ADC command to the proper ADC. Other blocks of logic are the result format and calibration submodule, the time stamp logic, and the MUX control logic.

The result format and calibration submodule formats the returning data into result messages and sends them to the RFIFOs. The returning data can be data read from an ADC register, a conversion result, or a time stamp. The formatting and calibration of conversion results also take place inside this submodule.

The time stamp logic latches the value of the time base counter when detecting the end of the analog input voltage sampling, and sends it to the result format and calibration submodule as time stamp information.

The MUX control logic generates the proper MUX control signals and, when the ADC0/1_EMUX bits are asserted, the MA signals based on the channel numbers extracted from the ADC Command.

ADC commands are stored in the ADC command buffers (2 entries) as they come in and they are executed on a first-in-first-out basis. After the execution of a command in ENTRY1 finishes, all commands are shifted one entry. After the shift, ENTRY0 is always empty and ready to receive a new command. Execution of configuration commands only starts when they reach ENTRY1. Consecutive conversion commands are pipelined, and their execution can start while in ENTRY0. This is explained below.

A/D conversion accuracy can be affected by the settling time of the input channel multiplexers. Some time is required for the channel multiplexer's internal capacitances to settle after the channel number is changed. If the time prior to and during sampling is not long enough to permit this settling, then the voltage on the sample capacitors do not accurately represent the voltage to be read. This is a problem in particular when external muxes are used.

To maximize settling time, when a conversion command is in buffer ENTRY1 and another conversion command is identified in ENTRY0, then the channel number of ENTRY0 is sent to the *MUX control logic* half an ADC clock before the start of the sampling phase of the command in ENTRY0. This pipelining of sample and settling phase is shown in Figure 19-52(b).

This provides more accurate sampling, which is specially important for applications that require high conversion speeds, i.e., with the ADC running at maximum clock frequency and with the analog input voltage sampling time set to a minimum (2 ADC clock cycles). In this case the short sampling time may not allow the multiplexers to completely settle. The second advantage of pipelining conversion commands is to provide equal conversion intervals even though the sample time increases on second and subsequent conversions. Refer to Figure 19-52. This is important for any digital signal process application.

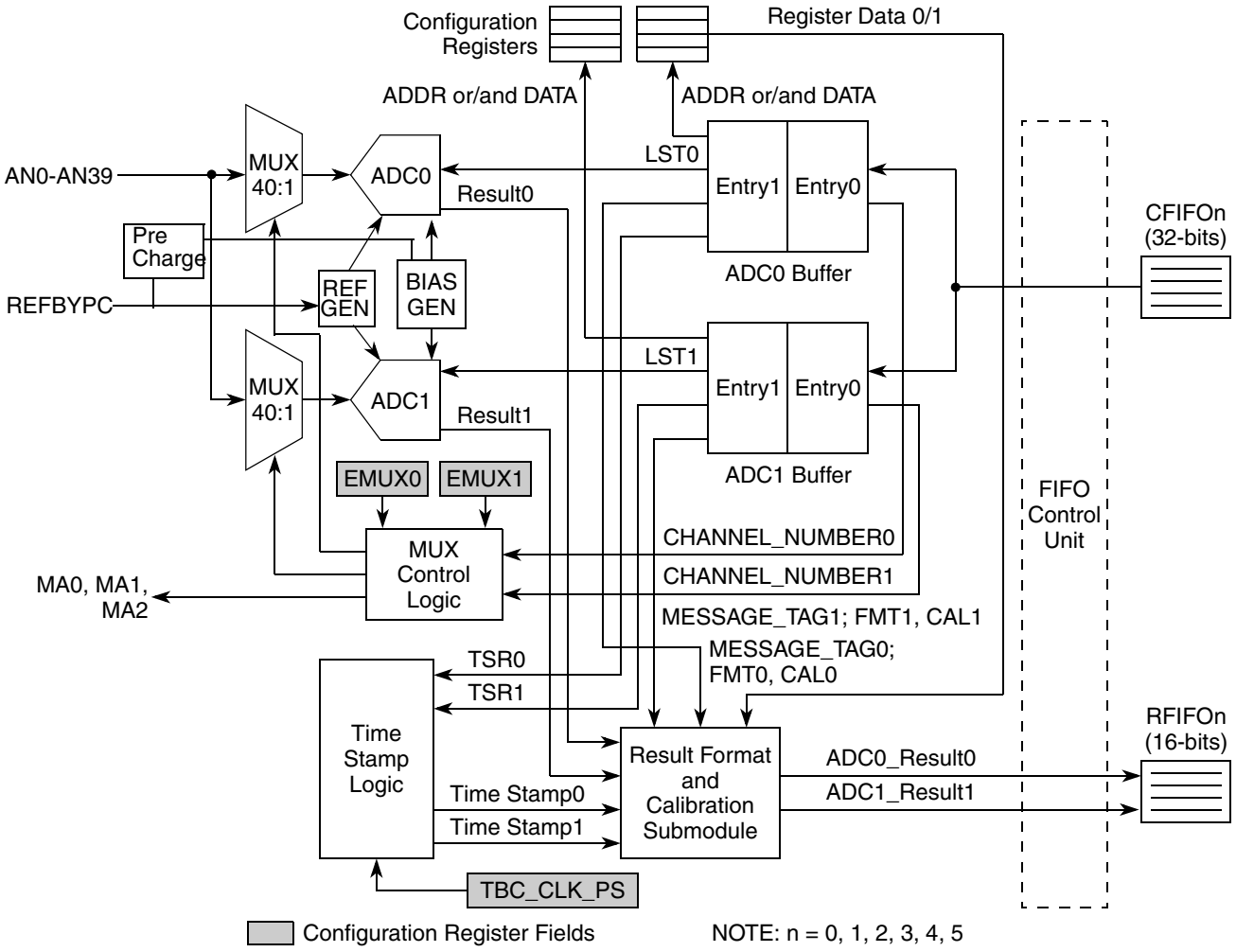


Figure 19-51. On-Chip ADC Control Scheme

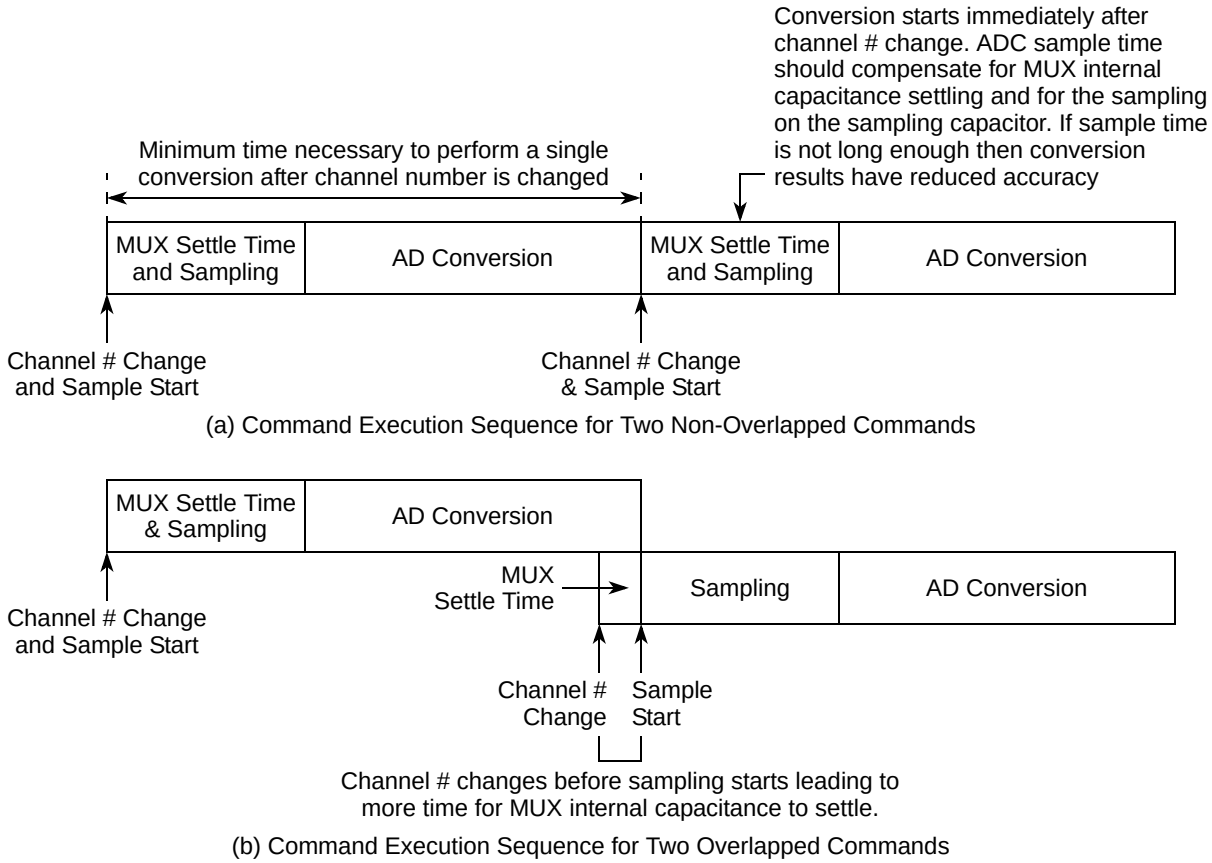


Figure 19-52. Overlapping Consecutive Conversion Commands

19.4.6 Internal/External Multiplexing

19.4.6.1 Channel Assignment

The internal analog multiplexers select one of the 40 analog input pins for conversion, based on the CHANNEL_NUMBER field of a Command Message. The analog input pin channel number assignments and the pin definitions vary depending on how the ADC0/1_EMUX are configured. Only one ADC can drive the external mux address pins: therefore ADC0_EMUX and ADC1_EMUX must not be asserted at the same time.

During differential conversions the analog multiplexer passes differential signals to both the positive and negative terminals of the ADC. The differential conversions can only be initiated on four channels: DAN0, DAN1, DAN2, and DAN3. Refer to Table 19-51 and Figure 19-52 for the channel numbers used to select differential conversions.

Table 19-50. ADC*n*_EMUX Bits Combinations

ADC0_EMUX	ADC1_EMUX	Set CHANNEL_NUMBER	
		ADC0	ADC1
0	0	No external mux	No external mux
0	1	ADC1 uses the external mux	ADC1 uses the external mux
1	0	ADC0 uses the external mux	ADC0 uses the external mux
1	1	Do not use – reserved	

Table 19-51 shows the channel number assignments for the non-multiplexed mode. The 40 single-ended channels and 4 differential pairs are shared between the two ADCs.

Table 19-51. Non-multiplexed Channel Assignments[1]

Input Pins			Channel Number in CHANNEL_NUMBER Field	
Analog Pin Name	Other Functions	Conversion Type	Binary	Decimal
AN[0]–AN[39]		Single-ended	0000_0000–0010_0111	0–39
V_{RH}		Single-ended	0010_1000	40
V_{RL}		Single-ended	0010_1001	41
	(V_{RH} - V_{RL}) ÷ 2 see footnote[2]	Single-ended	0010_1010	42
	75% x (V_{RH} - V_{RL})	Single-ended	0010_1011	43
	25% x (V_{RH} - V_{RL})	Single-ended	0010_1100	44
Reserved			0010_1101–0101_1111	45–95
DAN0+ and DAN0- DAN1+ and DAN1- DAN2+ and DAN2- DAN3+ and DAN3-		Differential Differential Differential Differential	0110_0000 0110_0001 0110_0010 0110_0011	96 97 98 99
Reserved			0110_0100–1111_1111	100–255

1 The two on-chip ADCs can access the same analog input pins but simultaneous conversions are not allowed. Also, when one ADC is performing a differential conversion on a pair of pins, the other ADC must not access either of these two pins as single-ended channels.

2 This equation only applies before calibration. After calibration, the 50% reference point returns approximately 20mV lower than the expected 50% of the difference between the High Reference Voltage (V_{RH}) and the Low Reference Voltage (V_{RL}). For calibration of the ADC, only use the 25% and 75% points as described in Section 19.5.6.1, "MAC Configuration Procedure"

Table 19-52 shows the channel number assignments for multiplexed mode. The ADC with the ADC*n*_EMUX bit asserted can access at most 33 single-ended and 32 externally multiplexed channels. Refer to Section 19.4.6.2, "External Multiplexing," for a detailed explanation about how external multiplexing can be achieved.

Table 19-52. Multiplexed Channel Assignments[1]

Input Pins			Channel Number in CHANNEL_NUMBER Field	
Analog Pin Name	**Other Functions**	**Conversion Type**	**Binary**	**Decimal**
AN[0]–AN[7]		Single-ended	0000_0000–0000_0111	0–7
Used for digital address lines of the external mux			0000_1000–0000_1011	8–11
AN[12]–AN[39]		Single-ended	0000_1100–0010_0111	12–39
V_{RH}		Single-ended	0010_1000	40
V_{RL}		Single-ended	0010_1001	41
	$(V_{RH} - V_{RL}) \div 2$	Single-ended	0010_1010	42
	75% x $(V_{RH} - V_{RL})$	Single-ended	0010_1011	43
	25% x $(V_{RH} - V_{RL})$	Single-ended	0010_1100	44
Reserved			0010_1101–0011_1111	45–63
ANW ANX ANY ANZ	— — — —	Single-ended Single-ended Single-ended Single-ended	0100_0xxx 0100_1xxx 0101_0xxx 0101_1xxx	64–71 72–79 80–87 88–95
DAN0+ and DAN0- DAN1+ and DAN1- DAN2+ and DAN2- DAN3+ and DAN3-		Differential Differential Differential Differential	0110_0000 0110_0001 0110_0010 0110_0011	96 97 98 99
Reserved			0011_0100–1111_1111	100–255

[1] The two on-chip ADCs can access the same analog input pins but simultaneous conversions are not allowed. Also, when one ADC is performing a differential conversion on a pair of pins, the other ADC must not access either of these two pins as single-ended channels.

19.4.6.2 External Multiplexing

The eQADC can use from one to four external multiplexers to expand the number of analog signals that may be converted. Using this configuration, up to 25 additional channels can be created.

- The first external multiplexer requires one common analog pin and three address pins, so although eight additional ADC channels are created, four existing channels are lost, so there is a net addition of four channels.
- For subsequent external multiplexers, only one additional internal channel is lost so there is a net addition of seven channels.

The externally multiplexed channels are automatically selected by the CHANNEL_NUMBER field of a command message, in the same way done with internally multiplexed channels. The software selects the external multiplexed mode by setting the ADC0/1_EMUX bit in either ADC0_CR or ADC1_CR depending on which ADC performs the conversion. Figure 19-52 shows the channel number assignments for the multiplexed mode. Only one ADC can have its ADC0/1_EMUX bit asserted at a time.

Figure 19-53 shows the maximum configuration of four external multiplexer chips connected to the eQADC. The external multiplexer chip selects one of eight analog inputs and connects it to a single analog output, which is fed to a specific input of the eQADC. The eQADC provides three multiplexed address signals, MA[0], MA[1], and MA[2], to select one of eight inputs. These three multiplexed address signals are connected to all four external multiplexer chips. The analog output of the four multiplex chips are each connected to four separate eQADC inputs, ANW, ANX, ANY, and ANZ. The MA pins correspond to the three least significant bits of the channel number that selects ANW, ANX, ANY, and ANZ with MA[0] being the most significant bit. Refer to Table 19-53.

Table 19-53. Encoding of MA Pins[1]

Channel Number selecting ANW, ANX, ANY, ANZ (decimal)				MA0	MA1	MA2
ANW	ANX	ANY	ANZ			
64	72	80	88	0	0	0
65	73	81	89	0	0	1
66	74	82	90	0	1	0
67	75	83	91	0	1	1
68	76	84	92	1	0	0
69	77	85	93	1	0	1
70	78	86	94	1	1	0
71	79	87	95	1	1	1

[1] 0 means pin is driven LOW and 1 that pin is driven HIGH.

When the external multiplexed mode is selected for either ADC, the eQADC automatically creates the MA output signals from CHANNEL_NUMBER field of a command message. The eQADC also converts the proper input channel (ANW, ANX, ANY, and ANZ) by interpreting the CHANNEL_NUMBER field. As a result, up to 32 externally multiplexed channels appear to the conversion queues as directly connected signals.

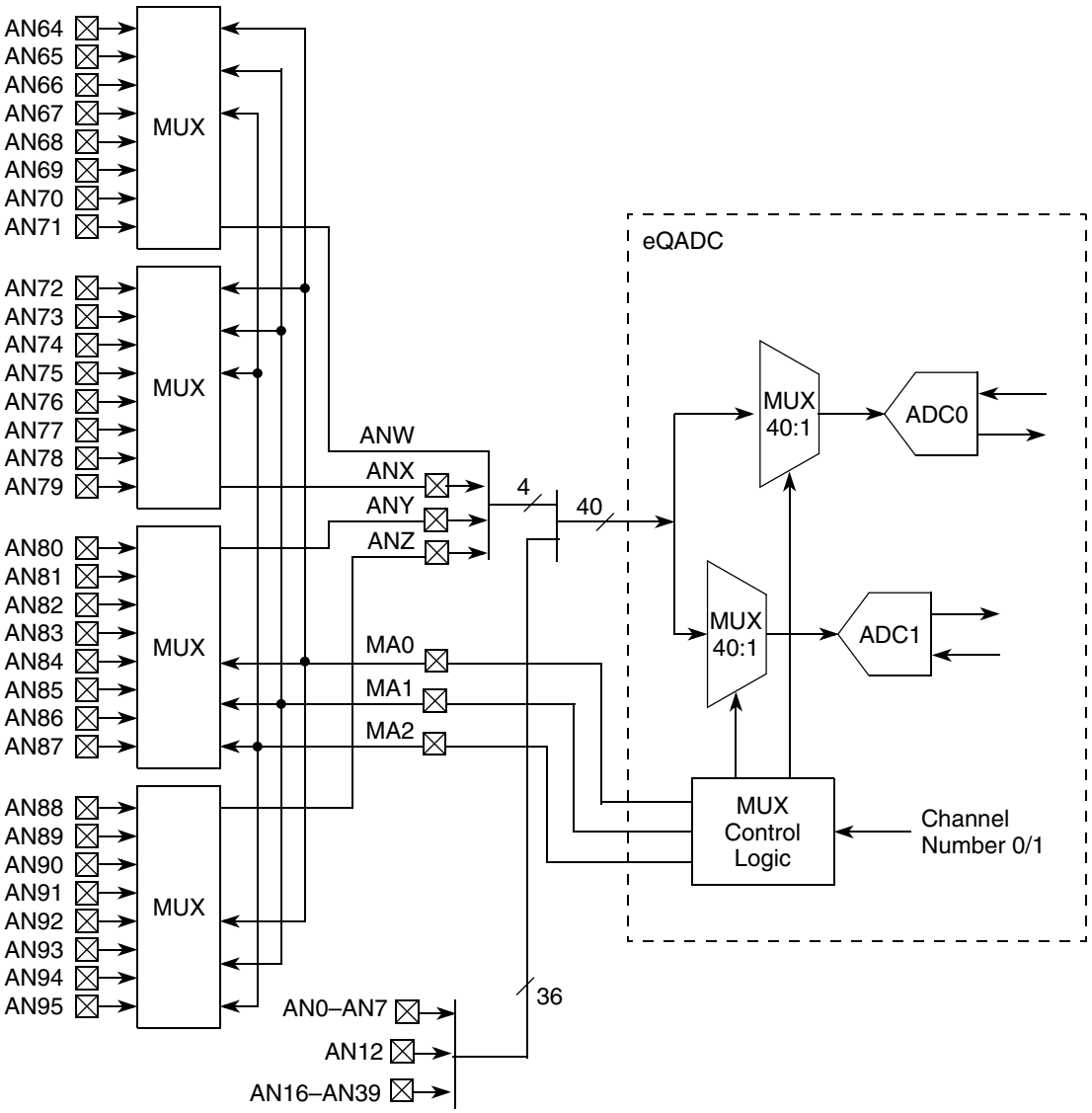


Figure 19-53. Example of External Multiplexing

19.4.7 eQADC eDMA/Interrupt Request

Table 19-54 lists methods to generate interrupt requests in the eQADC queuing control and triggering control. The eDMA/interrupt request select bits and the eDMA/interrupt enable bits are described in Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn),” and the interrupt flag bits are described in Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn).” Table 19-54 depicts all interrupts and eDMA requests generated by the eQADC.

Table 19-54. eQADC FIFO Interrupt Summary[1]

Interrupt	Condition	Clearing Mechanism
Non Coherency Interrupt	NCIE*n* = 1 NCF*n* = 1	Clear NCF*n* bit by writing a 1 to the bit.
Trigger Overrun Interrupt [2]	TORIE*n* = 1 TORF*n* =1	Clear TORF*n* bit by writing a 1 to the bit.
Pause Interrupt	PIE*n* = 1 PF*n* =1	Clear PF*n* bit by writing a 1 to the bit.
End of Queue Interrupt	EOQIE*n* = 1 EOQF*n* = 1	Clear EOQF*n* bit by writing a 1 to the bit.
Command FIFO Underflow Interrupt [2]	CFUIE*n* = 1 CFUF*n* = 1	Clear CFUF*n* bit by writing a 1 to the bit.
Command FIFO Fill Interrupt	CFFE*n* = 1 CFFS*n* = 0 CFFF*n* = 1	Clear CFFF*n* bit by writing a 1 to the bit.
Result FIFO Overflow Interrupt [2]	RFOIE*n* = 1 RFOF*n* = 1	Clear RFOF*n* bit by writing a 1 to the bit.
Result FIFO Drain Interrupt	RFDE*n* = 1 RFDS*n* = 0 RFDF*n* = 1	Clear RFDF*n* bit by writing a 1 to the bit.

1 For details refer to Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn),” and Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn).”

2 Apart from generating an independent interrupt request for when a RFIFO overflow interrupt, a CFIFO underflow interrupt, and a CFIFO trigger overrun interrupt occurs, the eQADC also provides a combined interrupt request at which these requests from ALL CFIFOs are ORed. Refer to Figure 19-54 for details.

Table 19-55 describes a list of methods to generate eDMA requests by the eQADC.

Table 19-55. eQADC FIFO eDMA Summary[1]

eDMA Request	Condition	Clearing Mechanism
Result FIFO Drain eDMA Request	RFDE*n* = 1 RFDS*n* = 1 RFDF*n* = 1	The eQADC automatically clears the RFDF*n* when RFIFO*n* becomes empty. Writing 1 to the RFDF*n* bit is not allowed while RDFS = 1.
Command FIFO Fill eDMA Request	CFFE*n* = 1 CFFS*n* = 1 CFFF*n* = 1	The eQADC automatically clears the CFFF*n* when CFIFO*n* becomes full. Writing 1 to the CFFF*n* bit is not allowed while CFDS = 1.

1 For details refer to Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn),” and Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn).”

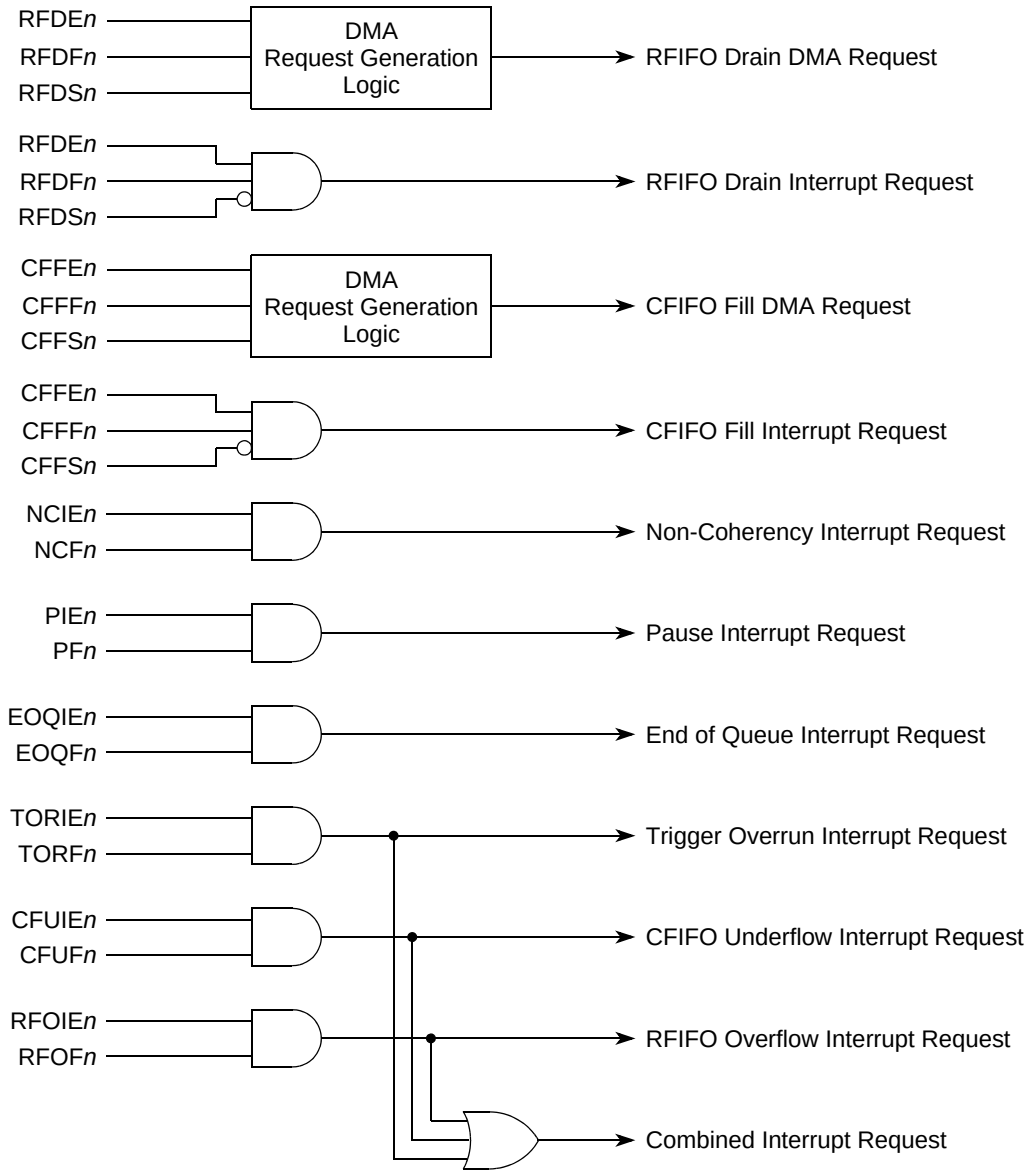


Figure 19-54. eQADC eDMA and Interrupt Requests

19.4.8 eQADC Synchronous Serial Interface (SSI) Submodule

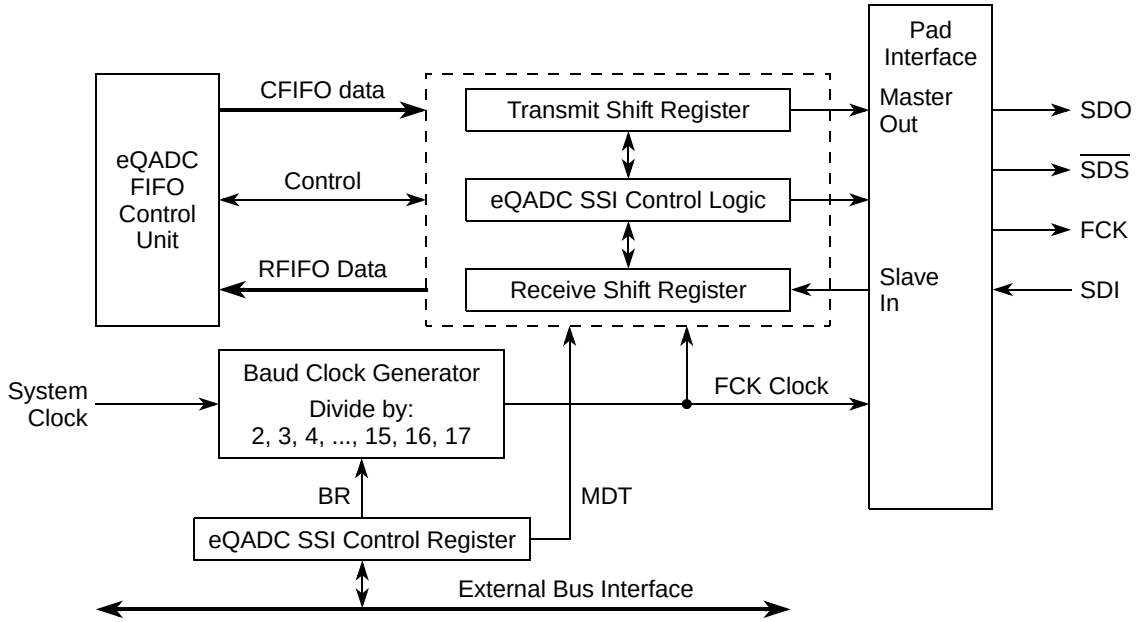


Figure 19-55. eQADC Synchronous Serial Interface Block Diagram

The eQADC SSI protocol allows for a full duplex, synchronous, serial communication between the eQADC and a single external device. Figure 19-55 shows the different components inside the eQADC SSI. The eQADC SSI submodule on the eQADC is always configured as a master. The eQADC SSI has four associated port pins:

- Free running clock (FCK)
- Serial data select ($\overline{\text{SDS}}$)
- Serial data in (SDI)
- Serial data out (SDO)

The FCK clock signal times the shifting and sampling of the two serial data signals and it is free running between transmissions, allowing it to be used as the clock for the external device. The $\overline{\text{SDS}}$ signal is asserted to indicate the start of a transmission, and negated to indicate the end or the abort of a transmission. SDI is the master serial data input and SDO the master serial data output.

The eQADC SSI submodule is enabled by setting the EQADC_MCR[ESSIE] (see Section 19.3.2.1, “eQADC Module Configuration Register (EQADC_MCR)”). When enabled, the eQADC SSI can be optionally capable of starting serial transmissions. When serial transmissions are disabled (ESSIE set to 0b10), no data is transmitted to the external device but FCK is free-running. This operation mode permits the control of the timing of the first serial transmission, and can be used to avoid the transmission of data to an unstable external device, for example, a device that is not fully reset. This mode of operation is specially important for the reset procedure of an external device that uses the FCK as its main clock.

The main elements of the eQADC SSI are the shift registers. The 26-bit transmit shift register in the master and 26-bit receive shift register in the slave are linked by the SDO pin. In a similar way, the 26-bit transmit shift register in the slave and 26-bit receive shift register in the master are linked by the SDI pin. Refer to

<xrefblue>Figure 19-56. When a data transmission operation is performed, data in the transmit registers is serially shifted twenty-six bit positions into the receive registers by the FCK clock from the master; data is exchanged between the master and the slave. Data in the master transmit shift register in the beginning of a transmission operation becomes the output data for the slave, and data in the master receive shift register after a transmission operation is the input data from the slave.

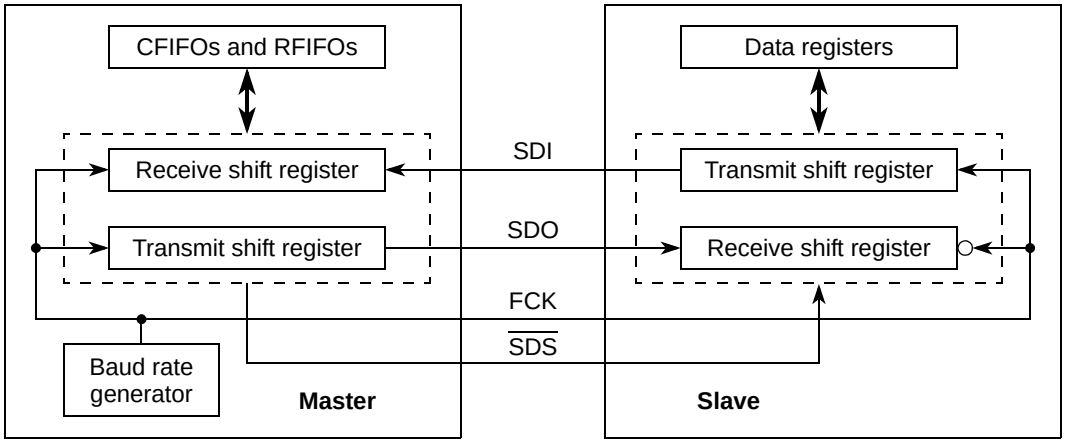


Figure 19-56. Full Duplex Pin Connection

19.4.8.1 eQADC SSI Data Transmission Protocol

Figure 19-57 shows the timing of an eQADC SSI transmission operation. The main characteristics of this protocol are the following:

- FCK is free running, it does not stop between data transmissions. FCK is driven low:
  - When the serial interface is disabled
  - In stop/debug mode
  - Immediately after reset
- Frame size is fixed to 26 bits.
- Msb bit is always transmitted first.
- Master drives data on the positive edge of FCK and latches incoming data on the next positive edge of FCK.
- Slave drives data on the positive edge of FCK and latches incoming data on the negative edge of FCK.

Master initiates a data transmission by driving $\overline{SDS}$ low, and its msb bit on SDO on the positive edge of FCK. After an asserted $\overline{SDS}$ is detected, the slave shifts its data out, one bit at a time, on every FCK positive edge. Both the master and the slave drive new data on the serial lines on every FCK positive edge. This process continues until all the initial 26-bits in the master shift register are moved into the slave shift register. t_{DT} is the delay between two consecutive serial transmissions, time during which $\overline{SDS}$ is negated. When ready to start of the next transmission, the slave must drive the msb bit of the message on every positive edge of FCK regardless of the state of the $\overline{SDS}$ signal. On the next positive edge, the second bit of the message is conditionally driven according to if an asserted $\overline{SDS}$ was detected by the slave on the preceding FCK negative edge. This is an important requisite since the $\overline{SDS}$ and the FCK are not

synchronous. The $\overline{SDS}$ signal is not generated by FCK, rather both are generated by the system clock, so that it is not guaranteed that FCK edges precede $\overline{SDS}$ edges. While $\overline{SDS}$ is negated, the slave continuously drives its msb bit on every positive edge of FCK until it detects an asserted $\overline{SDS}$ on the immediately next FCK negative edge. Refer to Figure 19-58 for three cases that show how the slave operates when $\overline{SDS}$ is asserted.

NOTE

On the master, the FCK is not used as a clock. Although, the eQADC SSI behavior is described in terms of the FCK positive and negative edges, all eQADC SSI related signals (SDI, SDS, SDO, and FCK) are synchronized by the system clock on the master side. There are no restrictions regarding the use of the FCK as a clock on the slave device.

19.4.8.1.1 Abort Feature

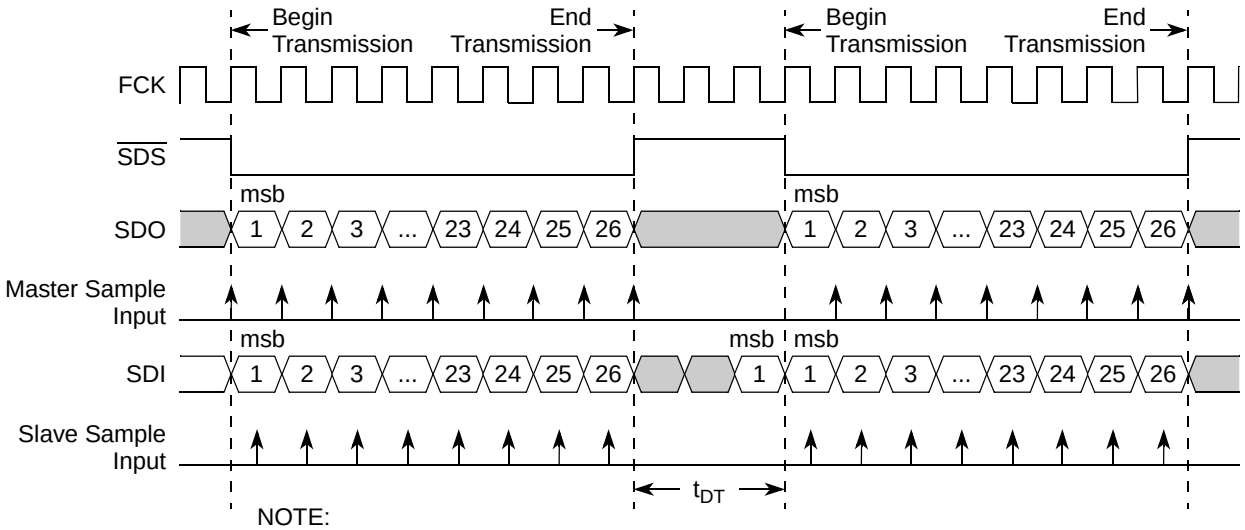
The master indicates it is aborting the current transfer by negating $\overline{SDS}$ before the whole data frame has being shifted out, that is the 26th bit of data being transferred has not being shifted out. The eQADC ignores the incompletely received message. The eQADC re-sends the aborted message whenever the corresponding CFIFO becomes again the highest priority CFIFO with commands bound for an external command buffer that is not full. Refer to Section 19.4.3.2, “CFIFO Prioritization and Command Transfer,” for more information on aborts and CFIFO priority.

19.4.8.2 Baud Clock Generation

As shown in Figure 19-55, the baud clock generator divides the system clock to produce the baud clock. The EQADC_SSICR[BR] field (see Section 19.3.2.12, “eQADC SSI Control Register (EQADC_SSICR)”) selects the system clock divide factor as in Table 19-21. [1]

$$\text{BaudClockFrequency} = \frac{\text{SystemClockFrequency(MHz)}}{\text{SystemClockDivideFactor}}$$

1. Maximum FCK frequency is highly dependable on track delays, master pad delays, and slave pad delays.



NOTE:
t_{MDT} = Minimum t_{DT} is programmable and defined in Section 18.3.2.12, 'eQADC SSI Control Register (EQADC_SSICR).'

Figure 19-57. Synchronous Serial Interface Protocol Timing

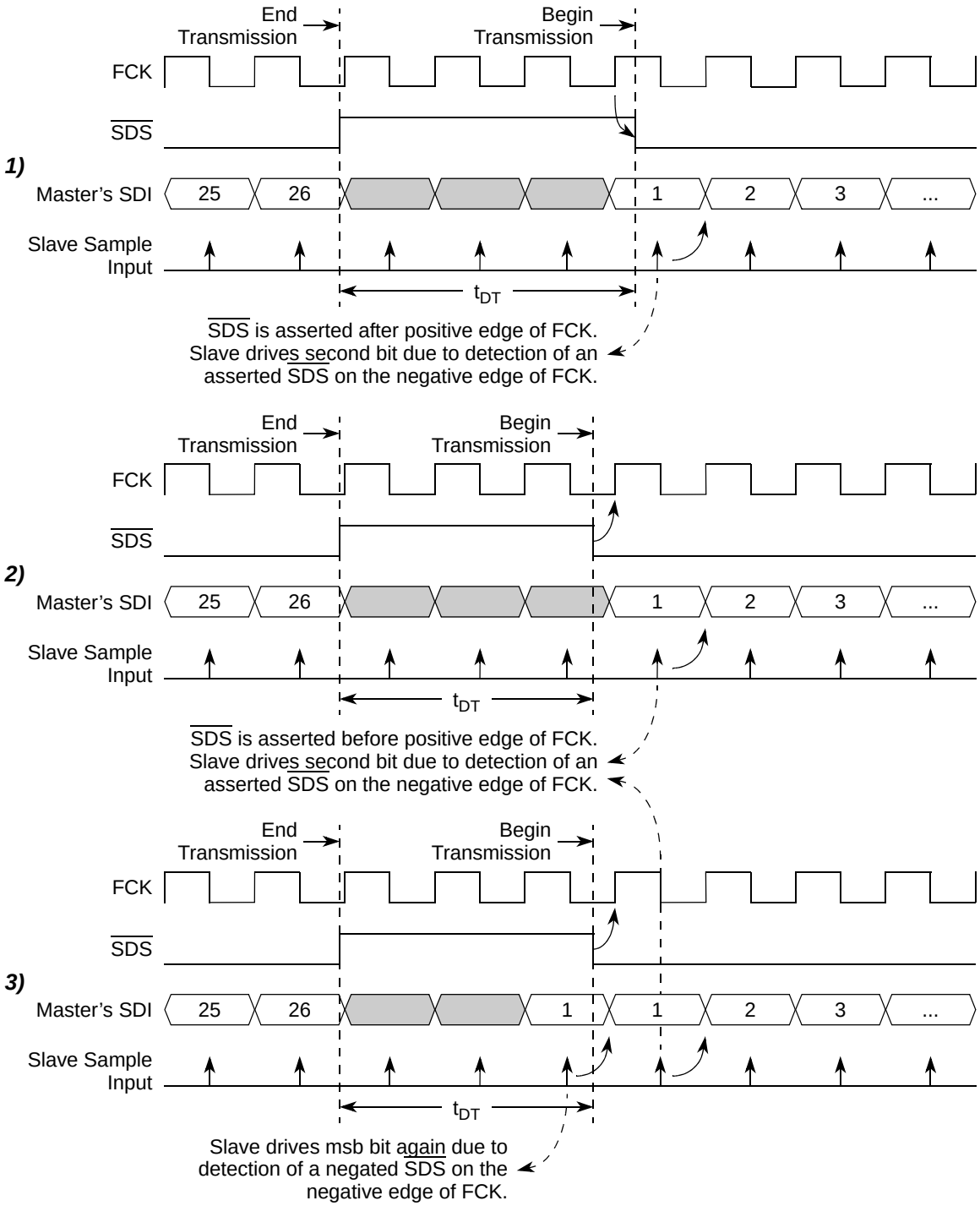


Figure 19-58. Slave Driving the msb and Consecutive Bits in a Data Transmission

19.4.9 Analog Submodule

19.4.9.1 Reference Bypass

The reference bypass capacitor (REFBYPC) signal requires a 100 nF capacitor connected to V_{RL} to filter noise on the internal reference used by the ADC.

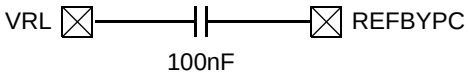


Figure 19-59. Reference Bypass Circuit

19.4.9.2 Analog-to-Digital Converter (ADC)

19.4.9.2.1 ADC Architecture

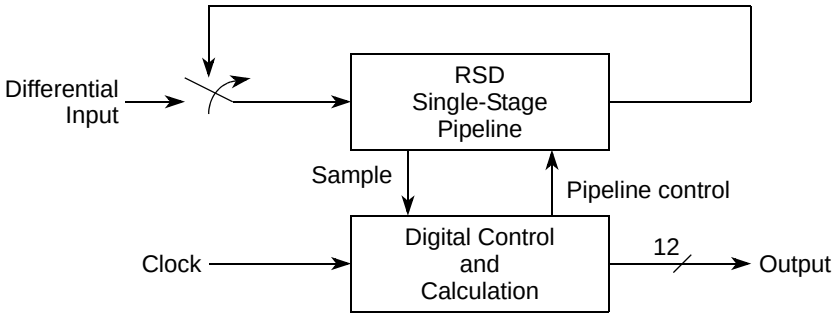


Figure 19-60. RSD ADC Block Diagram

The redundant signed digit (RSD) cyclic ADC consists of two main portions, the analog RSD stage, and the digital control and calculation module, as shown in Figure 19-60. To begin an analog-to-digital conversion, a differential input is passed into the analog RSD stage. The signal is passed through the RSD stage, and then from the RSD stage output, back to its input to be passed again. To complete a 12-bit conversion, the signal must pass through the RSD stage 12 times. Each time an input signal is read into the RSD stage, a digital sample is taken by the digital control/calculation module. The digital control/calculation module uses this sample to tell the analog module how to condition the signal. The digital module also saves each successive sample and adds them according to the RSD algorithm at the end of the entire conversion cycle.

19.4.9.2.2 RSD Overview

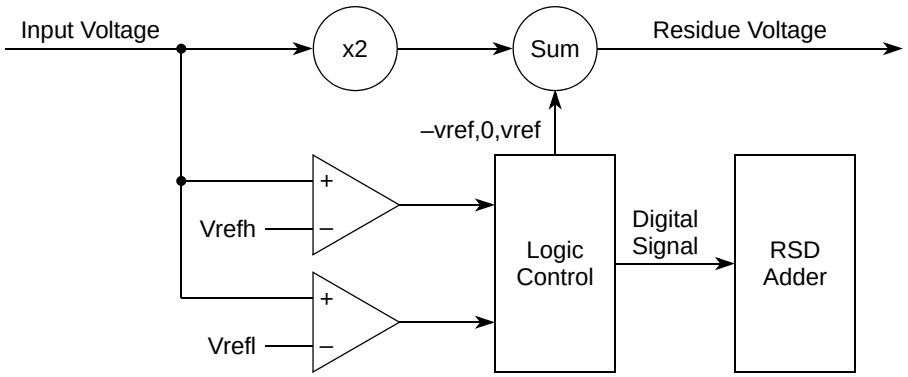


Figure 19-61. RSD Stage Block Diagram

On each pass through the RSD stage, the input signal are multiplied by exactly two, and summed with either –vref, 0, or vref, depending on the logic control. The logic control determines –vref, 0, or vref, depending on the two comparator inputs. As the logic control sets the summing operation, it also sends a digital value to the RSD adder. Each time an analog signal passes through the RSD single-stage, a digital value is collected by the RSD adder. At the end of an entire AD conversion cycle, the RSD adder uses these collected values to calculate the 12-bit digital output.

Figure 19-62 shows the transfer function for the RSD stage. Note how the digital value (AB) is dependent on the two comparator inputs.

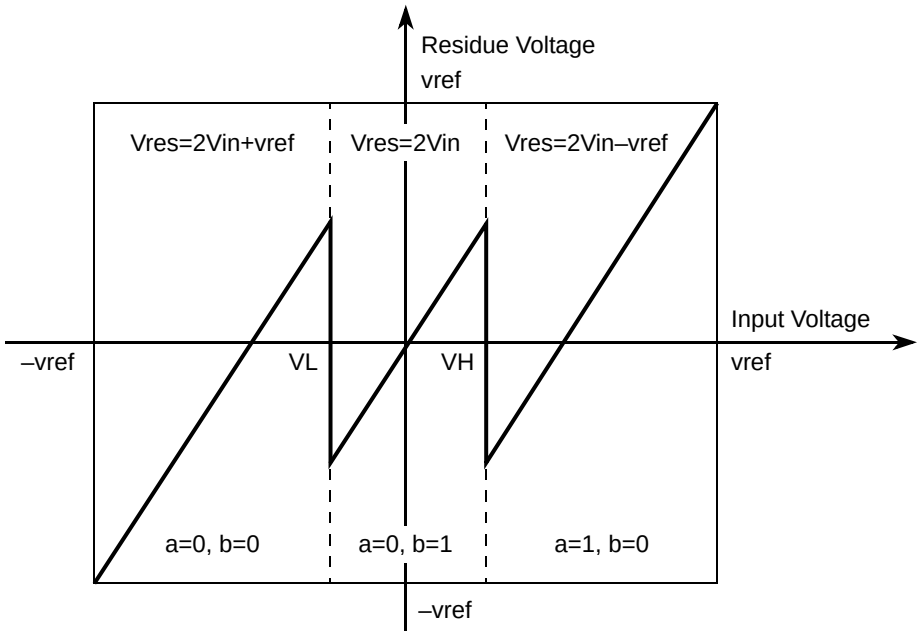


Figure 19-62. RSD Stage Transfer Function

In each pass through the RSD stage, the remainder is sent back as the new input, and the digital signals, a and b, are stored. For the 12-bit ADC, the input signal is sampled during the input phase, and after each of the 12 passes through the RSD stage. Thus, 13 total a and b values are collected. Upon collecting all these

values, they are added according to the RSD algorithm to create the 12-bit digital representation of the original analog input. The bits are added in the following manner:

19.4.9.2.3 RSD Adder

The array, s1 to s12, are the digital output of the RSD ADC with s1 being the MSB (most significant bit) and s12 being the LSB (least significant bit).

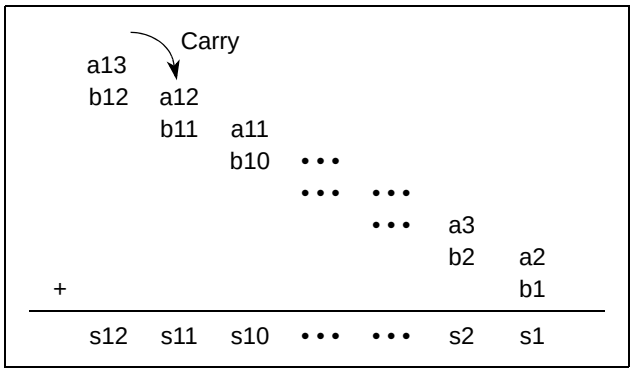


Figure 19-63. RSD Adder

19.5 Initialization and Application Information

19.5.1 Multiple Queues Control Setup Example

This section provides an example of how to configure multiple user command queues. Table 19-56 describes how each queue can be used for a different application. Also documented in this section are general guidelines on how to initialize the on-chip ADCs and the external device, and how to configure the command queues and the eQADC.

Table 19-56. Example Applications of Each Command Queue

Command Queue Number	Queue Type	Running Speed	Number of Contiguous Conversions	Example
0	Very fast burst time-based queue	Every 2 μs for 200 μs; pause for 300 μs and then repeat	2	Injector current profiling
1	Fast hardware-triggered queue	Every 900 μs	3	Current sensing of PWM controlled actuators
2	Fast repetitive time-based queue	Every 2 ms	8	Throttle position
3	Software-triggered queue	Every 3.9 ms	3	Command triggered by software strategy

Table 19-56. Example Applications of Each Command Queue (continued)

Command Queue Number	Queue Type	Running Speed	Number of Contiguous Conversions	Example
4	Repetitive angle-based queue	Every 625 µs	7	Airflow read every 30 degrees at 8000 RPM
5	Slow repetitive time-based queue	Every 100 ms	10	Temperature sensors

19.5.1.1 Initialization of On-Chip ADCs and an External Device

The following steps provide an example of configuring the eQADC to initialize the on-chip ADCs and the external device. In this example, commands are sent through CFIFO0.

1. Load all required configuration commands in the RAM in such way that they form a queue; this data structure is referred to below as Queue0. Figure 19-64 shows an example of a command queue able to configure the on-chip ADCs and external device at the same time.
2. Configure Section 19.3.2.2, "eQADC Null Message Send Format Register (EQADC_NMSFR)."
3. Configure Section 19.3.2.12, "eQADC SSI Control Register (EQADC_SSICR)," to communicate with the external device.
4. Enable the eQADC SSI by programming the ESSIE field the Section 19.3.2.1, "eQADC Module Configuration Register (EQADC_MCR)."
   a) Write 0b10 to ESSIE field to enable the eQADC SSI. FCK is free running but serial transmissions are not started.
   b) Wait until the external device becomes stable after reset.
   c) Write 0b11 to ESSIE field to enable the eQADC SSI to start serial transmissions.
5. Configure the eDMA to transfer data from Queue0 to CFIFO0 in the eQADC.
6. Configure Section 19.3.2.7, "eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn)."
   a) Set CFFS0 to configure the eQADC to generate an eDMA request to load commands from Queue0 to the CFIFO0.
   b) Set CFFE0 to enable the eQADC to generate an eDMA request to transfer commands from Queue0 to CFIFO0; Command transfers from the RAM to the CFIFO0 starts immediately.
   c) Set EOQIE0 to enable the eQADC to generate an interrupt after transferring all of the commands of Queue0 through CFIFO0.
7. Configure Section 19.3.2.6, "eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)."
   a) Write 0b0001 to the MODE0 field in eQADC_CFCR0 to program CFIFO0 for software single-scan mode.
   b) Write 1 to SSE0 to assert SSS0 and trigger CFIFO0.
8. Because CFIFO0 is in single-scan software mode and it is also the highest priority CFIFO, the eQADC starts to transfer configuration commands to the on-chip ADCs and to the external device.

9. When all of the configuration commands are transferred, EQADC_FISR*n*[CF0] is set. Refer to Section 19.3.2.8, "eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)." The eQADC generates an end of queue interrupt. The initialization procedure is complete.

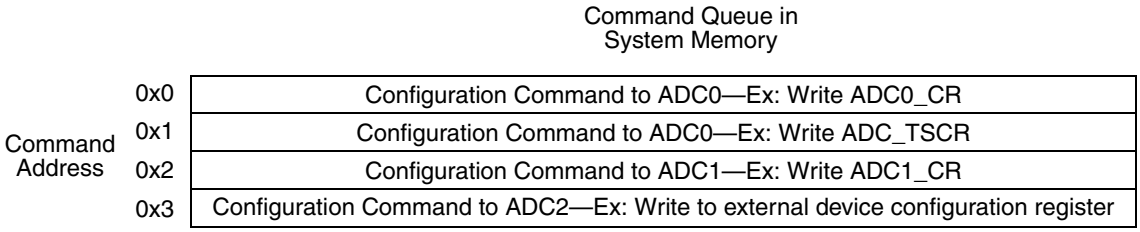


Figure 19-64. Example of a Command Queue Configuring the On-Chip ADCs/External Device

19.5.1.2 Configuring eQADC for Applications

This section provides an example based on the applications in Table 19-56. The example describes how to configure multiple command queues to be used for those applications and provides a step-by-step procedure to configure the eQADC and the associated command queue structures. In the example, the "Fast hardware-triggered command queue," described on the second row of Table 19-56, transfer its commands to ADC1; the conversion commands are executed by ADC1. The generated results are returned to RFIFO3 before being transferred to the result queues in the RAM by the eDMA.

NOTE

There is no fixed relationship between CFIFOs and RFIFOs with the same number. The results of commands being transferred through CFIFO1 can be returned to any RFIFO, regardless of its number. The destination of a result is determined by the MESSAGE_TAG field of the command that requested the result. Refer to Section 19.4.1.2, "Message Format in eQADC," for details.

Step One: Set up the command queues and result queues.

1. Load the RAM with configuration and conversion commands. Table 19-57 is an example of how to set commands for command queue 1 .
   a) Each trigger event causes four commands to be executed. When the eQADC detects the pause bit asserted, it waits for another trigger to restart transferring commands from the CFIFO.
   b) At the end of the command queue, the "EOQ" bit is asserted as shown in Table 19-57.
   c) Results are returned to RFIFO3 as specified in the MESSAGE_TAG field of commands.
2. Reserve memory space for storing results.

Table 19-57. Example of Command Queue Commands[1]

	0	1	2 3	4	5	6	7	8 9 10 11	12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
	EOQ	PAUSE	RESERVED	ABORT_ST	EB (0b1)	BN	CAL	MESSAGE_TAG	ADC COMMAND
CMD1	0	0	0	0	0	1	0	0b0011	Conversion command
CMD2	0	0	0	0	0	1	0	0b0011	Conversion command
CMD3	0	0	0	0	0	1	0	0b0011	Conversion command
CMD4	0	1	0	0	0	1	0	0b0011 [2]	Configure peripheral device for next conversion sequence
CMD5	0	0	0	0	0	1	0	0b0011	Conversion command
CMD6	0	0	0	0	0	1	0	0b0011	Conversion command
CMD7	0	0	0	0	0	1	0	0b0011	Conversion command
CMD8	0	1	0	0	0	1	0	0b0011[2]	Configure peripheral device for next conversion sequence
≈								etc.....	≈
CMDEOQ	1	0	0	0	0	1	0	0b0011	EOQ message
	CFIFO header								ADC command

[1] Fields LST, TSR, FMT, and CHANNEL_NUMBER are not shown for clarity. Refer to Section , “Conversion Command Message Format for On-Chip ADC Operation,” for details.

[2] MESSAGE_TAG field is only defined for read configuration commands.

Step Two: Configure the eDMA to handle data transfers between the command/result queues in RAM and the CFIFOs/RFIFOs in the eQADC.

1. For transferring, set the source address of the eDMA TCD*n* to point to the start address of command queue 1. Set the destination address of the eDMA to point to EQADC_CFPR1. Refer to Section 19.3.2.4, “eQADC CFIFO Push Registers 0–5 (EQADC_CFPRn).”
2. For receiving, set the source address of the eDMA TCD*n* to point to EQADC_RFPR3. Refer to Section 19.3.2.5, “eQADC Result FIFO Pop Registers 0–5 (EQADC_RFPRn).” Set the destination address of the eDMA to point to the starting address of result queue 1.

Step Three: Configure the eQADC control registers.

1. Configure Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn).”
   a) Set EOQIE1 to enable the End of Queue Interrupt request.
   b) Set CFFS1 and RFDS3 to configure the eQADC to generate eDMA requests to push commands into CFIFO1 and to pop result data from RFIF03.
   c) Set CFINV1 to invalidate the contents of CFIFO1.
   d) Set RFDE3 and CFFE1 to enable the eQADC to generate eDMA requests. Command transfers from the RAM to the CFIFO1 starts immediately.
   e) Set RFOIE3 to indicate if RFIFO3 overflows.
   f) Set CFUIE1 to indicate if CFIFO1 underflows.
2. Configure MODE1 to continuous-scan rising edge external trigger mode in Section 19.3.2.6, “eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn).”

Step Four: Command transfer to ADCs and result data reception.

When an external rising edge event occurs for CFIFO1, the eQADC automatically begins transferring commands from CFIFO1 when it becomes the highest priority CFIFO trying to send commands to ADC1. The received results are placed in RFIFO3 and then moved to result queue 1 by the eDMA.

19.5.2 eQADC/eDMA Controller Interface

This section provides an overview of the eQADC/eDMA interface and general guidelines about how to cinfugre the eDMA to correctly transfer data between the queues in system memory and the eQADC FIFOs.

19.5.2.1 Command Queue/CFIFO Transfers

In transfers involving command queues and CFIFOs, the eDMA moves data from a queued source to a single destination as shown in Figure 19-65.

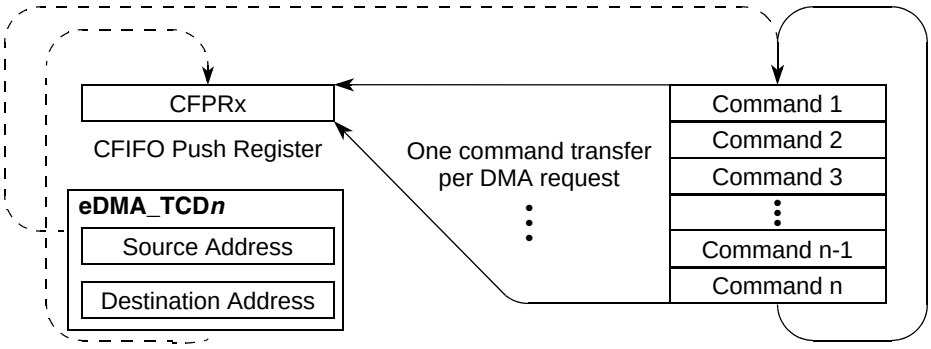


Figure 19-65. Command Queue/CFIFO Interface

The location of the data to be moved is indicated by the source address, and the final destination for that data, by the destination address. The eDMA has transfer control descriptors (TCDs) containing these addresses and other parameters used in the control of data transfers.

Refer to Section 9.2.2.17, “Transfer Control Descriptor (TCD)” for more information.

For every eDMA request issued by the eQADC, the eDMA must be configured to transfer a single command (32-bit data) from the command queue, pointed to by the source address, to the CFIFO push register, pointed to by the destination address. After the service of an eDMA request is completed, the source address has to be updated to point to the next valid command. The destination address remains unchanged. When the last command of a queue is transferred, do one of the following:

- Disable the eDMA channel. This might be desirable for CFIFOs in single scan mode.
- Update the source address to point to a valid command for the first command in the queue was transferred (cyclic queue), or the first command of any other command queue. This is desirable for CFIFOs in continuous scan mode, or in some cases, for CFIFOs in single-scan mode.

Refer to Chapter 9, “Enhanced Direct Memory Access (eDMA)” for details about how this functionality is supported.

19.5.2.2 Receive Queue/RFIFO Transfers

In transfers involving receive queues and RFIFOs, the eDMA controller moves data from a single source to a queue destination as shown in Figure 19-66. The location of the data to be moved is indicated by the source address, and the final destination for that data, by the destination address. For every eDMA request issued by the EQADC, the eDMA controller has to be configured to transfer a single result (16-bit data), pointed to by the source address, from the RFIFO pop register to the receive queue, pointed to by the destination address. After the service of an eDMA request is completed, the destination address has to be updated to point to the location where the next 16-bit result are stored. The source address remains unchanged. When the last expected result is written to the receive queue, do one of the following:

- Disable the eDMA channel.
- Update the destination address to point to the next location where in-coming results are stored: the first entry of the current receive queue (cyclic queue); or the beginning of a new receive queue.

Refer to Chapter 9, “Enhanced Direct Memory Access (eDMA)” for details about how this functionality is supported.

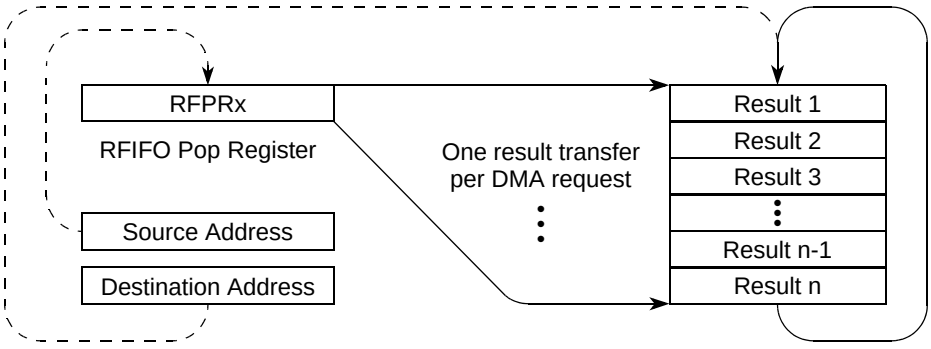


Figure 19-66. Receive Queue/RFIFO Interface

19.5.3 Sending Immediate Command Setup Example

In the eQADC, there is no immediate command register for sending a command immediately after writing to that register. However, a CFIFO can be configured to perform the same function as an immediate command register. The following steps illustrate how to configure CFIFO5 as an immediate command CFIFO. This eliminates the use of the eDMA. The results are returned to RFIFO5.

1. Configure the Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn).”
   a) Clear CFIFO fill enable5 (CFFE5 = 0) in EQADC_IDCR5.
   b) Clear CFIFO underflow interrupt enable5 (CFUIE5 = 0) in EQADC_IDCR2.
   c) Clear RFDS5 to configure the eQADC to generate interrupt requests to pop result data from RFIF05.
   d) Set RFIFO drain enable5 (RFDE5 = 1) in EQADC_IDCR5.
2. Configure the Section 19.3.2.6, “eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn).”
   a) Write 1 to CFINV5 in EQADC_CFCR5. This invalidates the contents of CFIFO5.
   a) Set MODE5 to continuous-scan software trigger mode in EQADC_CFCR5.
3. To transfer a command, write it to the eQADC CFIFO push register 5 (EQADC_CFPR5) with message tag = 0b0101. Refer to Section 19.3.2.4, “eQADC CFIFO Push Registers 0–5 (EQADC_CFPRn).”
4. Up to 4 commands can be queued in CFIFO5. Check the CFCTR5 status in EQADC_FISR5 before pushing another command to avoid overflowing the CFIFO. Refer to Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn).”
5. When the eQADC receives a conversion result for RFIFO5, it generates an interrupt request. RFIFO pop register 5 (EQADC_RFPR5) can be popped to read the result. Refer to Section 19.3.2.5, “eQADC Result FIFO Pop Registers 0–5 (EQADC_RFPRn).”

19.5.4 Modifying Queues

More command queues may be needed than the six supported by the eQADC. These additional command queues can be supported by interrupting command transfers from a configured CFIFO, even if it is triggered and transferring, modifying the corresponding command queue in the RAM or associating another command queue to it, and restarting the CFIFO. More details on disabling a CFIFO are described in Section 19.4.3.5.1, “Disabled Mode.”

1. Determine the resumption conditions when later resuming the scan of the command queue at the point before it was modified.
   a) Change EQADC_CFCRn[MODE*n*] (see Section 19.3.2.6, “eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)”) to disabled. Refer to Section 19.4.3.5.1, “Disabled Mode,” for a description of what happens when MODE*n* is changed to disabled.
   b) Poll EQADC_CFSR[CFS*n*] until it becomes IDLE (see Section 19.3.2.11, “eQADC CFIFO Status Register (EQADC_CFSR)”).

c) Read and save EQADC_CFTCRn[TC_CF*n*] (see Section 19.3.2.9, “eQADC CFIFO Transfer Counter Registers 0–5 (EQADC_CFTCRn)”) for later resuming the scan of the queue. The TC_CF*n* provides the point of resumption.

d) Since all result data may not have being stored in the appropriate RFIFO at the time MODE*n* is changed to disable, wait for all expected results to be stored in the RFIFO/result queue before reconfiguring the eDMA to work with the modified result queue. The number of results that must return can be estimated from the TC_CF*n* value obtained above.

2. Disable the eDMA from responding to the eDMA request generated by EQADC_FISRn[CFFF*n*] and EQADC_FISRn[RFDF*n*] (see Section 19.3.2.8, “eQADC FIFO and Interrupt Status Registers 0–5 (EQADC_FISRn)”).
3. Write “0x0000” to the TC_CF*n* field.
4. Load the new configuration and conversion commands into RAM. Configure the eDMA to support the new command/result queue, but do not configure it yet to respond to eDMA requests from CFIFO*n*/RFIFO*n*.
5. If necessary, modify the EQADC_IDCRn registers (see Section 19.3.2.7, “eQADC Interrupt and eDMA Control Registers 0–5 (EQADC_IDCRn)”) to suit the modified command queue.
6. Write 1 to EQADC_CFCRn[CFINV*n*] (see Section 19.3.2.6, “eQADC CFIFO Control Registers 0–5 (EQADC_CFCRn)”) to invalidate the entries of CFIFO*n*.
7. Configure the eDMA to respond to eDMA requests generated by CFFF*n* and RFDF*n*.
8. Change MODE*n* to the modified CFIFO operation mode. Write 1 to SSE*n* to trigger CFIFO*n* if MODE*n* is software trigger.

19.5.5 Command Queue and Result Queue Usage

Figure 19-67 is an example of command queue and result queue usage. It shows the command queue 0 commands requesting results that are stored in result queue 0 and result queue 1, and command queue 1 commands requesting results that are stored only in result queue 1. Some command messages request data to be returned from the on-chip ADC/external device, but some only configure them and do not request returning data. When a command queue contains both write and read commands like command queue 0, the command queue and result queue entries are not aligned, in Figure 19-67, the result for the second command of command queue 0 is the first entry of result queue 0. The figure also shows that command queue and result queue entries can also become unaligned even if all commands in a command queue request data as command queue 1. Command queue 1 entries became unaligned to result queue 1 entries because a result requested by the forth command queue 0 command was sent to result queue 1. This happens because the system can be configured so that several command queues can have results sent to a single result queue.

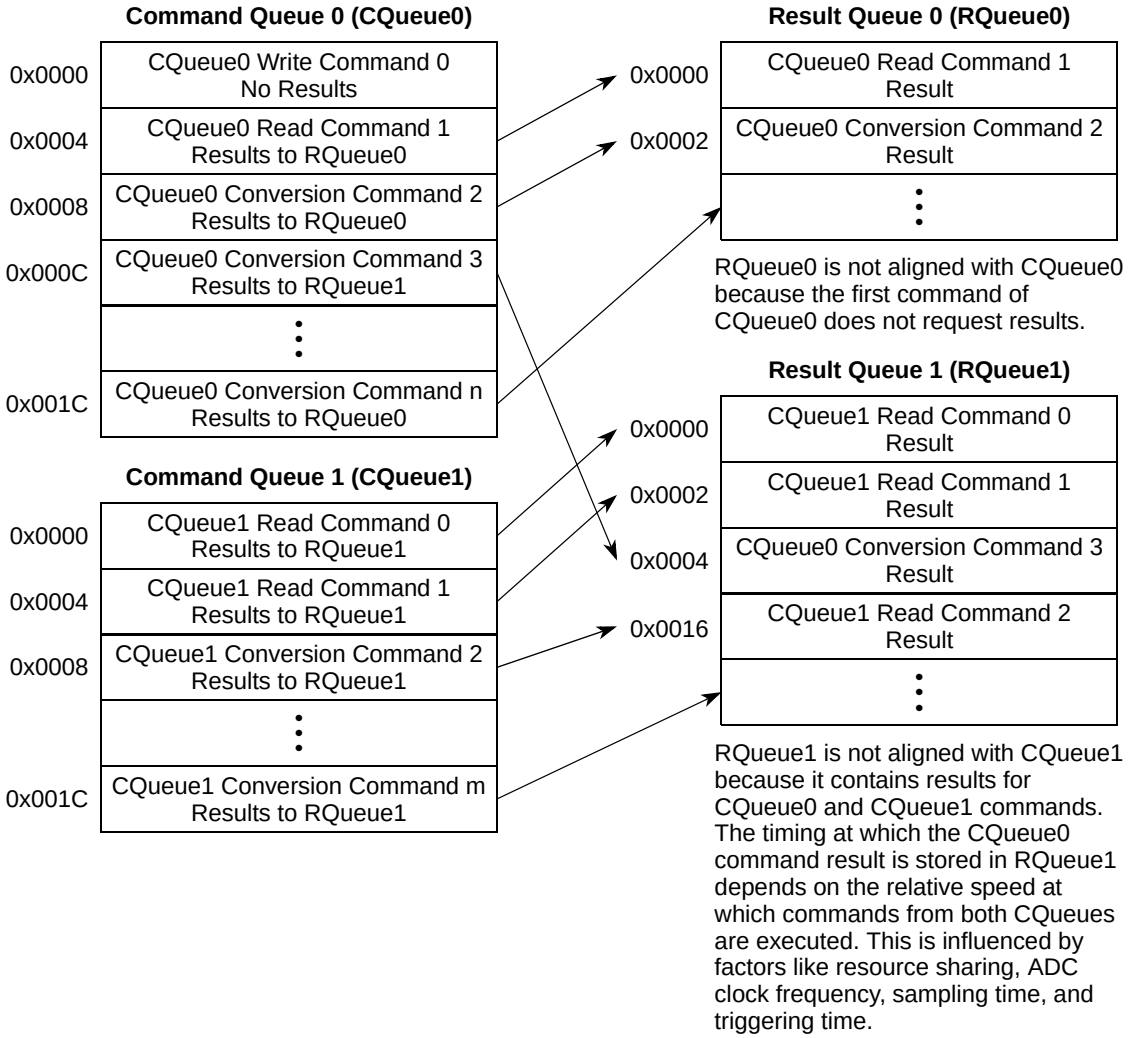


Figure 19-67. eQADC Command and Result Queues

19.5.6 ADC Result Calibration

The ADC result calibration process consists of two steps: determining the gain and offset calibration constants, and calibrating the raw results generated by the on-chip ADCs by solving the following equation discussed in Section 19.4.5.4.1, "Calibration Overview."

$$CAL\_RES = GCC \times RAW\_RES + OCC + 2; \qquad \textit{Eqn. 19-1}$$

The calibration constants GCC and OCC can be calculated from Equation 19-1 provided that two pairs of expected (CAL_RES) and measured (RAW_RES) result values are available for two different input voltages. Most likely calibration points to be used are 25% V_{REF}[1] and 75% V_{REF} since they are far apart but not too close to the end points of the full input voltage range. This allows for calculations of more representative calibration constants. The eQADC provides these voltages via channel numbers 43 and 44.

1. $V_{REF} = V_{RH} - V_{RL}$

The raw, uncalibrated results for these input voltages are obtained by converting these channels with conversion commands that have the CAL bit negated.

The transfer equations for when sampling these reference voltages are:

$$CAL\_RES_{75\%VREF} = GCC \times RAW\_RES_{75\%VREF} + OCC + 2; \quad \textit{Eqn. 19-2}$$

$$CAL\_RES_{25\%VREF} = GCC \times RAW\_RES_{25\%VREF} + OCC + 2; \quad \textit{Eqn. 19-3}$$

Thus;

$$GCC = (CAL\_RES_{75\%VREF} - CAL\_RES_{25\%VREF}) / (RAW\_RES_{75\%VREF} - RAW\_RES_{25\%VREF}); \quad \textit{Eqn. 19-4}$$

$$OCC = CAL\_RES_{75\%VREF} - GCC \times RAW\_RES_{75\%VREF} - 2; \quad \textit{Eqn. 19-5}$$

or

$$OCC = CAL\_RES_{25\%VREF} - GCC \times RAW\_RES_{25\%VREF} - 2; \quad \textit{Eqn. 19-6}$$

After being calculated, the GCC and OCC values must be written to ADC0_GCCR and ADC1_GCCR registers (see Section 19.3.3.4, “ADCn Gain Calibration Constant Registers (ADC0_GCCR and ADC1_GCCR)”) and the ADC0_OCCR and ADC1_OCCR registers (see Section 19.3.3.5, “ADCn Offset Calibration Constant Registers (ADC0_OCCR and ADC1_OCCR)”) using write configuration commands.

The eQADC automatically calibrates the results, according to Equation 19-1, of every conversion command that has its CAL bit asserted using the GCC and OCC values stored in the ADC calibration registers.

19.5.6.1 MAC Configuration Procedure

The following steps illustrate how to configure the calibration hardware, that is, determining the values of the gain and offset calibration constants, and the writing these constants to the calibration registers. This procedure should be performed for both ADC0 and ADC1.

1. Convert channel 44 with a command that has its CAL bit negated and obtain the raw, uncalibrated result for 25% V_{REF} ($RAW\_RES_{25\%VREF}$).
2. Convert channel 43 with a command that has its CAL bit negated and obtain the raw, uncalibrated result for 75% V_{REF} ($RAW\_RES_{75\%VREF}$).
3. Because the expected values for the conversion of these voltages are known ($CAL\_RES_{25\%VREF}$ and $CAL\_RES_{75\%VREF}$), GCC and OCC values can be calculated from Equation 19-4 and Equation 19-5 using these values, and the results determined in steps 1 and 2.
4. Reformat GCC and OCC to the proper data formats as specified in Section 19.4.5.4.2, “MAC Unit and Operand Data Format.” GCC is an unsigned 15-bit fixed point value and OCC is a signed 14-bit value.

5. Write the GCC value to ADCn gain calibration registers (see Section Section 19.3.3.4, “ADCn Gain Calibration Constant Registers (ADC0_GCCR and ADC1_GCCR)”) and the OCC value to ADCn offset calibration constant registers (see Section Section 19.3.3.5, “ADCn Offset Calibration Constant Registers (ADC0_OCCR and ADC1_OCCR)”) using write configuration commands.

19.5.6.2 Example Calculation of Calibration Constants

The raw results obtained when sampling reference voltages 25% V_{REF} and 75% V_{REF} were, respectively, 3798 and 11592. The results that should have been obtained from the conversion of these reference voltages are, respectively, 4096 and 12288. Therefore, using Equation 19-4 and Equation 19-5, the gain and offset calibration constants are:

```
GCC=(12288-4096)÷(11592-3798) = 1.05106492-> 1.05102539[1] = 0x4344
    OCC=12288-1.05106492*11592 -2 = 102.06-> 102 = 0x0066
```

Table 19-58 shows, for this particular case, examples of how the result values change according to GCC and OCC when result calibration is executed (CAL=1) and when it is not (CAL=0).

Table 19-58. Calibration Example

Input Voltage	Raw result (CAL=0)		Calibrated result (CAL=1)	
	Hexadecimal	Decimal	Hexadecimal	Decimal
25% VREF	0x0ED6	3798	0x1000	4095.794
75% VREF	0x2D48	11592	0x3000	12287.486

19.5.6.3 Quantization Error Reduction During Calibration

Figure 19-68 shows how the ADC transfer curve changes due to the addition of two to the MAC output during the calibration. See MAC output equation in Section 19.4.5.4, “ADC Calibration Feature**.”** The maximum absolute quantization error is reduced by half leading to an increase in accuracy.

1. This calculation is rounded down due to binary approximation.

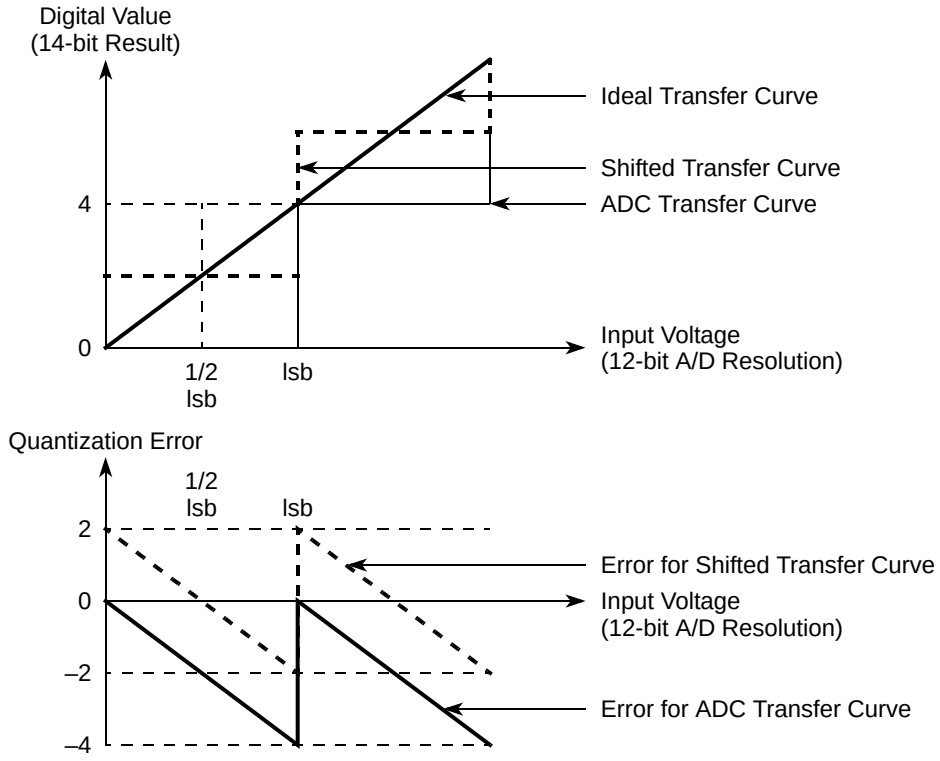


Figure 19-68. Quantization Error Reduction During Calibration

19.5.7 eQADC versus QADC

This section describes how the eQADC upgrades the QADC functionality. The section also provides a comparison between the eQADC and QADC in terms of their functionality. You must be familiar with QADC terminology to fully comprehend the following sections.

Figure 19-69 is an overview of a QADC.

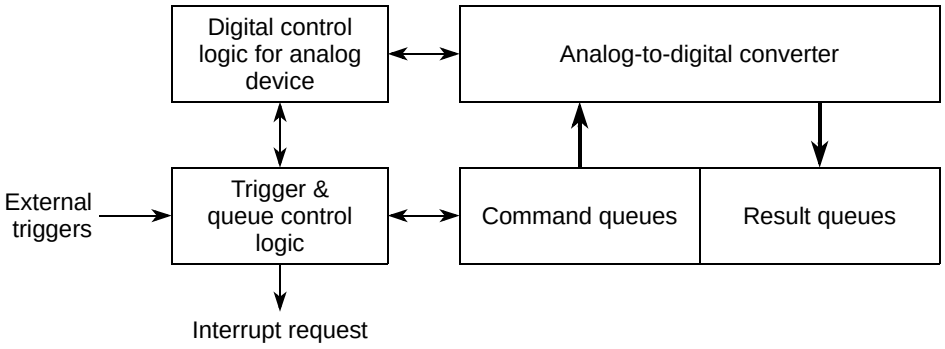


Figure 19-69. QADC Overview

Figure 19-70 is an overview of the eQADC system.

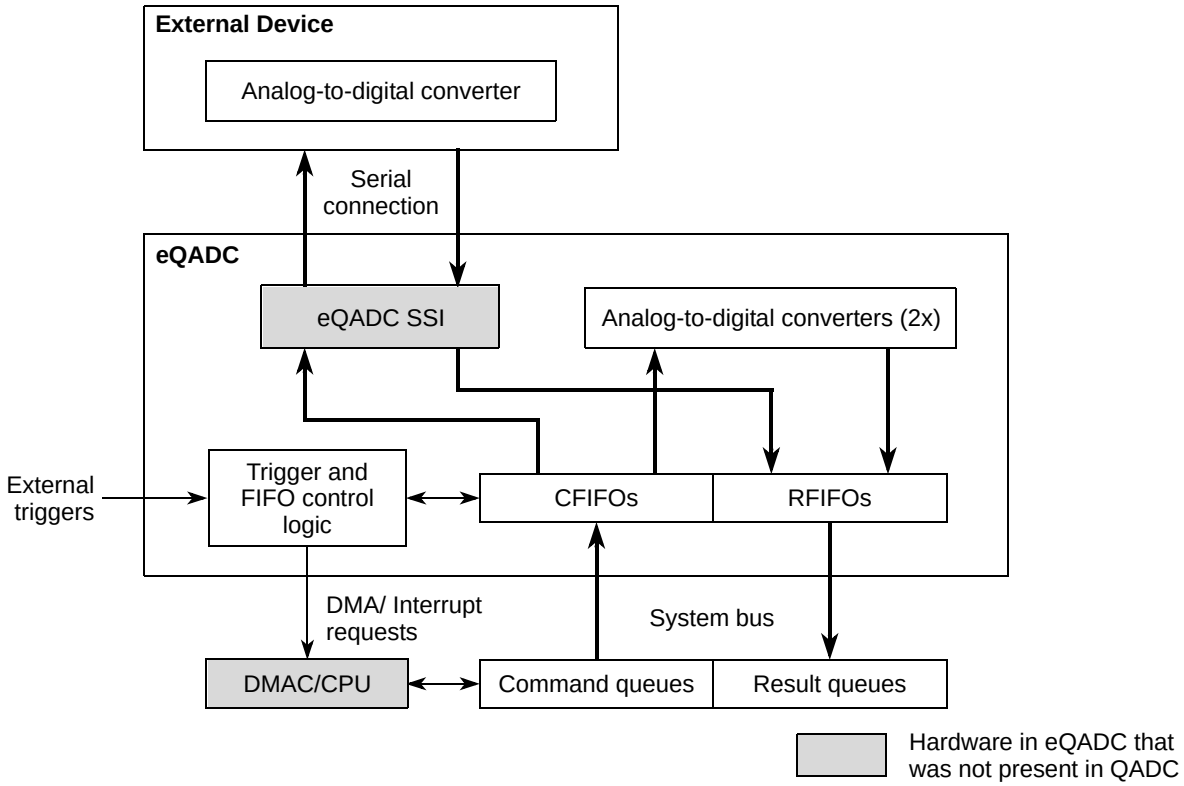


Figure 19-70. eQADC System Overview

The eQADC system consists of four parts: queues in system memory, the eQADC, on-chip ADCs, and an external device. As compared with the QADC, the eQADC system requires two pieces of extra hardware.

1. An eDMA or an MCU is required to move data between the eQADC's FIFOs and queues in the system memory.
2. A serial interface [eQADC synchronous serial interface (SSI)] is implemented to transmit and receive data between the eQADC and the external device.

Because there are only FIFOs inside the eQADC, much of the terminology or use of the register names, register contents, and signals of the eQADC involve FIFO instead of queue. These register names, register contents, and signals are functionally equivalent to the queue counterparts in the QADC. Table 19-59 lists how the eQADC register, register contents, and signals are related to QADC.

Table 19-59. Terminology Comparison between QADC and eQADC

QADC Terminology	eQADC Terminology	Function
CCW	Command Message	In the QADC, the hardware only executes conversion command words. In the eQADC, not all commands are conversion commands; some are configuration commands.
Queue Trigger	CFIFO Trigger	In the QADC, a trigger event is required to start the execution of a queue. In the eQADC, a trigger event is required to start command transfers from a CFIFO. When a CFIFO is triggered and transferring, commands are continuously moved from command queues to CFIFOs. Thus, the trigger event initiates the “execution of a queue” indirectly.
Command Word Pointer Queue *n* (CWPQ*n*)	Counter Value of Commands Transferred from Command FIFO*n* (TC_CF*n*)	In the QADC, CWPQ*n* allows the last executed command on queue *n* to be determined. In the eQADC, the TC_CF*n* value allows the last transferred command on command queue *n* to be determined.
Queue Pause Bit (P)	CFIFO Pause Bit	In the QADC, detecting a pause bit in the CCW pauses the queue execution. In the eQADC, detecting a pause bit in the command pauses command transfers from a CFIFO.
Queue Operation Mode (MQ*n*)	CFIFO Operation Mode (MODE*n*)	The eQADC supports all queue operation modes in the QADC except operation modes related to a periodic timer. A timer elsewhere in the system can provide the same functionality if it is connected to ETRIG*n*.
Queue Status (QS)	CFIFO Status (CFS*n*)	In the QADC, the queue status is read to check whether a queue is idle, active, paused, suspended, or trigger pending. In the eQADC, the CFIFO status is read to check whether a queue is IDLE, WAITING FOR TRIGGER (idle or paused in QADC), or triggered (suspended or trigger pending in QADC).

The eQADC and QADC also have similar procedures for the configuration or execution of applications. Table 19-60 shows the steps required for the QADC versus the steps required for the eQADC system.

Table 19-60. Usage Comparison between QADC and eQADC System

Procedure	QADC	eQADC System
Analog Control Configuration	Configure analog device by writing to the QADCs.	Program configuration commands into command queues.
Prepare Scan Sequence	Program scan commands into command queues.	Program scan commands into command queues.
Queue Control Configuration	Write to the QADC control registers.	Write to the eQADC control registers.
Data Transferred between Queues and Buffers	Not Required.	Program the eDMA or the CPU to handle the data transfer.
Serial Interface Configuration	Not Required.	Write to the eQADC SSI registers.
Queue Execution	Require software or external trigger events to start queue execution.	Require software or external trigger events to start command transfers from a CFIFO.

Chapter 20
Deserial Serial Peripheral Interface (DSPI)

20.1 Introduction

This chapter describes the deserial serial peripheral interface (DSPI), which provides a synchronous serial bus for communication between the MCU and an external peripheral device.

Microcontroller chips in the MPC55xx family implement different DSPI modules. Some implement DSPI A, B, C, and D, and others implement only B, C, and D, for example. The "*x*" appended to signal names signifies the module to which the signal applies. Thus PCS*x*[0] specifies that the PCS signal applies to module A, B, and so on.

20.1.1 Block Diagram

A block diagram of the DSPI is shown in Figure 20-1.

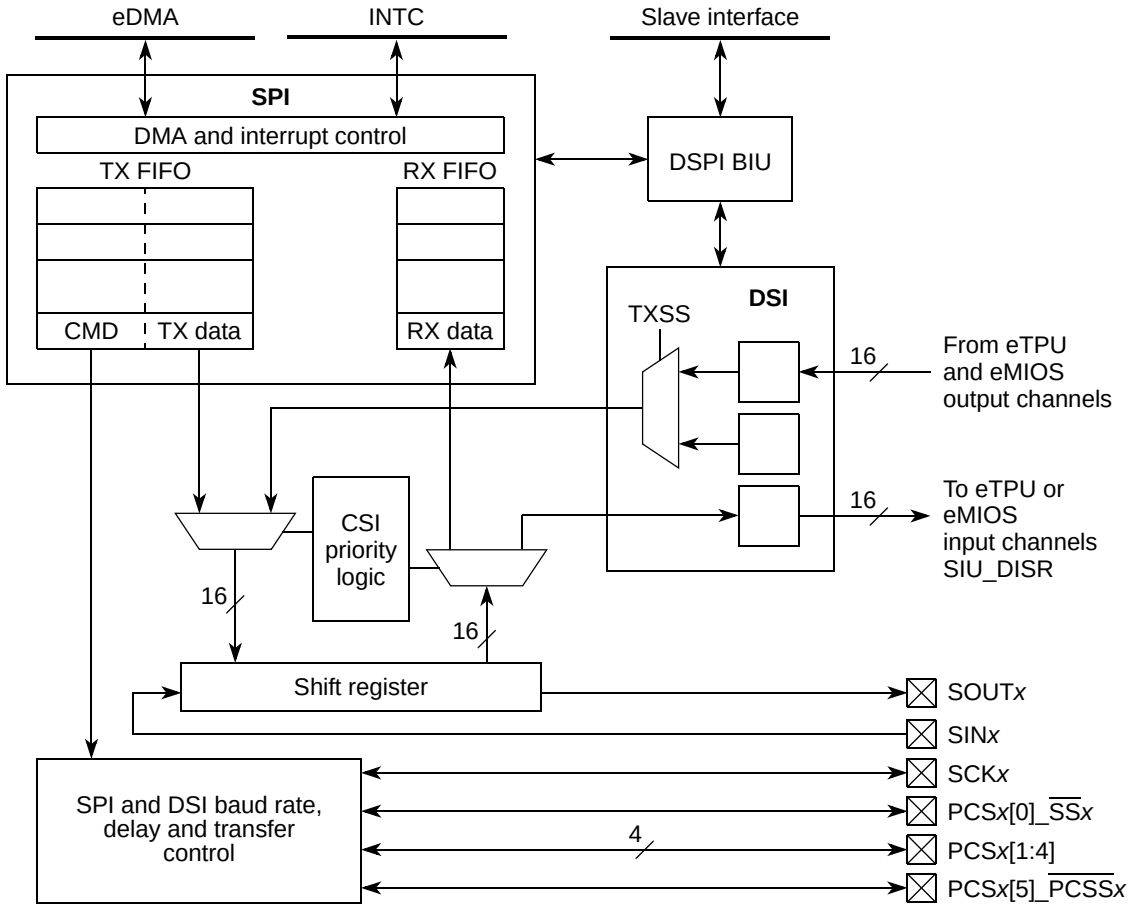


Figure 20-1. DSPI Block Diagram

20.1.2 Overview

The DSPI supports pin count reduction through serialization and deserialization of eTPU channels, eMIOS channels, and memory-mapped registers. Incoming serial data may be used to trigger external interrupt requests through DSPI deserialized output connections to the SIU. The channels and register content are transmitted using an SPI protocol. There are four identical DSPI modules (DSPI A, DSPI B, DSPI C, and DSPI D) on the device. The DSPI has three configurations:

- Serial peripheral interface (SPI) configuration where the DSPI operates as an SPI with support for queues.
- Deserial serial interface (DSI) configuration where the DSPI serializes eTPU and eMIOS output channels and deserializes the received data by placing the data on the eTPU and eMIOS input channels and as inputs to the external interrupt request submodule of the SIU.

- Combined serial interface (CSI) configuration where the DSPI operates in both SPI and DSI configurations interleaving DSI frames with SPI frames, giving priority to SPI frames.

For queued operations the SPI queues reside in internal SRAM which is external to the DSPI. Data transfers between the queues and the DSPI FIFOs are done using the eDMA controller or host software. Figure 20-2 shows a DSPI with external queues in internal SRAM.

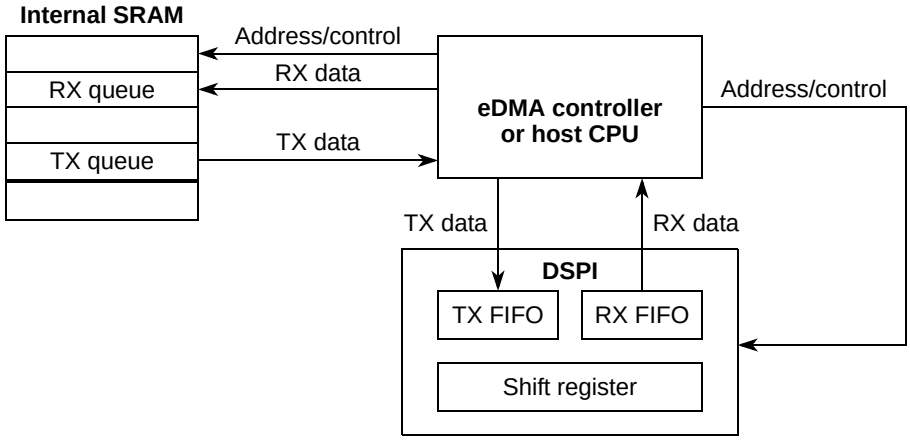


Figure 20-2. DSPI with Queues and eDMA

20.1.3 Features

The DSPI supports these SPI features:

- Full-duplex, three-wire synchronous transfers
- Master and slave mode
- Buffered transmit and receive operation using the TX and RX FIFOs, with depths of four entries
- Visibility into TX and RX FIFOs for ease of debugging
- FIFO bypass mode for low-latency updates to SPI queues
- Programmable transfer attributes on a per-frame basis
  - — Eight clock and transfer attribute registers
  - — Serial clock with programmable polarity and phase
  - — Programmable delays
    - – PCS to SCK delay
    - – SCK to PCS delay
    - – Delay between frames
  - — Programmable serial frame size of 4 to 16 bits, expandable with software control
  - — Continuously held chip select capability
- Six peripheral chip selects, expandable to 64 with external demultiplexer
- Deglitching support for up to 32 peripheral chip selects with external demultiplexer

- Two DMA conditions for SPI queues residing in RAM or flash
  - TX FIFO is not full (TFFF)
  - RX FIFO is not empty (RFDF)
- Six interrupt conditions:
  - End of queue reached (EOQF)
  - TX FIFO is not full (TFFF)
  - Transfer of current frame complete (TCF)
  - RX FIFO is not empty (RFDF)
  - FIFO overrun
    - Attempt to transmit an empty TX FIFO
    - Serial frame was received while RX FIFO is full (RFOF)
  - FIFO under flow
    For the slave only in SPI mode.
    Request to the slave for a data transfer when the TX FIFO is empty (TFUF)
- Modified SPI transfer formats for communication with slower peripheral devices
- Supports all functional modes from QSPI subblock of QSMCM (MPC500 family)
- Continuous serial communications clock (SCK)

When configured for DSI or CSI operation, the DSPI supports pin reduction through serialization and deserialization.

- Serialized data sources
  - eTPUA, eTPUB and eMIOS output channels
  - Memory-mapped register in the DSPI
- Deserialized data destinations
  - eTPUA and eMIOS input channels
  - SIU external interrupt request inputs
  - Memory-mapped register in the DSPI
- Transfer initiation conditions
  - Continuous
  - Edge-sensitive hardware trigger
  - Change in data
- Support for parallel and serial chaining of DSPI modules
- Pin serialization/deserialization with interleaved SPI frames for control and diagnostics

20.1.4 Modes of Operation

The DSPI has four modes of operation. These modes can be divided into two categories; module-specific modes such as master, slave, and module disable modes, and a second category that is an MCU-specific mode: debug mode.

The module-specific modes are entered by host software writing to a register. The MCU-specific mode is controlled by signals external to the DSPI. The MCU-specific mode is a mode that the entire device may enter, in parallel to the DSPI being in one of its module-specific modes.

20.1.4.1 Master Mode

Master mode allows the DSPI to initiate and control serial communication. In this mode the SCK, PCS*n* and SOUT signals are controlled by the DSPI and configured as outputs.

For more information, see Section 20.4.1.1, “Master Mode.”

20.1.4.2 Slave Mode

Slave mode allows the DSPI to communicate with SPI / DSI bus masters. In this mode the DSPI responds to externally controlled serial transfers. The DSPI cannot initiate serial transfers in slave mode. In slave mode, the SCK signal and the PCS*x*[0]_$\overline{SS}$ signal are configured as inputs and provided by a bus master. PCS*x*[0]_$\overline{SS}$ must be configured as input and pulled high. If the internal pullup is being used then the appropriate bits in the relevant SIU_PCR must be set (SIU_PCR [WPE = 1], [WPS = 1]).

For more information, see Section 20.4.1.2, “Slave Mode.”

20.1.4.3 Module Disable Mode

The module disable mode is used for MCU power management. The clock to the non-memory mapped logic in the DSPI is stopped while in module disable mode. The DSPI enters the module disable mode when the MDIS bit in DSPI*x*_MCR is set.

For more information, see Section 20.4.1.3, “Module Disable Mode.”

20.1.4.4 Debug Mode

Debug mode is used for system development and debugging. If the device enters debug mode while the FRZ bit in the DSPI*x*_MCR is set, the DSPI halts operation on the next frame boundary. If the device enters debug mode while the FRZ bit is cleared, the DSPI behavior is unaffected and remains dictated by the module-specific mode and configuration of the DSPI.

For more information, see Section 20.4.1.4, “Debug Mode.”

20.2 External Signal Description

20.2.1 Signal Overview

Table 20-1 lists off-chip DSPI signals.

Table 20-1. Signal Properties

Name	I/O Type	Function	
		Master Mode	Slave Mode
PCS*x*[0]_$\overline{SS}$	Output / input	Peripheral chip select 0	Slave select
PCS*x*[1:3]	Output	Peripheral chip select 1–3	Unused [1]
PCS*x*[4]_$\overline{MTRIG}$	Output	Peripheral chip select 4	Master trigger
PCS*x*[5]_$\overline{PCSS}$	Output	Peripheral chip select 5 / Peripheral chip select strobe	Unused [1]
SIN*x*	Input	Serial data in	Serial data in
SOUT*x*	Output	Serial data out	Serial data out
SCK*x*	Output / input	Serial clock (output)	Serial clock (input)

[1] The SIU allows you to select alternate pin functions for the device.

20.2.2 Signals and Descriptions

20.2.2.1 Peripheral Chip Select / Slave Select (PCS*x*[0]_$\overline{SS}$)

In master mode, the PCS*x*[0] signal is a peripheral chip select output that selects the slave device for the current transmission.

In slave mode, the $\overline{SS}$ signal is a slave select input signal that allows a SPI master to select the DSPI as the target for transmission. PCS*x*[0]_$\overline{SS}$ must be configured as input and pulled high. If the internal pullup is used then the bits in the SIU_PCR must be set (SIU_PCR [WPE = 1], [WPS = 1]).

Set the input buffer enable (IBE) and the output buffer enable (OBE) bits to 1 in the SIU_PCR for all PCSx[0] pins when the DSPI chip select or slave select primary function is configured for that pin. When the pin is used for DSPI master mode as a chip select output, set the OBE bit. When the pin is used in DSPI slave mode as a slave select input, set the IBE bit to 1.

See Section 6.3.1.12, “Pad Configuration Registers (SIU_PCR),” for more information.

20.2.2.2 Peripheral Chip Selects 1–3 (PCS*x*[1:3])

PCS*x*[1:3] are peripheral chip select output signals in master mode. In slave mode these signals are not used.

20.2.2.3 Peripheral Chip Select 4 / Master Trigger (PCS*x*[4]_$\overline{\text{MTRIG}}$)

PCS*x*[4] is a peripheral chip select output signal in master mode. In slave mode this signal is a master trigger.

20.2.2.4 Peripheral Chip Select 5 / Peripheral Chip Select Strobe (PCS*x*[5]_$\overline{\text{PCSS}}$)

PCSx[5] is a peripheral chip select output signal. When the DSPI is in master mode and the PCSSE bit in the DSPI*x*_MCR is cleared to 0, the PCS*x*[5] signal selects the slave device that receives the current transfer.

$\overline{\text{PCSS}}$ is a strobe signal used by external logic for deglitching of the PCS signals. When the DSPI is in master mode and the PCSSE bit in the DSPI*x*_MCR is set to 1, the $\overline{\text{PCSS}}$ signal indicates the timing used to decode PCS*x*[0:4] signals, which prevents glitches from occurring.

PCS*x*[5]_$\overline{\text{PCSS}}$ is not used in slave mode.

20.2.2.5 Serial Input (SIN*x*)

SIN*x* is a serial data input signal.

20.2.2.6 Serial Output (SOUT*x*)

SOUT*x* is a serial data output signal.

20.2.2.7 Serial Clock (SCK*x*)

SCK*x* is a serial communication clock signal. In master mode, the DSPI generates the SCK. In slave mode, SCK*x* is an input from an external bus master.

20.3 Memory Map and Register Definition

20.3.1 Memory Map

Table 20-2 shows the DSPI memory map.

Table 20-2. DSPI Detailed Memory Map

Address	Register Name	Register Description	Bits
Base: 0xFFF9_0000 (DSPI A) 0xFFF9_4000 (DSPI B) 0xFFF9_8000 (DSPI C) 0xFFF9_C000 (DSPI D)	DSPI*x*_MCR	DSPI module configuration register	32
Base + 0x0004	—	Reserved	—
Base + 0x0008	DSPI*x*_TCR	DSPI transfer count register	32
Base + 0x000C	DSPI*x*_CTAR0	DSPI clock and transfer attributes register 0	32

Table 20-2. DSPI Detailed Memory Map (continued)

Address	Register Name	Register Description	Bits
Base + 0x0010	DSPI*x*_CTAR1	DSPI clock and transfer attributes register 1	32
Base + 0x0014	DSPI*x*_CTAR2	DSPI clock and transfer attributes register 2	32
Base + 0x0018	DSPI*x*_CTAR3	DSPI clock and transfer attributes register 3	32
Base + 0x001C	DSPI*x*_CTAR4	DSPI clock and transfer attributes register 4	32
Base + 0x0020	DSPI*x*_CTAR5	DSPI clock and transfer attributes register 5	32
Base + 0x0024	DSPI*x*_CTAR6	DSPI clock and transfer attributes register 6	32
Base + 0x0028	DSPI*x*_CTAR7	DSPI clock and transfer attributes register 7	32
Base + 0x002C	DSPI*x*_SR	DSPI status register	32
Base + 0x0030	DSPI*x*_RSER	DSPI DMA/interrupt request select and enable register	32
Base + 0x0034	DSPI*x*_PUSHR	DSPI push TX FIFO register	32
Base + 0x0038	DSPI*x*_POPR	DSPI pop RX FIFO register	32
Base + 0x003C	DSPI*x*_TXFR0	DSPI transmit FIFO register 0	32
Base + 0x0040	DSPI*x*_TXFR1	DSPI transmit FIFO register 1	32
Base + 0x0044	DSPI*x*_TXFR2	DSPI transmit FIFO register 2	32
Base + 0x0048	DSPI*x*_TXFR3	DSPI transmit FIFO register 3	32
Base + 0x004C–0x0078	—	Reserved	—
Base + 0x007C	DSPI*x*_RXFR0	DSPI receive FIFO register 0	32
Base + 0x0080	DSPI*x*_RXFR1	DSPI receive FIFO register 1	32
Base + 0x0084	DSPI*x*_RXFR2	DSPI receive FIFO register 2	32
Base + 0x0088	DSPI*x*_RXFR3	DSPI receive FIFO register 3	32
Base + 0x008C–0x00B8	—	Reserved	—
Base + 0x00BC	DSPI*x*_DSICR	DSPI DSI configuration register	32
Base + 0x00C0	DSPI*x*_SDR	DSPI DSI serialization data register	32
Base + 0x00C4	DSPI*x*_ASDR	DSPI DSI alternate serialization data register	32
Base + 0x00C8	DSPI*x*_COMPR	DSPI DSI transmit comparison register	32
Base + 0x00CC	DSPI*x*_DDR	DSPI DSI deserialization data register	32

20.3.2 Register Descriptions

20.3.2.1 DSPI Module Configuration Register (DSPI*x*_MCR)

The DSPI*x*_MCR contains bits that configure the DSPI operation. The values of the HALT and MDIS bits can be changed at any time, but the effect begins on the next frame boundary. The HALT and MDIS bits in the DSPI*x*_MCR are the only bit values software can change while the DSPI is running.

Address: Base + 0x0000 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	MSTR	CONT_SCKE	DCONF		FRZ	MTFE	PCSSE	ROOE	0	0	PCSIS5	PCSIS4	PCSIS3	PCSIS2	PCSIS1	PCSIS0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	MDIS	DIS_TXF	DIS_RXF	CLR_TXF	CLR_RXF	SMPL_PT		0	0	0	0	0	0	0	HALT
W					w1c	w1c										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure 20-3. DSPI Module Configuration Register (DSPI*x*_MCR)

The following table describes the fields in the DSPI module configuration register:

Table 20-3. DSPI*x*_MCR Field Descriptions

Field	Description
0 MSTR	Master or slave mode select. Configures the DSPI for master mode or slave mode. 0 DSPI is in slave mode 1 DSPI is in master mode
1 CONT_SCKE	Continuous SCK enable. Enables the serial communication clock (SCK) to run continuously. See Section 20.4.8, “Continuous Serial Communications Clock,” for details. 0 Continuous SCK disabled 1 Continuous SCK enabled
2–3 DCONF [0:1]	DSPI configuration. Selects between the three different configurations of the DSPI. The following table lists the DCONF values for the various configurations. **DCONF** / **Configuration** 00 / SPI 01 / DSI 10 / CSI 11 / Invalid value
4 FRZ	Freeze. Enables the DSPI transfers to be stopped on the next frame boundary when the device enters debug mode. 0 Do not halt serial transfers 1 Halt serial transfers

Table 20-3. DSPI*x*_MCR Field Descriptions (continued)

Field	Description
5 MTFE	Modified timing format enable. Enables a modified transfer format to be used. See Section 20.4.7.4, "Modified Transfer Format Enabled (MTFE = 1) with Classic SPI Transfer Format Set (CPHA = 1) for SPI and DSI." 0 Modified SPI transfer format disabled 1 Modified SPI transfer format enabled
6 PCSSE	Peripheral chip select strobe enable. Enables the PCS*x*[5]_$\overline{\text{PCSS}}$ to operate as a PCS strobe output signal. See Section 20.4.6.5, "Peripheral Chip Select Strobe Enable (PCSS)." 0 PCS*x*[5]_$\overline{\text{PCSS}}$ is used as the peripheral chip select 5 signal 1 PCS*x*[5] _$\overline{\text{PCSS}}$ is used as an active-low PCS strobe signal
7 ROOE	Receive FIFO overflow overwrite enable. Enables an RX FIFO overflow condition to ignore the incoming serial data or to overwrite existing data. If the RX FIFO is full and new data is received, the data from the transfer that generated the overflow is ignored or put in the shift register. If the ROOE bit is set, the incoming data is put in the shift register. If the ROOE bit is cleared, the incoming data is ignored. See Section 20.4.9.6, "Receive FIFO Overflow Interrupt Request (RFOF)." 0 Incoming data is ignored 1 Incoming data is put in the shift register
8–9	Reserved, but implemented. These bits are writable, but have no effect.
10–15 PCSIS*n*	Peripheral chip select inactive state. Determines the inactive state of the PCS*x*[*n*] signal. You must configure PCS*x*[0]_$\overline{\text{SS}}$ as inactive high for slave mode operation. 0 The inactive state of PCS*x*[*n*] is low 1 The inactive state of PCS*x*[*n*] is high
16	Reserved
17 MDIS	Module disable. Allows the clock to stop to non-memory mapped logic in the DSPI, effectively putting the DSPI in a software controlled power-saving state. The reset value of the MDIS bit is parameterized, with a default reset value of 0. See Section 20.4.10, "Power Saving Features." 0 Enable DSPI clocks 1 Allow external logic to disable DSPI clocks
18 DIS_TXF	Disable transmit FIFO. Enables and disables the TX FIFO. When the TX FIFO is disabled, the transmit part of the DSPI operates as a simplified double-buffered SPI. See Section 20.4.3.3, "FIFO Disable Operation for details." 0 TX FIFO is enabled 1 TX FIFO is disabled
19 DIS_RXF	Disable receive FIFO. Enables and disables the RX FIFO. When the RX FIFO is disabled, the receive part of the DSPI operates as a simplified double-buffered SPI. See Section 20.4.3.3, "FIFO Disable Operation for details." 0 RX FIFO is enabled 1 RX FIFO is disabled

Table 20-3. DSPI*x*_MCR Field Descriptions (continued)

Field	Description
20 CLR_TXF	Clear TX FIFO. Flushes the TX FIFO. Write a 1 to the CLR_TXF bit to clear the TX FIFO counter. The CLR_TXF bit is always read as zero. 0 Do not clear the TX FIFO counter 1 Clear the TX FIFO counter
21 CLR_RXF	Clear RX FIFO. Flushes the RX FIFO. Write a 1 to the CLR_RXF bit to clear the RX counter. The CLR_RXF bit is always read as zero. 0 Do not clear the RX FIFO counter 1 Clear the RX FIFO counter
22–23 SMPL_ PT [0:1]	Sample point. Allows the host software to select when the DSPI master samples SIN in modified transfer format. Figure 20-36 shows where the master can sample the SIN pin. The following table lists the delayed sample points. **SMPL_PT** / **Number of system clock cycles between odd-numbered edge of SCK[*x*] and sampling of SIN[*x*].** 00 — 0 01 — 1 10 — 2 11 — Invalid value
24–30	Reserved
31 HALT	Halt. Provides a mechanism for software to start and stop DSPI transfers. See Section 20.4.2, “Start and Stop of DSPI Transfers,” for details on the operation of this bit. 0 Start transfers 1 Stop transfers

20.3.2.2 DSPI Transfer Count Register (DSPI*x*_TCR)

The DSPI*x*_TCR contains a counter that indicates the number of SPI transfers made. The transfer counter is intended to assist in queue management. The user must not write to the DSPI*x*_TCR while the DSPI is running.

Address: Base + 0x0008 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	SPI_TCNT															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-4. DSPI Transfer Count Register (DSPI*x*_TCR)

The following table describes the field in the DSPI transfer count register:

Table 20-4. DSPI*x*_TCR Field Descriptions

Field	Description
0–15 SPI_TCNT [0:15]	SPI transfer counter. Counts the number of SPI transfers the DSPI makes. The SPI_TCNT field is incremented every time the last bit of an SPI frame is transmitted. A value written to SPI_TCNT presets the counter to that value. SPI_TCNT is reset to zero at the beginning of the frame when the CTCNT field is set in the executing SPI command. The transfer counter 'wraps around,' incrementing the counter past 65535 resets the counter to zero.
16–31	Reserved

20.3.2.3 DSPI Clock and Transfer Attributes Registers 0–7 (DSPI*x*_CTAR*n*)

The DSPI modules each contain eight clock and transfer attribute registers (DSPI*x*_CTAR*n*) which are used to define different transfer attribute configurations. Each DSPI*x*_CTAR controls:

- Frame size
- Baud rate and transfer delay values
- Clock phase
- Clock polarity
- MSB or LSB first

DSPI*x*_CTARs support compatibility with the QSPI module in the MPC5xx family of MCUs. See Section 20.5.4, "MPC5xx QSPI Compatibility with the DSPI," for a discussion on DSPI and QSPI compatibility. At the initiation of an SPI or DSI transfer, control logic selects the DSPI*x*_CTAR that contains the transfer attributes. Do not write to the DSPI*x*_CTARs while the DSPI is running.

In master mode, the DSPI*x*_CTAR*n* registers define combinations of transfer attributes such as frame size, clock phase and polarity, data bit ordering, baud rate, and various delays. In slave mode, a subset of the bit fields in the DSPI*x*_CTAR0 and DSPI*x*_CTAR1 registers are used to set the slave transfer attributes. See the individual bit descriptions for details on which bits are used in slave modes.

When the DSPI is configured as a SPI master, the CTAS field in the command portion of the TX FIFO entry selects which of the DSPI*x*_CTAR registers is used on a per-frame basis. When the DSPI is configured as a SPI bus slave, the DSPI*x*_CTAR0 register is used.

When the DSPI is configured as a DSI master, the DSICTAS field in the DSPI DSI configuration register (DSPI*x*_DSICR) selects which of the DSPI*x*_CTAR register is used. See Section 20.3.2.10, “DSPI DSI Configuration Register (DSPIx_DSICR).” When the DSPI is configured as a DSI bus slave, the DSPI*x*_CTAR1 register is used.

In CSI configuration, the transfer attributes are selected based on whether the current frame is SPI data or DSI data. SPI transfers in CSI configuration follow the protocol described for SPI configuration, and DSI transfers in CSI configuration follow the protocol described for DSI configuration. CSI configuration is only valid in conjunction with master mode. See Section 20.4.5, “Combined Serial Interface (CSI) Configuration” for more details.

Address: Access: R/W
Base + 0x000C (DSPI*x*_CTAR0)
Base + 0x0010 (DSPI*x*_CTAR1)
Base + 0x0014 (DSPI*x*_CTAR2)
Base + 0x0018 (DSPI*x*_CTAR3)
Base + 0x001C (DSPIx_CTAR4)
Base + 0x0020 (DSPI*x*_CTAR5)
Base + 0x0024 (DSPI*x*_CTAR6)
Base + 0x0028 (DSPI*x*_CTAR7)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	DBR	FMSZ				CPOL	CPHA	LSB FE	PCSSCK		PASC		PDT		PBR	
Reset	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	CSSCK				ASC				DT				BR			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-5. DSPI Clock and Transfer Attributes Registers 0–7 (DSPI*x*_CTAR*n*)

The following table describes the fields in the DSPI clock and transfer attributes register:

Table 20-5. DSPI*x*_CTAR*n* Field Description

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>0
DBR</td><td>Double baud rate. The DBR bit doubles the effective baud rate of the serial communications clock (SCK). This field is only used in master mode. It effectively halves the baud rate division ratio supporting faster frequencies and odd division ratios for the serial communications clock (SCK). When the DBR bit is set, the duty cycle of the serial communications clock (SCK) depends on the value in the baud rate prescaler and the clock phase bit as listed in the following table. See the BR field and Section 20.4.6.1, “Baud Rate Generator” for details on how to compute the baud rate. If the overall baud rate is divided by two or three system clocks, do not enable continuous SCK or the modified timing format.

0 Baud rate is computed normally with a 50/50 duty cycle
1 Baud rate is doubled with the duty cycle depending on the baud rate prescaler
<table>
<tr><th>DBR</th><th>CPHA</th><th>PBR</th><th>SCK Duty Cycle</th></tr>
<tr><td>0</td><td>any</td><td>any</td><td>50/50</td></tr>
<tr><td>1</td><td>0</td><td>00</td><td>50/50</td></tr>
<tr><td>1</td><td>0</td><td>01</td><td>33/66</td></tr>
<tr><td>1</td><td>0</td><td>10</td><td>40/60</td></tr>
<tr><td>1</td><td>0</td><td>11</td><td>43/57</td></tr>
<tr><td>1</td><td>1</td><td>00</td><td>50/50</td></tr>
<tr><td>1</td><td>1</td><td>01</td><td>66/33</td></tr>
<tr><td>1</td><td>1</td><td>10</td><td>60/40</td></tr>
<tr><td>1</td><td>1</td><td>11</td><td>57/43</td></tr>
</table>
</td></tr>
<tr><td>1–4
FMSZ
[0:3]</td><td>FMSZ. Selects the number of bits transferred per frame. The FMSZ field is used in master mode and slave mode. The following table lists the frame sizes.
<table>
<tr><th>FMSZ</th><th>Frame Size</th><th>FMSZ</th><th>Frame Size</th></tr>
<tr><td>0000</td><td>Invalid value</td><td>1000</td><td>9</td></tr>
<tr><td>0001</td><td>Invalid value</td><td>1001</td><td>10</td></tr>
<tr><td>0010</td><td>Invalid value</td><td>1010</td><td>11</td></tr>
<tr><td>0011</td><td>4</td><td>1011</td><td>12</td></tr>
<tr><td>0100</td><td>5</td><td>1100</td><td>13</td></tr>
<tr><td>0101</td><td>6</td><td>1101</td><td>14</td></tr>
<tr><td>0110</td><td>7</td><td>1110</td><td>15</td></tr>
<tr><td>0111</td><td>8</td><td>1111</td><td>16</td></tr>
</table>
</td></tr>
</table>

Table 20-5. DSPI*x*_CTAR*n* Field Description (continued)

Field	Description
5 CPOL	Clock polarity. Selects the inactive state of the serial communications clock (SCK*x*). This bit is used in both master and slave mode. For successful communication between serial devices, the devices must have identical clock polarities. When the continuous selection format is selected (CONT = 1 or DCONT = 1), switching between clock polarities without stopping the DSPI can cause errors in the transfer due to the peripheral device interpreting the switch of clock polarity as a valid clock edge. For more information on continuous selection format, see Section 20.4.7.5, "Continuous Selection Format." 0 The inactive state value of SCK*x* is low 1 The inactive state value of SCK*x* is high
6 CPHA	Clock phase. Selects which edge of SCK*x* causes data to change and which edge causes data to be captured. This bit is used in both master and slave mode. For successful communication between serial devices, the devices must have identical clock phase settings. 0 Data is *captured* on the leading edge of SCK*x* and *changed* on the following edge 1 Data is *changed* on the leading edge of SCK*x* and *captured* on the following edge
7 LSBFE	LSB first enable. Selects if the LSB or MSB of the frame is transferred first. This bit is only used in master mode. 0 Data is transferred MSB first 1 Data is transferred LSB first
8–9 PCSSCK [0:1]	PCS*x* to SCK*x* delay prescaler. Selects the prescaler value for the delay between assertion of PCS*x* and the first edge of the SCK*x*. Use in master mode only. The following table lists the prescaler values. The description for bitfield CSSCK in Table 20-5 details how to compute the PCS to SCK delay. **PCSSCK Value** / **PCS*x* to SCK*x* Delay Prescaler Value** 00 / 1 01 / 3 10 / 5 11 / 7
10–11 PASC [0:1]	After SCK*x* delay prescaler. Selects the prescaler value for the delay between the last edge of SCK*x* and the negation of PCS*x*. Use in master mode only. The following table lists the prescaler values. The description for bitfield ASC in Table 20-5 details how to compute the after SCK*x* delay. **PASC Value** / **After SCK*x* Delay Prescaler Value** 00 / 1 01 / 3 10 / 5 11 / 7

Table 20-5. DSPI*x*_CTAR*n* Field Description (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>12–13
PDT
[0:1]</td><td>Delay after transfer prescaler. The PDT field selects the prescaler value for the delay between the negation of the PCSx signal at the end of a frame and the assertion of PCSx at the beginning of the next frame. The PDT field is only used in master mode. The following table lists the prescaler values. The description for bitfield DT in Table 20-5 details how to compute the delay after transfer.
<table>
<tr><th>PDT Value</th><th>Delay after Transfer Prescaler Value</th></tr>
<tr><td>00</td><td>1</td></tr>
<tr><td>01</td><td>3</td></tr>
<tr><td>10</td><td>5</td></tr>
<tr><td>11</td><td>7</td></tr>
</table></td></tr>
<tr><td>14–15
PBR
[0:1]</td><td>Baud rate prescaler. Selects the prescaler value for the baud rate. Use in master mode only. The baud rate is the frequency of the serial communications clock (SCKx). The system clock is divided by the prescaler value before the baud rate selection takes place. The baud rate prescaler values are listed in the following table. The description for PBR in Section 20.4.6.1, “Baud Rate Generator” details how to compute the baud rate.
<table>
<tr><th>PBR Value</th><th>Baud Rate Prescaler Value</th></tr>
<tr><td>00</td><td>2</td></tr>
<tr><td>01</td><td>3</td></tr>
<tr><td>10</td><td>5</td></tr>
<tr><td>11</td><td>7</td></tr>
</table></td></tr>
</table>

Table 20-5. DSPI*x*_CTAR*n* Field Description (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>16–19
CSSCK
[0:3]</td><td>PCSx to SCKx delay scaler. Selects the scaler value for the PCSx to SCKx delay. Use in master mode only. The PCSx to SCKx delay is the delay between the assertion of PCSx and the first edge of the SCKx. The following table lists the scaler values.
<table>
<tr><th>CSSCK Value</th><th>PCS to SCK Delay Scaler Value</th><th>CSSCK Value</th><th>PCS to SCK Delay Scaler Value</th></tr>
<tr><td>0000</td><td>2</td><td>1000</td><td>512</td></tr>
<tr><td>0001</td><td>4</td><td>1001</td><td>1024</td></tr>
<tr><td>0010</td><td>8</td><td>1010</td><td>2048</td></tr>
<tr><td>0011</td><td>16</td><td>1011</td><td>4096</td></tr>
<tr><td>0100</td><td>32</td><td>1100</td><td>8192</td></tr>
<tr><td>0101</td><td>64</td><td>1101</td><td>16384</td></tr>
<tr><td>0110</td><td>128</td><td>1110</td><td>32768</td></tr>
<tr><td>0111</td><td>256</td><td>1111</td><td>65536</td></tr>
</table>
The PCSx to SCKx delay is a multiple of the system clock period. It is computed using the following equation:
$t_{CSC} = \frac{1}{f_{SYS}} \times \text{PCSSCK prescaler value} \times \text{CSSCK scaler value}$
Note: See Section 20.4.6.2, “PCS to SCK Delay (tCSC),” for more details.</td></tr>
<tr><td>20-23
ASC[0:3]</td><td>After SCKx delay scaler. Selects the scaler value for the After SCKx delay. Use in master mode only. The after SCKx delay is the delay between the last edge of SCKx and the negation of PCSx. The following table lists the scaler values.
<table>
<tr><th>ASC Value</th><th>After SCK Delay Scaler Value</th><th>ASC Value</th><th>After SCK Delay Scaler Value</th></tr>
<tr><td>0000</td><td>2</td><td>1000</td><td>512</td></tr>
<tr><td>0001</td><td>4</td><td>1001</td><td>1024</td></tr>
<tr><td>0010</td><td>8</td><td>1010</td><td>2048</td></tr>
<tr><td>0011</td><td>16</td><td>1011</td><td>4096</td></tr>
<tr><td>0100</td><td>32</td><td>1100</td><td>8192</td></tr>
<tr><td>0101</td><td>64</td><td>1101</td><td>16384</td></tr>
<tr><td>0110</td><td>128</td><td>1110</td><td>32768</td></tr>
<tr><td>0111</td><td>256</td><td>1111</td><td>65536</td></tr>
</table>
The after SCKx delay is a multiple of the system clock period, and it is computed using the following equation:
$t_{ASC} = \frac{1}{f_{SYS}} \times \text{PASC Prescaler value} \times \text{ASC Scaler value}$
Note: See Section 20.4.6.3, “After SCK Delay (tASC),” for more details.</td></tr>
</table>

Table 20-5. DSPI*x*_CTAR*n* Field Description (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>24–27
DT[0:3]</td><td>Delay after transfer scaler. The DT field selects the delay after transfer scaler. Use in master mode only. The delay after transfer is the time between the negation of the PCSx signal at the end of a frame and the assertion of PCSx at the beginning of the next frame. The following table lists the scaler values.
<table>
<tr><th>DT Value</th><th>Delay after Transfer Scaler Value</th><th>DT Value</th><th>Delay after Transfer Scaler Value</th></tr>
<tr><td>0000</td><td>2</td><td>1000</td><td>512</td></tr>
<tr><td>0001</td><td>4</td><td>1001</td><td>1024</td></tr>
<tr><td>0010</td><td>8</td><td>1010</td><td>2048</td></tr>
<tr><td>0011</td><td>16</td><td>1011</td><td>4096</td></tr>
<tr><td>0100</td><td>32</td><td>1100</td><td>8192</td></tr>
<tr><td>0101</td><td>64</td><td>1101</td><td>16384</td></tr>
<tr><td>0110</td><td>128</td><td>1110</td><td>32768</td></tr>
<tr><td>0111</td><td>256</td><td>1111</td><td>65536</td></tr>
</table>
The delay after transfer is a multiple of the system clock period. It is computed using the following equation:
$$t_{DT} = \frac{1}{f_{SYS}} \times \text{PDT Prescaler value} \times \text{DT Scaler value}$$
Note: See Section 20.4.6.4, “Delay after Transfer (tDT),” for more details</td></tr>
</table>

Table 20-5. DSPI*x*_CTAR*n* Field Description (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>28–31
BR[0:3]</td><td>Baud rate scaler. Selects the scaler value for the baud rate. Use in master mode only. The pre-scaled system clock is divided by the baud rate scaler to generate the frequency of the SCK. The following table lists the baud rate scaler values.
<table>
<tr><th>BR Value</th><th>Baud Rate Scaler Value</th><th>BR Value</th><th>Baud Rate Scaler Value</th></tr>
<tr><td>0000</td><td>2</td><td>1000</td><td>256</td></tr>
<tr><td>0001</td><td>4</td><td>1001</td><td>512</td></tr>
<tr><td>0010</td><td>6</td><td>1010</td><td>1024</td></tr>
<tr><td>0011</td><td>8</td><td>1011</td><td>2048</td></tr>
<tr><td>0100</td><td>16</td><td>1100</td><td>4096</td></tr>
<tr><td>0101</td><td>32</td><td>1101</td><td>8192</td></tr>
<tr><td>0110</td><td>64</td><td>1110</td><td>16384</td></tr>
<tr><td>0111</td><td>128</td><td>1111</td><td>32768</td></tr>
</table>
The baud rate is computed using the following equation:
$$\text{SCK baud rate} = \frac{f_{SYS}}{\text{PBRPrescalerValue}} \times \frac{1 + \text{DBR}}{\text{BRScalerValue}}$$
Note: See Section 20.4.6.1, “Baud Rate Generator,” for more details.</td></tr>
</table>

20.3.2.4 DSPI Status Register (DSPI*x*_SR)

The DSPI*x*_SR contains status and flag bits. The bits are set by the hardware and reflect the status of the DSPI and indicate the occurrence of events that can generate interrupt or DMA requests. Software can clear flag bits in the DSPI*x*_SR by writing a 1 to clear it (w1c). Writing a 0 to a flag bit has no effect.

Address: Base + 0x002C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	TCF	TXRXS	0	EOQF	TFUF	0	TFFF	0	0	0	0	0	RFOF	0	RFDF	0
W	w1c			w1c	w1c		w1c						w1c		w1c	
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	TXCTR				TXNXTPTR				RXCTR				POPNXTPTR			
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-6. DSPI Status Register (DSPI*x*_SR)

The following table describes the fields in the DSPI status register:

Table 20-6. DSPI*x*_SR Field Descriptions

Field	Description
0 TCF	Transfer complete flag. Indicates that all bits in a frame have been shifted out. The TCF bit is set after the last incoming databit is sampled, but before the tASC delay starts. See Section 20.4.7.1, “Classic SPI Transfer Format (CPHA = 0)” for details. The TCF bit is cleared by writing 1 to it. 0 Transfer not complete 1 Transfer complete
1 TXRXS	TX and RX status. Reflects the status of the DSPI. See Section 20.4.2, “Start and Stop of DSPI Transfers” for information on what clears and sets this bit. 0 TX and RX operations are disabled (DSPI is in STOPPED state) 1 TX and RX operations are enabled (DSPI is in RUNNING state)
2	Reserved
3 EOQF	End of queue flag. Indicates that transmission in progress is the last entry in a queue. The EOQF bit is set when the TX FIFO entry has the EOQ bit set in the command halfword and after the last incoming databit is sampled, but before the tASC delay starts. See Section 20.4.7.1, “Classic SPI Transfer Format (CPHA = 0)” for details. The EOQF bit is cleared by writing 1 to it. When the EOQF bit is set, the TXRXS bit is automatically cleared. 0 EOQ is not set in the executing command 1 EOQ bit is set in the executing SPI command **Note:** EOQF does not function in slave mode.
4 TFUF	Transmit FIFO underflow flag. Indicates that an underflow condition in the TX FIFO has occurred. The transmit underflow condition is detected only for DSPI modules operating in slave mode and SPI configuration. The TFUF bit is set when the TX FIFO of a DSPI operating in SPI slave mode is empty, and a transfer is initiated by an external SPI master. The TFUF bit is cleared by writing 1 to it. 0 TX FIFO underflow has not occurred 1 TX FIFO underflow has occurred
5	Reserved
6 TFFF	Transmit FIFO fill flag. Indicates that the TX FIFO can be filled. Provides a method for the DSPI to request more entries to be added to the TX FIFO. The TFFF bit is set while the TX FIFO is not full. The TFFF bit can be cleared by writing 1 to it, or an by acknowledgement from the eDMA controller when the TX FIFO is full. 0 TX FIFO is full 1 TX FIFO is not full
7–11	Reserved
12 RFOF	Receive FIFO overflow flag. Indicates that an overflow condition in the RX FIFO has occurred. The bit is set when the RX FIFO and shift register are full and a transfer is initiated. The bit is cleared by writing 1 to it. 0 RX FIFO overflow has not occurred 1 RX FIFO overflow has occurred
13	Reserved

Table 20-6. DSPI*x*_SR Field Descriptions (continued)

Field	Description
14 RFDF	Receive FIFO drain flag. Indicates that the RX FIFO can be drained. Provides a method for the DSPI to request that entries be removed from the RX FIFO. The bit is set while the RX FIFO is not empty. The RFDF bit can be cleared by writing 1 to it, or by acknowledgement from the eDMA controller when the RX FIFO is empty. 0 RX FIFO is empty 1 RX FIFO is not empty **Note:** In the interrupt service routine, RFDF must be cleared only after the DSPIx_POPR register is read.
15	Reserved
16–19 TXCTR [0:3]	TX FIFO counter. Indicates the number of valid entries in the TX FIFO. The TXCTR is incremented every time the DSPI _PUSHR is written. The TXCTR is decremented every time an SPI command is executed and the SPI data is transferred to the shift register.
20–23 TXNXTPTR [0:3]	Transmit next pointer. Indicates which TX FIFO entry is transmitted during the next transfer. The TXNXTPTR field is updated every time SPI data is transferred from the TX FIFO to the shift register. See Section 20.4.3.4, “Using the TX FIFO Buffering Mechanism” for more details.
24–27 RXCTR [0:3]	RX FIFO counter. Indicates the number of entries in the RX FIFO. The RXCTR is decremented every time the DSPI _POPR is read. The RXCTR is incremented after the last incoming databit is sampled, but before the tASC delay starts. See Section 20.4.7.1, “Classic SPI Transfer Format (CPHA = 0)” for details.
28–31 POPNXTPTR [0:3]	Pop next pointer. Contains a pointer to the RX FIFO entry that is returned when the DSPI*x*_POPR is read. The POPNXTPTR is updated when the DSPI*x*_POPR is read. See Section 20.4.3.5, “Using the RX FIFO Buffering Mechanism” for more details.

20.3.2.5 DSPI DMA / Interrupt Request Select and Enable Register (DSPI*x*_RSER)

The DSPI*x*_RSER serves two purposes: enables flag bits in the DSPI*x*_SR to generate DMA requests or interrupt requests, and selects the type of request to generate. See the bit descriptions for the type of requests that are supported. Do not write to the DSPI*x*_RSER while the DSPI is running.

Address: Base + 0x0030 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	TCF_RE	0	0	EOQF_RE	TFUF_RE	0	TFFF_RE	TFFF_DIRS	0	0	0	0	RFOF_RE	0	RFDF_RE	RFDF_DIRS
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-7. DSPI DMA / Interrupt Request Select and Enable Register (DSPI*x*_RSER)

The following table describes the fields in the DSPI DMA / interrupt request and enable register:

Table 20-7. DSPI*x*_RSER Field Descriptions

Field	Description
0 TCF_RE	Transmission complete request enable. Enables TCF flag in the DSPI*x*_SR to generate an interrupt request. 0 TCF interrupt requests are disabled 1 TCF interrupt requests are enabled
1–2	Reserved
3 EOQF_RE	DSPI finished request enable. Enables the EOQF flag in the DSPI*x*_SR to generate an interrupt request. 0 EOQF interrupt requests are disabled 1 EOQF interrupt requests are enabled
4 TFUF_RE	Transmit FIFO underflow request enable. The TFUF_RE bit enables the TFUF flag in the DSPI*x*_SR to generate an interrupt request. 0 TFUF interrupt requests are disabled 1 TFUF interrupt requests are enabled
5	Reserved
6 TFFF_RE	Transmit FIFO fill request enable. Enables the TFFF flag in the DSPI*x*_SR to generate a request. The TFFF_DIRS bit selects between generating an interrupt request or a DMA requests. 0 TFFF interrupt requests or DMA requests are disabled 1 TFFF interrupt requests or DMA requests are enabled
7 TFFF_DIRS	Transmit FIFO fill DMA or interrupt request select. Selects between generating a DMA request or an interrupt request. When the TFFF flag bit in the DSPI*x*_SR is set, and the TFFF_RE bit in the DSPI*x*_RSER is set, this bit selects between generating an interrupt request or a DMA request. 0 Interrupt request is selected 1 DMA request is selected
8–11	Reserved
12 RFOF_RE	Receive FIFO overflow request enable. Enables the RFOF flag in the DSPI*x*_SR to generate an interrupt requests. 0 RFOF interrupt requests are disabled 1 RFOF interrupt requests are enabled
13	Reserved
14 RFDF_RE	Receive FIFO drain request enable. Enables the RFDF flag in the DSPI*x*_SR to generate a request. The RFDF_DIRS bit selects between generating an interrupt request or a DMA request. 0 RFDF interrupt requests or DMA requests are disabled 1 RFDF interrupt requests or DMA requests are enabled

Table 20-7. DSPI*x*_RSER Field Descriptions (continued)

Field	Description
15 RFDF_DIRS	Receive FIFO drain DMA or interrupt request select. Selects between generating a DMA request or an interrupt request. When the RFDF flag bit in the DSPI*x*_SR is set, and the RFDF_RE bit in the DSPI*x*_RSER is set, the RFDF_DIRS bit selects between generating an interrupt request or a DMA request. 0 Interrupt request is selected 1 DMA request is selected
16–31	Reserved

20.3.2.6 DSPI PUSH TX FIFO Register (DSPI*x*_PUSHR)

The DSPI*x*_PUSHR provides a means to write to the TX FIFO. Data written to this register is transferred to the TX FIFO. See Section 20.4.3.4, "Using the TX FIFO Buffering Mechanism," for more information. Write accesses of 8- or 16-bits to the DSPI*x*_PUSHR transfers 32 bits to the TX FIFO.

NOTE

TXDATA is used in master and slave modes.

Address: Base + 0x0034 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	CONT	CTAS			EOQ	CT CNT	0	0	0	0	PCS5	PCS4	PCS3	PCS2	PCS1	PCS0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	TXDATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-8. DSPI PUSH TX FIFO Register (DSPI*x*_PUSHR)

The following table describes the fields in the DSPI push transmit FIFO register:

Table 20-8. DSPI*x*_PUSHR Field Descriptions

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>0
CONT</td><td>Continuous peripheral chip select enable. Selects a continuous selection format. The bit is used in SPI master mode. The bit enables the selected PCS signals to remain asserted between transfers. See Section 20.4.7.5, “Continuous Selection Format,” for more information.

0 Return peripheral chip select signals to their inactive state between transfers
1 Keep peripheral chip select signals asserted between transfers</td></tr>
<tr><td>1–3
CTAS
[0:2]</td><td>Clock and transfer attributes select. Selects which of the DSPIx_CTARs is used to set the transfer attributes for the SPI frame. In SPI slave mode, DSPIx_CTAR0 is used. The following table shows how the CTAS values map to the DSPIx_CTARs. There are eight DSPIx_CTARs in the device DSPI implementation.

Note: Use in SPI master mode only.
<table>
<tr><th>CTAS</th><th>Use Clock and Transfer Attributes from</th></tr>
<tr><td>000</td><td>DSPIx_CTAR0</td></tr>
<tr><td>001</td><td>DSPIx_CTAR1</td></tr>
<tr><td>010</td><td>DSPIx_CTAR2</td></tr>
<tr><td>011</td><td>DSPIx_CTAR3</td></tr>
<tr><td>100</td><td>DSPIx_CTAR4</td></tr>
<tr><td>101</td><td>DSPIx_CTAR5</td></tr>
<tr><td>110</td><td>DSPIx_CTAR6</td></tr>
<tr><td>111</td><td>DSPIx_CTAR7</td></tr>
</table></td></tr>
<tr><td>4
EOQ</td><td>End of queue. Provides a means for host software to signal to the DSPI that the current SPI transfer is the last in a queue. At the end of the transfer the EOQF bit in the DSPIx_SR is set.

0 The SPI data is not the last data to transfer
1 The SPI data is the last data to transfer
Note: Use in SPI master mode only.</td></tr>
<tr><td>5
CTCNT</td><td>Clear SPI_TCNT. Provides a means for host software to clear the SPI transfer counter. The CTCNT bit clears the SPI_TCNT field in the DSPIx_TCR. The SPI_TCNT field is cleared before transmission of the current SPI frame begins.

0 Do not clear SPI_TCNT field in the DSPIx_TCR
1 Clear SPI_TCNT field in the DSPIx_TCR
Note: Use in SPI master mode only.</td></tr>
<tr><td>6–7</td><td>Reserved</td></tr>
<tr><td>8–9</td><td>Reserved, but implemented. These bits are writable, but have no effect.</td></tr>
</table>

Table 20-8. DSPI*x*_PUSHR Field Descriptions (continued)

Field	Description
10–15 PCS*x*	Peripheral chip select *x*. Selects which PCS*x* signals are asserted for the transfer. 0 Negate the PCS*x* signal 1 Assert the PCS*x* signal **Note:** Use in SPI master mode only.
16–31 TXDATA [0:15]	Transmit data. Holds SPI data for transfer according to the associated SPI command. **Note:** Use TXDATA in master and slave modes.

20.3.2.7 DSPI POP RX FIFO Register (DSPI*x*_POPR)

The DSPI*x*_POPR allows you to read the RX FIFO. See Section 20.4.3.5, “Using the RX FIFO Buffering Mechanism” for a description of the RX FIFO operations. Eight or 16-bit read accesses to the DSPI*x*_POPR fetch the RX FIFO data, and update the counter and pointer.

NOTE

Reading the RX FIFO field fetches data from the RX FIFO. Once the RX FIFO is read, the read data pointer is moved to the next entry in the RX FIFO. Therefore, read DSPI*x*_POPR only when you need the data. For compatibility, configure the TLB (MMU table) entry for DSPI*x*_POPR as guarded.

Address: Base + 0x0038 Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	RXDATA															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-9. DSPI POP RX FIFO Register (DSPI*x*_POPR)

The following table describes the fields in the DSPI pop receive FIFO register:

Table 20-9. DSPI*x*_POPR Field Descriptions

Field	Description
0–15	Reserved, must be cleared.
16–31 RXDATA [0:15]	Received data. The RXDATA field contains the SPI data from the RX FIFO entry pointed to by the pop next data pointer (POPNXTPTR).

20.3.2.8 DSPI Transmit FIFO Registers 0–3 (DSPI*x*_TXFR*n*)

The DSPI*x*_TXFR*n* registers provide visibility into the TX FIFO for debugging purposes. Each register is an entry in the TX FIFO. The registers are read-only and cannot be modified. Reading the DSPI*x*_TXFR*n* registers does not alter the state of the TX FIFO. The MCU uses four registers to implement the TX FIFO, that is DSPI*x*_TXFR0–DSPI*x*_TXFR3 are used.

Address:
Base + 0x003C (DSPI*x*_TXFR0)
Base + 0x0040 (DSPI*x*_TXFR1)
Base + 0x0044 (DSPI*x*_TXFR2)
Base + 0x0048 (DSPI*x*_TXFR3)

Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	TXCMD															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	TXDATA															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-10. DSPI Transmit FIFO Register 0–3 (DSPI*x*_TXFR*n*)

The following table describes the fields in the DSPI transmit FIFO register:

Table 20-10. DSPI*x*_TXFR*n* Field Descriptions

Field	Description
0–15 TXCMD [0:15]	Transmit command. Contains the command that sets the transfer attributes for the SPI data. See Section 20.3.2.6, “DSPI PUSH TX FIFO Register (DSPIx_PUSHR),” for details on the command field.
16–31 TXDATA [0:15]	Transmit data. Contains the SPI data to be shifted out.

20.3.2.9 DSPI Receive FIFO Registers 0–3 (DSPI*x*_RXFR*n*)

The DSPI*x*_RXFR*n* registers provide visibility into the RX FIFO for debugging purposes. Each register is an entry in the RX FIFO. The DSPI*x*_RXFR registers are read-only. Reading the DSPI*x*_RXFR*n* registers does not alter the state of the RX FIFO. The device uses four registers to implement the RX FIFO, that is DSPI*x*_RXFR0–DSPI*x*_RXFR3 are used.

Address:
Base + 0x007C (DSPI*x*_RXFR0)
Base + 0x0080 (DSPI*x*_RXFR1)
Base + 0x0084 (DSPI*x*_RXFR2)
Base + 0x0088 (DSPI*x*_RXFR3)

Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	RXDATA															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-11. DSPI Receive FIFO Registers 0–3 (DSPI*x*_RXFR*n*)

The following table describes the field in the DSPI receive FIFO register:

Table 20-11. DSPI*x*_RXFR*n* Field Description

Field	Description
0–15	Reserved, must be cleared.
16–31 RXDATA [15:0]	Receive data. Contains the received SPI data.

20.3.2.10 DSPI DSI Configuration Register (DSPI*x*_DSICR)

The DSPI*x*_DSICR selects attributes for DSI and CSI configurations. Do not write to the DSPI*x*_DSICR while the DSPI is running.

Address: Base + 0x00BC Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	MTOE	0	MTOCNT						0	0	0	0	TXSS	TPOL	TRRE	CID
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	DCONT	DSICTAS			0	0	0	0	0	0	DPCS5	DPCS4	DPCS3	DPCS2	DPCS1	DPCS0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-12. DSPI DSI Configuration Register (DSPI*x*_DSICR)

The following table describes the fields in the DSPI deserial serial interface configuration register:

Table 20-12. DSPI*x*_DSICR Field Descriptions

Field	Description
0 MTOE	Multiple transfer operation enable. Enables multiple DSPIs connected in a parallel or serial configuration. See Section 20.4.4.7, "Multiple Transfer Operation (MTO)," for more information. 0 Multiple transfer operation disabled 1 Multiple transfer operation enabled
1	Reserved
2–7 MTOCNT [0:5]	Multiple transfer operation count. Selects number of bits to be shifted out during a transfer in multiple transfer operation. The field sets the number of SCK cycles that the bus master needs to generate to complete the transfer. The number of SCK cycles used are one more than the value in the MTOCNT field. The number of SCK cycles defined by MTOCNT must be equal to or greater than the frame size.
8–11	Reserved
12 TXSS	Transmit data source select. Selects the source of data to be serialized. The source can be data from host software written to the DSPI DSI alternate serialization data register (DSPI*x*_ASDR), or parallel output pin states latched into the DSPI DSI serialization data register (DSPI*x*_SDR). 0 Source of serialized data is the DSPI*x*_SDR 1 Source of serialized data is the DSPI*x*_ASDR
13 TPOL	Trigger polarity. Selects the active edge of the internal hardware trigger input signal (*ht*). The bit selects which edge initiates a transfer in the DSI configuration. See Section 20.4.4.5, "DSI Transfer Initiation Control," for more information. 0 Falling-edge initiates a transfer 1 Rising-edge initiates a transfer

Table 20-12. DSPI*x*_DSICR Field Descriptions (continued)

<table>
<tr><th>Field</th><th>Description</th></tr>
<tr><td>14
TRRE</td><td>Trigger reception enable. Enables the DSPI to initiate a transfer when an external trigger signal is received. The bit is only valid in DSI configuration. See Section 20.4.4.5, “DSI Transfer Initiation Control,” for more information.

0 Trigger signal reception disabled
1 Trigger signal reception enabled</td></tr>
<tr><td>15
CID</td><td>Change in data transfer enable. Enables a change in serialization data to initiate a transfer. The bit is used in master mode in DSI and CSI configurations to control when to initiate transfers. When the CID bit is set, serialization is initiated when the current DSI data differs from the previous DSI data shifted out. The DSPIx_COMPR is compared with the DSPIx_SDR or DSPIx_ASDR to detect a change in data. See Section 20.4.4.5, “DSI Transfer Initiation Control,” for more information.

0 Change in data transfer operation disabled
1 Change in data transfer operation enabled</td></tr>
<tr><td>16
DCONT</td><td>DSI continuous peripheral chip select enable. Enables the PCSx signals to remain asserted between transfers. The DCONT bit only affects the PCS signals in DSI master mode. See Section 20.4.7.5, “Continuous Selection Format,” for details.

0 Return peripheral chip select signals to their inactive state after transfer is complete
1 Keep peripheral chip select signals asserted after transfer is complete</td></tr>
<tr><td>17–19
DSICTAS
[0:2]</td><td>DSI clock and transfer attributes select. The DSICTAS field selects which of the DSPIx_CTARs is used to provide transfer attributes in DSI configuration. The DSICTAS field is used in DSI master mode. In DSI slave mode, the DSPIx_CTAR1 is always selected. The following table lists the DSICTAS to DSPIx_CTARs mapping.
<table>
<tr><th>DSICTAS</th><th>DSI Clock and Transfer Attributes Controlled by</th></tr>
<tr><td>000</td><td>DSPIx_CTAR0</td></tr>
<tr><td>001</td><td>DSPIx_CTAR1</td></tr>
<tr><td>010</td><td>DSPIx_CTAR2</td></tr>
<tr><td>011</td><td>DSPIx_CTAR3</td></tr>
<tr><td>100</td><td>DSPIx_CTAR4</td></tr>
<tr><td>101</td><td>DSPIx_CTAR5</td></tr>
<tr><td>110</td><td>DSPIx_CTAR6</td></tr>
<tr><td>111</td><td>DSPIx_CTAR7</td></tr>
</table>
</td></tr>
<tr><td>20–23</td><td>Reserved</td></tr>
<tr><td>24–25</td><td>Reserved, but implemented. These bits are writable, but have no effect.</td></tr>
<tr><td>26–31
DPCSx</td><td>DSI peripheral chip select n. The DPCS bits select which of the PCSx signals to assert during a DSI transfer. The DPCS bits assert and negate the PCSx signals in DSI master mode only.

0 Negate PCSx
1 Assert PCSx</td></tr>
</table>

20.3.2.11 DSPI DSI Serialization Data Register (DSPI*x*_SDR)

The DSPI*x*_SDR contains the signal states of the parallel input signals from the eTPU or the eMIOS. The pin states of the parallel input signals are latched into the DSPI*x*_SDR on the rising edge of every system clock. The DSPI*x*_SDR is read-only. When the TXSS bit in the DSPI*x*_DSICR is negated, the data in the DSPI*x*_SDR is the source of the serialized data.

Address: Base + 0x00C0 Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	SER_DATA [15:0]															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-13. DSPI DSI Serialization Data Register (DSPI*x*_SDR)

The following table describes the field in the DSPI deserial serial interface serialization data register:

Table 20-13. DSPI*x*_SDR Field Description

Bits	Description
0–15	Reserved
16–31 SER_ DATA [15:0]	Serialized data. The SER_DATA field contains the signal states of the parallel input signals. SER_DATA [15:0] maps to DSPI serialization inputs IN[15:0]. See Section 20.4.4.6, “DSPI Connections to eTPUA, eTPUB, eMIOS and SIU.”

20.3.2.12 DSPI DSI Alternate Serialization Data Register (DSPI*x*_ASDR)

The DSPI*x*_ASDR allows the host software to write data to be serialized. When the TXSS bit in the DSPI*x*_DSICR is set, the data in the DSPI*x*_ASDR is the source of the serialized data. Writes to the DSPI*x*_ASDR take effect on the next frame boundary.

Address: Base + 0x00C4 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	ASER_DATA															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-14. DSPI DSI Alternate Serialization Data Register (DSPI*x*_ASDR)

The following table describes the field in the DSPI deserial serial interface alternate serialization data register:

Table 20-14. DSPI*x*_ASDR Field Description

Field	Description
0–15	Reserved
16–31 ASER_ DATA [0:15]	Alternate serialized data. The ASER_DATA field holds the alternate data to be serialized.

20.3.2.13 DSPI DSI Transmit Comparison Register (DSPI*x*_COMPR)

The DSPI*x*_COMPR holds a copy of the last transmitted DSI data. The DSPI*x*_COMPR is read-only. DSI data is transferred to this register as it is loaded into the transmit shift register.

Address: Base + 0x00C8 Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	COMP_DATA															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-15. DSPI DSI Transmit Comparison Register (DSPI*x*_COMPR)

The following table describes the field in the DSPI deserial serial interface transmit comparison register:

Table 20-15. DSPI*x*_COMPR Field Description

Field	Description
0–15	Reserved
16–31 COMP_ DATA [0:15]	Compare data. The COMP_DATA field holds the last serialized DSI data.

20.3.2.14 DSPI DSI Deserialization Data Register (DSPI*x*_DDR)

The DSPI*x*_DDR holds the signal states for the parallel output signals. The DSPI*x*_DDR is read-only and it is memory mapped so that host software can read the incoming DSI frames.

Address: Base + 0x00CC Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	DESER_DATA															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 20-16. DSPI Deserialization Data Register (DSPI*x*_DDR)

The following table describes the field in the DSPI deserialization data register:

Table 20-16. DSPI*x*_DDR Field Description

Field	Description
0–15	Reserved
16–31 DESER DATA	Deserialized data. Holds deserialized data which is presented as signal states to the parallel output signals.

20.4 Functional Description

The DSPI supports full-duplex, synchronous serial communications between the MCU and peripheral devices. The DSPI can also be used to reduce the number of pins required for I/O by serializing and deserializing up to 16 parallel input/output signals from the eTPU and eMIOS. All communications are through an SPI-like protocol.

The DSPI has three configurations:

- Serial peripheral interface (SPI) configuration in which the DSPI operates as a basic SPI or a queued SPI.
- Deserial serial interface (DSI) configuration where the DSPI serializes eTPU and eMIOS output channels and deserializes the received data by placing it on the eTPU and eMIOS input channels and as inputs to the External Interrupt Request subblock of the SIU.
- Combined serial interface (CSI) configuration where the DSPI operates in both SPI and DSI configurations interleaving DSI frames with SPI frames, giving priority to SPI frames.

The DCONF field in the DSPI*x*_MCR register determines the DSPI configuration. See Table 20-3 for the DSPI configuration values.

The DSPI*x*_CTAR0–DSPI*x*_CTAR7 registers hold clock and transfer attributes. The manner in which a CTAR is selected depends on the DSPI configuration (SPI, DSI, or CSI). The SPI configuration can select which CTAR to use on a frame by frame basis by setting the CTAS field in the DSPI*x*_PUSHR. The DSI configuration statically selects which CTAR to use. In CSI configuration, priority logic determines if SPI data or DSI data is transferred. The type of data transferred (whether DSI or SPI) dictates which CTAR the CSI configuration uses. See Section 20.3.2.3, "DSPI Clock and Transfer Attributes Registers 0–7 (DSPIx_CTARn)," for information on DSPI*x*_CTAR fields.

The 16-bit shift register in the master and the 16-bit shift register in the slave are linked by the SOUT*x* and SIN*x* signals to form a distributed 32-bit register. When a data transfer operation is performed, data is serially shifted a pre-determined number of bit positions. Because the registers are linked, data is exchanged between the master and the slave; the data that was in the master's shift register is now in the shift register of the slave, and vice versa. At the end of a transfer, the TCF bit in the DSPI*x*_SR is set to indicate a completed transfer. Figure 20-17 illustrates how master and slave data is exchanged.

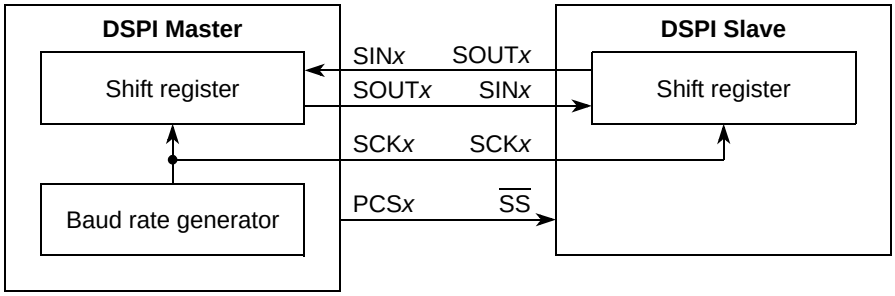


Figure 20-17. SPI and DSI Serial Protocol Overview

The DSPI has six peripheral chip select (PCS*x*) signals that are be used to select which of the slaves to communicate with.

Transfer protocols and timing properties are shared by the three DSPI configurations; these properties are described independently of the configuration in Section 20.4.7, "Transfer Formats." The transfer rate and delay settings are described in section Section 20.4.6, "DSPI Baud Rate and Clock Delay Generation."

See Section 20.4.10, "Power Saving Features" for information on the power-saving features of the DSPI.

20.4.1 Modes of Operation

The DSPI modules have four available distinct modes:

- Master mode
- Slave mode
- Module disable mode
- Debug mode

Master, slave, and module disable modes are module-specific modes while debug mode is a device-specific mode.

The module-specific modes are determined by bits in the DSPI*x*_MCR. Debug mode is a mode that the entire device can enter in parallel with the DSPI being configured in one of its module-specific modes.

20.4.1.1 Master Mode

In master mode the DSPI can initiate communications with peripheral devices. The DSPI operates as bus master when the MSTR bit in the DSPI*x*_MCR is set. The serial communications clock (SCK) is controlled by the master DSPI. All three DSPI configurations are valid in master mode.

In SPI configuration, master mode transfer attributes are controlled by the SPI command in the current TX FIFO entry. The CTAS field in the SPI command selects which of the eight DSPI*x*_CTARs are used to set the transfer attributes. Transfer attribute control is on a frame by frame basis.

See Section 20.4.3, "Serial Peripheral Interface (SPI) Configuration" for more details.

In DSI configuration, master mode transfer attributes are controlled by the DSPI*x*_DSCIR. A detailed description of the DSPI*x*_DSCIR is located in Section 20.3.2.10, "DSPI DSI Configuration Register (DSPIx_DSICR)." The DSISCTAS field in the DSPI*x*_DSICR selects which of the DSPI*x*_CTARs are used to set the transfer attributes. Transfer attributes are set up during initialization and must not be changed between frames.

See Section 20.4.4, "Deserial Serial Interface (DSI) Configuration," for more details.

The CSI configuration is only available in master mode. In CSI configuration, the DSI data is transferred using DSI configuration transfer attributes and SPI data is transferred using the SPI configuration transfer attributes. In order for the bus slave to distinguish between DSI and SPI frames, the transfer attributes for the two types of frames must utilize different peripheral chip select signals.

See Section 20.4.5, "Combined Serial Interface (CSI) Configuration," for details.

20.4.1.2 Slave Mode

In slave mode the DSPI responds to transfers initiated by an SPI master. The DSPI operates as bus slave when the MSTR bit in the DSPI*x*_MCR is negated. The DSPI slave is selected by a bus master by having the slave's $\overline{SS}$ asserted. In slave mode the SCK is provided by the bus master. All transfer attributes are controlled by the bus master, except the clock polarity, clock phase and the number of bits to transfer which must be configured in the DSPI slave to communicate correctly.

The SPI and DSI configurations are valid in slave mode. CSI configuration is not available in slave mode. In SPI slave mode the slave transfer attributes are set in the DSPI*x*_CTAR0. In DSI slave mode the slave transfer attributes are set in the DSPI*x*_CTAR1. In slave mode, for both SPI and DSI configurations, data is transferred MSB first. The LSBFE field of the associated CTAR is ignored.

20.4.1.3 Module Disable Mode

The module disable mode is used for MCU power management. The clock to the non-memory mapped logic in the DSPI is stopped while in module disable mode. The DSPI enters the module disable mode when the MDIS bit in DSPI*x*_MCR is set.

See Section 20.4.10, "Power Saving Features," for more details on the module disable mode.

20.4.1.4 Debug Mode

The debug mode is used for system development and debugging. If the MCU enters debug mode while the FRZ bit in the DSPI*x*_MCR is set, the DSPI stops all serial transfers and enters a stopped state. If the MCU enters debug mode while the FRZ bit is cleared, the DSPI behavior is unaffected and remains dictated by the module-specific mode and configuration of the DSPI. The DSPI enters debug mode when a debug request is asserted by an external controller.

See Figure 20-18 for a state diagram.

20.4.2 Start and Stop of DSPI Transfers

The DSPI has two operating states: STOPPED and RUNNING. The states are independent of DSPI configuration. The default state of the DSPI is STOPPED. In the STOPPED state no serial transfers are initiated in master mode and no transfers are responded to in slave mode. The STOPPED state is also a safe state for writing the various configuration registers of the DSPI without causing undetermined results. The TXRXS bit in the DSPI*x*_SR is cleared in this state. In the RUNNING state, serial transfers take place. The TXRXS bit in the DSPI*x*_SR is set in the RUNNING state.

Figure 20-18 shows a state diagram of the start and stop mechanism.

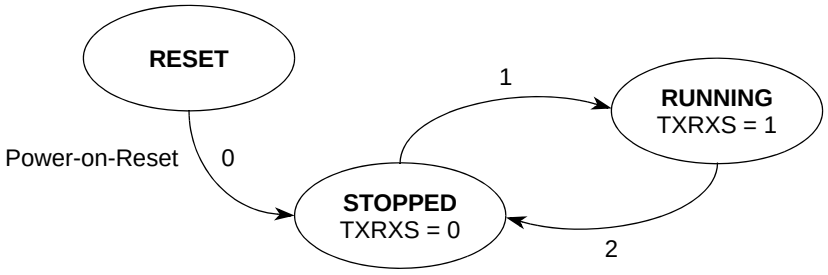


Figure 20-18. DSPI Start and Stop State Diagram

The transitions are described in Table 20-17.

Table 20-17. State Transitions for Start and Stop of DSPI Transfers

Transition #	Current State	Next State	Description
0	RESET	STOPPED	Generic power-on-reset transition
1	STOPPED	RUNNING	The DSPI starts (transitions from STOPPED to RUNNING) when all of the following conditions are true: • EOQF bit is clear • Debug mode is deselected or the FRZ bit is clear • HALT bit is clear
2	RUNNING	STOPPED	The DSPI stops (transitions from RUNNING to STOPPED) after the current frame for any one of the following conditions: • EOQF bit is set • Debug mode is selected and the FRZ bit is set • HALT bit is set

State transitions from RUNNING to STOPPED occur on the next frame boundary if a transfer is in progress, or on the next system clock cycle if no transfers are in progress.

20.4.3 Serial Peripheral Interface (SPI) Configuration

The SPI configuration transfers data serially using a shift register and a selection of programmable transfer attributes. The DSPI is in SPI configuration when the DCONF field in the DSPI*x*_MCR is 0b00. The SPI frames can be from 4 to 16 bits long. The data to be transmitted can come from queues stored in RAM external to the DSPI. Host software or an eDMA controller can transfer the SPI data from the queues to a first-in first-out (FIFO) buffer. The received data is stored in entries in the receive FIFO (RX FIFO) buffer. Host software or an eDMA controller transfers the received data from the RX FIFO to memory external to the DSPI.

The FIFO buffer operations are described in Section 20.4.3.4, "Using the TX FIFO Buffering Mechanism," and Section 20.4.3.5, "Using the RX FIFO Buffering Mechanism."

The interrupt and DMA request conditions are described in Section 20.4.9, "Interrupts and DMA Requests."

The SPI configuration supports two module-specific modes; master mode and slave mode. The FIFO operations are similar for the master mode and slave mode. The main difference is that in master mode the DSPI initiates and controls the transfer according to the fields in the SPI command field of the TX FIFO entry. In slave mode the DSPI only responds to transfers initiated by a bus master external to the DSPI and the SPI command field of the TX FIFO entry is ignored.

20.4.3.1 SPI Master Mode

In SPI master mode the DSPI initiates the serial transfers by controlling the serial communications clock (SCK*x*) and the peripheral chip select (PCS*x*) signals. The SPI command field in the executing TX FIFO entry determines which CTARs are used to set the transfer attributes and which PCS*x* signal to assert. The command field also contains various bits that help with queue management and transfer protocol. The data field in the executing TX FIFO entry is loaded into the shift register and shifted out on the serial out (SOUT*x*) pin. In SPI master mode, each SPI frame to be transmitted has a command associated with it allowing for transfer attribute control on a frame by frame basis.

See Section 20.3.2.6, "DSPI PUSH TX FIFO Register (DSPIx_PUSHR)," for details on the SPI command fields.

20.4.3.2 SPI Slave Mode

In SPI slave mode the DSPI responds to transfers initiated by an SPI bus master. The DSPI does not initiate transfers. Certain transfer attributes such as clock polarity, clock phase and frame size must be set for successful communication with an SPI master. The SPI slave mode transfer attributes are set in the DSPI*x*_CTAR0.

20.4.3.3 FIFO Disable Operation

The FIFO disable mechanisms allow SPI transfers without using the TX FIFO or RX FIFO. The DSPI operates as a double-buffered simplified SPI when the FIFOs are disabled. The TX and RX FIFOs are disabled separately. The TX FIFO is disabled by writing a 1 to the DIS_TXF bit in the DSPI*x*_MCR. The RX FIFO is disabled by writing a 1 to the DIS_RXF bit in the DSPI*x*_MCR.

The FIFO disable mechanisms are transparent to the user and to host software; transmit data and commands are written to the DSPI*x*_PUSHR and received data is read from the DSPI*x*_POPR. When the TX FIFO is disabled, the TFFF, TFUF, and TXCTR fields in DSPI*x*_SR behave as if there is a one-entry FIFO but the contents of the DSPI*x*_TXFRs and TXNXTPTR are undefined. When the RX FIFO is disabled, the RFDF, RFOF, and RXCTR fields in the DSPI*x*_SR behave as if there is a one-entry FIFO but the contents of the DSPI*x*_RXFRs and POPNXTPTR are undefined.

Disable the TX and RX FIFOs only if the FIFO must be disabled as a requirement of the application's operating mode. A FIFO must be disabled before it is accessed. Failure to disable a FIFO prior to a first FIFO access is not supported, and can result in incorrect results.

20.4.3.4 Using the TX FIFO Buffering Mechanism

The TX FIFO functions as a buffer of SPI data and SPI commands for transmission. The TX FIFO holds four entries, each consisting of a command field and a data field. SPI commands and data are added to the TX FIFO by writing to the DSPI push TX FIFO register (DSPI*x*_PUSHR). For more information on DSPI*x*_PUSHR. TX FIFO entries can only be removed from the TX FIFO by being shifted out or by flushing the TX FIFO.

See Section 20.3.2.6, “DSPI PUSH TX FIFO Register (DSPIx_PUSHR).”

The TX FIFO counter field (TXCTR) in the DSPI status register (DSPI*x*_SR) indicates the number of valid entries in the TX FIFO. The TXCTR is updated every time the DSPI _PUSHR is written or SPI data is transferred into the shift register from the TX FIFO.

See Section 20.3.2.4, “DSPI Status Register (DSPIx_SR)” for more information on DSPI*x*_SR.

The TXNXTPTR field indicates which TX FIFO entry is transmitted during the next transfer. The TXNXTPTR contains the positive offset from DSPI*x*_TXFR0 in number of 32-bit registers. For example, TXNXTPTR equal to two means that the DSPI*x*_TXFR2 contains the SPI data and command for the next transfer. The TXNXTPTR field is incremented every time SPI data is transferred from the TX FIFO to the shift register.

20.4.3.4.1 Filling the TX FIFO

Host software or the eDMA controller can add (push) entries to the TX FIFO by writing to the DSPI*x*_PUSHR. When the TX FIFO is not full, the TX FIFO fill flag (TFFF) in the DSPI*x*_SR is set. The TFFF bit is cleared when the TX FIFO is full and the eDMA controller indicates that a write to DSPI*x*_PUSHR is complete or alternatively by host software writing a 1 to the TFFF in the DSPI*x*_SR. The TFFF can generate a DMA request or an interrupt request.

See Section 20.4.9.2, “Transmit FIFO Fill Interrupt or DMA Request (TFFF),” for details.

The DSPI ignores attempts to push data to a full TX FIFO; that is, the state of the TX FIFO is unchanged. No error condition is indicated.

20.4.3.4.2 Draining the TX FIFO

The TX FIFO entries are removed (drained) by shifting SPI data out through the shift register. Entries are transferred from the TX FIFO to the shift register and shifted out as long as there are valid entries in the TX FIFO. Every time an entry is transferred from the TX FIFO to the shift register, the TX FIFO counter is decremented by one. At the end of a transfer, the TCF bit in the DSPI*x*_SR is set to indicate the completion of a transfer. The TX FIFO is flushed by writing a 1 to the CLR_TXF bit in DSPI*x*_MCR.

If an external SPI bus master initiates a transfer with a DSPI slave while the slave's DSPI TX FIFO is empty, the transmit FIFO underflow flag (TFUF) in the slave's DSPI*x*_SR is set.

See Section 20.4.9.4, "Transmit FIFO Underflow Interrupt Request (TFUF)," for details.

20.4.3.5 Using the RX FIFO Buffering Mechanism

The RX FIFO functions as a buffer for data received on the SIN pin. The RX FIFO holds four received SPI data frames. SPI data is added to the RX FIFO at the completion of a transfer when the received data in the shift register is transferred into the RX FIFO. SPI data is removed (popped) from the RX FIFO by reading the DSPI*x*_POPR register. RX FIFO entries can only be removed from the RX FIFO by reading the DSPI*x*_POPR or by flushing the RX FIFO.

See Section 20.3.2.7, "DSPI POP RX FIFO Register (DSPIx_POPR)" for more information on the DSPI*x*_POPR.

The RX FIFO counter field (RXCTR) in the DSPI status register (DSPI*x*_SR) indicates the number of valid entries in the RX FIFO. The RXCTR is updated every time the DSPI _POPR is read or SPI data is copied from the shift register to the RX FIFO.

The POPNXTPTR field in the DSPI*x*_SR points to the RX FIFO entry that is returned when the DSPI*x*_POPR is read. The POPNXTPTR contains the positive, 32-bit word offset from DSPI*x*_RXFR0. For example, POPNXTPTR equal to two means that the DSPI*x*_RXFR2 contains the received SPI data that is returned when DSPI*x*_POPR is read. The POPNXTPTR field is incremented every time the DSPI*x*_POPR is read. POPNXTPTR rolls over every four frames on the MCU.

20.4.3.5.1 Filling the RX FIFO

The RX FIFO is filled with the received SPI data from the shift register. While the RX FIFO is not full, SPI frames from the shift register are transferred to the RX FIFO. Every time an SPI frame is transferred to the RX FIFO the RX FIFO counter is incremented by one.

If the RX FIFO and shift register are full and a transfer is initiated, the RFOF bit in the DSPI*x*_SR is set indicating an overflow condition. Depending on the state of the ROOE bit in the DSPI*x*_MCR, the data from the transfer that generated the overflow is ignored or put in the shift register. If the ROOE bit is set, the incoming data is put in the shift register. If the ROOE bit is cleared, the incoming data is ignored.

20.4.3.5.2 Draining the RX FIFO

Host software or the eDMA can remove (pop) entries from the RX FIFO by reading the DSPI*x*_POPR. A read of the DSPI*x*_POPR decrements the RX FIFO counter by one. Attempts to pop data from an empty RX FIFO are ignored, the RX FIFO counter remains unchanged. The data returned from reading an empty RX FIFO is undetermined.

See Section 20.3.2.7, "DSPI POP RX FIFO Register (DSPIx_POPR)" for more information on DSPI*x*_POPR.

When the RX FIFO is not empty, the RX FIFO drain flag (RFDF) in the DSPI*x*_SR is set. The RFDF bit is cleared when the RX_FIFO is empty and the eDMA controller indicates that a read from DSPI*x*_POPR is complete; alternatively the RFDF bit can be cleared by the host writing a 1 to it.

20.4.4 Deserial Serial Interface (DSI) Configuration

The DSI configuration supports pin count reduction by serializing parallel input signals or register bits and shifting them out in an SPI-like protocol. The received serial frames are converted to a parallel form (deserialized) and placed on the parallel output signals or in a register. The various features of the DSI configuration are set in the DSPI*x*_DSICR. For more information on the DSPI*x*_DSICR. The DSPI is in DSI configuration when the DCONF field in the DSPI*x*_MCR is 0b01.

See Section 20.4.7, "Transfer Formats" for a description of the timing and transfer protocol.

See Section 20.3.2.10, "DSPI DSI Configuration Register (DSPIx_DSICR)."

The DSI frames can be from 4 to 16 bits long. With multiple transfer operation (MTO), the DSPI supports serial chaining of DSPI modules within the MCU to create DSI frames consisting of concatenated bits from multiple DSPIs. The DSPI also supports parallel chaining allowing several DSPIs and off-chip SPI devices to share the same serial communications clock (SCK) and peripheral chip select (PCS) signals.

See Section 20.4.4.7, "Multiple Transfer Operation (MTO)," for details on the serial and parallel chaining support.

20.4.4.1 DSI Master Mode

In DSI master mode the DSPI initiates and controls the DSI transfers. The DSI master has four different conditions that can initiate a transfer:

- Continuous
- Change in data
- Trigger signal
- Trigger signal combined with a change in data

The four transfer initiation conditions are described in Section 20.4.4.5, "DSI Transfer Initiation Control." Transfer attributes are set during initialization. The DSICTAS field in the DSPI*x*_DSICR determines which of the DSPI*x*_CTARs controls the transfer attributes.

20.4.4.2 DSI Slave Mode

In DSI slave mode the DSPI responds to transfers initiated by an SPI or DSI bus master. In this mode the DSPI does not initiate DSI transfers. Certain transfer attributes such as clock polarity and phase must be set for successful communication with a DSI master. The DSI slave mode transfer attributes are set in the DSPI*x*_CTAR1.

If the CID bit in the DSPI*x*_DSICR is set and the data in the DSPI*x*_COMPR differs from the selected source of the serialized data, the slave DSPI asserts the $\overline{\text{MTRIG}}$ signal. If the slave's internal hardware trigger signal is asserted and the TRRE is set, the slave DSPI asserts $\overline{\text{MTRIG}}$. These features are included to support chaining of several DSPI. Details about the $\overline{\text{MTRIG}}$ signal are found in Section 20.4.4.7, "Multiple Transfer Operation (MTO)."

20.4.4.3 DSI Serialization

In the DSI configuration, 4 to 16 bits can be serialized using two different sources. The TXSS bit in the DSPI*x*_DSICR selects between the DSPI*x*_SDR and DSPI*x*_ASDR as the source of serialized data. See Section 20.3.2.11, "DSPI DSI Serialization Data Register (DSPIx_SDR)," and Section 20.3.2.12, "DSPI DSI Alternate Serialization Data Register (DSPIx_ASDR)," for more details. The DSPI*x*_SDR holds the latest parallel input signal values which is sampled at every rising edge of the system clock. The DSPI*x*_ASDR is written by host software and used as an alternate source of serialized data.

A copy of the last DSI frame shifted out of the shift register is stored in the DSPI*x*_COMPR. This register provides added visibility for debugging and it serves as a reference for transfer initiation control. Section 20.3.2.13, "DSPI DSI Transmit Comparison Register (DSPIx_COMPR)," contains details on the DSPI*x*_COMPR.

Figure 20-19 shows the DSI serialization logic.

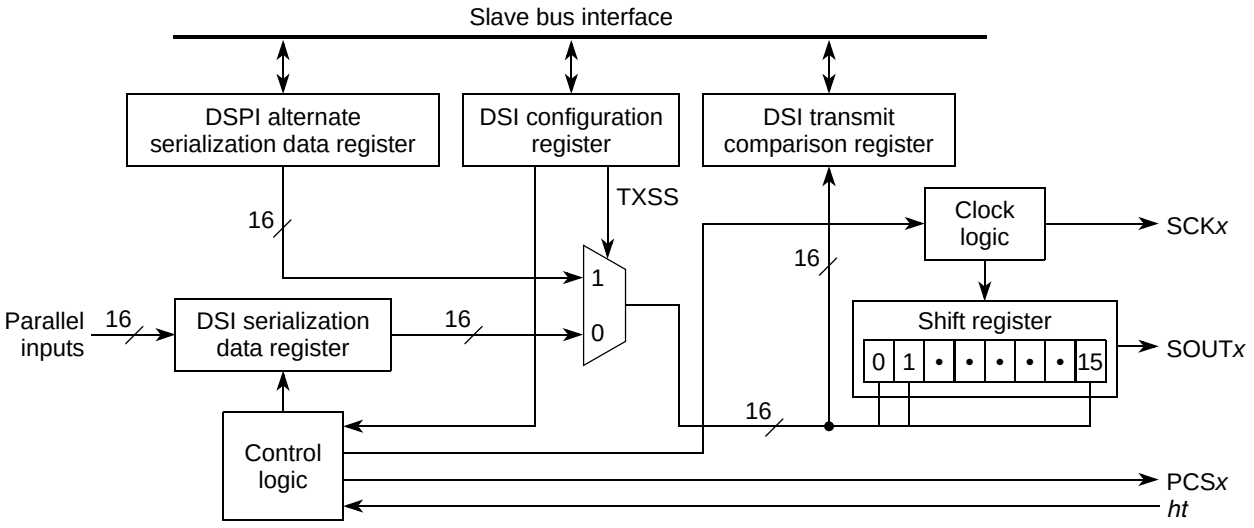


Figure 20-19. DSI Serialization Diagram

20.4.4.4 DSI Deserialization

When all bits in a DSI frame have been shifted in, the frame is copied to the DSPI*x*_DDR. This register presents the deserialized data as parallel output signal values. The DSPI*x*_DDR is memory mapped to allow host software to read the deserialized data directly. Figure 20-20 shows the DSI deserialization logic. for more information on the DSPI*x*_DDR.

See Section 20.3.2.14, "DSPI DSI Deserialization Data Register (DSPIx_DDR)."

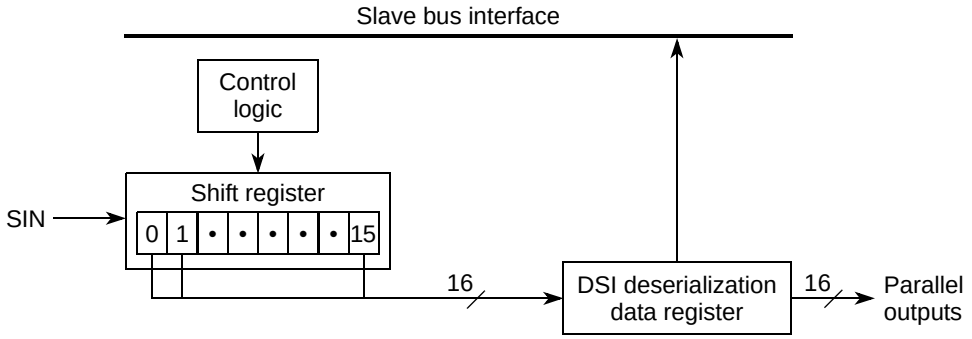


Figure 20-20. DSI Deserialization Diagram

20.4.4.5 DSI Transfer Initiation Control

Data transfers for a master DSPI in DSI configuration are initiated by a condition. When chaining DSPIs, the master and all slaves must be configured for the transfer initiation. The transfer initiation conditions are selected by the TRRE and CID bits in the DSPI*x*_DSICR.

Table 20-18 lists the four transfer initiation conditions.

Table 20-18. DSI Data Transfer Initiation Control

DSPI*x*_DSICR Bits		Type of Transfer Initiation Control
TRRE	CID	
0	0	Continuous
0	1	Change in data
1	0	Triggered
1	1	Triggered or change in data

20.4.4.5.1 Continuous Control

For continuous control, the initiation of a transfer is based on the baud rate at which data is transferred between the DSPI and the external device. The baud rate is set in the DSPI*x*_CTAR selected by the DSICTAS field in the DSPI*x*_DSICR. A new DSI frame shifts out when the previous transfer cycle has completed and the delay after transfer (t_{DT}) has elapsed.

20.4.4.5.2 Change In Data Control

For change in data control, a transfer is initiated when the data to be serialized has changed since the transfer of the last DSI frame. A copy of the previously transferred DSI data is stored in the DSPI*x*_COMPR. When the data in the DSPI*x*_SDR or the DSPI*x*_ASDR is different from the data in the DSPI*x*_COMPR, a new DSI frame is transmitted. The TXSS bit in the DSPI*x*_DSICR selects which register the DSPI*x*_COMPR is compared to. The $\overline{\text{MTRIG}}$ output signal is asserted every time a change in data is detected.

20.4.4.5.3 Triggered Control

For triggered control, initiation of a transfer is controlled by the internal hardware trigger signal (*ht*). The TPOL bit in the DSPI*x*_DSICR selects the active edge of *ht*. For *ht* to have any affect, the TRRE bit in the DSPI*x*_DSICR must be set.

20.4.4.5.4 Triggered or Change In Data Control

For triggered or change in data control, initiation of a transfer is controlled by the *ht* signal or by the detection of a change in data to be serialized.

20.4.4.6 DSPI Connections to eTPUA, eTPUB, eMIOS and SIU

The four DSPI blocks connect to the input and output channels of the eTPUs and the eMIOS. The MCU connects to eTPUA, eTPUB, eMIOS, and SIU. Some of the DSPI outputs connect to the external interrupt input multiplexing subblock in the SIU. See Section 6.4.3, “External Interrupt,” and Section 19.4.3.4, “External Trigger Event Detection,” for details on how the DSPI deserialized outputs can be used to trigger external interrupt requests and Section 18.3.2, “Output and Input Channel Signals” for a discussion on eTPU connections.

20.4.4.6.1 DSPI A Connectivity

The DSPI A connects to the eTPUB as shown in Figure 20-21.

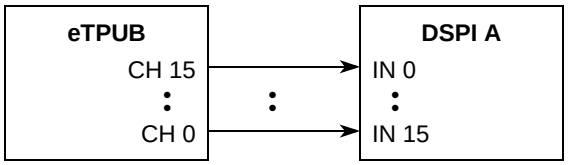


Figure 20-21. DSPI A Connectivity

Table 20-19 lists the DSPI A connections.

Table 20-19. DSPI A Connectivity Table

Connected to:	DSPI A IN[*n*]
eTPUB Output Channel 15	0
eTPUB Output Channel 14	1

DSPI A OUT[*n*]	Connected to:
0	N/C[1]
1	N/C

Table 20-19. DSPI A Connectivity Table (continued)

Connected to:	DSPI A IN[*n*]	DSPI A OUT[*n*]	Connected to:
eTPUB Output Channel 13	2	2	N/C
eTPUB Output Channel 12	3	3	N/C
eTPUB Output Channel 11	4	4	N/C
eTPUB Output Channel 10	5	5	N/C
eTPUB Output Channel 9	6	6	N/C
eTPUB Output Channel 8	7	7	N/C
eTPUB Output Channel 7	8	8	N/C
eTPUB Output Channel 6	9	9	N/C
eTPUB Output Channel 5	10	10	N/C
eTPUB Output Channel 4	11	11	N/C
eTPUB Output Channel 3	12	12	N/C
eTPUB Output Channel 2	13	13	N/C
eTPUB Output Channel 1	14	14	N/C
eTPUB Output Channel 0	15	15	N/C

[1] Not connected

20.4.4.6.2 DSPI B Connectivity

The DSPI B connects to the eMIOS, eTPUA, and SIU as shown in Figure 20-23.

Figure 20-22. eMIOS and DSPI B Connectivity

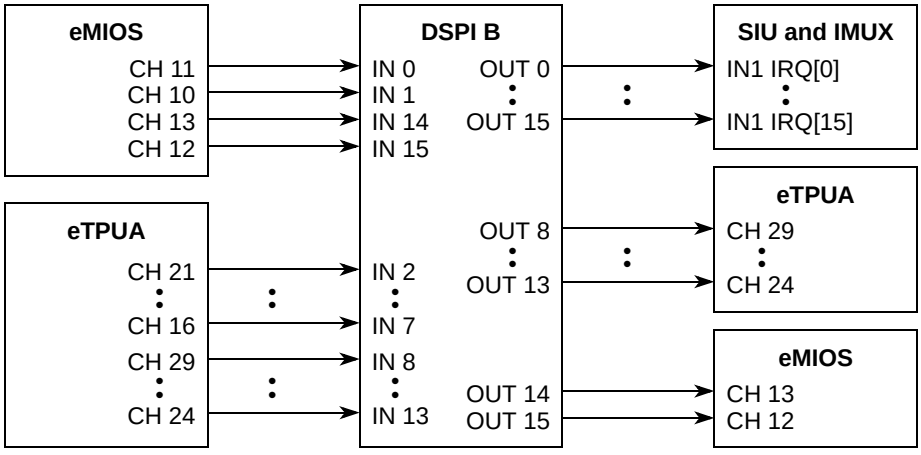


Figure 20-23. eMIOS, eTPUA and DSPI B Connectivity

Table 20-20. eMIOS, eTPUA, and DSPI B Connectivity

Connected to:	DSPI B IN[*n*]
eMIOS output channel 11	0
eMIOS output channel 10	1
eTPUA output channel 21	2
eTPUA output channel 20	3
eTPUA output channel 19	4
eTPUA output channel 18	5
eTPUA output channel 17	6
eTPUA output channel 16	7
eTPUA output channel 29	8
eTPUA output channel 28	9
eTPUA output channel 27	10
eTPUA output channel 26	11
eTPUA output channel 25	12
eTPUA output channel 24	13
eMIOS output channel 13	14
eMIOS output channel 12	15

DSPI B OUT[*n*]	Connected to:
0	Input 1 on IMUX for external $\overline{\text{IRQ}}$[0]
1	Input 1 on IMUX for external $\overline{\text{IRQ}}$[1]
2	Input 1 on IMUX for external $\overline{\text{IRQ}}$[2]
3	Input 1 on IMUX for external $\overline{\text{IRQ}}$[3]
4	Input 1 on IMUX for external $\overline{\text{IRQ}}$[4]
5	Input 1 on IMUX for external $\overline{\text{IRQ}}$[5]
6	Input 1 on IMUX for external $\overline{\text{IRQ}}$[6]
7	Input 1 on IMUX for external $\overline{\text{IRQ}}$[7]
8	eTPUA input channel 29, input 1 on IMUX for external $\overline{\text{IRQ}}$[8]
9	eTPUA input channel 28, input 1 on IMUX for external $\overline{\text{IRQ}}$[9]
10	eTPUA input channel 27, input 1 on IMUX for external $\overline{\text{IRQ}}$[10]
11	eTPUA input channel 26, input 1 on IMUX for external $\overline{\text{IRQ}}$[11]
12	eTPUA input channel 25, input 1 on IMUX for external $\overline{\text{IRQ}}$[12]
13	eTPUA input channel 24, input 1 on IMUX for external $\overline{\text{IRQ}}$[13]
14	eMIOS input channel 13, input 1 on IMUX for external $\overline{\text{IRQ}}$[14]
15	eMIOS input channel 12, input 1 on IMUX for external $\overline{\text{IRQ}}$[15]

20.4.4.6.3 DSPI C Connectivity

The DSPI C connects to the eTPUA and the SIU as shown in Figure 20-24.

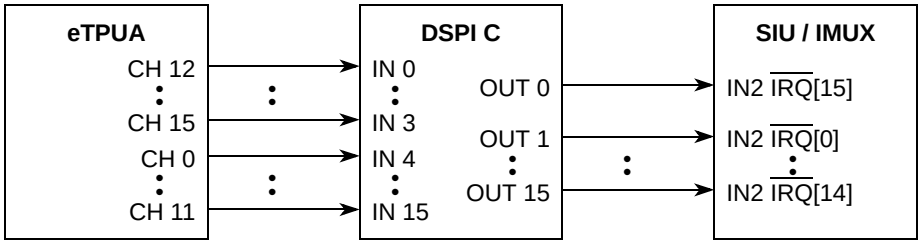


Figure 20-24. eTPUA and DSPI C Connectivity

Table 20-21 lists the eTPUA and DSPI C connections.

Table 20-21. eTPUA and DSPI C Connectivity

eTPU Channel	DSPI C IN[*n*]	DSPI C OUT[*n*]	Connected to:
eTPUA output channel 12	0	0	Input 2 on IMUX for external $\overline{\text{IRQ}}$[15]
eTPUA output channel 13	1	1	Input 2 on IMUX for external $\overline{\text{IRQ}}$[0]
eTPUA output channel 14	2	2	Input 2 on IMUX for external $\overline{\text{IRQ}}$[1]
eTPUA output channel 15	3	3	Input 2 on IMUX for external $\overline{\text{IRQ}}$[2]
eTPUA output channel 0	4	4	Input 2 on IMUX for external $\overline{\text{IRQ}}$[3]
eTPUA output channel 1	5	5	Input 2 on IMUX for external $\overline{\text{IRQ}}$[4]
eTPUA output channel 2	6	6	Input 2 on IMUX for external $\overline{\text{IRQ}}$[5]
eTPUA output channel 3	7	7	Input 2 on IMUX for external $\overline{\text{IRQ}}$[6]
eTPUA output channel 4	8	8	Input 2 on IMUX for external $\overline{\text{IRQ}}$[7]
eTPUA output channel 5	9	9	Input 2 on IMUX for external $\overline{\text{IRQ}}$[8]
eTPUA output channel 6	10	10	Input 2 on IMUX for external $\overline{\text{IRQ}}$[9]
eTPUA output channel 7	11	11	Input 2 on IMUX for external $\overline{\text{IRQ}}$[10]
eTPUA output channel 8	12	12	Input 2 on IMUX for external $\overline{\text{IRQ}}$[11]
eTPUA output channel 9	13	13	Input 2 on IMUX for external $\overline{\text{IRQ}}$[12]
eTPUA output channel 10	14	14	Input 2 on IMUX for external $\overline{\text{IRQ}}$[13]
eTPUA output channel 11	15	15	Input 2 on IMUX for external $\overline{\text{IRQ}}$[14]

20.4.4.6.4 DSPI D Connectivity

The DSPI D connects to the eTPUA, eMIOS and SIU as shown in Figure 20-25.

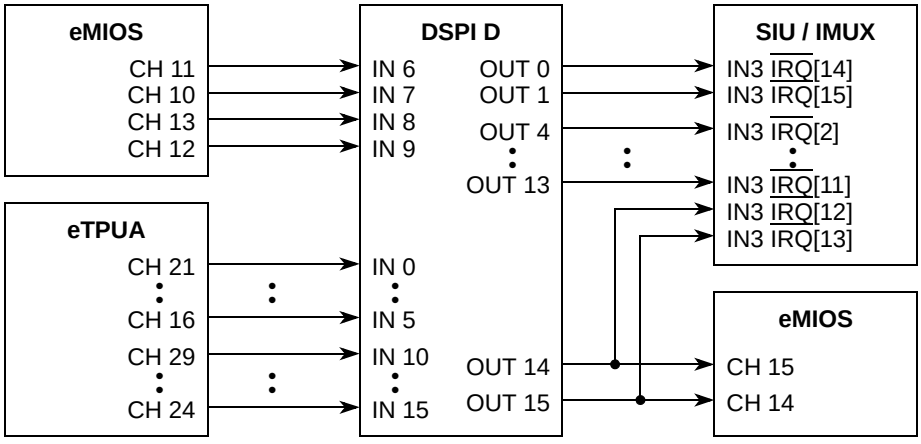


Figure 20-25. DSPI D Connectivity

Table 20-22 lists the DSPI D connections.

Table 20-22. DSPI D Connectivity Table

Connected to:	DSPI D IN[*n*]	DSPI D OUT[*n*]	Connected to:
eTPUA output channel 21	0	0	Input 3 on IMUX for external $\overline{\text{IRQ}}$[14]
eTPUA output channel 20	1	1	Input 3 on IMUX for external $\overline{\text{IRQ}}$[15]
eTPUA output channel 19	2	2	no connect
eTPUA output channel 18	3	3	no connect
eTPUA output channel 17	4	4	Input 3 on IMUX for external $\overline{\text{IRQ}}$[2]
eTPUA output channel 16	5	5	Input 3 on IMUX for external $\overline{\text{IRQ}}$[3]
eMIOS output channel 11	6	6	Input 3 on IMUX for external $\overline{\text{IRQ}}$[4]
eMIOS output channel 10	7	7	Input 3 on IMUX for external $\overline{\text{IRQ}}$[5]
eMIOS output channel 13	8	8	Input 3 on IMUX for external $\overline{\text{IRQ}}$[6]
eMIOS output channel 12	9	9	Input 3 on IMUX for external $\overline{\text{IRQ}}$[7]
eTPUA output channel 29	10	10	Input 3 on IMUX for external $\overline{\text{IRQ}}$[8]
eTPUA output channel 28	11	11	Input 3 on IMUX for external $\overline{\text{IRQ}}$[9]
eTPUA output channel 27	12	12	Input 3 on IMUX for external $\overline{\text{IRQ}}$[10]
eTPUA output channel 26	13	13	Input 3 on IMUX for external $\overline{\text{IRQ}}$[11]
eTPUA output channel 25	14	14	eMIOS input channel 15, Input 3 on IMUX for external $\overline{\text{IRQ}}$[12]
eTPUA output channel 24	15	15	eMIOS input channel 14, Input 3 on IMUX for external $\overline{\text{IRQ}}$[13]

20.4.4.7 Multiple Transfer Operation (MTO)

In DSI configuration the MTO feature allows for multiple DSPIs within the MCU to be chained together in a parallel or serial configuration. The parallel chaining allows multiple DSPIs internal to the MCU and multiple SPI devices external to the MCU to share SCK and PCS signals thereby saving pins. The serial chaining allows bits from multiple DSPIs to be concatenated into a single DSI frame. MTO is enabled by setting the MTOE bit in the DSPI*x*_DSICR.

In parallel and serial chaining there is one bus master and multiple bus slaves. The bus master initiates and controls the transfers, but the DSPI slaves generate trigger signals for the bus DSPI master when an internal condition in the slave warrants a transfer. The DSPI slaves also propagate triggers from other slaves to the master. When a DSPI slave detects a trigger signal on its *ht* input, the slave generates a trigger signal on the $\overline{\text{MTRIG}}$ output.

The SIU_DISR must be configured to use serial or parallel chaining.

20.4.4.7.1 Internal Muxing and SIU Support for Serial and Parallel Chaining

To support MTO, each DSPI in the device has multiplexers on the SIN*x*, SS*x*, SCK*x*, and *ht* inputs. The internal multiplexers are controlled by registers in the SIU block.

See Section 6.4.5.3, “Multiplexed Inputs for DSPI Multiple Transfer Operation.”

Figure 20-26 shows DSPI A and the multiplexers in the IMUX subblock of the SIU. The SOUT*x*,$\overline{\text{MTRIG}}$, SCK*x* and PCS*x*0 outputs from the other three DSPIs connect to the multiplexers on the DSPI A inputs.

DSPI B, DSPI C and DSPI D have similar multiplexers on their inputs.

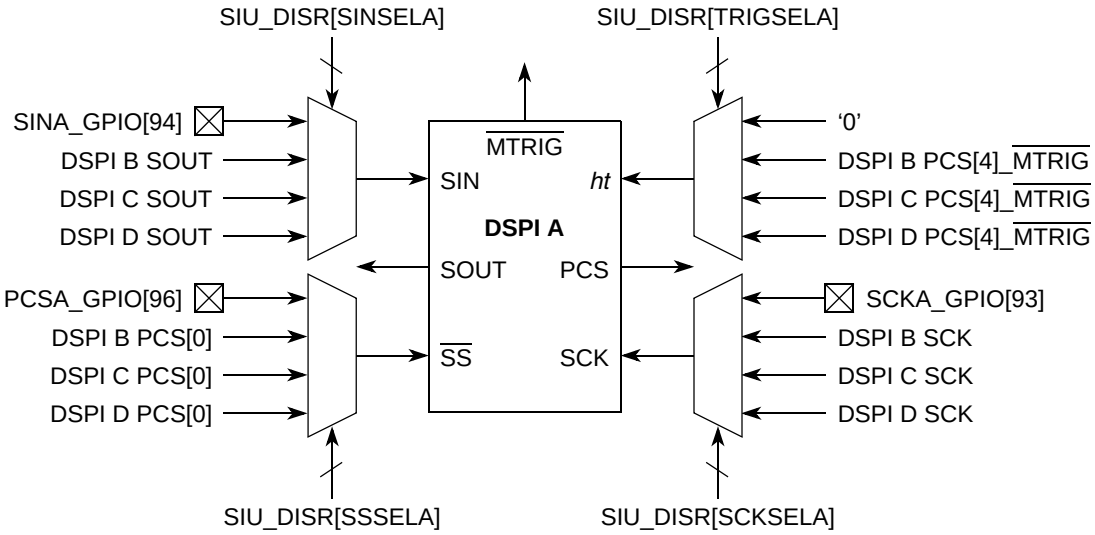


Figure 20-26. DSPI A, B, C, and D Inputs for Multi-transfer Operations

The source for the SIN*x* input of a DSPI can be a pin or the SOUT*x* of any of the other three DSPIs. The source for the $\overline{\text{SS}}$*x* input of a DSPI can be a pin or the PCS*x*[0] signal from any of the other DSPIs. The source for the SCK*x* input of a DSPI can be a pin or the SCK*x* output of any of the other DSPIs. The source for the hardware trigger (*ht*) input can be the $\overline{\text{MTRIG}}$ signal from any of the other DSPIs. The DSPI input select register (SIU_DSR) selects the source for each DSPI SIN*x*, $\overline{\text{SS}}$*x*, SCK*x*, and *ht* signal individually.

20.4.4.7.2 Parallel Chaining

Parallel chaining allows the PCS*x* and SCK*x* signals from a master DSPI to be shared by internal slave DSPIs and external slave SPI devices. Signal sharing reduces DSPI pin utilization. An example of a parallel chain is shown in Figure 20-27.

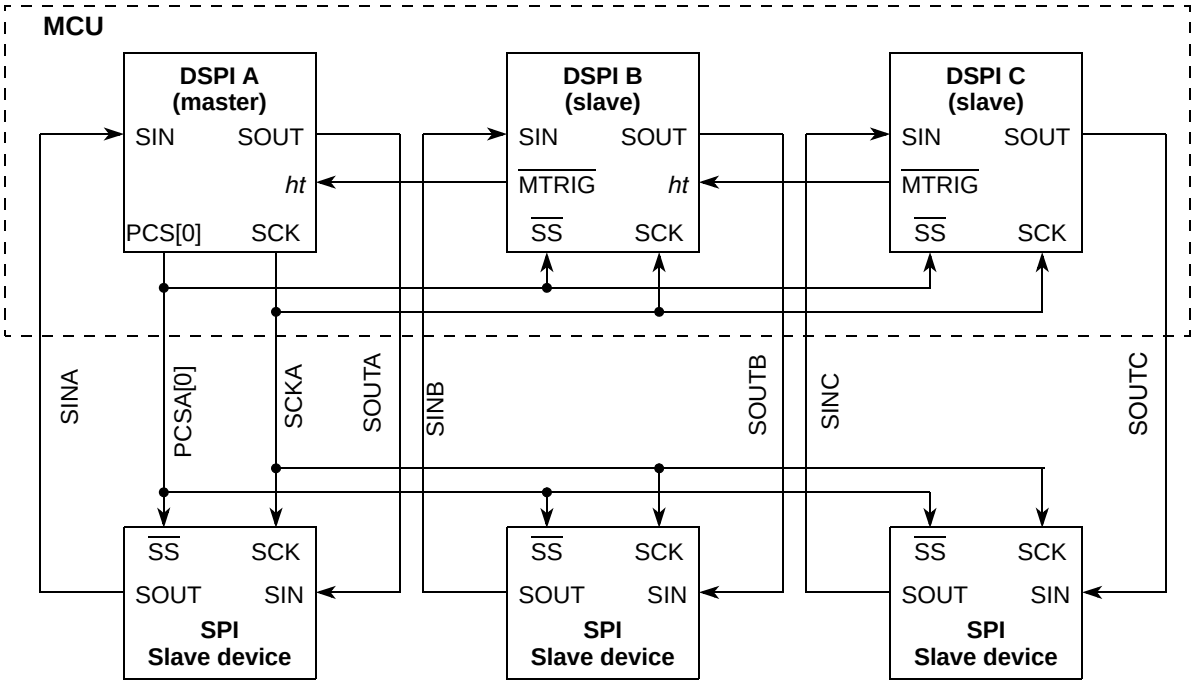


Figure 20-27. Example of Parallel Chaining of DSPI A, B, C and D

In the parallel chaining example, the SOUT*x* and SIN*x* of the DSPIs connect to separate external SPI devices. All internal and external SPI modules share PCS*x* and SCK*x* signals. DSPI A controls and initiates all transfers, but the DSPI slaves each have a trigger output signal $\overline{\text{MTRIG}}$ that indicates to DSPI A that a trigger condition has occurred in the DSPI slaves.

When the slave DSPI has a change in data to be serialized, it asserts the $\overline{\text{MTRIG}}$ signal that propagates to DSPI A which initiates the transfer. DSPI B propagates trigger signals from DSPI C to DSPI A.DSPI C propagates trigger signals from DSPI D to DSPI B.

The MTOCNT field in the DSPI*x*_DSICR must be written with the number of bits to be transferred. In parallel chaining the number written to MTOCNT must match the FMSZ field in the selected DSPI*x*_CTAR.

20.4.4.7.3 Serial Chaining

Serial chaining allows transfers of DSI frames consisting of concatenated bits from multiple DSPIs. The concatenated frames can be from 8- to 64-bits long. Figure 20-28 shows an example of how the modules can be connected.

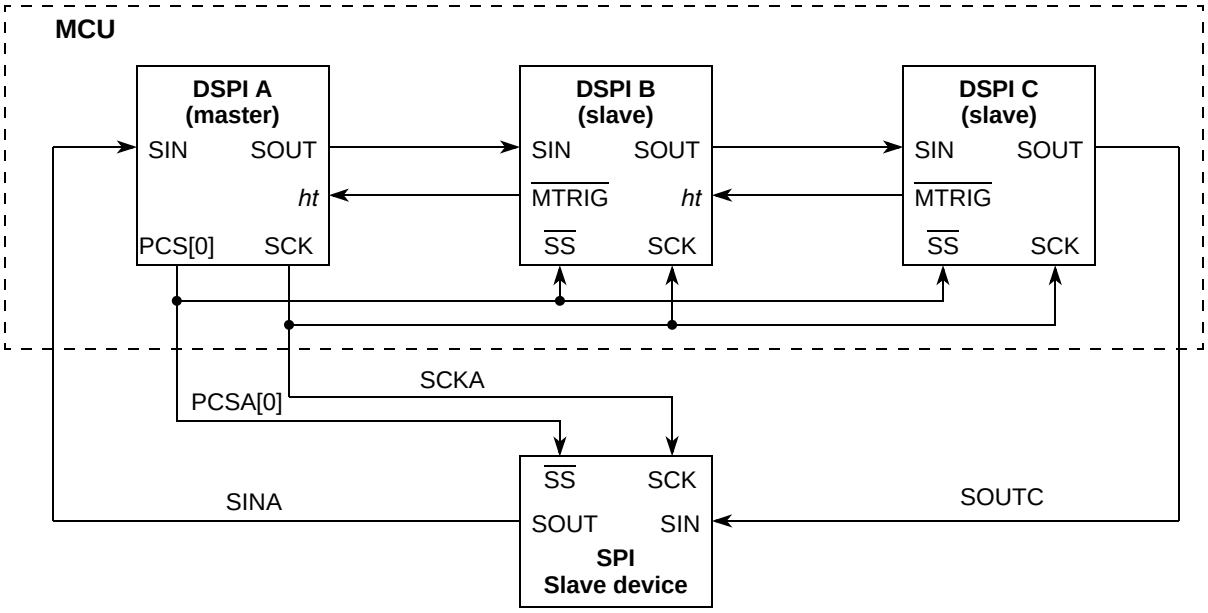


Figure 20-28. Example of Serial Chaining of DSPI A, B, C and D

In the MCU (master), the SOUT of DSPI A is connected to the SIN of DSPI B (slave). The SOUT of the DSPI B (slave) is connected to the SIN input of the DSPI C and so on (slave). The SOUT of the last on-chip DSPI slave is connected to the SIN of the external SPI slave. The SOUT of the external SPI slave is connected to the SIN of DSPI_A master.

The DSPI A master controls and initiates all transfers, but the slave DSPIs use the trigger output signal $\overline{\text{MTRIG}}$ to indicate to the DSPI_A master that a trigger condition has occurred. When an on-chip DSPI slave has a change in data to be serialized it can assert the $\overline{\text{MTRIG}}$ signal to the DSPI master which initiates the transfer. When a DSPI slave has its *ht* signal asserted, its $\overline{\text{MTRIG}}$ signal asserts and propagates trigger signals from other DSPI slaves to the DSPI master.

The MTOCNT field in the DSPI*x*_DSICR must be written with the total number of bits to be transferred. The MTOCNT field must equal the sum of all FMSZ fields in the selected DSPI*x*_CTARs for the DSPI master and all DSPI slaves. For example if one 16-bit DSI frame is created by concatenating 8 bits from the DSPI master, and 4 bits from each of the DSPI slaves in Figure 20-28, the DSPI master's frame size must be set to eight in the FMSZ field, and the DSPI slaves' frame size must be set to four. The largest DSI frame supported by the MTOCNT field is64 bits. Any number of DSPIs can be connected together to concatenate DSI frames, as long as each DSPI transfers a minimum of 4 bits and a maximum of 16 bits and the total size of the concatenated frame is less than or equal to64 bits long.

20.4.5 Combined Serial Interface (CSI) Configuration

In master mode, the CSI configuration of the DSPI is used to support SPI and DSI functions on a frame by frame basis. CSI configuration allows interleaving of DSI data frames from the parallel input signals (from the eTPU or eMIOS) with SPI commands and data from the TX FIFO. The data returned from the bus slave is either used to drive the parallel output signals (to the eTPU or eMIOS) or is stored in the RX FIFO. CSI configuration allows serialized data and configuration or diagnostic data to be transferred to a slave device using only one serial link. The DSPI is in CSI configuration when the DCONF field in the DSPI*x*_MCR is 0b10. Figure 20-29 shows an example of how a DSPI can be used with a deserializing peripheral that supports SPI control for control and diagnostic frames.

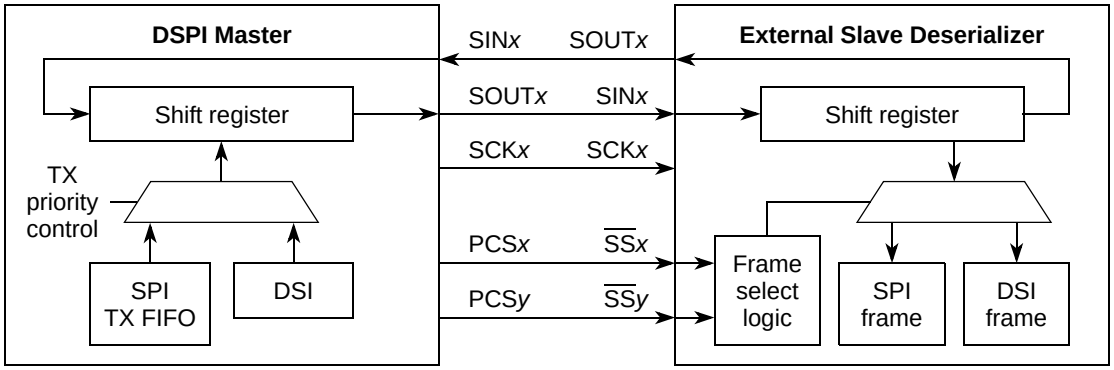


Figure 20-29. Example of System using DSPI in CSI Configuration

In CSI configuration the DSPI transfers DSI data based on Section 20.4.4.5, “DSI Transfer Initiation Control.” When there are SPI commands in the TX FIFO, the SPI data has priority over the DSI frames. When the TX FIFO is empty, DSI transfer resumes.

Two peripheral chip select signals indicate whether DSI data or SPI data is transmitted. You must configure the DSPI so the CTARs for the DSI data and SPI data assert different peripheral chip select signals denoted in the figure as PCSx and PCSy. The CSI configuration is only supported in master mode.

Data returned from the external slave while a DSI frame is transferred is placed on the parallel output signals. Data returned from the external slave while an SPI frame is transferred is moved to the RX FIFO. The TX FIFO and RX FIFO are fully functional in CSI mode.

20.4.5.1 CSI Serialization

Serialization in the CSI configuration is similar to serialization in DSI configuration. The transfer attributes for SPI frames are determined by the DSPI*x*_CTAR selected by the CTAS field in the SPI command halfword. The transfer attributes for the DSI frames are determined by the DSPI*x*_CTAR selected by the DSICTAS field in the DSPI*x*_DSICR. Figure 20-30 shows the CSI serialization logic.

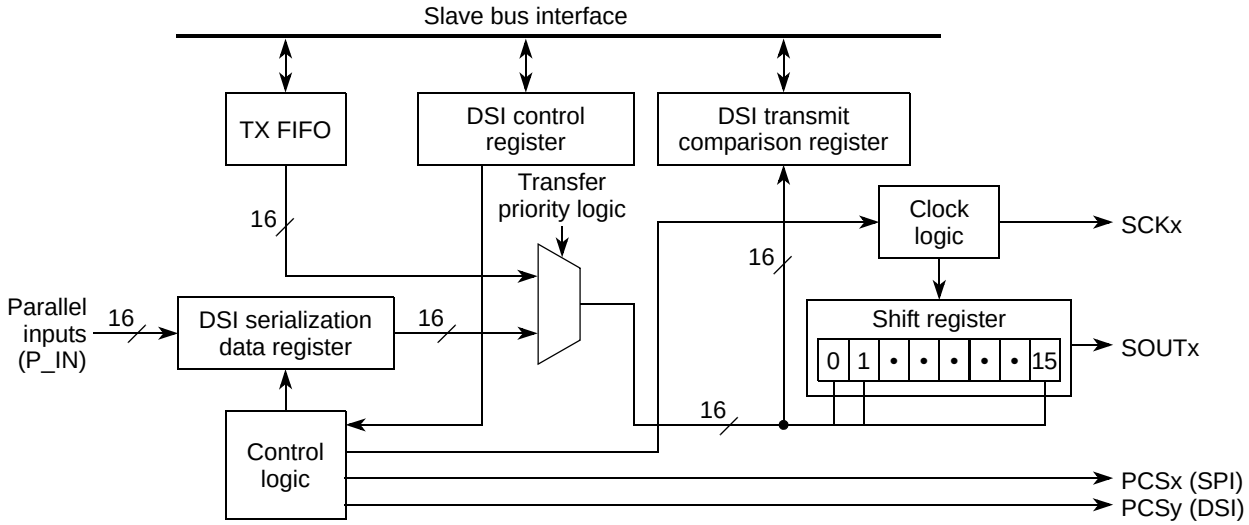


Figure 20-30. CSI Serialization Diagram

The parallel inputs signal states are latched into the DSPI*x*_SDR on the rising edge of every system clock and serialized based on the transfer initiation control settings in the DSPI*x*_DSICR. For more information on the DSPI*x*_SDR. SPI frames written to the TX FIFO have priority over DSI data from the DSPI*x*_SDR and are transferred at the next frame boundary. A copy of the most recently transferred DSI frame is stored in the DSPI*x*_COMPR. The transfer priority logic selects the source of the serialized data and asserts the chip select signal.

See Section 20.3.2.11, "DSPI DSI Serialization Data Register (DSPIx_SDR)."

20.4.5.2 CSI Deserialization

The deserialized frames in CSI configuration go into the DSPI*x*_SDR or the RX FIFO based on the transfer priority logic. When DSI frames are transferred the returned frames are deserialized and latched into the DSPI*x*_DDR. When SPI frames are transferred the returned frames are deserialized and written to the RX FIFO.

Figure 20-31 shows the CSI deserialization logic.

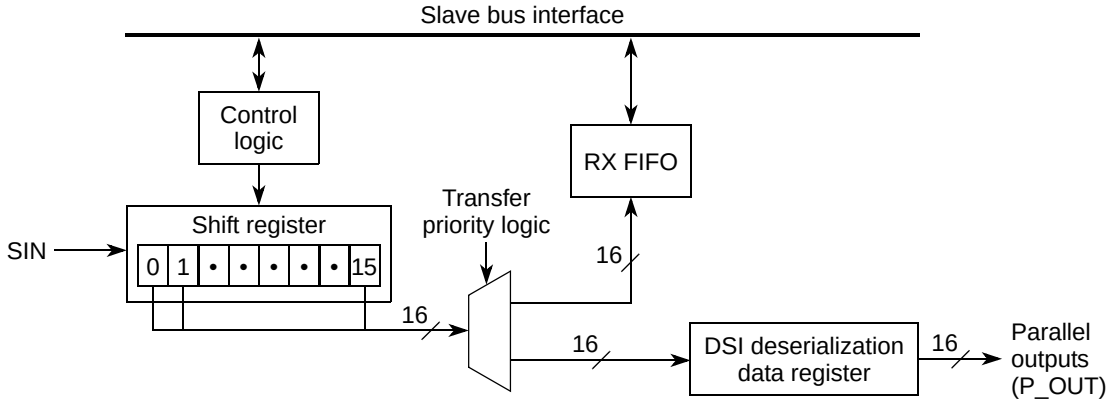


Figure 20-31. CSI Deserialization Diagram

20.4.6 DSPI Baud Rate and Clock Delay Generation

The SCK*x* frequency and the delay values for serial transfer are generated by dividing the system clock frequency by a prescaler and a scaler with the option of doubling the baud rate.

Figure 20-32 shows conceptually how the SCK signal is generated.

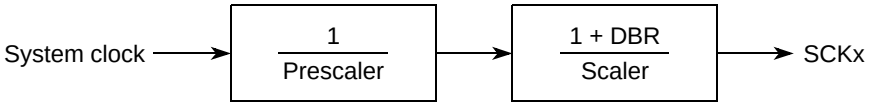


Figure 20-32. Communications Clock Prescalers and Scalers

20.4.6.1 Baud Rate Generator

The baud rate is the frequency of the serial communication clock (SCK*x*). The system clock is divided by a baud rate prescaler (defined by DSPI*x*_CTAR[PBR]) and baud rate scaler (defined by DSPI*x*_CTAR[BR]) to produce SCK*x* with the possibility of doubling the baud rate. The DBR, PBR, and BR fields in the DSPI*x*_CTARs select the frequency of SCK*x* using the following formula:

$$\text{SCK baud rate} = \frac{f_{SYS}}{\text{PBRPrescalerValue}} \times \frac{1 + \text{DBR}}{\text{BRScalerValue}}$$

Table 20-23 shows an example of a computed baud rate.

Table 20-23. Baud Rate Computation Example

f_{SYS}	PBR	Prescaler Value	BR	Scaler Value	DBR Value	Baud Rate
100 MHz	0b00	2	0b0000	2	0	25 Mb/sec
20 MHz	0b00	2	0b0000	2	1	10 Mb/sec

20.4.6.2 PCS to SCK Delay (t_{CSC})

The PCS*x* to SCK*x* delay is the length of time from assertion of the PCS*x* signal to the first SCK*x* edge. See Figure 20-34 for an illustration of the PCS*x* to SCK*x* delay. The PCSSCK and CSSCK fields in the DSPI*x*_CTAR*n* registers select the PCS*x* to SCK*x* delay, and the relationship is expressed by the following formula:

$$t_{CSC} = \frac{1}{f_{SYS}} \times \text{PCSSCK} \times \text{CSSCK}$$

Table 20-24 shows an example of the computed PCS to SCK delay.

Table 20-24. PCS to SCK Delay Computation Example

PCSSCK	Prescaler Value	CSSCK	Scaler Value	f_{SYS}	PCS to SCK Delay
0b01	3	0b0100	32	100 MHz	0.96 µs

20.4.6.3 After SCK Delay (t_{ASC})

The after SCK*x* delay is the length of time between the last edge of SCK*x* and the negation of PCS*x*. See Figure 20-34 and Figure 20-35 for illustrations of the after SCK*x* delay. The PASC and ASC fields in the DSPI*x*_CTAR*n* registers select the after SCK delay. The relationship between these variables is given in the following formula:

$$t_{ASC} = \frac{1}{f_{SYS}} \times PASC \times ASC$$

Table 20-25 shows an example of the computed after SCK delay.

Table 20-25. After SCK Delay Computation Example

PASC	Prescaler Value	ASC	Scaler Value	f_{SYS}	After SCK Delay
0b01	3	0b0100	32	100 MHz	0.96 µs

20.4.6.4 Delay after Transfer (t_{DT})

The delay-after-transfer field is the amount of time between negation of the PCS*x* signal for a frame and the assertion of the PCS*x* signal for the next frame. The PDT and DT fields in the DSPI*x*_CTAR*n* registers select the delay after transfer.

See Figure 20-34 for an illustration of the delay after transfer. The following formula expresses the PDT and DT delay-after-transfer relationship:

$$t_{DT} = \frac{1}{f_{SYS}} \times PDT \times DT$$

Table 20-26 shows an example of the computed delay after transfer.

Table 20-26. Delay after Transfer Computation Example

PDT	Prescaler Value	DT	Scaler Value	f_{SYS}	Delay after Transfer
0b01	3	0b1110	32768	100 MHz	0.98 ms

20.4.6.5 Peripheral Chip Select Strobe Enable ($\overline{PCSS}$)

The $\overline{PCSS}$ signal provides a delay to allow the PCS*x* signals to settle after transitioning thereby avoiding glitches. When the DSPI is in master mode and PCSSE bit is set in the DSPI*x*_MCR, $\overline{PCSS}$ provides a signal for an external demultiplexer to decode the PCS*x*[0:4] signals into as many as 32 glitch-free PCS*x* signals.

Figure 20-33 shows the timing of the $\overline{\text{PCSS}}$ signal relative to PCS signals.

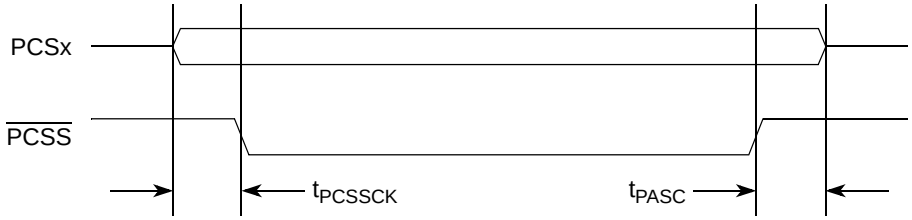


Figure 20-33. Peripheral Chip Select Strobe Timing

The delay between the assertion of the PCS*x* signals and the assertion of $\overline{\text{PCSS}}$ is selected by the PCSSCK field in the DSPI*x*_CTAR based on the following formula:

$$tPCSSCK = \frac{1}{f_{SYS}} \times PCSSCK$$

At the end of the transfer the delay between $\overline{\text{PCSS}}$ negation and PCS*x* negation is selected by the PASC field in the DSPI*x*_CTAR based on the following formula:

$$tPASC = \frac{1}{f_{SYS}} \times PASC$$

Table 20-27 shows an example of the computed t_{PCSSCK} delay.

Table 20-27. Peripheral Chip Select Strobe Assert Computation Example

PCSSCK	Prescaler	f_{SYS}	Delay before Transfer
0b11	7	100 MHz	70.0 ns

Table 20-28 shows an example of the computed the t_{PASC} delay.

Table 20-28. Peripheral Chip Select Strobe Negate Computation Example

PASC	Prescaler	f_{SYS}	Delay after Transfer
0b11	7	100 MHz	70.0 ns

20.4.7 Transfer Formats

The SPI serial communication is controlled by the serial communications clock (SCK*x*) signal and the PCS*x* signals. The SCK*x* signal provided by the master device synchronizes shifting and sampling of the data by the SIN*x* and SOUT*x* pins. The PCS*x* signals serve as enable signals for the slave devices.

When the DSPI is the bus master, the CPOL and CPHA bits in the DSPI clock and transfer attributes registers (DSPI*x*_CTAR*n*) select the polarity and phase of the serial clock, SCK*x*. The polarity bit selects the idle state of the SCK*x*. The clock phase bit selects if the data on SOUT*x* is valid before or on the first SCK*x* edge.

When the DSPI is the bus slave, CPOL and CPHA bits in the DSPI*x*_CTAR0 (SPI slave mode) or DSPI*x*_CTAR1 (DSI slave mode) select the polarity and phase of the serial clock. Even though the bus slave does not control the SCK signal, clock polarity, clock phase and number of bits to transfer must be identical for the master device and the slave device to ensure proper transmission.

The DSPI supports four different transfer formats:

- Classic SPI with CPHA = 0
- Classic SPI with CPHA = 1
- Modified transfer format with CPHA = 0
- Modified transfer format with CPHA = 1

A modified transfer format supports high-speed communication with peripherals that require longer setup times. The DSPI can sample the incoming data later than halfway through the cycle to give the peripheral more setup time. The MTFE bit in the DSPI*x*_MCR selects between classic SPI format and modified transfer format. The classic SPI formats are described in Section 20.4.7.1, “Classic SPI Transfer Format (CPHA = 0)” and Section 20.4.7.2, “Classic SPI Transfer Format (CPHA = 1).” The modified transfer formats are described in Section 20.4.7.3, “Modified Transfer Format Enabled (MTFE = 1) with Classic SPI Transfer Format Cleared (CPHA = 0) for SPI and DSI” and Section 20.4.7.4, “Modified Transfer Format Enabled (MTFE = 1) with Classic SPI Transfer Format Set (CPHA = 1) for SPI and DSI.”

In the SPI and DSI configurations, the DSPI provides the option of keeping the PCS signals asserted between frames. See Section 20.4.7.5, “Continuous Selection Format” for details.

20.4.7.1 Classic SPI Transfer Format (CPHA = 0)

The transfer format shown in Figure 20-34 is used to communicate with peripheral SPI slave devices where the first data bit is available on the first clock edge. In this format, the master and slave sample the SIN*x* pins on the odd-numbered SCK*x* edges, and change the data on the SOUT*x* pins on the even-numbered SCK*x* edges.

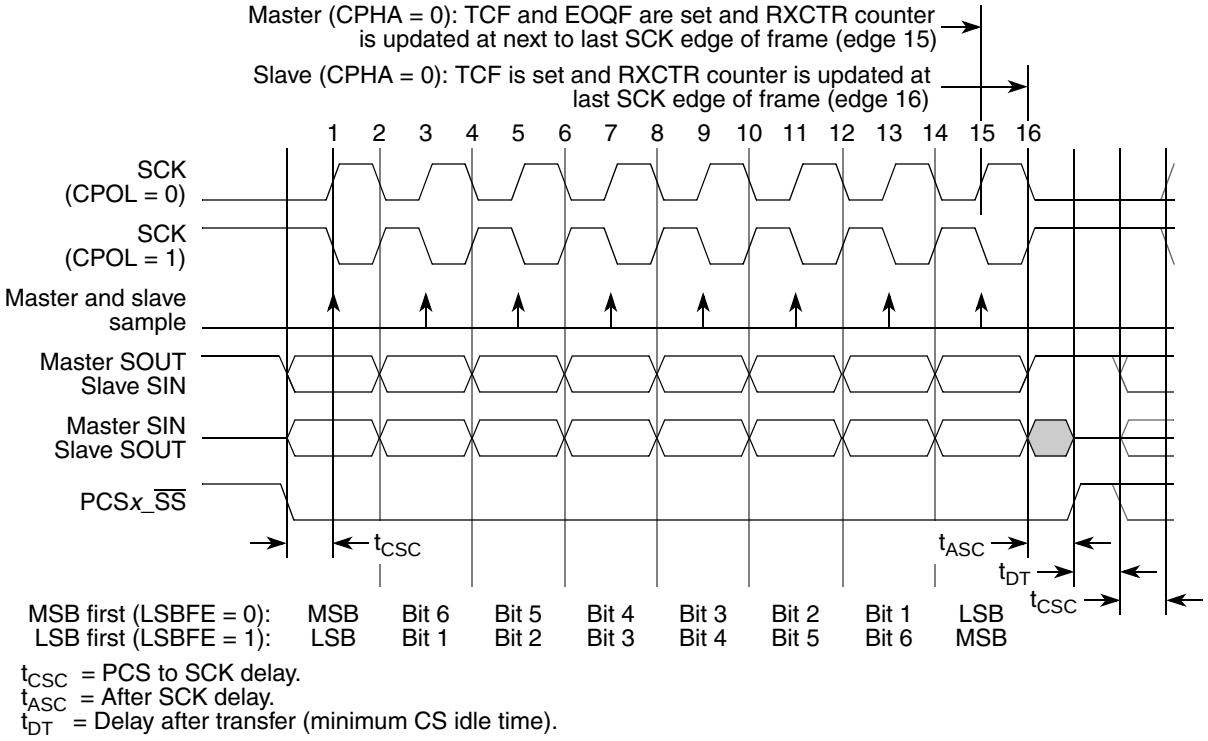


Figure 20-34. DSPI Transfer Timing Diagram (MTFE = 0, CPHA = 0, FMSZ = 8)

The master initiates the transfer by placing its first data bit on the SOUT*x* pin and asserting the appropriate peripheral chip select signals to the slave device. The slave responds by placing its first data bit on its SOUT*x* pin. After the t_{CSC} delay has elapsed, the master outputs the first edge of SCK*x*. This is the edge used by the master and slave devices to sample the first input data bit on their serial data input signals. At the second edge of the SCK*x* the master and slave devices place their second data bit on their serial data output signals. For the rest of the frame the master and the slave sample their SIN*x* pins on the odd-numbered clock edges and changes the data on their SOUT*x* pins on the even-numbered clock edges. After the last clock edge occurs a delay of t_{ASC} is inserted before the master negates the PCS signals. A delay of t_{DT} is inserted before a new frame transfer can be initiated by the master.

For the CPHA = 0 condition of the master, TCF and EOQF are set and the RXCTR counter is updated at the next to last serial clock edge of the frame (edge 15) of Figure 20-34.

For the CPHA = 0 condition of the slave, TCF is set and the RXCTR counter is updated at the last serial clock edge of the frame (edge 16) of Figure 20-34.

20.4.7.2 Classic SPI Transfer Format (CPHA = 1)

This transfer format shown in Figure 20-35 is used to communicate with peripheral SPI slave devices that require the first SCK*x* edge before the first data bit becomes available on the slave SOUT pin. In this format the master and slave devices change the data on their SOUT*x* pins on the odd-numbered SCK*x* edges and sample the data on their SIN*x* pins on the even-numbered SCK*x* edges.

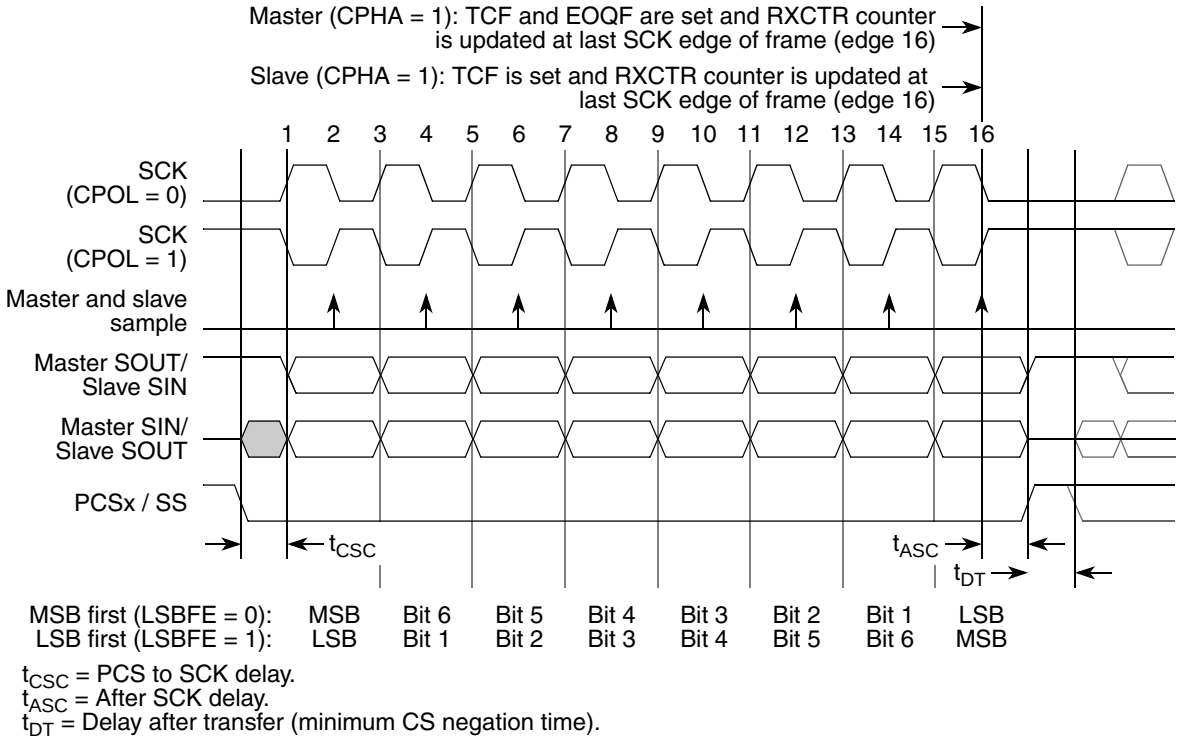


Figure 20-35. DSPI Transfer Timing Diagram (MTFE = 0, CPHA = 1, FMSZ = 8)

The master initiates the transfer by asserting the PCS*x* signal to the slave. After the t_{CSC} delay has elapsed, the master generates the first SCK*x* edge and at the same time places valid data on the master SOUT*x* pin. The slave responds to the first SCK*x* edge by placing its first data bit on its slave SOUT*x* pin.

At the second edge of the SCK*x* the master and slave sample their SIN*x* pins. For the rest of the frame the master and the slave change the data on their SOUT*x* pins on the odd-numbered clock edges and sample their SIN*x* pins on the even-numbered clock edges. After the last clock edge occurs a delay of t_{ASC} is inserted before the master negates the PCS*x* signal. A delay of t_{DT} is inserted before a new frame transfer can be initiated by the master.

For CPHA = 1 the master EOQF and TCF and slave TCF are set at the last serial clock edge (edge 16) of Figure 20-35. For CPHA = 1 the master and slave RXCTR counters are updated on the same clock edge.

20.4.7.3 Modified Transfer Format Enabled (MTFE = 1) with Classic SPI Transfer Format Cleared (CPHA = 0) for SPI and DSI

In the modified transfer format, the master and the slave sample later in the SCK period than in classic SPI mode to allow for delays in device pads and board traces. These delays become a more significant fraction of the SCK period as the SCK period decreases with increasing baud rates.

NOTE

For the modified transfer format to operate correctly, you must thoroughly analyze the SPI link timing budget.

The master and the slave send data to the SOUT*x* pins when the PCS*x* signal asserts. After the PCS*x* to SCK*x* delay elapses the first SCK*x* edge is generated. The slave samples the master SOUT*x* signal on every odd numbered SCK*x* edge. The slave also sends more data on the slave SOUT*x* on every odd numbered clock edge.

The master sends its second data bit to the SOUT*x* pin one system clock after the odd numbered SCK*x* edge. The master samples the slave SOUT*x* pins by writing to the SMPL_PT field in the DSPI*x*_MCR. Table 20-29 lists the number of system clock cycles (between the active-edge of SCK*x* and the master sample point) for different values of the SMPL_PT bit field. The master sample point can be delayed by one or two system clock cycles.

Table 20-29. Delayed Master Sample Point

SMPL_PT	Number of System Clock Cycles between Odd-numbered Edge of SCK and Sampling of SIN
00	0
01	1
10	2
11	Invalid value

Figure 20-36 shows the modified transfer format for CPHA = 0. Only the condition where CPOL = 0 is illustrated. The delayed master sample points are indicated with a lighter shaded arrow.

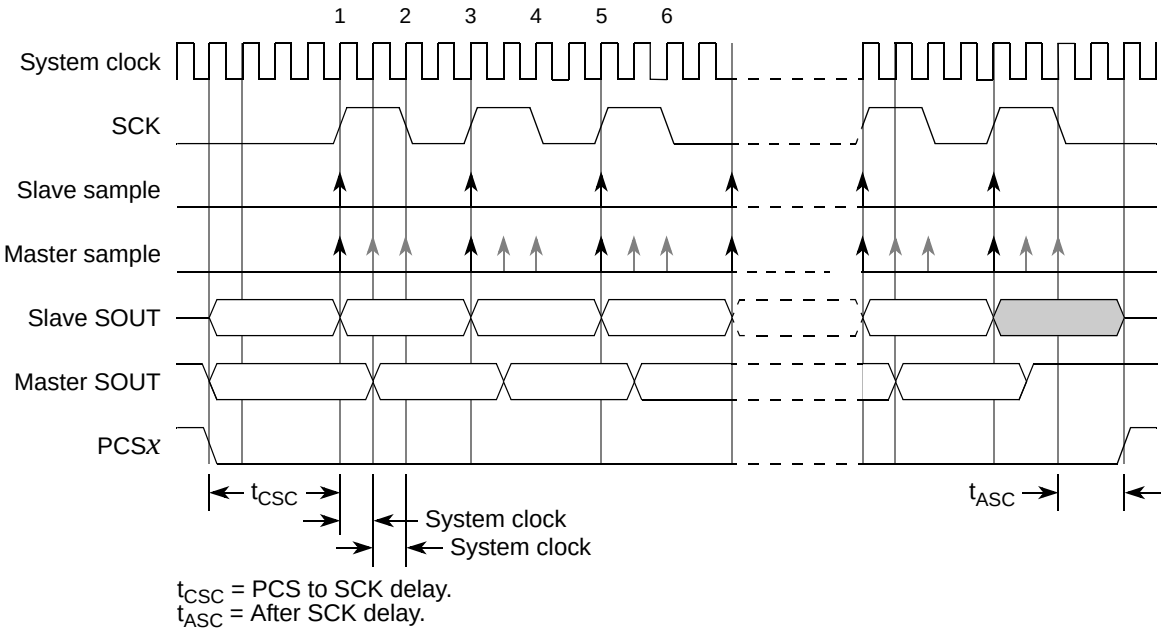


Figure 20-36. DSPI Modified Transfer Format (MTFE = 1, CPHA = 0, $f_{SCK} = f_{SYS} \div 4$)

20.4.7.4 Modified Transfer Format Enabled (MTFE = 1) with Classic SPI Transfer Format Set (CPHA = 1) for SPI and DSI

At the start of a transfer the DSPI asserts the PCS signal to the slave device. After the PCS to SCK delay has elapsed the master and the slave put data on their SOUT pins at the first edge of SCK. The slave samples the master SOUT signal on the even numbered edges of SCK. The master samples the slave SOUT signal on the odd numbered SCK edges starting with the third SCK edge. The slave samples the last bit on the last edge of the SCK. The master samples the last slave SOUT bit one half SCK cycle after the last edge of SCK. No clock edge is visible on the master SCK pin during the sampling of the last bit. The SCK-to-PCS delay must be greater or equal to half of the SCK period.

NOTE

For the modified transfer format to operate correctly, you must thoroughly analyze the SPI link timing budget.

Figure 20-37 shows the modified transfer format for CPHA = 1. Only the condition where CPOL = 0 is described.

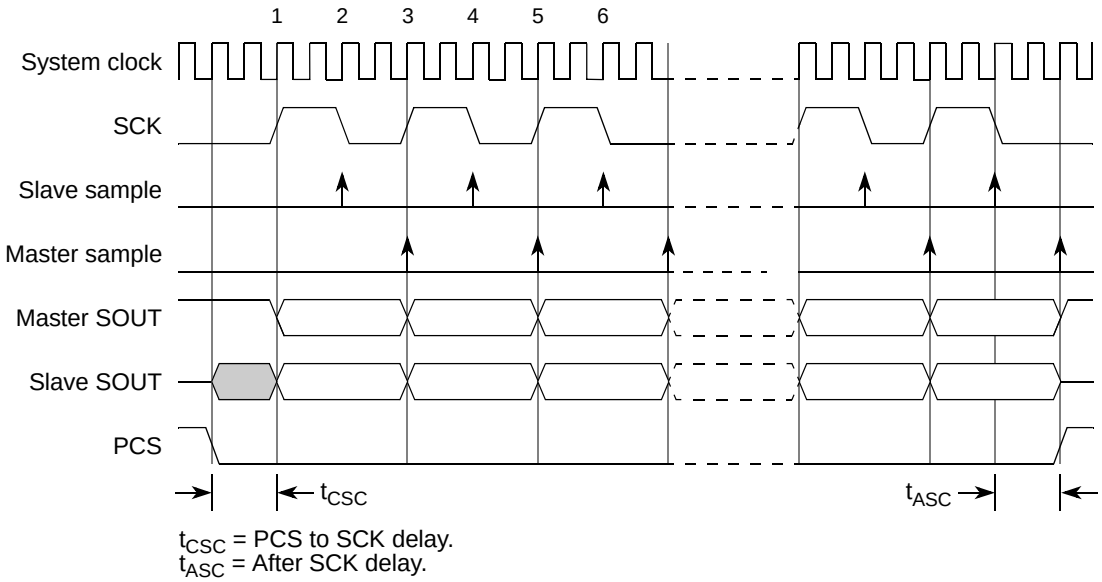


Figure 20-37. DSPI Modified Transfer Format (MTFE = 1, CPHA = 1, $f_{SCK} = f_{SYS} / 4$)

20.4.7.5 Continuous Selection Format

Some peripherals must be deselected between every transfer. Other peripherals must remain selected between several sequential serial transfers. The continuous selection format provides the flexibility to handle both cases. The continuous selection format is enabled for the SPI configuration by setting the CONT bit in the SPI command. Continuous selection is enabled for the DSI configuration by setting the DCONT bit in the DSPI*x*_DSICR. The behavior of the PCS signals in the two configurations is identical so only the SPI configuration is described.

When the CONT bit = 0, the DSPI drives the asserted chip select signals to their idle states in between frames. The idle states of the chip select signals are selected by the PCSIS field in the DSPI*x*_MCR.

Figure 20-38 shows the timing diagram for two four-bit transfers with CPHA = 1 and CONT = 0.

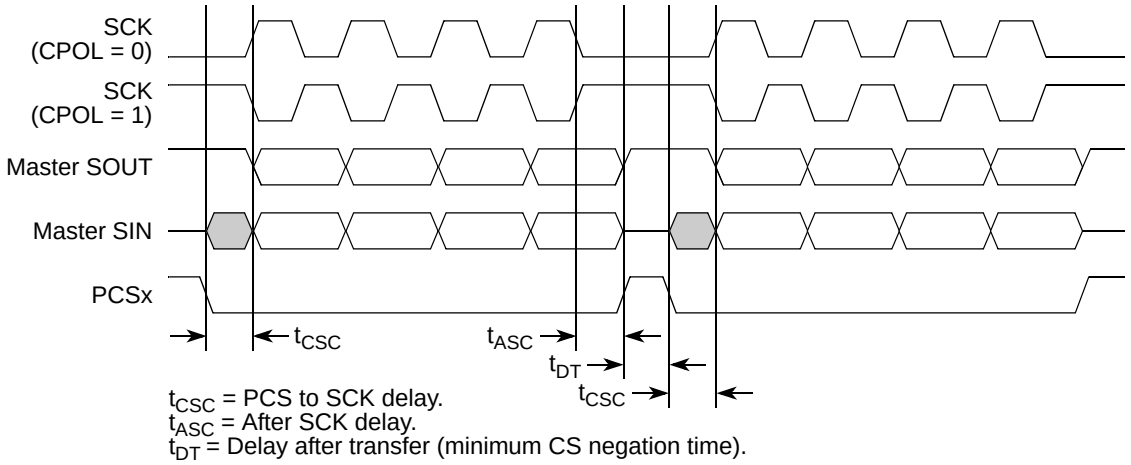


Figure 20-38. Example of Non-continuous Format (CPHA = 1, CONT = 0)

When the CONT = 1 and the PCS signal for the next transfer is the same as for the current transfer, the PCS signal remains asserted for the duration of the two transfers. The delay between transfers (t_{DT}) is not inserted between the transfers.

Figure 20-39 shows the timing diagram for two 4-bit transfers with CPHA = 1 and CONT = 1.

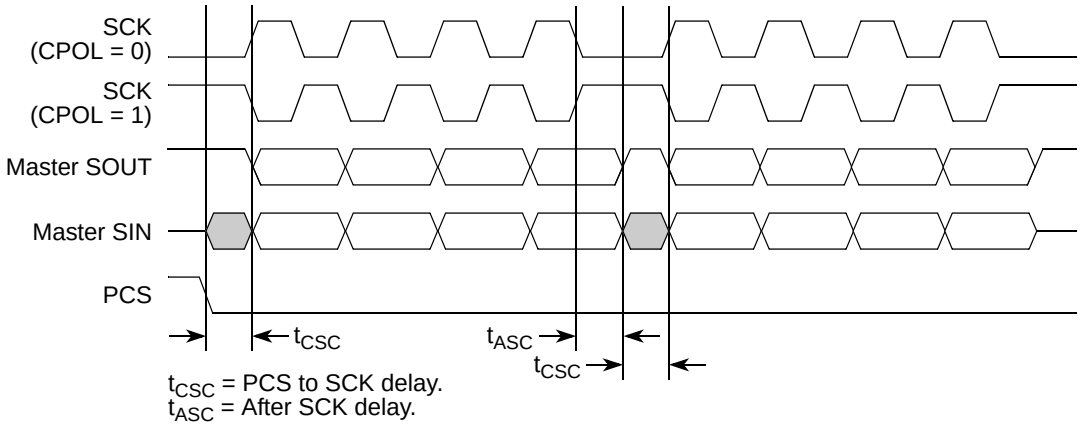


Figure 20-39. Example of Continuous Transfer (CPHA = 1, CONT = 1)

In Figure 20-39, the period length at the start of the next transfer is the sum of t_{ASC} and t_{CSC}; i.e., it does not include a half-clock period. The default settings for these provide a total of four system clocks. In many situations, t_{ASC} and t_{CSC} must be increased if a full half-clock period is required.

Switching CTARs between frames while using continuous selection can cause errors in the transfer. The PCS signal must be negated before CTAR is switched.

When the CONT bit = 1 and the PCS signals for the next transfer are different from the present transfer, the PCS signals behave as if the CONT bit was not set.

20.4.7.6 Clock Polarity Switching between DSPI Transfers

To switch polarity between non-continuous DSPI frames, the edge generated by the change in the idle state of the clock occurs one system clock before the chip select pin for the next frame asserts.

See Section 20.3.2.3, “DSPI Clock and Transfer Attributes Registers 0–7 (DSPIx_CTARn).”

In Figure 20-40, time ‘A’ shows the one clock interval. Time ‘B’ is programmable with a minimum of two system clocks.

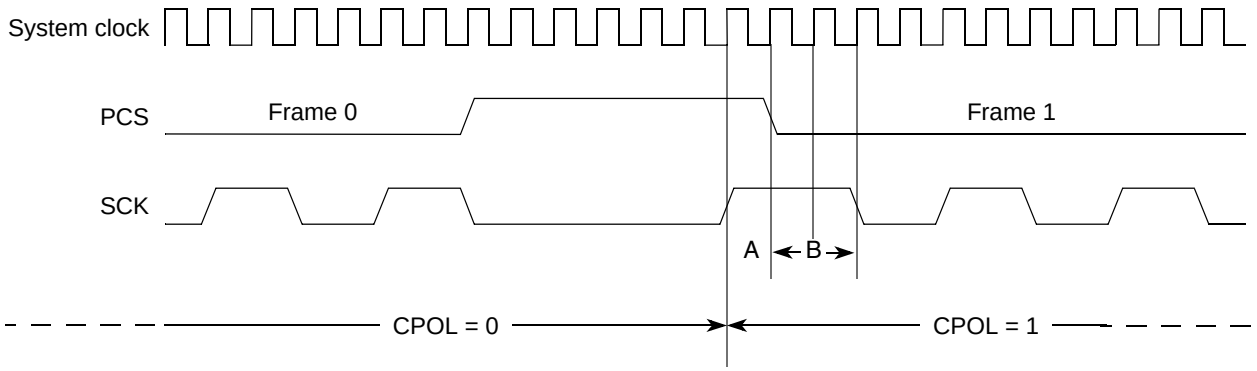


Figure 20-40. Polarity Switching between Frames

20.4.8 Continuous Serial Communications Clock

The DSPI provides the option of generating a continuous SCK signal for slave peripherals that require a continuous clock.

Continuous SCK is enabled by setting the CONT_SCKE bit in the DSPI*x*_MCR. Continuous SCK is valid in all configurations.

Continuous SCK is only supported for CPHA = 1. Setting CPHA = 0 is ignored if the CONT_SCKE bit is set. Continuous SCK is supported for modified transfer format.

Clock and transfer attributes for the continuous SCK mode are set according to the following rules:

- When the DSPI is in SPI configuration, CTAR0 is used initially. At the start of each SPI frame transfer, the CTAR specified by the CTAS for the frame is used.
- When the DSPI is in DSI configuration, the CTAR specified by the DSICTAS field is used at all times.
- When the DSPI is in CSI configuration, the CTAR selected by the DSICTAS field is used initially. At the start of an SPI frame transfer, the CTAR specified by the CTAS value for the frame is used. At the start of a DSI frame transfer, the CTAR specified by the DSICTAS field is used.
- In all configurations, the currently selected CTAR remains in use until the start of a frame with a different CTAR specified, or the continuous SCK mode is terminated.

The device is designed to use the same baud rate for all transfers made while using the continuous SCK. Switching clock polarity between frames while using continuous SCK can cause errors in the transfer. Continuous SCK operation is not guaranteed if the DSPI is put into module disable mode.

Enabling continuous SCK disables the PCS to SCK delay and the After SCK delay. The delay after transfer is fixed at one SCK cycle. Figure 20-41 shows timing diagram for continuous SCK format with continuous selection disabled.

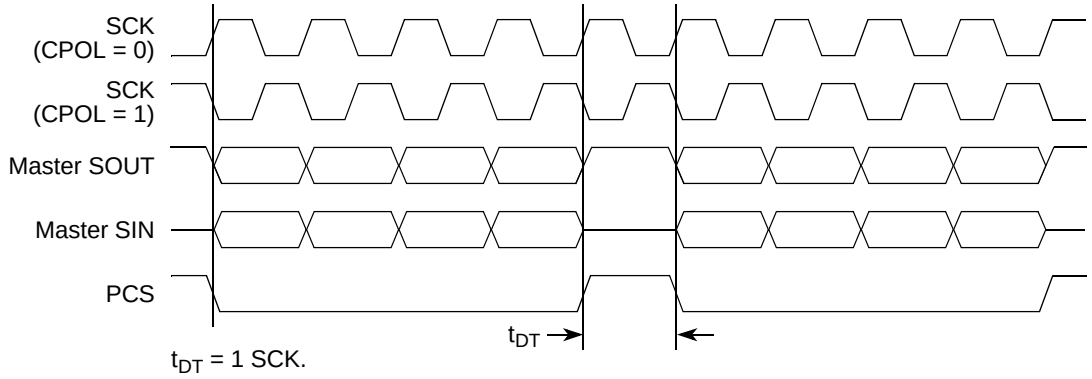


Figure 20-41. Continuous SCK Timing Diagram (CONT= 0)

If the CONT bit in the TX FIFO entry is set or the DCONT in the DSPI*x*_DSICR is set, PCS remains asserted between the transfers when the PCS signal for the next transfer is the same as for the current transfer. Figure 20-42 shows timing diagram for continuous SCK format with continuous selection enabled.

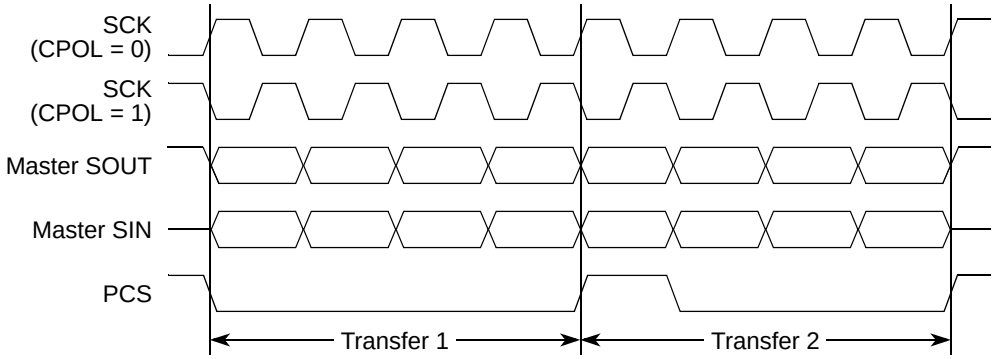


Figure 20-42. Continuous SCK Timing Diagram (CONT=1)

20.4.9 Interrupts and DMA Requests

The DSPI has five conditions that can generate interrupt requests only, and two conditions that can generate interrupt or DMA requests. Table 20-30 lists the conditions that can generate a DMA request or interrupt request.

Table 20-30. Interrupt and DMA Request Conditions

Condition	Flag	Interrupt	DMA
End of transfer queue has been reached (EOQ)	EOQF	X	
TX FIFO is not full	TFFF	X	X
Current frame transfer is complete	TCF	X	
TX FIFO underflow has occurred	TFUF	X	
RX FIFO is not empty	RFDF	X	X
RX FIFO overflow occurred	RFOF	X	
A FIFO overrun occurred[1]	TFUF ORed with RFOF	X	

[1] The FIFO overrun condition is created by ORing the TFUF and RFOF flags together.

Each condition has a flag bit and a request enable bit. The flag bits are described in the Section 20.3.2.4, "DSPI Status Register (DSPIx_SR)" and the request enable bits are described in the Section 20.3.2.5, "DSPI DMA / Interrupt Request Select and Enable Register (DSPIx_RSER)." The TX FIFO fill flag (TFFF) and RX FIFO drain flag (RFDF) generate interrupt requests or DMA requests depending on the TFFF_DIRS and RFDF_DIRS bits in the DSPI*x*_RSER.

20.4.9.1 End-of-Queue Interrupt Request (EOQF)

The end of queue equest indicates that the end of a transmit queue is reached. The end of queue request is generated when the EOQ bit in the executing SPI command is asserted and the EOQF_RE bit in the DSPI*x*_RSER is set. See the EOQ bit description in Section 20.3.2.4, "DSPI Status Register (DSPIx_SR)." See Figure 20-34 and Figure 20-35 that illustrate when EOQF is set.

20.4.9.2 Transmit FIFO Fill Interrupt or DMA Request (TFFF)

The transmit FIFO fill request indicates that the TX FIFO is not full. The transmit FIFO fill request is generated when the number of entries in the TX FIFO is less than the maximum number of possible entries, and the TFFF_RE bit in the DSPI*x*_RSER is set. The TFFF_DIRS bit in the DSPI*x*_RSER selects whether a DMA request or an interrupt request is generated.

20.4.9.3 Transfer Complete Interrupt Request (TCF)

The transfer complete request indicates the end of the transfer of a serial frame. The transfer complete request is generated at the end of each frame transfer when the TCF_RE bit is set in the DSPI*x*_RSER. See the TCF bit description in Section 20.3.2.4, "DSPI Status Register (DSPIx_SR)." See Figure 20-34 and Figure 20-35 that illustrate when TCF is set.

20.4.9.4 Transmit FIFO Underflow Interrupt Request (TFUF)

The transmit FIFO underflow request indicates that an underflow condition in the TX FIFO has occurred. The transmit underflow condition is detected only for DSPI modules operating in slave mode and SPI configuration. The TFUF bit is set when the TX FIFO of a DSPI operating in slave mode and SPI configuration is empty, and a transfer is initiated from an external SPI master. If the TFUF bit is set while the TFUF_RE bit in the DSPI*x*_RSER is set, an interrupt request is generated.

20.4.9.5 Receive FIFO Drain Interrupt or DMA Request (RFDF)

The receive FIFO drain request indicates that the RX FIFO is not empty. The receive FIFO drain request is generated when the number of entries in the RX FIFO is not zero, and the RFDF_RE bit in the DSPI*x*_RSER is set. The RFDF_DIRS bit in the DSPI*x*_RSER selects whether a DMA request or an interrupt request is generated.

20.4.9.6 Receive FIFO Overflow Interrupt Request (RFOF)

The receive FIFO overflow request indicates that an overflow condition in the RX FIFO has occurred. A receive FIFO overflow request is generated when RX FIFO and shift register are full and a transfer is initiated. The RFOF_RE bit in the DSPI*x*_RSER must be set for the interrupt request to be generated.

Depending on the state of the ROOE bit in the DSPI*x*_MCR, the data from the transfer that generated the overflow is either ignored or shifted in to the shift register. If the ROOE bit is set, the incoming data is shifted in to the shift register. If the ROOE bit is negated, the incoming data is ignored.

20.4.9.7 FIFO Overrun Request (TFUF) or (RFOF)

The FIFO overrun request indicates that at least one of the FIFOs in the DSPI has exceeded its capacity. The FIFO overrun request is generated by logically OR'ing together the RX FIFO overflow and TX FIFO underflow signals.

20.4.10 Power Saving Features

The DSPI supports two power-saving strategies:

- Module disable mode—clock gating of non-memory mapped logic
- Clock gating of slave interface signals and clock to memory-mapped logic

20.4.10.1 Module Disable Mode

Module disable mode is a module-specific mode that the DSPI can enter to save power. Host software can initiate the module disable mode by writing a 1 to the MDIS bit in the DSPI*x*_MCR. In module disable mode, the DSPI is in a dormant state, but the memory mapped registers are still accessible. Certain read or write operations have a different affect when the DSPI is in the module disable mode. Reading the RX FIFO pop register does not change the state of the RX FIFO. Likewise, writing to the TX FIFO push register does not change the state of the TX FIFO. Clearing either of the FIFOs does not have any effect in the module disable mode. Changes to the DIS_TXF and DIS_RXF fields of the DSPI*x*_MCR does not have any affect in the module disable mode. In the module disable mode, all status bits and register flags

in the DSPI return the correct values when read, but writing to them has no affect. Writing to the DSPI*x*_TCR during module disable mode does not have an effect. Interrupt and DMA request signals cannot be cleared while in the module disable mode.

20.4.10.2 Slave Interface Signal Gating

The DSPI module enable signal is used to gate slave interface signals such as address, byte enable, read/write and data. This prevents toggling slave interface signals from consuming power unless the DSPI is accessed.

20.5 Initialization and Application Information

20.5.1 How to Change Queues

DSPI queues are not part of the DSPI module, but the DSPI includes features in support of queue management. Queues are primarily supported in SPI configuration. This section presents an example of how to change queues for the DSPI.

1. Set the EOQ bit in the command word to indicate the last entry in the queue for the DSPI after the last command word from a queue is executed.
2. Sample the command word that has the EOQ bit set at the end of the transfer. Set the EOQ flag (EOQF) in the DSPI*x*_SR is set.

   If EOQF flag is set to 1, the serial interface is disabled, preventing data transmission and reception. The DSPI is put into the STOPPED state and the TXRXS bit is negated to indicate the STOPPED state. The eDMA continues to fill the TX FIFO until one of the following conditions occur:

   — TX FIFO is full

   — Modified DMA descriptor that adds queues to the TX and RX channels is received (step 5).
3. Disable the DSPI DMA transfers by clearing the DMA channel enable bit for the DMA channel assigned to the TX FIFO and RX FIFO. This is done in the eDMA controller.
4. Ensure all received data in the RX FIFO was transferred to the memory receive queue using one of the following methods:

   — Read RXCNT in DSPI*x*_SR

   — Check RFDF in the DSPI*x*_SR after each read operation of the DSPI*x*_POPR.
5. Modify the DMA descriptor for the TX and RX channels for additional queues.
6. Flush the TX FIFO and RX FIFO by writing a 1 to the CLR_TXF and the CLR_RXF bits respectively in the DSPI*x*_MCR register.
7. Clear the transfer count using one of the following methods:

   — Set the CTCNT bit in the command word of the first entry in the new queue

   — Write directly to SPI_TCNT field in DSPI*x*_TCR
8. Enable the DMA channel by setting the DMA enable request bit for the DMA channel assigned to the DSPI TX and RX FIFOs.
9. Enable serial transmission and serial reception of data by clearing the EOQF bit.

20.5.2 Baud Rate Settings

Table 20-31 shows the baud rate that is generated based on the combination of the baud rate prescaler PBR and the baud rate scaler BR in the DSPI*x*_CTARs. The values are calculated at a 100 MHz system frequency.

Table 20-31. Baud Rate Values

		Baud Rate Divider Prescaler Values (DSPI_CTAR[PBR])			
		2	**3**	**5**	**7**
Baud Rate Scaler Values (DSPI_CTAR[BR])	**2**	25.0 MHz	16.7 MHz	10.0 MHz	7.14 MHz
	4	12.5 MHz	8.33 MHz	5.00 MHz	3.57 MHz
	6	8.33 MHz	5.56 MHz	3.33 MHz	2.38 MHz
	8	6.25 MHz	4.17 MHz	2.50 MHz	1.79 MHz
	16	3.12 MHz	2.08 MHz	1.25 MHz	893 kHz
	32	1.56 MHz	1.04 MHz	625 kHz	446 kHz
	64	781 kHz	521 kHz	312 kHz	223 kHz
	128	391 kHz	260 kHz	156 kHz	112 kHz
	256	195 kHz	130 kHz	78.1 kHz	55.8 kHz
	512	97.7 kHz	65.1 kHz	39.1 kHz	27.9 kHz
	1024	48.8 kHz	32.6 kHz	19.5 kHz	14.0 kHz
	2048	24.4 kHz	16.3 kHz	9.77 kHz	6.98 kHz
	4096	12.2 kHz	8.14 kHz	4.88 kHz	3.49 kHz
	8192	6.10 kHz	4.07 kHz	2.44 kHz	1.74 kHz
	16384	3.05 kHz	2.04 kHz	1.22 kHz	872 Hz
	32768	1.53 kHz	1.02 kHz	610 Hz	436 Hz

20.5.3 Delay Settings

Table 20-32 shows the values for the delay after transfer (t_{DT}) and CS to SCK delay (t_{CSC}) that can be generated based on the prescaler values and the scaler values set in the DSPI*x*_CTARs. The values calculated assume a 100 MHz system frequency.

Table 20-32. Delay Values

		Delay Prescaler Values (DSPI_CTAR[PBR])			
		1	**3**	**5**	**7**
Delay Scaler Values (DSPI_CTAR[DT])	**2**	20.0 ns	60.0 ns	100.0 ns	140.0 ns
	4	40.0 ns	120.0 ns	200.0 ns	280.0 ns
	8	80.0 ns	240.0 ns	400.0 ns	560.0 ns
	16	160.0 ns	480.0 ns	800.0 ns	1.1 µs
	32	320.0 ns	960.0 ns	1.6 µs	2.2 µs
	64	640.0 ns	1.9 µs	3.2 µs	4.5 µs
	128	1.3 µs	3.8 µs	6.4 µs	9.0 µs
	256	2.6 µs	7.7 µs	12.8 µs	17.9 µs
	512	5.1 µs	15.4 µs	25.6 µs	35.8 µs
	1024	10.2 µs	30.7 µs	51.2 µs	71.7 µs
	2048	20.5 µs	61.4 µs	102.4 µs	143.4 µs
	4096	41.0 µs	122.9 µs	204.8 µs	286.7 µs
	8192	81.9 µs	245.8 µs	409.6 µs	573.4 µs
	16384	163.8 µs	491.5 µs	819.2 µs	1.1 ms
	32768	327.7 µs	983.0 µs	1.6 ms	2.3 ms
	65536	655.4 µs	2.0 ms	3.3 ms	4.6 ms

20.5.4 MPC5xx QSPI Compatibility with the DSPI

Table 20-33 shows the translation of commands written to the TX FIFO command halfword with commands written to the command RAM of the MPC5xx family QSPI. The table illustrates how to configure the DSPI*x*_CTARs to match the default cases for the possible combinations of the MPC5xx family control bits in its command RAM. The defaults for the MPC5xx family are based on a system clock of 40 MHz.

The following delay variables generate the same delay, or as close as possible, from the DSPI 100 MHz system clock that an MPC5xx family part generates from a 40 MHz system clock. For other system clock frequencies, you can recompute the values using the information presented in Section 20.5.3, "Delay Settings."

For BITSE = 0 --> 8 bits per transfer

For DT = 0 --> 0.425 µs delay: for this value, the closest value in the DSPI is 0.480 µs

For DSCK = 0 --> 0.5 of the SCK period: for this value, the value for the DSPI is 20 ns

Table 20-33. MPC5xx QSPI Compatibility with the DSPI

MPC5xx Family Control Bits DSPI Corresponding Control Bits						Corresponding DSPI*x*_CTAR Register Configuration					
BITSE	**CTAS[0]**	**DT**	**CTAS[1]**	**DSCK**	**CTAS[2]**	**DSPI*x*_CTAR*x***	**FMSZ**	**PDT**	**DT**	**PCSSCK**	**CSSCK**
0		0		0		0	0111	10	0011	00	0000
0		0		1		1	0111	10	0011	User	User
0		1		0		2	0111	User[1]	User	00	0000
0		1		1		3	0111	User	User	User	User
1		0		0		4	User	10	0011	00	0000
1		0		1		5	User	10	0011	User	User
1		1		0		6	User	User	User	00	0000
1		1		1		7	User	User	User	User	User

[1] Selected by user

20.5.5 Calculation of FIFO Pointer Addresses

The user has complete visibility of the TX and RX FIFO contents through the FIFO registers, and valid entries can be identified through a memory mapped pointer and a memory mapped counter for each FIFO. The pointer to the first-in entry in each FIFO is memory mapped. For the TX FIFO the first-in pointer is the transmit next pointer (TXNXTPTR). For the RX FIFO the first-in pointer is the pop next pointer (POPNXTPTR).

See Section 20.4.3.4, "Using the TX FIFO Buffering Mechanism," and Section 20.4.3.5, "Using the RX FIFO Buffering Mechanism," for details on the FIFO operation. The TX FIFO is chosen for the illustration, but the concepts carry over to the RX FIFO.

Figure 20-43 illustrates the concept of first-in and last-in FIFO entries along with the FIFO counter.

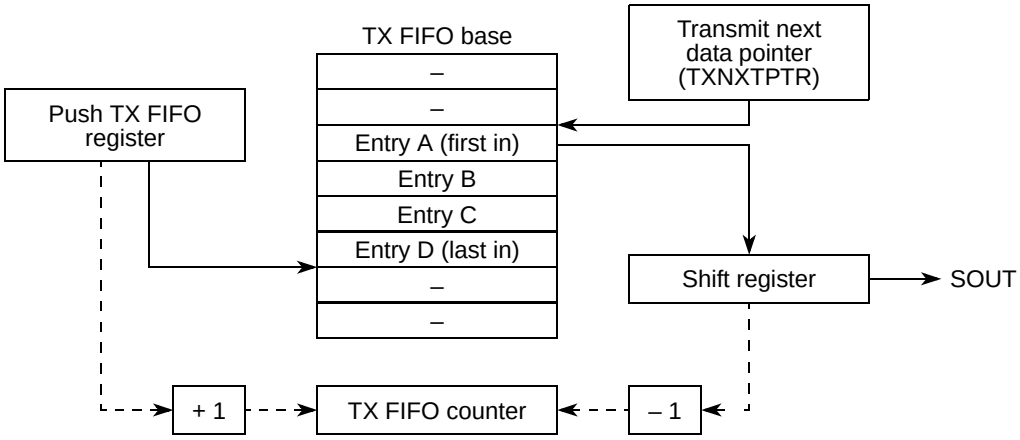


Figure 20-43. TX FIFO Pointers and Counter

20.5.5.1 Address Calculation for the First-in Entry and Last-in Entry in the TX FIFO

The memory address of the first-in entry in the TX FIFO is computed by the following equation:

First-in entry address = TXFIFO base + 4 (TXNXTPTR)

The memory address of the last-in entry in the TX FIFO is computed by the following equation:

Last-in entry address = TXFIFO base + (4 x [(TXCTR + TXNXTPTR - 1) modulo TXFIFO depth])

where:

TXFIFO base = base address of transmit FIFO

TXCTR = transmit FIFO counter

TXNXTPTR = transmit next pointer

TX FIFO depth = transmit FIFO depth, implementation specific

20.5.5.2 Address Calculation for the First-in Entry and Last-in Entry in the RX FIFO

The memory address of the first-in entry in the RX FIFO is computed by the following equation:

First-in entry address = RXFIFO base + 4 x (POPNXTPTR)

The memory address of the last-in entry in the RX FIFO is computed by the following equation:

Last-in entry address = RXFIFO base + 4 x [(RXCTR + POPNXTPTR - 1) modulo RXFIFO depth]

where:

RXFIFO base = base address of receive FIFO

RXCTR = receive FIFO counter

POPNXTPTR = pop next pointer

RX FIFO depth = receive FIFO depth, implementation specific

Chapter 21
Enhanced Serial Communication Interface (eSCI)

21.1 Introduction

This section gives an overview of the enhanced serial communication interface (eSCI) module, and presents a block diagram, its features and operating modes.

21.1.1 Block Diagram

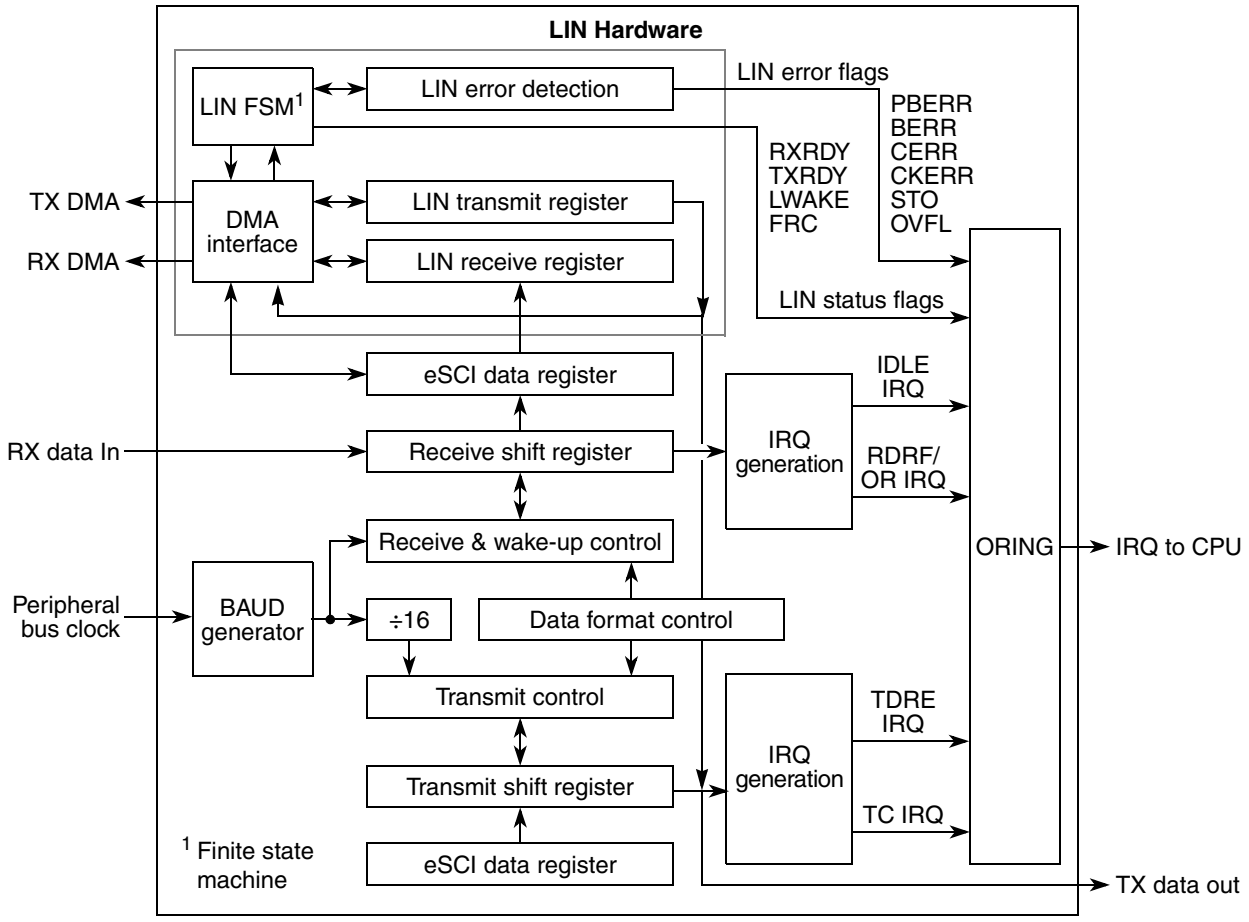


Figure 21-1. eSCI Block Diagram

21.1.2 Overview

The eSCI allows asynchronous serial communications with peripheral devices and other CPUs. The eSCI features allow it to operate as a LIN bus master, complying with the LIN 2.0 specification.

Each of the eSCI modules can be independently disabled by writing to the module disable (MDIS) bit in the module control register 2 (ESCI*x*_CR2). Disabling the module turns off the clock to the module, although the core can access some of eSCI registers via the slave bus. When the eSCI module is not used in the application, set the MDIS bit.

21.1.3 Features

The eSCI includes these features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- Configurable baud rate
- Programmable 8- or 9-bit data format
- LIN master node support
- Configurable CRC detection for LIN
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- Two receiver wake-up methods:
  - — Idle line wake-up
  - — Address mark wake-up
- Interrupt-driven operation
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- Two-channel DMA interface

21.1.4 Modes of Operation

The eSCI functions the same in normal, special, and emulation modes. It has a low-power module disable mode.

21.2 External Signal Description

This section provides a description of all eSCI external to the MCU.

Each eSCI module has two I/O signals connected to the external MCU pins. These signals are summarized in Table 21-1 and described in more detail in the following sections.

Table 21-1. eSCI Signals

Signal Name[1]	I/O	Description
RXD*x*	I	eSCI receive
TXD*x*	O	eSCI transmit

1 *x* indicates eSCI module A or B

21.2.1 Detailed Signal Description

21.2.1.1 eSCI Transmit (TXDA, TXDB)

These signals transmit data out for the eSCI.

21.2.1.2 eSCI Receive Pin (RXDA, RXDB)

These signals receive data input for the eSCI.

21.3 Memory Map and Register Definition

21.3.1 Overview

This section provides a detailed description of all memory and registers.

21.3.2 Module Memory Map

The memory map for the eSCI module is shown in Table 21-2. The address offset is listed for each register. The total address for each register is the sum of the base address for the eSCI module (ESCI*x*_base) and the address offset for each register. There are two eSCI modules on this device:

- eSCI A base address is 0xFFFB_0000
- eSCI B base address is 0xFFFB_4000

Table 21-2. Module Memory Map

Address	Register Name	Register Description	Bits
Base 0xFFFB_0000 (A) 0xFFFB_4000 (B)	ESCI*x*_CR1	eSCI control register 1	32
Base + 0x0004	ESCI*x*_CR2	eSCI control register 2	16
Base + 0x0006	ESCI*x*_DR	eSCI data register	16
Base + 0x0008	ESCI*x*_SR	eSCI status register	32
Base + 0x000C	ESCI*x*_LCR	LIN control register	32
Base + 0x0010	ESCI*x*_LTR	LIN transmit register	32
Base + 0x0014	ESCI*x*_LRR	LIN receive register	32
Base + 0x0018	ESCI*x*_LPR	LIN cyclic redundancy check polynomial register	32

21.3.3 Register Descriptions

This section contains the register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field functions follow the register diagrams, in bit order.

21.3.3.1 eSCI Control Register 1 (ESCI*x*_CR1)

Address: Base + 0x0000 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	SBR 0	SBR 1	SBR 2	SBR 3	SBR 4	SBR 5	SBR 6	SBR 7	SBR 8	SBR 9	SBR 10	SBR 11	SBR 12
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	LOOPS	0	RSRC	M	WAKE	ILT	PE	PT	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 21-2. eSCI Control Register 1 (ESCI*x*_CR1)

Table 21-3. ESCI*x*_CR1 Field Descriptions

Field	Description
0–2	Reserved.
3–15 SBR*n*	SCI baud rate. Used by the counter to determine the baud rate of the eSCI. The formula for calculating the baud rate is: $\text{SCI baud rate} = \frac{\text{eSCI system clock}}{16 \times \text{BR}}$ where BR is the content of the eSCI control register 1 (ESCI*x*_CR1), bits SBR0–SBR12. SBR0–SBR12 can contain a value from 1 to 8191. Refer to the ESCIx_LCR[WU] bit description on page 21-12.
16 LOOPS	Loop select. Enables loop operation. In loop operation, the RXD pin is disconnected from the eSCI and the transmitter output is internally connected to the receiver input. Both the transmitter and the receiver must be enabled to use the loop function. 0 Normal operation enabled, loop operation disabled 1 Loop operation enabled **Note:** The receiver input is determined by the RSRC bit.
17	Reserved.
18 RSRC	Receiver source. When LOOPS = 1, the RSRC bit determines the source for the receiver shift register input. 0 Receiver input internally connected to transmitter output 1 Receiver input connected externally to transmitter The table below shows how LOOPS and RSRC determine the loop function of the eSCI.
19 M	Data format mode. Determines whether data characters are 8 or 9 bits long. 0 1 start bit, 8 data bits, 1 stop bit 1 1 start bit, 9 data bits, 1 stop bit
20 WAKE	Wake-up condition. Determines which condition wakes up the eSCI: a logic 1 (address mark) in the most significant bit (MSB) position of a received data character or an idle condition on the RXD. 0 Idle line wake-up 1 Address mark wake-up **Note:** This is not a wake-up from a power-save mode; this function applies to the receiver standby mode only.
21 ILT	Idle line type. Determines when the receiver starts counting logic 1s as idle character bits. The counting begins either after the start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit can cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions. 0 Idle character bit count begins after start bit 1 Idle character bit count begins after stop bit
22 PE	Parity enable. Enables the parity function. When enabled, the parity function inserts a parity bit in the most significant bit position of the transmitted word. During reception, the received parity bit is verified in the most significant bit position. The received parity bit is not masked out. 0 Parity function disabled 1 Parity function enabled

LOOPS	RSRC	Function
0	–	Normal operation
1	0	Loop mode with RXD input internally connected to TXD output
1	1	Single-wire mode with RXD input connected to TXD

Table 21-3. ESCI*x*_CR1 Field Descriptions (continued)

Field	Description
23 PT	Parity type. Determines whether the eSCI generates and checks for even parity or odd parity. With even parity, an even number of 1s clears the parity bit and an odd number of 1s sets the parity bit. With odd parity, an odd number of 1s clears the parity bit and an even number of 1s sets the parity bit. 0 Even parity 1 Odd parity
24 TIE	Transmitter interrupt enable. Enables the transmit data register empty flag ESCI*x*_SR[TDRE] to generate interrupt requests. The interrupt is suppressed in TX DMA mode. 0 TDRE interrupt requests disabled 1 TDRE interrupt requests enabled
25 TCIE	Transmission complete interrupt enable. Enables the transmission complete flag ESCIx_SR[TC] to generate interrupt requests. The interrupt is suppressed in TX DMA mode. 0 TC interrupt requests disabled 1 TC interrupt requests enabled
26 RIE	Receiver full interrupt enable. Enables the receive data register full flag ESCIx_SR[RDRF] and the overrun flag ESCIx_SR[OR] to generate interrupt requests. The interrupt is suppressed in RX DMA mode. 0 RDRF and OR interrupt requests disabled 1 RDRF and OR interrupt requests enabled
27 ILIE	Idle line interrupt enable. Enables the idle line flag ESCIx_SR[IDLE] to generate interrupt requests. 0 IDLE interrupt requests disabled 1 IDLE interrupt requests enabled
28 TE	Transmitter enable. Enables the eSCI transmitter and configures the TXD pin as being controlled by the eSCI. The TE bit can be used to queue an idle preamble. 0 Transmitter disabled 1 Transmitter enabled
29 RE	Receiver enable. Enables the eSCI receiver. 0 Receiver disabled 1 Receiver enabled
30 RWU	Receiver wake-up. Standby state. 0 Normal operation. 1 RWU enables the wake-up function and inhibits further receiver interrupt requests. Normally, hardware wakes the receiver by automatically clearing RWU.
31 SBK	Send break. Toggling SBK sends one break character (Refer to the description of ESCI*x*_CR2[BRK13] for break character length). Toggling implies clearing the SBK bit before the break character has finished transmitting. As long as SBK is set, the transmitter continues to send complete break characters. 0 No break characters 1 Transmit break characters

NOTES

After a reset, the baud rate generator is disabled until the TE bit or the RE bit is initialized (set for the first time).

The baud rate generator is disabled when SBR0–SBR12 = 0x0000.

The baud rate is usually written using a single write. If using 8-bit writes, writing to ESCI*x*_CR1[0–7] has no effect until ESCI*x*_CR1[8–15] is written, since ESCI*x*_CR1[0–7] is temporarily buffered until ESCI*x*_CR1[8–15] is written.

When parity is enabled, the RX Data parity bit is in the data register.

21.3.3.2 eSCI Control Register 2 (ESCI*x*_CR2)

NOTE

DMA requests are negated when in module disable mode.

Address: Base + 0x0004 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	MDIS	FBR	BSTP	IEB ERR	RX DMA	TX DMA	BRK 13	0	BESM 13	SB STP	0	0	ORIE	NFIE	FEIE	PFIE
W																
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 21-3. eSCI Control Register 2 (ESCIx_CR2)

Table 21-4. ESCI*x*_CR2 Field Description

Field	Description
0 MDIS	Module disable. By default the module is enabled, but can be disabled by writing a 1 to this bit. DMA requests are negated if the device is in module disable mode. 0 Module enabled 1 Module disabled
1 FBR	Fast bit error detection. Handles bit error detection on a per bit basis. If this is not enabled, bit errors are detected on a byte basis.
2 BSTP	Bit error/physical bus error stop. Causes DMA TX requests to be suppressed, as long as the bit error and physical bus error flags are not cleared. This stops further DMA writes, which would otherwise cause data bytes to be interpreted as LIN header information.
3 IEBERR	Enable bit error interrupt. Generates an interrupt, when a LIN bit error is detected. For a list of interrupt enables and flags, Refer to Table 21-21.
4 RXDMA	Activate RX DMA channel. If this bit is enabled and the eSCI has received data, it raises a DMA RX request.
5 TXDMA	Activate TX DMA channel. Whenever the eSCI is able to transmit data, it raises a DMA TX request.

Table 21-4. ESCI*x*_CR2 Field Description (continued)

Field	Description
6 BRK13	Break transmit character length. Determines whether the transmit break character is either 10 or 11, or 13 or 14 bits long. The detection of a framing error is not affected by this bit. **Break Length:** BRK13 = 0, ESCI*x*_CR1[M] = 0: 10 BRK13 = 0, ESCI*x*_CR1[M] = 1: 11 BRK13 = 1, ESCI*x*_CR1[M] = 0: 13 BRK13 = 1, ESCI*x*_CR1[M] = 1: 14 0 Break Character is 10 or 11 bits long 1 Break character is 13 or 14 bits long **Note:** LIN 2.0 now requires that a break character is always 13 bits long, always set this bit to 1. The eSCI works with BRK13=0, but it violates LIN 2.0.
7	Reserved. This bit is readable/writable, but has no effect on the operation of the eSCI module.
8 BESM13	Bit error sample mode, bit 13. Determines when to sample the incoming bit to detect a bit error. This only applies when FBR is set. 0 Sample at RT clock 9 1 Sample at RT clock 13 (Refer to Section 21.4.5.3, “Data Sampling”)
9 SBSTP	SCI bit error stop. Stops the SCI when a bit error is asserted. This allows to stop driving the LIN bus quickly after a bit error has been detected. 0 Byte is completely transmitted 1 Byte is partially transmitted
10–11	Reserved.
12 ORIE	Overrun error interrupt enable. Generates an interrupt, when a frame error is detected. For a list of interrupt enables and flags, Refer to Table 21-21.
13 NFIE	Noise flag interrupt enable. Generates an interrupt, when noise flag is set. For a list of interrupt enables and flags, Refer to Table 21-21.
14 FEIE	Frame error interrupt enable. Generates an interrupt, when a frame error is detected. For a list of interrupt enables and flags, Refer to Table 21-21.
15 PFIE	Parity flag interrupt enable. Generates an interrupt, when parity flag is set. For a list of interrupt enables and flags, Refer to Table 21-21.

21.3.3.3 eSCI Data Register (ESCI*x*_DR)

Address: Base + 0x0006 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	R8	T8	0	0	0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0
W									T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 21-4. eSCI Data Register (ESCI*x*_DR)

Table 21-5. ESCI*x*_DR Field Description

Field	Description
0 R8	Received bit 8. R8 is the ninth data bit received when the eSCI is configured for 9-bit data format (M = 1).
1 T8	Transmit bit 8. T8 is the ninth data bit transmitted when the eSCI is configured for 9-bit data format (M = 1). **Note:** If the value of T8 is the same as in the previous transmission, T8 does not have to be rewritten.The same value is transmitted until T8 is rewritten.
2–7	Reserved.
8–15 R7–R0 T7–T0	Received bits/transmit bits 7–0 for 9-bit or 8-bit formats. Bits 7–0 from SCI communication can be read from ESCI*x*_DR[8–15] (provided that SCI communication was successful). Writing to ESCI*x*_DR [8–15] provides bits 7–0 for SCI transmission.

NOTES

In 8-bit data format, only bits 8–15 of ESCI*x*_DR need to be accessed.

When transmitting in 9-bit data format and using 8-bit write instructions, write first to ESCI*x*_DR[0–7], then ESCI*x*_DR[8–15]. For 9-bit transmissions, a single write can also be used.

Do not use ESCI*x*_DR in LIN mode, writes to this register are blocked in LIN mode.

Even if parity generation/checking is enabled via ESCIx_CR[PE], the parity bit is not masked out.

21.3.3.4 eSCI Status Register (ESCI*x*_SR)

The ESCI*x*_SR indicates the current status. The status flags can be polled, and some can also be used to generate interrupts. All bits in ESCI*x*_SR except for RAF are cleared by writing 1 to them.

Address: Base + 0x0008 Access: R/W1c

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	0	0	0	BERR	0	0	0	RAF
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c				w1c				
Reset	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	RX RDY	TX RDY	LWAKE	STO	PB ERR	CERR	CK ERR	FRC	0	0	0	0	0	0	0	OVFL
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c								w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 21-5. eSCI Status Register (ESCI*x*_SR)

Table 21-6. ESCI*x*_SR Field Descriptions

Field	Description
0 TDRE	Transmit data register empty flag. TDRE is set when the transmit shift register receives a byte from the eSCI data register. When TDRE is 1, the data register (ESCI*x*_DR) is empty and can receive a new value to transmit. Clear TDRE by writing 1 to it. 0 eSCI has not transferred data to the transmit shift register since the last time software cleared TDRE 1 Byte transferred to transmit shift register; transmit data register empty
1 TC	Transmit complete flag. TC is set low when there is a transmission in progress or when a preamble or break character is loaded. TC is set high when the TDRE flag is set and no data, preamble, or break character is being transmitted. When TC is set, the TXD out signal becomes idle (logic 1). After the device is switched on (by clearing the MDIS bit, Refer to Section 21.3.3.2, "eSCI Control Register 2 (ESCIx_CR2)," a preamble is transmitted; if no byte is written to the SCI data register then the completion of the preamble can be monitored using the TC flag. Clear TC by writing 1 to it. 0 Transmission in progress 1 No transmission in progress. Indicates that TXD out is idle.
2 RDRF	Receive data register full flag. RDRF is set when the data in the receive shift register transfers to the eSCI data register. Clear RDRF by writing 1 to it. 0 eSCI has not transferred data to the receive data register since last time software cleared RDRF 1 Received data available in eSCI data register
3 IDLE	Idle line flag. IDLE is set when 10 consecutive logic 1s (if M = 0) or 11 consecutive logic 1s (if M = 1) appear on the receiver input. After the IDLE flag is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag. Clear IDLE by writing 1 to it. 0 Receiver input is either active now or has never become active since the IDLE flag was last cleared 1 Receiver input has become idle **Note:** When the receiver wake-up bit (RWU) is set, an idle line condition does not set the IDLE flag.
4 OR	Overrun flag. OR is set when software fails to read the eSCI data register before the receive shift register receives the next frame. The OR bit is set immediately after the stop bit has been completely received for the second frame. The data in the shift register is lost, but the data already in the eSCI data registers is not affected. Clear OR by writing 1 to it. 0 No overrun 1 Overrun
5 NF	Noise flag. NF is set when the eSCI detects noise on the receiver input. NF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear NF by writing 1 to it. 0 No noise 1 Noise
6 FE	Framing error flag. FE is set when a logic 0 is accepted as the stop bit. FE bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear FE by writing 1 to it. 0 No framing error 1 Framing error
7 PF	Parity error flag. PF is set when the parity enable bit, PE, is set and the parity of the received data does not match its parity bit. Clear PE by writing 1 to it. 0 No parity error 1 Parity error
8–10	Reserved, Must be 0.

Table 21-6. ESCI*x*_SR Field Descriptions (continued)

Field	Description
11 BERR	Bit error. Indicates a bit on the bus did not match the transmitted bit. If FBR = 0, checking happens after a complete byte has been transmitted and received again. If FBR = 1, checking happens bit by bit. This bit is only used for LIN mode. BERR is also set if an unrequested byte is received (i.e. a byte that is not part of an RX frame) that is not recognized as a wake-up flag. (Because the data on the RX line does not match the idle state that was assigned to the TX line.) Clear BERR by writing 1 to it. A bit error causes the LIN finite state machine (FSM) to reset unless ESCI*x*_LCR[LDBG] is set.
12–14	Reserved.
15 RAF	Receiver active flag. RAF is set when the receiver detects a logic 0 during the RT1 time period of the start bit search. RAF is cleared when the receiver detects an idle character. 0 No reception in progress. 1 Reception in progress.
16 RXRDY	The eSCI has received LIN data. This bit is set when the ESCI*x*_LCR receives a byte. Write a one to RXRDY to clear it to 0.
17 TXRDY	The LIN FSM can accept another write to ESCI*x*_LTR. This bit is set when the ESCI*x*_LTR register becomes free. Write a one to TXRDY to clear it to 0.
18 LWAKE	Received LIN wake-up signal. A LIN slave has sent a wake-up signal on the bus. When this signal is detected, the LIN FSM resets. If the setup of a frame had already started, it therefore must be repeated. LWAKE is set if ESCI receives a LIN 2.0 wake-up signal (in which the baud rate is lower than 32K baud). Refer to the WU bit.
19 STO	Slave time out. Represents a NO_RESPONSE_ERROR. This is set if a slave does not complete a frame within the specified maximum frame length. For LIN 1.3 the following formula is used: $$TFRAME\_MAX = (10 \times NDATA + 44) \times 1.4$$
20 PBERR	Physical bus error. No valid message can be generated on the bus. This is set if, after the start of a byte transmission, the input remains unchanged for 31 cycles. This resets the LIN FSM.
21 CERR	CRC error. The CRC pattern received with an extended frame was not correct. 0 No error 1 CRC error
22 CKERR	Checksum error. Checksum error on a received frame.
23 FRC	Frame complete. LIN frame completely transmitted. All LIN data bytes received.
24–30	Reserved.
31 OVFL	ESCI*x*_LRR overflow. The LIN receive register has not been read before a new data byte, CRC, or checksum byte has been received from the LIN bus. Set when the condition is detected, and cleared by writing 1 to it.

21.3.3.5 LIN Control Register (ESCI*x*_LCR)

ESCI*x*_LCR can be written only when there are no ongoing transmissions.

Address: Base + 0x000C Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	LRES	0	WUD 0	WUD 1	LDBG	DSF	PRTY	LIN	RXIE	TXIE	WUIE	STIE	PBIE	CIE	CKIE	FCIE
W		WU														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	OFIE	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 21-6. LIN Control Register (ESCI*x*_LCR)

Table 21-7. ESCI*x*_LCR Field Descriptions

Field	Description
0 LRES	LIN resynchronize. Causes the LIN protocol engine to return to start state. This happens automatically after bit errors, but software can force a return to start state manually via this bit. The bit first must be set then cleared, so that the protocol engine is operational again.
1 WU	LIN bus wake-up. Generates a wake-up signal on the LIN bus. This must be set before a transmission, if the bus is in sleep mode. This bit auto-clears, so a read from this bit always returns 0. According to LIN 2.0, generating a valid wake-up character requires programming the SCI baud rate to a range of 32K baud down to 1.6K baud.
2–3 WUD [0:1]	Wake-up delimiter time. Determines how long the LIN engine waits after generating a wake-up signal, before starting a new frame. The eSCI does not set ESCIx_SR[TXRDY] before this time expires. In addition to this delimiter time, the CPU and the eSCI require some setup time to start a new transmission. Typically there is an additional bit time delay. The following table shows how WUD0 and WUD1 affect the delimiter time. **WUD0 / WUD1 / Bit Times** 0 / 0 / 4 0 / 1 / 8 1 / 0 / 32 1 / 1 / 64
4 LDBG	LIN debug mode. Prevents the LIN FSM from automatically resetting, after an exception (bit error, physical bus error, wake-up flag) has been received. This is for debug purposes only.
5 DSF	Double stop flags. When a bit error is detected, an additional stop flag is added to the byte in which the error occurred.
6 PRTY	Activating parity generation. Generate the two parity bits in the LIN header.

Table 21-7. ESCI*x*_LCR Field Descriptions (continued)

Field	Description
7 LIN	LIN mode. Switch device into LIN mode. 0 LIN disabled 1 LIN enabled
8 RXIE	LIN RXREG ready interrupt enable. Generates an Interrupt when new data is available in the LIN RXREG. For a list of interrupt enables and flags, Refer to Table 21-21.
9 TXIE	LIN TXREG ready interrupt enable. Generates an Interrupt when new data can be written to the LIN TXREG. For a list of interrupt enables and flags, Refer to Table 21-21.
10 WUIE	RX wake-up interrupt enable. Generates an Interrupt when a wake-up flag from a LIN slave has been received. For a list of interrupt enables and flags, Refer to Table 21-21.
11 STIE	Slave timeout error interrupt enable. Generates an Interrupt when the slave response is too slow. For a list of interrupt enables and flags, Refer to Table 21-21.
12 PBIE	Physical bus error interrupt enable. Generates an Interrupt when no valid message can be generated on the bus. For a list of interrupt enables and flags, Refer to Table 21-21.
13 CIE	CRC error interrupt enable. Generates an Interrupt when a CRC error on a received extended frame is detected. For a list of interrupt enables and flags, Refer to Table 21-21.
14 CKIE	Checksum error interrupt enable. Generates an Interrupt on a detected checksum error. For a list of interrupt enables and flags, Refer to Table 21-21.
15 FCIE	Frame complete interrupt enable. Generates an Interrupt after complete transmission of a TX frame, or after the last byte of an RX frame is received. (The complete frame includes all header, data, CRC and checksum bytes as applicable.) For a list of interrupt enables and flags, Refer to Table 21-21.
16–22	Reserved.
23 OFIE	Overflow interrupt enable. Generates an Interrupt when a data byte in the ESCIx_LRR has not been read before the next data byte is received. For a list of interrupt enables and flags, Refer to Table 21-21.
24–31	Reserved.

21.3.3.6 LIN Transmit Register (ESCI*x*_LTR)

ESCI*x*_LTR can be written to only when TXRDY is set. The first byte written to the register selects the transmit address, the second byte determines the frame length, the third and fourth byte set various frame options and determine the timeout counter. Header parity is automatically generated if the ESCI*x*_LCR[PRTY] bit is set. For TX frames, the fourth byte (bits T7–T0) is skipped, since the timeout function does not apply. All following bytes are data bytes for the frame. CRC and checksum bytes are automatically appended when the appropriate options are selected.

When a bit error is detected, an interrupt is set and the transmission aborted. The register can only be written again after the interrupt is cleared. Afterwards a new frame starts, and the first byte needs to contain a header again.

Additionally it is possible to flush the ESCI*x*_LTR by setting the ESCI*x*_LCR[LRES] bit.

NOTE

Not all values written to the ESCI*x*_LTR generate valid LIN frames. The values are determined according to the LIN specification.

Address: Base + 0x0010 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R									0	0	0	0	0	0	0	0
W	P1/ L7/ HDCHK/ T7/ D7	P0/ L6/ CSUM/ T6/ D6	ID5/ L5/ CRC/ T5/ D5	ID4/ L4/ TX/ T4/ D4	ID3/ L3/ T11/ T3/ D3	ID2/ L2/ T10/ T2/ D2	ID1/ L1/ T9/ T1/ D1	ID0/ L0/ T8/ T0/ D0								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 21-7. LIN Transmit Register (ESCI*x*_LTR)

Address: eSCI *x* Base + 0x0010 Access: W/O

	0	1	2	3	4	5	6	7
R								
1st Write (Table 21-8) W	P[1:0]				ID[5:0]			
2nd Write (Table 21-9) W	L[7:0]							
3rd Write (Table 21-10) W	HDCHK	CSUM	CRC	TX ($\overline{RX}$)	T[11:8]			
4th Write (Table 21-11) W	T[7:0]							
5th Write (Table 21-12) W	D[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 21-8. LIN Transmit Register (ESCIx_LTR) Alternate Diagram

Table 21-8. ESCI*x*_LTR First Byte Field Description

Field	Description
0–1 P*n*	Parity bit *n*. When parity generation is enabled (ESCI*x*_LCR[PRTY] = 1), the parity bits are generated automatically. Otherwise they must be provided in this field.
2–7 ID*n*[1]	Header bit *n*. The LIN address, for LIN 1.x standard frames the length bits must be set appropriately so the extended frames are recognized by their specific patterns. Refer to the Table 21-9.
8–31	Reserved.

ID5	ID4	data bytes
0	0	2
0	1	2
1	0	4
1	1	8

[1] The values 3C, 3D, 3E and 3F of the ID-field (ID0-5) indicate command and extended frames. Refer to LIN Specification Package Revision 2.0.

Table 21-9. ESCI*x*_LTR Second-Byte Field Description

Field	Description
0–7 L*n*	Length bit *n*. Defines the length of the frame (0 to 255 data bytes). This information is needed by the LIN state machine to insert the checksum or CRC pattern as required. LIN 1.x slaves only accepts frames with 2, 4, or 8 data bytes.
8–31	Reserved.

Table 21-10. ESCI*x*_LTR Third-Byte Field Descriptions

Field	Description
0 HDCHK	Header checksum enable. Include the header fields into the mod 256 checksum of the standard frames.
1 CSUM	Checksum enable. Append a checksum byte to the end of a TX frame. Verify the checksum byte of an RX frame.
2 CRC	CRC enable. Append two CRC bytes to the end of a TX frame. Verify the two CRC bytes of an RX frame are correct. If both CSUM and CRC bits are set, the LIN FSM first appends the CRC bytes, then the checksum byte, and are processed in this order. If HDCHK is set, the CRC calculation includes the header and data bytes, otherwise, the CRC is performed on the data bytes only. CRC bytes are not part of the LIN standard; they are normal data bytes and belong to a higher-level protocol.
3 TX	Transmit direction. Indicates that the eSCI transmits a frame to a slave. Otherwise, an RX frame is assumed, and the eSCI only transmits the header. The data bytes are received from the slave. 0 RX frame 1 TX frame

Table 21-10. ESCI*x*_LTR Third-Byte Field Descriptions (continued)

Field	Description
4–7 T*n*	Timeout bit *n*. Sets the counter to determine a NO_RESPONSE_ERROR, if the frame is a read access to a LIN slave. Following LIN standard rev 1.3, the value $(10 \times N_{DATA} + 45) \times 1.4$ is recommended. For transmissions, this counter has to be set to 0. The timeout bits 7–0 are not written on a TX frame. For TX frames, the fourth byte written to the LIN transmit register (ESCI*x*_LTR) is the first data byte, for RX frames it contains timeout bits 7–0.The time is specified in multiples of bit times. The timeout period starts with the transmission of the LIN break character.
8–31	Reserved.

Table 21-11. ESCI*x*_LTR Rx Frame Fourth Byte Field Description

Field	Description
0–7 T*n*	Timeout bit *n*. Sets the counter to determine a NO_RESPONSE_ERROR, if the frame is a read access to a LIN slave. Follow the LIN standard rev 1.3, the value $(10 \times N_{DATA} + 45) \times 1.4$. For transmissions, this counter must be set to 0. The timeout bits 7–0 are not written on a TX frame. For TX frames, the fourth byte written to the LIN transmit register (ESCI*x*_LTR) is the first data byte. For RX frames, it contains timeout bits 7–0.The time is specified in multiples of bit times. The timeout period starts with the transmission of the LIN break character.
8–31	Reserved.

Table 21-12. ESCI*x*_LTR Tx Frame Fourth+ Byte/ Rx Frame Fifth+ Byte Field Description

Field	Description
0–7 D*n*	Data bits for transmission.
8–31	Reserved.

21.3.3.7 LIN Receive Register (ESCI*x*_LRR)

ESCI*x*_LRR can be ready only when ESCI*x*_SR[RXRDY] is set.

NOTE

Application software must ensure that ESCI*x*_LRR be read before new data or checksum bytes or CRCs are received from the LIN bus.

Address: Base + 0x0014 Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 21-9. LIN Receive Register (ESCI*x*_LRR)

Table 21-13. ESCI*x*_LRR Field Descriptions

Field	Description
0–7 D*n*	Data bit *n*. Provides received data bytes from RX frames. Data is only valid when the ESCI*x*_SR[RXRDY] flag is set. CRC and checksum information are not available in the ESCI*x*_LRR unless they are treated as data. It is possible to treat CRC and checksum bytes as data by deactivating the CSUM respectively CRC control bits in the ESCI*x*_LTR; however, then CRC and CSUM checking has to be performed by software. Data bytes must be read from the ESCI*x*_LRR (by CPU or DMA) before any new bytes (including CRC or checksum) are received from the LIN bus otherwise the data byte is lost and OVFL is set. **Note:** The data must be collected and the LIN frame finished (including CRC and checksum if applicable) before a wake-up character can be sent.
8–31	Reserved.

21.3.3.8 LIN CRC Polynomial Register (ESCI*x*_LPR)

ESCI*x*_LPR*n* can be written when there are no ongoing transmissions.

Address: Base + 0x0018 Access: R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
Reset	1	1	0	0	0	1	0	1	1	0	0	1	1	0	0	1

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 21-10. LIN CRC Polynomial Register (ESCI*x*_LPR)

Table 21-14. ESCI*x*_LPR Field Description

Field	Description
0–15 P*n*	Polynomial bit x^n. Bits P15–P0 are used to define the LIN polynomial - standard is $x^{15} + x^{14} + x^{10} + x^8 + x^7 + x^4 + x^3 + 1$ (the polynomial used for the CAN protocol).
16–31	Reserved.

21.4 Functional Description

21.4.1 Overview

This section provides a complete functional description of the eSCI module, detailing the operation of the design from the end user perspective in a number of subsections.

Figure 21-11 shows the structure of the eSCI module. The eSCI allows full duplex, asynchronous, NRZ serial communication between the CPU and remote devices, including other CPUs. The eSCI transmitter and receiver operate independently, although they use the same baud rate generator. The CPU monitors the status of the eSCI, writes the data to be transmitted, and processes received data.

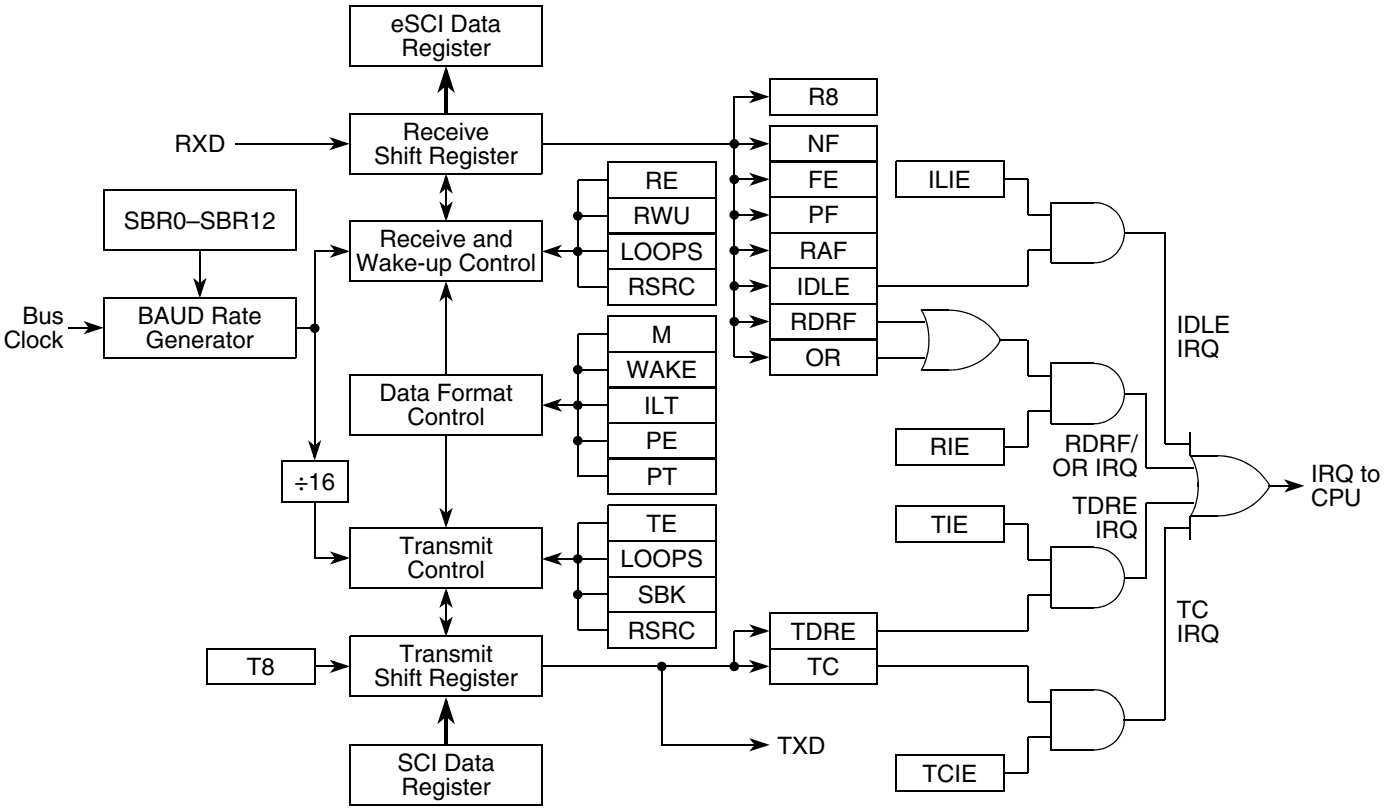


Figure 21-11. eSCI Operation Block Diagram

21.4.2 Data Format

The eSCI uses the standard NRZ mark/space data format. Each data character is contained in a frame that includes a start bit, eight or nine data bits, and a stop bit. Clearing the M bit in eSCI control register 1 configures the eSCI for 8-bit data characters. A frame with eight data bits has a total of 10 bits. Setting the M bit configures the eSCI for 9-bit data characters. A frame with nine data bits has a total of 11 bits.

When the eSCI is configured for 9-bit data characters, the ninth data bit is the T8 bit in the eSCI data register (ESCI*x*_DR). It remains unchanged after transmission and can be used repeatedly without rewriting it. A frame with nine data bits has a total of 11 bits.

The two different data formats are illustrated in Figure 21-12. Table 21-15 and Table 21-16 show the number of each type of bit in 8-bit data format and 9-bit data format, respectively.

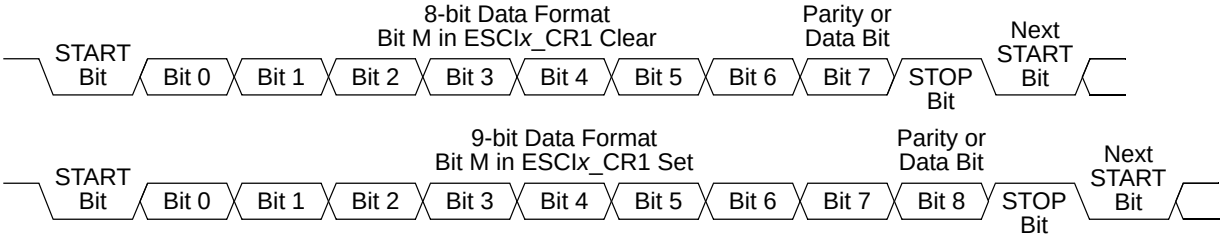


Figure 21-12. eSCI Data Formats

Table 21-15. Example of 8-bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	8	0	0	1
1	7	0	1	1
1	7	1 [1]	0	1

[1] The address bit identifies the frame as an address character. Refer to Section 21.4.5.6, “Receiver Wake-up.”

Table 21-16. Example of 9-Bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	9	0	0	1
1	8	0	1	1
1	8	1 [1]	0	1

[1] The address bit identifies the frame as an address character. Refer to Section 21.4.5.6, “Receiver Wake-up.”

21.4.3 Baud Rate Generation

A 13-bit modulus counter in the baud rate generator derives the baud rate for both the receiver and the transmitter. The value, 1 to 8191, written to the SBR0–SBR12 bits determines the system clock divider. The SBR bits are in the eSCI control register 1 (ESCI*x*_CR1). The baud rate clock is synchronized with the system clock and drives the receiver. The baud rate clock divided by 16 drives the transmitter. The receiver has an acquisition rate of 16 samples per bit time.

Baud rate generation is subject to one source of error when integer division of the system clock does not result in the exact target frequency.

Table 21-17 lists some examples of achieving target baud rates with a system clock frequency of 128 MHz.

$$\text{SCI baud rate} = \frac{\text{System clock}}{16 \times \text{ESCIx\_CR1[SBR]}}$$

Table 21-17. Baud Rates (Example: System Clock = 128 MHz)

Bits SBR[0:12]	Receiver Clock (Hz)	Transmitter Clock (Hz)	Target Baud Rate	Error (%)
0x0023	3,657,143	228,571	230,400	–0.79
0x0045	1,855,072	115,942	115,200	+0.64
0x008B	920,863	57,554	57,600	–0.01
0x00D0	615,385	38,462	38,400	+0.16
0x01A1	306,954	19,185	19,200	–0.08
0x022C	230,216	14,388	14,400	–0.08
0x0341	153,661	9,604	9600	+.04
0x0683	76,785	4,799	4800	–0.02
0x0D05	38,404	2,400.2	2400	+.01
0x1A0A	19,202	1,200.1	1200	+.01

21.4.4 Transmitter

Figure 21-13 illustrates the features of the eSCI transmitter.

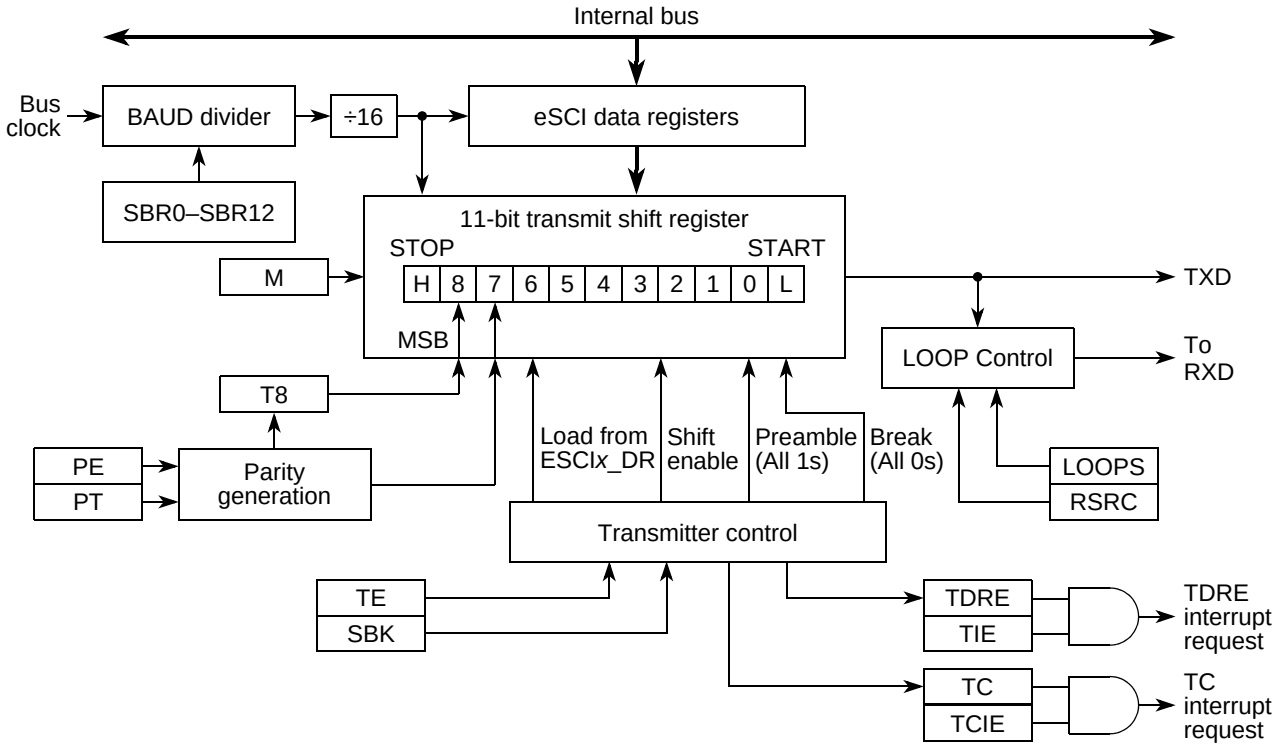


Figure 21-13. eSCI Transmitter Block Diagram

21.4.4.1 Transmitter Character Length

The eSCI transmitter can accommodate either 8-bit or 9-bit data characters. The state of the M bit in eSCI control register 1 (ESCI*x*_CR1) determines the length of data characters. When transmitting 9-bit data, bit T8 in the eSCI data register (ESCI*x*_DR) is the ninth bit (bit 8).

21.4.4.2 Character Transmission

To transmit data, the MCU writes the data bits to the eSCI data register (ESCI*x*_DR), which in turn are transferred to the transmit shift register. The transmit shift register then shifts a frame out through the TXD signal, after it has prefaced them with a start bit and appended them with a stop bit. The eSCI data register (ESCI*x*_DR) is the buffer (write-only during transmit) between the internal data bus and the transmit shift register.

The eSCI also sets a flag, the transmit data register empty flag (TDRE), every time it transfers data from the buffer (ESCI*x*_DR) to the transmit shift register. The transmit driver routine can respond to this flag by writing another byte to the transmitter buffer (ESCI*x*_DR), while the shift register is still shifting out the first byte.

To initiate an eSCI transmission:

1. Configure the eSCI:
   a) Turn on the module by clearing ESCI*x*_CR2[MDIS] if this bit is set.
   b) Select a baud rate. Write this value to the eSCI control register 1 (ESCI*x*_CR1) to start the baud rate generator. Remember that the baud rate generator is disabled when the ESCI*x*_CR1[SBR] field is zero. When using 8-bit writes, writes to the ESCI*x*_CR1[0–7] have no effect without also writing to ESCI*x*_CR1[8–15].
   c) Write to ESCIx_CR1 to configure word length, parity, and other configuration bits (LOOPS, RSRC, M, WAKE, ILT, PE, PT).
   d) Enable the transmitter, interrupts, receive, and wake-up as required, by writing to the ESCI*x*_CR1 register bits (TIE, TCIE, RIE, ILIE, TE, RE, RWU, SBK). A preamble or idle character is shifted out of the transmitter shift register.

NOTE

A single 32-bit write to ESCI_CR1 can be used to perform steps b–d above.

2. Transmit procedure for each byte:
   a) Poll the TDRE flag by reading the ESCI*x*_SR or responding to the TDRE interrupt. Keep in mind that the TDRE bit resets to 1.
   b) If the TDRE flag is set, software should then clear it, followed by writing the data to be transmitted to ESCIx_DR, where the ninth bit is written to the T8 bit in ESCIx_DR if the eSCI is in 9-bit data format.
3. Repeat step 2 for each subsequent transmission.

NOTE

The TDRE flag is set when the shift register is loaded with the next data to transmit from ESCI*x*_DR, which occurs approximately half-way through the stop bit of the previous frame. This transfer occurs 9/16ths of a bit time AFTER the start of the stop bit of the previous frame.

Toggling the TE bit from 0 to 1 automatically loads the transmit shift register with a preamble of 10 logic 1s (if M = 0) or 11 logic 1s (if M = 1). After the preamble shifts out, control logic transfers the data from the eSCI data register into the transmit shift register. A logic 0 start bit automatically goes into the least significant bit position of the transmit shift register. A logic 1 stop bit goes into the most significant bit position.

The eSCI hardware supports odd or even parity. When parity is enabled, the most significant bit (Msb) of the data character is the parity bit.

The transmit data register empty flag, TDRE, in the eSCI status register (ESCI*x*_SR) is set when the eSCI data register transfers a byte to the transmit shift register. The TDRE flag indicates that the eSCI data register can accept new data from the internal data bus. If the transmit interrupt enable bit (TIE), in eSCI control register 1 (ESCI*x*_CR1) is also set, the TDRE flag generates a transmit interrupt request.

When the transmit shift register is not transmitting a frame, the TXD output goes to the idle condition, logic 1. If at any time software clears the TE bit in eSCI control register 1 (ESCI*x*_CR1), the transmit enable signal goes low and the TXD output goes idle.

If software clears TE while a transmission is in progress (ESCI*x*_CR1[TC] = 0), the frame in the transmit shift register continues to shift out. To avoid accidentally cutting off the last frame in a message, always wait for TDRE to go high after the last frame before clearing TE.

To separate messages with preambles with minimum idle line time, use the following sequence between messages:

1. Write the last byte of the first message to ESCI*x*_DR.
2. Wait for the TDRE flag to go high, indicating the transfer of the last frame to the transmit shift register.
3. Queue a preamble by clearing and then setting the TE bit.
4. Write the first byte of the second message to ESCI*x*_DR.

21.4.4.3 Break Characters

Setting the break bit, SBK, in eSCI control register 1 (ESCI*x*_CR1) loads the transmit shift register with a break character. A break character contains all logic 0s and has no start, stop, or parity bit. Break character length depends on the M bit in the eSCI control register 1 (ESCI*x*_CR1) and on the BRK13 bit in the eSCI control register 2 (ESCI*x*_CR2). As long as SBK is set, the transmitter logic continuously loads break characters into the transmit shift register. After software clears the SBK bit, the shift register finishes transmitting the last break character and then transmits at least one logic 1. The automatic logic 1 at the end of a break character guarantees the recognition of the start bit of the next frame.

NOTE

LIN 2.0 requires that a break character be 13-bits long, so always set the BRK13 bit to 1. The eSCI works with BRK13 = 0, but it violates LIN 2.0.

The eSCI recognizes a break character when a start bit is followed by eight or nine logic 0 data bits and a logic 0 where the stop bit should be. Receiving a break character has the following effects on eSCI registers:

- Sets the framing error flag, FE.
- Sets the receive data register full flag, RDRF.
- Clears the eSCI data register (ESCI*x*_DR).
- Can set a flag: overrun (OR), noise flag (NF), parity error flag (PF), or the receiver active flag (RAF). For more details, refer to Section 21.3.3.4, “eSCI Status Register (ESCIx_SR).”

21.4.4.4 Idle Characters

An idle character contains all logic 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in eSCI control register 1 (ESCI*x*_CR1). The preamble is a synchronizing idle character that begins the first transmission initiated after toggling the TE bit from 0 to 1.

If the TE bit is cleared during a transmission, the TXD output becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle character to be sent after the frame currently being transmitted.

NOTE

When queueing an idle character, return the TE bit to logic 1 before the stop bit of the current frame shifts out through the TXD output. Setting the TE bit after the stop bit shifts out through the TXD output causes data previously written to the eSCI data register to be lost. Toggle the TE bit for a queued idle character while the TDRE flag is set and immediately before writing the next byte to the eSCI data register.

21.4.4.5 Fast Bit Error Detection in LIN Mode

Fast bit error detection has been designed to allow flagging of LIN bit errors while they occur, rather than flagging them after a byte transmission has completed. To use this feature, it is assumed a physical interface connects to the LIN bus as shown in Figure 21-14.

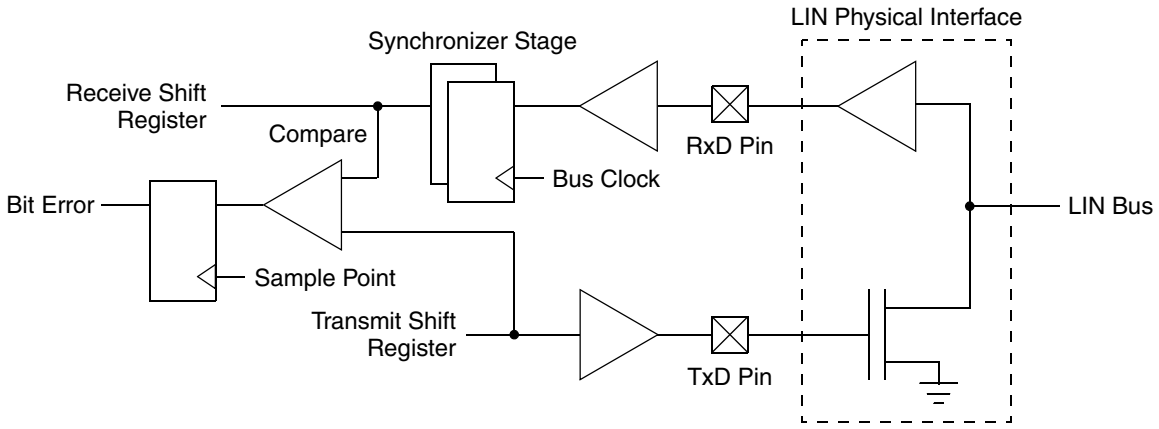


Figure 21-14. Fast Bit Error Detection on a LIN Bus

If fast bit error detection is enabled (FBR = 1), the eSCI compares the transmitted and the received data stream when the transmitter is active (not idle). After a mismatch between the transmitted data and the received data is detected the following actions are performed:

- The LIN frame is aborted (provided LDBG=0).
- The bit error flag BERR is set.
- If SBSTP is 0, the remainder of the byte is transmitted normally.
- If SBSTP is 1, the remaining bits in the byte after the error bit are transmitted as 1s (idle).

To adjust to different bus loads the sample point at which the incoming bit is compared to the one which was transmitted can be selected with the BESM13 bit (refer to Figure 21-15). If set, the comparison is performed at RT clock 13, otherwise at RT clock 9 (refer to Section 21.4.5.3, “Data Sampling.”).

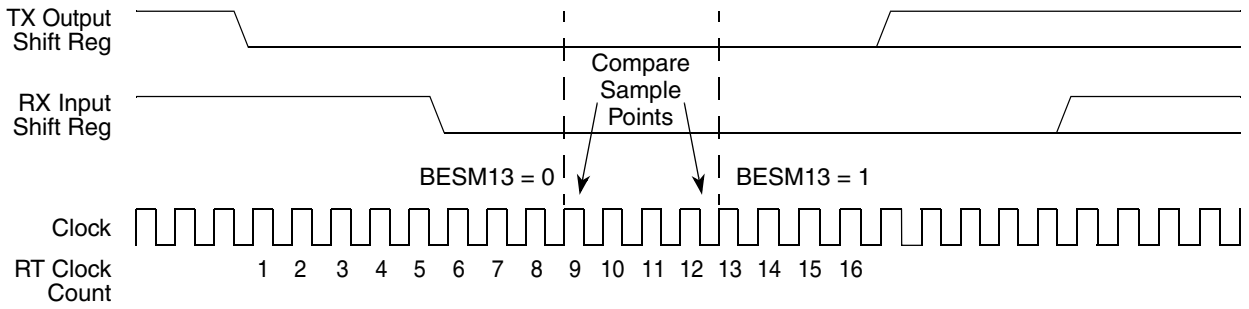


Figure 21-15. Fast Bit Error Detection Timing Diagram

21.4.5 Receiver

Figure 21-16 illustrates the eSCI receiver.

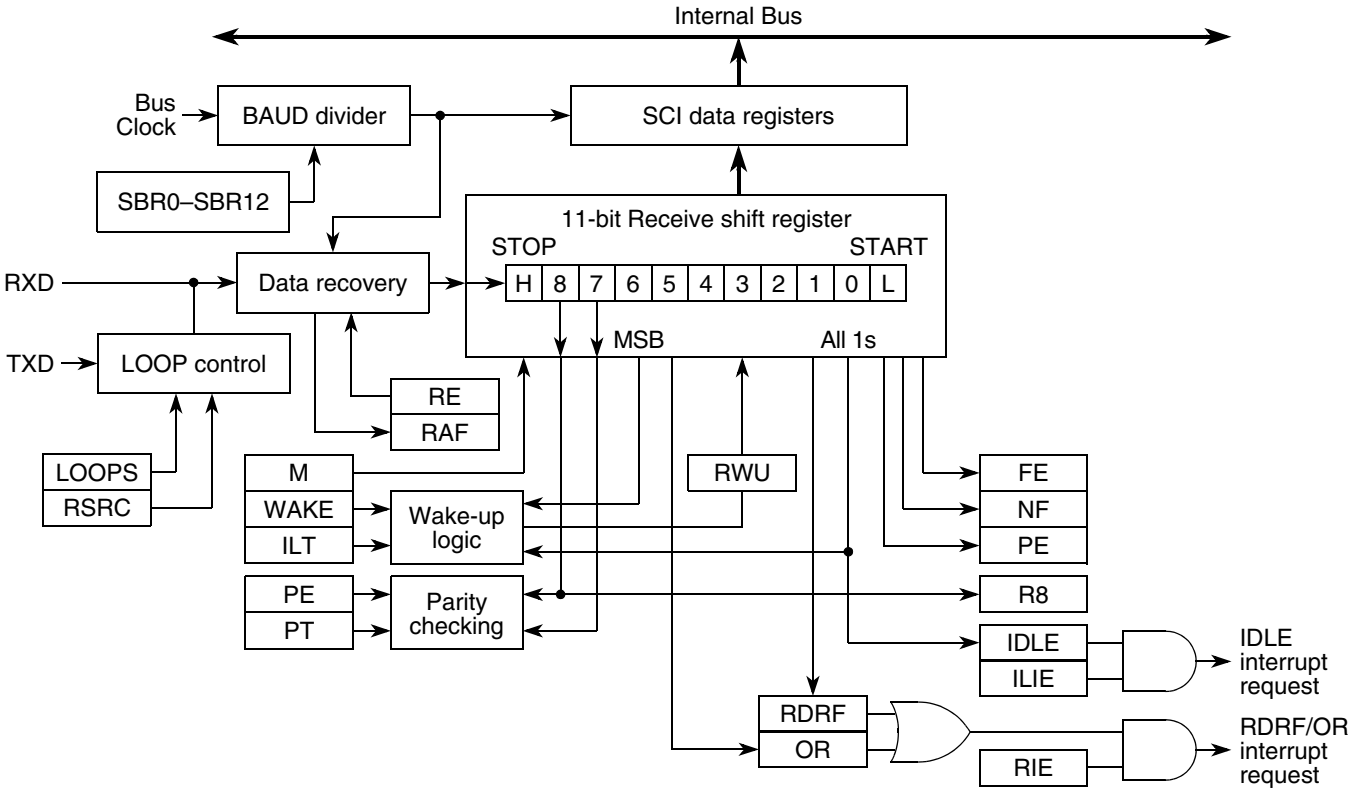


Figure 21-16. eSCI Receiver Block Diagram

21.4.5.1 Receiver Character Length

The eSCI receiver accepts 8-bit or 9-bit data characters. The state of the M bit in eSCI control register 1 (ESCI*x*_CR1) determines the bit-length of data characters. When receiving 9-bit data, bit R8 in the eSCI data register (ESCI*x*_DR) is the ninth bit (bit 8).

21.4.5.2 Character Reception

During an eSCI reception, the receive shift register shifts a frame in from the RXD input signal. The eSCI data register is the buffer (read-only during receive) between the internal data bus and the receive shift register.

After a complete frame shifts into the receive shift register, the data portion of the frame transfers to the eSCI data register. The receive data register full flag, RDRF, in eSCI status register (ESCI*x*_SR) is then set, indicating that the received byte can be read. If the receive interrupt enable bit, RIE, in eSCI control register 1 (ESCI*x*_CR1) is also set, the RDRF flag generates an RDRF interrupt request.

21.4.5.3 Data Sampling

The receiver uses a sampling clock to sample the RXD input signal at the 16 times the baud-rate frequency. This sampling clock is called the RT clock. To adjust for baud rate mismatch, the RT clock is re-synchronized (refer to Figure 21-17).

- After every start bit.
- After the receiver detects a data bit change from logic 1 to logic 0. This data bit change is detected when a majority of data samples return a valid logic 1 and a majority of the next data samples return a valid logic 0. Data samples are taken at RT8, RT9, and RT10, as shown in Figure 21-17.

To locate the start bit, eSCI data recovery logic performs an asynchronous search for a logic 0 preceded by three logic 1s. When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

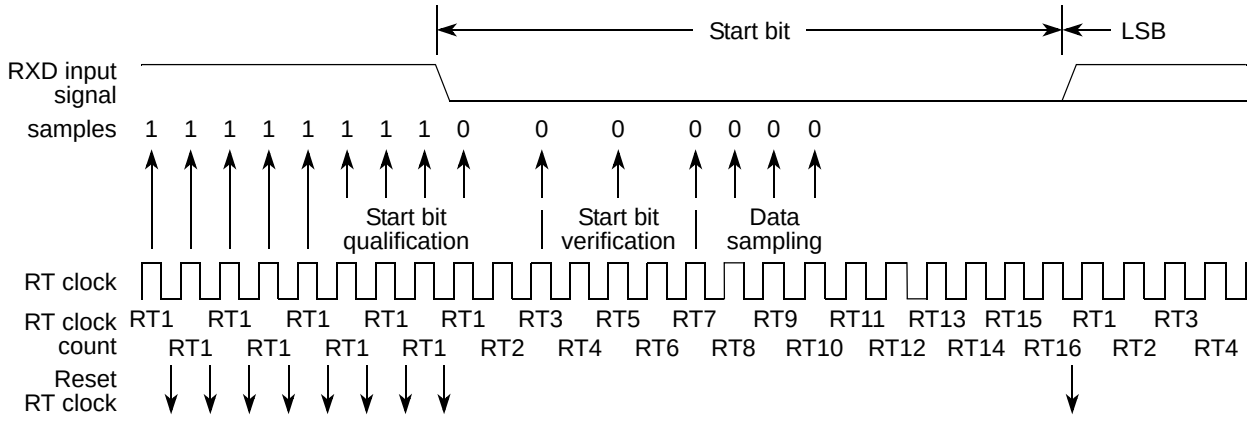


Figure 21-17. Receiver Data Sampling

To verify the start bit and to detect noise, the eSCI data recovery logic takes samples at RT3, RT5, and RT7. Table 21-18 summarizes the results of the start bit verification samples.

Table 21-18. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1

Table 21-18. Start Bit Verification (continued)

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

To determine the value of a data bit and to detect noise, eSCI recovery logic takes samples at RT8, RT9, and RT10. Table 21-19 summarizes the results of the data bit samples.

Table 21-19. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

NOTE

The RT8, RT9, and RT10 samples do not affect start bit verification. If any or all of the RT8, RT9, and RT10 start bit samples are logic 1s following a successful start bit verification, the noise flag (NF) is set.

To verify a stop bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 21-20 summarizes the results of the stop bit samples.

Table 21-20. Stop Bit Recovery

RT8, RT9, and RT10 Samples	Framing Error Flag	Noise Flag
000	1	0
001	1	1
010	1	1
011	0	1
100	1	1
101	0	1

Table 21-20. Stop Bit Recovery (continued)

RT8, RT9, and RT10 Samples	Framing Error Flag	Noise Flag
110	0	1
111	0	0

In Figure 21-18 the verification samples RT3 and RT5 determine that the first low detected was noise and not the beginning of a start bit. The RT clock is reset and the start bit search begins again. The noise flag is not set because the noise occurred before the start bit was found.

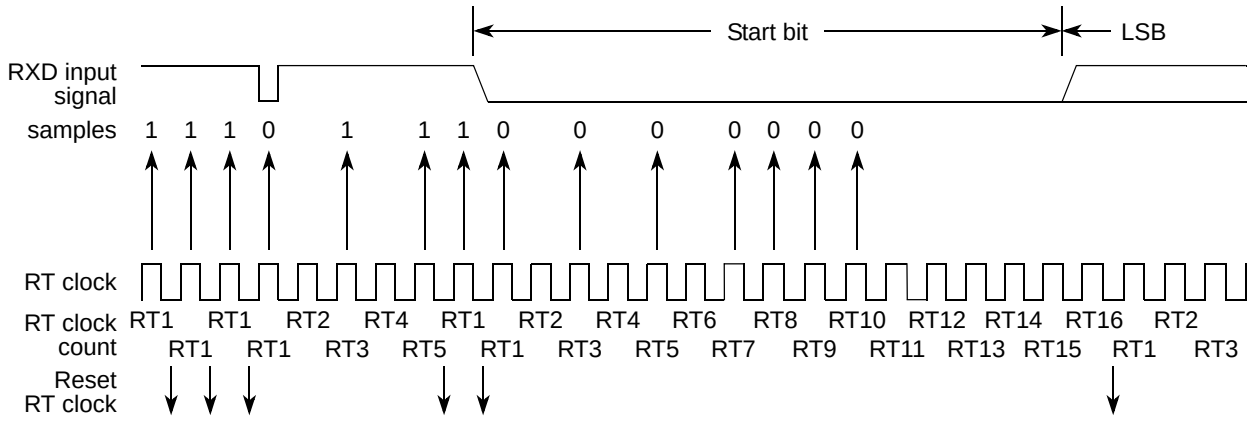


Figure 21-18. Start Bit Search Example 1

21.4.5.4 Framing Errors

If the data recovery logic sets the framing error flag, ESCI*x*_SR[FE], it does not detect a logic 1 where the stop bit should be in an incoming frame. A break character also sets the FE flag because a break character has no stop bit. The FE flag is set at the same time that the RDRF flag is set.

21.4.5.5 Baud Rate Tolerance

When a transmitting device operates at a baud rate below or above the receiver baud rate, accumulated bit-time misalignment can cause one of the three stop bit data samples (RT8, RT9, and RT10) to fall outside the stop bit. A noise error occurs if the RT8, RT9, and RT10 samples are not all the same logical values. A framing error occurs if the receiver clock is misaligned such that the majority of the RT8, RT9, and RT10 stop bit samples are a logic zero.

The receiver samples an incoming frame and re-synchronizes the RT clock on any valid falling edge within the frame. Re-synchronization within frames corrects a misalignment between transmitter bit times and receiver bit times.

21.4.5.5.1 Slow Data Tolerance

Figure 21-19 shows how much a slow received frame can be misaligned without causing a noise error or a framing error. The slow stop bit begins at RT8 instead of RT1 but arrives in time for the stop bit data samples at RT8, RT9, and RT10.

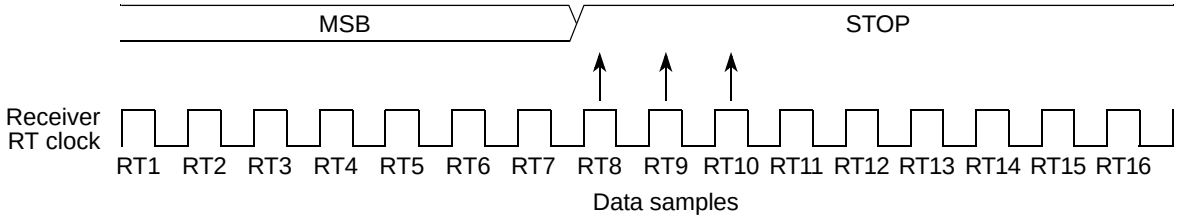


Figure 21-19. Slow Data

For an 8-bit data character, data sampling of the stop bit takes the receiver RT clock 151 clock cycles, as is shown below:

$$9 \text{ bit times} \times 16 \text{ RT cycles} + 7 \text{ RT cycles} = 151 \text{ RT cycles}$$

With the misaligned character shown in Figure 21-19, the receiver counts 151 RT cycles at the point when the count of the transmitting device is 9 bit times x 16 RT cycles = 147 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 8-bit data character with no errors is 4.63%, as is shown below:

$$\frac{151 - 144}{151} \times 100 = 4.63\%$$

For a 9-bit data character, data sampling of the stop bit takes the receiver 167 RT cycles, as is shown below:

$$10 \text{ bit times} \times 16 \text{ RT cycles} + 7 \text{ RT cycles} = 167 \text{ RT cycles}$$

With the misaligned character shown in Figure 21-19, the receiver counts 167 RT cycles at the point when the count of the transmitting device is 10 bit times x 16 RT cycles = 160 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit character with no errors is 4.19%, as is shown below:

$$\frac{167 - 160}{167} \times 100 = 4.19\%$$

21.4.5.5.2 Fast Data Tolerance

Figure 21-20 shows how much a fast received frame can be misaligned. The fast stop bit ends at RT10 instead of RT16 but is still sampled at RT8, RT9, and RT10.

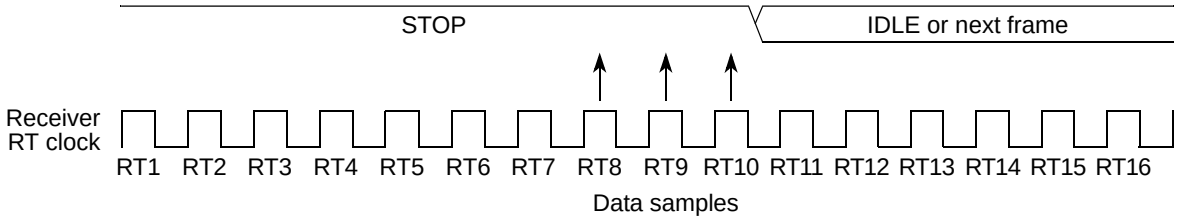


Figure 21-20. Fast Data

For an 8-bit data character, data sampling of the stop bit takes the receiver 154 RT cycles, as is shown below:

$$9 \text{ bit times} \times 16 \text{ RT cycles} + 10 \text{ RT cycles} = 154 \text{ RT cycles}$$

With the misaligned character shown in Figure 21-20, the receiver counts 154 RT cycles at the point when the count of the transmitting device is 10 bit times x 16 RT cycles = 160 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit character with no errors is 3.40%, as is shown below:

$$\frac{160 - 154}{160} \times 100 = 3.40\%$$

For a 9-bit data character, data sampling of the stop bit takes the receiver 170 RT cycles, as shown below:

$$10 \text{ bit times} \times 16 \text{ RT cycles} + 10 \text{ RT cycles} = 170 \text{ RT cycles}$$

With the misaligned character shown in Figure 21-20, the receiver counts 170 RT cycles at the point when the count of the transmitting device is 11 bit times x 16 RT cycles = 176 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit character with no errors is 3.40%, as is shown below:

$$\frac{176 - 170}{176} \times 100 = 3.40\%$$

21.4.5.6 Receiver Wake-up

The receiver can be put into a standby state, which disregards all input requests targeted for other receivers in multiple-receiver systems. Setting the receiver wake-up bit (RWU) in eSCI control register 1 (ESCI*x*_CR1) puts the receiver into the standby state, which disregards all receiver interrupts tar. The eSCI loads the received data into the ESCI*x*_DR, but does not set the receive data register full (RDRF) flag.

The transmitting device can address messages to selected receivers by including addressing information (address bits) in the initial frame or frames of each message. Refer to section Section 21.4.2, "Data Format," for an example of address bits.

The WAKE bit in eSCI control register 1 (ESCI*x*_CR1) determines how the eSCI is brought out of the standby state to process an incoming message. The WAKE bit enables either idle line wake-up or address mark wake-up.

21.4.5.6.1 Idle Input Line Wake-up (WAKE = 0)

Using the receiver idle input line wake-up method allows an idle condition on the RXD signal clears the ESCI*x*_CR1[RWU] bit and wakes up the eSCI. The initial frame or frames of every message contain addressing information. All receivers evaluate the addressing information, and receivers for which the message is addressed process the frames that follow. Any receiver for which a message is not addressed can set its RWU bit and return to the standby state. The RWU bit remains set and the receiver remains on standby until another idle character appears on the RXD signal.

Idle line wake-up requires that messages be separated by at least one idle character and that no message contains idle characters.

The idle character that wakes a receiver does not set the receiver idle bit, ESCI*x*_SR[IDLE], or the receive data register full flag, RDRF.

The idle line type bit, ESCI*x*_CR1[ILT], determines whether the receiver begins counting logic 1s as idle character bits after the start bit or after the stop bit.

21.4.5.6.2 Address Mark Wake-up (WAKE = 1)

Using the address mark wake-up method allows a logic 1 in the most significant bit (MSB) position of a frame to clear the RWU bit and wake-up the eSCI. The logic 1 in the msb position marks a frame as an address frame that contains addressing information. All receivers evaluate the addressing information, and the receivers for which the message is addressed process the frames that follow. Any receiver for which a message is not addressed can set its RWU bit and return to the standby state. The RWU bit remains set and the receiver remains on standby until another address frame appears on the RXD signal.

The logic 1 msb of an address frame clears the receiver's RWU bit before the stop bit is received and sets the RDRF flag.

Address mark wake-up allows messages to contain idle characters but requires that the msb be reserved for use in address frames.

NOTE

With the WAKE bit clear, setting the RWU bit after the RXD signal has been idle can cause the receiver to wake-up immediately.

21.4.6 Single-Wire Operation

Normally, the eSCI uses two pins for transmitting and receiving. In single-wire operation, the RXD pin is disconnected from the eSCI. The eSCI uses the TXD pin for both receiving and transmitting.

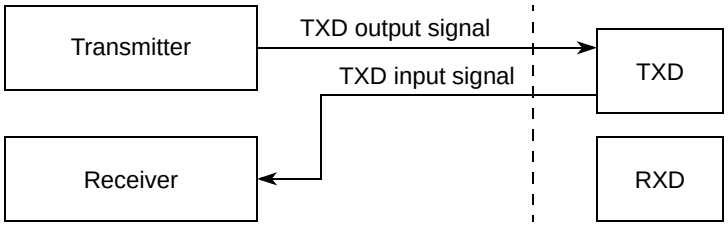


Figure 21-21. Single-Wire Operation (LOOPS = 1, RSRC = 1)

Enable single-wire operation by setting the LOOPS bit and the receiver source bit, RSRC, in eSCI control register 1 (ESCI*x*_CR1). Setting the LOOPS bit disables the path from the RXD signal to the receiver. Setting the RSRC bit connects the receiver input to the output of the TXD pin driver.

During reception, both the transmitter and receiver must be enabled (TE = 1 and RE = 1). The SIU_PCR89[PA] and SIU_PCR91[PA] bits must be set to select the TXD function for the relevant eSCI module, and the TXD pin should be set for open drain operation (SIU_PCR*nn*[ODE] = 1). Optionally, if the external transmitting device is also open drain, a weak pullup can be enabled.

Refer to Section 6.3.1.12, “Pad Configuration Registers (SIU_PCR)”.

During transmission, the transmitter must be enabled (TE = 1); the receiver can be enabled or disabled. If the receiver is enabled (RE = 1), transmissions are echoed back on the receiver. Set or clear open drain output enable depending on desired operation.

21.4.7 Loop Operation

In loop operation the transmitter output goes to the receiver input. The RXD signal is disconnected from the eSCI.

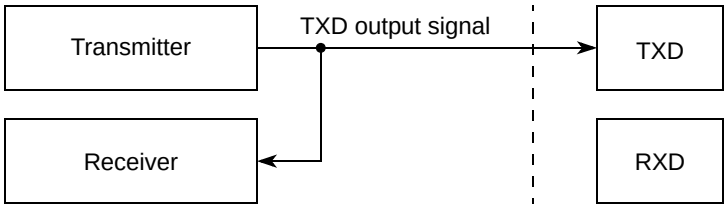


Figure 21-22. Loop Operation (LOOPS = 1, RSRC = 0)

Enable loop operation by setting the LOOPS bit and clearing the RSRC bit in eSCI control register 1 (ESCI*x*_CR1). Setting the LOOPS bit disables the path from the RXD signal to the receiver. Clearing the RSRC bit connects the transmitter output to the receiver input. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).

21.4.8 Modes of Operation

21.4.8.1 Run Mode

Run mode is the normal operating mode.

21.4.8.2 Disabling the eSCI

The module disable bit (ESCIx_CR2[MDIS]) in the eSCI control register 2 can be used to turn off the eSCI. This saves power by stopping the eSCI core from being clocked. By default the eSCI is enabled (ESCIx_CR2[MDIS]=0).

21.4.9 Interrupt Operation

Only the eSCI originates interrupt requests. The following sections describe how the eSCI generates a request and how the MCU acknowledges that request. The eSCI only has a single interrupt line (eSCI interrupt signal, active high operation) and all the following interrupts, when generated, are ORed together and issued through that port.

21.4.9.1 Interrupt Sources

There are several interrupt sources that can generate an eSCI interrupt to the CPU. They are listed with details and descriptions in Table 21-21.

Table 21-21. eSCI Interrupt Flags, Sources, Mask Bits, and Descriptions

Interrupt Source	Flag	Description	Source	Local Enable
Transmitter	TDRE	Indicates that a byte was transferred from ESCIx_DR to the transmit shift register. The transmit data register empty (TDRE) interrupt is set high by the eSCI when the transmit shift register receives data, 8 or 9 bits, from the eSCI data register, ESCI*x*_DR. A TDRE interrupt indicates that the transmit data register (ESCI*x*_DR) is empty and that a new data can be written to the ESCI*x*_DR for transmission. The TDRE bit is cleared by writing a one to the TDRE bit location in the ESCI*x*_SR.	ESCI*x*_SR[0]	TIE
Transmitter	TC	Indicates that a transmit is complete. The transmit complete (TC) interrupt is set by the eSCI when a transmission has completed. A TC interrupt indicates that there is no transmission in progress. TC is set high when the TDRE flag is set and no data, preamble, or break character is being transmitted. When TC is set, the TXD pin becomes idle (logic 1). The TC bit is cleared by writing a one to the TC bit location in the ESCI*x*_SR.	ESCI*x*_SR[1]	TCIE
Receiver	RDRF	Indicates that received data is available in the eSCI data register. The receive data register full (RDRF) interrupt is set when the data in the receive shift register transfers to the eSCI data register. An RDRF interrupt indicates that the received data has been transferred to the eSCI data register and that the received data can now be read by the MCU. The RDRF bit is cleared by writing a one to the RDRF bit location in the ESCI*x*_SR.	ESCI*x*_SR[2]	RIE
Receiver	IDLE	Indicates that receiver input has become idle. The idle line (IDLE) interrupt is set when 10 consecutive logic 1s (if M = 0) or 11 consecutive logic 1s (if M = 1) appear on the receiver input. After the IDLE is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag. The IDLE bit is cleared by writing a one to the IDLE bit location in the ESCI*x*_SR.	ESCI*x*_SR[3]	ILIE

Table 21-21. eSCI Interrupt Flags, Sources, Mask Bits, and Descriptions (continued)

Interrupt Source	Flag	Description	Source	Local Enable
Receiver	OR	Indicates that an overrun condition has occurred. The overrun (OR) interrupt is set when software fails to read the eSCI data register before the receive shift register receives the next frame. The newly acquired data in the shift register is lost in this case, but the data already in the eSCI data registers is not affected.The OR bit is cleared by writing a one to the OR bit location in the ESCI*x*_SR.	ESCI*x*_SR[4]	ORIE
Receiver	NF	Detect noise error on receiver input. The NF interrupt is set when the eSCI detects noise on the receiver input.	ESCI*x*_SR[5]	NFIE
Receiver	FE	Framing error has occurred. The interrupt is set when the stop bit is read as a 0; which violates the SCI protocol. FE is cleared by writing it with 1.	ESCI*x*_SR[6]	FEIE
Receiver	PF	Parity of received data does not match parity bit; parity error has occurred. The interrupt is set when the parity of the received data is not correct. PF is cleared by writing it with 1.	ESCI*x*_SR[7]	PFIE
LIN	BERR	Detected a bit error, only valid in LIN mode. While the eSCI is in LIN mode, the bit error (BERR) flag is set when one or more bits in the last transmitted byte is not read back with the same value. The BERR flag is cleared by writing a 1 to the bit. A bit error causes the LIN FSM to reset. Clear the BERR flag by writing a 1 to the bit.	ESCI*x*_SR[11]	IEBERR
LIN	RXRDY	Indicates LIN hardware has received a data byte. While in LIN mode, the receiver ready (RXRDY) flag is set when the eSCI receives a valid data byte in an RX frame. RXRDY is not set for bytes which the receiver obtains by reading back the data which the LIN finite state machine (FSM) has sent out. Clear the RXRDY flag by writing a 1 to the bit.	ESCI*x*_SR[16]	RXIE
LIN	TXRDY	Indicates LIN hardware can accept a control or data byte. While in LIN mode, the transmitter ready (TXRDY) flag is set when the eSCI can accept a control or data byte. Clear the TXRDY flag by writing a 1 to the bit.	ESCI*x*_SR[17]	TXIE
LIN	LWAKE	A wake-up character has been received from a LIN frame. The LIN wake-up (LWAKE) flag is set when the LIN hardware receives a wake-up character sent by one of the LIN slaves. This occurs only when the LIN bus is in sleep mode. Clear the LWAKE flag by writing a 1 to the bit.	ESCI*x*_SR[18]	WUIE
LIN	STO	The response of the slave has been too slow (slave timeout). The slave timeout (STO) flag is set during an RX frame when the LIN slave has not transmitted all requested data bytes before the specified timeout period. Clear the STO flag by writing a 1 to the bit.	ESCI*x*_SR[19]	STIE
LIN	PBERR	Physical bus error detected. If the RXD input remains at the same value for 15 cycles after a transmission has started, the LIN hardware sets the physical bus error (PBERR) flag. Clear the PBERR flag by writing a 1 to the bit.	ESCI*x*_SR[20]	PBIE
LIN	CERR	CRC error detected. If an RX frame has the CRC checking flag set, and the two CRC bytes do not match the calculated CRC pattern, the CRC error (CERR) flag is set. Clear the CERR flag by writing a 1 to the bit.	ESCI*x*_SR[21]	CIE

Table 21-21. eSCI Interrupt Flags, Sources, Mask Bits, and Descriptions (continued)

Interrupt Source	Flag	Description	Source	Local Enable
LIN	CKERR	Checksum error detected. If an RX frame has the checksum checking flag set and the last byte does not match the calculated checksum, the checksum error (CKERR) flag is set. Clear the CKERR flag by writing a 1 to the bit.	ESCI*x*_SR[22]	CKIE
LIN	FRC	LIN frame completed. The frame complete (FRC) flag is set after the last byte of a TX frame is transmitted, or after the last byte of an RX frame is received. The FRC flag indicates that the next frame can be set up. Clear the FRC flag by writing a 1 to the bit. **Note:** The last byte of an outgoing TX frame or incoming RX frame indicates that the checksum comparison occurred. **Note:** It is possible to set the FRC flag before the DMA controller has completed transferring the last byte from the eSCI port to system memory. Do not set the FRC flag if the frame will be processed. For frames that will be processed, use the DMA controller interrupt.	ESCI*x*_SR[23]	FCIE
LIN	OVFL	ESCIx_LRR overflow. The overflow (OVFL) flag is set when a byte is received in the ESCI*x*_LRR before the previous byte is read. Since the system is responsible for reading the register before the next byte arrives, this condition indicates a problem with CPU load. The OVFL flag is cleared by writing a 1 to the bit.	ESCI*x*_SR[31]	OFIE

21.4.10 Using the LIN Hardware

The eSCI provides special support for the LIN protocol. It can be used to automate most tasks of a LIN master. In conjunction with the DMA interface it is possible to transmit entire frames (or sequences of frames) and receive data from LIN slaves without any CPU intervention. There is no special support for LIN slave mode. If required, LIN slave mode can be implemented in software.

A LIN frame consists of a break character (10 or 13 bits), a sync field, an ID field, *n* data fields (*n* could be 0) and a checksum field. The data and checksum bytes are either provided by the LIN master (TX frame) or by the LIN slave (RX frame). The header fields are always generated by the LIN master.

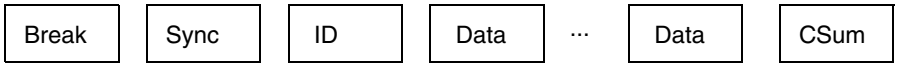


Figure 21-23. Typical LIN frame

The LIN hardware is highly configurable. This configurability allows the eSCI's LIN hardware to generate frames for LIN slaves from all revisions of the LIN standard. The settings are adjusted according to the capabilities of the slave device.

To activate the LIN hardware, the LIN mode bit in the ESCI*x*_LCR needs to be set. Other settings, such as double stop flags after bit errors and automatic parity bit generation, are also available for use in LIN mode.

The eSCI settings must be made according to the LIN specification. The eSCI must be configured for 2-wire operation (2 wires connected to the LIN transceiver) with 8 data bytes and no parity. Normally a 13-bit break is used, but the eSCI can also be configured for 10-bit breaks as required by the application.

21.4.10.1 Features of the LIN Hardware

The eSCI's LIN hardware has several features to support different revisions of the LIN slaves. The ESCI*x*_LTR can be configured to include or not include header bits in the checksum on a frame by frame basis. This feature supports LIN slaves with different LIN revisions. The LIN control register allows the application to automatically calculate the parity bits in the ID field and insert double stop flags a bit error. The BRK13 bit in ESCI*x*_CR2 decides whether to generate 10 or 13 bit break characters.

NOTE

LIN 2.0 requires a 13-bit break character. Set the BRK13 bit to 1. The eSCI bus works when BRK13 = 0, but the setting does not comply with LIN 2.0.

The application software can disable checksum generation/verification for individual frames to perform the functions externally and use the LIN hardware to append two CRC bytes (Figure 21-24). Although the LIN standard does not include CRCs, CRCs are processed as data bytes by the LIN protocol. CRCs are used in software applications that process very large frames. The eSCI and FlexCAN modules use the same CRC polynomial, the LIN protocol processes CAN bytes as data bytes.

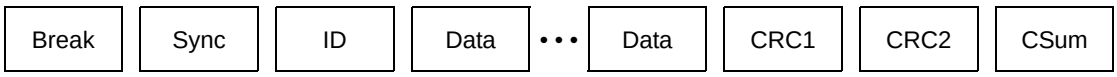


Figure 21-24. LIN Frame with CRC bytes

To force a resync of the LIN FSM, use the LRES bit in the LIN control register. Typically LIN hardware automatically discards the frame when a bit error is detected.

21.4.10.2 Generating a TX Frame

The following procedure describes how a basic TX frame is generated.

The frame is controlled via the LIN transmit register (ESCI*x*_LTR). Initially, the application software must check the TXRDY bit (either using an interrupt, the TX DMA interface, or by polling the LIN status register). If TXRDY is set, the register is writable. Before each write, TXRDY must be checked (though this step is performed automatically in DMA mode). The first write to the ESCI*x*_LTR must contain the LIN ID field. The next write to ESCI*x*_LTR specifies the length of the frame (0 to 255 Bytes). The third write to ESCI*x*_LTR contains the control byte (frame direction, checksum/CRC settings). Note that timeout bits are not included in TX frames, since they only refer to LIN slaves. The three previously mentioned writes to the ESCI*x*_LTR specify the LIN frame data. After the LIN frame data is specified, the eSCI LIN hardware starts to generate a LIN frame.

First, the eSCI transmits a break field. The sync field is transmitted next. The third field is the ID field. After these three fields have been broadcast, the ESCIx_LTR accepts data bytes; the LIN hardware transmits these data bytes as soon as they are available and can be sent out. After the last step the LIN hardware automatically appends the checksum field.

It is possible to set up a DMA channel to handle all the tasks required to send a TX frame. For this operation, the TX DMA channel must be activated by setting the ESCI*x*_CR2[TXDMA] bit. The control information for the LIN frame (ID, message length, TX/RX type, timeout, etc.) and the data bytes are stored at an appropriate memory location. The DMA controller is then set up to transfer this block of memory to a location (the ESCI*x*_LTR). After transmission is complete, either the DMA controller or the LIN hardware can generate an interrupt to the CPU.

NOTE

In contrast to the standard software implementation where each byte transmission requires several interrupts, the DMA controller and eSCI handle communication, bit error and physical bus error checking, checksum, and CRC generation (checking on the RX side).

Refer to Figure 21-25 for more information.

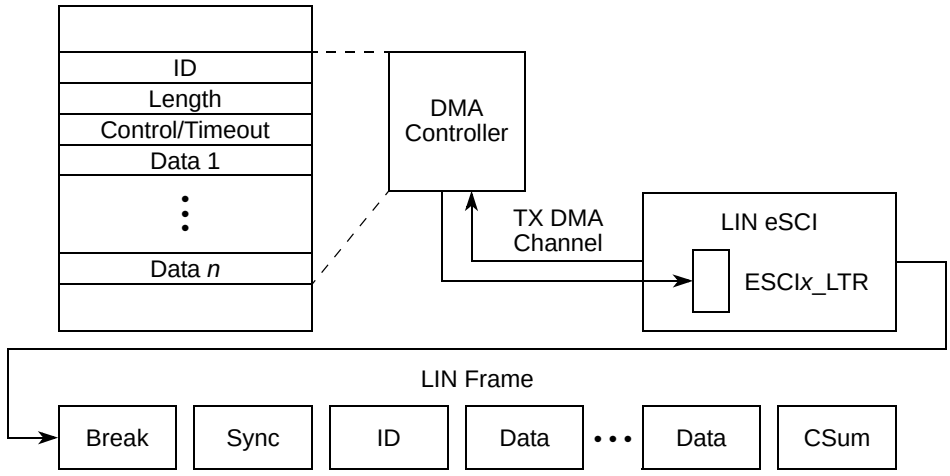


Figure 21-25. DMA Transfer of a TX Frame

21.4.10.3 Generating an RX Frame

For RX frames the header information is provided by the LIN master. The data, CRC and checksum bytes (as enabled) are provided by the LIN slave. The LIN master verifies CRC and checksum bytes transmitted by the slave.

For an RX frame, control information must be written to the ESCI*x*_LTR in the same manner as for the TX frames. Additionally the timeout bits, which define the time to complete the entire frame, must be written. Then the ESCI*x*_SR[RXRDY] bit must be checked (either with an interrupt, RX DMA interface, or by polling) to detect incoming data bytes. The checksum byte normally does not appear in the ESCI*x*_LRR, instead the LIN hardware verifies the checksum and issue an interrupt, if the checksum value is not correct.

Two DMA channels can be used when executing an RX frame: one to transfer the header/control information from a memory location to the ESCI*x*_LTR, and one to transfer the incoming data bytes from the ESCI*x*_LRR to a table in memory. After the last byte from the RX frame has been stored, the DMA controller can indicate completion to the CPU.

NOTE

It is also possible to setup a whole sequence of RX and TX frames, and generate a single event at the end of that sequence.

Refer to Figure 21-26 for more information.

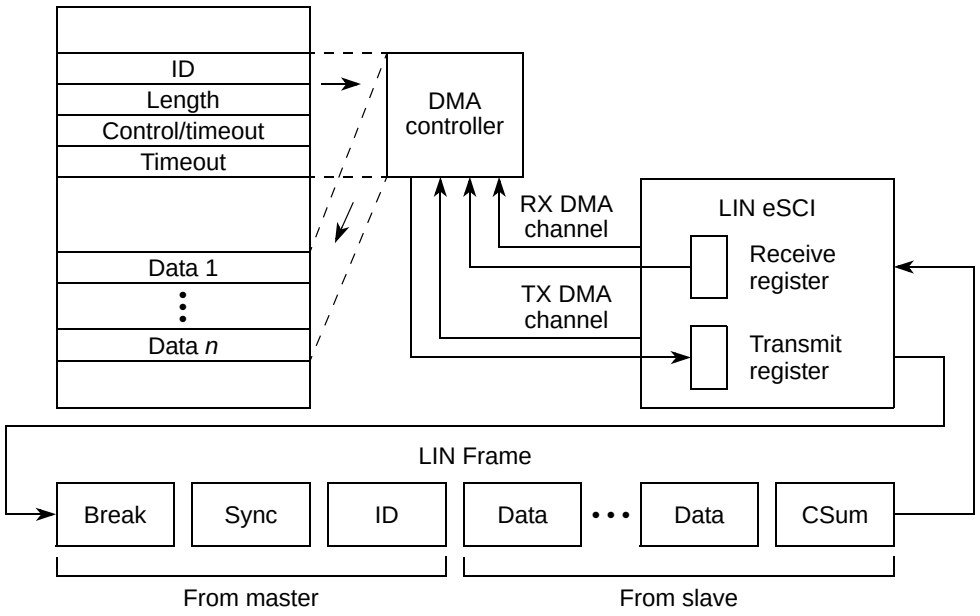


Figure 21-26. DMA Transfer of an RX frame

21.4.10.4 LIN Error Handling

The LIN hardware can detect several error conditions of the LIN protocol. LIN hardware receives all transmitted bytes, and compares the values with expected values to determine if the data is valid. If a mismatch occurs, a bit error is generated and the LIN FSM returns to its start state.

For an RX frame the LIN hardware can detect a slave timeout error. The exact slave timeout error value can be set via the timeout bits in the ESCI*x*_LTR. If the frame is not complete within the number of clock cycles specified in the register, the LIN FSM returns to its start state, and the STO interrupt is issued.

The LIN protocol supports a sleep mode. After 25,000 bus cycles of inactivity the bus is assumed to be in sleep mode. Normally entering sleep mode can be avoided, if the LIN master is regularly creating some bus activity. Otherwise the timeout state needs to be detected by the application software, for example by setting a timer.

Both LIN masters and LIN slaves can cause the bus to exit sleep mode by sending a break signal. The LIN hardware generates a break when the WU bit in the LIN control register is written. After transmitting the break, data is not sent out (TXRDY = 0) until the wake-up period expires. Define the wakeup period using the WUD bits in the LIN control register.

Break signals sent by a LIN slave are received by the LIN hardware, and so indicated by setting the WAKE flag in the LIN status register.

A physical bus error (LIN bus is permanently stuck at a fixed value) sets several error flags. If the input is permanently low, the eSCI sets the framing error (FE) flag in the eSCI status register. If the RXD input remains at the same value for 15 cycles after a transmission starts, the LIN hardware sets the PBERR flag in the LIN status register. A bit error can also occur.

21.4.10.5 LIN Setup

Since the eSCI is for general-purpose use, some of the settings are not applicable for LIN operation. The following setup applies for most applications, regardless of which kind of LIN slave is addressed:

1. Enable the module by clearing the ESCI*x*_CR2[MDIS] bit to 0.
2. Enable transmit and receive by setting ESCI*x*_CR1[TE] = 1, ESCI*x*_CR1[RE] = 1.
3. Clear the data format bit (ESCI*x*_CR1[M] = 0) to select 8 data bits, and disable the parity bit (PE = 0).
4. Use the LIN interrupts by clearing the interrupt enable bits: ESCI*x*_CR1[TIE], ESCI*x*_CR1[TCIE], and ESCI*x*_CR1[RIE]. Select LIN mode by setting ESCI*x*_LCR[LIN] = 1.
5. Set the break character (ESCI*x*_CR2[BRK13] = 1) to comply with the LIN standard requirements. The eSCI works when BRK13 = 0, but violates LIN 2.0.
6. Bit errors are commonly configured to: reset the LIN FSM, immediately stop bus transfers, and suspend DMA requests until the BERR flag is cleared. Use the following bit settings to perform these functions: ESCI*x*_LCR[LDBG] = 0, ESCI*x*_CR2[SBSTP] = 1, and ESCI*x*_CR2[BSTP] = 1.
7. Fast bit error detection provides superior error checking. Set ESCI*x*_CR2[FBR]; it is commonly used with ESCI*x*_CR2[BESM13] = 1.
8. If available, enable a pulldown on the RX input. (If the transceiver fails, the RX pin does not float).
9. Enable the following error indicators NF, FE, BERR, STO, PBERR, CERR, CKERR, and OVFL.
10. Transmit a wake-up character on the LIN bus to activate the LIN slaves.

Other settings like baud rate, length of break character etc., depend on the LIN slaves to which the eSCI is connected.

Chapter 22
FlexCAN2 Controller Area Network

22.1 Introduction

The device MCU contains four controller area network (FlexCAN2) modules. Each FlexCAN2 module is a communication controller implementing the CAN protocol according to CAN Specification version 2.0B and ISO Standard 11898.

Each FlexCAN2 module contains a 1024-byte embedded memory, capable of storing up to 64 message buffers (MBs). The respective functions are described in subsequent sections.

This FlexCAN2 version implements individual mask registers and a reception queue thereby allowing queuing of received frames before requiring interrupt processing. Also included is a feature for disabling self-reception of TX frames.

22.1.1 Block Diagram

A general block diagram is shown in Figure 22-1, which describes the main submodules implemented in the FlexCAN2 module, including an embedded RAM for up to 64 message buffers.

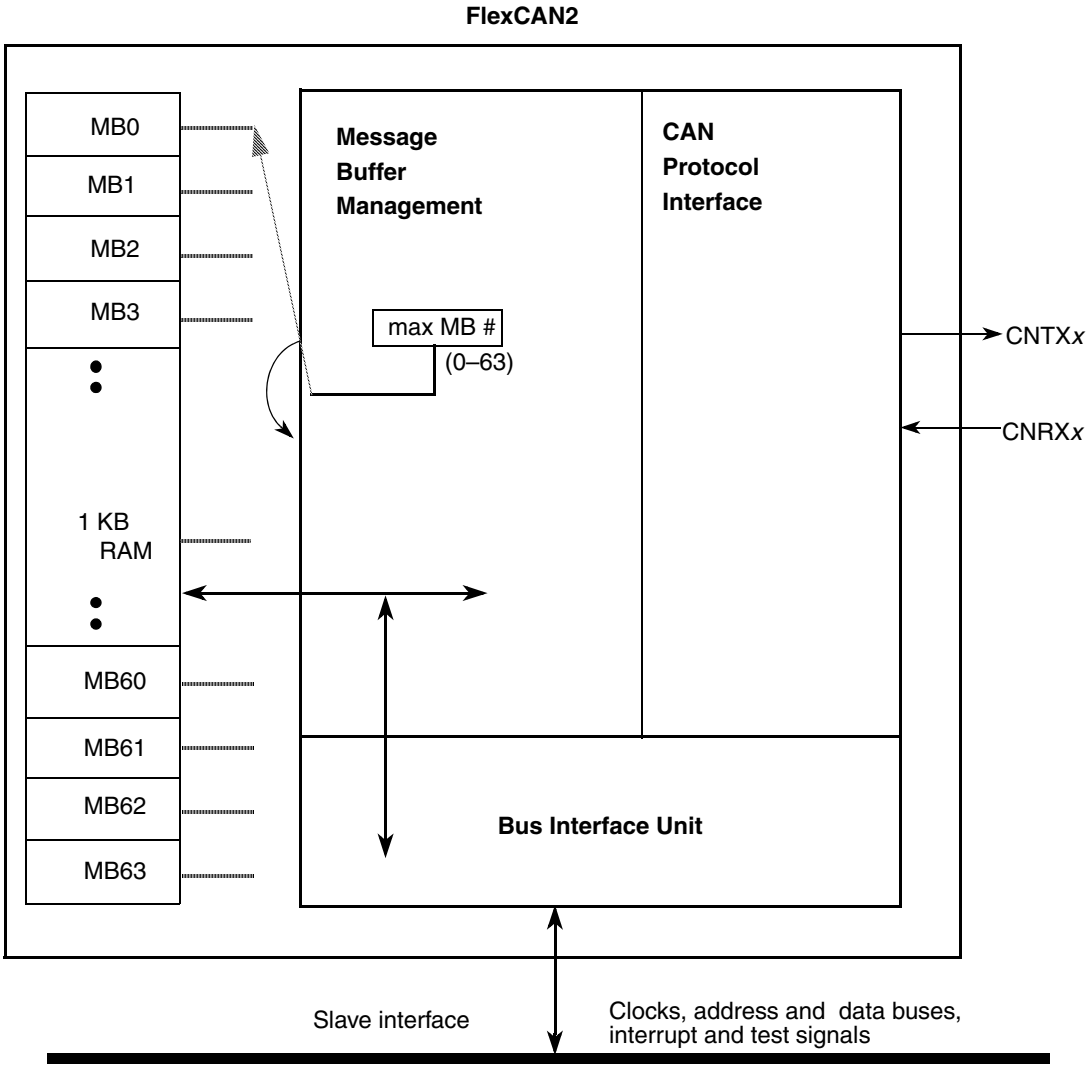


Figure 22-1. FlexCAN2 Block Diagram

22.1.2 Overview

The CAN protocol was designed primarily, but not exclusively, to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN2 module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames. Sixty-four message buffers (MBs) are stored in an embedded 1024-byte RAM dedicated to the FlexCAN2 module.

The CAN protocol interface (CPI) manages the serial communication on the CAN bus, requesting RAM access for receiving and transmitting message frames, validating received messages and performing error handling. The message buffer management (MBM) handles message buffer selection for reception and transmission, taking care of arbitration and ID matching algorithms. The bus interface unit (BIU) controls the access to and from the internal interface bus, to establish connection to the CPU and to any other modules. Clocks, address and data buses, interrupt outputs and test signals are accessed through the bus interface unit.

22.1.3 Features

The FlexCAN2 module includes these distinctive features:

- Based on and includes all existing features of the Freescale TouCAN module
- Reception queue available by setting more than one RX message buffer with the same ID
- Programmable for global (compatible with previous versions) or individual receive ID masking
- Maskable self-reception by setting MCR[SRXDIS]
- Full implementation of the CAN protocol specification, version 2.0B
  - — Standard data and remote frames
  - — Extended data and remote frames
  - — Data length of 0–8 bytes
  - — Programmable bit rate up to 1 Mb/sec
- Content-related addressing
- 64 flexible message buffers of 0–8 bytes data length
- Each MB configurable as RX or TX, all supporting standard and extended messages
- Includes 1024 bytes of RAM used for message buffer storage
- Programmable clock source to the CAN protocol interface, either system clock or oscillator clock
- Listen-only mode capability
- Programmable loop-back mode supporting self-test operation
- Three programmable mask registers are turned off by default:
  - — Global
  - — RX Buffer 14
- RX Buffer 15Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- Multi master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages

22.1.4 Modes of Operation

The device supports four FlexCAN functional modes: normal, freeze, listen-only and loop-back. One low power mode, module disabled, is supported.

22.1.4.1 Normal Mode

In normal mode, the module operates receiving and/or transmitting message frames, errors are handled normally and all the CAN protocol functions are enabled. In this device, there is no distinction between user and supervisor modes.

22.1.4.2 Freeze Mode

Freeze mode is entered when the FRZ bit in the module configuration register (CAN*x*_MCR) is asserted while the HALT bit in the CAN*x*_MCR is set or debug mode is requested by the NPC. In freeze mode no transmission or reception of frames is done, and synchronization with the CAN bus is lost. See Section 22.4.6.1, “Freeze Mode,” for more information.

22.1.4.3 Listen-Only Mode

The module enters this mode when the LOM bit in the CAN*x*_CR is asserted. In this mode, FlexCAN operates in a CAN error passive mode, freezing all error counters and receiving messages without sending acknowledgments.

22.1.4.4 Loop-Back Mode

The module enters this mode when the LPB bit in the CAN*x*_CR is asserted. In this mode, FlexCAN performs an internal loop back that can be used for self test operation. The bit stream output of the transmitter is internally fed back to the receiver input. The CAN receive input pin (CNRX*x*) is ignored and the transmit output (CNTX*x*) goes to the recessive state (logic 1). FlexCAN behaves as it normally does when transmitting, and treats its own transmitted message as a message received from a remote node. In this mode, FlexCAN ignores the bit sent during the ACK slot in the CAN frame acknowledge field to ensure proper reception of its own message. Both transmit and receive interrupts are generated.

22.1.4.5 Module Disabled Mode

This low power mode is entered when the MDIS bit in the CAN_MCR is asserted. When disabled, the module shuts down the clocks to the CAN protocol interface and message buffer management submodules. Exit from this mode is done by negating the CAN_MCR[MDIS] bit. See Section 22.4.6.2, “Module Disabled Mode,” for more information.

22.2 External Signal Description

22.2.1 Overview

The FlexCAN2 module has two I/O signals connected to the external MCU pins. These signals are summarized in Table 22-1 and described in more detail in the next sub-sections.

Table 22-1. FlexCAN2 Signals

Signal Name[1]	Direction	Description
CNRX*x*	I	CAN receive
CNTX*x*	O	CAN transmit

1 *x* indicates FlexCAN2 module A, B, C, or D.

22.2.2 Detailed Signal Description

22.2.2.1 CNRX*x*

This pin is the receive pin to the CAN bus transceiver. The dominant state is represented by logic level 0. The recessive state is represented by logic level 1.

22.2.2.2 CNTX*x*

This pin is the transmit pin to the CAN bus transceiver. The dominant state is represented by logic level 0. The recessive state is represented by logic level 1.

22.3 Memory Map/Register Definition

This section describes the registers and data structures in the FlexCAN2 module. The addresses presented are relative to the base address of the module.

The address space occupied by FlexCAN2 is contiguous:

- 128 bytes for registers starting at the module base address
- Extra space for message buffer storage
- 1024 bytes for 64 message buffers

22.3.1 Memory Map

The complete memory map for a FlexCAN2 module with its 64 MBs is shown in Table 22-2. Except for the base addresses, the four FlexCAN2 modules have identical memory maps. Each individual register is identified by its complete name and the corresponding mnemonic.

Table 22-2. Module Memory Map

Address	Register Name	Register Description	Bits
Base = 0xFFFC_0000 (A) Base = 0xFFFC_4000 (B) Base = 0xFFFC_8000 (C) Base = 0xFFFC_C000 (D)	CAN*x*_MCR	Module configuration register	32
Base + 0x0004	CAN*x*_CR	Control register	32
Base + 0x0008	CAN*x*_TIMER	Free running timer	32
Base + 0x000C	—	Reserved	—
Base + 0x0010	CAN*x*_RXGMASK	RX global mask	32
Base + 0x0014	CAN*x*_RX14MASK	RX buffer 14 mask	32
Base + 0x0018	CAN*x*_RX15MASK	RX buffer 15 mask	32
Base + 0x001C	CAN*x*_ECR	Error counter register	32
Base + 0x0020	CAN*x*_ESR	Error and status register	32
Base + 0x0024	CAN*x*_IMRH	Interrupt masks high register	32
Base + 0x0028	CAN*x*_IMRL	Interrupt masks low register	32
Base + 0x002C	CAN*x*_IFRH	Interrupt flags high register	32
Base + 0x0030	CAN*x*_IFRL	Interrupt flags low register	32
Base + (0x0034–0x005F)	—	Reserved	—
Base + (0x0060–0x007F)	—	Reserved	—
Base + (0x0080–0x017F)	MB0–MB15	Message buffers 0–15	128 per buffer
Base + (0x0180–0x027F)	MB16–MB31	Message buffers 16–31	128 per buffer
Base + (0x0280–0x047F)	MB32–MB63	Message buffers 32–63	128 per buffer
Base + (0x0880–0x08BF)	CANx_RXIMR0–CANx_RXIMR15	RX individual mask register 0–15	32
Base + (0x08C0–0x08FF)	CANx_RXIMR16–CANx_RXIMR31	RX individual mask register 16–31	32
Base + (0x0900–0x097F)	CANx_RXIMR32–CANx_RXIMR63	RX individual mask register 32–63	32

The FlexCAN2 module stores CAN messages for transmission and reception using a message buffer structure. Each individual MB is formed by 16 bytes of memory mapped as described in Table 22-3. The FlexCAN2 module can manage up to 64 message buffers. Table 22-3 shows the standard and extended message buffer (MB0) memory map, using 16 bytes (0x80–0x8F) total space.

Table 22-3. Message Buffer MB0 Memory Mapping

Address Offset	MB Field
0x80	Control and status (C/S)
0x84	Identifier field
0x88–0x8F	Data fields 0–7 (1 byte each)

NOTE

Reading the control and status word (first word) of a message buffer locks it from receiving further messages until it is unlocked by reading: another message buffer, or the timer.

22.3.2 Message Buffer Structure

The message buffer structure used by the FlexCAN2 module is represented in Figure 22-2. Both extended and standard frames (29-bit and 11-bit identifier, respectively) used in the CAN specification (version 2.0 Part B) are represented.

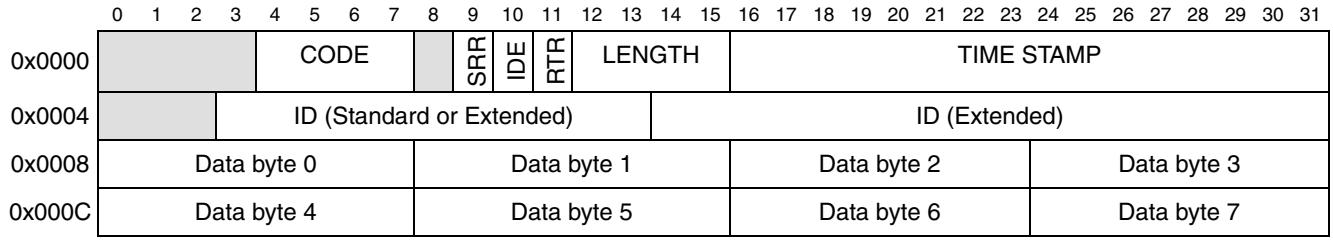


Figure 22-2. Message Buffer Structure

Table 22-4. Message Buffer Field Descriptions

Name	Description
CODE	Message buffer code. This 4-bit field can be accessed (read or write) by the CPU and by the FlexCAN2 module itself, as part of the message buffer matching and arbitration process. The encoding is shown in Table 22-5 and Table 22-6. See Section 22.4, “Functional Description,” for additional information.
SRR	Substitute remote request. Fixed recessive bit, used only in extended format. It must be set to ‘1’ by the user for transmission (TX Buffers) and is stored with the value received on the CAN bus for RX receiving buffers. It can be received as either recessive or dominant. If FlexCAN2 receives this bit as dominant, then it is interpreted as arbitration loss. 0 Dominant is not a valid value for transmission in extended format frames 1 Recessive value is compulsory for transmission in extended format frames
IDE	ID extended bit. This bit identifies whether the frame format is standard or extended. 0 Frame format is standard 1 Frame format is extended

Table 22-4. Message Buffer Field Descriptions (continued)

Name	Description
RTR	Remote transmission request. This bit is used for requesting transmissions of a data frame. If FlexCAN2 transmits this bit as '1' (recessive) and receives it as '0' (dominant), it is interpreted as arbitration loss. If this bit is transmitted as '0' (dominant), then if it is received as '1' (recessive), the FlexCAN2 module treats it as bit error. If the value received matches the value transmitted, it is considered as a successful bit transmission. 0 Indicates the current MB has a data frame to be transmitted 1 Indicates the current MB has a remote frame to be transmitted
LENGTH	Length of data in bytes. This 4-bit field is the length (in bytes) of the RX or TX data, which is located in offset 0x8 through 0xF of the MB space (see Figure 22-2). In reception, this field is written by the FlexCAN2 module, copied from the DLC (data length code) field of the received frame. In transmission, this field is written by the CPU and corresponds to the DLC field value of the frame to be transmitted. When RTR = 1, the Frame to be transmitted is a remote frame and does not include the data field, regardless of the length field.
TIME STAMP	Free-running counter time stamp. This 16-bit field is a copy of the free-running timer, captured for Tx and Rx frames at the time when the beginning of the Identifier field appears on the CAN bus.
ID	Frame identifier. • Standard frame format: the 11 (3:13) most significant bits (MSB) are the frame ID in receive and transmit frames. The 18 (14:31) least significant bits (LSB) are ignored. • Extended frame format: all bits are the frame ID in receive and transmit frames.
DATA	Data field. Up to eight bytes can be used for a data frame. For RX frames, the data is stored as it is received from the CAN bus. For TX frames, the CPU prepares the data field to be transmitted within the frame.

Table 22-5. Message Buffer Codes for RX Buffers

RX Code before RX Frame	Description	RX Code after RX Frame	Comment
0000	NOT ACTIVE: MB is not active.	—	MB does not participate in the matching process.
0100	EMPTY: MB is active and empty.	0010	MB participates in the matching process. When a frame is received successfully, the code is automatically updated to FULL.
0010	FULL: MB is full.	0010	The act of reading the C/S word followed by unlocking the MB does not make the code return to EMPTY. It remains FULL. If a new frame is written to the MB after the C/S word was read and the MB was unlocked, the code still remains FULL.
		0110	If the MB is FULL and a new frame is overwritten to this MB before the CPU had time to read it, the code is automatically updated to OVERRUN. See Section 22.4.3.1, "Matching Process for details about overrun behavior.

Table 22-5. Message Buffer Codes for RX Buffers (continued)

RX Code before RX Frame	Description	RX Code after RX Frame	Comment
0110	OVERRUN: A frame was overwritten into a full buffer.	0010	If the code indicates OVERRUN but the CPU reads the C/S word and then unlocks the MB, when a new frame is written to the MB the code returns to FULL.
		0110	If the code already indicates OVERRUN, and yet another new frame must be written, the MB is overwritten again, and the code remains OVERRUN. See Section 22.4.3.1, "Matching Process for details about overrun behavior.
0XY1[1]	BUSY: FlexCAN is updating the contents of the MB. The CPU must not access the MB.	0010	EMPTY buffer was written with a new frame (XY was 01).
		0110	FULL/OVERRUN buffer was overwritten (XY was 11).

[1] For TX message buffers (see Table 22-6), the BUSY bit must be ignored when read.

Table 22-6. Message Buffer Code for TX Buffers

RTR	Initial TX Code	Code after Successful Transmission	Description
X	1000	—	INACTIVE: MB does not participate in the arbitration process.
0	1100	1000	Transmit data frame unconditionally once. After transmission, the MB automatically returns to the INACTIVE state.
1	1100	0100	Transmit remote frame unconditionally once. After transmission, the MB automatically becomes and RX MB with the same ID.
0	1010	1010	Transmit a data frame whenever a remote request frame with the same ID is received. This MB participates simultaneously in both the matching and arbitration processes. The matching process compares the ID of the incoming remote request frame with the ID of the MB. If a match occurs this MB is allowed to participate in the current arbitration process and the CODE field is automatically updated to '1110' to allow the MB to participate in future arbitration runs. When the frame is eventually transmitted successfully, the Code automatically returns to '1010' to restart the process again.
0	1110	1010	The MBM generates this code as a result of match to a remote request frame. The data frame is transmitted unconditionally once, and then the code automatically returns to '1010'. The CPU can write the code with the same effect.

22.3.3 Register Descriptions

The FlexCAN2 registers are described in this section. There are four separate, identical FlexCAN2 modules: A, B, C, and D. In the following sections, the '*x*' in the registers' names represents the individual module.

22.3.3.1 Module Configuration Register (CAN*x*_MCR)

CAN*x*_MCR defines global system configurations, such as the module operation mode and maximum message buffer configuration. Most of the fields in this register can be accessed at any time, except the MAXMB field, which can be changed only while the module is in freeze mode.

Address: Base + 0x0000 Access: User read/write

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	MDIS	FRZ	0	HALT	NOTRDY	0	SOFTRST	FRZACK	1	0	WRN EN	MDISACK	0	0	SRX DIS	MBFEN
W																
Reset	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	MAXMB					
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Figure 22-3. Module Configuration Register (CAN*x*_MCR)

Table 22-7. CAN*x*_MCR Field Descriptions

Field	Description
0 MDIS	Module disable. Controls whether FlexCAN2 is enabled or not. When disabled, FlexCAN2 shuts down the clock to the CAN protocol interface and message buffer management submodules. This is the only bit in CAN*x*_MCR not affected by soft reset. See Section 22.4.6.2, "Module Disabled Mode," for more information. 0 Enable the FlexCAN2 module 1 Disable the FlexCAN2 module
1 FRZ	Freeze enable. Specifies the FlexCAN2 behavior when the HALT bit in the CAN*x*_MCR is set or when debug mode is requested at MCU level. When FRZ is asserted, FlexCAN2 is enabled to enter freeze mode. Negation of this bit field causes FlexCAN2 to exit from freeze mode. 0 Not enabled to enter freeze mode 1 Enabled to enter freeze mode
2	Reserved.
3 HALT	Halt FlexCAN. Assertion of this bit puts the FlexCAN2 module into freeze mode if FRZ is asserted. The CPU must clear it after initializing the message buffers and CAN*x*_CR. If FRZ is set, no reception or transmission is performed by FlexCAN2 before this bit is cleared. While in freeze mode, the CPU has write access to the CAN*x*_ECR, that is otherwise read-only. Freeze mode cannot be entered while FlexCAN2 is disabled. See Section 22.4.6.1, "Freeze Mode," for more information. 0 No freeze mode request. 1 Enters freeze mode if the FRZ bit is asserted.
4 NOTRDY	FlexCAN2 not ready. Indicates that FlexCAN2 is either disabled or in freeze mode. It is negated after FlexCAN2 has exited these modes. 0 FlexCAN2 module is either in normal mode, listen-only mode or loop-back mode 1 FlexCAN2 module is either disabled or freeze mode
5	Reserved.

Table 22-7. CAN*x*_MCR Field Descriptions (continued)

Field	Description
6 SOFTRST	Soft reset. When asserted, FlexCAN2 resets its internal state machines and some of the memory-mapped registers. The following registers are affected by soft reset: • CAN*x*_MCR (except the MDIS bit) • CAN*x*_TIMER • CAN*x*_ECR • CAN*x*_ESR • CAN*x*_IMRL • CAN*x*_IMRH • CAN*x*_IFRL • CAN*x*_IFRH Configuration registers that control the interface to the CAN bus are not affected by soft reset. The following registers are unaffected: • CANx_CR • CAN*x*_RXGMASK • CAN*x*_RX14MASK • CAN*x*_RX15MASK • all Message buffers The SOFTRST bit can be asserted directly by the CPU when it writes to the CAN*x*_MCR, but it is also asserted when global soft reset is requested at MCU level. Because soft reset is synchronous and has to follow a request/acknowledge procedure across clock domains, it can take time to fully propagate its effect. The SOFTRST bit remains asserted while reset is pending, and is automatically negated when reset completes. Therefore, software can poll this bit to know when the soft reset has completed. 0 No reset request 1 Resets values in registers indicated above.
7 FRZACK	Freeze mode acknowledge. Indicates that FlexCAN2 is in freeze mode and its prescaler is stopped. The freeze mode request cannot be granted until current transmission and reception processes have finished. Therefore the software can poll the FRZACK bit to know when FlexCAN2 has actually entered freeze mode. If freeze mode request is negated, then this bit is negated after the FlexCAN2 prescaler is running again. If freeze mode is requested while FlexCAN2 is disabled, then the FRZACK bit is set only after exiting the low power mode. See Section 22.4.6.1, “Freeze Mode,” for more information. 0 FlexCAN2 not in freeze mode, prescaler running 1 FlexCAN2 in freeze mode, prescaler stopped
8–9	Reserved.
10 WRNEN	Warning interrupt enable. When asserted, this bit enables the generation of the TWRNINT and RWRNINT flags in the Error and Status Register. If WRNEN is negated, the TWRNINT and RWRNINT flags are always 0, independent of the values of the error counters, and no warning interrupt is generated. 1 = TWRNINT and RWRNINT bits are set when the respective error counter transition from less than 96 to greater than or equal to 96. 0 = TWRNINT and RWRNINT bits are zero, independent of the values in the error counters.
11 MDISACK	Low power mode acknowledge. Indicates whether FlexCAN2 is disabled. This cannot be performed until all current transmission and reception processes have finished, so the CPU can poll the MDISACK bit to know when FlexCAN2 has actually been disabled. See Section 22.4.6.2, “Module Disabled Mode,” for more information. 0 FlexCAN2 not disabled 1 FlexCAN2 is disabled
12–13	Reserved.

Table 22-7. CAN*x*_MCR Field Descriptions (continued)

Field	Description
14 SRXDIS	This bit defines whether FlexCAN is allowed to receive frames transmitted by itself. If this bit is asserted, frames transmitted by the module is not stored in any MB, regardless if the MB is programmed with an ID that matches the transmitted frame, and no interrupt flag or interrupt signal is generated due to the frame reception. 1 = Self reception disabled 0 = Self reception enabled
15 MBFEN	Message buffer filter enable. This bit provides the capability of enabling either individual masking of every message buffer, or global masking of message buffers. By negating MBFEN, global masking is enabled and FlexCAN uses the Rx ID masking scheme of RXGMASK, RX14MASK and RX15MASK. MB14 and MB15 have individual masks and the others share the global mask. The scheme does not provide a reception queue; i.e. a received message always fills the first matching buffer, setting the CODE field to overrun if the buffer contained an unread message. See Section 22.3.3.4, “RX Mask Registers” for more information. Use global masking for compatibility with previous FlexCAN versions, which negates MBFEN at reset to retain compatibility with existing software. By asserting MBFEN, individual Rx ID masking and the reception queue features are enabled. In this scheme, individual receive mask registers (RXIM[0-63]) are provided for each MB. Upon receiving a message, FlexCAN searches the reception queue for the first empty matching MB. See Section 22.3.3.5, “RX Individual Mask Registers (CANx_RXIMR0 through CANx_RXIMR63)” and Section 22.4.3.2, “Reception Queue” for more information. 0 = Individual RX masking and reception queue features are disabled (thus the device is compatible with previous FlexCAN versions, i.e. one global mask register is used). 1 = Individual RX masking and reception queue features are enabled.
16–25	Reserved.
26–31 MAXMB[0:5]	Maximum number of message buffers. This 6-bit field defines the maximum number of message buffers of the FlexCAN2 module. The reset value (0x0F) is equivalent to 16 MB configuration. FlexCAN must be in freeze mode before changing this value. Maximum MBs in use = MAXMB + 1 **Note:** MAXMB must be less than or equal to the number of available message buffers. FlexCAN2 cannot transmit or receive frames if this value is greater than the number of available message buffers.

22.3.3.2 Control Register (CAN*x*_CR)

CAN*x*_CR is defined for specific FlexCAN2 control features related to the CAN bus, such as bit-rate, programmable sampling point within an RX bit, loop-back mode, listen-only mode, bus off recovery behavior, and interrupt enabling (for example, bus-off, error). It also determines the division factor for the clock prescaler. BOFFMSK, ERRMSK, and BOFFREC bits can be accessed at any time. CANx_CR is unaffected by soft reset, which occurs when CAN_MCR[SOFTRST] is asserted.

Address: Base + 0x0004 Access: User read/write

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	PRESDIV								RJW		PSEG1			PSEG2		
Reset[1]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	BOFF MSK	ERR MSK	CLK_ SRC	LPB	TWRN MSK	RWRN MSK	0	0	SMP	BOFF REC	TSYN	LBUF	LOM	PROPSEG		
Reset[1]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[1] CAN*x*_CR is unaffected by soft reset (which occurs when CAN_MCR[SOFTRST] is asserted).

Figure 22-4. Control Register (CAN*x*_CR)

Table 22-8. CAN*x*_CR Field Descriptions

Bits	Description
0–7 PRESDIV[0:7]	Prescaler division factor. Defines the ratio between the CPI clock frequency and the serial clock (SCK) frequency. The SCK period defines the time quantum of the CAN protocol. For the reset value, the SCK frequency is equal to the CPI clock frequency. The maximum value of this register is 0xFF, that gives a minimum SCK frequency equal to the CPI clock frequency divided by 256. For more information, see Section 22.4.5.4, "Protocol Timing." $\text{S-clock frequency} = \frac{\text{CPI clock frequency}}{\text{PRESDIV} + 1}$
8–9 RJW[0:1]	Resync jump width. Defines the maximum number of time quanta[1] that a bit time can be changed by one re-synchronization. The valid programmable values are 0–3. $\text{Resync Jump Width} = \text{RJW} + 1$
10–12 PSEG1[0:2]	Phase segment 1. Defines the length of phase buffer segment 1 in the bit time. The valid programmable values are 0–7. $\text{Phase Buffer Segment 1} = (\text{PSEG1} + 1) \times \text{Time Quanta}$
13–15 PSEG2[0:2]	Phase segment 2. Defines the length of phase buffer segment 2 in the bit time. The valid programmable values are 1–7. $\text{Phase Buffer Segment 2} = (\text{PSEG2} + 1) \times \text{Time Quanta}$
16 BOFFMSK	Bus off mask. Provides a mask for the bus off interrupt. 0 Bus off interrupt disabled 1 Bus off interrupt enabled
17 ERRMSK	Error mask. Provides a mask for the error interrupt. 0 Error interrupt disabled 1 Error interrupt enabled
18 CLK_SRC	CAN engine clock source. Selects the clock source to the CAN Protocol Interface (CPI) to be either the system clock (driven by the PLL) or the crystal oscillator clock. The selected clock is fed into the prescaler to generate the serial clock (SCK). 0 = The CAN engine clock source is the oscillator clock 1 = The CAN engine clock source is the system clock

Table 22-8. CAN*x*_CR Field Descriptions

Bits	Description
19 LPB	Loop back. Configures FlexCAN2 to operate in loop-back mode. See Section 22.1.4, "Modes of Operation" for information about this operating mode. 0 Loop back disabled 1 Loop back enabled
20 TWRNMSK	This bit provides a mask for the TX Warning Interrupt associated with the TWRNINT flag in the Error and Status Register. This bit has no effect if the WRNEN bit in CAN*x*_MCR is negated and it is read as zero when WRNEN is negated. 1 = Tx Warning Interrupt enabled 0 = Tx Warning Interrupt disabled
21 RWRNMSK	This bit provides a mask for the RX Warning Interrupt associated with the RWRNINT flag in the Error and Status Register. This bit has no effect if the WRNEN bit in CAN*x*_MCR is negated and it is read as zero when WRNEN is negated. 1 = Rx Warning Interrupt enabled 0 = Rx Warning Interrupt disabled
22–23	Reserved.
24 SMP	Sampling mode. Defines the sampling mode of each bit in the receiving messages (RX). 0 Just one sample is used to determine the RX bit value 1 Three samples are used to determine the value of the received bit: the regular one (sample point) and two preceding samples, a majority rule is used
25 BOFFREC	Bus off recovery mode. Defines how FlexCAN2 recovers from bus off state. If this bit is negated, automatic recovering from bus off state occurs according to the CAN Specification 2.0B. If the bit is asserted, automatic recovering from bus off is disabled and the module remains in bus off state until the bit is negated by the user. If the negation occurs before 128 sequences of 11 recessive bits are detected on the CAN bus, then bus off recovery happens as if the BOFFREC bit had never been asserted. If the negation occurs after 128 sequences of 11 recessive bits are detected, then FlexCAN2 re-synchronizes to the bus by waiting for 11 recessive bits before joining the bus. After negation, the BOFFREC bit can be re-asserted again during bus off, but it is only effective the next time the module enters bus off. If BOFFREC was negated when the module entered bus off, asserting it during bus off is not effective for the current bus off recovery. 0 Automatic recovering from bus off state enabled, according to CAN Spec 2.0 part B 1 Automatic recovering from bus off state disabled
26 TSYN	Timer sync mode. Enables a mechanism that resets the free-running timer each time a message is received in message buffer 0. This feature provides means to synchronize multiple FlexCAN2 stations with a special SYNC message (that is, global network time). 0 Timer sync feature disabled 1 Timer sync feature enabled **Note:** There is a possibility of 4–5 ticks count skew between the different FlexCAN2 stations that would operate in this mode.
27 LBUF	Lowest buffer transmitted first. This bit defines the ordering mechanism for message buffer transmission. 0 Buffer with lowest ID is transmitted first 1 Lowest number buffer is transmitted first

Table 22-8. CAN*x*_CR Field Descriptions

Bits	Description
28 LOM	Listen-only mode. Configures FlexCAN2 to operate in listen-only mode. In this mode, the FlexCAN2 module receives messages without giving any acknowledge. It is not possible to transmit any message in this mode. 0 FlexCAN2 module is in normal active operation, listen only mode is deactivated 1 FlexCAN2 module is in listen only mode operation
29–31 PROPSEG [0:2]	Propagation segment. Defines the length of the propagation segment in the bit time. The valid programmable values are 0–7. Propagation Segment Time = (PROPSEG + 1) × Time Quanta Time Quantum = one S clock period

1 One time quantum is equal to the S clock period.

22.3.3.3 Free Running Timer (CAN*x*_TIMER)

CAN*x*_TIMER represents a 16-bit free running counter that can be read and written by the CPU. The timer starts from 0x0000 after Reset, counts linearly to 0xFFFF, and wraps around.

The timer is clocked by the FlexCAN2 bit-clock (which defines the baud rate on the CAN bus). During a message transmission/reception, it increments by one for each bit that is received or transmitted. When there is no message on the bus, it counts using the previously programmed baud rate. During freeze mode, the timer is not incremented.

The timer value is captured at the beginning of the identifier field of any frame on the CAN bus. This captured value is written into the TIME STAMP entry in a message buffer after a successful reception or transmission of a message.

Writing to the timer is an indirect operation. The data is first written to an auxiliary register and then an internal request/acknowledge procedure across clock domains is executed. All this is transparent to the user, except for the time delay required for the data write to the register. Software can poll the register to verify the data is written.

Address: Base + 0x0008 Access: User read/write

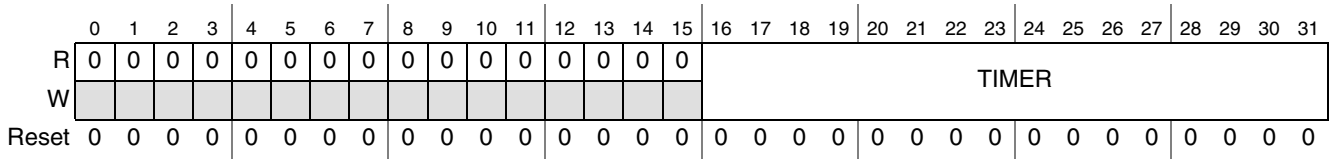


Figure 22-5. Free Running Timer (CAN*x*_TIMER)

22.3.3.4 RX Mask Registers

By negating the CAN*x*_MCR[MBFEN] bit, the CANx_RXGMASK, CANx_RX14MASK, and CANx_RX15MASK registers are used as acceptance masks for received frame IDs. Three masks are defined: a global mask, used for RX buffers 0–13 and 16–63, and two extra masks dedicated for buffers 14 and 15.

The meaning of each mask bit is the following:

- Mask bit = 0: the corresponding incoming ID bit is “don’t care.”
- Mask bit = 1: the corresponding ID bit is checked against the incoming ID bit, to see if a match exists.

Note that these masks are used both for standard and extended ID formats. Do not change the value of mask registers while in normal operation. Locked frames which match a message buffer through a mask can be transferred into the message buffer (upon release) even if they no longer match. Table 22-9 shows some examples of ID masking for standard and extended message buffers.

Table 22-9. Mask Examples for Standard/Extended Message Buffers

Mask ID	Base ID ID28.....ID18	IDE	Extended ID ID17.....ID0	Match
MB2 ID	1 1 1 1 1 1 1 1 0 0 0	0		
MB3 ID	1 1 1 1 1 1 1 1 0 0 0	1	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	
MB4 ID	0 0 0 0 0 0 0 1 1 1 1	0		
MB5 ID	0 0 0 0 0 0 0 1 1 1 0 1	1	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	
MB14 ID	1 1 1 1 1 1 1 1 0 0 0	1	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	
RX Global Mask	1 1 1 1 1 1 1 1 1 1 0		1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 1	
RX Msg in [1]	1 1 1 1 1 1 1 1 0 0 1	1	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	3
RX Msg in [2]	1 1 1 1 1 1 1 1 0 0 1	0		2
RX Msg in [3]	1 1 1 1 1 1 1 1 0 0 1	1	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0	
RX Msg in [4]	0 1 1 1 1 1 1 1 0 0 0	0		
RX Msg in [5]	0 1 1 1 1 1 1 1 0 0 0	1	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	14
RX 14 Mask	0 1 1 1 1 1 1 1 1 1 1		1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	
RX Msg in [6]	1 0 1 1 1 1 1 1 0 0 0	1	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	
RX Msg in [7]	0 1 1 1 1 1 1 1 0 0 0	1	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	14

[1] Match for Extended Format (message buffer 3).

[2] Match for Standard Format. (message buffer 2).

[3] Mismatch for message buffer 3 because of ID0.

[4] Mismatch for message buffer 2 because of ID28.

[5] Mismatch for message buffer 3 because of ID28, match for message buffer 14 (uses RX14MASK).

[6] Mismatch for message buffer 14 because of ID27 (uses RX14MASK).

[7] Match for message buffer 14 (uses RX14MASK).

22.3.3.4.1 RX Global Mask (CAN*x*_RXGMASK)

The RX global mask bits are applied to all RX identifiers excluding RX buffers 14 and 15, that have their specific RX mask registers. Access to this register is unrestricted. Note that CANx_RXGMASK is unaffected by soft reset (which occurs when CAN_MCR[SOFTRST] asserts).

Address: Base + 0x0010 (CANx_RXGMASK)
Base + 0x0014 (CANx_RX14MASK)
Base + 0x0018 (CANx_RX15MASK)

Access: User read/write

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	MI28	MI27	MI26	MI25	MI24	MI23	MI22	MI21	MI20	MI19	MI18	MI17	MI16
W																
Reset [1]	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	MI15	MI14	MI13	MI12	MI11	MI10	MI9	MI8	MI7	MI6	MI5	MI4	MI3	MI2	MI1	MI0
W																
Reset [1]	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[1] CAN*x*_RXGMASK is unaffected by soft reset (which occurs when CAN_MCR[SOFTRST] is asserted).

Figure 22-6. RX Global Mask Register (CAN*x*_RXGMASK)

Table 22-10. CAN*x*_RXGMASK Field Descriptions

Field	Description
0–2	Reserved, must be cleared.
3–13 MI*n*	Standard ID mask bits. These bits are the same mask bits for the standard and extended formats.
14–31 MI*n*	Extended ID mask bits. These bits are used to mask comparison only in extended format.

22.3.3.4.2 RX 14 Mask (CAN*x*_RX14MASK)

The CAN*x*_RX14MASK register has the same structure as the RX global mask register and is used to mask message buffer 14. Access to this register is unrestricted. Note that CANx_RX14MASK is unaffected by soft reset (which occurs when CAN_MCR[SOFTRST] is asserted).

- Address offset: 0x0014
- Reset value: 0x1FFF_FFFF

22.3.3.4.3 RX 15 Mask (CAN*x*_RX15MASK)

The CAN*x*_RX15MASK register has the same structure as the RX global mask register and is used to mask message buffer 15. Access to this register is unrestricted. Note that CANx_RX15MASK is unaffected by soft reset (which occurs when CAN_MCR[SOFTRST] is asserted).

- Address offset: 0x0018
- Reset value: 0x1FFF_FFFF

22.3.3.5 RX Individual Mask Registers (CAN*x*_RXIMR0 through CAN*x*_RXIMR63)

By asserting the CAN*x*_MCR[MBFEN] bit, the CAN*x*_RXIMR[0–63] registers are used as acceptance masks for received frame IDs, in both standard and extended ID formats. One mask register is provided for each message buffer for individual ID masking per message buffer.

The meaning of each mask bit is the following:

- Mask bit = 0: The corresponding incoming ID bit is a “don’t care.”
- Mask bit = 1: The corresponding ID bit is checked against the incoming ID bit, to see if a match exists.

The Individual Rx Mask Registers are implemented in RAM, so they are not affected by reset and must be explicitly initialized prior to any reception. Furthermore, they can only be accessed by the CPU while the module is in freeze mode. Out of freeze mode, write accesses are blocked and read accesses return all 0s. Furthermore, if the MBFEN bit in the MCR register is negated, any read or write operation to these RXIMR*n* registers results in access error.

Address: Base + 0x0880–0x097F Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	MI28	MI27	MI26	MI25	MI24	MI23	MI22	MI21	MI20	MI19	MI18	MI17	MI16
W																
Reset [1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	MI15	MI14	MI13	MI12	MI11	MI10	MI9	MI8	MI7	MI6	MI5	MI4	MI3	MI2	MI1	MI0
W																
Reset [1]	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

[1] The ‘U’ indicates the value is undefined after reset.

Figure 22-7. RX Individual Mask Registers (CANx_RXIMR0 through CANx_RXIMR63)

Table 22-11. CANx_RXIMR0–CANx_RXIMR63 Field Descriptions

Field	Description
0–2	Reserved.
3–13 MI28–MI18	Standard ID mask bits. These bits are the same mask bits for the standard and extended formats.
14–31 MI17–MI0	Extended ID mask bits. These bits are used to mask comparison only in extended format.

22.3.3.6 Error Counter Register (CAN*x*_ECR)

CAN*x*_ECR has two 8-bit fields reflecting the value of two FlexCAN2 error counters: the transmit error counter (TXECTR field) and receive error counter (RXECTR field). The rules for increasing and decreasing these counters are described in the CAN protocol and are completely implemented in the FlexCAN2 module. Both counters are read only except in freeze mode, where they can be written by the CPU.

Writing to the CAN*x*_ECR while in freeze mode is an indirect operation. The data is first written to an auxiliary register, and then an internal request/acknowledge procedure across clock domains is executed. This occurs internally without indication, except for the time delay required for the data write to the register. Software can poll the register to verify that the data is written.

FlexCAN2 responds to any bus state as described in the protocol: transmitting, for example, an ‘error active’ or ‘error passive’ flag, delaying its transmission start time (‘error passive’), and avoiding any influence on the bus when in the bus off state. The following are the basic rules for FlexCAN2 bus state transitions:

- If the value of TXECTR or RXECTR increases to be greater than or equal to 128, the FLTCONF field in the CAN*x*_ESR is updated to reflect the ‘error passive’ state.
- If the FlexCAN2 state is ‘error passive,’ and either TXECTR or RXECTR decrements to a value less than or equal to 127 while the other already satisfies this condition, the FLTCONF field in the CAN*x*_ESR is updated to reflect the ‘error active’ state.
- If the value of TXECTR increases to greater than 255, the FLTCONF field in the CAN*x*_ESR is updated to reflect the bus off state, and can issue an interrupt. The value of TXECTR is then reset to zero.
- If FlexCAN2 is in the bus off state, then TXECTR is cascaded together with another internal counter to count the 128th occurrences of 11 consecutive recessive bits on the bus. Hence, TXECTR is reset to zero and counts in a manner where the internal counter counts 11 such bits and then wraps around while incrementing the TXECTR. When TXECTR reaches the value of 128, the FLTCONF field in CAN*x*_ESR is updated to be ‘error active’ and both error counters are reset to zero. At any instance of dominant bit following a stream of less than 11 consecutive recessive bits, the internal counter resets itself to zero without affecting the TXECTR value.
- If during system start-up, only one node is operating, then its TXECTR increases in each message it is trying to transmit, as a result of acknowledge errors (indicated by the ACKERR bit in CAN*x*_ESR). After the transition to the ‘error passive’ state, the TXECTR does not increment anymore by acknowledge errors. Therefore the device never goes to the bus off state.
- If the RXECTR increases to a value greater than 127, it is not incremented further, even if more errors are detected while being a receiver. At the next successful message reception, the counter is set to a value between 119 and 127 to resume to ‘error active’ state.

Address: Base + 0x001C Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RXECTR								TXECTR							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 22-8. Error Counter Register (CAN*x*_ECR)

22.3.3.7 Error and Status Register (CAN*x*_ESR)

CAN*x*_ESR reflects various error conditions, some general status of the device, and it is the source of two interrupts to the CPU. The reported error conditions (bits 16–21) are those that occurred since the last time the CPU read this register. The CPU read action clears BIT1ERR, BIT0ERR, ACKERR, CRCERR, FRMERR, and STFERR. TXWRN, RXWRN, IDLE, TXRX, FLTCONF, BOFFINT, and ERRINT are status bits.

Most bits in this register are read-only, except BOFFINT, ERRINT, TWRNINT, and RWRNINT which are interrupt flags that can be cleared by writing 1 to them (writing 0 has no effect).

See Section 22.4.7, “Interrupts,” for more details.

NOTE

A read clears BIT1ERR, BIT0ERR, ACKERR, CRCERR, FRMERR, and STFERR, therefore these bits must not be read speculatively. For future compatibility, the TLB entry covering the CAN*x*_ESR must be configured to be guarded.

Address: Base + 0x0020 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TWRN INT	RWRN INT
W															w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	BIT1 ERR	BIT0 ERR	ACK ERR	CRC ERR	FRM ERR	STF ERR	TX WRN	RX WRN	IDLE	TXRX	FLTCONF		0	BOFF INT	ERR INT	0
W														w1c	w1c	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 22-9. Error and Status Register (CAN*x*_ESR)

Table 22-12. CAN*x*_ESR Field Descriptions

Field	Description
0–13	Reserved.
14 TWRNINT	If the WRNEN bit in CAN*x*_MCR is asserted, the TWRNINT bit is set when the TXWRN flag transitions from 0 to 1, meaning that the TX error counter reached 96. If the corresponding mask bit in the Control Register (TWRNMSK) is set, an interrupt is generated to the CPU. This bit is cleared by writing to 1. Writing 0 has no effect. 0 No such occurrence 1 TXECTR ≥ 96
15 RWRNINT	If the WRNEN bit in CAN*x*_MCR is asserted, the RWRNINT bit is set when the RXWRN flag transitions from 0 to 1, meaning that the RX error counter reached 96. If the corresponding mask bit in the Control Register (RWRNMSK) is set, an interrupt is generated to the CPU. This bit is cleared by writing to 1. Writing 0 has no effect. 0 No such occurrence 1 RXECTR ≥ 96
16 BIT1ERR	Bit 1 error. Indicates when an inconsistency occurs between the transmitted and the received message in a bit. A read clears BIT1ERR. 0 No such occurrence 1 At least one bit sent as recessive is received as dominant **Note:** This bit is not set by a transmitter in case of arbitration field or ACK slot, or in case of a node sending a passive error flag that detects dominant bits.
17 BIT0ERR	Bit 0 error. Indicates when an inconsistency occurs between the transmitted and the received message in a bit. A read clears BIT0ERR. 0 No such occurrence 1 At least one bit sent as dominant is received as recessive

Table 22-12. CAN*x*_ESR Field Descriptions (continued)

Field	Description
18 ACKERR	Acknowledge error. Indicates that an acknowledge error has been detected by the transmitter node; that is, a dominant bit has not been detected during the ACK SLOT. A read clears ACKERR. 0 No such occurrence 1 An ACK error occurred since last read of this register
19 CRCERR	Cyclic redundancy code error. Indicates that a CRC error has been detected by the receiver node; that is, the calculated CRC is different from the received. A read clears CRCERR. 0 No such occurrence 1 A CRC error occurred since last read of this register.
20 FRMERR	Form error. Indicates that a form error has been detected by the receiver node; that is, a fixed-form bit field contains at least one illegal bit. A read clears FRMERR. 0 No such occurrence 1 A form error occurred since last read of this register
21 STFERR	Stuffing error. Indicates that a stuffing error has been detected. A read clears STFERR. 0 No such occurrence. 1 A stuffing error occurred since last read of this register.
22 TXWRN	TX error counter. This status bit indicates that repetitive errors are occurring during message transmission. 0 No such occurrence 1 TXECTR ≥ 96
23 RXWRN	RX error counter. This status bit indicates when repetitive errors are occurring during messages reception. 0 No such occurrence 1 RXECTR ≥ 96
24 IDLE	CAN bus IDLE state. This status bit indicates when CAN bus is in IDLE state. 0 No such occurrence 1 CAN bus is now IDLE
25 TXRX	Current FlexCAN2 status (transmitting/receiving). This status bit indicates if FlexCAN2 is transmitting or receiving a message when the CAN bus is not in IDLE state. This bit has no meaning when IDLE is asserted. 0 FlexCAN2 is receiving a message (IDLE = 0) 1 FlexCAN2 is transmitting a message (IDLE = 0)
26–27 FLTCONF[0:1]	Fault confinement state. This status bit indicates the confinement state of the FlexCAN2 module. If the LOM bit in the CAN*x*_CR asserts, the FLTCONF field indicates “Error Passive”. Since the CAN*x*_CR is not affected by a soft reset, the FLTCONF field is not affected by a soft reset if the LOM bit asserts. 00 Error active 01 Error passive 1X Bus off
28	Reserved.
29 BOFFINT	Bus off interrupt. This status bit is set when FlexCAN2 is in the bus off state. If CAN*x*_CR[BOFFMSK] is set, an interrupt is generated to the CPU. This bit is cleared by writing it to 1. Writing 0 has no effect. 0 No such occurrence 1 FlexCAN2 module is in ‘Bus Off’ state

Table 22-12. CAN*x*_ESR Field Descriptions (continued)

Field	Description
30 ERRINT	Error interrupt. This status bit indicates that at least one of the error bits (bits 16-21) is set. If CAN*x*_CR[ERRMSK] is set, an interrupt is generated to the CPU. This bit is cleared by writing it to 1. Writing 0 has no effect. 0 No such occurrence 1 Indicates setting of any error bit in the CAN*x*_ESR
31	Reserved.

22.3.3.8 Interrupt Masks High Register (ICAN*x*_IMRH)

CAN*x*_IMRH allows any number of a range of 32 message buffer interrupts to be enabled or disabled. It contains one interrupt mask bit per buffer, enabling the CPU to determine which buffer generates an interrupt after a successful transmission or reception (that is, when the corresponding IFRH bit is set).

Address: Base + 0x0024 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R W	BUF 63M	BUF 62M	BUF 61M	BUF 60M	BUF 59M	BUF 58M	BUF 57M	BUF 56M	BUF 55M	BUF 54M	BUF 53M	BUF 52M	BUF 51M	BUF 50M	BUF 49M	BUF 48M
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R W	BUF 47M	BUF 46M	BUF 45M	BUF 44M	BUF 43M	BUF 42M	BUF 41M	BUF 40M	BUF 39M	BUF 38M	BUF 37M	BUF 36M	BUF 35M	BUF 34M	BUF 33M	BUF 32M
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 22-10. Interrupt Masks High Register (CAN*x*_IMRH)

Table 22-13. CAN*x*_IMRH Field Descriptions

Field	Description
0–31 BUF*n*M	Message buffer *n* mask. Enables or disables the respective FlexCAN2 message buffer (MB63 to MB32) Interrupt. 0 The corresponding buffer Interrupt is disabled 1 The corresponding buffer Interrupt is enabled **Note:** Setting or clearing a bit in the IMRH register can assert or negate an interrupt request, respectively.

22.3.3.9 Interrupt Masks Low Register (CAN*x*_IMRL)

CAN*x*_IMRL allows enabling or disabling any number of a range of 32 message buffer interrupts. It contains one interrupt mask bit per buffer, enabling the CPU to determine which buffer generates an interrupt after a successful transmission or reception (that is, when the corresponding IFRL bit is set).

Address: Base + 0x0028 Access: User R/W

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	BUF 31M	BUF 30M	BUF 29M	BUF 28M	BUF 27M	BUF 26M	BUF 25M	BUF 24M	BUF 23M	BUF 22M	BUF 21M	BUF 20M	BUF 19M	BUF 18M	BUF 17M	BUF 16M
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	BUF 15M	BUF 14M	BUF 13M	BUF 12M	BUF 11M	BUF 10M	BUF 09M	BUF 08M	BUF 07M	BUF 06M	BUF 05M	BUF 04M	BUF 03M	BUF 02M	BUF 01M	BUF 00M
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 22-11. Interrupt Masks Low Register (CAN*x*_IMRL)

Table 22-14. CAN*x*_IMRL Field Descriptions

Field	Description
0–31 BUF*n*M	Message buffer *n* mask. Enables or disables the respective FlexCAN2 message buffer (MB31 to MB0) Interrupt. 0 The corresponding buffer Interrupt is disabled 1 The corresponding buffer Interrupt is enabled **Note:** Setting or clearing a bit in the IMRL register can assert or negate an interrupt request, respectively.

22.3.3.10 Interrupt Flags High Register (CAN*x*_IFRH)

CAN*x*_IFRH defines the flags for 32 message buffer interrupts. It contains one interrupt flag bit per buffer. Each successful transmission or reception sets the corresponding IFRH bit. If the corresponding IMRH bit is set, an interrupt is generated. Write a 1 to the interrupt flag to clear its value to zero. Writing a 0 has no effect.

Address: Base + 0x002C Access: User R/W1c

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	BUF 63I	BUF 62I	BUF 61I	BUF 60I	BUF 59I	BUF 58I	BUF 57I	BUF 56I	BUF 55I	BUF 54I	BUF 53I	BUF 52I	BUF 51I	BUF 50I	BUF 49I	BUF 48I
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	BUF 47I	BUF 46I	BUF 45I	BUF 44I	BUF 43I	BUF 42I	BUF 41I	BUF 40I	BUF 39I	BUF 38I	BUF 37I	BUF 36I	BUF 35I	BUF 34I	BUF 33I	BUF 32I
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 22-12. Interrupt Flags High Register (CAN*x*_IFRH)

Table 22-15. CAN*x*_IFRH Field Descriptions

Field	Description
0–31 BUF*n*I	Message buffer *n* interrupt. Each bit represents the respective FlexCAN2 message buffer (MB63–MB32) interrupt. Write 1 to clear. 0 No such occurrence 1 The corresponding buffer has successfully completed transmission or reception.

22.3.3.11 Interrupt Flags Low Register (CAN*x*_IFRL)

CAN*x*_IFRL defines the flags for 32 message buffer interrupts. It contains one interrupt flag bit per buffer. Each successful transmission or reception sets the corresponding IFRL bit. If the corresponding IMRL bit is set, an interrupt is generated. Write a 1 to the interrupt flag to clear its value to zero. Writing 0 has no effect.

Address: Base + 0x0030 Access: User R/W1c

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	BUF 31I	BUF 30I	BUF 29I	BUF 28I	BUF 27I	BUF 26I	BUF 25	BUF 24I	BUF 23I	BUF 22I	BUF 21I	BUF 20I	BUF 19I	BUF 18I	BUF 17I	BUF 16I
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	BUF 15I	BUF 14I	BUF 13I	BUF 12I	BUF 11I	BUF 10I	BUF 09I	BUF 08I	BUF 07I	BUF 06I	BUF 05I	BUF 04I	BUF 03I	BUF 02I	BUF 01I	BUF 00I
W	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c	w1c
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 22-13. Interrupt Flags Low Register (CAN*x*_IFRL)

Table 22-16. CAN*x*_IFRL Field Descriptions

Field	Description
0–31 BUF*n*I	Message buffer *n* interrupt. Each bit represents the respective FlexCAN2 message buffer (MB31 to MB0) interrupt. Write 1 to clear. 0 No such occurrence 1 The corresponding buffer has successfully completed transmission or reception.

22.4 Functional Description

22.4.1 Overview

The FlexCAN2 module is a CAN protocol engine with a very flexible message buffer configuration scheme. The module can have up to 64 message buffers, any of which can be assigned as either a TX buffer or an RX buffer. Each message buffer has an assigned interrupt flag to indicate successful completion of transmission or reception.

22.4.2 Transmit Process

The CPU prepares a message buffer for transmission by executing the following steps:

- Write the CODE field of the control and status word to keep the TX MB inactive (code = 1000).
- Write the ID word.
- Write the DATA bytes.
- Write the LENGTH, SRR, IDE, RTR, and CODE fields of the control and status word to activate the TX MB.

The first and last steps are mandatory.

22.4.2.1 Arbitration Process

This process selects the next MB to transmit. All MBs programmed as transmit buffers are scanned to find the lowest ID[1] or the lowest MB number, depending on the LBUF bit in the CAN*x*_CR. The selected MB is transferred to an internal serial message buffer (SMB), which is not software accessible, and then transmitted.

The arbitration process is triggered by the following events:

- During the CRC field of the CAN frame
- During the error delimiter field of the CAN frame
- During Intermission, if the winner MB defined in a previous arbitration was deactivated, or if there was no MB to transmit, but the CPU wrote to the C/S word of any MB after the previous arbitration finished.
- When MBM is in idle or bus off state and the CPU writes to the C/S word of any MB
- Upon leaving freeze mode

When arbitration is complete, and an MB is selected to transmit, the frame is first transferred to the SMB. This is called ‘move out.’ After move out, the CAN transmit machine starts to transmit the frame according to the CAN protocol rules. FlexCAN2 transmits up to eight data bytes, even if the value of the data length code (DLC) is greater.

At the end of a successful transmission, the value of the free running timer at the beginning of the identifier field is written into the TIME STAMP field in the MB, the CODE field in the control and status word of the MB is updated, a status flag is set in CAN*x*_IFRL or CAN*x*_IFRH, and an MB interrupt is generated if allowed by the corresponding interrupt mask register bit.

1. Actually, if LBUF is negated, the arbitration considers not only the ID, but also the RTR and IDE bits placed inside the ID at the same positions they are transmitted in the CAN frame.

22.4.3 Receive Process

The CPU prepares a message buffer for frame reception by executing the following steps:

1. Write the CODE field of the control and status word to keep the RX MB as INACTIVE (CODE = 0000).
2. Write the ID word.
3. Write the CODE field of the control and status word to mark the MB as EMPTY.

The first and last steps are mandatory.

22.4.3.1 Matching Process

The matching process compares the IDs of all active RX message buffers to newly received frames, so that, if a match occurs, a newly received frame is transferred (moved in) to the first (that is, lowest entry) matching MB when the reception queue feature is disabled. Only MBs marked as EMPTY, FULL, or OVERRUN participate in the internal matching process at the CRC frame field. The internal matching process takes place every time the receiver receives an error free frame.

The value of the free running timer is written into the TIME STAMP field in the MB. The ID field, the DATA field (8 bytes at most), and the LENGTH field are stored, the CODE field is updated, and a status flag is set in CAN*x*_IFRL or CAN*x*_IFRH, and an interrupt is generated if the corresponding interrupt mask is enabled in CAN*x*_IMRL/H.

The CPU must read an RX frame from its MB in the following way:

- Control and status word (mandatory, activates internal lock for this buffer)
- ID (optional, needed only if a mask was used)
- DATA field words
- Free running timer (optional, releases internal lock)

Reading the free running timer is not mandatory. If not executed, the MB remains locked, unless the CPU starts reading another MB. Note that only a single MB is locked at a time. The only mandatory CPU read operation is of the control and status word, to assure data coherency. If the BUSY bit is set in the CODE field, then the CPU must defer the access to the MB until this bit is negated.

The CPU must synchronize to frame reception by the status flag bit for the specific MB in one of the CANx_IFRH and CANx_IFRL registers and not by the control and status word code field of that MB. Polling the CODE field does not work because after a frame was received and the CPU services the MB (by reading the C/S word followed by unlocking the MB), the CODE field does not return to EMPTY. It remains FULL, as explained in Table 22-5. If the CPU tries to work around this behavior by writing to the C/S word to force an EMPTY code after reading the MB, the MB is deactivated from any current matching process. As a result, a newly received frame matching the ID of that MB can be lost. Never poll by directly reading the C/S word of the MBs. Instead, read the CANx_IFRH and CANx_IFRL registers.

The received ID field is always stored in the matching MB, thus the contents of the ID field in a MB can change if the match was due to mask.

22.4.3.2 Reception Queue

A queue of received messages can be implemented that allows the CPU more time for servicing MBs. By programming more than one MB with the same ID, received messages are queued into the MBs. Matching to a range of IDs is possible by using ID acceptance masks that mask individual MBs. During the matching algorithm, if a mask bit is asserted, then the corresponding ID bit is compared. If the mask bit is negated, the corresponding ID bit is a don't care.

Suppose, for example, that the second and fifth MBs in an array have the same ID, and FlexCAN starts receiving messages with that ID. When FlexCAN receives the first message, the matching algorithm matches it to MB number 2. The code of this MB is EMPTY, so the message is stored there. When the second message arrives, the matching algorithm finds MB number 2 again, but it is not free to receive[1]. Therefore, the matching process continues, finds MB number 5, and stores the message there. If yet another message with the same ID arrives, the matching algorithm determines that no matching MBs are free to receive the data, and overwrites the last matched MB (number 5). When this occurs, the code field of the MB is set to OVERRUN.

A reception queue is built that orders the messages according to the value in the time stamp field that is read by the CPU. This functionality is set by asserting the CAN*x*_MCR[MBFEN] bit. The RXIMR*n* registers are not initialized out of reset, since they reside in RAM and can only be programmed if the MBFEN bit is asserted while the module is in freeze mode.

FlexCAN also supports an alternate masking scheme with only three mask registers (CAN*x*_RXGMASK, CAN*x*_RX14MASK, and CAN*x*_RX15MASK) for backwards compatibility. This alternate masking scheme is enabled when CAN*x*_MCR[MBFEN] is negated.

See Section 22.3.3.4, "RX Mask Registers."

22.4.3.3 Self Received Frames

FlexCAN2 receives frames transmitted by itself if there exists an RX matching MB, but only if an ACK is generated by an external node or if loop-back mode is enabled. Note also that FlexCAN does receive frames transmitted by itself if there exists an RX matching MB, provided the MCR[SRXDIS] bit is not asserted. If SRXDIS is asserted, FlexCAN does not store frames transmitted by itself in any MB, even if it contains a matching MB, and no interrupt flag or interrupt signal is generated due to the frame reception.

22.4.4 Message Buffer Handling

To maintain data coherency and FlexCAN2 proper operation, the CPU must obey the rules described in Section 22.4.2, "Transmit Process," and Section 22.4.3, "Receive Process." Any form of CPU accessing a MB structure within FlexCAN2 other than those specified can cause FlexCAN2 to behave in an unpredictable way.

Deactivation of a message buffer is a CPU action that causes that MB to be excluded from FlexCAN2 transmit or receive processes during the current match/arbitration round. Any CPU write access to a control and status word of the MB structure deactivates that MB, excluding it from the current RX/TX

1. If, however, the CPU has read the MB2 data and released it before the next matching process at the CRC frame, then, even if the MB2 RX code is FULL, the MB2 is free to receive and the message is stored in MB2 rather than in MB5.

process. However, deactivation is not permanent. The MB that was deactivated during the current match/arbitration pass is available to transmit or receive in the next pass.

The purpose of deactivation is data coherency. The match/arbitration process scans the MBs to decide which MB to transmit or receive. If the CPU updates the MB in the middle of a match or arbitration process, the data coherency in the MB can become corrupt, therefore that MB is deactivated.

Match and arbitration are one-pass processes. After scanning all MBs, a winner is determined. If MBs are changed after they are scanned, no re-evaluation is done to determine a new match/winner; and a frame can be lost if the matched MB has been deactivated. If two RX MBs have a matching ID to a received frame, then it is not guaranteed reception if the matching MB is deactivated after FlexCAN2 has scanned the second.

22.4.4.1 Notes on TX Message Buffer Deactivation

There is a point in time until which the deactivation of a TX MB causes it not to be transmitted (end of move out). After this point, it is transmitted but no interrupt is issued and the CODE field is not updated.

If a TX MB containing the lowest ID (or lowest buffer if LBUF is set) is deactivated after FlexCAN2 has scanned it while in arbitration process, then FlexCAN2 can transmit a MB with an ID that is not the lowest at that time.

22.4.4.2 Notes on RX Message Buffer Deactivation

If the deactivation occurs during move in, the move operation is aborted and no interrupt is issued, but the MB contains mixed data from two different frames.

In case the CPU writes data into RX MB data words while it is being moved in, the move operation is aborted and no interrupt is issued, but the control/status word can change to reflect FULL or OVRN. This action must be avoided.

22.4.4.3 Data Coherency Mechanisms

The FlexCAN2 module has a mechanism to assure data coherency in both receive and transmit processes. The mechanism includes a lock status for MBs and two internal storage areas, called serial message buffers (SMB), to buffer frame transfers within FlexCAN. The details of the mechanism are the following:

- CPU reads the control and status word of an MB, which triggers a lock for that MB; therefore a new RX frame that matches the MB cannot be written to the MB.
- To release a locked MB, the CPU must either lock another MB (by reading its control and status word), or globally release any locked MB (by reading the free-running timer).
- If the CPU reads a RX MB while it is being transferred to (from) SMB, then the BUSY bit is set in the CODE field of the control and status word. To ensure data coherency, the CPU must wait until this BUSY bit is negated before further reading from that MB. In this case, the MB is not locked.
- If the CPU deactivates a locked RX MB, then its lock status is negated, but no data is transferred to the MB.

The following bullets apply only if:

reception queue is disabled,

no other matching buffers in the reception queue or for the last available queue element when all other MBs are not free to receive (the last queue element is overwritten in this manner for a single MB in non-queue mode). If the reception queue is enabled, the state machine searches for the next matching message buffer.

- If while an MB is locked and an RX frame with a matching ID is received, the RX frame cannot be stored in the MB and remains in the SMB. The CAN*x*_ESR does not indicate the RX frame remained in the SMB.
- If while a MB is locked when two or more RX frames with matching ID are received, the last RX frame remains in the SMB, while all preceding RX frames are lost. The CAN*x*_ESR does not indicate that the preceding frames are discarded.
- If a locked MB is released and a matching frame exists in the SMB, the frame is transferred to the matching MB.

22.4.5 CAN Protocol Related Features

22.4.5.1 Remote Frames

A remote frame is a special kind of frame. The user can program a MB to be a request remote frame by writing the MB as transmit with the RTR bit set to 1. After the remote request frame is transmitted successfully, the MB becomes a receive message buffer, with the same ID as before.

When a remote request frame is received by FlexCAN, its ID is compared to the IDs of the transmit message buffers with the CODE field ‘1010’. If there is a matching ID, then the MB frame is transmitted. If the matching MB has the RTR bit set, then FlexCAN2 transmits a remote frame as a response.

A received remote request frame is not stored in a receive buffer. It is only used to trigger a transmission of a frame in response. The mask registers are not used in remote frame matching, and all ID bits (except RTR) of the incoming received frame must match.

In the case that a remote request frame was received and matched a MB, this message buffer immediately enters the internal arbitration process, but is considered as normal TX MB, with no higher priority. The data length of this frame is independent of the DLC field in the remote frame that initiated its transmission.

22.4.5.2 Overload Frames

FlexCAN2 transmits overload frames if the dominant bit satisfies any of the following conditions:

- First or second bit of intermission
- Seventh (last) bit of the end-of-frame field in RX frames
- Eighth bit (last) of error frame delimiter or overload frame delimiter

22.4.5.3 Time Stamp

The value of the free running timer is sampled at the beginning of the identifier field on the CAN bus, and is stored at the end of ‘move in’ in the TIME STAMP field, providing network behavior with respect to time.

The free running timer can be reset upon a specific frame reception, enabling network time synchronization. See TSYN description in Section 22.3.3.2, “Control Register (CANx_CR).”

22.4.5.4 Protocol Timing

The clock source to the CAN protocol interface (CPI) can be either the system clock or a direct feed from the oscillator pin EXTAL. The clock source is selected by the CLK_SRC bit in the CAN_CR. The clock is fed to the prescaler to generate the serial clock (SCK).

The FlexCAN2 module supports a variety of means to setup bit timing parameters that are required by the CAN protocol. The CAN*x*_CR has various fields used to control bit timing parameters: PRESDIV, PROPSEG, PSEG1, PSEG2 and RJW. See Section 22.3.3.2, “Control Register (CANx_CR).”

The PRESDIV field controls a prescaler that generates the serial clock (SCK), whose period defines the ‘time quantum’ used to compose the CAN waveform. A time quantum is the atomic unit of time handled by FlexCAN.

$$f_{Tq} = \frac{f_{CANCLK}}{\text{Prescaler Value}}$$

A bit time is subdivided into three segments[1] (see Figure 22-14 and Table 22-17):

- SYNCSEG: This segment has a fixed length of one time quantum. Signal edges are expected to happen within this section.
- Time segment 1: This segment includes the propagation segment and the phase segment 1 of the CAN standard. It can be programmed by setting the PROPSEG and the PSEG1 fields of the CTRL register so that their sum (plus 2) is in the range of 4 to 16 time quanta.
- Time segment 2: This segment represents the phase segment 2 of the CAN standard. It can be programmed by setting the PSEG2 field of the CTRL register (plus 1) to be 2 to 8 time quanta long.

$$\text{Bit rate} = \frac{f_{Tq}}{(\text{Number of Time Quanta})}$$

1. For further explanation of the underlying concepts see ISO/DIS 11519–1, Section 10.3. See also the Bosch CAN 2.0A/B protocol specification dated September 1991 for bit timing.

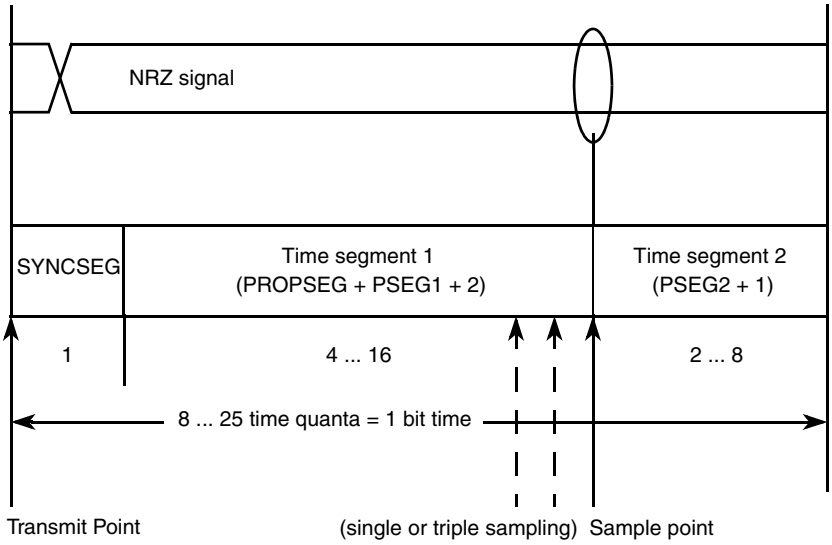


Figure 22-14. Segments within the Bit Time

Table 22-17 describes the time segment syntax:

Table 22-17. Time Segment Syntax

Syntax	Description
SYNCSEG	System expects transitions to occur on the bus during this period.
Transmit point	A node in transmit mode transfers a new value to the CAN bus at this point.
Sample point	A node in receive mode samples the bus at this point. If the three samples per bit option is selected, then this point marks the position of the third sample.

Table 22-18 gives an overview of the CAN compliant segment settings and the related parameter values.

NOTE

Ensure the bit time settings are in compliance with the CAN standard.

Table 22-18. CAN Standard Compliant Bit Time Segment Settings

Time Segment 1	Time Segment 2	Resynchronization Jump Width
5 .. 10	2	1 .. 2
4 .. 11	3	1 .. 3
5 .. 12	4	1 .. 4
6 .. 13	5	1 .. 4
7 .. 14	6	1 .. 4
8 .. 15	7	1 .. 4
9 .. 16	8	1 .. 4

22.4.5.5 Arbitration and Matching Timing

During normal transmission or reception of frames, the arbitration, match, move in and move out processes are executed during certain time windows inside the CAN frame, as shown in Figure 22-15. When doing matching and arbitration, FlexCAN2 needs to scan the whole message buffer memory during the available time slot. To have sufficient time to do that, the following restrictions must be observed:

- A valid CAN bit timing must be programmed, as indicated in Figure 22-15.
- The system clock frequency cannot be smaller than the oscillator clock frequency, i.e. the PLL cannot be programmed to divide down the oscillator clock.
- There must be a minimum ratio of 16 between the system clock frequency and the CAN bit rate.

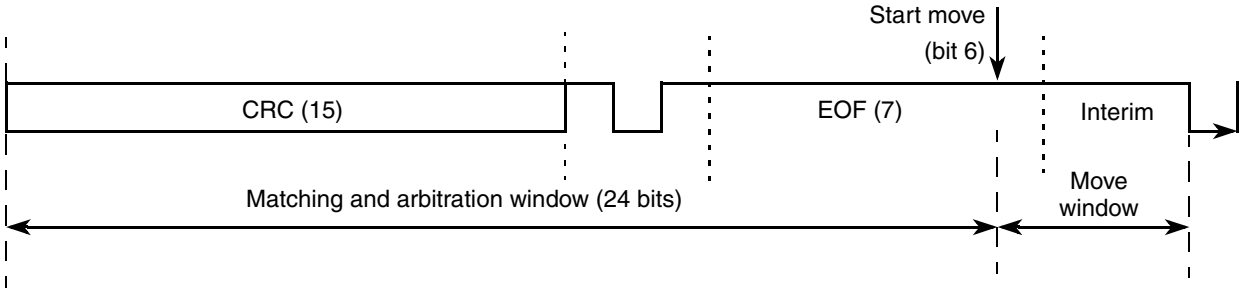


Figure 22-15. Arbitration, Match and Move Time Windows

22.4.6 Modes of Operation Details

22.4.6.1 Freeze Mode

This mode is entered by asserting the HALT bit in the CAN*x*_MCR or when the MCU is put into debug mode. In both cases it is also necessary that the FRZ bit is asserted in the CAN*x*_MCR. When freeze mode is requested during transmission or reception, FlexCAN2 does the following:

- Waits to be in either intermission, passive error, bus off or idle state
- Waits for all internal activities like move in or move out to finish
- Ignores the RX input pin and drives the TX pin as recessive
- Stops the prescaler, thus halting all CAN protocol activities
- Grants write access to the CAN*x*_ECR, which is read-only in other modes
- Sets the NOTRDY and FRZACK bits in CAN*x*_MCR

After requesting freeze mode, the user must wait for the FRZACK bit to be asserted in CAN*x*_MCR before executing any other action, otherwise FlexCAN2 can operate in an unpredictable way. In freeze mode, all memory mapped registers are accessible; CANx_RXIMR*n* registers can be programmed only if the MBFEN bit is asserted.

Exit freeze mode using one of the following methods:

- CPU negates the FRZ bit in the CAN*x*_MCR
- The MCU exits debug mode and/or the HALT bit negates.

After exiting freeze mode, FlexCAN2 tries to re-synchronize to the CAN bus by waiting for 11 consecutive recessive bits.

22.4.6.2 Module Disabled Mode

This low power mode is entered when the CAN*x*_MCR[MDIS] bit is asserted. If the module is disabled during freeze mode, it shuts down the clocks to the CPI and MBM sub-modules, sets the CAN*x*_MCR[MDISACK] bit and negates the CAN*x*_MCR[FRZACK] bit.

If the module is disabled during transmission or reception, FlexCAN2 completes the following sequence:

1. Waits to enter the idle or bus off state, or waits for the third bit of the intermission and checks to determine if the bit is recessive.
2. Waits for all internal activities, like move-in or move-out, to finish.
3. Ignores the RX input pin and drives the TX pin as recessive.
4. Shuts down the clocks to the CPI and MBM sub-modules.
5. Sets the NOTRDY and MDISACK bits in CAN*x*_MCR.

The bus interface unit continues to operate by enabling the CPU to access memory mapped registers except the free running timer, CAN*x*_ECR, and the message buffers, which cannot be accessed when the module is disabled. To exit this mode, negate the CAN*x*_MCR[MDIS] bit, which resumes the clocks and negates the CAN*x*_MCR[MDISACK] bit.

22.4.7 Interrupts

The module can generate interrupts from 20 interrupt sources (16 interrupts due to message buffers, one interrupt due to an error condition, two interrupts for the OR'd MB16–MB31 and MB32–63, and one interrupt for one of the following: a bus off condition, a transmit warning, or a receive warning).

Each of the 64 message buffers can be an interrupt source, if its corresponding CAN*x*_IMRH or CAN*x*_IMRL bit is set. There is no distinction between TX and RX interrupts for a particular buffer, under the assumption that the buffer is initialized for either transmission or reception. Each of the buffers has assigned a flag bit in the CAN*x*_IFRH or CAN*x*_IFRL registers. The bit is set when the corresponding buffer completes a successful transmission/reception and is cleared when the CPU writes it to 1.

A combined interrupt for each of two MB groups, MB16–MB31 and MB32–MB63, is also generated by an OR of all the interrupt sources from the associated MBs. This interrupt gets generated when any of the MBs generates an interrupt. In this case the CPU must read the CAN*x*_IFRH and CAN*x*_IFRL registers to determine which MB caused the interrupt.

The other two interrupt sources (bus off/transmit warning/receive warning and error) generate interrupts like the MB interrupt sources, and can be read from CAN*x*_ESR. The bus off/transmit warning/receive warning and error interrupt mask bits are located in the CAN*x*_CR.

22.4.8 Bus Interface

The CPU access to FlexCAN2 registers are subject to the following rules:

- Read and write access to unimplemented or reserved address space also results in access error. Any access to unimplemented MB locations results in access error.
- For a FlexCAN2 configuration that uses less than the total number of MBs and MAXMB is set accordingly, the remaining MB and RX mask register memory can be used as general-purpose RAM space. Byte, word and long word accesses are allowed to the unused MB space.

NOTE

Unused MB space must not be used as general purpose RAM while FlexCAN is transmitting and receiving CAN frames.

22.5 Initialization and Application Information

This section provides instructions for initializing the FlexCAN2 module.

22.5.1 FlexCAN2 Initialization Sequence

The FlexCAN2 module can be reset in three ways:

- MCU-level hard reset, which resets all memory mapped registers asynchronously
- MCU-level soft reset, which resets some of the memory mapped registers synchronously (see Table 22-2 for the registers affected by a soft reset)
- SOFTRST bit in CAN*x*_MCR, which has the same effect as the MCU level soft reset

A soft reset is synchronous and must follow an internal request/acknowledge procedure across clock domains. Therefore, it can take some time to fully propagate its effects. The SOFTRST bit remains asserted while a soft reset is pending, so software can poll this bit to determine when the reset completes.

After the module is enabled (CAN*x*_MCR[MDIS] bit negated), put FlexCAN2 in freeze mode before beginning the configuration. In freeze mode, FlexCAN2 is un-synchronized to the CAN bus, the HALT and FRZ bits in CAN*x*_MCR are set, the internal state machines are disabled and the FRZACK and NOTRDY bits in the CAN*x*_MCR are set. The CNTX pin is in recessive state and FlexCAN2 does not initiate frame transmission nor receives any frames from the CAN bus. The message buffer contents are not affected by reset, therefore are not automatically initialized.

For any configuration change or initialization, FlexCAN2 must be set to freeze mode (see Section 22.4.6.1, “Freeze Mode). A generic initialization process for the FlexCAN2 module is:

1. Initialize CANx_CR.
   — Determine bit timing parameters: PROPSEG, PSEG1, PSEG2, RJW.
   — Determine the bit rate by programming the PRESDIV field.
   — Determine internal arbitration mode (LBUF bit).
2. Initialize message buffers.
   — The control and status word of all message buffers can be written as active or inactive.
   — Initialize other entries in each message buffer as required.

3. Initialize CANx_MCR bits MBFEN, SRXDIS, and WRNEN.

   The initialization of FlexCAN registers for either global or individual acceptance masking depends on the configuration of MBFEN:

   — If MBFEN is negated, initialize CANx_RXGMASK, CANx_RX14MASK, and CANx_RX15MASK registers for acceptance mask.

   — If MBFEN is asserted, initialize CANx_RXIMR[0-63] for individual acceptance masking.

4. Set required mask bits in CAN*x*_IMRH and CAN*x*_IMRL registers (for all MBs interrupts), and in CAN*x*_CR (for bus off and error interrupts).
5. Negate the CAN*x*_MCR[HALT] bit.

Starting with this last event, FlexCAN2 attempts to synchronize with the CAN bus.

22.5.2 FlexCAN2 Addressing and RAM Size

There are 1024 bytes of RAM for a maximum of 64 message buffers. You can program the maximum number of message buffers (MBs) using the MAXMB field in the CAN*x*_MCR. For a 1024-byte RAM configuration, MAXMB can be any number from 0–63.

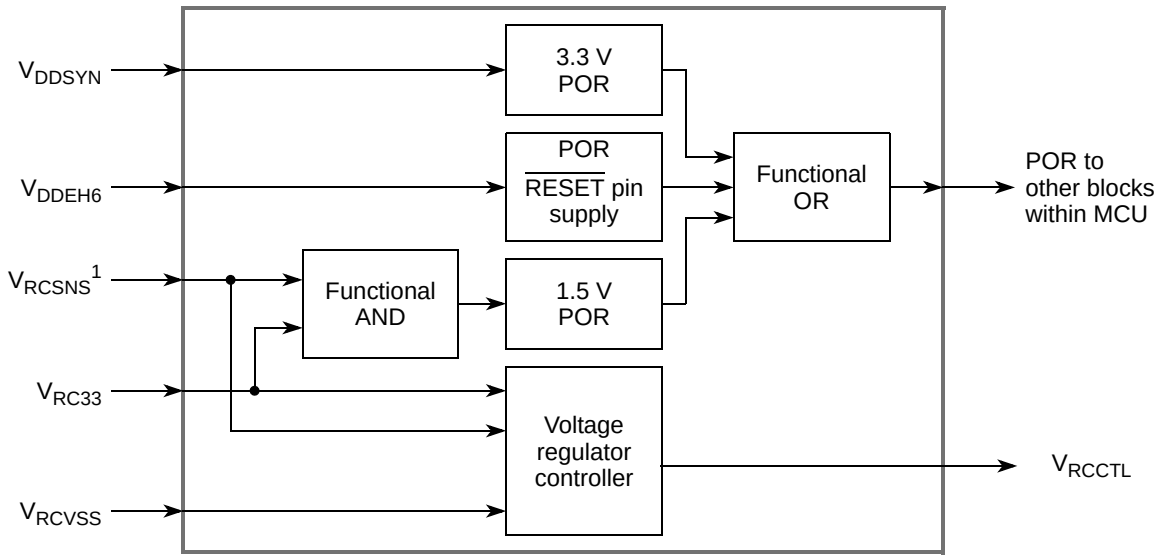
Chapter 23
Voltage Regulator Controller (VRC) and POR Module

23.1 Introduction

The voltage regulator controller (VRC) and power-on reset (POR) module contains circuitry to control regulation of the external 1.5 V supply used by the MPC5566. It also contains POR circuits for the 1.5 V supply, V_{DDSYN} and the V_{DDE} supply that powers the $\overline{\text{RESET}}$ pad.

23.1.1 Block Diagram

The block diagram of the VRC and POR module is shown in Figure 23-1. The diagram represents the various submodules as implemented on the device.



[1] This is not a package pin

Figure 23-1. Voltage Regulator Controller and POR Blocks

23.2 External Signal Description

Table 23-1 describes the VRC signals.

Table 23-1. Voltage Regulator Controller and POR Block External Signals

Signal	Type	Signal Level	Description
V_{RC33}	Supply pin	3.3 V	Regulator supply input. 3.3 V VRC supply input.
V_{DDSYN}	Supply pin	3.3 V	FMPLL supply input. This is the 3.3 V supply input for the frequency modulated phase lock loop (FMPLL) module.
V_{DDEH6}	Supply pin	3.3–5.0 V	$\overline{\text{RESET}}$ pin supply input. Power supply input for padring segment that contains the $\overline{\text{RESET}}$ pad.
V_{RCVSS}	Supply pin	0.0 V	Regulator supply ground. V_{RCVSS} is the 3.3 V ground reference for the on-chip 1.5 V regulator control circuit.
V_{RCSNS}	1.5 V sense	1.5 V	1.5 V sense used by VRC. Pad connected to V_{DD} plane in package—not a package ball. This is the 1.5 V sense from the external 1.5 V supply output of NPN transistor. This input is monitored by the VRC to determine the value for V_{RCCTL}. V_{RCSNS} is a pad on the die that is connected to a V_{DD} plane inside the package. It is not a package ball.
V_{RCCTL}	Current output	—	Regulator control output. The V_{RCCTL} sources base current to the external bypass transistor. The V_{RCCTL} signal is used with internal and external transistors to provide V_{DD}, which is the MCU 1.5 V power supply.
V_{DD}	Supply pin	1.5 V	Internal 1.5 V power supply input.

23.3 Memory Map and Register Definition

The VRC and POR module have no memory-mapped registers.

23.4 Functional Description

The VRC portion of the module contains a voltage regulator controller, and the POR portion contains circuits to monitor the voltage levels of the 1.5 V and V_{DDSYN} power supplies, as well as circuits to monitor the power supply for the $\overline{\text{RESET}}$ pad. The PORs indicate whether each supply monitored is above the specified voltage threshold. The PORs ensure that the device is correctly powered up during a power-on reset. POR holds the device in reset when any of the monitored supplies fall below the specified minimum voltage.

23.4.1 Voltage Regulator Controller

The VRC circuit has a control current for use with an external NPN transistor and an external resistor to power the 1.5 V V_{DD} supply. The control current is output on the V_{RCCTL} pin. The voltage regulator controller slowly turns on the pass transistor while the 3.3 V POR is asserted. The pass transistor is completely turned on by the time the 3.3 V POR negates.

The voltage regulator controller keeps the 1.5 V supply in regulation as long as V_{RC33} is in regulation. If more protection is desired, you can also supply an external 1.5 V low voltage reset circuit.

- If the on-chip voltage regulator controller is not used, an external 1.5 V supply is required. To avoid a power sequencing requirement when an external power supply is used, external 3.3 V must power V_{RC33} while the V_{RCCTL} pad is unconnected. In this case, the internal 1.5 V POR remains enabled.
- If V_{RC33} is not powered, the device is subject to the power sequencing requirements for the 1.5 V and 3.3 V, or $\overline{\text{RESET}}$ supplies. This ensures that the 1.5 V supply is high enough for internal logic to operate correctly during power-up.

Refer to Section 23.5.3, “Power Sequencing Requirements” for more information.

23.4.2 POR Circuits

The individual POR circuits asserts whenever the supply being monitored drops below the specified threshold. The entire device is in power-on reset if any of these supplies are below the values specified in the *MPC5566 Microcontroller Data Sheet*.

Power-on reset asserts as soon as possible after the voltage level of the POR supplies begin to rise. Each POR circuit negates before its supply rises to its specified range. Power-on reset remains asserted until all POR supplies rise above the maximum POR threshold. Each POR asserts after its supply drops below its specified range. The behavior for each POR during power sequencing is shown in Figure 23-2.

Before the 3.3 V POR circuit asserts when ramping up, or after it negates when ramping down, the device can exit POR but remain in system reset. In this case, MDO[0] is driving high and no clocks are toggling.

If the 3.3 V POR circuit is asserted, the device behaves as if in POR even if the 1.5 V and $\overline{\text{RESET}}$ power POR circuits have not yet asserted when ramping up or have negated when ramping down.

NOTE

The PORs for each supply are not intended to indicate that the voltage has dropped below the specified voltage range. You must monitor the supplies externally and assert $\overline{\text{RESET}}$ to achieve precise monitoring.

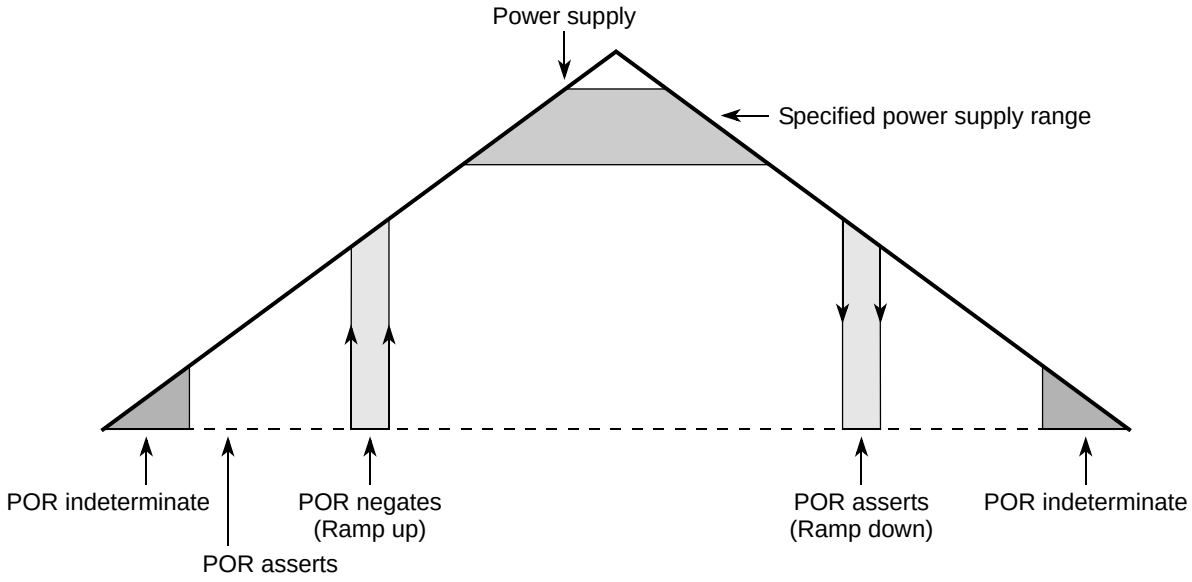


Figure 23-2. Regions POR is Asserted

23.4.2.1 1.5 V POR Circuit

The 1.5 V POR circuit monitors the voltage on the V_{RCSNS} pad. The 1.5 V POR functions if the V_{RC33} pad is powered. If the user does not power V_{RC33} to the specified voltage, the 1.5 V POR is disabled and the user must follow the specified power sequence.

23.4.2.2 3.3 V POR Circuit

The 3.3 V POR circuit is used to ensure that V_{DDSYN} is high enough that the FMPLL begins to operate correctly.

23.4.2.3 $\overline{\text{RESET}}$ Power POR Circuit

The $\overline{\text{RESET}}$ power POR circuit monitors the supply that powers the $\overline{\text{RESET}}$ pin, and ensures that the voltage supply to the $\overline{\text{RESET}}$ pin is high enough to reliably propagate the state of the input. The supply monitored by this POR cannot exceed 5.5 V.

23.5 Initialization and Application Information

23.5.1 Voltage Regulator Example

Figure 23-3 shows how to connect the VRC to the device.

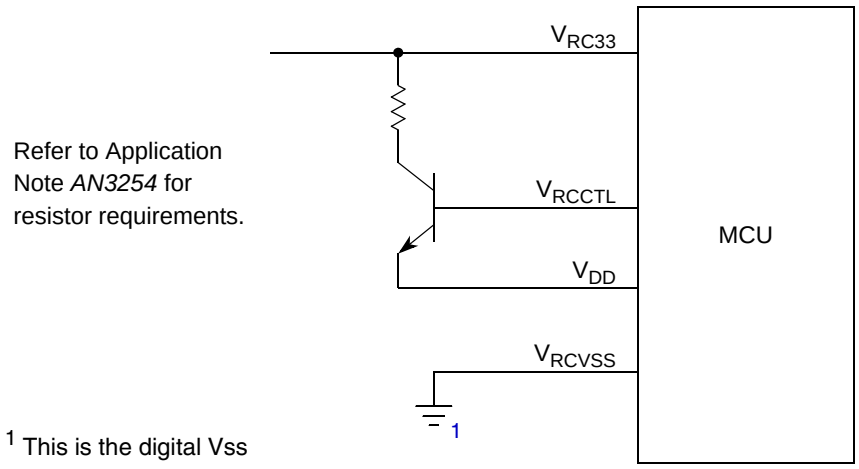


Figure 23-3. Voltage Regulator Controller Hookup

NOTE

Do not use Figure 23-3 as a reference for board design. Refer to *Application Note AN3254* for resistor requirements.

23.5.2 Compatible Power Transistors

The following NPN transistors are compatible with the on-chip VRC:

- ON Semiconductor™ NJD2873
- Phillips Semiconductor™ BCP68

Refer to the *MPC5566 Microcontroller Data Sheet* for information on the operating characteristics.

23.5.3 Power Sequencing Requirements

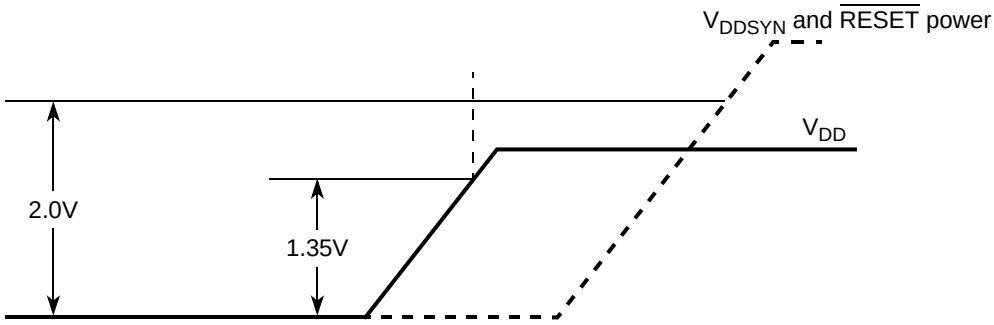
This section describes the following power sequencing requirements for the device:

- If an external 1.5 V power supply is used and V_{RC33} is tied to ground, power sequencing is required between the 1.5 V power supply, and V_{DDSYN} and the $\overline{\text{RESET}}$ power supplies. To avoid this power sequencing requirement, power up V_{RC33} within the specified operating range, even if not using the on-chip voltage regulator controller.
  Refer to Section 23.5.3.1, "Power-Up Sequence If V_{RC33} Grounded" and Section 23.5.3.2, "Power-Down Sequence If V_{RC33} Grounded."
- The V_{DD33} voltage must be high enough before POR negates to ensure the values on certain pins are treated as 1s when POR negates.
  Refer to Section 23.5.3.3, "Input Value of Pins During POR Dependent on V_{DD33}."

- When powering up, power sequencing is not required between V_{RC33} and V_{DDSYN}. However, for the VRC staged turn-on to operate within specification, V_{RC33} must not lead V_{DDSYN} by more than 600 mV, nor lag by more than 100 mV. Higher spikes in the emitter current of the pass transistor occur if V_{RC33} leads or lags V_{DDSYN} by exceeding these tolerances. The value of the current for the higher spikes depends on the board power supply circuitry and the amount of board-level capacitance.
- When powering down, delta tolerances between V_{RC33} and V_{DDSYN} are not required because the bypass capacitors internal and external to the device are already charged.
- When not powering up or down, delta tolerances between V_{RC33} and V_{DDSYN} are not required for the VRC to operate within specification.

23.5.3.1 Power-Up Sequence If V_{RC33} Grounded

The 1.5 V V_{DD} supply must rise to 1.35 V before the 3.3 V V_{DDSYN} and the $\overline{\text{RESET}}$ supplies rise above 2.0 V. This ensures that digital logic in the PLL for the 1.5 V supply does not begin to operate below the lower limit of the 1.35 V operation range. Because the internal 1.5 V POR is disabled, the internal 3.3 V POR or the $\overline{\text{RESET}}$ power POR must hold the device in reset. Since they can negate as low as 2.0 V, V_{DD} must be within the specification range before the 3.3 V POR and the $\overline{\text{RESET}}$ power POR negate.



NOTE: V_{DD} must reach 1.35 V before V_{DDSYN} and $\overline{\text{RESET}}$ reach 2.0 V.

Figure 23-4. Power-Up Sequence, V_{RC33} Grounded

23.5.3.2 Power-Down Sequence If V_{RC33} Grounded

The only requirement for the power-down sequence when V_{RC33} is grounded is that if V_{DD} decreases to less than its operating range, V_{DDSYN} or the $\overline{\text{RESET}}$ power must decrease to less than 2.0 V before the V_{DD} power is allowed to increase to its operating range. This ensures that the digital 1.5 V logic, which is reset by the ORed POR only that can cause the 1.5 V supply to decrease below its specification, is reset correctly.

23.5.3.3 Input Value of Pins During POR Dependent on V_{DD33}

To avoid selecting the bypass clock because PLLCFG[0:1] and $\overline{\text{RSTCFG}}$ were not treated as 1s when POR negates, V_{DD33} must not lag V_{DDSYN} and the $\overline{\text{RESET}}$ pin power when powering the device by more than the V_{DD33_LAG} specification. V_{DD33} can independently lag V_{DDSYN} *or* $\overline{\text{RESET}}$ by more than the V_{DD33_LAG} specification. The V_{DD33_LAG} specification applies regardless of whether V_{RC33} is powered. The V_{DD33_LAG} specification only applies during power up. V_{DD33} has no lead or lag requirements when powering down.

Refer to the following sections or documents for more information:

Section 23.5.3.4, “Pin Values after POR Negates”

MPC5566 Microcontroller Data Sheet for the V_{DD33_LAG} specification.

23.5.3.4 Pin Values after POR Negates

Depending on the final PLL mode required, the PLLCFG[0:1] and $\overline{\text{RSTCFG}}$ pins must have the values shown in Table 23-2 after POR negates. Refer to application note *AN2613, “MPC5554 Minimum Board Configuration”* for one example of the external configuration circuit.

Table 23-2. Values after POR Negation

Final PLL Mode	$\overline{\text{RSTCFG}}$	PLLCFG[0]	PLLCFG[1]
Crystal reference. Using $\overline{\text{RSTCFG}}$ to select Crystal Reference as the default.	1	—	—
Crystal reference. Using $\overline{\text{RSTCFG}}$ to *not* select Crystal Reference as the default.	—	1	—
External reference	0	1	1
Dual-controller	—	1	—

NOTE

After POR negates, $\overline{\text{RSTCFG}}$ and PLLCFG[0:1] can change to their final value, but do not switch through the 0, 0, 0 state on the pins.

Chapter 24
IEEE 1149.1 Test Access Port Controller (JTAGC)

24.1 Introduction

The JTAG port of the device consists of four inputs and one output. These pins include JTAG compliance select (JCOMP), test data input (TDI), test data output (TDO), test mode select (TMS), and test clock input (TCK). TDI, TDO, TMS, and TCK are compliant with the IEEE 1149.1-2001 standard and are shared with the NDI through the test access port (TAP) interface.

24.1.1 Block Diagram

Figure 24-1 is a block diagram of the JTAG Controller (JTAGC).

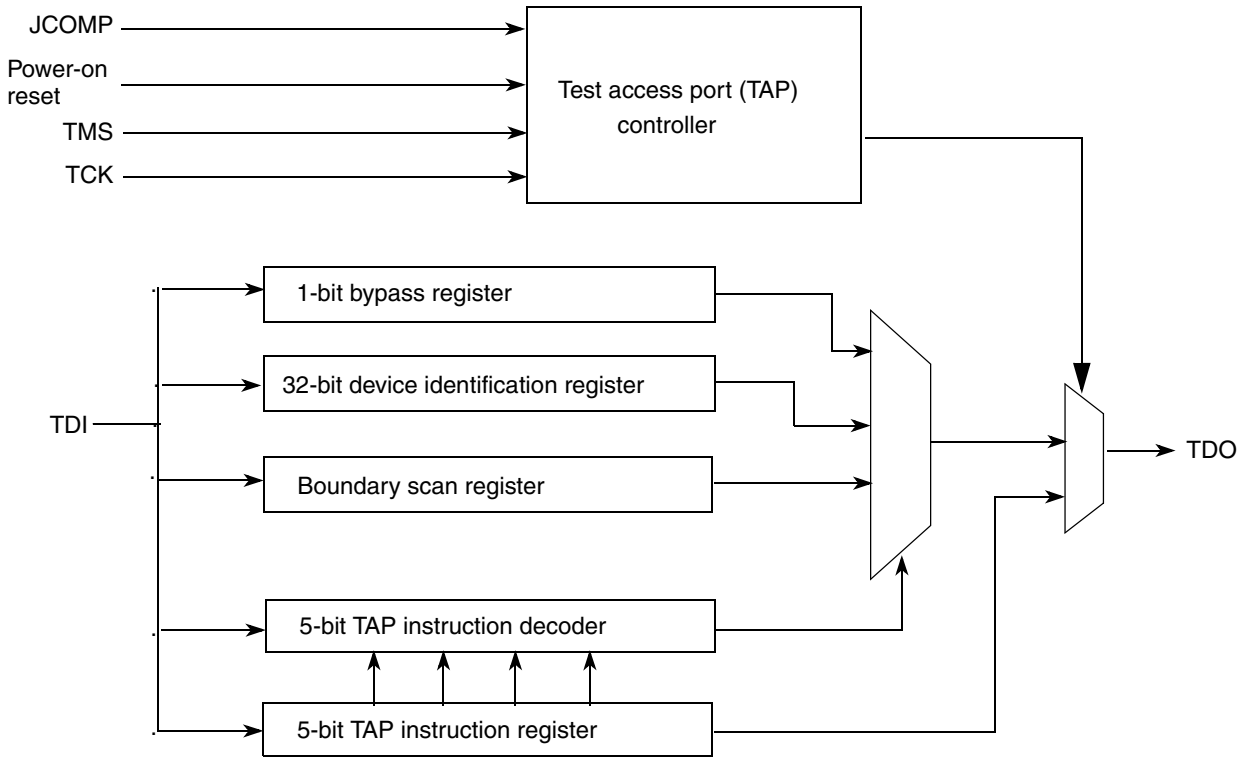


Figure 24-1. JTAG Controller Block Diagram

24.1.2 Overview

The JTAGC provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. In addition, instructions can be executed that allow the Test Access Port (TAP) to be shared with other modules on the MCU. All data input to and output from the JTAGC is communicated in serial format.

24.1.3 Features

The JTAGC is compliant with the IEEE 1149.1-2001 standard, and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface.
- 4 pins (TDI, TMS, TCK, and TDO), Refer to Section 24.2, “External Signal Description.”
- A JCOMP input that provides the ability to share the TAP.
- A 5-bit instruction register that supports several IEEE 1149.1-2001 defined instructions, as well as several public and private MCU specific instructions.
- Four test data registers: a bypass register, a boundary scan register, and a device identification register. The size of the boundary scan register is 480 bits.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

24.1.4 Modes of Operation

The JTAGC uses JCOMP and a power-on reset indication as its primary reset signals. Several IEEE 1149.1-2001 defined test modes are supported, as well as a bypass mode.

24.1.4.1 Reset

The JTAGC is placed in reset when the TAP controller state machine is in the TEST-LOGIC-RESET state. The TEST-LOGIC-RESET state is entered upon the assertion of the power-on reset signal, negation of JCOMP, or through TAP controller state machine transitions controlled by TMS. Asserting power-on reset or negating JCOMP results in asynchronous entry into the reset state. While in reset, the following actions occur:

- The TAP controller is forced into the test-logic-reset state, thereby disabling the test logic and allowing normal operation of the on-chip system logic to continue unhindered.
- The instruction register is loaded with the IDCODE instruction.

In addition, execution of certain instructions can result in assertion of the internal system reset. These instructions include EXTEST, CLAMP, and HIGHZ.

24.1.4.2 IEEE 1149.1-2001 Defined Test Modes

The JTAGC supports several IEEE 1149.1-2001 defined test modes. The test mode is selected by loading the appropriate instruction into the instruction register while the JTAGC is enabled. Supported test instructions include EXTEST, HIGHZ, CLAMP, SAMPLE and SAMPLE/PRELOAD. Each instruction defines the set of data registers that can operate and interact with the on-chip system logic while the instruction is current. Only one test data register path is enabled to shift data between TDI and TDO for each instruction.

The boundary scan register is enabled for serial access between TDI and TDO when the EXTEST, SAMPLE or SAMPLE/PRELOAD instructions are active. The single-bit bypass register shift stage is enabled for serial access between TDI and TDO when the HIGHZ, CLAMP or reserved instructions are active. The functionality of each test mode is explained in more detail in Section 24.4.4, "JTAGC Instructions."

24.1.4.3 Bypass Mode

When no test operation is required, the BYPASS instruction can be loaded to place the JTAGC into bypass mode. While in bypass mode, the single-bit bypass shift register is used to provide a minimum-length serial path to shift data between TDI and TDO.

24.1.4.4 TAP Sharing Mode

There are four selectable auxiliary TAP controllers that share the TAP with the JTAGC. Selectable TAP controllers include the Nexus port controller (NPC), e200 OnCE, eTPU Nexus, and eDMA Nexus. The instructions required to grant ownership of the TAP to the auxiliary TAP controllers are ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE, ACCESS_AUX_TAP_eTPU, ACCESS_AUX_TAP_DMA. Instruction opcodes for each instruction are shown in Table 24-3.

When the access instruction for an auxiliary TAP is loaded, control of the JTAG pins is transferred to the selected TAP controller. Any data input via TDI and TMS is passed to the selected TAP controller, and any TDO output from the selected TAP controller is sent back to the JTAGC to be output on the pins. The JTAGC regains control of the JTAG port during the UPDATE-DR state if the PAUSE-DR state was entered. Auxiliary TAP controllers are held in RUN-TEST/IDLE while they are inactive.

For more information on the TAP controllers refer to Chapter 25, "Nexus Development Interface."

24.2 External Signal Description

The JTAGC consists of five signals that connect to off-chip development tools and allow access to test support functions. The JTAGC signals are outlined in the following table:

Table 24-1. JTAG Signal Properties

Name	I/O	Function	Reset State	Pull[1]
TCK	I	Test clock	—	Down
TDI	I	Test data in	—	Up
TDO	O	Test data out	High Z [2]	Down [2]
TMS	I	Test mode select	—	Up
JCOMP	I	JTAG compliancy	—	Down

1 The pull is not implemented in this module. Pullup/down devices are implemented in the pads.

2 TDO output buffer enable is negated when JTAGC is not in the Shift-IR or Shift-DR states. A weak pulldown can be implemented on TDO.

24.3 Memory Map/Register Definition

This section provides a detailed description of the JTAGC registers accessible through the TAP interface, including data registers and the instruction register. Individual bit-level descriptions and reset states of each register are included. These registers are not memory-mapped and can only be accessed through the TAP.

24.3.1 Instruction Register

The JTAGC uses a 5-bit instruction register as shown in Figure 24-2. The instruction register allows instructions to be loaded into the module to select the test to be performed or the test data register to be accessed or both. Instructions are shifted in through TDI while the TAP controller is in the Shift-IR state, and latched on the falling edge of TCK in the Update-IR state. The latched instruction value can only be changed in the update-IR and test-logic-reset TAP controller states. Synchronous entry into the test-logic-reset state results in the IDCODE instruction being loaded on the falling edge of TCK. Asynchronous entry into the test-logic-reset state results in asynchronous loading of the IDCODE instruction. During the capture-IR TAP controller state, the instruction shift register is loaded with the value 0b10101, making this value the register's read value when the TAP controller is sequenced into the Shift-IR state.

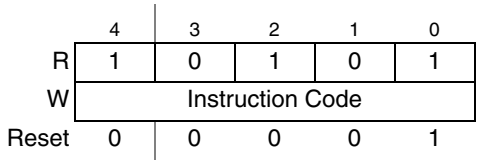


Figure 24-2. 5-Bit Instruction Register

24.3.2 Bypass Register

The bypass register is a single-bit shift register path selected for serial data transfer between TDI and TDO when the BYPASS, CLAMP, HIGHZ or reserve instructions are active. After entry into the capture-DR state, the single-bit shift register is set to a logic 0. Therefore, the first bit shifted out after selecting the bypass register is always a logic 0.

24.3.3 Device Identification Register

The device identification register, shown in Figure 24-3, allows the part revision number, design center, part identification number, and manufacturer identity code to be determined through the TAP. The device identification register is selected for serial data transfer between TDI and TDO when the IDCODE instruction is active. Entry into the capture-DR state while the device identification register is selected loads the IDCODE into the shift register to be shifted out on TDO in the Shift-DR state. No action occurs in the update-DR state.

IR[4:0]: 0_0001 (IDCODE) Access: R/O

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	PRN				DC						PIN										MIC											ID
W																																
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1

Figure 24-3. Device Identification Register

Table 24-2. Device Identification Register Field Descriptions

Field	Description
0–3 PRN	Part revision number. Contains the revision number of the device. This field changes with each revision of the device or module.
4–9 DC	Design center. Indicates the Freescale design center. For the MPC5566 this value is 0x20.
10–19 PIN	Part identification number. Contains the part number of the device. For the MPC5566, this value is 0x166.
20–30 MIC	Manufacturer identity code. Contains the reduced Joint Electron Device Engineering Council (JEDEC) ID for Freescale, 0xE.
31 ID	IDCODE register ID. Identifies this register as the device identification register and not the bypass register. Always set to 1.

24.3.4 Boundary Scan Register

The boundary scan register is connected between TDI and TDO when the EXTEST, SAMPLE or SAMPLE/PRELOAD instructions are active. It is used to capture input pin data, force fixed values on output pins, and select a logic value and direction for bidirectional pins. Each bit of the boundary scan register represents a separate boundary scan register cell, as described in the IEEE 1149.1-2001 standard and discussed in Section 24.4.5, “Boundary Scan.” The size of the boundary scan register is 480 bits.

24.4 Functional Description

24.4.1 JTAGC Reset Configuration

While in reset, the TAP controller is forced into the test-logic-reset state, thus disabling the test logic and allowing normal operation of the on-chip system logic. In addition, the instruction register is loaded with the IDCODE instruction.

24.4.2 IEEE 1149.1-2001 (JTAG) Test Access Port

The JTAGC uses the IEEE 1149.1-2001 TAP for accessing registers. This port can be shared with other TAP controllers on the MCU. Ownership of the port is determined by the value of the JCOMP signal and the currently loaded instruction. For more detail on TAP sharing via JTAGC instructions refer to Section 24.4.4.2, “ACCESS_AUX_TAP_x Instructions.”

Data is shifted between TDI and TDO though the selected register starting with the least significant bit, as illustrated in Figure 24-4. This applies for the instruction register, test data registers, and the bypass register.

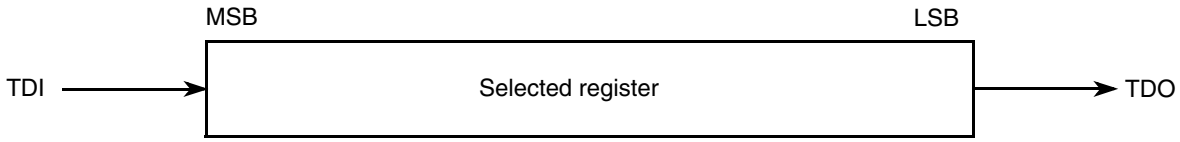
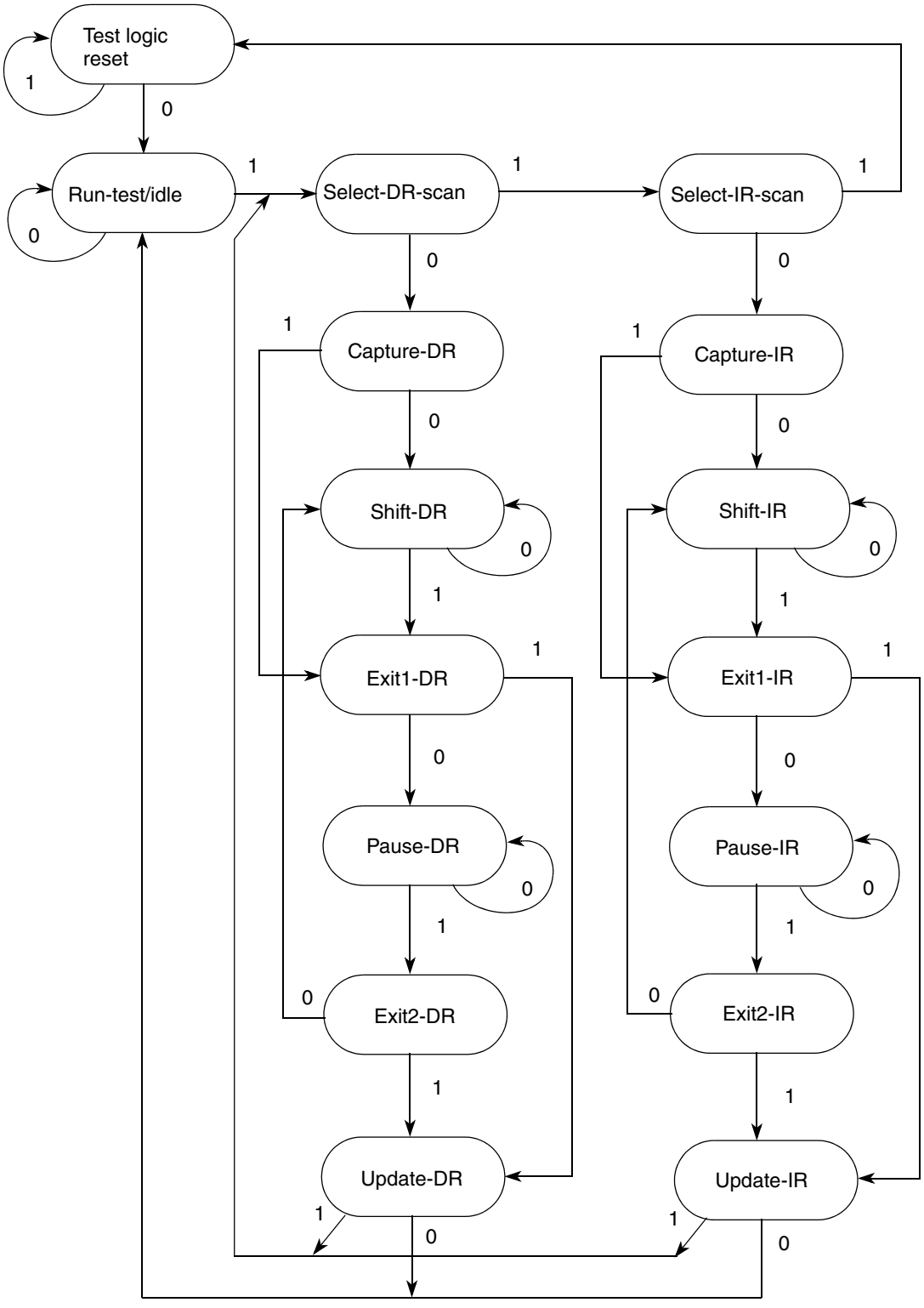


Figure 24-4. Shifting Data Through a Register

24.4.3 TAP Controller State Machine

The TAP controller is a synchronous state machine that interprets the sequence of logical values on the TMS pin. Figure 24-5 shows the machine’s states. The value shown next to each state is the value of the TMS signal sampled on the rising edge of the TCK signal.

As Figure 24-5 shows, holding TMS at logic 1 while clocking TCK through a sufficient number of rising edges also causes the state machine to enter the test-logic-reset state.



NOTE: The value shown adjacent to each state transition in this figure represents the value of TMS at the time of a rising edge of TCK.

Figure 24-5. IEEE 1149.1-2001 TAP Controller Finite State Machine

24.4.3.1 Enabling the TAP Controller

The JTAGC TAP controller is enabled by setting JCOMP to a logic 1 value.

24.4.3.2 Selecting an IEEE 1149.1-2001 Register

Access to the JTAGC data registers is done by loading the instruction register with any of the JTAGC instructions while the JTAGC is enabled. Instructions are shifted in via the select-IR-scan path and loaded in the update-IR state. At this point, all data register access is performed via the select-DR-scan path.

The select-DR-scan path is used to read or write the register data by shifting in the data (LSB first) during the shift-DR state. When reading a register, the register value is loaded into the IEEE 1149.1-2001 shifter during the capture-DR state. When writing a register, the value is loaded from the IEEE 1149.1-2001 shifter to the register during the update-DR state. When reading a register, there is no requirement to shift out the entire register contents. Shifting can be terminated after fetching the required number of bits.

24.4.4 JTAGC Instructions

This section gives an overview of each instruction, refer to the IEEE 1149.1-2001 standard for more details.

The JTAGC implements the IEEE 1149.1-2001 defined instructions listed in Table 24-3.

Table 24-3. JTAG Instructions

Instruction	Code[4:0]	Instruction Summary
IDCODE	00001	Selects device identification register for shift
SAMPLE/PRELOAD	00010	Selects boundary scan register for shifting, sampling, and preloading without disturbing functional operation
SAMPLE	00011	Selects boundary scan register for shifting and sampling without disturbing functional operation
EXTEST	00100	Selects boundary scan register while applying preloaded values to output pins and asserting functional reset
HIGHZ	01001	Selects bypass register while three-stating all output pins and asserting functional reset
CLAMP	01100	Selects bypass register while applying preloaded values to output pins and asserting functional reset
ACCESS_AUX_TAP_NPC	10000	Grants the Nexus port controller (NPC) ownership of the TAP
ACCESS_AUX_TAP_ONCE	10001	Grants the Nexus e200z6 core interface (NZ6C3) ownership of the TAP
ACCESS_AUX_TAP_eTPU	10010	Grants the Nexus dual-eTPU development interface (NDEDI) ownership of the TAP
ACCESS_AUX_TAP_DMA	10011	Grants the Nexus crossbar DMA interface (NXDM) ownership of the TAP
BYPASS	11111	Selects bypass register for data operations

Table 24-3. JTAG Instructions (continued)

Instruction	Code[4:0]	Instruction Summary
Factory Debug Reserved[1]	00101 00110 01010	Intended for factory debug only
Reserved[2]	All Other Codes	Decoded to select bypass register

1 Intended for factory debug, and not customer use

2 Freescale reserves the right to change the decoding of reserved instruction codes

24.4.4.1 BYPASS Instruction

BYPASS selects the bypass register, creating a single-bit shift register path between TDI and TDO. BYPASS enhances test efficiency by reducing the overall shift path when no test operation of the MCU is required. This allows more rapid movement of test data to and from other components on a board that are required to perform test functions. While the BYPASS instruction is active the system logic operates normally.

24.4.4.2 ACCESS_AUX_TAP_*x* Instructions

The ACCESS_AUX_TAP_*x* instructions allow the Nexus modules on the MCU to take control of the TAP. When this instruction is loaded, control of the TAP pins is transferred to the selected auxiliary TAP controller. Any data input via TDI and TMS is passed to the selected TAP controller, and any TDO output from the selected TAP controller is sent back to the JTAGC to be output on the pins. The JTAGC regains control of the JTAG port during the UPDATE-DR state if the PAUSE-DR state was entered. Auxiliary TAP controllers are held in RUN-TEST/IDLE while they are inactive.

24.4.4.3 CLAMP Instruction

CLAMP allows the state of signals driven from MCU pins to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. CLAMP enhances test efficiency by reducing the overall shift path to a single bit (the bypass register) while conducting an EXTEST type of instruction through the boundary scan register. CLAMP also asserts the internal system reset for the MCU to force a predictable internal state.

24.4.4.4 EXTEST — External Test Instruction

EXTEST selects the boundary scan register as the shift path between TDI and TDO. It allows testing of off-chip circuitry and board-level interconnections by driving preloaded data contained in the boundary scan register onto the system output pins. Typically, the preloaded data is loaded into the boundary scan register using the SAMPLE/PRELOAD instruction before the selection of EXTEST. EXTEST asserts the internal system reset for the MCU to force a predictable internal state while performing external boundary scan operations.

24.4.4.5 HIGHZ Instruction

HIGHZ selects the bypass register as the shift path between TDI and TDO. While HIGHZ is active, all output drivers are placed in an inactive drive state (for example, high impedance). HIGHZ also asserts the internal system reset for the MCU to force a predictable internal state.

24.4.4.6 IDCODE Instruction

IDCODE selects the 32-bit device identification register as the shift path between TDI and TDO. This instruction allows interrogation of the MCU to determine its version number and other part identification data. IDCODE is the instruction placed into the instruction register when the JTAGC is reset.

24.4.4.7 SAMPLE Instruction

The SAMPLE instruction obtains a sample of the system data and control signals present at the MCU input pins and just before the boundary scan register cells at the output pins. This sampling occurs on the rising edge of TCK in the capture-DR state when the SAMPLE instruction is active. The sampled data is viewed by shifting it through the boundary scan register to the TDO output during the Shift-DR state. There is no defined action in the update-DR state. Both the data capture and the shift operation are transparent to system operation.

24.4.4.8 SAMPLE/PRELOAD Instruction

The SAMPLE/PRELOAD instruction has two functions:

- The SAMPLE part of the instruction samples the system data and control signals on the MCU input pins and just before the boundary scan register cells at the output pins. This sampling occurs on the rising-edge of TCK in the capture-DR state when the SAMPLE/PRELOAD instruction is active. The sampled data is viewed by shifting it through the boundary scan register to the TDO output during the shift-DR state. Both the data capture and the shift operation are transparent to system operation.
- The PRELOAD part of the instruction initializes the boundary scan register cells before selecting the EXTEST or CLAMP instructions to perform boundary scan tests. This is achieved by shifting in initialization data to the boundary scan register during the shift-DR state. The initialization data is transferred to the parallel outputs of the boundary scan register cells on the falling edge of TCK in the update-DR state. The data is applied to the external output pins by the EXTEST or CLAMP instruction. System operation is not affected.

24.4.5 Boundary Scan

The boundary scan technique allows signals at component boundaries to be controlled and observed through the shift-register stage associated with each pad. Each stage is part of a larger boundary scan register cell, and cells for each pad are interconnected serially to form a shift-register chain around the border of the design. The boundary scan register consists of this shift-register chain, and is connected between TDI and TDO when the EXTEST, SAMPLE, or SAMPLE/PRELOAD instructions are loaded. The shift-register chain contains a serial input and serial output, as well as clock and control signals.

24.5 Initialization/Application Information

The test logic is a static logic design, and TCK can be stopped in either a high or low state without loss of data. However, the system clock is not synchronized to TCK internally. Any mixed operation using both the test logic and the system functional logic requires external synchronization.

To initialize the JTAGC module and enable access to registers, the following sequence is required:

1. Set the JCOMP signal to logic 1, thereby enabling the JTAGC TAP controller.
2. Load the appropriate instruction for the test or action to be performed.

Chapter 25
Nexus Development Interface

25.1 Introduction

The device microcontroller contains multiple Nexus clients that communicate over a single IEEE®-ISTO 5001™-2003 Nexus class 3 combined JTAG IEEE® 1149.1/auxiliary out interface. Combined, all of the Nexus clients are referred to as the Nexus development interface (NDI). Class 3 Nexus allows for program, data, and ownership trace of the microcontroller execution without access to the external data and address buses.

This chapter is organized in the following manner:

- The chapter opens with sections that provide a high level view of the Nexus development interface: Section 25.1, "Introduction" through Section 25.8, "NPC Initialization/Application Information."

The remainder of the chapter contains sections that discuss the remaining modules of the Nexus development interface:

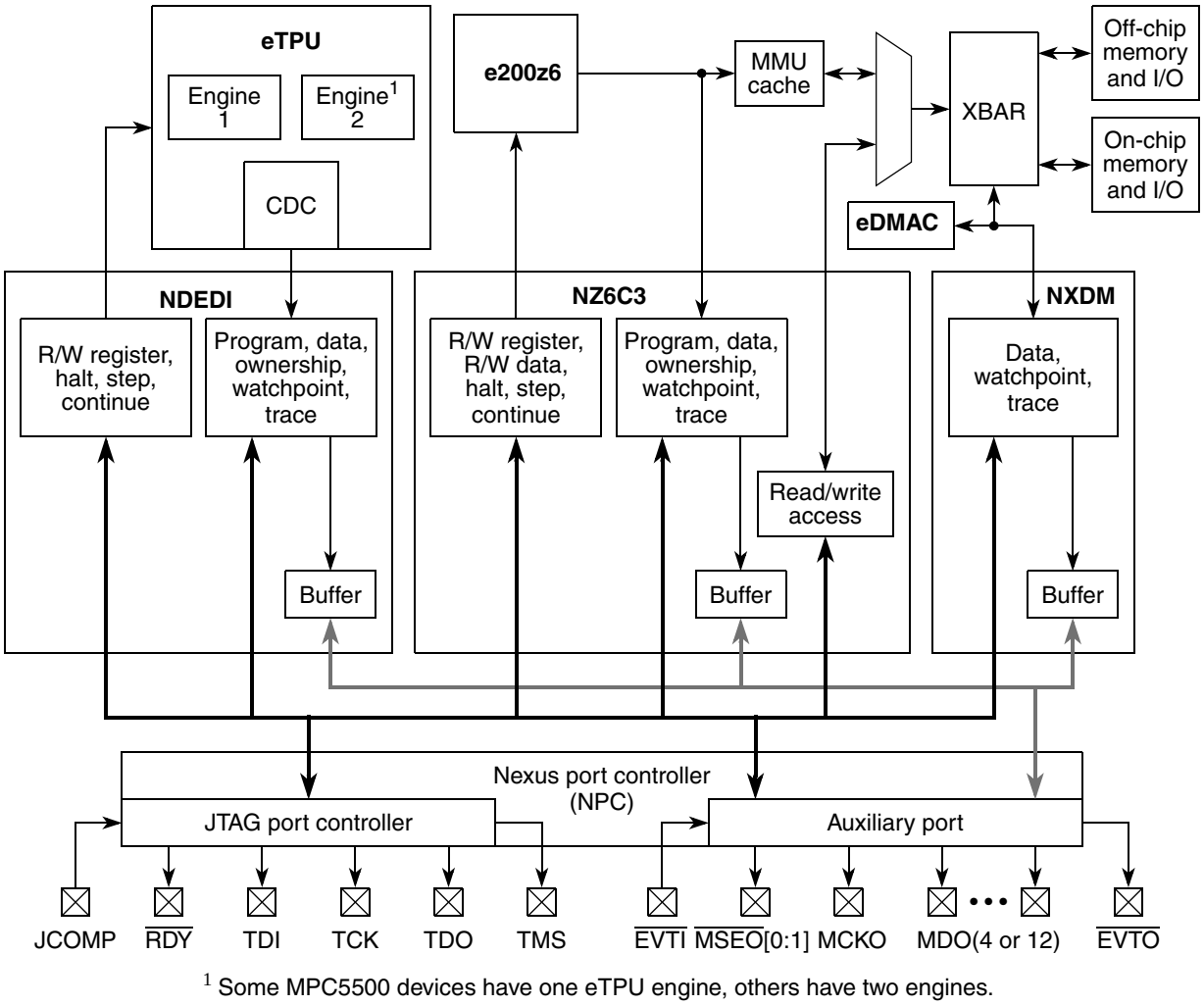
- Nexus dual-eTPU development interface (NDEDI). The device has two eTPU engines. Refer to Section 25.9, "Nexus Dual eTPU Development Interface (NDEDI)" and the *eTPU Reference Manual* for information about the NDEDI.
- Nexus e200z6 core interface (NZ6C3). In this chapter, the NZ6C3 interface is discussed in Section 25.10, "e200z6 Class 3 Nexus Module (NZ6C3) through Section 25.11, "NZ6C3 Memory Map and Register Definition."
- Nexus crossbar eDMA interface (NXDM). Refer to Section 25.15, "Nexus Crossbar eDMA Interface (NXDM)."

Communication to the NDI is handled via the auxiliary port and the JTAG port.

- The auxiliary port is comprised of nine or 17 output pins and 1 input pin. The output pins include one message clock out (MCKO) pin, four or 12 message data out (MDO) pins, two message start/end out ($\overline{\text{MSEO}}$) pins, one ready ($\overline{\text{RDY}}$) pin, and one event out ($\overline{\text{EVTO}}$) pin. Event in ($\overline{\text{EVTI}}$) is the only input pin for the auxiliary port.
- The JTAG port consists of four inputs and one output. These pins include JTAG compliance select (JCOMP), test data input (TDI), test data output (TDO), test mode select (TMS), and test clock input (TCK). TDI, TDO, TMS, and TCK are compliant with the IEEE® 1149.1-2001 standard and are shared with the NDI through the test access port (TAP) interface. JCOMP along with power-on reset and the TAP state machine are used to control reset for the NDI module. Ownership of the TAP is achieved by loading the appropriate enable instruction for the desired Nexus client in the JTAG controller (JTAGC) when JCOMP is asserted. Refer to Table 25-4 for the JTAGC opcodes to access the different Nexus clients.

25.1.1 Block Diagram

Figure 25.1.2 shows a general block diagram of the NDI components.



[1] Some MPC5500 devices have one eTPU engine, others have two engines.

Figure 25-1. NDI General Block Diagram

25.1.2 Features

The NDI module is compliant with the IEEE-ISTO 5001-2003 standard. The following features are implemented:

- 15- or 23-bit full duplex pin interface for medium and high visibility throughput
  - — One of two modes selected by register configuration: full port mode (FPM) and reduced port mode (RPM). FPM comprises 12 MDO pins, and RPM comprises 4 MDO pins.
  - — Auxiliary output port
    - – One MCKO (message clock out) pin
    - – Four or 12 MDO (message data out) pins

  - Two $\overline{\text{MSEO}}$ (message start/end out) pins
  - One $\overline{\text{RDY}}$ (ready) pin
  - One $\overline{\text{EVTO}}$ (event out) pin
- Auxiliary input port uses one $\overline{\text{EVTI}}$ (event in) pin
- Five-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)

- Host processor (e200z6) development support features (NZ6C3)
  - IEEE-ISTO 5001-2003 standard class 3 compliant.
  - Data trace via data write messaging (DWM) and data read messaging (DRM). This allows the development tool to trace reads and/or writes to selected internal memory resources.
  - Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An ownership trace message is transmitted when a new process/task is activated, allowing development tools to trace ownership flow.
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code can be traced.
  - Watchpoint messaging (WPM) via the auxiliary port.
  - Watchpoint trigger enable of program and/or data trace messaging.
  - Data tracing of instruction fetches via private opcodes.
  - Subset of Power Architecture Book E software debug facilities with OnCE block (Nexus class 1 features).
- eDMA development support features (NXDM)
  - Data trace via data write messaging (DWM) and data read messaging (DRM). This allows the development tool to trace DMA generated reads and/or writes to selected address ranges in the device's memory map.
  - Watchpoint messaging (WPM) via the auxiliary port.
  - Watchpoint trigger enable/disable of data trace messaging.
- eTPU development support features (NDEDI)
  - IEEE-ISTO 5001-2002 standard Class 3 compliant for the eTPU engines.
  - Data trace via data write messaging and data read messaging. This allows the development tool to trace reads and writes to selected shared parameter RAM (SPRAM) address ranges. Four data trace windows are shared by the two eTPU engines.
  - Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which channel is being serviced. An ownership trace message is transmitted to indicate when a new channel service request is scheduled, allowing the development tools to trace task flow. A special OTM is sent when the engine enters in idle state, meaning that all requests were serviced and no new requests are yet scheduled.
  - Program trace via branch trace messaging. BTM displays program flow discontinuities (start, jumps, return, etc.), allowing the development tool to interpolate what transpires between the

discontinuities. Thus static code can be traced. The branch trace messaging method uses the branch/predicate method to reduce the number of generated messages.

— Watchpoint messaging via the auxiliary port. WPM provides visibility of the occurrence of the eTPU's' watchpoints and breakpoints.

— Nexus based breakpoint/watchpoint configuration and single step support.

- Run-time access to the on-chip memory map via the Nexus read/write access protocol. This feature supports accesses for run-time internal visibility, calibration variable acquisition, calibration constant tuning, and external rapid prototyping for powertrain automotive development systems.
- All features are independently configurable and controllable via the IEEE® 1149.1 I/O port.
- The NDI block reset is controlled with JCOMP, power-on reset, and the TAP state machine. These sources are independent of system reset.
- System clock locked status indication via MDO0 following power-on reset.

25.1.3 Modes of Operation

The NDI block is in reset when the TAP controller state machine is in the TEST-LOGIC-RESET state. The TEST-LOGIC-RESET state is entered on the assertion of the power-on reset signal, negation of JCOMP, or through state machine transitions controlled by TMS. Assertion of JCOMP allows the NDI to move out of the reset state, and is a prerequisite to grant Nexus clients control of the TAP. Ownership of the TAP is achieved by loading the appropriate enable instruction for the desired Nexus client in the JTAGC controller (JTAGC) block when JCOMP is asserted.

Following negation of power-on reset, the NPC remains in reset until the system clock achieves lock. In PLL bypass mode, the NDI can transition out of the reset state immediately following negation of power-on reset. Refer to Section 25.4.5, "System Clock Locked Indication" for more details.

25.1.3.1 Nexus Reset Mode

In Nexus reset mode, the following actions occur:

- Register values default back to their reset values.
- The message queues are marked as empty.
- The auxiliary output port pins are negated if the NDI controls the pads.
- The TDO output buffer is disabled if the NDI has control of the TAP.
- The TDI, TMS, and TCK inputs are ignored.
- The NDI block indicates to the MCU that it is not using the auxiliary output port. This indication can be used to three-state the output pins or use them for another function.

25.1.3.2 Full-Port Mode

In full-port mode, all the available MDO pins are used to transmit messages. All trace features are enabled or can be enabled by writing the configuration registers via the JTAG port. The number of MDO pins available is 12.

25.1.3.3 Reduced-Port Mode

In reduced-port mode, a subset of the available MDO pins are used to transmit messages. All trace features are enabled or can be enabled by writing the configuration registers via the JTAG port. The number of MDO pins available is 4. Unused MDO (MDO[11:4]) pins can be used as GPIO. Details on GPIO functionality configuration can be found in Chapter 6, "System Integration Unit (SIU)."

25.1.3.4 Disabled-Port Mode

In disabled-port mode, message transmission is disabled. Any debug feature that generates messages can not be used. The primary features available are class 1 features and read/write access.

25.1.3.5 Censored Mode

When the device is in censored mode, reading the contents of internal flash externally is not allowed. To prevent Nexus modules from violating censorship, the NPC is held in reset when in censored mode, asynchronously holding all other Nexus modules in reset as well. This prevents Nexus read/write to memory mapped resources and the transmission of Nexus trace messages. Refer to Table 13-17 for information on Nexus port enabling and disabling regarding censorship.

25.2 External Signal Description

The auxiliary and JTAG pin interfaces provide for the transmission of messages from Nexus modules to the external development tools and for access to Nexus client registers. The auxiliary/JTAG pin definitions are outlined in Table 25-1.

Table 25-1. Signal Properties

Signal Name	Port	Function	Reset State
$\overline{\text{EVTO}}$	Auxiliary	Event out pin	Negated
$\overline{\text{EVTI}}$	Auxiliary	Event in pin	Pullup
MCKO	Auxiliary	Message clock out pin (from NPC)	Enabled
MDO[3:0] or MDO[11:0]	Auxiliary	Message data out pins	Driven Low[1]
$\overline{\text{MSEO}}$[1:0]	Auxiliary	Message start/end out pins	Negated
$\overline{\text{RDY}}$	Auxiliary	Ready out pin	Negated
JCOMP	JTAG	JTAG compliancy and TAP sharing control	Pulldown
TCK	JTAG	Test clock input	Pulldown
TDI	JTAG	Test data input	Pullup
TDO	JTAG	Test data output	Pullup
TMS	JTAG	Test mode select input	Pullup

[1] Following a power-on reset, MDO[0] remains asserted until power-on reset is exited and the system clock achieves lock.

25.2.1 Detailed Signal Descriptions

This section describes each of the signals listed in Table 25-1 in more detail.

25.2.1.1 Event Out (EVTO)

EVTO is an output pin that is asserted upon breakpoint occurrence to provide breakpoint status indication or to signify that an event has occurred. The EVTO output of the NPC is generated based on the values of the individual EVTO signals from all Nexus modules that implement the signal.

25.2.1.2 Event In (EVTI)

EVTI is used to initiate program and data trace synchronization messages or to generate a breakpoint. EVTI is edge-sensitive for synchronization and breakpoint generation.

25.2.1.3 Message Data Out (MDO[3:0] or [11:0])

Message data out (MDO) are output pins used for uploading OTM, BTM, DTM, and other messages to the development tool. The development tool should sample MDO on the rising edge of MCKO. The width of the MDO bus used is determined by the Nexus PCR[FPM] configuration.

Following a power-on reset, MDO[0] remains asserted until power-on reset is exited and the system clock achieves lock.

25.2.1.4 Message Start/End Out (MSEO[1:0])

MSEO[1:0] are output pins that indicates when a message on the MDO pins has started, when a variable length packet has ended, or when the message has ended. The development tool should sample the MSEO pins on the rising edge of MCKO.

25.2.1.5 Ready (RDY)

RDY is an output pin that indicates when a device is ready for the next access.

25.2.1.6 JTAG Compliancy (JCOMP)

The JCOMP signal enables or disables the TAP controller. The TAP controller is enabled when JCOMP asserted, otherwise the TAP controller remains in reset.

25.2.1.7 Test Data Output (TDO)

The TDO pin transmits serial output for instructions and data. TDO is tri-stateable and is actively driven in the SHIFT-IR and SHIFT-DR controller states. TDO is updated on the falling edge of TCK and sampled by the development tool on the rising edge of TCK.

25.2.1.8 Test Clock Input (TCK)

The TCK pin is used to synchronize the test logic and control register access through the JTAG port.

25.2.1.9 Test Data Input (TDI)

The TDI pin receives serial test instruction and data. TDI is sampled on the rising edge of TCK.

25.2.1.10 Test Mode Select (TMS)

The TMS pin is used to sequence the IEEE® 1149.1-2001 TAP controller state machine. TMS is sampled on the rising edge of TCK.

25.3 Memory Map

The NDI block contains no memory mapped registers. Nexus registers are accessed by the development tool via the JTAG port using a register index and a client select value. The client select is controlled by loading the correct access instruction into the JTAG controller; refer to Table 25-4. OnCE registers are accessed by loading the appropriate value in the RS[0:6] field of the OnCE command register (OCMD) via the JTAG port.

Table 25-2 shows the NDI registers by Client Source ID and Index values.

Table 25-2. Nexus Development Interface (NDI) Registers

Client Source ID	Index	Register
e200z6 Control and Status Registers[1]		
0b0000	2	e200z6 Development Control1 (NZ6C3_DC1)
0b0000	3	e200z6 Development Control2 (NZ6C3_DC2)
0b0000	4	e200z6 Development Status (NZ6C3_DS)
0b0000	6	e200z6 User Base Address (NZ6C3_UBA)
0b0000	7	Read/Write Access Control/Status (NZ6C3_RWCS)
0b0000	9	Read/Write Access Address (NZ6C3_RWA)
0b0000	10	Read/Write Access Data (NZ6C3_RWD)
0b0000	11	e200z6 Watchpoint Trigger (NZ6C3_WT)
0b0000	13	e200z6 Data Trace Control (NZ6C3_DTC)
0b0000	14	e200z6 Data Trace Start Address 0 (NZ6C3_DTSA1)
0b0000	15	e200z6 Data Trace Start Address 1 (NZ6C3_DTSA2)
0b0000	18	e200z6 Data Trace End Address 0 (NZ6C3_DTEA1)
0b0000	19	e200z6 Data Trace End Address 1 (NZ6C3_DTEA2)
eDMA 1 Control and Status Registers		
0b0001	2	eDMA 1 Development Control (NXDM_DC)
0b0001	11	eDMA 1 Watchpoint Trigger (NXDM_WT)
0b0001	13	eDMA 1 Data Trace Control (NXDM_DTC)

Table 25-2. Nexus Development Interface (NDI) Registers (continued)

Client Source ID	Index	Register
0b0001	14	eDMA 1 Data Trace Start Address 0 (NXDM_DTSA1)
0b0001	15	eDMA 1 Data Trace Start Address 1 (NXDM_DTSA2)
0b0001	18	eDMA 1 Data Trace End Address 0 (NXDM_DTEA1)
0b0001	19	eDMA 1 Data Trace End Address 1 (NXDM_DTEA2)
0b0001	22	eDMA 1 Breakpoint and Watchpoint Control 1 (NXDM_BWC1)
0b0001	23	eDMA 1 Breakpoint and Watchpoint Control 2 (NXDM_BWC2)
0b0001	30	eDMA 1 Breakpoint and Watchpoint Address 1 (NXDM_BWA1)
0b0001	31	eDMA 1 Breakpoint and Watchpoint Address 2 (NXDM_BWA2)
eDMA_2 Control/Status Registers		
0b0101	2	eDMA 2 Development Control (AHB_DC*n*)
0b0101	11	eDMA 2 Watchpoint Trigger (AHB_WT*n*)
0b0101	13	eDMA 2 Data Trace Control (AHB_DTC*n*)
0b0101	14	eDMA 2 Data Trace Start Address 0 (AHB_DTSA1*n*)
0b0101	15	eDMA 2 Data Trace Start Address 1 (AHB_DTSA2*n*)
0b0101	18	eDMA 2 Data Trace End Address 0 (AHB_DTEA1*n*)
0b0101	19	eDMA 2 Data Trace End Address 1 (AHB_DTEA2*n*)
0b0101	22	eDMA 2 Breakpoint/Watchpoint Control 1 (AHB_BWC1*n*)
0b0101	23	eDMA 2 Breakpoint/Watchpoint Control 2 (AHB_BWC2*n*)
0b0101	30	eDMA 2 Breakpoint/Watchpoint Address 1 (AHB_BWA1*n*)
0b0101	31	eDMA 2 Breakpoint/Watchpoint Address 2 (AHB_BWA2*n*)
eTPU B Control/Status Registers		
0bxxxx	0	Device ID (DID)
0b0011	2	eTPU2 Development Control (NDI_eTPU2_DC)
0b0011	4	eTPU2 Development Status (NDEDI_eTPU2_DS)
0b0000	7	Read/Write Access Control/Status (RWCS)
0b0000	9	Read/Write Access Address (RWA)
0b0000	10	Read/Write Access Data (RWD)
0b0011	11	eTPU2 Watchpoint Trigger (NDI_eTPU2_WT)
0b0011	13	eTPU2 Data Trace Control (NDI_eTPU2_DTC)
0b0011	22	eTPU2 Breakpoint/Watchpoint Control 1 (NDEDI_eTPU2_BWC1)
0b0011	23	eTPU2 Breakpoint/Watchpoint Control 2 (NDEDI_eTPU2_BWC2)
0b0011	24	eTPU2 Breakpoint/Watchpoint Control 3 (NDEDI_eTPU2_BWC3)

Table 25-2. Nexus Development Interface (NDI) Registers (continued)

Client Source ID	Index	Register
0b0011	30	eTPU2 Breakpoint/Watchpoint Address 1 (NDEDI_eTPU2_BWA1)
0b0011	31	eTPU2 Breakpoint/Watchpoint Address 2 (NDEDI_eTPU2_BWA2)
0b0011	38	eTPU2 Breakpoint/Watchpoint Data 1 (NDEDI_eTPU2_BWD1)
0b0011	39	eTPU2 Breakpoint/Watchpoint Data 1 (NDEDI_eTPU2_BWD2)
0b0011	64	eTPU2 Program Trace Channel Enable (NDI_eTPU2_PTCE)
0b0011	69	eTPU2 Microinstruction Debug Register (NDEDI_eTPU2_INST)
0b0011	70	eTPU2 Microprogram Counter Debug Register (NDEDI_eTPU2_MPC)
0b0011	71	eTPU2 Channel Flag Status Register (NDEDI_eTPU2_CFSR)
0bxxxx	127	Port Configuration Register (PCR)
eTPU CDC Control/Status Registers		
0b0100	13	eTPU CDC Data Trace Control (NDEDI_CDC_DTC)
eTPU1 / eTPU2 / CDC Shared Control/Status Registers		
0b0010 or 0b0011 or 0b0100	65	eTPU Data Trace Address Range 0 (eTPU_DTAR0)
0b0010 or 0b0011 or 0b0100	66	eTPU Data Trace Address Range 1 (eTPU_DTAR1)
0b0010 or 0b0011 or 0b0100	67	eTPU Data Trace Address Range 2 (eTPU_DTAR2)
0b0010 or 0b0011 or 0b0100	68	eTPU Data Trace Address Range 3 (eTPU_DTAR3)

[1] These e200z6 registers are described in the *e200z6 PowerPC™ Core Reference Manual*.

Table 25-3 shows the OnCE register addressing.

Table 25-3. e200z6 OnCE Register Addressing

OCMD, RS[0:6]	Register Selected
000 0000–000 0001	Reserved
000 0010	JTAG DID (read-only)
000 0011–000 1111	Reserved
001 0000	CPU Scan Register (CPUSCR)
001 0001	No Register Selected (Bypass)
001 0010	OnCE Control Register (OCR)

Table 25-3. e200z6 OnCE Register Addressing (continued)

OCMD, RS[0:6]	Register Selected
001 0011–001 1111	Reserved
010 0000	Instruction Address Compare 1 (IAC1)
010 0001	Instruction Address Compare 2 (IAC2)
010 0010	Instruction Address Compare 3 (IAC3)
010 0011	Instruction Address Compare 4 (IAC4)
010 0100	Data Address Compare 1 (DAC1)
010 0101	Data Address Compare 2 (DAC2)
010 0110–010 1011	Reserved
010 1100	Debug Counter Register (DBCNT)
010 1101	Debug PCFIFO (PCFIFO) (read-only)
010 1110–010 1111	Reserved
011 0000	Debug Status Register (DBSR)
011 0001	Debug Control Register 0 (DBCR0)
011 0010	Debug control register 1 (DBCR1)
011 0011	Debug control register 2 (DBCR2)
011 0100	Debug control register 3 (DBCR3)
011 0101–101 1111	Reserved (do not access)
111 0000–111 1011	General purpose register selects [0:11]
111 1100	Nexus3-access
111 1101	LSRL select
111 1110	Enable_OnCE (and bypass)
111 1111	Bypass

25.4 NDI Functional Description

25.4.1 Enabling Nexus Clients for TAP Access

After the NDI is out of the reset state, the loading of a specific instruction in the JTAG controller (JTAGC) block is required to grant the NDI ownership of the TAP. Each Nexus client has its own JTAGC instruction opcode for ownership of the TAP, granting that client the means to read/write its registers. The JTAGC instruction opcode for each Nexus client is shown in Table 25-4. After the JTAGC opcode for a client has been loaded, the client is enabled by loading its NEXUS-ENABLE instruction. The NEXUS-ENABLE instruction opcode for each Nexus client is listed in Table 25-5. Opcodes for all other instructions supported by Nexus clients can be found in the relevant sections of this chapter.

Table 25-4. JTAG Client Select Instructions

JTAGC Instruction	Opcode	Description
ACCESS_AUX_TAP_NPC	10000	Enables access to the NPC TAP controller
ACCESS_AUX_TAP_ONCE	10001	Enables access to the e200z6 OnCE TAP controller
ACCESS_AUX_TAP_eTPU	10010	Enables access to the eTPU Nexus TAP controller
ACCESS_AUX_TAP_DMA	10011	Enables access to the eDMA Nexus TAP controller

Table 25-5. Nexus Client JTAG Instructions

Instruction	Description	Opcode
NPC JTAG Instruction Opcodes		
NEXUS_ENABLE	Opcode for NPC Nexus Enable instruction (4-bits)	0x0
BYPASS	Opcode for the NPC BYPASS instruction (4-bits)	0xF
e200z6 OnCE JTAG Instruction Opcodes[1]		
NEXUS3_ACCESS	Opcode for e200z6 OnCE Nexus Enable instruction (10-bits)	0x7C
BYPASS	Opcode for the e200z6 OnCE BYPASS instruction (10-bits)	0x7F
eDMA Nexus JTAG Instruction Opcodes		
NEXUS_ACCESS	Opcode for eDMA Nexus Enable instruction (4-bits)	0x0
BYPASS	Opcode for the eDMA Nexus BYPASS instruction (4-bits)	0xF

[1] Refer to the e200z6 Reference Manual for a complete list of available OnCE instructions.

25.4.2 Configuring the NDI for Nexus Messaging

The NDI is placed in disabled mode upon exit of power-on reset. If message transmission via the auxiliary port is desired, a write to the port configuration register (PCR) located in the NPC is then required to enable the NDI and select the mode of operation. Asserting MCKO_EN in the PCR places the NDI in enabled mode and enables MCKO. The frequency of MCKO is selected by writing the MCKO_DIV field. Asserting or negating the FPM bit selects full-port or reduced-port mode, respectively. When writing to the PCR, the PCR lsb (least significant bit) must be written to a logic 0. Setting the lsb of the PCR enables factory debug mode and prevents the transmission of Nexus messages.

Table 25-6 describes the NDI configuration options.

Table 25-6. NDI Configuration Options

JCOMP Asserted	MCKO_EN bit of the Port Configuration Register	FPM bit of the Port Configuration Register	Configuration
No	X	X	Reset
Yes	0	X	Disabled
Yes	1	1	Full-port mode
Yes	1	0	Reduced-port mode

25.4.3 Programmable MCKO Frequency

MCKO is an output clock to the development tools used for the timing of $\overline{\text{MSEO}}$ and MDO pin functions. MCKO is derived from the system clock, and its frequency is determined by the value of the MCKO_DIV field in the port configuration register (PCR) located in the NPC. Possible operating frequencies include one-half, one-quarter, and one-eighth system clock speed.

Table 25-7 shows the MCKO_DIV encodings. In this table, SYS_CLK represents the system clock frequency. The default value selected if a reserved encoding is programmed is SYS_CLK/2.

Table 25-7. MCKO_DIV Values

MCKO_DIV[2:0]	MCKO Frequency
0b000	SYS_CLK
0b001	SYS_CLK / 2
0b010	Reserved
0b011	SYS_CLK / 4
0b100	Reserved
0b101	Reserved
0b110	Reserved
0b111	SYS_CLK / 8

25.4.4 Nexus Messaging

Most of the messages transmitted by the NDI include a SRC field. This field is used to identify which source generated the message. Table 25-8 shows the values used for the SRC field by the different clients on the device. These 4-bit values are specific to the device. The same values are used for the client select values written to the client select control register.

Table 25-8. SRC Packet Encodings

SRC[3:0]	Client
0b0000	e200z6
0b0001	eDMA
0b0011	eTPU2 (ENGINE2_SRC)
0b0100	eTPU CDC[1] (CDC_SRC)
0b0101–0b1111	Reserved

[1] CDC is the eTPU Coherent Dual-Parameter Controller. Refer to the *eTPU Reference Manual* for more information.

25.4.5 System Clock Locked Indication

Following a power-on reset, the lsb of the auxiliary output port pins (MDO0) can be monitored to provide the lock status of the system clock. MDO0 is driven to a logic 1 until the system clock achieves lock after

exiting power-on reset. After the system clock is locked, MDO0 is negated and tools may begin Nexus configuration. Loss of lock conditions that occur subsequent to the exit of power-on reset and the initial lock of the system clock do not cause a Nexus reset, and therefore do not result in MDO0 driven high.

25.5 Nexus Port Controller (NPC)

The Nexus port controller (NPC) is that part of the NDI that controls access and arbitration of the device's internal Nexus modules. The NPC contains the port configuration register (PCR) and the device identification register (DID). The contents of the NPC DID are the same as the JTAGC device identification register.

25.5.1 Overview

The device incorporates multiple modules that require development support. Each of these modules implements a development interface based on the IEEE-ISTO 5001-2001 standard and must share the input and output ports that interface with the development tool. The NPC controls the usage of these ports in a manner that allows the individual modules to share the ports, while appearing to the development tool as a single module.

25.5.2 Features

The NPC performs the following functions:

- Controls arbitration for ownership of the Nexus auxiliary output port
- Nexus device identification register and messaging
- Generates MCKO enable and frequency division control signals
- Controls sharing of $\overline{\text{EVTO}}$
- Control of the device-wide debug mode
- Generates asynchronous reset signal for Nexus modules based on JCOMP input, censorship status, and power-on reset status
- System clock locked status indication via MDO[0] during Nexus reset
- Provides Nexus support for censorship mode

25.6 Memory Map/Register Definition

This section provides a detailed description of the NPC registers accessible to the end user. Individual bit-level descriptions and reset states of the registers are included.

25.6.1 Memory Map

Table 25-9 shows the NPC registers by index values. The registers are not memory-mapped and can only be accessed via the TAP. The NPC does not implement the client select control register because the value does not matter when accessing the registers. The bypass register (refer to Section 25.6.2.1, "Bypass Register") and instruction register (refer to Section 25.6.2.2, "Instruction Register") have no index values. These registers are not accessed in the same manner as Nexus client registers.

Table 25-9. NPC Memory Map

Index	Register Name	Register Description	Bits
0	DID	Device ID register	32
127	PCR	Port configuration register	32

25.6.2 Register Descriptions

This section consists of NPC register descriptions. Additional information regarding references to the TAP controller state may be found in Section 24.4.3, "TAP Controller State Machine."

25.6.2.1 Bypass Register

The bypass register is a single-bit shift register path selected for serial data transfer between TDI and TDO when the BYPASS instruction or any unimplemented instructions are active. After entry into the Capture-DR state, the single-bit shift register is set to a logic 0. Therefore, the first bit shifted out after selecting the bypass register is always a logic 0.

25.6.2.2 Instruction Register

The NPC uses a 4-bit instruction register as shown in Figure 25-2. The instruction register is accessed via the SELECT_IR_SCAN path of the tap controller state machine, and allows instructions to be loaded into the module to enable the NPC for register access (NEXUS_ENABLE) or select the bypass register as the shift path from TDI to TDO (BYPASS or unimplemented instructions).

Instructions are shifted in through TDI while the TAP controller is in the Shift-IR state, and latched on the falling edge of TCK in the Update-IR state. The latched instruction value can only be changed in the Update-IR and test-logic-reset TAP controller states. Synchronous entry into the test-logic-reset state results in synchronous loading of the BYPASS instruction. Asynchronous entry into the test-logic-reset state results in asynchronous loading of the BYPASS instruction. During the Capture-IR TAP controller state, the instruction register is loaded with the value of the previously executed instruction, making this value the register's read value when the TAP controller is sequenced into the Shift-IR state.

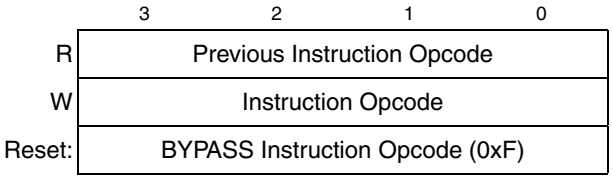


Figure 25-2. 4-Bit Instruction Register

25.6.2.3 Nexus Device ID Register (DID)

The NPC device identification register, shown in Figure 25-3, allows the part revision number, design center, part identification number, and manufacturer identity code of the part to be determined through the auxiliary output port.

Reg Index: 0 Access: User R/O

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Part Revision Number				Design Center						Part Identification Number					
W																
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Part Identification Number (*continued*)				Manufacturer Identity Code											1
W																
Reset	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	1

Figure 25-3. Nexus Device ID Register (DID)

Table 25-10. DID Register Field Descriptions

Field	Description
31–28 PRN	Part revision number. Contains the revision number of the part. This field changes with each revision of the device or module.
27–22 DC	Design center. Indicates the Freescale design center. This value is 0x20.
21–12 PIN	Part identification number. Contains the part number of the device. The PIN for the MPC5566 is 0x166.
11–1 MIC	Manufacturer identity code. Contains the reduced Joint Electron Device Engineering Council (JEDEC) ID for Freescale, 0xE.
0	Fixed per JTAG 1149.1 Always set to 1.

25.6.2.4 Port Configuration Register (PCR)

The PCR, shown in Figure 25-4, is used to select the NPC mode of operation, enable MCKO and select the MCKO frequency, and enable or disable MCKO gating. This register must be configured as soon as the NPC is enabled.

NOTE

The mode (MCKO_GT) or clock division (MCKO_DIV) bits must not be modified after MCKO has been enabled. Changing the mode or clock division while MCKO is enabled can produce unpredictable results.

Reg Index: 127 Access: R/W

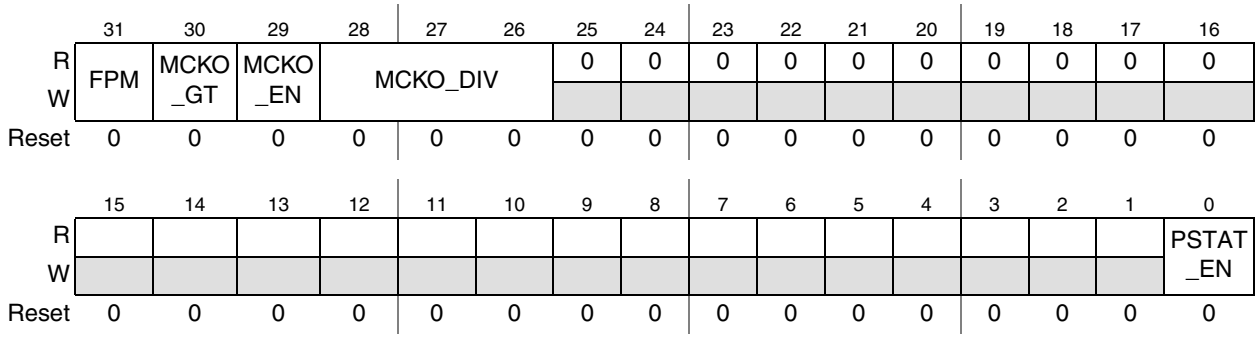


Figure 25-4. Port Configuration Register (PCR)

Table 25-11. PCR Field Descriptions

Field	Description
31 FPM	Full port mode. Determines if the auxiliary output port uses the full MDO port or a reduced MDO port to transmit messages. 0 The subset of MDO[3:0] pins are used to transmit messages. 1 All MDO[11:0] pins are used to transmit messages. Section 6.3.1.48, "Pad Configuration Register 82–75 (SIU_PCR82–SIU_PCR75)" shows how GPIO is enabled or disabled by the FPM setting.
30 MCKO_GT	MCKO clock gating control. Enables or disables MCKO clock gating. If clock gating is enabled, the MCKO clock is gated when the NPC is in enabled mode but not actively transmitting messages on the auxiliary output port. When clock gating is disabled, MCKO is allowed to run even if no auxiliary output port messages are being transmitted. 0 MCKO gating is disabled. 1 MCKO gating is enabled.
29 MCKO_EN	MCKO enable. Enables the MCKO clock. When enabled, the frequency of MCKO is determined by the MCKO_DIV field. 0 MCKO clock is driven to zero. 1 MCKO clock is enabled.
28–26 MCKO_DIV [2:0]	MCKO division factor. Determines the frequency of MCKO relative to the system clock frequency when MCKO_EN is asserted. The table below shows the meaning of MCKO_DIV values. In this table, SYS_CLK represents the system clock frequency.

MCKO_DIV[2:0]	MCKO Frequency
0	SYS_CLK
1	SYS_CLK / 2
2	Reserved
3	SYS_CLK / 4
4	Reserved
5	Reserved
6	Reserved
7	SYS_CLK / 8

Table 25-11. PCR Field Descriptions (continued)

Field	Description
25–1	Reserved
0 PSTAT_EN	Processor status mode enable. Enables processor status (PSTAT) mode. In PSTAT mode, all auxiliary output port MDO pins are used to transmit processor status information, and Nexus messaging is unavailable. 0 PSTAT mode disabled 1 PSTAT mode enabled **Note:** PSTAT mode is intended for factory processor debug only. The PSTAT_EN bit should be written to disable PSTAT mode by the customer. No Nexus messages are transmitted under any circumstances when PSTAT mode is enabled

25.7 NPC Functional Description

25.7.1 NPC Reset Configuration

The NPC is placed in disabled mode upon exit of reset. If message transmission via the auxiliary port is desired, a write to the PCR is then required to enable the NPC and select the mode of operation. Asserting MCKO_EN places the NPC in enabled mode and enables MCKO. The frequency of MCKO is selected by writing the MCKO_DIV field. Asserting or negating the FPM bit selects full-port or reduced-port mode, respectively.

Table 25-12 describes the NPC reset configuration options.

Table 25-12. NPC Reset Configuration Options

JCOMP Asserted?	PCR[MCKO_EN]	PCR[FPM]	Configuration
No	X	X	Reset
Yes	0	X	Disabled
Yes	1	1	Full-Port Mode
Yes	1	0	Reduced-Port Mode

25.7.2 Auxiliary Output Port

The auxiliary output port is shared by each of the Nexus modules on the device. The NPC communicates with each of the individual modules and arbitrates for access to the port. Additional information about the auxiliary port is found in Section 25.2, “External Signal Description.”

25.7.2.1 Output Message Protocol

The protocol for transmitting messages via the auxiliary port is accomplished with the $\overline{\text{MSEO}}$ functions. The $\overline{\text{MSEO}}$ pins are used to signal the end of variable-length packets and the end of messages. They are not required to indicate the end of fixed-length packets. MDO and $\overline{\text{MSEO}}$ are sampled on the rising edge of MCKO.

Figure 25-5 illustrates the state diagram for $\overline{\text{MSEO}}$ transfers. All transitions not included in the figure are reserved, and must not be used.

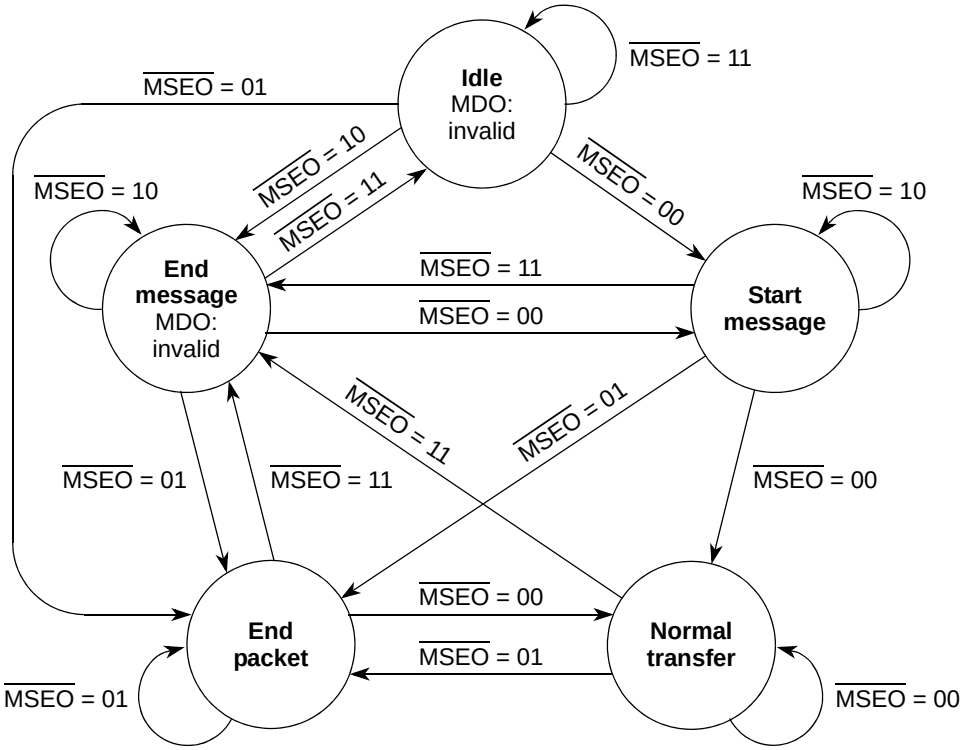


Figure 25-5. $\overline{\text{MSEO}}$ Transfers

25.7.2.2 Output Messages

In addition to sending out messages generated in other Nexus modules, the NPC can also output the device ID message contained in the device ID register on the MDO pins. The device ID message can also be sent out serially through TDO.

Table 25-13 describes the device ID message that the NPC can transmit on the auxiliary port. The TCODE is the first packet transmitted.

Table 25-13. NPC Output Messages

Message Name	Min. Packet Bits	Max Packet Bits	Packet Type	Packet Name	Packet Description
Device ID Message	6	6	Fixed	TCODE	Value = 1
	32	32	Fixed	ID	DID register contents

Figure 25-6 shows the various message formats that the pin interface formatter has to encounter.

Message	TCODE	Field #1	Field #2	Field #3	Field #4	Field #5	Min. Size[1] Bits	Max. Size[2] Bits
Device ID Message	1	Fixed = 32	N/A	N/A	N/A	N/A	38	38

[1] Minimum information size. The actual number of bits transmitted depends on the number of MDO pins

[2] Maximum information size. The actual number of bits transmitted depends on the number of MDO pins

Figure 25-6. Message Field Sizes

The double edges in Figure 25-6 indicate the starts and ends of messages. Fields without shaded areas between them are grouped into super-fields and can be transmitted together without end-of-packet indications between them.

25.7.2.2.1 Rules of Messages

The rules of messages include the following:

- A variable-sized field within a message must end on a port boundary. (Port boundaries depend on the number of MDO pins active with the current reset configuration.)
- A variable-sized field may start within a port boundary only when following a fixed-length field.
- Super-fields must end on a port boundary.
- When a variable-length field is sized such that it does not end on a port boundary, it is necessary to extend and zero fill the remaining bits after the highest order bit so that it can end on a port boundary.
- Multiple fixed-length packets may start and/or end on a single clock.
- When any packet follows a variable-length packet, it must start on a port boundary.
- The field containing the TCODE number is always transferred out first, followed by subsequent fields of information.
- Within a field, the lowest significant bits are shifted out first. Figure 25-7 shows the transmission sequence of a message that is made up of a TCODE followed by three fields.

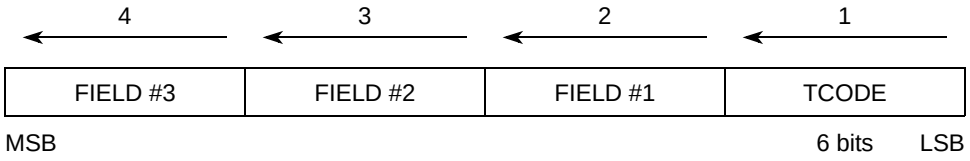


Figure 25-7. Transmission Sequence of Messages

25.7.2.3 IEEE® 1149.1-2001 (JTAG) TAP

The NPC uses the IEEE® 1149.1-2001 TAP for accessing registers. Each of the individual Nexus modules on the device implements a TAP controller for accessing its registers as well. TAP signals include TCK, TDI, TMS, and TDO. Detailed information about the TAP controller state machine may be found in Section 24.4.3, “TAP Controller State Machine.”

The IEEE® 1149.1-2001 specification may be ordered for further detail on electrical and pin protocol compliance requirements.

The NPC implements a Nexus controller state machine that transitions based on the state of the IEEE® 1149.1-2001 state machine shown in Figure 25-5. The Nexus controller state machine is defined by the IEEE-ISTO 5001-2003 standard. It is shown in Figure 25-10.

The instructions implemented by the NPC TAP controller are listed in Table 25-14. The value of the NEXUS-ENABLE instruction is 0b0000. Each unimplemented instruction acts like the BYPASS instruction. The size of the NPC instruction register is 4-bits.

Table 25-14. Implemented Instructions

Instruction Name	Private/Public	Opcode	Description
NEXUS-ENABLE	Public	0x0	Activate Nexus controller state machine to read and write NPC registers.
BYPASS	Private	0xF	NPC BYPASS instruction. Also the value loaded into the NPC IR upon exit of reset.

Data is shifted between TDI and TDO starting with the least significant bit as illustrated in Figure 25-8. This applies for the instruction register and all Nexus tool-mapped registers.

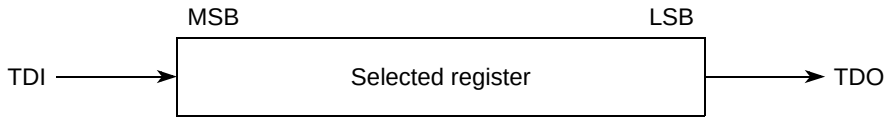
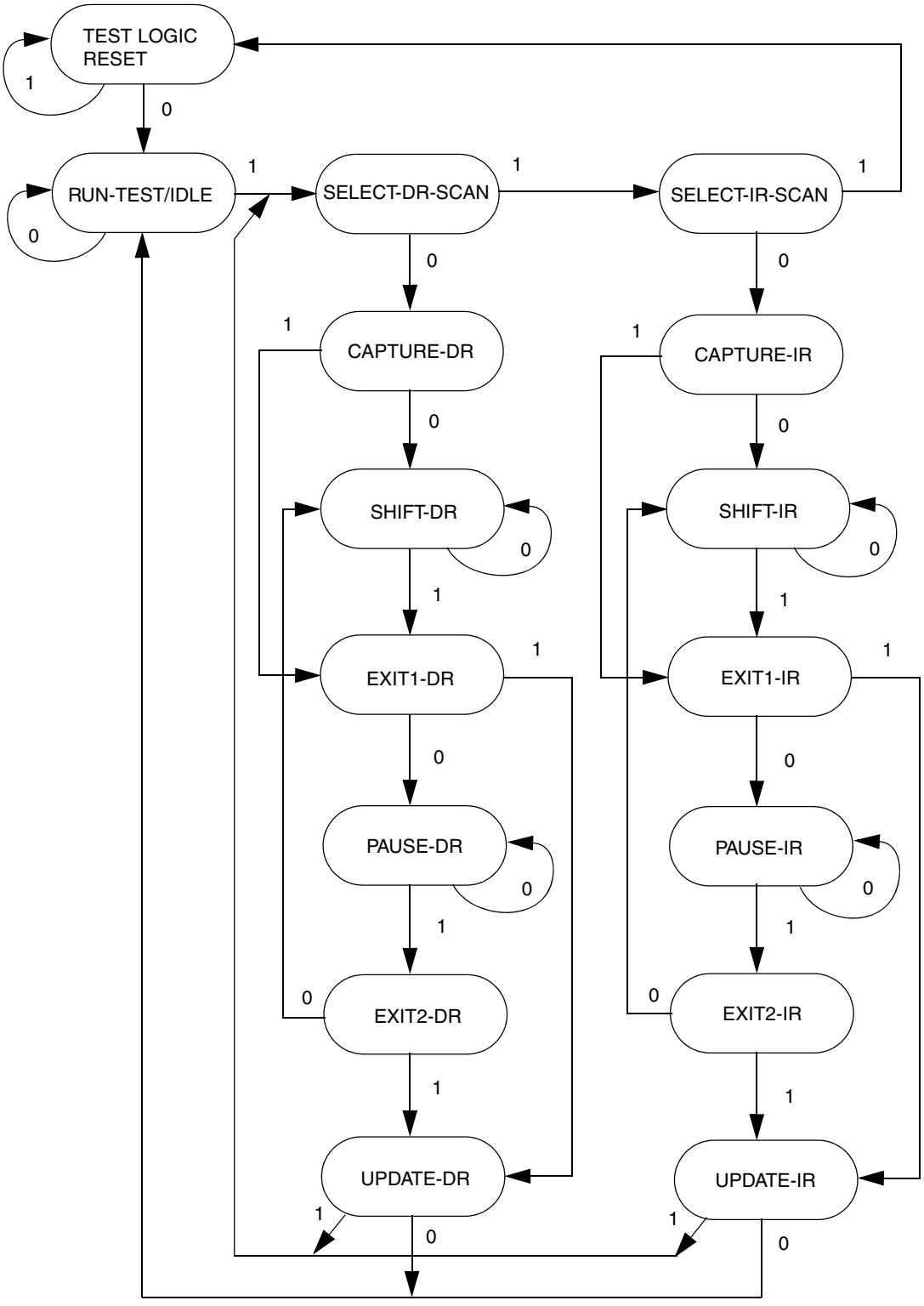


Figure 25-8. Shifting Data Into a Register

25.7.2.3.1 Enabling the NPC TAP Controller

Assertion of the power-on reset signal, entry into censored mode, or negating JCOMP resets the NPC TAP controller. When not in power-on reset or censored mode, the NPC TAP controller is enabled by asserting JCOMP and loading the ACCESS_AUX_TAP_NPC instruction in the JTAGC. Loading the NEXUS-ENABLE instruction then grants access to NPC registers.



NOTE: The value shown adjacent to each state transition in this figure represents the value of TMS at the time of a rising edge of TCK.

Figure 25-9. IEEE 1149.1-2001 TAP Controller State Machine

25.7.2.3.2 Retrieving Device IDCODE

The Nexus TAP controller does not implement the IDCODE instruction. However, the device identification message can be output by the NPC through the auxiliary output port or shifted out serially by accessing the NPC device ID register through the TAP. If the NPC is enabled, transmission of the device identification message on the auxiliary output port MDO pins occurs immediately after a write to the PCR. Transmission of the device identification message serially through TDO is achieved by performing a read of the register contents as described in Section 25.7.2.3.4, "Selecting a Nexus Client Register."

25.7.2.3.3 Loading NEXUS-ENABLE Instruction

Access to the NPC registers is enabled by loading the NPC NEXUS-ENABLE instruction when NPC has ownership of the TAP. This instruction is shifted in via the SELECT-IR-SCAN path and loaded in the UPDATE-IR state. At this point, the Nexus controller state machine, shown in Figure 25-10, transitions to the REG_SELECT state. The Nexus controller has three states: idle, register select, and data access. Table 25-15 illustrates the IEEE® 1149.1 sequence to load the NEXUS-ENABLE instruction.

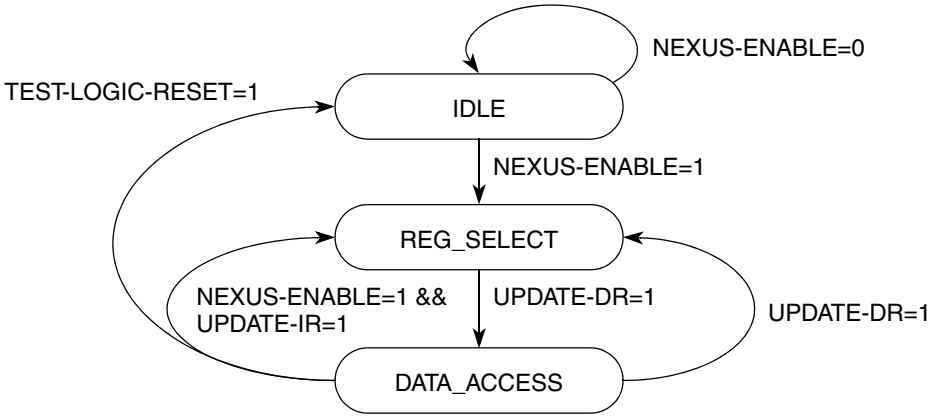


Figure 25-10. NEXUS Controller State Machine

Table 25-15. Loading NEXUS-ENABLE Instruction

Clock	TDI	TMS	IEEE® 1149.1 State	Nexus State	Description
0	—	0	RUN-TEST/IDLE	IDLE	IEEE 1149.1-2001 TAP controller in idle state
1	—	1	SELECT-DR-SCAN	IDLE	Transitional state
2	—	1	SELECT-IR-SCAN	IDLE	Transitional state
3	—	0	CAPTURE-IR	IDLE	Internal shifter loaded with current instruction
4	—	0	SHIFT-IR	IDLE	TDO becomes active, and the IEEE® 1149.1-2001 shifter is ready. Shift in all but the last bit of the NEXUS_ENABLE instruction.
5–7	0	0	3 TCKS in SHIFT-IR	IDLE	
8	0	1	EXIT1-IR	IDLE	Last bit of instruction shifted in
9	—	1	UPDATE-IR	IDLE	NEXUS-ENABLE loaded into instruction register
10	—	0	RUN-TEST/IDLE	REG_SELECT	Ready to be read/write Nexus registers

25.7.2.3.4 Selecting a Nexus Client Register

When the NEXUS-ENABLE instruction is decoded by the TAP controller, the input port allows development tool access to all Nexus registers. Each register has a 7-bit address index.

All register access is performed via the SELECT-DR-SCAN path of the IEEE® 1149.1–2001 TAP controller state machine. The Nexus controller defaults to the REG_SELECT state when enabled. Accessing a register requires two passes through the SELECT-DR-SCAN path: one pass to select the register and the second pass to read/write the register.

The first pass through the SELECT-DR-SCAN path is used to enter an 8-bit Nexus command consisting of a read/write control bit in the lsb followed by a 7-bit register address index, as illustrated in Figure 25-11. The read/write control bit is set to 1 for writes and 0 for reads.

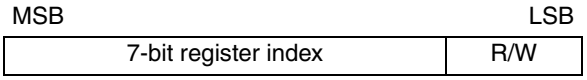


Figure 25-11. IEEE® 1149.1 Controller Command Input

The second pass through the SELECT-DR-SCAN path is used to read or write the register data by shifting in the data (lsb first) during the SHIFT-DR state. When reading a register, the register value is loaded into the IEEE® 1149.1-2001 shifter during the CAPTURE-DR state. When writing a register, the value is loaded from the IEEE® 1149.1-2001 shifter to the register during the UPDATE-DR state. When reading a register, there is no requirement to shift out the entire register contents. Shifting may be terminated after the required number of bits have been acquired.

Table 25-16 illustrates a sequence that writes a 32-bit value to a register.

Table 25-16. Write to a 32-Bit Nexus Client Register

Clock	TMS	IEEE 1149.1 State	Nexus State	Description
0	0	RUN-TEST/IDLE	REG_SELECT	IEEE 1149.1-2001 TAP controller in idle state
1	1	SELECT-DR-SCAN	REG_SELECT	First pass through SELECT-DR-SCAN path
2	0	CAPTURE-DR	REG_SELECT	Internal shifter loaded with current value of controller command input.
3	0	SHIFT-DR	REG_SELECT	TDO becomes active, and write bit and 6 bits of register index shifted in.
7 TCKs				
11	1	EXIT1-DR	REG_SELECT	Last bit of register index shifted into TDI
12	1	UPDATE-DR	REG_SELECT	Controller decodes and selects register
13	1	SELECT-DR-SCAN	DATA_ACCESS	Second pass through SELECT-DR-SCAN path
14	0	CAPTURE-DR	DATA_ACCESS	Internal shifter loaded with current value of register
15	0	SHIFT-DR	DATA_ACCESS	TDO becomes active, and outputs current value of register while new value is shifted in through TDI
31 TCKs				
47	1	EXIT1-DR	DATA_ACCESS	Last bit of current value shifted out TDO. Last bit of new value shifted in TDI.

Table 25-16. Write to a 32-Bit Nexus Client Register (continued)

Clock	TMS	IEEE 1149.1 State	Nexus State	Description
48	1	UPDATE-DR	DATA_ACCESS	Value written to register
49	0	RUN-TEST/IDLE	REG_SELECT	Controller returned to idle state. It could also return to SELECT-DR-SCAN to write another register.

25.7.2.4 Nexus Auxiliary Port Sharing

Each of the Nexus modules on the MCU implements a request/grant scheme to arbitrate for control of the Nexus auxiliary port when Nexus data is ready to be transmitted.

All modules arbitrating for the port are given fixed priority levels relative to each other. If multiple modules have the same request level, this priority level is used as a tie-breaker. To avoid monopolization of the port, the module given the highest priority level alternates following each grant. Immediately out of reset the order of priority, from highest to lowest, is: NPC, NZ6C3, NDEDI, NXDM. This arbitration mechanism is controlled internally and is not programmable by tools or the user.

25.7.2.5 Nexus JTAG Port Sharing

Each of the individual Nexus modules on the device implements a TAP controller for accessing its registers. When JCOMP is asserted, only the module whose ACCESS_AUX_TAP instruction is loaded has control of the TAP (Refer to Section 24.4.4, “JTAGC Instructions”). This allows the interface to all of these individual TAP controllers to appear to be a single port from outside the device. After a Nexus module has ownership of the TAP, that module acts like a single-bit shift register, or bypass register, if no register is selected as the shift path.

25.7.2.6 MCKO

MCKO is an output clock to the development tools used for the timing of $\overline{\text{MSEO}}$ and MDO pin functions. MCKO is derived from the system clock and its frequency is determined by the value of the MCKO_DIV[2:0] field in the PCR. Possible operating frequencies include one-half, one-quarter, and one-eighth system clock speed. MCKO is enabled by setting the MCKO_EN bit in the PCR.

The NPC also controls dynamic MCKO clock gating when in full- or reduced-port modes. The setting of the MCKO_GT bit inside the PCR determines whether or not MCKO gating control is enabled. The MCKO_GT bit resets to a logic 0. In this state gating of MCKO is disabled. To enable gating of MCKO, the MCKO_GT bit in the PCR is written to a logic 1. When MCKO gating is enabled, MCKO is driven to a logic 0 if the auxiliary port is enabled but not transmitting messages and there are no pending messages from Nexus clients.

25.7.2.7 $\overline{\text{EVTO}}$ Sharing

The NPC controls sharing of the $\overline{\text{EVTO}}$ output between all Nexus clients that produce an $\overline{\text{EVTO}}$ signal. $\overline{\text{EVTO}}$ is driven for one MCKO period whenever any module drives its $\overline{\text{EVTO}}$. When there is no active MCKO, such as in disabled mode, the NPC assumes an MCKO frequency of one-half system clock speed when driving $\overline{\text{EVTO}}$. $\overline{\text{EVTO}}$ sharing is active as long as the NPC is not in reset.

25.7.2.8 Nexus Reset Control

The JCOMP input that is used as the primary reset signal for the NPC is also used by the NPC to generate a single-bit reset signal for other Nexus modules. If JCOMP is negated, an internal reset signal is asserted, indicating that all Nexus modules should be held in reset. This internal reset signal is also asserted during a power-on reset, or if nex_disable is asserted (SIU_CCR[DISNEX]), indicating the device is in censored mode. This single bit reset signal functions much like the IEEE® 1149.1-2001 defined $\overline{\text{TRST}}$ signal and allows JCOMP reset information to be provided to the Nexus modules without each module having to sense the JCOMP signal directly or monitor the status of censored mode.

25.8 NPC Initialization/Application Information

25.8.1 Accessing NPC Tool-Mapped Registers

To initialize the TAP for NPC register accesses, the following sequence is required:

1. Enable the NPC TAP controller. This is achieved by asserting JCOMP and loading the ACCESS_AUX_TAP_NPC instruction in the JTAGC.
2. Load the TAP controller with the NEXUS-ENABLE instruction.

To write control data to NPC tool-mapped registers, the following sequence is required:

1. Write the 7-bit register index and set the write bit to select the register with a pass through the SELECT-DR-SCAN path in the TAP controller state machine.
2. Write the register value with a second pass through the SELECT-DR-SCAN path. Note that the prior value of this register is shifted out during the write.

To read status and control data from NPC tool-mapped registers, the following sequence is required:

1. Write the 7-bit register index and clear the write bit to select register with a pass through SELECT-DR-SCAN path in the TAP controller state machine.
2. Read the register value with a second pass through the SELECT-DR-SCAN path. Data shifted in is ignored.

Refer to the IEEE®-ISTO 5001-2003 standard for more detail.

25.9 Nexus Dual eTPU Development Interface (NDEDI)

The enhanced timing processor unit (eTPU) has its own Nexus class 3 interface, the Nexus dual eTPU development interface (NDEDI). The two eTPU engines and a coherent dual parameter controller (CDC) appear as three separate Nexus clients. Refer to the *Enhanced Time Processor Unit Reference Manual* for more information about the NDEDI module.

Reg Index: 0 Access: R/O

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	PRN				DC						PIN					
W																
Reset	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PIN				MIC											1
W																
Reset	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1

Figure 25-12. NDEDI Device ID Register (DID)

Table 25-17. NDEDI DID Register Field Descriptions

Field	Description
31–28 PRN	Part revision number. Contains the revision number of the part. This field changes with each revision of the device or module.
27–22 DC	Design center. Indicates the Freescale design center. This value is 0x20.
21–12 PIN	Part identification number. Contains the part number of the device. The PIN for the MPC5566 is 0x224.
11–1 MIC	Manufacturer identity code. Contains the reduced Joint Electron Device Engineering Council (JEDEC) ID for Freescale, 0xE.
0	Fixed per JTAG 1149.1 1 Always set

25.10 e200z6 Class 3 Nexus Module (NZ6C3)

The NZ6C3 module provides real-time development capabilities for the device core in compliance with the IEEE®-ISTO Nexus 5001-2003 standard. This module provides development support capabilities without requiring the use of address and data pins for internal visibility.

25.10.1 Introduction

This section defines the auxiliary pin functions, transfer protocols and standard development features of the NZ6C3 module. The development features supported are Program trace, data trace, watchpoint messaging, ownership trace, and read/write access via the JTAG interface.

NOTE

Throughout this section references are made to the auxiliary port and its specific signals, such as MCKO, $\overline{\text{MSEO}}$[0:1], MDO[11:0] and others. The device NPC module arbitrates the access of the single auxiliary port. To simplify the description of the function of the NZ6C3 module, the interaction of the NPC is omitted and the configuration in this chapter describes an NPC with a dedicated auxiliary port. The auxiliary port is fully described in Section 25.2, "External Signal Description."

25.10.2 Block Diagram

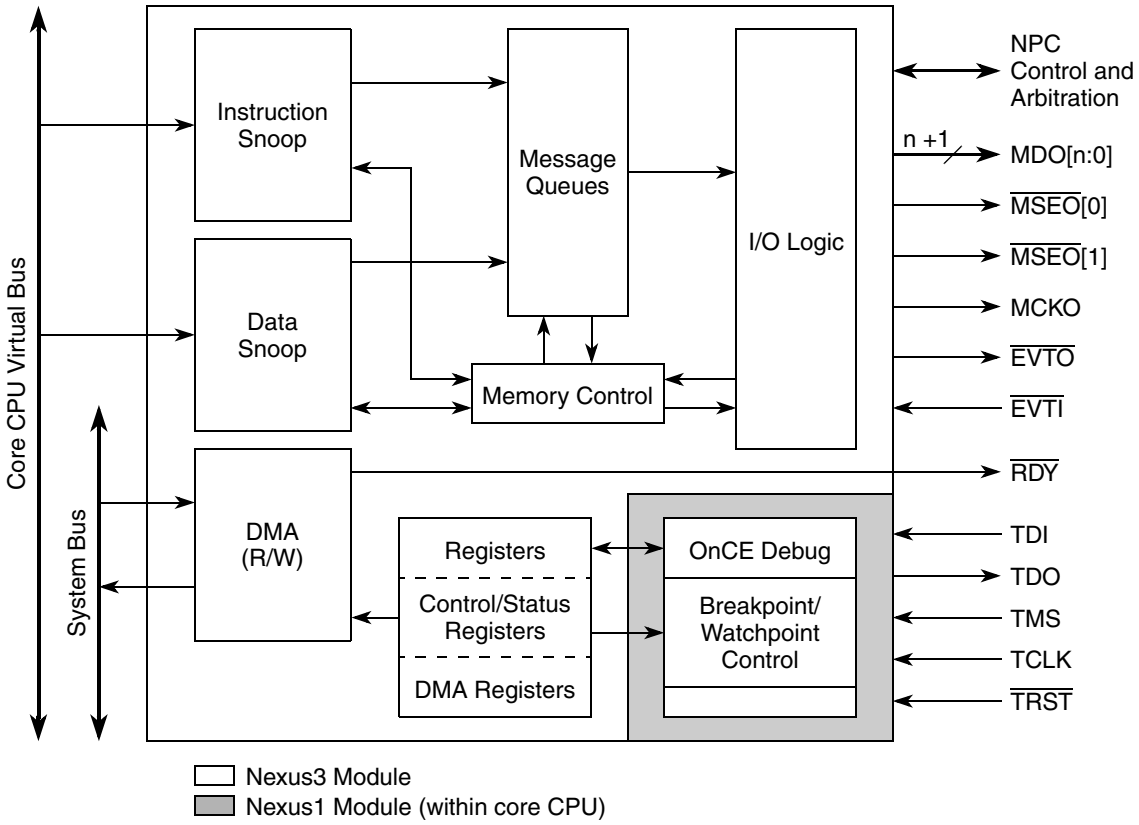


Figure 25-13. e200z6 Nexus3 Functional Block Diagram

25.10.3 Overview

Table 25-18 contains a set of terms and definitions associated with the NZ6C3 module.

Table 25-18. Terms and Definitions

Term	Description
IEEE®-ISTO 5001	Consortium and standard for real-time embedded system design. World wide Web documentation at http://www.ieee-isto.org/Nexus5001
Auxiliary Port	Refers to Nexus auxiliary port. Used as auxiliary port to the IEEE® 1149.1 JTAG interface.
Branch Trace Messaging (BTM)	Visibility of addresses for taken branches and exceptions, and the number of sequential instructions executed between each taken branch.
Client	A functional block on an embedded processor which requires development visibility and controllability. Examples are a central processing unit (CPU) or an intelligent peripheral.
Data Read Message (DRM)	External visibility of data reads to memory-mapped resources.
Data Write Message (DWM)	External visibility of data writes to memory-mapped resources.
Data Trace Messaging (DTM)	External visibility of how data flows through the embedded system. This may include DRM and/or DWM.
JTAG Compliant	Device complying to IEEE® 1149.1 JTAG standard
JTAG IR & DR Sequence	JTAG instruction register (IR) scan to load an opcode value for selecting a development register. The JTAG IR corresponds to the OnCE command register (OCMD). The selected development register is then accessed via a JTAG data register (DR) scan.
Nexus1	The e200z6 (OnCE) debug module. This module integrated with each e200z6 processor provides all static (core halted) debug functionality. This module is compliant with Class1 of the IEEE®-ISTO 5001 standard.
Ownership Trace Message (OTM)	Visibility of process/function that is currently executing.
Public Messages	Messages on the auxiliary pins for accomplishing common visibility and controllability requirements
Standard	The phrase ‘according to the standard’ is used to indicate according to the IEEE®-ISTO 5001 standard.
Transfer Code (TCODE)	Message header that identifies the number and/or size of packets to be transferred, and how to interpret each of the packets.
Watchpoint	A data or instruction breakpoint which does not cause the processor to halt. Instead, a pin is used to signal that the condition occurred. A watchpoint message is also generated.

25.10.4 Features

The NZ6C3 module is compliant with Class 3 of the IEEE®-ISTO 5001-2003 standard. The following features are implemented:

- Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct and indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus static code may be traced.

- Data trace via data write messaging (DWM) and data read messaging (DRM). This provides the capability for the development tool to trace reads and/or writes to selected internal memory resources.
- Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An ownership trace message is transmitted when a new process/task is activated, allowing the development tool to trace ownership flow.
- Run-time access to embedded processor registers and memory map via the JTAG port. This allows for enhanced download/upload capabilities.
- Watchpoint messaging via the auxiliary pins.
- Watchpoint trigger enable of program and/or data trace messaging.
- High-speed data input/output via the auxiliary port.
- Auxiliary interface for higher data input/output
  - Configurable (minimum and maximum) message data out pins (**nex_mdo[n:0]**)
  - One or two message start/end out pins (**nex_mseo_b[1:0]**)
  - One read/write ready pin (**nex_rdy_b**) pin
  - One watchpoint-event pin (**nex_evto_b**)
  - One event-in pin (**nex_evti_b**)
  - One MCKO (message clock out) pin
- Registers for program trace, data trace, ownership trace and watchpoint trigger.
- All features controllable and configurable via the JTAG port.

25.10.5 Enabling Nexus3 Operation

The Nexus module is enabled by loading a single instruction (ACCESS_AUX_TAP_ONCE, as shown in Table 25-4) into the JTAGC instruction register (IR), and then loading the corresponding OnCE OCMD register with the NEXUS3_ACCESS instruction (refer to Table 25-5). For the e200z6 Class 3 Nexus module, the OCMD value is 0b00_0111_1100. After it is enabled, the module is ready to accept control input via the JTAG pins.

Refer to Section 25.7, “NPC Functional Description” for more information.

The Nexus module is disabled when the JTAG state machine reaches the test-logic-reset state. This state can be reached by asserting the JCOMP pin or cycling through the state machine using the TMS pin. The Nexus module is also disabled if a power-on-reset (POR) event occurs. If the Nexus3 module is disabled, no trace output is provided, and the module disables (drive inactive) auxiliary port output pins MDO[n:0], $\overline{\text{MSEO}}$[1:0], MCKO. Nexus registers are not available for reads or writes.

25.10.6 TCODEs Supported by NZ6C3

The Nexus3 pins allow for flexible transfer operations via public messages. A TCODE defines the transfer format, the number and/or size of the packets to be transferred, and the purpose of each packet. The IEEE®-ISTO 5001-2003 standard defines a set of public messages. The NZ6C3 module supports the public TCODEs seen in Table 25-19. Each message contains multiple packets transmitted in the order shown in the table.

Table 25-19. Public TCODEs Supported by NZ6C3

Message Name	Packet Size (bits)		Packet Name	Packet Type	Packet Description
	Min	Max			
Debug Status	6	6	TCODE	Fixed	TCODE number = 0 (0x00)
	4	4	SRC	Fixed	Source processor identifier
	8	8	STATUS	Fixed	Debug status register (DS[31:24])
Ownership Trace Message	6	6	TCODE	Fixed	TCODE number = 2 (0x02)
	4	4	SRC	Fixed	Source processor identifier
	32	32	PROCESS	Fixed	Task/Process ID tag
Program Trace - Direct Branch Message[1]	6	6	TCODE	Fixed	TCODE number = 3 (0x03)
	4	4	SRC	Fixed	Source processor identifier
	1	8	I-CNT	Variable	Number of sequential instructions executed since last taken branch
Program Trace - Indirect Branch Message[1]	6	6	TCODE	Fixed	TCODE number = 4 (0x04)
	4	4	SRC	Fixed	Source processor identifier
	1	8	I-CNT	Variable	Number of sequential instructions executed since last taken branch
	1	32	U-ADDR	Variable	Unique part of target address for taken branches/exceptions
Data Trace - Data Write Message	6	6	TCODE	Fixed	TCODE number = 5 (0x05)
	4	4	SRC	Fixed	Source processor identifier
	3	3	DSIZ	Fixed	Data size (refer to Table 25-23)
	1	32	U-ADDR	Variable	Unique portion of the data write address
	1	64	DATA	Variable	Data write values (refer to Section 25.14.6, “Data Trace,” for details)

Table 25-19. Public TCODEs Supported by NZ6C3 (continued)

Message Name	Packet Size (bits)		Packet Name	Packet Type	Packet Description
	Min	Max			
Data Trace - Data Read Message	6	6	TCODE	Fixed	TCODE number = 6 (0x06)
	4	4	SRC	Fixed	Source processor identifier
	3	3	DSIZ	Fixed	Data size (refer to Table 25-23)
	1	32	U-ADDR	Variable	Unique portion of the data read address
	1	64	DATA	Variable	Data read values (refer to Section 25.14.6, "Data Trace," for details)
Error Message	6	6	TCODE	Fixed	TCODE number = 8 (0x08)
	4	4	SRC	Fixed	Source processor identifier
	5	5	ECODE	Fixed	Error code
Program Trace - Direct Branch Message w/ Sync[1]	6	6	TCODE	Fixed	TCODE number = 11 (0x0B)
	4	4	SRC	Fixed	Source processor identifier
	1	8	I-CNT	Variable	Number of sequential instructions executed since last taken branch
	1	32	F-ADDR	Variable	Full target address (leading zeros truncated)
Program Trace - Indirect Branch Message w/ Sync[1]	6	6	TCODE	Fixed	TCODE number = 12 (0x0C)
	4	4	SRC	Fixed	Source processor identifier
	1	8	I-CNT	Variable	Number of sequential instructions executed since last taken branch
	1	32	F-ADDR	Variable	Full target address (leading zeros truncated)
Data Trace - Data Write Message w/ Sync	6	6	TCODE	Fixed	TCODE number = 13 (0x0D)
	4	4	SRC	Fixed	Source processor identifier
	3	3	DSZ	Fixed	Data size (refer to Table 25-23)
	1	32	F-ADDR	Variable	Full access address (leading zeros truncated)
	1	64	DATA	Variable	Data write values (refer to Section 25.14.6, "Data Trace," for details)
Data Trace - Data Read Message w/ Sync	6	6	TCODE	Fixed	TCODE number = 14 (0x0E)
	4	4	SRC	Fixed	Source processor identifier
	3	3	DSZ	Fixed	Data size (refer to Table 25-23)
	1	32	F-ADDR	Variable	Full access address (leading zeros truncated)
	1	64	DATA	Variable	Data read values (refer to Section 25.14.6, "Data Trace," for details)

Table 25-19. Public TCODEs Supported by NZ6C3 (continued)

Message Name	Packet Size (bits)		Packet Name	Packet Type	Packet Description
	Min	Max			
Watchpoint Message	6	6	TCODE	Fixed	TCODE number = 15 (0x0F)
	4	4	SRC	Fixed	Source processor identifier
	4	4	WPHIT	Fixed	Number indicating watchpoint sources
Resource Full Message	6	6	TCODE	Fixed	TCODE number = 27 (0x1B)
	4	4	SRC	Fixed	Source processor identifier
	4	4	RCODE	Fixed	Resource code (Refer to RCODE values in Table 25-22) - indicates which resource is the cause of this message
	1	32	RDATA	Variable	Branch / predicate instruction history (refer to Section 25.13.1, “Branch Trace Messaging (BTM)”)
Program Trace - Indirect Branch History Message	6	6	TCODE	Fixed	TCODE number = 28 (0x1C) (refer to footnote 1 below)
	4	4	SRC	Fixed	Source processor identifier
	1	8	I-CNT	Variable	Number of sequential instructions executed since last taken branch
	1	32	U-ADDR	Variable	Unique part of target address for taken branches/exceptions
	1	32	HIST	Variable	Branch / predicate instruction history (refer to Section 25.13.1, “Branch Trace Messaging (BTM)”)
Program Trace - Indirect Branch History Message w/ Sync	6	6	TCODE	Fixed	TCODE number = 29 (0x1D) (refer to footnote 1 below)
	4	4	SRC	Fixed	Source processor identifier
	1	8	I-CNT	Variable	Number of sequential instructions executed since last taken branch
	1	32	F-ADDR	Variable	Full target address (leading zero (0) truncated)
	1	32	HIST	Variable	Branch / predicate instruction history (refer to Section 25.13.1, “Branch Trace Messaging (BTM)”)

Table 25-19. Public TCODEs Supported by NZ6C3 (continued)

Message Name	Packet Size (bits)		Packet Name	Packet Type	Packet Description
	Min	Max			
Program Trace - Program Correlation Message	6	6	TCODE	Fixed	TCODE number = 33 (0x21)
	4	4	SRC	Fixed	Source processor identifier
	4	4	EVCODE	Fixed	Event correlated w/ program flow (refer to Table 25-22)
	1	8	I-CNT	Variable	Number of sequential instructions executed since last taken branch
	1	32	HIST	Variable	Branch / predicate instruction history (refer to Section 25.13.1, “Branch Trace Messaging (BTM)”)

[1] You can select between the two types of program trace. The advantages for each are discussed in Section 25.13.1, “Branch Trace Messaging (BTM). If the branch history method is selected, the shaded TCODES above are not messaged out.

Table 25-20 shows the error code encodings used when reporting an error via the Nexus3 Error Message.

Table 25-20. Error Code Encoding (TCODE = 8)

Error Code (ECODE)	Description
00000	Ownership trace overrun
00001	Program trace overrun
00010	Data trace overrun
00011	Read/write access error
00101	Invalid access opcode (Nexus register unimplemented)
00110	Watchpoint overrun
00111	(Program trace or data trace) and ownership trace overrun
01000	(Program trace or data trace or ownership trace) and watchpoint overrun
01001–10111	Reserved
11000	BTM lost due to collision w/ higher priority message
11001–11111	Reserved

Table 25-21 shows the encodings used for resource codes for certain messages.

Table 25-21. RCODE values (TCODE = 27)

Resource Code (RCODE)	Description	Resource Data (RDATA)
0000	Program Trace Instruction Counter overflow (reached 255 and was reset)	0xFF
0001	Program Trace, Branch / Predicate Instruction History. This type of packet is terminated by a stop bit set to 1 after the last history bit.	Branch History. This type of packet is terminated by a stop bit set to a 1 after the last history bit.

Table 25-22 shows the event code encodings used for certain messages.

Table 25-22. Event Code Encoding (TCODE = 33)

Event Code	Description
0000	Entry into Debug Mode
0001	Entry into Low Power Mode (CPU only)[1]
0010–0011	Reserved for future functionality
0100	Disabling Program Trace
0101–1101	Reserved for future functionality
1110	Entry into a VLE page from a non-VLE page
1111	Entry into a non-VLE page from a VLE page

[1] The device enters Low Power Mode when the Nexus stall mode is enabled (NZ6C3_DC1[OVC]=0b011) and a trace message is in danger of over-flowing the Nexus queue.

Table 25-23 shows the data trace size encodings used for certain messages.

Table 25-23. Data Trace Size Encodings (TCODE = 5, 6, 13, 14)

DTM Size Encoding	Transfer Size
000	Byte
001	Halfword (two bytes)
010	Word (four bytes)
011	Doubleword (eight bytes)
100	String (three bytes)
101–111	Reserved

NOTE

Program trace can be implemented using either branch history/predicate instruction messages, or traditional direct and indirect branch messages. The user can select between the two types of Program Trace. The advantages for each are discussed in Section 25.13.1, “Branch Trace Messaging (BTM). If the Branch History method is selected, the shaded TCODES are not messaged out.

25.11 NZ6C3 Memory Map and Register Definition

This section describes the NZ6C3 programmer’s model. NZ6C3 registers are accessed using the JTAG/OnCE port in compliance with IEEE® 1149.1. Refer to Section 25.11.11, “ NZ6C3 Register Access via JTAG / OnCE” for details on NZ6C3 register access.

NOTE

NZ6C3 registers and output signals are numbered using bit 0 as the least significant bit. This bit ordering is consistent with the ordering defined by the IEEE®-ISTO 5001 standard.

Table 25-24 details the register map for the NZ6C3 module.

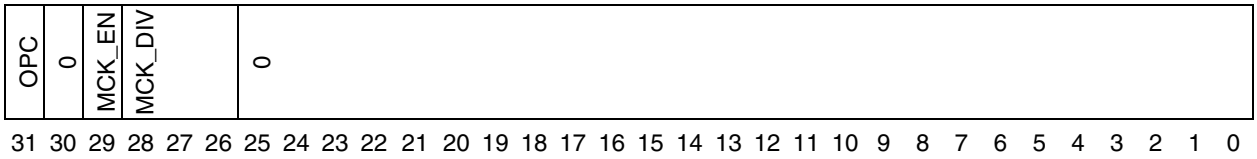
Table 25-24. NZ6C3 Memory Map

Access Opcode	Register Name	Register Description	Read Address	Write Address
0x0001	CSC	Client select control [1]	0x0002	—
Refer to NPC	PCR	Port configuration register [1]	—	—
0x0002	DC1	Development control 1	0x0004	0x0005
0x0003	DC2	Development control 2	0x0006	0x0007
0x0004	DS	Development status	0x0008	—
0x0007	RWCS	Read/write access control/status	0x000E	0x000F
0x0009	RWA	Read/write access address	0x0012	0x0013
0x000A	RWD	Read/write access data	0x0014	0x0015
0x000B	WT	Watchpoint trigger	0x0016	0x0017
0x000D	DTC	Data trace control	0x001A	0x001B
0x000E	DTSA1	Data trace start address 1	0x001C	0x001D
0x000F	DTSA2	Data trace start address 2	0x001E	0x001F
0x0012	DTEA1	Data trace end address 1	0x0024	0x0025
0x0013	DTEA2	Data trace end address 2	0x0026	0x0027
0x0014–0x003F	—	Reserved	0x0028–0x007E	0x0029–0x007F

[1] The CSC and PCR registers are shown in this table as part of the Nexus programmer’s model. They are only present at the top level Nexus3 controller (NPC), not in the NZ6C3 module. The device’s CSC register is readable through Nexus3, but the PCR is shown for reference only.

25.11.1 Port Configuration Register (PCR)

The Port Configuration Register (PCR) controls the basic port functions for all Nexus modules in a multi-Nexus environment. This includes clock control and auxiliary port width. All bits in this register are writable only once after system reset.



Nexus Reg# - PCR_INDEX; R/W; Reset - 0x0

Figure 25-14. Port Configuration Register

Table 25-25. Port Configuration Register Fields

PCR[31]	OPC	OPC — Output Port Mode Control 0 = Reduced Port Mode configuration (minimum # **nex_mdo[n:0]** pins) 1 = Full Port Mode configuration (max# **nex_mdo[n:0]** pins defined by SOC)
PCR[30]	—	Reserved for future functionality
PCR[29]	MCK_EN	MCK_EN — MCKO Clock enable 0 = **nex_mcko** is disabled 1 = **nex_mcko** is enabled
PCR[28:26]	MCK_DIV	MCK_DIV — MCKO Clock Divide Ratio (read note that follows this table) 000 = **nex_mcko** is 1x processor clock frequency. 001 = **nex_mcko** is 1/2x processor clock frequency. 010 = Reserved (defaults to 1/2x processor clock frequency.) 011 = **nex_mcko** is 1/4x processor clock frequency. 100–110 = Reserved (defaults to 1/2x processor clock frequency.) 111 = **nex_mcko** is 1/8x processor clock frequency.
PCR[25:0]	—	Reserved for future functionality

NOTE

The CSC and PCR registers are in separate system module for a multi-Nexus environment. If the e200z6 Nexus3 module is the only Nexus module, the CSC and PCR registers are not implemented, and the e200z6 Nexus3 development control register 1 (DC1) set the Nexus port functionality.

25.11.2 Development Control Registers 1 and 2 (DC1, DC2)

The development control registers are used to control the basic development features of the NZ6C3 module. Development control register 1 is shown in Figure 25-15 and its fields are described in Table 25-26.

Nexus Reg: 0x0002 Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	OPC	MCK_DIV		EOC		0	PTM	WEN	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R									OVC			EIC		TM		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-15. Development Control Register 1 (DC1)

Table 25-26. DC1 Field Descriptions

Field	Description
31 OPC[1]	Output port mode control. 0 Reduced-port mode configuration (four MDO pins) 1 Full-port mode configuration (12 MDO pins)
30–29 MCK_DIV [1:0][1]	MCKO clock divide ratio (refer to note below). 00 MCKO is 1x processor clock frequency. 01 MCKO is 1/2x processor clock frequency. 10 MCKO is 1/4x processor clock frequency. 11 MCKO is 1/8x processor clock frequency.
28–27 EOC[1:0]	$\overline{\text{EVTO}}$ control. 00 $\overline{\text{EVTO}}$ upon occurrence of watchpoints (configured in DC2) 01 $\overline{\text{EVTO}}$ upon entry into debug mode 10 $\overline{\text{EVTO}}$ upon time-stamping event 11 Reserved
26	Reserved
25 PTM	Program trace method. 0 Program trace uses traditional branch messages 1 Program trace uses branch history messages
24 WEN	Watchpoint trace enable. 0 Watchpoint Messaging disabled 1 Watchpoint Messaging enabled
23–8	Reserved
7–5 OVC[2:0]	Overrun control. 000 Generate overrun messages 001–010 Reserved 011 Delay processor for BTM / DTM / OTM overruns 1XX Reserved

Table 25-26. DC1 Field Descriptions (continued)

Field	Description
4–3 EIC[1:0]	EVTI control. 00 EVTI is used for synchronization (program trace/ data trace) 01 EVTI is used for debug request 1X Reserved
2–0 TM[2:0]	Trace mode. Any or all of the TM bits may set, enabling one or more traces. 000 No trace 1XX Program trace enabled X1X Data trace enabled XX1 Ownership trace enabled

[1] The output port mode control bit (OPC) and MCKO divide bits (MCK_DIV) are shown for clarity. These functions are controlled globally by the NPC port control register (PCR). These bits are writable in the PCR but have no effect.

Development control register 2 is shown in Figure 25-16 and its fields are described in Table 25-27.

Nexus Reg: 0x0003 Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	EWC								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-16. Development Control Register 2 (DC2)

Table 25-27. DC2 Field Descriptions

Field	Description
31–24 EWC[7:0]	$\overline{\text{EVTO}}$ watchpoint configuration. Any or all of the bits in EWC may be set to configure the $\overline{\text{EVTO}}$ watchpoint. 00000000No Watchpoints trigger $\overline{\text{EVTO}}$ 1XXXXXXXWatchpoint #0 (IAC1 from Nexus1) triggers $\overline{\text{EVTO}}$ X1XXXXXXWatchpoint #1 (IAC2 from Nexus1) triggers $\overline{\text{EVTO}}$ XX1XXXXXWatchpoint #2 (IAC3 from Nexus1) triggers $\overline{\text{EVTO}}$ XXX1XXXXWatchpoint #3 (IAC4 from Nexus1) triggers $\overline{\text{EVTO}}$ XXXX1XXXWatchpoint #4 (DAC1 from Nexus1) triggers $\overline{\text{EVTO}}$ XXXXX1XXWatchpoint #5 (DAC2 from Nexus1) triggers $\overline{\text{EVTO}}$ XXXXXX1XWatchpoint #6 (DCNT1 from Nexus1) triggers $\overline{\text{EVTO}}$ XXXXXXX1Watchpoint #7 (DCNT2 from Nexus1) triggers $\overline{\text{EVTO}}$
23–0	Reserved

NOTE

The EOC bits in DC1 must be programmed to trigger $\overline{\text{EVTO}}$ on watchpoint occurrence for the EWC bits to have any effect.

25.11.3 Development Status Register (DS)

The development status register is used to report system debug status. When debug mode is entered or exited, or an e200z6-defined low power mode is entered, a debug status message is transmitted with DS[31:24]. The external tool can read this register at any time.

Nexus Reg: 0x0004 Access: R/O

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	DBG	0	0	0	LPC		CHK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-17. Development Status Register (DS)

Table 25-28. DS Field Descriptions

Field	Description
31–28 DBG	Bit 31 is the e200z6 CPU debug mode transition status. Bits 31–28 are sent as the debug status message. 0 CPU not in debug mode 1 CPU in debug mode
27–26 LPC[1:0]	e200z6 CPU low power mode status. 00 Normal (run) mode 01 CPU in halted state 10 CPU in stopped state 11 Reserved
25 CHK	e200z6 CPU checkstop status. 0 CPU not in checkstop state 1 CPU in checkstop state
24–0	Reserved

25.11.4 Read/Write Access Control and Status (RWCS)

The read write access control/status register provides control for read/write access. Read/write access provides DMA-like access to memory-mapped resources on the system bus either while the processor is halted, or during runtime. The RWCS register also provides read/write access status information as shown in Table 25-30.

Nexus Reg: 0x0007 Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	AC	RW	SZ			MAP			PR		BST	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CNT														ERR	DV
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-18. Read/Write Access Control and Status Register (RWCS)

Table 25-29 describes the fields and functions in the read/write control and status (RWCS) register:

Table 25-29. RWCS Field Description

Field	Description
31 AC	Access control. 0 End access 1 Start access
30 RW	Read/write select. 0 Read access 1 Write access
29–27 SZ[2:0]	Word size. 000 8-bit (byte) 001 6-bit (halfword) 010 32-bit (word) 011 64-bit (doubleword - only in burst mode) 100–111 Reserved (default to word)
26–24 MAP[2:0]	MAP select. 000 Primary memory map 001–111 Reserved
23–22 PR[1:0]	Read/write access priority. 00 Lowest access priority 01 Reserved (default to lowest priority) 10 Reserved (default to lowest priority) 11 Highest access priority
21 BST	Burst control. 0 Module accesses are single bus cycle at a time. 1 Module accesses are performed as burst operation.
20–16	Reserved

Table 25-29. RWCS Field Description (continued)

Field	Description
15–2 CNT[13:0]	Access control count. Number of accesses of word size SZ
1 ERR	Read/write access error. Refer to Table 25-30.
0 DV	Read/write access data valid. Refer to Table 25-30.

Table 25-30 details the status bit encodings.

Table 25-30. Read/Write Access Status Bit Encoding

Read Action	Write Action	ERR	DV
Read access has not completed	Write access completed without error	0	0
Read access error has occurred	Write access error has occurred	1	0
Read access completed without error	Write access has not completed	0	1
Not allowed	Not allowed	1	1

25.11.5 Read/Write Access Address (RWA)

The read/write access address register provides the system bus address to be accessed when initiating a read or a write access.

Nexus Reg: 0x0009 Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Read/Write Address																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-19. Read/Write Access Address Register (RWA)

25.11.6 Read/Write Access Data (RWD)

The read/write access data register provides the data to/from system bus memory-mapped locations when initiating a read or a write access.

Nexus Reg: 0x000A Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Read/Write Data																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-20. Read/Write Access Data Register (RWD)

25.11.7 Watchpoint Trigger Register (WT)

The watchpoint trigger register allows the watchpoints defined within the e200z6 Nexus1 logic to trigger actions. These watchpoints can control program and/or data trace enable and disable. The WT bits can be used to produce an address related ‘window’ for triggering trace messages.

Nexus Reg: 0x000B — Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PTS				PTE				DTS				DTE				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-21. Watchpoint Trigger Register (WT)

Table 25-31 details the watchpoint trigger register fields.

Table 25-31. WT Field Descriptions

Field	Description
31–29 PTS[2:0]	Program trace start control. 000 Trigger disabled 001 Use watchpoint #0 (IAC1 from Nexus1) 010 Use watchpoint #1 (IAC2 from Nexus1) 011 Use watchpoint #2 (IAC3 from Nexus1) 100 Use watchpoint #3 (IAC4 from Nexus1) 101 Use watchpoint #4 (DAC1 from Nexus1) 110 Use watchpoint #5 (DAC2 from Nexus1) 111 Use watchpoint #6 or #7 (DCNT1 or DCNT2 from Nexus1)
28–26 PTE[2:0]	Program trace end control. 000 Trigger disabled 001 Use watchpoint #0 (IAC1 from Nexus1) 010 Use watchpoint #1 (IAC2 from Nexus1) 011 Use watchpoint #2 (IAC3 from Nexus1) 100 Use watchpoint #3 (IAC4 from Nexus1) 101 Use watchpoint #4 (DAC1 from Nexus1) 110 Use watchpoint #5 (DAC2 from Nexus1) 111 Use watchpoint #6 or #7 (DCNT1 or DCNT2 from Nexus1)
25–23 DTS[2:0]	Data trace start control. 000 Trigger disabled 001 Use watchpoint #0 (IAC1 from Nexus1) 010 Use watchpoint #1 (IAC2 from Nexus1) 011 Use watchpoint #2 (IAC3 from Nexus1) 100 Use watchpoint #3 (IAC4 from Nexus1) 101 Use watchpoint #4 (DAC1 from Nexus1) 110 Use watchpoint #5 (DAC2 from Nexus1) 111 Use watchpoint #6 or #7 (DCNT1 or DCNT2 from Nexus1)

Table 25-31. WT Field Descriptions (continued)

Field	Description
22–20 DTE[2:0]	Data trace end control. 000 Trigger disabled 001 Use watchpoint #0 (IAC1 from Nexus1) 010 Use watchpoint #1 (IAC2 from Nexus1) 011 Use watchpoint #2 (IAC3 from Nexus1) 100 Use watchpoint #3 (IAC4 from Nexus1) 101 Use watchpoint #4 (DAC1 from Nexus1) 110 Use watchpoint #5 (DAC2 from Nexus1) 111 Use watchpoint #6 or #7 (DCNT1 or DCNT2 from Nexus1)
19–0	Reserved

NOTE

The WT bits control program and data trace only if the TM bits in the development control register 1 (DC1) have not been set to enable program and data trace, respectively.

25.11.8 Data Trace Control Register (DTC)

The data trace control register controls whether DTM messages are restricted to reads, writes, or both for a user programmable address range. There are two data trace channels controlled by the DTC for the Nexus3 module. Each channel can also be programmed to trace data accesses or instruction accesses.

Nexus Reg: 0x000D — Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RWT1		RWT2										0	0	0	0	0	0	0	0	0	0	0	0	RC1	RC2	0	0	DI1	DI2	0	0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-22. Data Trace Control Register (DTC)

Table 25-32 details the data trace control register fields.

Table 25-32. DTC Field Description

Field	Description
31–30 RWT1[1:0]	Read/write trace 1. 00 No trace enabled X1 Enable data read trace 1X Enable data write trace
29–28 RWT2[1:0]	Read/write trace 2. 00 No trace enabled X1 Enable data read trace 1X Enable data write trace
27–8	Reserved

Table 25-32. DTC Field Description (continued)

Field	Description
7 RC1	Range control 1. 0 Condition trace on address within range 1 Condition trace on address outside of range
6 RC2	Range control 2 0 Condition trace on address within range 1 Condition trace on address outside of range
5–4	Reserved
3 DI1	Data access/instruction access trace 1. 0 Condition trace on data accesses 1 Condition trace on instruction accesses
2 DI2	Data access/instruction access trace 2 0 Condition trace on data accesses 1 Condition trace on instruction accesses
1–0	Reserved

25.11.9 Data Trace Start Address Registers 1 and 2 (DTSA*n*)

The data trace start address registers define the start addresses for each trace channel.

Nexus Reg: 0x000E Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Data Trace Start Address																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-23. Data Trace Start Address Register 1 (DTSA1)

Nexus Reg: 0x000F Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Data Trace Start Address																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-24. Data Trace Start Address Register 2 (DTSA2)

25.11.10 Data Trace End Address Registers 1 and 2 (DTEA*n*)

The data trace end address registers define the end addresses for each trace channel.

Nexus Reg: 0x0012 Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Data Trace End Address																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-25. Data Trace End Address Register 1 (DTEA1)

Nexus Reg: 0x0013 Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Data Trace End Address																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-26. Data Trace End Address Register 2 (DTEA2)

Table 25-33 illustrates the range that is selected for data trace for various cases of DTSA being less than, greater than, or equal to DTEA.

Table 25-33. Data Trace—Address Range Options

Programmed Values	Range Control Bit Value	Range Selected
DTSA < DTEA	0	DTSA -> <- DTEA
DTSA < DTEA	1	<- DTSA DTEA ->
DTSA > DTEA	N/A	Invalid range—no trace
DTSA = DTEA	N/A	Invalid range—no trace

NOTE

DTSA must be less than DTEA to guarantee correct data write/read traces. Data trace ranges are exclusive of the DTSA and DTEA addresses.

25.11.11 NZ6C3 Register Access via JTAG / OnCE

Access to Nexus3 register resources is enabled by loading a single instruction (ACCESS_AUX_TAP_ONCE) into the JTAGC instruction register (IR), and then loading the corresponding OnCE OCMD register with the NEXUS3_ACCESS instruction (refer to Table 25-5). For the NZ6C3 module, the OCMD value is 0b00_0111_1100.

After the ACCESS_AUX_TAP_ONCE instruction has been loaded, the JTAG/OnCE port allows tool/target communications with all Nexus3 registers according to the register map in Table 25-24.

Reading/writing of a NZ6C3 register then requires two (2) passes through the data-scan (DR) path of the JTAG state machine (refer to 25.14.10).

1. The first pass through the DR selects the NZ6C3 register to be accessed by providing an index (refer to Table 25-24), and the direction (read/write). This is achieved by loading an 8-bit value into the JTAG data register (DR). This register has the following format:

(7-bits)	(1-bit)
Nexus register index	R/W

RESET Value: 0x00

Nexus Register Index:	Selected from values in Table 25-24
Read/Write (R/W):	0 Read 1 Write

2. The second pass through the DR then shifts the data in or out of the JTAG port, lsb first.
   a) During a read access, data is latched from the selected Nexus register when the JTAG state machine passes through the capture-DR state.
   b) During a write access, data is latched into the selected Nexus register when the JTAG state machine passes through the update-DR state.

25.12 Ownership Trace

This section details the ownership trace features of the NZ6C3 module.

Ownership trace provides a macroscopic view, such as task flow reconstruction, when debugging software written in a high level (or object-oriented) language. It offers the highest level of abstraction for tracking operating system software execution. This is especially useful when the developer is not interested in debugging at lower levels.

25.12.1 Ownership Trace Messaging (OTM)

Ownership trace information is messaged via the auxiliary port using an ownership trace message (OTM). The e200z6 processor contains a Power Architecture Book E defined process ID register within the CPU.

The process ID register is updated by the operating system software to provide task/process ID information. The contents of this register are replicated on the pins of the processor and connected to Nexus. The process ID register value can be accessed using the **mfspr**/**mtspr** instructions. Please refer to the *e200z6 PowerPC*^{TM} *Core Reference Manual*for more details on the process ID register.

The only condition that causes an ownership trace message occurs when the OTR register is updated or process ID register by the e200z6 processor, the data is latched within Nexus, and is messaged out via the auxiliary port, allowing development tools to trace ownership flow.

Ownership trace information is messaged out in the following format:

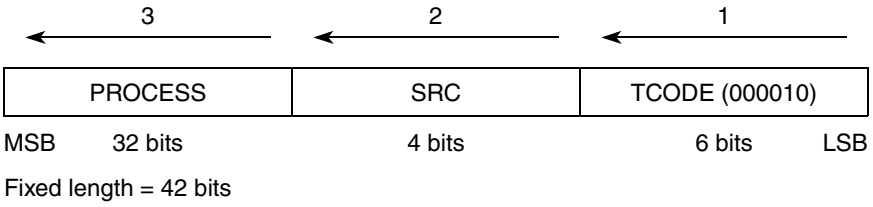


Figure 25-27. Ownership Trace Message Format

25.12.2 OTM Error Messages

An error message occurs when a new message cannot be queued due to the message queue being full. The FIFO discards incoming messages until the queue the queue is completely empty. After it empties, an error message is queued. The error encoding indicate the message types denied service to the queue while the FIFO was emptying.

If an OTM message only attempts to enter the queue while the queue is emptying, the error message incorporates the OTM error encoding (00000) only. If OTM and either BTM or DTM messages attempt to enter the queue, the error message incorporates the OTM and (program or data) trace error encoding (00111). If a watchpoint also attempts to enter the queue while the FIFO is emptying, then the error message incorporates error encoding (01000).

NOTE

The OVC bits within the DC1 register can be set to delay the CPU to alleviate (but not eliminate) potential overrun situations.

Error information is messaged out in the following format (refer to Table 25-20):

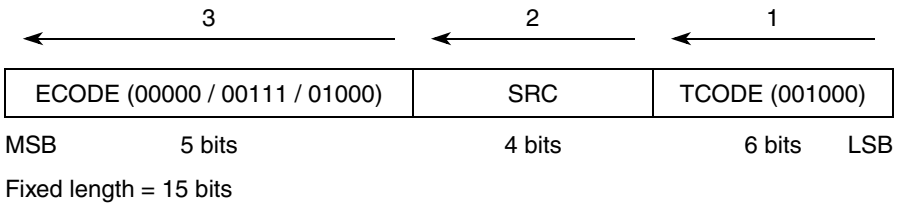


Figure 25-28. Error Message Format

25.12.3 OTM Flow

Ownership trace messages are generated when the operating system writes to the e200z6 process ID register or the memory mapped ownership trace register.

The following flow describes the OTM process:

1. The process ID register is a system control register. It is internal to the e200z6 processor and can be accessed by using PPC instructions **mtspr** and **mfspr**. The contents of this register are replicated on the pins of the processor and connected to Nexus.
2. OTR/process ID register reads do not cause ownership trace messages to be transmitted by the NZ6C3 module.
3. If the periodic OTM message counter expires (after 255 queued messages without an OTM), an OTM is sent using the latched data from the previous OTM or process ID register write.

25.13 Program Trace

This section details the program trace mechanism supported by NZ6C3 for the e200z6 processor. Program trace is implemented via branch trace messaging (BTM) as per the Class 3 IEEE®-ISTO 5001-2003 standard definition. Branch trace messaging for e200z6 processors is accomplished by snooping the e200z6 virtual address bus (between the CPU and MMU), attribute signals, and CPU status.

25.13.1 Branch Trace Messaging (BTM)

Traditional branch trace messaging facilitates program trace by providing the following types of information:

- Messages generated for direct branches that were taken indicate the number of sequential instructions executed since the last branch or exception. Branches not taken (direct or indirect) are not counted as sequential instructions.
- Messages generated for indirect branches and exceptions that were taken indicate:
  - Number of sequential instructions executed since the last branch that was taken
  - Exception with the unique portion of the branch target address or exception vector address
- History field in the branch and predicate instructions that can generate the following messages for program trace:
  - Number of sequential instructions executed since the last indirect branch was taken, as well as the unique portion of the indirect branch address
  - Number of sequential instructions executed since the last exception was processed, as well as the unique portion of the exception vector address
  - Number of sequential instructions executed since the last predicate instruction was taken
  - History field in the branch and predicate instruction unique to the branch target address or exception vector address. Each bit in the history field represents a direct branch or predicated instruction where a value of one (1) indicates taken, and a value of zero (0) indicates not taken. Certain instructions (**evsel**) generate a pair of predicate bits which are both reported as consecutive bits in the history field.

25.13.1.1 e200z6 Indirect Branch Message Instructions (Power Architecture Book E)

Table 25-34 shows the types of instructions and events which cause indirect branch messages or branch history messages to be encoded.

Table 25-34. Indirect Branch Message Sources

Source of Indirect Branch Message	Instructions
Taken branch relative to a register value	bcctr, bcctrl, bclr, bclrl
System call / trap exceptions taken	sc, tw, twi
Return from interrupts / exceptions	rfi, rfci, rfdi

25.13.1.2 e200z6 Direct Branch Message Instructions (Power Architecture Book E)

Table 25-35 shows the instruction types that cause direct branch messages, or toggles a bit in the instruction history buffer in a resource full message or branch history message before it is sent out.

Table 25-35. Direct Branch Message Sources

Source of Direct Branch Message	Instructions
Taken direct branch instructions	b, ba, bl, bla, bc, bca, bcl, bcla
Instruction synchronize	isync

25.13.1.3 BTM Using Branch History Messages

Traditional BTM messaging can accurately track the number of sequential instructions between branches, but cannot accurately indicate which instructions were conditionally executed, and which were not.

Branch history messaging solves this problem by providing a predicated instruction history field in each indirect branch message. Each bit in the history represents a predicated instruction or direct branch. A value of one (1) indicates the conditional instruction was executed or the direct branch was taken. A value of zero (0) indicates the conditional instruction was not executed or the direct branch was not taken. Certain instructions (**evsel**) generate a pair of predicate bits which are both reported as consecutive bits in the history field.

Branch history messages solve predicated instruction tracking and save bandwidth since only indirect branches cause messages to be queued.

25.13.1.4 BTM Using Traditional Program Trace Messages

Based on the PTM bit in the DC register (DC[PTM]), program tracing can use:

- Branch history messages (DC[PTM] = 1); or
- Traditional direct and indirect branch messages (DC[PTM] = 0)

Branch history saves bandwidth and keeps consistency between methods of program trace, yet can lose temporal order between BTM messages and other types of messages. Since direct branches are not messaged, but are instead included in the history field of the indirect branch history message, other types of messages can enter the FIFO between branch history messages. The development tool cannot determine the order of “events” that occurred for direct branches by the order in which messages are sent out.

Traditional BTM messages maintain their temporal ordering because each event that queues a message to the FIFO is processed and sent in the order it was generated, and the message order is maintained when it is transmitted.

25.13.2 BTM Message Formats

The e200z6 Nexus3 module supports three types of traditional BTM messages—direct, indirect, and synchronization messages. It supports two types of branch history BTM messages—indirect branch history, and indirect branch history with synchronization messages. Debug status messages and error messages are also supported.

25.13.2.1 Indirect Branch Messages (History)

Indirect branches include all taken branches whose destination is determined at run time, interrupts and exceptions. If DC[PTM] is set, indirect branch information is messaged out in the following format:

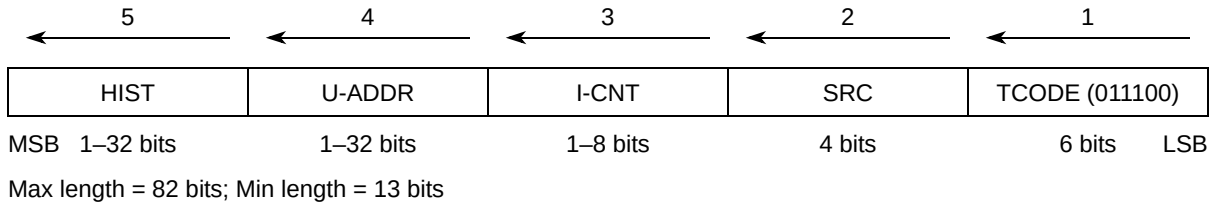


Figure 25-29. Indirect Branch Message (History) Format

25.13.2.2 Indirect Branch Messages (Traditional)

If DC[PTM] is cleared, indirect branch information is messaged out in the following format:

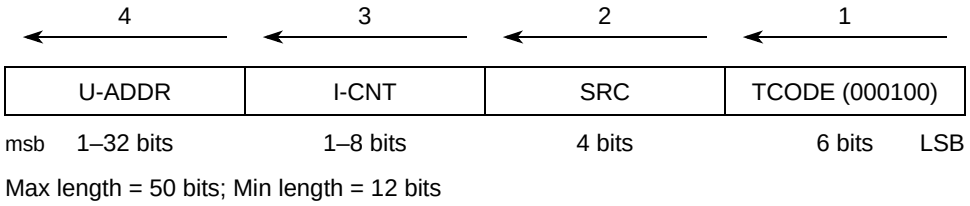


Figure 25-30. Indirect Branch Message Format

25.13.2.3 Direct Branch Messages (Traditional)

Direct branches (conditional or unconditional) are all taken branches whose destination is fixed in the instruction opcode. Direct branch information is messaged out in the following format:

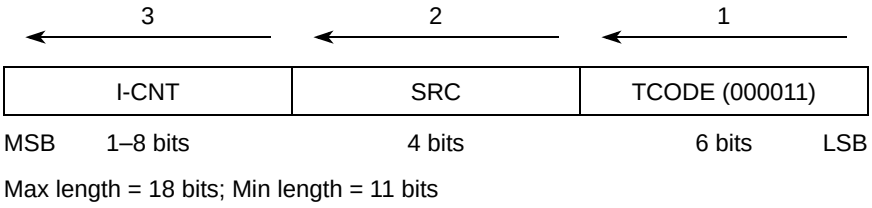


Figure 25-31. Direct Branch Message Format

NOTE

When DC[PTM] is set, direct branch messages are not transmitted. Instead, each direct branch or predicated instruction toggles a bit in the history buffer.

25.13.2.4 Resource Full Messages

The resource full message is used in conjunction with the branch history messages. The resource full message is generated when the internal branch/predicate history buffer is full, or if the BTM Instruction sequence counter (I-CNT) overflows. If synchronization is needed at the time this message is generated, the synchronization is delayed until the next branch trace message that is not a resource full message.

The current value of the history buffer is transmitted as part of the resource full message. This information can be concatenated by the tool with the branch/predicate history information from subsequent messages to obtain the complete branch history for a message. The internal history value is reset by this message, and the I-CNT value is reset as a result of a bit being added to the history buffer.

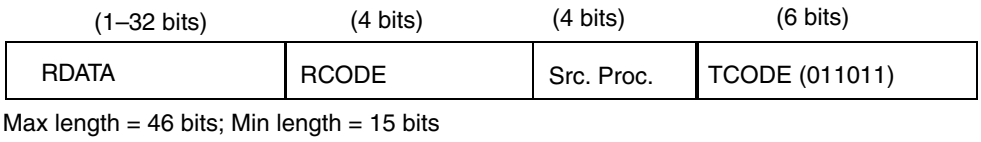


Figure 25-32. Resource Full Message Format

25.13.2.5 Debug Status Messages

NOTE

Debug Status Messages (DSMs) are enabled if the Nexus module is enabled.

Debug status messages report low power mode and debug status. Entering/exiting debug mode as well as entering a low power mode triggers a debug status message.

Debug status information is sent out in the following format:

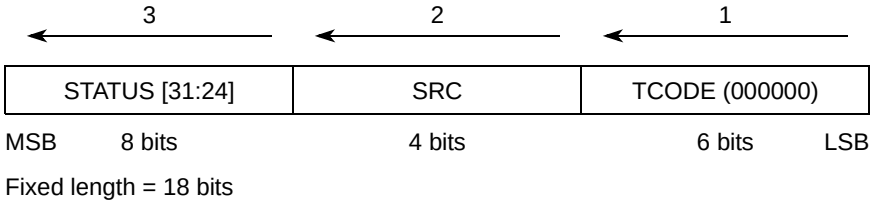


Figure 25-33. Debug Status Message Format

25.13.2.6 Program Correlation Messages

Program correlation messages are used to correlate events to the program flow that may not be associated with the instruction stream. To maintain accurate instruction tracing information when entering debug mode or a CPU low power mode (where tracing may be disabled), this message is sent upon entry into one of these two modes and includes the instruction count and branch history. Program correlation is messaged out in the following format:

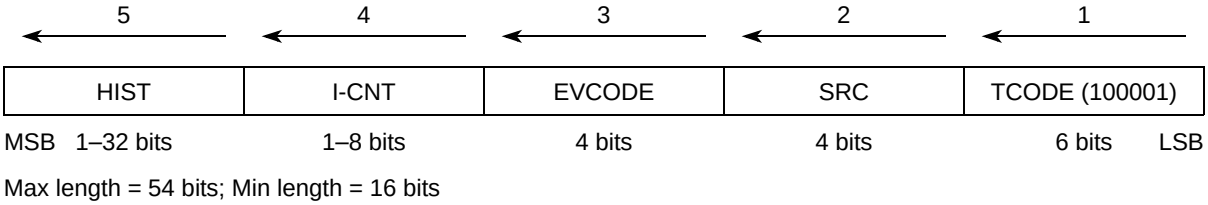


Figure 25-34. Program Correlation Message Format

25.13.2.7 BTM Overflow Error Messages

An error message occurs when a new message cannot be queued because the message queue is full. The FIFO discards incoming messages until the queue is completely empty. After it is empty, an error message is queued. The error encoding indicates which message types were denied queueing while the FIFO was emptying.

If only a program trace message attempts to enter the queue while it is being emptied, the error message incorporates the program trace only error encoding (00001). If both OTM and program trace messages attempt to enter the queue, the error message incorporates the OTM and program trace error encoding (00111). If a watchpoint also attempts to be queued while the FIFO is being emptied, then the error message incorporates error encoding (01000).

NOTE

The OVC bits within the DC1 register can be set to delay the CPU to alleviate (but not eliminate) potential overrun situations.

Error information is messaged out in the following format:

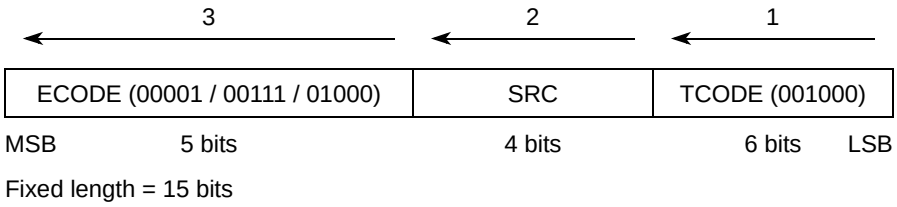


Figure 25-35. Error Message Format

25.13.3 Program Trace Synchronization Messages

A program trace direct/indirect branch with sync message is messaged via the auxiliary port (provided program trace is enabled) for the following conditions (refer to Table 25-36):

- Initial program trace message upon the first direct/indirect branch after exit from system reset or whenever program trace is enabled
- Upon direct/indirect branch after returning from a CPU low power state
- Upon direct/indirect branch after returning from debug mode
- Upon direct/indirect branch after occurrence of queue overrun (can be caused by any trace message), provided program trace is enabled
- Upon direct/indirect branch after the periodic program trace counter has expired indicating 255 *without-sync* program trace messages have occurred since the last *with-sync* message occurred
- Upon direct/indirect branch after assertion of the event in (EVTI) pin if the EIC bits within the DC1 register have enabled this feature
- Upon direct/indirect branch after the sequential instruction counter has expired indicating 255 instructions have occurred between branches
- Upon direct/indirect branch after a BTM message was lost due to an attempted access to a secure memory location.
- Upon direct/indirect branch after a BTM message was lost due to a collision entering the FIFO between the BTM message and either a watchpoint message or an ownership trace message

If the NZ6C3 module is enabled at reset, a EVTI assertion initiates a program trace direct/indirect branch with sync message (if program trace is enabled) upon the first direct/indirect branch. The format for program trace direct/indirect branch with sync messages is as follows:

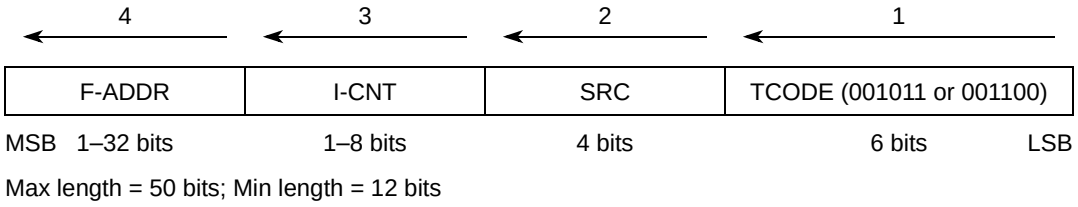


Figure 25-36. Direct/Indirect Branch with Sync Message Format

The formats for program trace direct/indirect branch with sync. messages and indirect branch history with sync. messages are as follows:

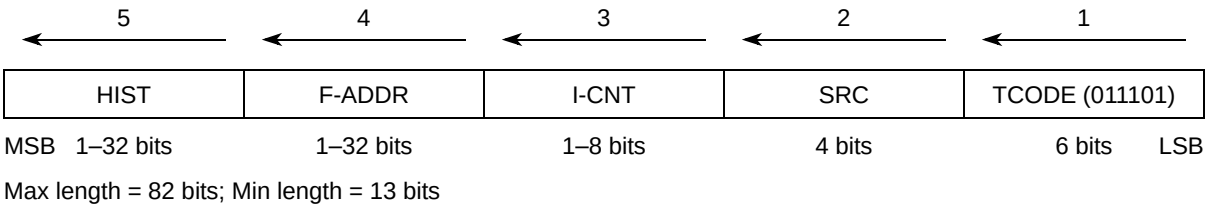


Figure 25-37. Indirect Branch History with Sync. Message Format

Exception conditions that result in program trace synchronization are summarized in Table 25-36.

Table 25-36. Program Trace Exception Summary

Exception Condition	Exception Handling
System Reset Negation	At the negation of JTAG reset (JCOMP), queue pointers, counters, state machines, and registers within the NZ6C3 module are reset. Upon the first branch out of system reset (if program trace is enabled), the first program trace message is a direct/indirect branch with sync. message.
Program Trace Enabled	The first program trace message (after program trace has been enabled) is a synchronization message.
Exit from Low Power/Debug	Upon exiting from the low power or debug modes, the next direct/indirect branch is converted to a direct/indirect branch with sync. message.
Queue Overrun	An error message occurs when a new message cannot be queued due to the message queue being full. The FIFO discards messages until the queue is completely empty. After it is empty, an error message is queued. The error encoding indicates the message types denied queueing while the FIFO was emptying. The next BTM message in the queue is a direct/indirect branch with sync. message.
Periodic Program Trace Sync.	A forced synchronization occurs periodically after 255 program trace messages have been queued. A direct/indirect branch with sync. message is queued. The periodic program trace message counter then resets.
Event In	If the Nexus module is enabled, an EVTI assertion initiates a direct/indirect branch with sync. message upon the next direct/indirect branch (if program trace is enabled and the EIC bits of the DC1 register have enabled this feature).
Sequential Instruction Count Overflow	When the sequential instruction counter reaches its maximum count (up to 255 sequential instructions may be executed), a forced synchronization occurs. The sequential counter then resets. A program trace direct/indirect branch with sync.message is queued upon execution of the next branch.
Attempted Access to Secure Memory	For devices which implement security, any attempt to branch to secure memory locations temporarily disables program trace & cause the corresponding BTM to be lost. The following direct/indirect branch queues a direct/indirect branch with sync. message. The count value within this message can be inaccurate since re-enabling program trace does not guarantee alignment on an instruction boundary.
Collision Priority	All messages have the following priority: WPM -> OTM -> BTM -> DTM. A BTM message which attempts to enter the queue at the same time as a watchpoint message or ownership trace message is lost. An error message is sent indicating the BTM was lost. The following direct/indirect branch queues a direct/indirect branch with sync. message. The count value within this message reflects the number of sequential instructions executed after the last successful BTM message was generated. This count includes the branch which did not generate a message due to the collision.

25.14 BTM Operation

25.14.1 Enabling Program Trace

Both types of branch trace messaging can be enabled in one of two ways:

- Setting the TM field of the DC1 register to enable program trace (DC1[TM])
- Using the PTS field of the WT register to enable program trace on watchpoint hits (e200z6 watchpoints are configured within the CPU)

25.14.2 Relative Addressing

The relative address feature is compliant with the IEEE®-ISTO 5001-2003 standard recommendations, and is designed to reduce the number of bits transmitted for addresses of indirect branch messages.

The address transmitted is relative to the target address of the instruction which triggered the previous indirect branch (or sync) message. It is generated by XOR'ing the new address with the previous address, and then using only the results up to the most significant 1 in the result. To recreate this address, an XOR of the (most-significant 0-padded) message address with the previously decoded address gives the current address.

```
Previous address (A1) =0x0003FC01, New address (A2) = 0x0003F365
```

Message Generation:

A1 = 0000 0000 0000 0011 1111 1100 0000 0001
A2 = 0000 0000 0000 0011 1111 0011 0110 0101

A1 ⊕ A2 = 0000 0000 0000 0000 0000 1111 0110 0100

Address Message (M1) = 1111 0110 0100

Address Re-creation:

A1 ⊕ M1 = A2
A1 = 0000 0000 0000 0011 1111 1100 0000 0001
M1 = 0000 0000 0000 0000 0000 1111 0110 0100

A2 = 0000 0000 0000 0011 1111 0011 0110 0101

Figure 25-38. Relative Address Generation and Re-creation

25.14.3 Branch and Predicate Instruction History (HIST)

If DC[PTM] is set, BTM messaging uses the branch history format. The branch history (HIST) packet in these messages provides a history of direct branch execution used for reconstructing the program flow. This packet is implemented as a left-shifting shift register. The register is always pre-loaded with a value of one (1). This bit acts as a stop bit so that the development tools can determine which bit is the end of the history information. The pre-loaded bit itself is not part of the history, but is transmitted with the packet.

A value of one (1) is shifted into the history buffer on a taken branch (condition or unconditional) and on any instruction whose predicate condition executed as true. A value of zero (0) is shifted into the history buffer on any instruction whose predicate condition executed as false as well as on branches not taken. This includes indirect as well as direct branches were not taken. For the **evsel** instruction, two bits are shifted in, corresponding to the low element (shifted in first) and the high element (shifted in second) conditions.

25.14.4 Sequential Instruction Count (I-CNT)

The I-CNT packet, is present in all BTM messages. For traditional branch messages, I-CNT represents the number of sequential instructions, or non-taken branches in between direct/indirect branch messages.

For branch history messages, I-CNT represents the number of instructions executed since the last taken/non-taken direct branch, last taken indirect branch or exception. Not taken indirect branches are considered sequential instructions and cause the instruction count to increment. I-CNT also represents the number of instructions executed since the last predicate instruction.

The sequential instruction counter overflows when its value reaches 255. The next BTM message is converted to a synchronization type message.

25.14.5 Program Trace Queueing

NZ6C3 implements a message queue. Messages that enter the queue are transmitted via the auxiliary pins in the order in which they are queued.

NOTE

If multiple trace messages must be queued at the same time, Watchpoint Messages have the highest priority (WPM –> OTM –> BTM –> DTM).

25.14.5.1 Program Trace Timing Diagrams

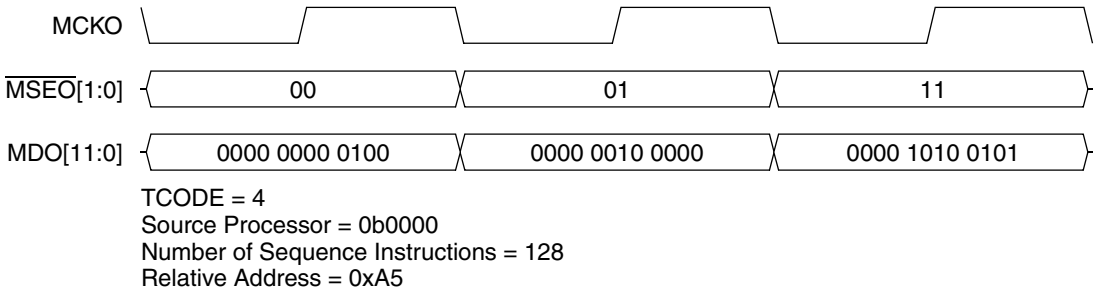


Figure 25-39. Program Trace (MDO = 12)—Indirect Branch Message (Traditional)

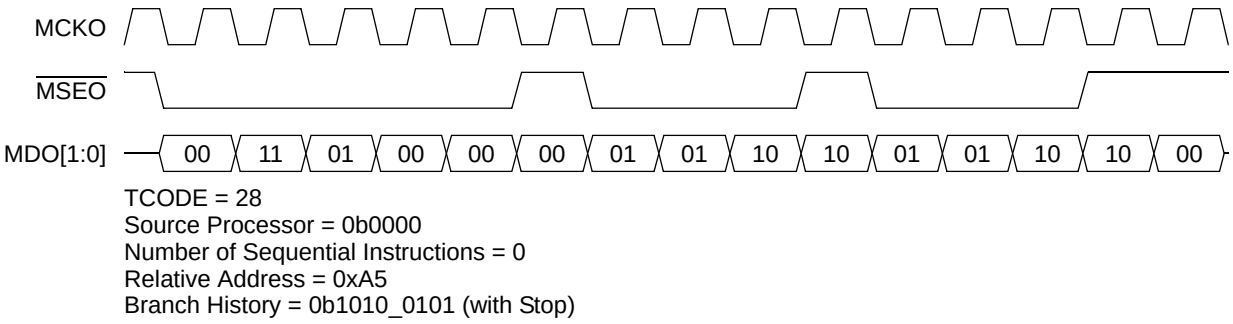


Figure 25-40. Program Trace (MDO = 2)—Indirect Branch Message (History)

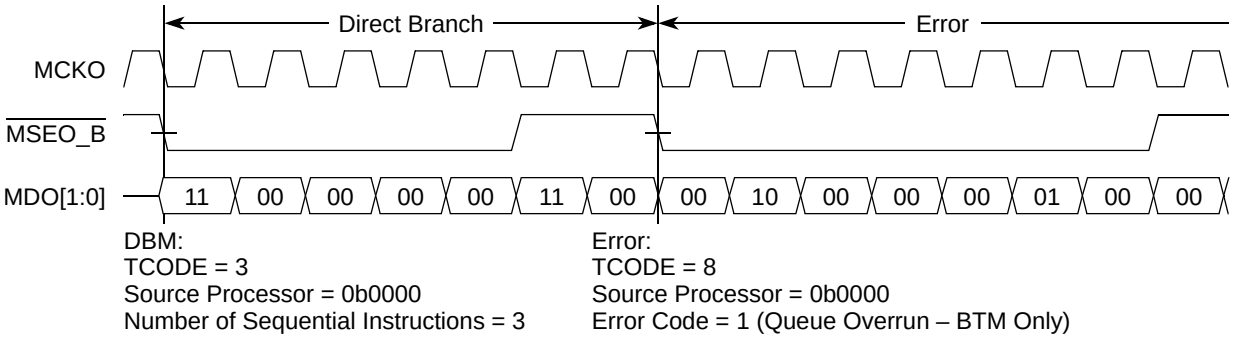


Figure 25-41. Program Trace—Direct Branch (Traditional) and Error Messages

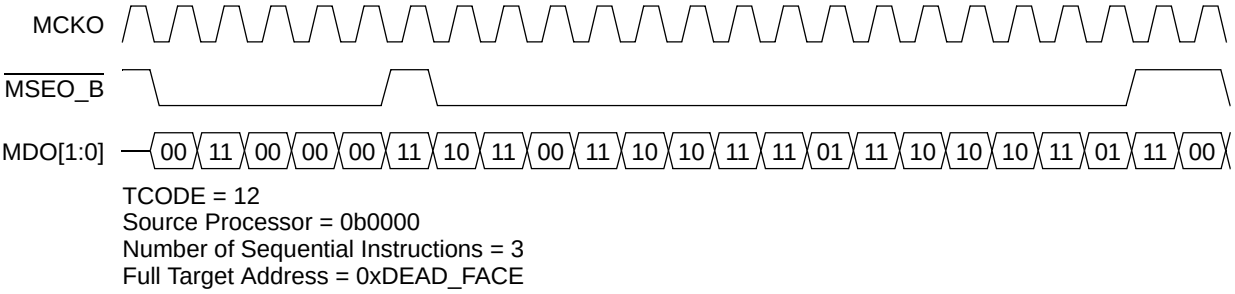


Figure 25-42. Program Trace—Indirect Branch with Sync. Message

25.14.6 Data Trace

This section deals with the data trace mechanism supported by the NZ6C3 module. Data trace is implemented via data write messaging (DWM) and data read messaging (DRM), as per the IEEE®-ISTO 5001-2003 standard.

25.14.6.1 Data Trace Messaging (DTM)

Data trace messaging for e200z6 is accomplished by snooping the e200z6 virtual data bus (between the CPU and MMU), and storing the information for qualifying accesses (based on enabled features and matching target addresses). The NZ6C3 module traces all data access that meet the selected range and attributes.

NOTE

Data trace is only performed on the e200z6 virtual data bus. This allows for data visibility for the incorporated data cache. Only e200z6 CPU initiated accesses are traced. No DMA accesses to the NXDM system bus are traced.

Data trace messaging can be enabled in one of two ways:

- Setting the TM field of the DC1 register to enable data trace (DC1[TM]).
- Using WT[DTS] to enable data trace on watchpoint hits (e200z6 watchpoints are configured within the Nexus1 module)

25.14.6.2 DTM Message Formats

The Nexus3 module supports five types of DTM messages: data write, data read, data write synchronization, data read synchronization and error messages.

25.14.6.2.1 Data Write Messages

The data write message contains the data write value and the address of the write access, relative to the previous data trace message. Data write message information is messaged out in the following format:

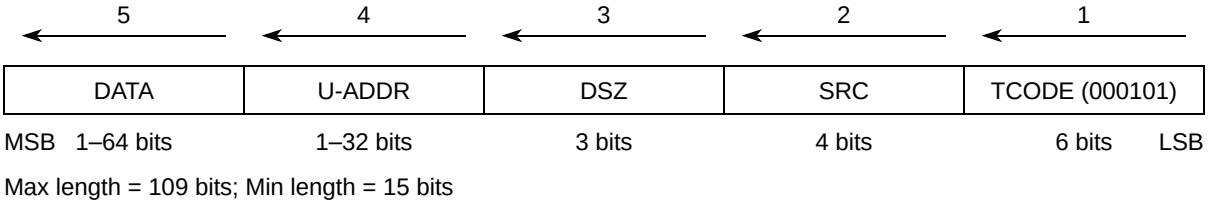


Figure 25-43. Data Write Message Format

25.14.6.2.2 Data Read Messages

The data read message contains the data read value and the address of the read access, relative to the previous data trace message. Data read message information is messaged out in the following format:

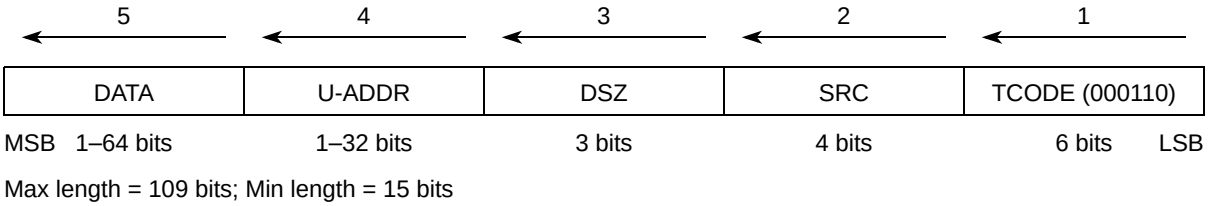


Figure 25-44. Data Read Message Format

NOTE

For the e200z6 based CPU, the doubleword encoding (data size = 0b000) indicates a doubleword access and sends out as a single data trace message with a single 64-bit data value.

25.14.6.2.3 DTM Overflow Error Messages

An error message occurs when the next message is denied service because the message queue is full. The FIFO discards all incoming messages until the queue is completely empty. After it is empty, an error message is queued that indicates the message types denied into the queue while the FIFO is emptying.

If a data trace message only attempts to enter the queue while it is emptying, the error message incorporates the data trace only error encoding (00010). If both OTM and data trace messages attempt to enter the queue, the error message incorporates the OTM and data trace error encoding (00111). If a watchpoint also attempts to be queued while the FIFO is being emptied, then the error message incorporates error encoding (01000).

NOTE

The OVC bits within the DC1 register can be set to delay the CPU to alleviate (but not eliminate) potential overrun situations.

Error information is messaged out in the following format:

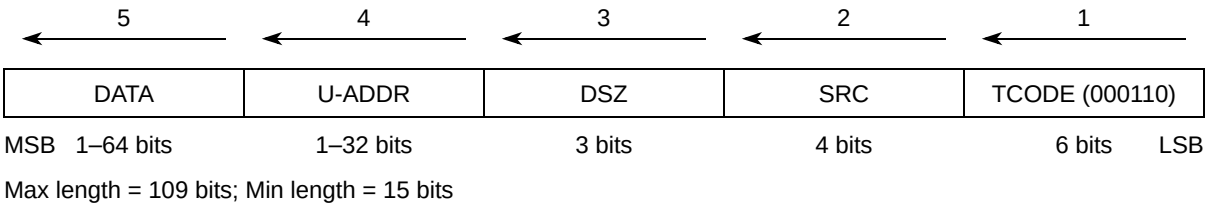


Figure 25-45. Error Message Format

25.14.6.2.4 Data Trace Synchronization Messages

A data trace write/read with sync. message is messaged via the auxiliary port (provided data trace is enabled) for the following conditions (refer to Table 25-37):

- Initial data trace message after exit from system reset or whenever data trace is enabled
- Upon exiting debug mode
- After occurrence of queue overrun (can be caused by any trace message), provided data trace is enabled
- After the periodic data trace counter has expired indicating 255 *without-sync* data trace messages have occurred since the last *with-sync* message occurred
- Upon assertion of the event in (EVTI) pin, the first data trace message is a synchronization message if the EIC bits of the DC1 register have enabled this feature
- Upon data trace write/read after the previous DTM message was lost due to an attempted access to a secure memory location

- Upon data trace write/read after the previous DTM message was lost due to a collision entering the FIFO between the DTM message and any of the following: watchpoint message, ownership trace message, or branch trace message

Data trace synchronization messages provide the full address (without leading zeros) and insure that development tools fully synchronize with data trace regularly. Synchronization messages provide a reference address for subsequent data messages, in which only the unique portion of the data trace address is transmitted. The format for data trace write/read with sync. messages is as follows:

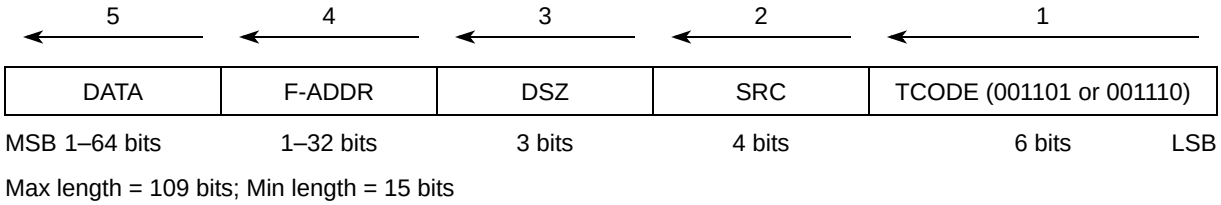


Figure 25-46. Data Write/Read with Sync. Message Format

Exception conditions that result in data trace synchronization are summarized in Table 25-37.

Table 25-37. Data Trace Exception Summary

Exception Condition	Exception Handling
System Reset Negation	At the negation of JTAG reset (JCOMP), queue pointers, counters, state machines, and registers within the NZ6C3 module are reset. If data trace is enabled, the first data trace message is a data write/read with sync. message.
Data Trace Enabled	The first data trace message (after data trace has been enabled) is a synchronization message.
Exit from Low Power/Debug	Upon exiting from low power or debug modes, the next data trace message is converted to a data write/read with sync. message.
Queue Overrun	An error message occurs when a new message cannot be queued due to a full message queue. The FIFO discards messages until it has completely emptied the queue. After the queue is empty, an error message is queued that indicates the message types denied queuing while the FIFO was emptying. The next DTM message in the queue is a data write/read with sync. message.
Periodic Data Trace Sync.	A forced synchronization occurs periodically after 255 data trace messages have been queued. A data write/read with sync. message is queued. The periodic data trace message counter then resets.
Event In	If the Nexus module is enabled, a EVTI assertion initiates a data trace write/read with sync. message upon the next data write/read (if data trace is enabled and the EIC bits of the DC1 register have enabled this feature).
Attempted Access to Secure Memory	For devices which implement security, any attempted read or write to secure memory locations temporarily disables data trace and loses the DTM. A subsequent read/write queues a data trace read/write with sync. message.
Collision Priority	All messages have the following priority: WPM –> OTM –> BTM –> DTM. A DTM message which attempts to enter the queue at the same time as a watchpoint message or ownership trace message or branch trace message can be lost. A subsequent read/write queues a data trace read/write with sync. message.

25.14.6.3 DTM Operation

25.14.6.3.1 DTM Queueing

NZ6C3 implements a message queue for DTM messages. Messages that enter the queue are transmitted via the auxiliary pins in the order in which they are queued.

NOTE

If multiple trace messages must be queued at the same time, watchpoint messages have the highest priority (WPM –> OTM –> BTM –> DTM).

25.14.6.3.2 Relative Addressing

The relative address feature is compliant with the IEEE®-ISTO 5001-2003 standard recommendations, and is designed to reduce the number of bits transmitted for addresses of data trace messages. Refer to Section 25.14.2, " Relative Addressing for details.

25.14.6.3.3 Data Trace Windowing

Data write/read messages are enabled via the RWT1(2) field in the data trace control register (DTC) for each DTM channel. Data trace windowing is achieved via the address range defined by the DTEA and DTSA registers and by the RC1(2) field in the DTC. All e200z6 initiated read/write accesses which fall inside or outside these address ranges, as programmed, are candidates to be traced.

25.14.6.3.4 Data Access/Instruction Access Data Tracing

The Nexus3 module is capable of tracing both instruction access data or data access data. Each trace window can be configured for either type of data trace by setting the DI1(2) field within the data trace control register for each DTM channel.

25.14.6.3.5 e200z6 Bus Cycle Special Cases

Table 25-38. e200z6 Bus Cycle Cases

Special Case	Action
e200z6 bus cycle aborted	Cycle ignored
e200z6 bus cycle with data error ($\overline{\text{TEA}}$)	Data Trace Message discarded
e200z6 bus cycle completed without error	Cycle captured & transmitted
e200z6 bus cycle initiated by NZ6C3	Cycle ignored
e200z6 bus cycle is an instruction fetch	Cycle ignored
e200z6 bus cycle accesses misaligned data (across 64-bit boundary)—both 1st and 2nd transactions within data trace range	1st and 2nd cycle captured, and 2 DTM's transmitted (refer to Note)

Table 25-38. e200z6 Bus Cycle Cases (continued)

Special Case	Action
e200z6 bus cycle accesses misaligned data (across 64-bit boundary)—1st transaction within data trace range; 2nd transaction out of data trace range	1st cycle captured and transmitted; 2nd cycle ignored
e200z6 bus cycle accesses misaligned data (across 64-bit boundary)—1st transaction out of data trace range; 2nd transaction within data trace range	1st cycle ignored; 2nd cycle capture and transmitted

NOTE

For misaligned accesses (crossing 64-bit boundary), the access is broken into two accesses. If both accesses are within the data trace range, two DTMs are sent: one with a size encoding indicating the size of the original access (that is, word), and one with a size encoding for the portion which crossed the boundary (that is, 3-byte).

NOTE

An STM to the cache's store buffer within the data trace range initiates a DTM message. If the corresponding memory access causes an error, a checkstop condition occurs. The debug/development tool must use this indication to invalidate the previous DTM.

25.14.6.4 Data Trace Timing Diagrams (Eight MDO Configuration)

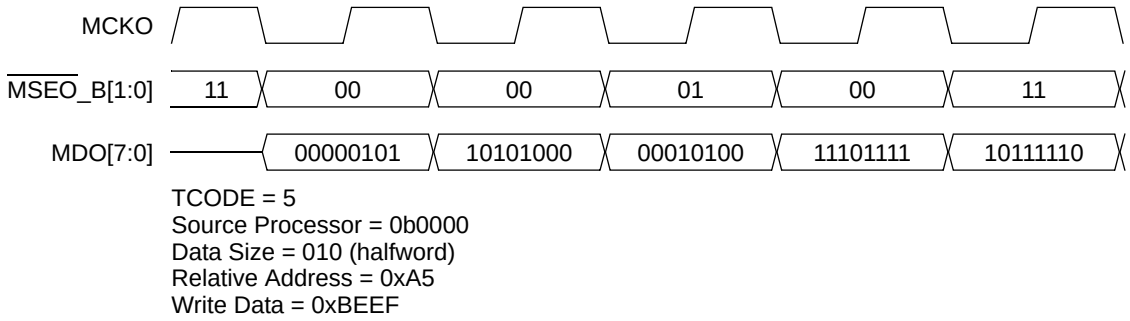


Figure 25-47. Data Trace—Data Write Message

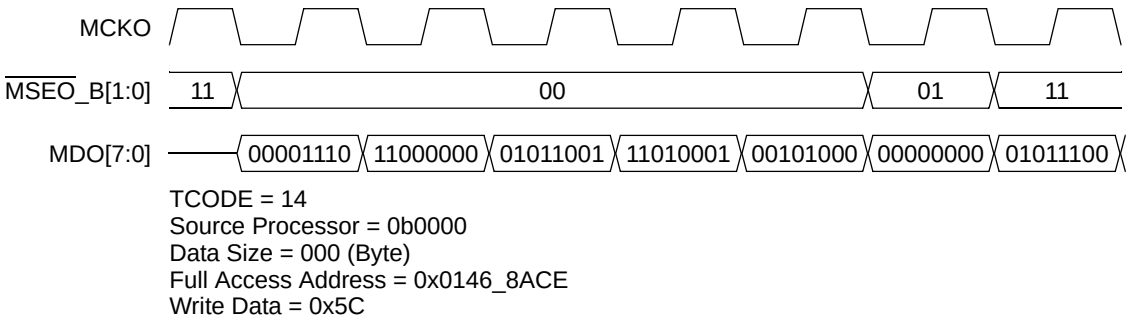


Figure 25-48. Data Trace—Data Read with Sync Message

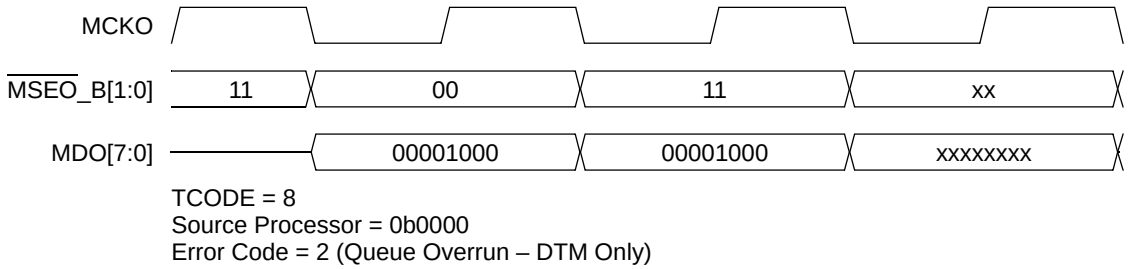


Figure 25-49. Error Message (Data Trace only encoded)

25.14.7 Watchpoint Support

This section details the watchpoint features of the NZ6C3 module.

25.14.7.1 Overview

The NZ6C3 module provides watchpoint messaging via the auxiliary pins, as defined by the IEEE®-ISTO 5001-2003 standard.

NZ6C3 is not compliant with Class4 breakpoint/watchpoint requirements defined in the standard. The breakpoint/watchpoint control register is not implemented.

25.14.7.2 Watchpoint Messaging

Enabling watchpoint messaging is done by setting the watchpoint enable bit in the DC1 register. Setting the individual watchpoint sources is supported through the e200z6 Nexus1 module. The e200z6 Nexus1 module is capable of setting multiple address and/or data watchpoints. Please refer to the e200z6 Core Reference Manual for more information on watchpoint initialization.

When these watchpoints occur, a watchpoint event signal from the Nexus1 module causes a message to be sent to the queue to be messaged out. This message includes the watchpoint number indicating which watchpoint caused the message.

The occurrence of any of the e200z6 defined watchpoints can be programmed to assert the event out $\overline{\text{EVTO}}$ pin for one period of the output clock (MCKO).

Watchpoint information is messaged out in the following format:

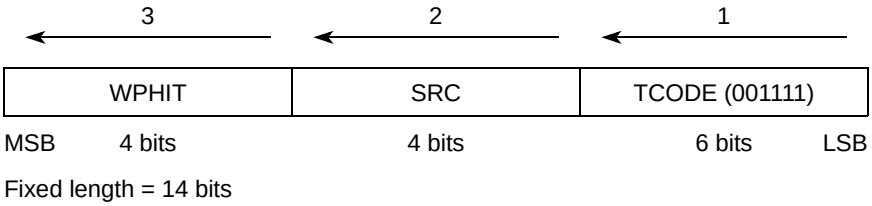


Figure 25-50. Watchpoint Message Format.

Table 25-39. Watchpoint Source Encoding

Watchpoint Source (8 bits)	Watchpoint Description
00000001	e200z6 Watchpoint #0 (IAC1 from Nexus1)
00000010	e200z6 Watchpoint #1 (IAC2 from Nexus1)
00000100	e200z6 Watchpoint #2 (IAC3 from Nexus1)
00001000	e200z6 Watchpoint #3 (IAC4 from Nexus1)
00010000	e200z6 Watchpoint #4 (DAC1 from Nexus1)
00100000	e200z6 Watchpoint #5 (DAC2 from Nexus1)
01000000	e200z6 Watchpoint #6 (DCNT1 from Nexus1)
10000000	e200z6 Watchpoint #7 (DCNT2 from Nexus1)

25.14.7.3 Watchpoint Error Message

An error message occurs when a new message cannot be queued due to the message queue being full. The FIFO discards messages until it has completely emptied the queue. After it is emptied, an error message is queued. The error encoding indicates the types of messages that attempted to be queued while the FIFO was being emptied.

If only a watchpoint message attempts to enter the queue while it is being emptied, the error message incorporates the watchpoint only error encoding (00110). If an OTM and/or program trace and/or data trace message also attempts to enter the queue while it is being emptied, the error message incorporates error encoding (01000).

NOTE

The OVC bits within the DC1 register can be set to delay the CPU to alleviate (but not eliminate) potential overrun situations.

Error information is messaged out in the following format (refer to Table 25-20):

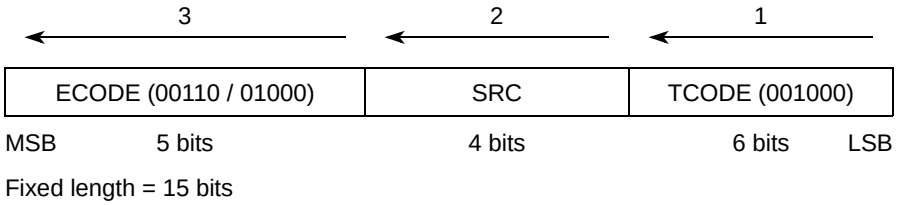


Figure 25-51. Error Message Format

25.14.7.4 Watchpoint Timing Diagram (2 MDO and 1 MSEO Configuration)

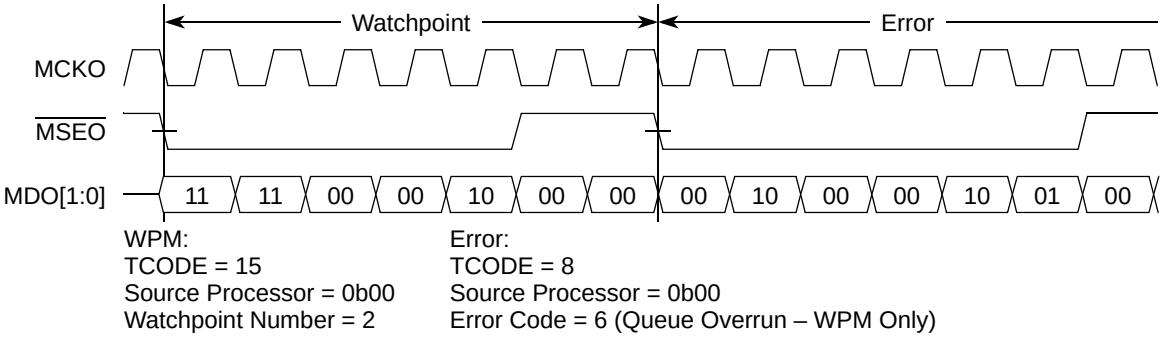


Figure 25-52. Watchpoint Message and Watchpoint Error Message

25.14.8 NZ6C3 Read/Write Access to Memory-Mapped Resources

The read/write access feature allows access to memory-mapped resources via the JTAG/OnCE port. The read/write mechanism supports single as well as block reads and writes to e200z6 system bus resources.

The NZ6C3 module is capable of accessing resources on the e200z6 system bus, with multiple configurable priority levels. Memory-mapped registers and other non-cached memory can be accessed via the standard memory map settings.

All accesses are setup and initiated by the read/write access control/status register (RWCS), as well as the read/write access address (RWA) and read/write access data registers (RWD).

Using the read/write access registers (RWCS/RWA/RWD), memory-mapped e200z6 system bus resources can be accessed through NZ6C3. The following subsections describe the steps which are required to access memory-mapped resources.

NOTE

Read/write access can only access memory mapped resources when system reset is de-asserted.

Misaligned accesses are NOT supported in the e200z6 Nexus3 module.

25.14.8.1 Single Write Access

1. Initialize the read/write access address register (RWA) through the access method outlined in Section 25.11.11, " NZ6C3 Register Access via JTAG / OnCE" using the Nexus register index of 0x9 (refer to Table 25-24). Configure as follows:
   – Write Address -> 0xnnnnnnnn (write address)
2. Initialize the read/write access control/status register (RWCS) through the access method outlined in Section 25.11.11, " NZ6C3 Register Access via JTAG / OnCE," using the Nexus Register Index of 0x7 (refer to Table 25-24). Configure the bits as follows:
   – Access Control RWCS[AC] –> 0b1 (to indicate start access)
   – Map Select RWCS[MAP] –> 0b000 (primary memory map)
   – Access Priority RWCS[PR] –> 0b00 (lowest priority)
   – Read/Write RWCS[RW] –> 0b1 (write access)
   – Word Size RWCS[SZ] –> 0b0xx (32-bit, 16-bit, 8-bit)
   – Access Count RWCS[CNT] –> 0x0000 or 0x0001 (single access)

NOTE

Access count RWCS[CNT] of 0x0000 or 0x0001 performs a single access.

3. Initialize the read/write access data register (RWD) through the access method outlined in Section 25.11.11, " NZ6C3 Register Access via JTAG / OnCE," using the Nexus register index of 0xA (refer to Table 25-24). Configure as follows:
   – Write Data -> 0xnnnnnnnn (write data)
4. The NZ6C3 module then arbitrates for the system bus and transfer the data value from the data buffer RWD register to the memory mapped address in the read/write access address register (RWA). When the access has completed without error (ERR=1'b0), NZ6C3 asserts the RDY pin and clears the DV bit in the RWCS register. This indicates that the device is ready for the next access.

NOTE

Only the RDY pin as well as the DV and ERR bits within the RWCS provide read/write access status to the external development tool.

25.14.8.2 Block Write Access (Non-Burst Mode)

1. For a non-burst block write access, follow Steps 1, 2, and 3 outlined in Section 25.14.8.1, "Single Write Access to initialize the registers," but using a value greater than one (0x1) for the RWCS[CNT] field.
2. The NZ6C3 module then arbitrates for the system bus and transfer the first data value from the RWD register to the memory mapped address in the read/write access address register (RWA). When the transfer has completed without error (ERR = 0), the address from the RWA register is incremented to the next word size (specified in the SZ field) and the number from the CNT field is decremented. Nexus then asserts the RDY pin. This indicates that the device is ready for the next access.

3. Repeat step 3 in Section 25.14.8.1, “Single Write Access” until the internal CNT value is zero (0). When this occurs, the DV bit within the RWCS is cleared to indicate the end of the block write access.

25.14.8.3 Block Write Access (Burst Mode)

1. For a burst block write access, follow Steps 1 and 2 outlined in Section 25.14.8.1, “Single Write Access” to initialize the registers, using a value of four (doublewords) for the CNT field and a RWCS[SZ] field indicating 64-bit access.
2. Initialize the burst data buffer (read/write access data register) through the access method outlined in Section 25.11.11, “ NZ6C3 Register Access via JTAG / OnCE,” using the Nexus register Index of 0xA (refer to Table 25-24).
3. Repeat step 2 until all doubleword values are written to the buffer.

NOTE

The data values must be shifted in 32-bits at a time lsb first (that is, doubleword write = two word writes to the RWD).

4. The Nexus module then arbitrates for the system bus and transfer the burst data values from the data buffer to the system bus beginning from the memory mapped address in the read/write access address register (RWA). For each access within the burst, the address from the RWA register is incremented to the next doubleword size (specified in the SZ field) modulo the length of the burst, and the number from the CNT field is decremented.
5. When the entire burst transfer has completed without error (ERR = 0), NZ6C3 then asserts the RDY pin, and the DV bit within the RWCS is cleared to indicate the end of the block write access.

NOTE

The actual RWA value as well as the CNT field within the RWCS are not changed when executing a block write access (burst or non-burst). The original values can be read by the external development tool at any time.

25.14.8.4 Single Read Access

1. Initialize the read/write access address register (RWA) through the access method outlined in Section 25.11.11, “ NZ6C3 Register Access via JTAG / OnCE,” using the Nexus register index of 0x9 (refer to Table 25-24). Configure as follows:
   – Read Address –> 0xnnnnnnnn (read address)
2. Initialize the read/write access control/status register (RWCS) through the access method outlined in Section 25.11.11, “ NZ6C3 Register Access via JTAG / OnCE,” using the Nexus register index of 0x7 (refer to Table 25-24). Configure the bits as follows:
   – Access Control RWCS[AC]–> 0b1 (to indicate start access)
   – Map Select RWCS[MAP] –> 0b000 (primary memory map)
   – Access Priority RWCS[PR] –> 0b00 (lowest priority)
   – Read/Write RWCS[RW] –> 0b0 (read access)
   – Word Size RWCS[SZ] –> 0b0xx (32-bit, 16-bit, 8-bit)

– Access Count RWCS[CNT]–> 0x0000 or 0x0001 (single access)

NOTE

Access Count (CNT) of 0x0000 or 0x0001 performs a single access.

3. The NZ6C3 module then arbitrates for the system bus and the read data is transferred from the system bus to the RWD register. When the transfer is completed without error (ERR = 0), Nexus asserts the RDY pin and sets the DV bit in the RWCS register. This indicates that the device is ready for the next access.
4. The data can then be read from the read/write access data register (RWD) through the access method outlined in Section 25.11.11, " NZ6C3 Register Access via JTAG / OnCE," using the Nexus register index of 0xA (refer to Table 25-24).

NOTE

Only the RDY pin as well as the DV and ERR bits within the RWCS provide Read/Write Access status to the external development tool.

25.14.8.5 Block Read Access (Non-Burst Mode)

1. For a non-burst block read access, follow Steps 1 and 2 outlined in Section 25.14.8.4, "Single Read Access" to initialize the registers, but using a value greater than one (0x1) for the CNT field in the RWCS register.
2. The NZ6C3 module then arbitrates for the system bus and the read data is transferred from the system bus to the RWD register. When the transfer has completed without error (ERR=0b0), the address from the RWA register is incremented to the next word size (specified in the SZ field) and the number from the CNT field is decremented. Nexus then asserts the RDY pin. This indicates that the device is ready for the next access.
3. The data can then be read from the read/write access data register (RWD) through the access method outlined in Section 25.11.11, " NZ6C3 Register Access via JTAG / OnCE," using the Nexus register index of 0xA (refer to Table 25-24).
4. Repeat steps 3 and 4 in Section 25.14.8.4, "Single Read Access" until the CNT value is zero (0). When this occurs, the DV bit within the RWCS is set to indicate the end of the block read access.

25.14.8.6 Block Read Access (Burst Mode)

1. For a burst block read access, follow Steps 1 and 2 outlined in Section 25.14.8.4, "Single Read Access" to initialize the registers, using a value of four (doublewords) for the CNT field and an RWCS[SZ] field indicating 64-bit access.
2. The NZ6C3 module then arbitrates for the system bus and the burst read data is transferred from the system bus to the data buffer (RWD register). For each access within the burst, the address from the RWA register is incremented to the next doubleword (specified in the SZ field) and the number from the CNT field is decremented.
3. When the entire burst transfer has completed without error (ERR = 0), Nexus then asserts the RDY pin and the DV bit within the RWCS is set to indicate the end of the block read access.

4. The data can then be read from the burst data buffer (read/write access data register) through the access method outlined in Section 25.11.11, “ NZ6C3 Register Access via JTAG / OnCE,” using the Nexus register index of 0xA (refer to Table 25-24).
5. Repeat step 3 until all doubleword values are read from the buffer.

NOTE

The data values must be shifted out 32-bits at a time lsb first (that is, doubleword read = two word reads from the RWD).

NOTE

The actual RWA value as well as the CNT field within the RWCS are not changed when executing a block read access (burst or non-burst). The original values can be read by the external development tool at any time.

25.14.8.7 Error Handling

The NZ6C3 module handles various error conditions as follows:

25.14.8.7.1 System Bus Read/Write Error

All address and data errors that occur on read/write accesses to the e200z6 system bus returns a transfer error. If this occurs:

1. The access is terminated without re-trying (AC bit is cleared).
2. The ERR bit in the RWCS register is set.
3. The error message is sent (TCODE = 8) indicating read/write error.

25.14.8.7.2 Access Termination

The following cases are defined for sequences of the read/write protocol that differ from those described in the above sections:

1. If the AC bit in the RWCS register is set to start read/write accesses and invalid values are loaded into the RWD and/or RWA, then a system bus access error may occur. This is handled as described above.
2. If a block access is in progress (all cycles not completed), and the RWCS register is written, then the original block access is terminated at the boundary of the nearest completed access.
   a) If the RWCS is written with the AC bit set, the next read/write access begins and the RWD can be written to/ read from.
   b) If the RWCS is written with the AC bit cleared, the read/write access is terminated at the nearest completed access. This method can be used to break (early terminate) block accesses.

25.14.8.8 Read/Write Access Error Message

The read/write access error message is sent out when an system bus access error (read or write) has occurred.

Error information is messaged out in the following format:

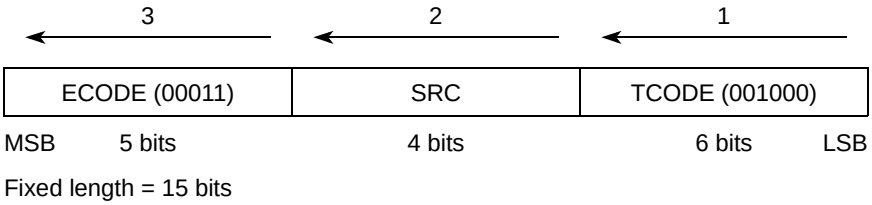


Figure 25-53. Error Message Format

25.14.9 Examples

The following are examples of program trace and data trace messages.

Table 25-40 illustrates an example indirect branch message with an 8 MDO and 2 MSEO configuration.

Note that T0 and S0 are the least significant bits where:

- Tx = TCODE number (fixed)
- Sx = Source processor (fixed)
- Ix = Number of instructions (variable)
- Ax = Unique portion of the address (variable)

Table 25-40. Indirect Branch Message Example (12 MDO and 2 MSEO)

Clock	MDO[11:0]												$\overline{\text{MSEO}}$[1:0]		State
	11	10	9	8	7	6	5	4	3	2	1	0			
0	X	X	X	X	X	X	X	X	X	X	X	X	1	1	Idle (or end of last message)
1	I1	I0	S3	S2	S1	S0	T5	T4	T3	T2	T1	T0	0	0	Start Message
2	0	0	0	0	0	0	0	0	I5	I4	I3	I2	0	1	End Packet
3	0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	1	1	End Packet/End Message
4	X	X	S3	S2	S1	S0	T5	T4	T3	T2	T1	T0	0	0	Start of Next Message

Table 25-41 illustrates an example of direct branch message with 12 MDO and 2 MSEO.

Note that T0 and I0 are the least significant bits where:

- Tx = TCODE number (fixed)
- Sx = Source processor (fixed)
- Ix = Number of instructions (variable)

Table 25-41. Direct Branch Message Example (12 MDO and 2 MSEO)

Clock	MDO[11:0]												$\overline{\text{MSEO}}$[1:0]		State
	11	10	9	8	7	6	5	4	3	2	1	0			
0	X	X	X	X	X	X	X	X	X	X	X	X	1	1	Idle (or end of last message)
1	I1	I0	S3	S2	S1	S0	T5	T4	T3	T2	T1	T0	0	0	Start Message
2	0	0	0	0	0	0	0	0	0	0	I3	I2	1	1	End Packet and End Message
3	X	X	X	X	S1	S0	T5	T4	T3	T2	T1	T0	0	0	Start of Next Message

Table 25-42 an example data write message with 12 MDO and two MSEO configuration.

T0, A0, D0 are the least significant bits (LSB) where:

- Tx = TCODE number (fixed)
- Sx = Source processor (fixed)
- Zx = Data size (fixed)
- Ax = Unique portion of the address (variable)
- Dx = Write data (variable: 8-, 16- or 32-bit)

Table 25-42. Direct Write Message Example (12 MDO and 2 $\overline{\text{MSEO}}$)

Clock	MDO[11:0]												MSEO[1:0]		State
	11	10	9	8	7	6	5	4	3	2	1	0			
0	X	X	X	X	X	X	X	X	X	X	X	X	1	1	Idle (or end of last message)
1	Z1	Z0	S3	S2	S1	S0	T5	T4	T3	T2	T1	T0	0	0	Start Message
2	0	0	0	0	0	0	0	A3	A2	A1	A0	Z2	0	1	End Packet
3	X	X	X	X	D7	D6	D5	D4	D3	D2	D1	D0	1	1	End Packet/End Message

25.14.10 IEEE® 1149.1 (JTAG) RD/WR Sequences

This section contains example JTAG/OnCE sequences used to access resources.

25.14.10.1 JTAG Sequence for Accessing Internal Nexus Registers

Table 25-43. Accessing Internal Nexus3 Registers via JTAG/OnCE

Step #	TMS Pin	Description
1	1	IDLE –> SELECT-DR_SCAN
2	0	SELECT-DR_SCAN –> CAPTURE-DR (Nexus command register value loaded in shifter)
3	0	CAPTURE-DR –> SHIFT-DR
4	0	(7) TCK clocks issued to shift in direction (read/write) bit and first 6 bits of Nexus reg. addr.
5	1	SHIFT-DR –> EXIT1-DR (7th bit of Nexus reg. shifted in)

Table 25-43. Accessing Internal Nexus3 Registers via JTAG/OnCE (continued)

Step #	TMS Pin	Description
6	1	EXIT1-DR –> UPDATE-DR (Nexus shifter is transferred to Nexus command register)
7	1	UPDATE-DR –> SELECT-DR_SCAN
8	0	SELECT-DR_SCAN –> CAPTURE-DR (Register value is transferred to Nexus shifter)
9	0	CAPTURE-DR –> SHIFT-DR
10	0	(31) TCK clocks issued to transfer register value to TDO pin while shifting in TDI value
11	1	SHIFT-DR –> EXIT1-DR (msb of value is shifted in/out of shifter)
12	1	EXIT1-DR –> UPDATE -DR (if access is write, shifter is transferred to register)
13	0	UPDATE-DR–> RUN-TEST/IDLE (transfer complete - Nexus controller to reg. select state)

25.14.10.2 JTAG Sequence for Read Access of Memory-Mapped Resources

Table 25-44. Accessing Memory-Mapped Resources (Reads)

Step #	TCLK clocks	Description
1	13	Nexus Command = write to read/write access address register (RWA)
2	37	Write RWA (initialize starting read address—data input on TDI)
3	13	Nexus Command = write to read/write control/status register (RWCS)
4	37	Write RWCS (initialize read access mode and CNT value—data input on TDI)
5	—	Wait for falling edge of RDY pin
6	13	Nexus Command = read the read/write access data register (RWD)
7	37	Read RWD (data output on TDO)
8	—	If CNT > 0, go back to Step #5

25.14.10.3 JTAG Sequence for Write Access of Memory-Mapped Resources

Table 25-45. Accessing Memory-Mapped Resources (Writes)

Step #	TCLK clocks	Description
1	13	Nexus Command = write to read/write access control/status register (RWCS)
2	37	Write RWCS (initialize write access mode and CNT value—data input on TDI)
3	13	Nexus Command = write to read/write address register (RWA)
4	37	Write RWA (initialize starting write address—data input on TDI)
5	13	Nexus Command = read the read/write access data register (RWD)
6	37	Write RWD (data output on TDO)
7	—	Wait for falling edge of RDY pin
8	—	If CNT > 0, go back to Step #5

25.15 Nexus Crossbar eDMA Interface (NXDM)

The third module of the device NDI interface is the e200z6 eDMA Nexus module (NXDM) which is compliant with the Class 3 defined data trace feature of the IEEE®-ISTO 5001-2003 standard. The NXDM can be programmed to trace data accesses for the eDMA module on the system bus. This eDMA module as well as the Nexus module are components of the e200z6 platform. All output messages and register accesses are compliant with the protocol defined in the IEEE®-ISTO 5001 standard.

NOTE

Throughout this section references are made to the auxiliary port and its specific signals, such as MCKO, MSEO[1:0], MDO[12:0] and others. In actual use the device NPC module arbitrates the access of the single auxiliary port. To simplify the description of the function of the NXDM module, the interaction of the NPC is omitted and the behavior described as if the module has its own dedicated auxiliary port. The auxiliary port function is fully described in Section 25.2, "External Signal Description."

25.15.1 Block Diagram

Figure 25-54 shows a block diagram of the NXDM.

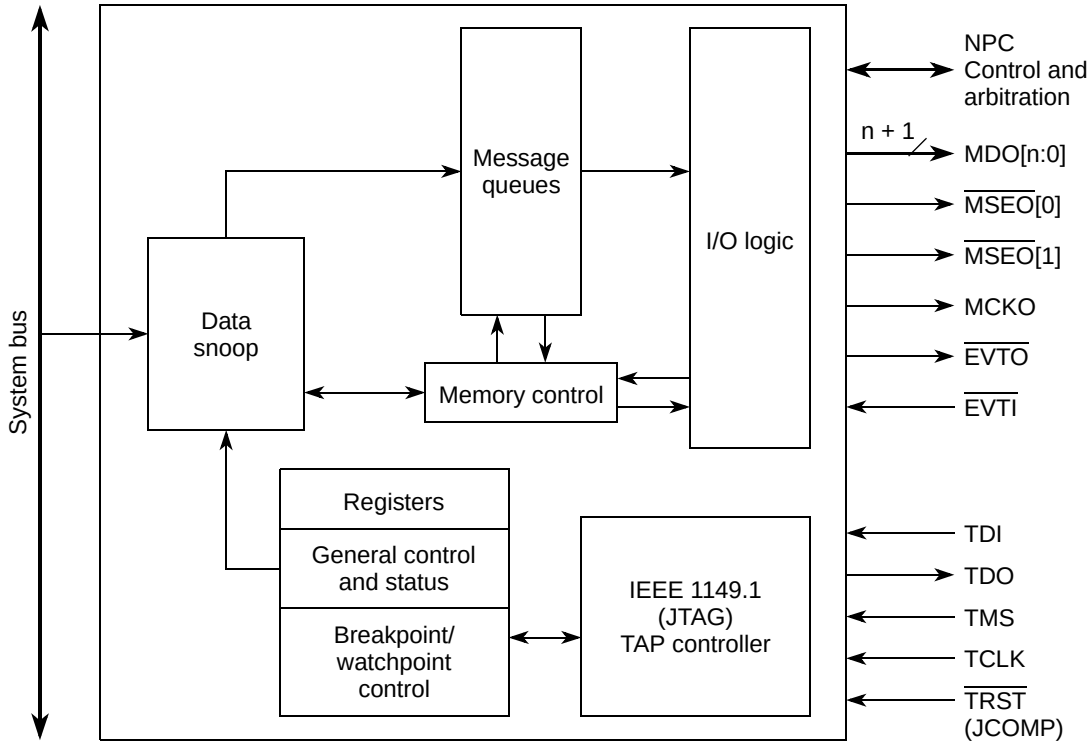


Figure 25-54. NXDM Block Diagram

25.15.2 Features

Features include the following:

- Data trace via data write messaging (DWM) and data read messaging (DRM). This provides the capability for the development tool to trace reads and/or writes through the eDMA module to (selected) internal memory resources.
- Watchpoint messaging via the auxiliary pins.
- Watchpoint trigger enable of data trace messaging (DTM).
- Registers for data trace, watchpoint generation, and watchpoint trigger.
- All features controllable and configurable via the JTAG port.
- Power management.
  - Low power design
  - Dynamic power management of FIFOs and control logic

25.16 External Signal Description

The NXDM module uses the same pins and pin protocol as defined in Section 25.2, “External Signal Description.”

25.16.1 Rules for Output Messages

The NXDM module observe the same rules for output messages as the NPC. Refer to Section 25.7.2.2.1, “Rules of Messages.”

25.16.2 Auxiliary Port Arbitration

The NXDM module arbitrate for the shared Nexus port. This arbitration is handled by the NPC (Refer to Section 25.5, “Nexus Port Controller (NPC)”) based on prioritized requests from the NXDM, and the other Nexus clients sharing the port.

25.17 NXDM Programmers Model

This section describes the programmers model. Nexus registers are accessed using the JTAG port in compliance with IEEE® 1149.1. Refer to Chapter 24, “IEEE 1149.1 Test Access Port Controller (JTAGC)” and Section 25.7.2.3, “IEEE, 1149.1-2001 (JTAG) TAP” for details on Nexus register access.

25.17.1 NXDM Nexus Register Map

Table 25-46. NXDM Register Map

Nexus Register	Nexus Access Opcode	Read/Write	Read Address	Write Address
Client Select Control (CSC) [1]	0x1	R	0x02	–
Port Configuration Register (PCR) [1]	Refer to NPC	R/W	–	–
Development Control 1 (DC1_*n*)	0x2	R/W	0x04	0x05
Development Control 2 (DC2_*n*)	0x3	R/W	0x05	0x06
Watchpoint Trigger (WT_*n*)	0xB	R/W	0x16	0x17
Data Trace Control (DTC_*n*)	0xD	R/W	0x1A	0x1B
Data Trace Start Address 1 (DTSA1_*n*)	0xE	R/W	0x1C	0x1D
Data Trace Start Address 2 (DTSA2_*n*)	0xF	R/W	0x1E	0x1F
Data Trace End Address 1 (DTEA1_*n*)	0x12	R/W	0x24	0x25
Data Trace End Address 2 (DTEA2_*n*)	0x13	R/W	0x26	0x27
Breakpoint/Watchpoint Control Register 1 (BWC1_*n*)	0x16	R/W	0x2C	0x2D
Breakpoint/Watchpoint Control Register 2 (BWC2_*n*)	0x17	R/W	0x2E	0x2F
Breakpoint/Watchpoint Address Register 1 (BWA1_*n*)	0x1E	R/W	0x3C	0x3D
Breakpoint/Watchpoint Address Register 2 (BWA2_*n*)	0x1F	R/W	0x3E	0x3F
Reserved	0x20–0x3F	–	0x40–0x7E	0x41–0x7F

[1] The CSC and PCR registers are shown in this table as part of the Nexus programmer's model. They are only present at the top level Nexus3 controller (NPC), not in the NXDM module. The device's CSC register is readable through Nexus3; the PCR is shown for reference only.

25.17.2 NXDM Registers

Detailed register definitions for the NXDM implementation are as follows:

25.17.2.1 Development Control Registers (DC1 and DC2)

The development control registers control the basic development features of the NXDM module.

Access: R/W

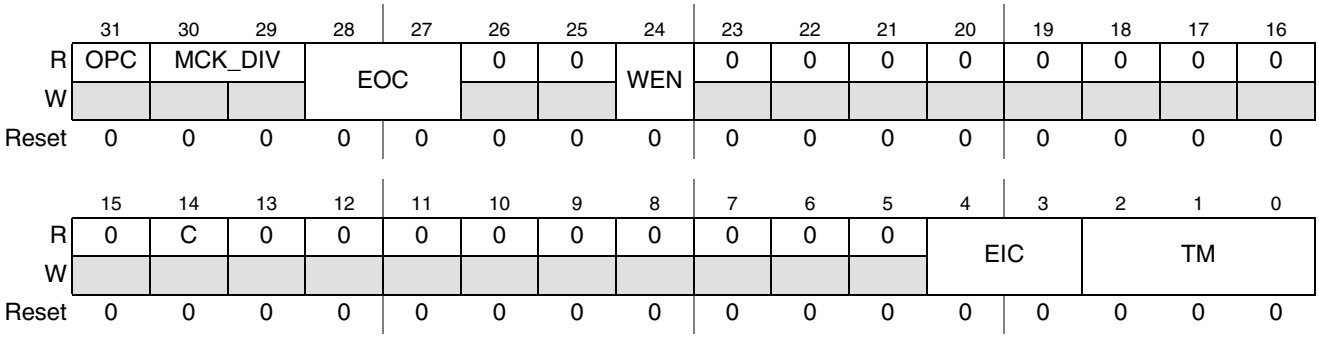


Figure 25-55. Development Control Register 1 (DC1)

Table 25-47. DC1 Field Description

Field	Description
31 OPC[1]	Output port mode control 0 Reduced port mode configuration 1 Full port mode configuration
30–29 MCK_DIV[1]	MCK_DIV - nexus message clock divide ratio 00 MCKO is 1x system bus clock frequency. 01 MCKO is 1/2x system bus clock frequency. 10 MCKO is 1/4x system bus clock frequency. 11 MCKO is 1/8x system bus clock frequency.
28–27 EOC	$\overline{\text{EVTO}}$ control 00 $\overline{\text{EVTO}}$ upon occurrence of watchpoint (internal or external) 01 $\overline{\text{EVTO}}$ upon entry into system-level debug mode (ipg_debug) 1X Reserved
26–25	Reserved, read as 0.
24 WEN	Watchpoint trace enable 0 Watchpoint messaging disabled 1 Watchpoint messaging enabled.
23–5	Reserved, read as 0.
4–3 EIC	$\overline{\text{EVTI}}$ control 00 $\overline{\text{EVTI}}$ for synchronization (Data Trace) 01 Reserved 10 $\overline{\text{EVTI}}$ disabled for this module 11 Reserved
2–0 TM	Trace mode 000 No Trace 1XX Reserved X1X Data trace enabled XX1 Reserved

[1] The output port mode control bit (OPC) and MCKO divide bits (MCK_DIV) are shown for clarity. These functions are controlled globally by the NPC port control register (PCR).

Access: R/W

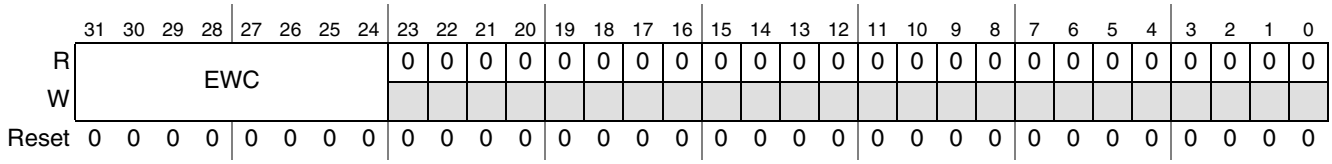


Figure 25-56. Development Control Register 2 (DC2)

Table 25-48. DC2 Field Description

Field	Description
31–24 EWC[1]	$\overline{\text{EVTO}}$ Watchpoint Configuration 00000000 = No watchpoints trigger $\overline{\text{EVTO}}$ 1XXXXXXX = Reserved X1XXXXXX = Reserved XX1XXXXX = Reserved XXX1XXXX = Reserved XXXX1XXX = Internal watchpoint #1 triggers $\overline{\text{EVTO}}$ XXXXX1XX = Internal watchpoint #2 triggers $\overline{\text{EVTO}}$ XXXXXX1X = Reserved XXXXXXX1 = Reserved
23–0	Reserved, read as 0.

[1] The EOC bits in DC1 must be programmed to trigger $\overline{\text{EVTO}}$ on watchpoint occurrence for the EWC bits to have any effect.

25.17.2.2 Watchpoint Trigger Register (WT)

The watchpoint trigger register allows the watchpoints defined internally to the NXDM modules to trigger actions. These watchpoints can control data trace enable and disable. The WT bits can be used to produce an address related window for triggering trace messages.

Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DTS		DTE				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-57. Watchpoint Trigger Register (WT)

Table 25-49. WT Field Description

Field	Description
31–26	Reserved, read as 0.
25–23 DTS	DTS - Data trace start control 000 Trigger disabled 001–100 Reserved 101 Use internal watchpoint #1 (BWA1 register) 110 Use internal watchpoint #2 (BWA2 register) 111 Reserved
22–20 DTE	DTE - Data trace end control 000 Trigger disabled 001–100 Reserved 101 Use internal watchpoint #1 (BWA1 register) 110 Use internal watchpoint #2 (BWA2 register) 111 Reserved
19–0	Reserved, read as 0.

NOTE

The WT bits ONLY enable data trace if the tm bits within the development control register (DC) have not already been set to enable data trace.

25.17.2.3 Data Trace Control Register (DTC)

The data trace control register controls whether DTM Messages are restricted to reads, writes or both for a user programmable address range. There are two data trace channels controlled by the DTC for the NXDM module.

Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RWT1		RWT2		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RC1	RC2	0	0	0	0	0	0
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-58. Data Trace Control Register (DTC)

Table 25-50. DTC Field Description

Bit	Description
31–30 RWT1	Read/write trace 1 00 No trace messages generated X1 Enable data read trace 1X Enable data write trace
29–28 RWT2	Read/write trace 2 00 No trace messages generated X1 Enable data read trace 1X Enable data write trace
27–8	Reserved, read as 0.
7 RC1	Range control 1 0 Condition trace on address within range (endpoints inclusive) 1 Condition trace on address outside of range (endpoints exclusive)
6 RC2	Range control 2 0 Condition trace on address within range (endpoints inclusive) 1 Condition trace on address outside of range (endpoints exclusive)
5–0	Reserved, read as 0.

25.17.2.4 Data Trace Start Address Registers 1 and 2 (DTSA1 and DTSA2)

The data trace start address registers define the start addresses for each trace channel.

Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	DATA TRACE START ADDRESS																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-59. Data Trace Start Address Registers (DTSA1, DTSA2)

25.17.2.5 Data Trace End Address Registers 1 and 2 (DTEA1 and DTEA2)

The data trace end address registers define the end addresses for each trace channel.

Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	DATA TRACE END ADDRESS																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-60. Data Trace Start Address Registers (DTEA1, DTEA2)

Table 25-51 illustrates the range that is selected for data trace for various cases of DTSA being less than, greater than, or equal to DTEA.

Table 25-51. Data Trace Address Range Options

Programmed Values	Range Control Bit Value	Range Selected
DTSA < or = DTEA	0	DTSA-> <-DTEA
DTSA < or = DTEA	1	<- DTSA DTEA ->
DTSA > DTEA	N/A	Invalid range, no trace

NOTE

DTSA must be less than (or equal to) DTEA to guarantee correct data write/read traces. When the range control bit is 0 (internal range), accesses to DTSA and DTEA addresses are traced. When the range control bit is 1 (external range), accesses to DTSA and DTEA are not traced.

25.17.2.6 Breakpoint / Watchpoint Control Register 1 (BWC1)

Breakpoint/watchpoint control register 1 controls attributes for generation of NXDM watchpoint number 1.

Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BWE1		BRW1												BWR1		BWT1															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-61. Break / Watchpoint Control Register 1 (BWC1)

Table 25-52. BWC1 Field Description

Field	Description
31–30 BWE1	Breakpoint/watchpoint #1 enable 00 Internal Nexus watchpoint #1 disabled 01–10 Reserved 11 Internal Nexus watchpoint #1 enabled
29–28 BRW1	Breakpoint/watchpoint #1 read/write select 00 Watchpoint #1 hit on read accesses 01 Watchpoint #1 hit on write accesses 10 Watchpoint #1 on read or write accesses 11 Reserved
27–18	Reserved, read as 0.
17–16 BWR1	Breakpoint/watchpoint #1 register compare 00 No register compare (same as BWC1[31:30] = 2'b00) 01 Reserved 10 Compare with BWA1 value 11 Reserved
15 BWT1	Breakpoint/watchpoint #1 type 0 Reserved 1 Watchpoint #1 on data accesses
14–0	Reserved, read as 0.

25.17.2.7 Breakpoint / Watchpoint Control Register 2 (BWC2)

Breakpoint/watchpoint control register2 controls attributes for generation of NXDM watchpoint number 2.

Access: R/W

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BWE2		BRW2												BWR2		BWT2															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 25-62. Break / Watchpoint Control Register 2 (BWC2)

Table 25-53. BWC2 Field Description

Field	Description
31–30 BWE2	Breakpoint/watchpoint #2 enable 00Internal Nexus watchpoint #2 disabled 01–10 Reserved 11 Internal Nexus watchpoint #2 enabled
29–28 BRW2	Breakpoint/watchpoint #2 read/write select 00 Watchpoint #2 hit on read accesses 01 Watchpoint #2 hit on write accesses 10 Watchpoint #2 on read or write accesses 11 Reserved
27–18	Reserved, read as 0.

Table 25-53. BWC2 Field Description (continued)

Field	Description
17–16 BWR2	Breakpoint/watchpoint #2 register compare 00 No register compare (same as BWC1[31:30] = 2'b00) 01 Reserved 10 Compare with BWA2 value 11 Reserved
15 BWT2	Breakpoint/watchpoint #2 Type 0 Reserved 1 Watchpoint #2 on data accesses
14–0	Reserved, read as 0.

25.17.2.8 Breakpoint/Watchpoint Address Registers 1 and 2 (BWA1 and BWA2)

The breakpoint/watchpoint address registers are compared with bus addresses to generate internal watchpoints.

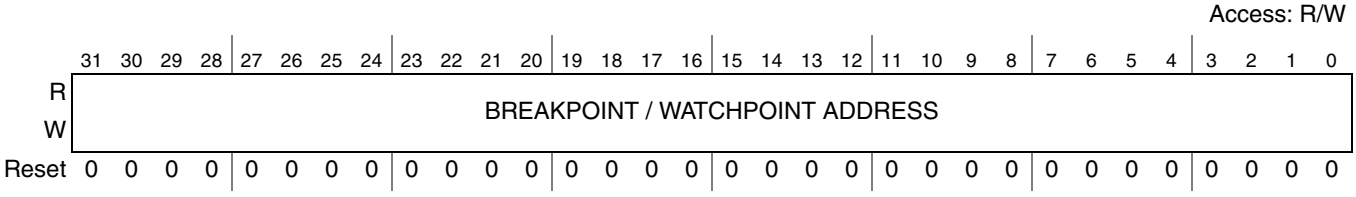


Figure 25-63. Breakpoint / Watchpoint Address Registers (BWA1, BWA2)

25.17.2.9 Unimplemented Registers

Unimplemented registers are those with client select and index value combinations other than those listed in Table 25-46. For unimplemented registers, the NXDM module drives TDO to zero during the "SHIFT-DR" state. It also transmits an error message with the invalid access opcode encoding.

25.17.2.10 Programming Considerations ($\overline{\text{RESET}}$)

If Nexus3 register configuration is to occur during system reset (as opposed to debug mode), all NXDM configuration should be completed between the negation of JCOMP and system reset de-assertion, after the JTAG DID register has been read by the tool.

25.17.2.11 IEEE® 1149.1 (JTAG) Test Access Port

The NXDM module uses the IEEE® 1149.1 TAP controller for accessing Nexus resources. The JTAG signals themselves are shared by all TAP controllers on the device. Refer to Chapter 24, "IEEE 1149.1 Test Access Port Controller (JTAGC) for more information on the JTAG interface.

The NXDM modules implements a 4-bit instruction register (IR). The valid instructions and method for register access are outlined in Section 25.7.2.3, "IEEE, 1149.1-2001 (JTAG) TAP."

25.17.2.11.1 NXDM JTAG DID Register

This JTAG DID register that is included in the NXDM module provides key development attributes to the development tool concerning the NXDM block. The register is accessed through the standard JTAG IR/DR paths. Refer to Chapter 23, “Voltage Regulator Controller (VRC) and POR Module.”

Access: R/W

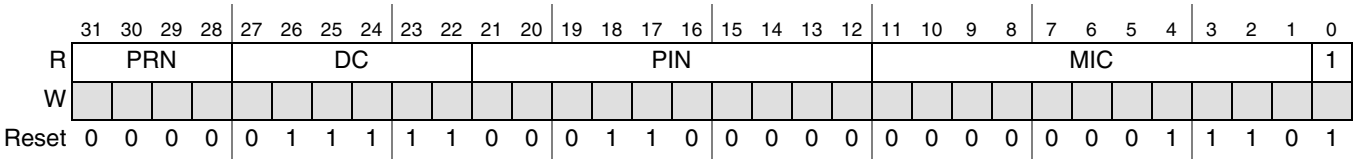


Figure 25-64. NXDM JTAG DID Register

Table 25-54. NXDM JTAG DID Field Descriptions

Field	Description
31–28 PRN[1]	Embedded part revision number (0x0)
27–22 DC	Freescale design center ID number (0x1F)
21–12 PIN	NXDM module part identification number, defines the features set. (0x60)
11–1 MIC	Manufacturer identity code 0x00E Freescale
0	Fixed per JTAG 1149.1 1 Always set

[1] The revision number is initially 0 and could change in the future.

25.17.2.11.2 Enabling the NXDM TAP Controller

Assertion of a power-on-reset signal or assertion of the JCOMP pin resets all TAP controllers on the device. Upon exit from the test-logic-reset state, the IR value is loaded with the JTAG DID. When the NXDM TAP is accessed, this information helps the development tool obtain information about the Nexus module it is accessing, such as version, sequence, feature set, and so forth.

25.17.2.11.3 NXDM Register Access via JTAG

Access to Nexus register resources is enabled by loading a single instruction (NEXUS_ACCESS) into the JTAG Instruction Register (IR). This IR is part of the IEEE® 1149.1 TAP controller within the NXDM modules. Refer to Section 24.4.4, “JTAGC Instructions.”

After the JTAG NEXUS_ACCESS instruction has been loaded, the JTAG port allows tool/target communications with all Nexus registers according to the map in Table 25-46.

Reading/writing of a Nexus register then requires two (2) passes through the data-scan (DR) path of the JTAG state machine (refer to Chapter 24, “IEEE 1149.1 Test Access Port Controller (JTAGC)”).

1. The first pass through the DR selects the Nexus register to be accessed by providing an index (refer to Table 25-46), and the direction (read/write). This is achieved by loading an 8-bit value into the JTAG data register (DR). This register has the following format:

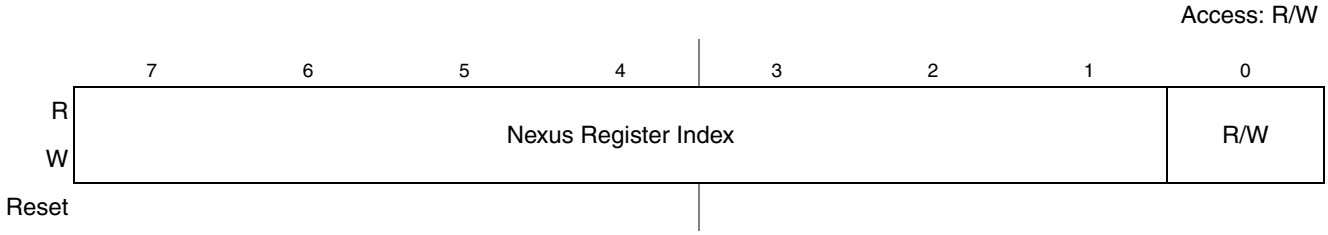


Figure 25-65. JTAG DR for NEXUS Register Access

Table 25-55. DR Read/Write Encoding

Nexus Register Index	Description
Read/Write (R/W)	0 Read 1 Write

2. The second pass through the DR then shifts the data in or out of the JTAG port, lsb first.
   a) During a read access, data is latched from the selected Nexus register when the JTAG state machine passes through the capture-DR state.
   b) During a write access, data is latched into the selected Nexus register when the JTAG state machine passes through the update-DR state.

25.17.3 Functional Description

25.17.4 Enabling NXDM Operation

The NXDM module is enabled by loading a single instruction (ACCESS_AUX_TAP_DMA as shown in Table 25-4) into the JTAG instruction register (IR), and then loading the corresponding OnCE OCMD register with the NEXUS_ACCESS instruction (refer to Table 25-5). After it is enabled, the module is ready to accept control input via the JTAG pins.

The Nexus module is disabled when the JTAG state machine reaches the test-logic-reset state. This state can be reached by the assertion of the JCOMP pin or by cycling through the state machine using the TMS pin. The Nexus module is also disabled if a power-on reset (POR) event occurs.

If the NXDM module is disabled, no trace output is provided, and the module disables (drive inactive) auxiliary port output pins (MDO[11:0], $\overline{\text{MSEO}}$[1:0], MCKO). Nexus registers are not be available for reads or writes.

25.17.5 TCODEs Supported by NXDM

The NXDM pins allow for flexible transfer operations via public messages. A TCODE defines the transfer format, the number and/or size of the packets to be transferred, and the purpose of each packet. The IEEE®-ISTO 5001-2003 standard defines a set of public messages. The NXDM block currently support the public TCODEs seen in Table 25-56.

Table 25-56. Public TCODEs Supported

Message Name	Packet Size Bits		Packet Name	Packet Type	Packet Description
	Min	Max			
Data Trace - Date Write Message	6	6	TCODE	Fixed	TCODE number = 5
	4	4	SRC	Fixed	Source processor identifier (multiple Nexus configuration)
	3	3	DSZ	Fixed	Data size (refer to Table 25-58)
	1	32	U-ADDR	Variable	Unique portion of the data write value
	1	64	DATA	Variable	Data write value
Data Trace - Data Read Message	6	6	TCODE	Fixed	TCODE number = 6
	4	4	SRC	Fixed	Source processor identifier (multiple Nexus configuration)
	3	3	DSZ	Fixed	Data size (refer to Table 25-58)
	1	32	U-ADDR	Variable	Unique portion of the data read value
	1	64	DATA	Variable	Data read value
Error Message	6	6	TCODE	Fixed	TCODE number = 8
	4	4	SRC	Fixed	Source processor identifier (multiple Nexus configuration)
	5	5	ECODE	Fixed	Error code (refer to Table 25-57)
Data Trace - Data Write Message w/ Sync	6	6	TCODE	Fixed	TCODE number = 13 (0xD)
	4	4	SRC	Fixed	Source processor identifier (multiple Nexus configuration)
	3	3	DSZ	Fixed	Data size (refer to Table 25-58)
	1	32	F-ADDR	Variable	Full access address (leading zero (0) truncated)
	1	64	DATA	Variable	Data write value
Data Trace - Data Read Message w/ Sync	6	6	TCODE	Fixed	TCODE number = 14 (0xE)
	4	4	SRC	Fixed	Source processor identifier (multiple Nexus configuration)
	3	3	DSZ	Fixed	Data size (refer to Table 25-58)
	1	32	F-ADDR	Variable	Full access address (leading zero (0) truncated)
	1	64	DATA	Variable	Data read valued
Watchpoint Message	6	6	TCODE	Fixed	TCODE number = 15 (0xF)
	4	4	SRC	Fixed	Source processor identifier (multiple Nexus configuration)
	4	4	WPHIT	Fixed	Number indicating watchpoint sources

Table 25-57. Error Code (ECODE) Encoding (TCODE = 8)

Error Code (ECODE)	Description
00000	Reserved
00001	Reserved
00010	Data Trace overrun
00011	Reserved
00100	Reserved
00101	Invalid access opcode (Nexus Register unimplemented)
00110	Watchpoint overrun
00111	Reserved
01000	Data Trace and Watchpoint overrun
01001–11111	Reserved

Table 25-58. Data Trace Size (DSZ) Encodings (TCODE = 5, 6, 13, 14)

DTM Size Encoding	Transfer Size
000	Byte
001	Halfword (two bytes)
010	Word (four bytes)
011	Doubleword (eight bytes)
100–111	Reserved

25.17.5.1 Data Trace

This section deals with the data trace mechanism supported by the NXDM module. Data trace is implemented via data write messaging (DWM) and data read messaging (DRM).

25.17.5.2 Data Trace Messaging (DTM)

NXDM data trace messaging is accomplished by snooping the NXDM data bus, and storing the information for qualifying accesses (based on enabled features and matching target addresses). The NXDM module traces all data access that meet the selected range and attributes.

NOTE

Data trace is ONLY performed on DMA accesses to the system bus.

25.17.5.3 DTM Message Formats

The NXDM block supports five types of DTM Messages — data write, data read, data write synchronization, data read synchronization and error messages.

25.17.5.3.1 Data Write and Data Read Messages

The data write and data read messages contain the data write/read value and the address of the write/read access, relative to the previous data trace message. Data write message and data read message information is messaged out in the following format:

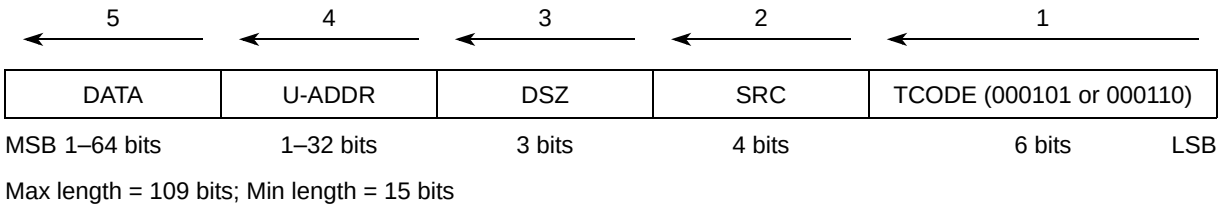


Figure 25-66. Data Write/Read Message Format

25.17.5.3.2 DTM Overflow Error Messages

An error message occurs when a new message cannot be queued due to the message queue being full. The FIFO discards incoming messages until it has completely emptied the queue. After it is emptied, an error message is queued. The error encoding indicates which types of messages attempted to be queued while the FIFO was being emptied.

If only a data trace message attempts to enter the queue while it is being emptied, the error message incorporates the data trace only error encoding (00010). If a watchpoint also attempts to be queued while the FIFO is being emptied, then the error message incorporates error encoding (01000).

Error information is messaged out in the following format:

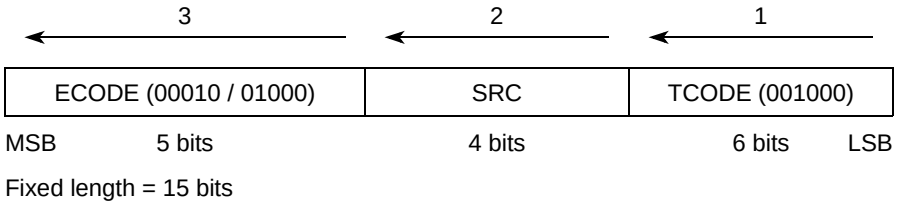


Figure 25-67. Error Message Format

25.17.5.3.3 Data Trace Synchronization Messages

A data trace write/read w/ sync. message is messaged via the auxiliary port (provided data trace is enabled) for the following conditions (refer to Table 25-59):

- Initial data trace message upon exit from system reset or whenever data trace is enabled is a synchronization message.
- Upon returning from a low power state, the first data trace message is a synchronization message.
- Upon returning from debug mode, the first data trace message is a synchronization message.
- After occurrence of queue overrun (can be caused by any trace message), the first data trace message is a synchronization message.
- After the periodic data trace counter has expired indicating 255 *without-sync* data trace messages have occurred since the last *with-sync* message occurred.
- Upon assertion of the Event In ($\overline{\text{EVTI}}$) pin, the first data trace message is a synchronization message if the eic bits of the dc register have enabled this feature.
- Upon data trace write/read after the previous dtm message was lost due to an attempted access to a secure memory location.
- Upon data trace write/read after the previous dtm message was lost due to a collision entering the fifo between the dtm message and any of the following: error message, or watchpoint message.

Data trace synchronization messages provide the full address (without leading zeros) and insure that development tools fully synchronize with data trace regularly. Synchronization messages provide a reference address for subsequent DTMs, in which only the unique portion of the data trace address is transmitted. The format for data trace write/read w/ sync. messages is as follows:

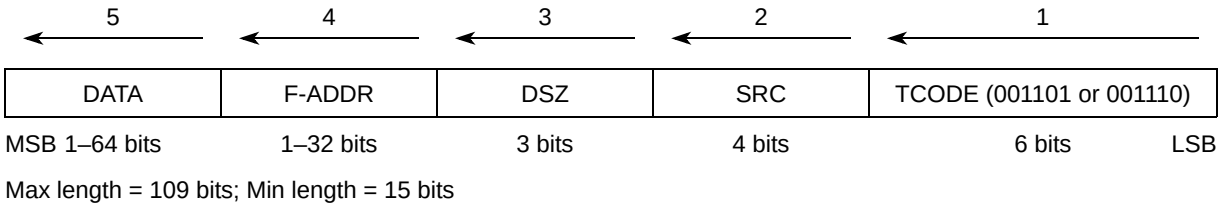


Figure 25-68. Data Write/Read w/ Sync Message Format

Exception conditions that result in data trace synchronization are summarized in Table 25-59., "Data Trace Exception Summary."

Table 25-59. Data Trace Exception Summary

Exception Condition	Exception Handling
System Reset Negation	At the negation of JTAG reset (JCOMP), queue pointers, counters, state machines, and registers within the NXDM module are reset. If data trace is enabled, the first data trace message is a data write/read w/ sync. message.
Data Trace Enabled	The first data trace message (after data trace has been enabled) is a synchronization message.
Exit from Low Power/Debug	Upon exit from a low power mode or debug mode the next data trace message is converted to a data write/read w/ sync. message.
Queue Overrun	An error message occurs when a new message cannot be queued due to the message queue being full. The FIFO discards messages until it has completely emptied the queue. After it is emptied, an error message is queued. The error encoding indicates the types of messages that attempted to be queued while the FIFO was being emptied. The next DTM message in the queue is a data write/read w/ sync. message.
Periodic Data Trace Synchronization	A forced synchronization occurs periodically after 255 data trace messages have been queued. A data write/read w/ sync. message is queued. The periodic data trace message counter then resets.
Event In	If the nexus module is enabled, an $\overline{\text{EVTI}}$ assertion initiates a data trace write/read w/ sync. message upon the next data write/read (if data trace is enabled and the eic bits of the dc register have enabled this feature).
Attempted Access to Secure Memory	Any attempted read or write to secure memory locations temporarily disable data trace & cause the corresponding DTM to be lost. A subsequent read/write queues a data trace read/write with sync. message.
Collision Priority	All messages have the following priority: Error -> WPM -> DTM. A DTM message which attempts to enter the queue at the same time as an error message, or watchpoint message is lost. A subsequent read/write queues a data trace read/write with sync. message.

25.17.5.4 DTM Operation

25.17.5.4.1 Enabling Data Trace Messaging

Data trace messaging can be enabled in one of two ways.

- Setting the DC1[TM] field to enable data trace
- Using the WT[DTS] field to enable data trace on watchpoint hits

25.17.5.4.2 DTM Queueing

NXDM implements a programmable depth queue for queuing all messages. Messages that enter the queue are transmitted via the auxiliary pins in the order in which they are queued.

NOTE

If multiple trace messages must be queued at the same time, watchpoint messages have the highest priority (WPM -> DTM).

25.17.5.4.3 Relative Addressing

The relative address feature is compliant with IEEE®-ISTO Nexus 5001-2003 and is designed to reduce the number of bits transmitted for addresses of data trace messages. Relative addressing is the same as described for the NZ6C3 in Section 25.14.2, “ Relative Addressing.”

25.17.5.4.4 Data Trace Windowing

Data write/read messages are enabled via the RWT1(2) field in the data trace control register (DTC) for each DTM channel. Data trace windowing is achieved via the address range defined by the DTEA and DTSA registers and by the RC1(2) field in the DTC. All eDMA initiated read/write accesses that fall inside or outside these address ranges, as programmed, are candidates to be traced.

25.17.5.4.5 System Bus Cycle Special Cases

Table 25-60. System Bus Cycle Special Cases

Special Case	Action
System bus cycle aborted (DABORT asserted)	Cycle ignored
System bus cycle with data error	Data Trace Message discarded
System bus cycle completed without error	Cycle captured and transmitted
System bus cycle is an instruction fetch	Cycle ignored

25.17.5.5 Data Trace Timing Diagrams (Eight MDO configuration)

Data trace timing for the NXDM is the same as for the NZ6C3. Refer to Section 25.14.6.4, “ Data Trace Timing Diagrams (Eight MDO Configuration).”

25.17.6 Watchpoint Support

The NXDM module provides watchpoint messaging via the auxiliary pins, as defined by IEEE®-ISTO 5001-2003.

Watchpoint messages can be generated using the NXDM defined internal watchpoints.

25.17.6.1 Watchpoint Messaging

Enabling watchpoint messaging is accomplished by setting the watchpoint messaging enable bit, DC1[WEN]. Using the BWC1 and BWC2 registers, two independently controlled internal watchpoints can be initialized. When a DMA access address matches on BWA1 or BWA2, a watchpoint message is transmitted.

The Nexus module provides watchpoint messaging using the TCODE. When either of the two possible watchpoint sources asserts, a message is sent to the queue to be messaged out. This message indicates the watchpoint number.

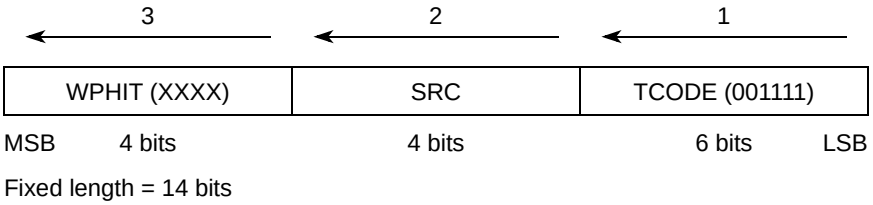


Figure 25-69. Watchpoint Message Format

Table 25-61. Watchpoint Source Description

Watchpoint Source (4 bits)	Watchpoint Description
XXX1	Reserved
XX1X	Reserved
X1XX	Internal Watchpoint #1 (BWA1 match)
1XXX	Internal Watchpoint #2 (BWA2 match)

25.17.6.2 Watchpoint Error Message

An error message occurs when a new message cannot be queued due to the message queue being full. The FIFO discards messages until it has completely emptied the queue. After it is emptied, an error message is queued. The error encoding indicates which types of messages attempted to be queued while the FIFO was being emptied.

If only a watchpoint message attempts to enter the queue while it is being emptied, the error message incorporates the watchpoint only error encoding (00110). If a data trace message also attempts to enter the queue while it is being emptied, the error message incorporates error encoding (01000).

Error information is messaged out in the following format (refer to Figure 25-70).

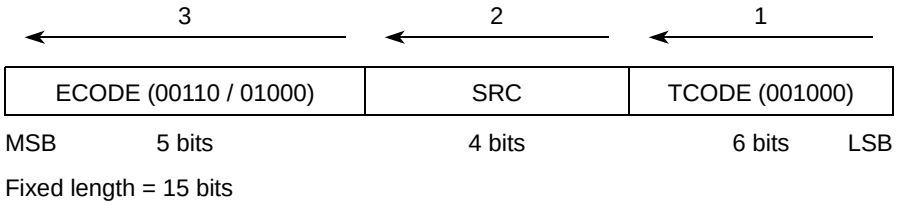


Figure 25-70. Error Message Format

Appendix A
MPC5566 Register Map

A.1 Base Addresses of the Device Modules

The following table lists the base address and the page link to the device modules:

Table A-1. Module Base Addresses

Module	Base Address	Page
Peripheral Bridge A (PBRIDGEA)	0xC3F0_0000	Page A-2
Frequency Modulated Phase-Locked Loop (FMPLL)	0xC3F8_0000	Page A-2
External Bus Interface (EBI)	0xC3F8_4000	Page A-2
Flash Module and Flash Bus Interface Unit (FLASH)	0xC3F8_8000	Page A-3
System Integration Unit (SIU)	0xC3F9_0000	Page A-3
Enhanced Modular Input/Output Subsystem (eMIOS)	0xC3FA_0000	Page A-25
Enhanced Time Processing Unit (eTPU)	0xC3FC_0000	Page A-26
Peripheral Bridge B (PBRIDGEB)	0xFFF0_0000	Page A-35
System Bus Crossbar Switch (XBAR)	0xFFF0_4000	Page A-36
Error Correction Status Module (ECSM)	0xFFF4_0000	Page A-36
Enhanced Direct Memory Access (eDMA)	0xFFF4_4000	Page A-37
Interrupt Controller (INTC)	0xFFF4_8000	Page A-42
Fast Ethernet Controller (FEC)	0xFFF4_C000	Page A-52
Enhanced Queued Analog-to-Digital Converter (eQADC)	0xFFF8_0000	Page A-53
Deserial / Serial Peripheral Interface (DSPIx)	0xFFF9_0000 (DSPI A) 0xFFF9_4000 (DSPI B) 0xFFF9_8000 (DSPI C) 0xFFF9_C000 (DSPI D)	Page A-57
Enhanced Serial Communication Interface (eSCIx)	0xFFFB_0000 (A) 0xFFFB_4000 (B)	Page A-58
FlexCAN2 Controller Area Network (CANx)	0xFFFC_0000 (FlexCAN A) 0xFFFC_4000 (FlexCAN B) 0xFFFC_8000 (FlexCAN C) 0xFFFC_C000 (FlexCAN D)	Page A-58
Boot Assist Module (BAM)	0xFFFF_C000	Page A-60

A.2 MPC5566 Register Map

The following table shows a detailed list of the MPC5566 register map:

Table A-2. MPC5566 Detailed Register Map

Register Description	Register Name	Used Size	Address
Peripheral Bridge A (PBRIDGEA) Chapter 5, "Peripheral Bridge (PBRIDGE A and PBRIDGE B)"			0xC3F0_0000
Peripheral bridge A master privilege control register	PBRIDGEA_MPCR	32-bit	Base + 0x0000
Reserved	—	—	Base + (0x0004–0x001F)
Peripheral bridge A peripheral access control register 0	PBRIDGEA_PACR0	32-bit	Base + 0x0020
Reserved	—	—	Base + (0x0024–0x003F)
Peripheral bridge A off-platform peripheral access control register 0	PBRIDGEA_OPACR0	32-bit	Base + 0x0040
Peripheral bridge A off-platform peripheral access control register 1	PBRIDGEA_OPACR1	32-bit	Base + 0x0044
Peripheral bridge A off-platform peripheral access control register 2	PBRIDGEA_OPACR2	32-bit	Base + 0x0048
Reserved	—	—	Base + 0x004C–0xC3F7_FFFF
Frequency Modulated Phase-Locked Loop (FMPLL) Chapter 11, "Frequency Modulated Phase Locked Loop and System Clocks (FMPLL)"			0xC3F8_0000
Synthesizer control register	FMPLL_SYNCR	32-bit	Base + 0x0000
Synthesizer status register	FMPLL_SYNSR	32-bit	Base + 0x0004
Reserved	—	—	Base + 0x0008–0xC3F8_3FFF
External Bus Interface (EBI) Chapter 12, "External Bus Interface (EBI)			0xC3F8_4000
Module configuration register	EBI_MCR	32-bit	Base + 0x0000
Reserved	—	—	Base + (0x0004–0x0007)
Transfer error status register	EBI_TESR	32-bit	Base + 0x0008
Bus monitor control register	EBI_BMCR	32-bit	Base + 0x000C
Base register bank 0	EBI_BR0	32-bit	Base + 0x0010
Option register bank 0	EBI_OR0	32-bit	Base + 0x0014
Base register bank 1	EBI_BR1	32-bit	Base + 0x0018
Option register bank 1	EBI_OR1	32-bit	Base + 0x001C
Base register bank 2	EBI_BR2	32-bit	Base + 0x0020
Option register bank 2	EBI_OR2	32-bit	Base + 0x0024
Base register bank 3	EBI_BR3	32-bit	Base + 0x0028

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Option register bank 3	EBI_OR3	32-bit	Base + 0x002C
Calibration base register bank 0	EBI_CAL_BR0	32-bit	Base + 0x0040
Calibration option register bank 0	EBI_CAL_OR0	32-bit	Base + 0x0044
Calibration base register bank 1	EBI_CAL_BR1	32-bit	Base + 0x0048
Calibration option register bank 1	EBI_CAL_OR1	32-bit	Base + 0x004C
Calibration base register bank 2	EBI_CAL_BR2	32-bit	Base + 0x0050
Calibration option register bank 2	EBI_CAL_OR2	32-bit	Base + 0x0054
Calibration base register bank 3	EBI_CAL_BR3	32-bit	Base + 0x0058
Calibration option register bank 3	EBI_CAL_OR3	32-bit	Base + 0x005C
Flash Module and Flash Bus Interface Unit (FLASH) Chapter 13, “Flash Memory”			0xC3F8_8000
Module configuration register	FLASH_MCR	32-bit	Base + 0x0000
Low/mid address space block locking register	FLASH_LMLR	32-bit	Base + 0x0004
High address space block locking register	FLASH_HLR	32-bit	Base + 0x0008
Secondary low/mid address space block locking register	FLASH_SLMLR	32-bit	Base + 0x000C
Low/mid address block select register	FLASH_LMSR	32-bit	Base + 0x0010
High address space block select register	FLASH_HSR	32-bit	Base + 0x0014
Address register	FLASH_AR	32-bit	Base + 0x0018
Bus interface unit control register	FLASH_BIUCR	32-bit	Base + 0x001C
Bus interface unit access protection register	FLASH_BIUAPR	32-bit	Base + 0x0020
Reserved	—	—	Base + (0x0024–0xC3F8_FFFF)
System Integration Unit (SIU) Chapter 6, “System Integration Unit (SIU)”			0xC3F9_0000
MCU ID Register	SIU_MIDR		Base + 0x0004
Reserved	—	—	Base + (0x0008–0x000B)
Reset status register	SIU_RSR		Base + 0x000C
System reset control register	SIU_SRCR		Base + 0x0010
External interrupt status register	SIU_EISR		Base + 0x0014
DMA / Interrupt request enable register	SIU_DIRER		Base + 0x0018
DMA / Interrupt request status register	SIU_DIRSR		Base + 0x001C
Overrun status register	SIU_OSR		Base + 0x0020
Overrun request enable register	SIU_ORER		Base + 0x0024

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
IRQ rising-edge event enable register	SIU_IREER		Base + 0x0028
IRQ falling-edge event enable register	SIU_IFEER		Base + 0x002C
IRQ digital filter register	SIU_IDFR		Base + 0x0030
Reserved	—	—	Base + (0x0034–0x003F)
Pad configuration register 0 ($\overline{CS}$[0])	SIU_PCR0	16-bits	Base + 0x0040
Pad configuration register 1 ($\overline{CS}$[1])	SIU_PCR1	16-bits	Base + 0x0042
Pad configuration register 2 ($\overline{CS}$[2])	SIU_PCR2	16-bits	Base + 0x0044
Pad configuration register 3 ($\overline{CS}$[3])	SIU_PCR3	16-bits	Base + 0x0046
Pad configuration register 4 (ADDR[8])	SIU_PCR4	16-bits	Base + 0x0048
Pad configuration register 5 (ADDR[9])	SIU_PCR5	16-bits	Base + 0x004A
Pad configuration register 6 (ADDR[10])	SIU_PCR6	16-bits	Base + 0x004C
Pad configuration register 7 (ADDR[11])	SIU_PCR7	16-bits	Base + 0x004E
Pad configuration register 8 (ADDR[12])	SIU_PCR8	16-bits	Base + 0x0050
Pad configuration register 9 (ADDR[13])	SIU_PCR9	16-bits	Base + 0x0052
Pad configuration register 10 (ADDR[14])	SIU_PCR10	16-bits	Base + 0x0054
Pad configuration register 11 (ADDR[15])	SIU_PCR11	16-bits	Base + 0x0056
Pad configuration register 12 (ADDR[16])	SIU_PCR12	16-bits	Base + 0x0058
Pad configuration register 13 (ADDR[17])	SIU_PCR13	16-bits	Base + 0x005A
Pad configuration register 14 (ADDR[18])	SIU_PCR14	16-bits	Base + 0x005C
Pad configuration register 15 (ADDR[19])	SIU_PCR15	16-bits	Base + 0x005E
Pad configuration register 16 (ADDR[20])	SIU_PCR16	16-bits	Base + 0x0060
Pad configuration register 17 (ADDR[21])	SIU_PCR17	16-bits	Base + 0x0062
Pad configuration register 18 (ADDR[22])	SIU_PCR18	16-bits	Base + 0x0064
Pad configuration register 19 (ADDR[23])	SIU_PCR19	16-bits	Base + 0x0066
Pad configuration register 20 (ADDR[24])	SIU_PCR20	16-bits	Base + 0x0068
Pad configuration register 21 (ADDR[25])	SIU_PCR21	16-bits	Base + 0x006A
Pad configuration register 22 (ADDR[26])	SIU_PCR22	16-bits	Base + 0x006C
Pad configuration register 23 (ADDR[27])	SIU_PCR23	16-bits	Base + 0x006E
Pad configuration register 24 (ADDR[28])	SIU_PCR24	16-bits	Base + 0x0070
Pad configuration register 25 (ADDR[29])	SIU_PCR25	16-bits	Base + 0x0072
Pad configuration register 26 (ADDR[30])	SIU_PCR26	16-bits	Base + 0x0074
Pad configuration register 27 (ADDR[31])	SIU_PCR27	16-bits	Base + 0x0076

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Pad configuration register 28 (DATA[0])	SIU_PCR28	16-bits	Base + 0x0078
Pad configuration register 29 (DATA[1])	SIU_PCR29	16-bits	Base + 0x007A
Pad configuration register 30 (DATA[2])	SIU_PCR30	16-bits	Base + 0x007C
Pad configuration register 31 (DATA[3])	SIU_PCR31	16-bits	Base + 0x007E
Pad configuration register 32 (DATA[4])	SIU_PCR32	16-bits	Base + 0x0080
Pad configuration register 33 (DATA[5])	SIU_PCR33	16-bits	Base + 0x0082
Pad configuration register 34 (DATA[6])	SIU_PCR34	16-bits	Base + 0x0084
Pad configuration register 35 (DATA[7])	SIU_PCR35	16-bits	Base + 0x0086
Pad configuration register 36 (DATA[8])	SIU_PCR36	16-bits	Base + 0x0088
Pad configuration register 37 (DATA[9])	SIU_PCR37	16-bits	Base + 0x008A
Pad configuration register 38 (DATA[10])	SIU_PCR38	16-bits	Base + 0x008C
Pad configuration register 39 (DATA[11])	SIU_PCR39	16-bits	Base + 0x008E
Pad configuration register 40 (DATA[12])	SIU_PCR40	16-bits	Base + 0x0090
Pad configuration register 41 (DATA[13])	SIU_PCR41	16-bits	Base + 0x0092
Pad configuration register 42 (DATA[14])	SIU_PCR42	16-bits	Base + 0x0094
Pad configuration register 43 (DATA[15])	SIU_PCR43	16-bits	Base + 0x0096
Pad configuration register 44 (DATA[16])	SIU_PCR44	16-bits	Base + 0x0098
Pad configuration register 45 (DATA[17])	SIU_PCR45	16-bits	Base + 0x009A
Pad configuration register 46 (DATA[18])	SIU_PCR46	16-bits	Base + 0x009C
Pad configuration register 47 (DATA[19])	SIU_PCR47	16-bits	Base + 0x009E
Pad configuration register 48 (DATA[20])	SIU_PCR48	16-bits	Base + 0x00A0
Pad configuration register 49 (DATA[21])	SIU_PCR49	16-bits	Base + 0x00A2
Pad configuration register 50 (DATA[22])	SIU_PCR50	16-bits	Base + 0x00A4
Pad configuration register 51 (DATA[23])	SIU_PCR51	16-bits	Base + 0x00A6
Pad configuration register 52 (DATA[24])	SIU_PCR52	16-bits	Base + 0x00A8
Pad configuration register 53 (DATA[25])	SIU_PCR53	16-bits	Base + 0x00AA
Pad configuration register 54 (DATA[26])	SIU_PCR54	16-bits	Base + 0x00AC
Pad configuration register 55 (DATA[27])	SIU_PCR55	16-bits	Base + 0x00AE
Pad configuration register 56 (DATA[28])	SIU_PCR56	16-bits	Base + 0x00B0
Pad configuration register 57 (DATA[29])	SIU_PCR57	16-bits	Base + 0x00B2
Pad configuration register 58 (DATA[30])	SIU_PCR58	16-bits	Base + 0x00B4
Pad configuration register 59 (DATA[31])	SIU_PCR59	16-bits	Base + 0x00B6

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Pad configuration register 60 (TSIZ[0])	SIU_PCR60	16-bits	Base + 0x00B8
Pad configuration register 61 (TSIZ[1])	SIU_PCR61	16-bits	Base + 0x00BA
Pad configuration register 62 (RD_$\overline{WR}$)	SIU_PCR62	16-bits	Base + 0x00BC
Pad configuration register 63 ($\overline{BDIP}$)	SIU_PCR63	16-bits	Base + 0x00BE
Pad configuration register 64 ($\overline{WE}$/$\overline{BE}$[0])	SIU_PCR64	16-bits	Base + 0x00C0
Pad configuration register 65 ($\overline{WE}$/$\overline{BE}$[1])	SIU_PCR65	16-bits	Base + 0x00C2
Pad configuration register 66 ($\overline{WE}$/$\overline{BE}$[2])	SIU_PCR66	16-bits	Base + 0x00C4
Pad configuration register 67 ($\overline{WE}$/$\overline{BE}$[3])	SIU_PCR67	16-bits	Base + 0x00C6
Pad configuration register 68 ($\overline{OE}$)	SIU_PCR68	16-bits	Base + 0x00C8
Pad configuration register 69 ($\overline{TS}$)	SIU_PCR69	16-bits	Base + 0x00CA
Pad configuration register 70 ($\overline{TA}$)	SIU_PCR70	16-bits	Base + 0x00CC
Pad configuration register 71 ($\overline{TEA}$)	SIU_PCR71	16-bits	Base + 0x00CE
Pad configuration register 72 ($\overline{BR}$)	SIU_PCR72	16-bits	Base + 0x00D0
Pad configuration register 73 ($\overline{BG}$)	SIU_PCR73	16-bits	Base + 0x00D2
Pad configuration register 74 ($\overline{BB}$)	SIU_PCR74	16-bits	Base + 0x00D4
Pad configuration register 75 (MDO[4])	SIU_PCR75	16-bits	Base + 0x00D6
Pad configuration register 76 (MDO[5])	SIU_PCR76	16-bits	Base + 0x00D8
Pad configuration register 77 (MDO[6])	SIU_PCR77	16-bits	Base + 0x00DA
Pad configuration register 78 (MDO[7])	SIU_PCR78	16-bits	Base + 0x00DC
Pad configuration register 79 (MDO[8])	SIU_PCR79	16-bits	Base + 0x00DE
Pad configuration register 80 (MDO[9])	SIU_PCR80	16-bits	Base + 0x00E0
Pad configuration register 81 (MDO[10])	SIU_PCR81	16-bits	Base + 0x00E2
Pad configuration register 82 (MDO[11])	SIU_PCR82	16-bits	Base + 0x00E4
Pad configuration register 83 (CNTXA)	SIU_PCR83	16-bits	Base + 0x00E6
Pad configuration register 84 (CNRXA)	SIU_PCR84	16-bits	Base + 0x00E8
Pad configuration register 85 (CNTXB)	SIU_PCR85	16-bits	Base + 0x00EA
Pad configuration register 86 (CNRXB)	SIU_PCR86	16-bits	Base + 0x00EC
Pad configuration register 87 (CNTXC)	SIU_PCR87	16-bits	Base + 0x00EE
Pad configuration register 88 (CNRXC)	SIU_PCR88	16-bits	Base + 0x00F0
Pad configuration register 89 (TXDA)	SIU_PCR89	16-bits	Base + 0x00F2
Pad configuration register 90 (RXDA)	SIU_PCR90	16-bits	Base + 0x00F4
Pad configuration register 91 (TXDB)	SIU_PCR91	16-bits	Base + 0x00F6

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Pad configuration register 92 (RXDB)	SIU_PCR92	16-bits	Base + 0x00F8
Pad configuration register 93 (SCKA)	SIU_PCR93	16-bits	Base + 0x00FA
Pad configuration register 94 (SINA)	SIU_PCR94	16-bits	Base + 0x00FC
Pad configuration register 95 (SOUTA)	SIU_PCR95	16-bits	Base + 0x00FE
Pad configuration register 96 (PCSA[0])	SIU_PCR96	16-bits	Base + 0x0100
Pad configuration register 97 (PCSA[1])	SIU_PCR97	16-bits	Base + 0x0102
Pad configuration register 98 (PCSA[2])	SIU_PCR98	16-bits	Base + 0x0104
Pad configuration register 99 (PCSA[3])	SIU_PCR99	16-bits	Base + 0x0106
Pad configuration register 100 (PCSA[4])	SIU_PCR100	16-bits	Base + 0x0108
Pad configuration register 101 (PCSA[5])	SIU_PCR101	16-bits	Base + 0x010A
Pad configuration register 102 (SCKB)	SIU_PCR102	16-bits	Base + 0x010C
Pad configuration register 103 (SINB)	SIU_PCR103	16-bits	Base + 0x010E
Pad configuration register 104 (SOUTB)	SIU_PCR104	16-bits	Base + 0x0110
Pad configuration register 105 (PCSB[0])	SIU_PCR105	16-bits	Base + 0x0112
Pad configuration register 106 (PCSB[1])	SIU_PCR106	16-bits	Base + 0x0114
Pad configuration register 107 (PCSB[2])	SIU_PCR107	16-bits	Base + 0x0116
Pad configuration register 108 (PCSB[3])	SIU_PCR108	16-bits	Base + 0x0118
Pad configuration register 109 (PCSB[4])	SIU_PCR109	16-bits	Base + 0x011A
Pad configuration register 110 (PCSB[5])	SIU_PCR110	16-bits	Base + 0x011C
Pad configuration register 111 (ETRIG[0])	SIU_PCR111	16-bits	Base + 0x011E
Pad configuration register 112 (ETRIG[1])	SIU_PCR112	16-bits	Base + 0x0120
Pad configuration register 113 (TCRCLKA)	SIU_PCR113	16-bits	Base + 0x0122
Pad configuration register 114 (eTPU A[0])	SIU_PCR114	16-bits	Base + 0x0124
Pad configuration register 115 (eTPU A[1])	SIU_PCR115	16-bits	Base + 0x0126
Pad configuration register 116 (eTPU A[2])	SIU_PCR116	16-bits	Base + 0x0128
Pad configuration register 117 (eTPU A[3])	SIU_PCR117	16-bits	Base + 0x012A
Pad configuration register 118 (eTPU A[4])	SIU_PCR118	16-bits	Base + 0x012C
Pad configuration register 119 (eTPU A[5])	SIU_PCR119	16-bits	Base + 0x012E
Pad configuration register 120 (eTPU A[6])	SIU_PCR120	16-bits	Base + 0x0130
Pad configuration register 121 (eTPU A[7])	SIU_PCR121	16-bits	Base + 0x0132
Pad configuration register 122 (eTPU A[8])	SIU_PCR122	16-bits	Base + 0x0134
Pad configuration register 123 (eTPU A[[]9)	SIU_PCR123	16-bits	Base + 0x0136

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Pad configuration register 124 (eTPU A[10])	SIU_PCR124	16-bits	Base + 0x0138
Pad configuration register 125 (eTPU A[11])	SIU_PCR125	16-bits	Base + 0x013A
Pad configuration register 126 (eTPU A[12])	SIU_PCR126	16-bits	Base + 0x013C
Pad configuration register 127 (eTPU A[13])	SIU_PCR127	16-bits	Base + 0x013E
Pad configuration register 128 (eTPU A[14])	SIU_PCR128	16-bits	Base + 0x0140
Pad configuration register 129 (eTPU A[15])	SIU_PCR129	16-bits	Base + 0x0142
Pad configuration register 130 (eTPU A[16])	SIU_PCR130	16-bits	Base + 0x0144
Pad configuration register 131 (eTPU A[17])	SIU_PCR131	16-bits	Base + 0x0146
Pad configuration register 132 (eTPU A[18])	SIU_PCR132	16-bits	Base + 0x0148
Pad configuration register 133 (eTPU A[19])	SIU_PCR133	16-bits	Base + 0x014A
Pad configuration register 134 (eTPU A[20])	SIU_PCR134	16-bits	Base + 0x014C
Pad configuration register 135 (eTPU A[21])	SIU_PCR135	16-bits	Base + 0x014E
Pad configuration register 136 (eTPU A[22])	SIU_PCR136	16-bits	Base + 0x0150
Pad configuration register 137 (eTPU A[23])	SIU_PCR137	16-bits	Base + 0x0152
Pad configuration register 138 (eTPU A[24])	SIU_PCR138	16-bits	Base + 0x0154
Pad configuration register 139 (eTPU A[25])	SIU_PCR139	16-bits	Base + 0x0156
Pad configuration register 140 (eTPU A[26])	SIU_PCR140	16-bits	Base + 0x0158
Pad configuration register 141 (eTPU A[27])	SIU_PCR141	16-bits	Base + 0x015A
Pad configuration register 142 (eTPU A[28])	SIU_PCR142	16-bits	Base + 0x015C
Pad configuration register 143 (eTPU A[29])	SIU_PCR143	16-bits	Base + 0x015E
Pad configuration register 144 (eTPU A[30])	SIU_PCR144	16-bits	Base + 0x0160
Pad configuration register 145 (eTPU A[31])	SIU_PCR145	16-bits	Base + 0x0162
Pad configuration register 146 (TCRCLKB)	SIU_PCR146	16-bits	Base + 0x0164
Pad configuration register 147 (eTPU B[0])	SIU_PCR147	16-bits	Base + 0x0166
Pad configuration register 148 (eTPU B[1])	SIU_PCR148	16-bits	Base + 0x0168
Pad configuration register 149 (eTPU B[2])	SIU_PCR149	16-bits	Base + 0x016A
Pad configuration register 150 (eTPU B[3])	SIU_PCR150	16-bits	Base + 0x016C
Pad configuration register 151 (eTPU B[4])	SIU_PCR151	16-bits	Base + 0x016E
Pad configuration register 152 (eTPU B[5])	SIU_PCR152	16-bits	Base + 0x0170
Pad configuration register 153 (eTPU B[6])	SIU_PCR153	16-bits	Base + 0x0172
Pad configuration register 154 (eTPU B[7])	SIU_PCR154	16-bits	Base + 0x0174
Pad configuration register 155 (eTPU B[8])	SIU_PCR155	16-bits	Base + 0x0176

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Pad configuration register 156 (eTPU B[9])	SIU_PCR156	16-bits	Base + 0x0178
Pad configuration register 157 (eTPU B[10])	SIU_PCR157	16-bits	Base + 0x017A
Pad configuration register 158 (eTPU B[11])	SIU_PCR158	16-bits	Base + 0x017C
Pad configuration register 159 (eTPU B[12])	SIU_PCR159	16-bits	Base + 0x017E
Pad configuration register 160 (eTPU B[13])	SIU_PCR160	16-bits	Base + 0x0180
Pad configuration register 161 (eTPU B[14])	SIU_PCR161	16-bits	Base + 0x0182
Pad configuration register 162 (eTPU B[15])	SIU_PCR162	16-bits	Base + 0x0184
Pad configuration register 163 (eTPU B[16])	SIU_PCR163	16-bits	Base + 0x0186
Pad configuration register 164 (eTPU B[17])	SIU_PCR164	16-bits	Base + 0x0188
Pad configuration register 165 (eTPU B[18])	SIU_PCR165	16-bits	Base + 0x018A
Pad configuration register 166 (eTPU B[19])	SIU_PCR166	16-bits	Base + 0x018C
Pad configuration register 167 (eTPU B[20])	SIU_PCR167	16-bits	Base + 0x018E
Pad configuration register 168 (eTPU B[21])	SIU_PCR168	16-bits	Base + 0x0190
Pad configuration register 169 (eTPU B[22])	SIU_PCR169	16-bits	Base + 0x0192
Pad configuration register 170 (eTPU B[23])	SIU_PCR170	16-bits	Base + 0x0194
Pad configuration register 171 (eTPU B[24])	SIU_PCR171	16-bits	Base + 0x0196
Pad configuration register 172 (eTPU B[25])	SIU_PCR172	16-bits	Base + 0x0198
Pad configuration register 173 (eTPU B[26])	SIU_PCR173	16-bits	Base + 0x019A
Pad configuration register 174 (eTPU B[27])	SIU_PCR174	16-bits	Base + 0x019C
Pad configuration register 175 (eTPU B[28])	SIU_PCR175	16-bits	Base + 0x019E
Pad configuration register 176 (eTPU B[29])	SIU_PCR176	16-bits	Base + 0x01A0
Pad configuration register 177 (eTPU B[30])	SIU_PCR177	16-bits	Base + 0x01A2
Pad configuration register 178 (eTPU B[31])	SIU_PCR178	16-bits	Base + 0x01A4
Pad configuration register 179 (eMIOS[0])	SIU_PCR179	16-bits	Base + 0x01A6
Pad configuration register 180 (eMIOS[1])	SIU_PCR180	16-bits	Base + 0x01A8
Pad configuration register 181 (eMIOS[2])	SIU_PCR181	16-bits	Base + 0x01AA
Pad configuration register 182 (eMIOS[3])	SIU_PCR182	16-bits	Base + 0x01AC
Pad configuration register 183 (eMIOS[4])	SIU_PCR183	16-bits	Base + 0x01AE
Pad configuration register 184 (eMIOS[5])	SIU_PCR184	16-bits	Base + 0x01B0
Pad configuration register 185 (eMIOS[6])	SIU_PCR185	16-bits	Base + 0x01B2
Pad configuration register 186 (eMIOS[7])	SIU_PCR186	16-bits	Base + 0x01B4
Pad configuration register 187 (eMIOS[8])	SIU_PCR187	16-bits	Base + 0x01B6

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Pad configuration register 188 (eMIOS[9])	SIU_PCR188	16-bits	Base + 0x01B8
Pad configuration register 189 (eMIOS[10])	SIU_PCR189	16-bits	Base + 0x01BA
Pad configuration register 190 (eMIOS[11])	SIU_PCR190	16-bits	Base + 0x01BC
Pad configuration register 191 (eMIOS[12])	SIU_PCR191	16-bits	Base + 0x01BE
Pad configuration register 192 (eMIOS[13])	SIU_PCR192	16-bits	Base + 0x01C0
Pad configuration register 193 (eMIOS[14])	SIU_PCR193	16-bits	Base + 0x01C2
Pad configuration register 194 (eMIOS[15])	SIU_PCR194	16-bits	Base + 0x01C4
Pad configuration register 195 (eMIOS[16])	SIU_PCR195	16-bits	Base + 0x01C6
Pad configuration register 196 (eMIOS[17])	SIU_PCR196	16-bits	Base + 0x01C8
Pad configuration register 197 (eMIOS[18])	SIU_PCR197	16-bits	Base + 0x01CA
Pad configuration register 198 (eMIOS[19])	SIU_PCR198	16-bits	Base + 0x01CC
Pad configuration register 199 (eMIOS[20])	SIU_PCR199	16-bits	Base + 0x01CE
Pad configuration register 200 (eMIOS[21])	SIU_PCR200	16-bits	Base + 0x01D0
Pad configuration register 201 (eMIOS[22])	SIU_PCR201	16-bits	Base + 0x01D2
Pad configuration register 202 (eMIOS[23])	SIU_PCR202	16-bits	Base + 0x01D4
Pad configuration register 203 (GPIO[203])	SIU_PCR203	16-bits	Base + 0x01D6
Pad configuration register 204 (GPIO[204])	SIU_PCR204	16-bits	Base + 0x01D8
Pad configuration register 205 (GPIO[205])	SIU_PCR205	16-bits	Base + 0x01DA
Pad configuration register 206 (GPIO[206])	SIU_PCR206	16-bits	Base + 0x01DC
Pad configuration register 207 (GPIO[207])	SIU_PCR207	16-bits	Base + 0x01DE
Pad configuration register 208 (PLLCFG[0])	SIU_PCR208	16-bits	Base + 0x01E0
Pad configuration register 209 (PLLCFG[1])	SIU_PCR209	16-bits	Base + 0x01E2
Pad configuration register 210 ($\overline{\text{RSTCFG}}$)	SIU_PCR210	16-bits	Base + 0x01E4
Pad configuration register 211 (BOOTCFG[0])	SIU_PCR211	16-bits	Base + 0x01E6
Pad configuration register 212 (BOOTCFG[1])	SIU_PCR212	16-bits	Base + 0x01E8
Pad configuration register 213 (WKPCFG)	SIU_PCR213	16-bits	Base + 0x01EA
Pad configuration register 214 (ENGCLK)	SIU_PCR214	16-bits	Base + 0x01EC
Pad configuration register 215 (AN[12])	SIU_PCR215	16-bits	Base + 0x01EE
Pad configuration register 216 (AN[13])	SIU_PCR216	16-bits	Base + 0x01F0
Pad configuration register 217 (AN[14])	SIU_PCR217	16-bits	Base + 0x01F2
Pad configuration register 218 (AN[15])	SIU_PCR218	16-bits	Base + 0x01F4
Pad configuration register 219 (MCKO)	SIU_PCR219	16-bits	Base + 0x01F6

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Pad configuration register 220 (MDO[0])	SIU_PCR220	16-bits	Base + 0x01F8
Pad configuration register 221 (MDO[1])	SIU_PCR221	16-bits	Base + 0x01FA
Pad configuration register 222 (MDO[2])	SIU_PCR222	16-bits	Base + 0x01FC
Pad configuration register 223 (MDO[3])	SIU_PCR223	16-bits	Base + 0x01FE
Pad configuration register 224 ($\overline{\text{MSEO}}$[0])	SIU_PCR224	16-bits	Base + 0x0200
Pad configuration register 225 ($\overline{\text{MSEO}}$[1])	SIU_PCR225	16-bits	Base + 0x0202
Pad configuration register 226 ($\overline{\text{RDY}}$)	SIU_PCR226	16-bits	Base + 0x0204
Pad configuration register 227 ($\overline{\text{EVTO}}$)	SIU_PCR227	16-bits	Base + 0x0206
Pad configuration register 228 (TDO)	SIU_PCR228	16-bits	Base + 0x0208
Pad configuration register 229 (CLKOUT)	SIU_PCR229	16-bits	Base + 0x020A
Pad configuration register 230 ($\overline{\text{RSTOUT}}$)	SIU_PCR230	16-bits	Base + 0x020C
Reserved	—	—	Base + (0x020E–0x023F)
Pad configuration register 256	SIU_PCR256	16-bits	Base + 0x0240
Pad configuration register 257	SIU_PCR257	16-bits	Base + 0x0242
Pad configuration register 258	SIU_PCR258	16-bits	Base + 0x0244
Pad configuration register 259	SIU_PCR259	16-bits	Base + 0x0246
Pad configuration register 260	SIU_PCR260	16-bits	Base + 0x0248
Pad configuration register 261	SIU_PCR261	16-bits	Base + 0x024A
Pad configuration register 262	SIU_PCR262	16-bits	Base + 0x024C
Pad configuration register 263	SIU_PCR263	16-bits	Base + 0x024E
Pad configuration register 264	SIU_PCR264	16-bits	Base + 0x0250
Pad configuration register 265	SIU_PCR265	16-bits	Base + 0x0252
Pad configuration register 266	SIU_PCR266	16-bits	Base + 0x0254
Pad configuration register 267	SIU_PCR267	16-bits	Base + 0x0256
Pad configuration register 268	SIU_PCR268	16-bits	Base + 0x0258
Pad configuration register 269	SIU_PCR269	16-bits	Base + 0x025A
Pad configuration register 270	SIU_PCR270	16-bits	Base + 0x025C
Pad configuration register 271	SIU_PCR271	16-bits	Base + 0x025E
Pad configuration register 272	SIU_PCR272	16-bits	Base + 0x0260
Pad configuration register 273	SIU_PCR273	16-bits	Base + 0x0262
Pad configuration register 274	SIU_PCR274	16-bits	Base + 0x0264
Pad configuration register 275	SIU_PCR275	16-bits	Base + 0x0266

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Pad configuration register 276	SIU_PCR276	16-bits	Base + 0x0268
Pad configuration register 277	SIU_PCR277	16-bits	Base + 0x026A
Pad configuration register 278	SIU_PCR278	16-bits	Base + 0x026C
Pad configuration register 279	SIU_PCR279	16-bits	Base + 0x026E
Pad configuration register 280	SIU_PCR280	16-bits	Base + 0x0270
Pad configuration register 281	SIU_PCR281	16-bits	Base + 0x0272
Pad configuration register 282	SIU_PCR282	16-bits	Base + 0x0274
Pad configuration register 283	SIU_PCR283	16-bits	Base + 0x0276
Pad configuration register 284	SIU_PCR284	16-bits	Base + 0x0278
Pad configuration register 285	SIU_PCR285	16-bits	Base + 0x027A
Pad configuration register 286	SIU_PCR286	16-bits	Base + 0x027C
Pad configuration register 287	SIU_PCR287	16-bits	Base + 0x027E
Pad configuration register 288	SIU_PCR288	16-bits	Base + 0x0280
Pad configuration register 289	SIU_PCR289	16-bits	Base + 0x0282
Pad configuration register 290	SIU_PCR290	16-bits	Base + 0x0284
Pad configuration register 291	SIU_PCR291	16-bits	Base + 0x0286
Pad configuration register 292	SIU_PCR292	16-bits	Base + 0x0288
Pad configuration register 293	SIU_PCR293	16-bits	Base + 0x028A
Pad configuration register 294	SIU_PCR294	16-bits	Base + 0x028C
Pad configuration register 295	SIU_PCR295	16-bits	Base + 0x028E
Pad configuration register 296	SIU_PCR296	16-bits	Base + 0x0290
Pad configuration register 297	SIU_PCR297	16-bits	Base + 0x0292
Pad configuration register 298	SIU_PCR298	16-bits	Base + 0x0294
Reserved	—	—	Base + (0x020E–0x05FF)
GPIO pin data output register 0	SIU_GPDO0	8-bits	Base + 0x0600
GPIO pin data output register 1	SIU_GPDO1	8-bits	Base + 0x0601
GPIO pin data output register 2	SIU_GPDO2	8-bits	Base + 0x0602
GPIO pin data output register 3	SIU_GPDO3	8-bits	Base + 0x0603
GPIO pin data output register 4	SIU_GPDO4	8-bits	Base + 0x0604
GPIO pin data output register 5	SIU_GPDO5	8-bits	Base + 0x0605
GPIO pin data output register 6	SIU_GPDO6	8-bits	Base + 0x0606
GPIO pin data output register 7	SIU_GPDO7	8-bits	Base + 0x0607

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data output register 8	SIU_GPDO8	8-bits	Base + 0x0608
GPIO pin data output register 9	SIU_GPDO9	8-bits	Base + 0x0609
GPIO pin data output register 10	SIU_GPDO10	8-bits	Base + 0x060A
GPIO pin data output register 11	SIU_GPDO11	8-bits	Base + 0x060B
GPIO pin data output register 12	SIU_GPDO12	8-bits	Base + 0x060C
GPIO pin data output register 13	SIU_GPDO13	8-bits	Base + 0x060D
GPIO pin data output register 14	SIU_GPDO14	8-bits	Base + 0x060E
GPIO pin data output register 15	SIU_GPDO15	8-bits	Base + 0x060F
GPIO pin data output register 16	SIU_GPDO16	8-bits	Base + 0x0610
GPIO pin data output register 17	SIU_GPDO17	8-bits	Base + 0x0611
GPIO pin data output register 18	SIU_GPDO18	8-bits	Base + 0x0612
GPIO pin data output register 19	SIU_GPDO19	8-bits	Base + 0x0613
GPIO pin data output register 20	SIU_GPDO20	8-bits	Base + 0x0614
GPIO pin data output register 21	SIU_GPDO21	8-bits	Base + 0x0615
GPIO pin data output register 22	SIU_GPDO22	8-bits	Base + 0x0616
GPIO pin data output register 23	SIU_GPDO23	8-bits	Base + 0x0617
GPIO pin data output register 24	SIU_GPDO24	8-bits	Base + 0x0618
GPIO pin data output register 25	SIU_GPDO25	8-bits	Base + 0x0619
GPIO pin data output register 26	SIU_GPDO26	8-bits	Base + 0x061A
GPIO pin data output register 27	SIU_GPDO27	8-bits	Base + 0x061B
GPIO pin data output register 28	SIU_GPDO28	8-bits	Base + 0x061C
GPIO pin data output register 29	SIU_GPDO29	8-bits	Base + 0x061D
GPIO pin data output register 30	SIU_GPDO30	8-bits	Base + 0x061E
GPIO pin data output register 31	SIU_GPDO31	8-bits	Base + 0x061F
GPIO pin data output register 32	SIU_GPDO32	8-bits	Base + 0x0620
GPIO pin data output register 33	SIU_GPDO33	8-bits	Base + 0x0621
GPIO pin data output register 34	SIU_GPDO34	8-bits	Base + 0x0622
GPIO pin data output register 35	SIU_GPDO35	8-bits	Base + 0x0623
GPIO pin data output register 36	SIU_GPDO36	8-bits	Base + 0x0624
GPIO pin data output register 37	SIU_GPDO37	8-bits	Base + 0x0625
GPIO pin data output register 38	SIU_GPDO38	8-bits	Base + 0x0626
GPIO pin data output register 39	SIU_GPDO39	8-bits	Base + 0x0627

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data output register 40	SIU_GPDO40	8-bits	Base + 0x0628
GPIO pin data output register 41	SIU_GPDO41	8-bits	Base + 0x0629
GPIO pin data output register 42	SIU_GPDO42	8-bits	Base + 0x062A
GPIO pin data output register 43	SIU_GPDO43	8-bits	Base + 0x062B
GPIO pin data output register 44	SIU_GPDO44	8-bits	Base + 0x062C
GPIO pin data output register 45	SIU_GPDO45	8-bits	Base + 0x062D
GPIO pin data output register 46	SIU_GPDO46	8-bits	Base + 0x062E
GPIO pin data output register 47	SIU_GPDO47	8-bits	Base + 0x062F
GPIO pin data output register 48	SIU_GPDO48	8-bits	Base + 0x0630
GPIO pin data output register 49	SIU_GPDO49	8-bits	Base + 0x0631
GPIO pin data output register 50	SIU_GPDO50	8-bits	Base + 0x0632
GPIO pin data output register 51	SIU_GPDO51	8-bits	Base + 0x0633
GPIO pin data output register 52	SIU_GPDO52	8-bits	Base + 0x0634
GPIO pin data output register 53	SIU_GPDO53	8-bits	Base + 0x0635
GPIO pin data output register 54	SIU_GPDO54	8-bits	Base + 0x0636
GPIO pin data output register 55	SIU_GPDO55	8-bits	Base + 0x0637
GPIO pin data output register 56	SIU_GPDO56	8-bits	Base + 0x0638
GPIO pin data output register 57	SIU_GPDO57	8-bits	Base + 0x0639
GPIO pin data output register 58	SIU_GPDO58	8-bits	Base + 0x063A
GPIO pin data output register 59	SIU_GPDO59	8-bits	Base + 0x063B
GPIO pin data output register 60	SIU_GPDO60	8-bits	Base + 0x063C
GPIO pin data output register 61	SIU_GPDO61	8-bits	Base + 0x063D
GPIO pin data output register 62	SIU_GPDO62	8-bits	Base + 0x063E
GPIO pin data output register 63	SIU_GPDO63	8-bits	Base + 0x063F
GPIO pin data output register 64	SIU_GPDO64	8-bits	Base + 0x0640
GPIO pin data output register 65	SIU_GPDO65	8-bits	Base + 0x0641
GPIO pin data output register 66	SIU_GPDO66	8-bits	Base + 0x0642
GPIO pin data output register 67	SIU_GPDO67	8-bits	Base + 0x0643
GPIO pin data output register 68	SIU_GPDO68	8-bits	Base + 0x0644
GPIO pin data output register 69	SIU_GPDO69	8-bits	Base + 0x0645
GPIO pin data output register 70	SIU_GPDO70	8-bits	Base + 0x0646
GPIO pin data output register 71	SIU_GPDO71	8-bits	Base + 0x0647

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data output register 72	SIU_GPDO72	8-bits	Base + 0x0648
GPIO pin data output register 73	SIU_GPDO73	8-bits	Base + 0x0649
GPIO pin data output register 74	SIU_GPDO74	8-bits	Base + 0x064A
GPIO pin data output register 75	SIU_GPDO75	8-bits	Base + 0x064B
GPIO pin data output register 76	SIU_GPDO76	8-bits	Base + 0x064C
GPIO pin data output register 77	SIU_GPDO77	8-bits	Base + 0x064D
GPIO pin data output register 78	SIU_GPDO78	8-bits	Base + 0x064E
GPIO pin data output register 79	SIU_GPDO79	8-bits	Base + 0x064F
GPIO pin data output register 80	SIU_GPDO80	8-bits	Base + 0x0650
GPIO pin data output register 81	SIU_GPDO81	8-bits	Base + 0x0651
GPIO pin data output register 82	SIU_GPDO82	8-bits	Base + 0x0652
GPIO pin data output register 83	SIU_GPDO83	8-bits	Base + 0x0653
GPIO pin data output register 84	SIU_GPDO84	8-bits	Base + 0x0654
GPIO pin data output register 85	SIU_GPDO85	8-bits	Base + 0x0655
GPIO pin data output register 86	SIU_GPDO86	8-bits	Base + 0x0656
GPIO pin data output register 87	SIU_GPDO87	8-bits	Base + 0x0657
GPIO pin data output register 88	SIU_GPDO88	8-bits	Base + 0x0658
GPIO pin data output register 89	SIU_GPDO89	8-bits	Base + 0x0659
GPIO pin data output register 90	SIU_GPDO90	8-bits	Base + 0x065A
GPIO pin data output register 91	SIU_GPDO91	8-bits	Base + 0x065B
GPIO pin data output register 92	SIU_GPDO92	8-bits	Base + 0x065C
GPIO pin data output register 93	SIU_GPDO93	8-bits	Base + 0x065D
GPIO pin data output register 94	SIU_GPDO94	8-bits	Base + 0x065E
GPIO pin data output register 95	SIU_GPDO95	8-bits	Base + 0x065F
GPIO pin data output register 96	SIU_GPDO96	8-bits	Base + 0x0660
GPIO pin data output register 97	SIU_GPDO97	8-bits	Base + 0x0661
GPIO pin data output register 98	SIU_GPDO98	8-bits	Base + 0x0662
GPIO pin data output register 99	SIU_GPDO99	8-bits	Base + 0x0663
GPIO pin data output register 100	SIU_GPDO100	8-bits	Base + 0x0664
GPIO pin data output register 101	SIU_GPDO101	8-bits	Base + 0x0665
GPIO pin data output register 102	SIU_GPDO102	8-bits	Base + 0x0666
GPIO pin data output register 103	SIU_GPDO103	8-bits	Base + 0x0667

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data output register 104	SIU_GPDO104	8-bits	Base + 0x0668
GPIO pin data output register 105	SIU_GPDO105	8-bits	Base + 0x0669
GPIO pin data output register 106	SIU_GPDO106	8-bits	Base + 0x066A
GPIO pin data output register 107	SIU_GPDO107	8-bits	Base + 0x066B
GPIO pin data output register 108	SIU_GPDO108	8-bits	Base + 0x066C
GPIO pin data output register 109	SIU_GPDO109	8-bits	Base + 0x066D
GPIO pin data output register 110	SIU_GPDO110	8-bits	Base + 0x066E
GPIO pin data output register 111	SIU_GPDO111	8-bits	Base + 0x066F
GPIO pin data output register 112	SIU_GPDO112	8-bits	Base + 0x0670
GPIO pin data output register 113	SIU_GPDO113	8-bits	Base + 0x0671
GPIO pin data output register 114	SIU_GPDO114	8-bits	Base + 0x0672
GPIO pin data output register 115	SIU_GPDO115	8-bits	Base + 0x0673
GPIO pin data output register 116	SIU_GPDO116	8-bits	Base + 0x0674
GPIO pin data output register 117	SIU_GPDO117	8-bits	Base + 0x0675
GPIO pin data output register 118	SIU_GPDO118	8-bits	Base + 0x0676
GPIO pin data output register 119	SIU_GPDO119	8-bits	Base + 0x0677
GPIO pin data output register 120	SIU_GPDO120	8-bits	Base + 0x0678
GPIO pin data output register 121	SIU_GPDO121	8-bits	Base + 0x0679
GPIO pin data output register 122	SIU_GPDO122	8-bits	Base + 0x067A
GPIO pin data output register 123	SIU_GPDO123	8-bits	Base + 0x067B
GPIO pin data output register 124	SIU_GPDO124	8-bits	Base + 0x067C
GPIO pin data output register 125	SIU_GPDO125	8-bits	Base + 0x067D
GPIO pin data output register 126	SIU_GPDO126	8-bits	Base + 0x067E
GPIO pin data output register 127	SIU_GPDO127	8-bits	Base + 0x067F
GPIO pin data output register 128	SIU_GPDO128	8-bits	Base + 0x0680
GPIO pin data output register 129	SIU_GPDO129	8-bits	Base + 0x0681
GPIO pin data output register 130	SIU_GPDO130	8-bits	Base + 0x0682
GPIO pin data output register 131	SIU_GPDO131	8-bits	Base + 0x0683
GPIO pin data output register 132	SIU_GPDO132	8-bits	Base + 0x0684
GPIO pin data output register 133	SIU_GPDO133	8-bits	Base + 0x0685
GPIO pin data output register 134	SIU_GPDO134	8-bits	Base + 0x0686
GPIO pin data output register 135	SIU_GPDO135	8-bits	Base + 0x0687

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data output register 136	SIU_GPDO136	8-bits	Base + 0x0688
GPIO pin data output register 137	SIU_GPDO137	8-bits	Base + 0x0689
GPIO pin data output register 138	SIU_GPDO138	8-bits	Base + 0x068A
GPIO pin data output register 139	SIU_GPDO139	8-bits	Base + 0x068B
GPIO pin data output register 140	SIU_GPDO140	8-bits	Base + 0x068C
GPIO pin data output register 141	SIU_GPDO141	8-bits	Base + 0x068D
GPIO pin data output register 142	SIU_GPDO142	8-bits	Base + 0x068E
GPIO pin data output register 143	SIU_GPDO143	8-bits	Base + 0x068F
GPIO pin data output register 144	SIU_GPDO144	8-bits	Base + 0x0690
GPIO pin data output register 145	SIU_GPDO145	8-bits	Base + 0x0691
GPIO pin data output register 146	SIU_GPDO146	8-bits	Base + 0x0692
GPIO pin data output register 147	SIU_GPDO147	8-bits	Base + 0x0693
GPIO pin data output register 148	SIU_GPDO148	8-bits	Base + 0x0694
GPIO pin data output register 149	SIU_GPDO149	8-bits	Base + 0x0695
GPIO pin data output register 150	SIU_GPDO150	8-bits	Base + 0x0696
GPIO pin data output register 151	SIU_GPDO151	8-bits	Base + 0x0697
GPIO pin data output register 152	SIU_GPDO152	8-bits	Base + 0x0698
GPIO pin data output register 153	SIU_GPDO153	8-bits	Base + 0x0699
GPIO pin data output register 154	SIU_GPDO154	8-bits	Base + 0x069A
GPIO pin data output register 155	SIU_GPDO155	8-bits	Base + 0x069B
GPIO pin data output register 156	SIU_GPDO156	8-bits	Base + 0x069C
GPIO pin data output register 157	SIU_GPDO157	8-bits	Base + 0x069D
GPIO pin data output register 158	SIU_GPDO158	8-bits	Base + 0x069E
GPIO pin data output register 159	SIU_GPDO159	8-bits	Base + 0x069F
GPIO pin data output register 160	SIU_GPDO160	8-bits	Base + 0x06A0
GPIO pin data output register 161	SIU_GPDO161	8-bits	Base + 0x06A1
GPIO pin data output register 162	SIU_GPDO162	8-bits	Base + 0x06A2
GPIO pin data output register 163	SIU_GPDO163	8-bits	Base + 0x06A3
GPIO pin data output register 164	SIU_GPDO164	8-bits	Base + 0x06A4
GPIO pin data output register 165	SIU_GPDO165	8-bits	Base + 0x06A5
GPIO pin data output register 166	SIU_GPDO166	8-bits	Base + 0x06A6
GPIO pin data output register 167	SIU_GPDO167	8-bits	Base + 0x06A7

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data output register 168	SIU_GPDO168	8-bits	Base + 0x06A8
GPIO pin data output register 169	SIU_GPDO169	8-bits	Base + 0x06A9
GPIO pin data output register 170	SIU_GPDO170	8-bits	Base + 0x06AA
GPIO pin data output register 171	SIU_GPDO171	8-bits	Base + 0x06AB
GPIO pin data output register 172	SIU_GPDO172	8-bits	Base + 0x06AC
GPIO pin data output register 173	SIU_GPDO173	8-bits	Base + 0x06AD
GPIO pin data output register 174	SIU_GPDO174	8-bits	Base + 0x06AE
GPIO pin data output register 175	SIU_GPDO175	8-bits	Base + 0x06AF
GPIO pin data output register 176	SIU_GPDO176	8-bits	Base + 0x06B0
GPIO pin data output register 177	SIU_GPDO177	8-bits	Base + 0x06B1
GPIO pin data output register 178	SIU_GPDO178	8-bits	Base + 0x06B2
GPIO pin data output register 179	SIU_GPDO179	8-bits	Base + 0x06B3
GPIO pin data output register 180	SIU_GPDO180	8-bits	Base + 0x06B4
GPIO pin data output register 181	SIU_GPDO181	8-bits	Base + 0x06B5
GPIO pin data output register 182	SIU_GPDO182	8-bits	Base + 0x06B6
GPIO pin data output register 183	SIU_GPDO183	8-bits	Base + 0x06B7
GPIO pin data output register 184	SIU_GPDO184	8-bits	Base + 0x06B8
GPIO pin data output register 185	SIU_GPDO185	8-bits	Base + 0x06B9
GPIO pin data output register 186	SIU_GPDO186	8-bits	Base + 0x06BA
GPIO pin data output register 187	SIU_GPDO187	8-bits	Base + 0x06BB
GPIO pin data output register 188	SIU_GPDO188	8-bits	Base + 0x06BC
GPIO pin data output register 189	SIU_GPDO189	8-bits	Base + 0x06BD
GPIO pin data output register 190	SIU_GPDO190	8-bits	Base + 0x06BE
GPIO pin data output register 191	SIU_GPDO191	8-bits	Base + 0x06BF
GPIO pin data output register 192	SIU_GPDO192	8-bits	Base + 0x06C0
GPIO pin data output register 193	SIU_GPDO193	8-bits	Base + 0x06C1
GPIO pin data output register 194	SIU_GPDO194	8-bits	Base + 0x06C2
GPIO pin data output register 195	SIU_GPDO195	8-bits	Base + 0x06C3
GPIO pin data output register 196	SIU_GPDO196	8-bits	Base + 0x06C4
GPIO pin data output register 197	SIU_GPDO197	8-bits	Base + 0x06C5
GPIO pin data output register 198	SIU_GPDO198	8-bits	Base + 0x06C6
GPIO pin data output register 199	SIU_GPDO199	8-bits	Base + 0x06C7

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data output register 200	SIU_GPDO200	8-bits	Base + 0x06C8
GPIO pin data output register 201	SIU_GPDO201	8-bits	Base + 0x06C9
GPIO pin data output register 202	SIU_GPDO202	8-bits	Base + 0x06CA
GPIO pin data output register 203	SIU_GPDO203	8-bits	Base + 0x06CB
GPIO pin data output register 204	SIU_GPDO204	8-bits	Base + 0x06CC
GPIO pin data output register 205	SIU_GPDO205	8-bits	Base + 0x06CD
GPIO pin data output register 206	SIU_GPDO206	8-bits	Base + 0x06CE
GPIO pin data output register 207	SIU_GPDO207	8-bits	Base + 0x06CF
GPIO pin data output register 208	SIU_GPDO208	8-bits	Base + 0x06D0
GPIO pin data output register 209	SIU_GPDO209	8-bits	Base + 0x06D1
GPIO pin data output register 210	SIU_GPDO210	8-bits	Base + 0x06D2
GPIO pin data output register 211	SIU_GPDO211	8-bits	Base + 0x06D3
GPIO pin data output register 212	SIU_GPDO212	8-bits	Base + 0x06D4
GPIO pin data output register 213	SIU_GPDO213	8-bits	Base + 0x06D5
Reserved	—	—	Base + (0x06D6–0x07FF)
GPIO pin data input register 0	SIU_GPDI0	8-bits	Base + 0x0800
GPIO pin data input register 1	SIU_GPDI1	8-bits	Base + 0x0801
GPIO pin data input register 2	SIU_GPDI2	8-bits	Base + 0x0802
GPIO pin data input register 3	SIU_GPDI3	8-bits	Base + 0x0803
GPIO pin data input register 4	SIU_GPDI4	8-bits	Base + 0x0804
GPIO pin data input register 5	SIU_GPDI5	8-bits	Base + 0x0805
GPIO pin data input register 6	SIU_GPDI6	8-bits	Base + 0x0806
GPIO pin data input register 7	SIU_GPDI7	8-bits	Base + 0x0807
GPIO pin data input register 8	SIU_GPDI8	8-bits	Base + 0x0808
GPIO pin data input register 9	SIU_GPDI9	8-bits	Base + 0x0809
GPIO pin data input register 10	SIU_GPDI10	8-bits	Base + 0x080A
GPIO pin data input register 11	SIU_GPDI11	8-bits	Base + 0x080B
GPIO pin data input register 12	SIU_GPDI12	8-bits	Base + 0x080C
GPIO pin data input register 13	SIU_GPDI13	8-bits	Base + 0x080D
GPIO pin data input register 14	SIU_GPDI14	8-bits	Base + 0x080E
GPIO pin data input register 15	SIU_GPDI15	8-bits	Base + 0x080F
GPIO pin data input register 16	SIU_GPDI16	8-bits	Base + 0x0810

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data input register 17	SIU_GPDI17	8-bits	Base + 0x0811
GPIO pin data input register 18	SIU_GPDI18	8-bits	Base + 0x0812
GPIO pin data input register 19	SIU_GPDI19	8-bits	Base + 0x0813
GPIO pin data input register 20	SIU_GPDI20	8-bits	Base + 0x0814
GPIO pin data input register 21	SIU_GPDI21	8-bits	Base + 0x0815
GPIO pin data input register 22	SIU_GPDI22	8-bits	Base + 0x0816
GPIO pin data input register 23	SIU_GPDI23	8-bits	Base + 0x0817
GPIO pin data input register 24	SIU_GPDI24	8-bits	Base + 0x0818
GPIO pin data input register 25	SIU_GPDI25	8-bits	Base + 0x0819
GPIO pin data input register 26	SIU_GPDI26	8-bits	Base + 0x081A
GPIO pin data input register 27	SIU_GPDI27	8-bits	Base + 0x081B
GPIO pin data input register 28	SIU_GPDI28	8-bits	Base + 0x081C
GPIO pin data input register 29	SIU_GPDI29	8-bits	Base + 0x081D
GPIO pin data input register 30	SIU_GPDI30	8-bits	Base + 0x081E
GPIO pin data input register 31	SIU_GPDI31	8-bits	Base + 0x081F
GPIO pin data input register 32	SIU_GPDI32	8-bits	Base + 0x0820
GPIO pin data input register 33	SIU_GPDI33	8-bits	Base + 0x0821
GPIO pin data input register 34	SIU_GPDI34	8-bits	Base + 0x0822
GPIO pin data input register 35	SIU_GPDI35	8-bits	Base + 0x0823
GPIO pin data input register 36	SIU_GPDI36	8-bits	Base + 0x0824
GPIO pin data input register 37	SIU_GPDI37	8-bits	Base + 0x0825
GPIO pin data input register 38	SIU_GPDI38	8-bits	Base + 0x0826
GPIO pin data input register 39	SIU_GPDI39	8-bits	Base + 0x0827
GPIO pin data input register 40	SIU_GPDI40	8-bits	Base + 0x0828
GPIO pin data input register 41	SIU_GPDI41	8-bits	Base + 0x0829
GPIO pin data input register 42	SIU_GPDI42	8-bits	Base + 0x082A
GPIO pin data input register 43	SIU_GPDI43	8-bits	Base + 0x082B
GPIO pin data input register 44	SIU_GPDI44	8-bits	Base + 0x082C
GPIO pin data input register 45	SIU_GPDI45	8-bits	Base + 0x082D
GPIO pin data input register 46	SIU_GPDI46	8-bits	Base + 0x082E
GPIO pin data input register 47	SIU_GPDI47	8-bits	Base + 0x082F
GPIO pin data input register 48	SIU_GPDI48	8-bits	Base + 0x0830

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data input register 49	SIU_GPDI49	8-bits	Base + 0x0831
GPIO pin data input register 50	SIU_GPDI50	8-bits	Base + 0x0832
GPIO pin data input register 51	SIU_GPDI51	8-bits	Base + 0x0833
GPIO pin data input register 52	SIU_GPDI52	8-bits	Base + 0x0834
GPIO pin data input register 53	SIU_GPDI53	8-bits	Base + 0x0835
GPIO pin data input register 54	SIU_GPDI54	8-bits	Base + 0x0836
GPIO pin data input register 55	SIU_GPDI55	8-bits	Base + 0x0837
GPIO pin data input register 56	SIU_GPDI56	8-bits	Base + 0x0838
GPIO pin data input register 57	SIU_GPDI57	8-bits	Base + 0x0839
GPIO pin data input register 58	SIU_GPDI58	8-bits	Base + 0x083A
GPIO pin data input register 59	SIU_GPDI59	8-bits	Base + 0x083B
GPIO pin data input register 60	SIU_GPDI60	8-bits	Base + 0x083C
GPIO pin data input register 61	SIU_GPDI61	8-bits	Base + 0x083D
GPIO pin data input register 62	SIU_GPDI62	8-bits	Base + 0x083E
GPIO pin data input register 63	SIU_GPDI63	8-bits	Base + 0x083F
GPIO pin data input register 64	SIU_GPDI64	8-bits	Base + 0x0840
GPIO pin data input register 65	SIU_GPDI65	8-bits	Base + 0x0841
GPIO pin data input register 66	SIU_GPDI66	8-bits	Base + 0x0842
GPIO pin data input register 67	SIU_GPDI67	8-bits	Base + 0x0843
GPIO pin data input register 68	SIU_GPDI68	8-bits	Base + 0x0844
GPIO pin data input register 69	SIU_GPDI69	8-bits	Base + 0x0845
GPIO pin data input register 70	SIU_GPDI70	8-bits	Base + 0x0846
GPIO pin data input register 71	SIU_GPDI71	8-bits	Base + 0x0847
GPIO pin data input register 72	SIU_GPDI72	8-bits	Base + 0x0848
GPIO pin data input register 73	SIU_GPDI73	8-bits	Base + 0x0849
GPIO pin data input register 74	SIU_GPDI74	8-bits	Base + 0x084A
GPIO pin data input register 75	SIU_GPDI75	8-bits	Base + 0x084B
GPIO pin data input register 76	SIU_GPDI76	8-bits	Base + 0x084C
GPIO pin data input register 77	SIU_GPDI77	8-bits	Base + 0x084D
GPIO pin data input register 78	SIU_GPDI78	8-bits	Base + 0x084E
GPIO pin data input register 79	SIU_GPDI79	8-bits	Base + 0x084F
GPIO pin data input register 80	SIU_GPDI80	8-bits	Base + 0x0850

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data input register 81	SIU_GPDI81	8-bits	Base + 0x0851
GPIO pin data input register 82	SIU_GPDI82	8-bits	Base + 0x0852
GPIO pin data input register 83	SIU_GPDI83	8-bits	Base + 0x0853
GPIO pin data input register 84	SIU_GPDI84	8-bits	Base + 0x0854
GPIO pin data input register 85	SIU_GPDI85	8-bits	Base + 0x0855
GPIO pin data input register 86	SIU_GPDI86	8-bits	Base + 0x0856
GPIO pin data input register 87	SIU_GPDI87	8-bits	Base + 0x0857
GPIO pin data input register 88	SIU_GPDI88	8-bits	Base + 0x0858
GPIO pin data input register 89	SIU_GPDI89	8-bits	Base + 0x0859
GPIO pin data input register 90	SIU_GPDI90	8-bits	Base + 0x085A
GPIO pin data input register 91	SIU_GPDI91	8-bits	Base + 0x085B
GPIO pin data input register 92	SIU_GPDI92	8-bits	Base + 0x085C
GPIO pin data input register 93	SIU_GPDI93	8-bits	Base + 0x085D
GPIO pin data input register 94	SIU_GPDI94	8-bits	Base + 0x085E
GPIO pin data input register 95	SIU_GPDI95	8-bits	Base + 0x085F
GPIO pin data input register 96	SIU_GPDI96	8-bits	Base + 0x0860
GPIO pin data input register 97	SIU_GPDI97	8-bits	Base + 0x0861
GPIO pin data input register 98	SIU_GPDI98	8-bits	Base + 0x0862
GPIO pin data input register 99	SIU_GPDI99	8-bits	Base + 0x0863
GPIO pin data input register 100	SIU_GPDI100	8-bits	Base + 0x0864
GPIO pin data input register 101	SIU_GPDI101	8-bits	Base + 0x0865
GPIO pin data input register 102	SIU_GPDI102	8-bits	Base + 0x0866
GPIO pin data input register 103	SIU_GPDI103	8-bits	Base + 0x0867
GPIO pin data input register 104	SIU_GPDI104	8-bits	Base + 0x0868
GPIO pin data input register 105	SIU_GPDI105	8-bits	Base + 0x0869
GPIO pin data input register 106	SIU_GPDI106	8-bits	Base + 0x086A
GPIO pin data input register 107	SIU_GPDI107	8-bits	Base + 0x086B
GPIO pin data input register 108	SIU_GPDI108	8-bits	Base + 0x086C
GPIO pin data input register 109	SIU_GPDI109	8-bits	Base + 0x086D
GPIO pin data input register 110	SIU_GPDI110	8-bits	Base + 0x086E
GPIO pin data input register 111	SIU_GPDI111	8-bits	Base + 0x086F
GPIO pin data input register 112	SIU_GPDI112	8-bits	Base + 0x0870

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data input register 113	SIU_GPDI113	8-bits	Base + 0x0871
GPIO pin data input register 114	SIU_GPDI114	8-bits	Base + 0x0872
GPIO pin data input register 115	SIU_GPDI115	8-bits	Base + 0x0873
GPIO pin data input register 116	SIU_GPDI116	8-bits	Base + 0x0874
GPIO pin data input register 117	SIU_GPDI117	8-bits	Base + 0x0875
GPIO pin data input register 118	SIU_GPDI118	8-bits	Base + 0x0876
GPIO pin data input register 119	SIU_GPDI119	8-bits	Base + 0x0877
GPIO pin data input register 120	SIU_GPDI120	8-bits	Base + 0x0878
GPIO pin data input register 121	SIU_GPDI121	8-bits	Base + 0x0879
GPIO pin data input register 122	SIU_GPDI122	8-bits	Base + 0x087A
GPIO pin data input register 123	SIU_GPDI123	8-bits	Base + 0x087B
GPIO pin data input register 124	SIU_GPDI124	8-bits	Base + 0x087C
GPIO pin data input register 125	SIU_GPDI125	8-bits	Base + 0x087D
GPIO pin data input register 126	SIU_GPDI126	8-bits	Base + 0x087E
GPIO pin data input register 127	SIU_GPDI127	8-bits	Base + 0x087F
GPIO pin data input register 128	SIU_GPDI128	8-bits	Base + 0x0880
GPIO pin data input register 129	SIU_GPDI129	8-bits	Base + 0x0881
GPIO pin data input register 130	SIU_GPDI130	8-bits	Base + 0x0882
GPIO pin data input register 131	SIU_GPDI131	8-bits	Base + 0x0883
GPIO pin data input register 132	SIU_GPDI132	8-bits	Base + 0x0884
GPIO pin data input register 133	SIU_GPDI133	8-bits	Base + 0x0885
GPIO pin data input register 134	SIU_GPDI134	8-bits	Base + 0x0886
GPIO pin data input register 135	SIU_GPDI135	8-bits	Base + 0x0887
GPIO pin data input register 136	SIU_GPDI136	8-bits	Base + 0x0888
GPIO pin data input register 137	SIU_GPDI137	8-bits	Base + 0x0889
GPIO pin data input register 138	SIU_GPDI138	8-bits	Base + 0x088A
GPIO pin data input register 139	SIU_GPDI139	8-bits	Base + 0x088B
GPIO pin data input register 140	SIU_GPDI140	8-bits	Base + 0x088C
GPIO pin data input register 141	SIU_GPDI141	8-bits	Base + 0x088D
GPIO pin data input register 142	SIU_GPDI142	8-bits	Base + 0x088E
GPIO pin data input register 143	SIU_GPDI143	8-bits	Base + 0x088F
GPIO pin data input register 144	SIU_GPDI144	8-bits	Base + 0x0890

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data input register 145	SIU_GPDI145	8-bits	Base + 0x0891
GPIO pin data input register 146	SIU_GPDI146	8-bits	Base + 0x0892
GPIO pin data input register 147	SIU_GPDI147	8-bits	Base + 0x0893
GPIO pin data input register 148	SIU_GPDI148	8-bits	Base + 0x0894
GPIO pin data input register 149	SIU_GPDI149	8-bits	Base + 0x0895
GPIO pin data input register 150	SIU_GPDI150	8-bits	Base + 0x0896
GPIO pin data input register 151	SIU_GPDI151	8-bits	Base + 0x0897
GPIO pin data input register 152	SIU_GPDI152	8-bits	Base + 0x0898
GPIO pin data input register 153	SIU_GPDI153	8-bits	Base + 0x0899
GPIO pin data input register 154	SIU_GPDI154	8-bits	Base + 0x089A
GPIO pin data input register 155	SIU_GPDI155	8-bits	Base + 0x089B
GPIO pin data input register 156	SIU_GPDI156	8-bits	Base + 0x089C
GPIO pin data input register 157	SIU_GPDI157	8-bits	Base + 0x089D
GPIO pin data input register 158	SIU_GPDI158	8-bits	Base + 0x089E
GPIO pin data input register 159	SIU_GPDI159	8-bits	Base + 0x089F
GPIO pin data input register 160	SIU_GPDI160	8-bits	Base + 0x08A0
GPIO pin data input register 161	SIU_GPDI161	8-bits	Base + 0x08A1
GPIO pin data input register 162	SIU_GPDI162	8-bits	Base + 0x08A2
GPIO pin data input register 163	SIU_GPDI163	8-bits	Base + 0x08A3
GPIO pin data input register 164	SIU_GPDI164	8-bits	Base + 0x08A4
GPIO pin data input register 165	SIU_GPDI165	8-bits	Base + 0x08A5
GPIO pin data input register 166	SIU_GPDI166	8-bits	Base + 0x08A6
GPIO pin data input register 167	SIU_GPDI167	8-bits	Base + 0x08A7
GPIO pin data input register 168	SIU_GPDI168	8-bits	Base + 0x08A8
GPIO pin data input register 169	SIU_GPDI169	8-bits	Base + 0x08A9
GPIO pin data input register 170	SIU_GPDI170	8-bits	Base + 0x08AA
GPIO pin data input register 171	SIU_GPDI171	8-bits	Base + 0x08AB
GPIO pin data input register 172	SIU_GPDI172	8-bits	Base + 0x08AC
GPIO pin data input register 173	SIU_GPDI173	8-bits	Base + 0x08AD
GPIO pin data input register 174	SIU_GPDI174	8-bits	Base + 0x08AE
GPIO pin data input register 175	SIU_GPDI175	8-bits	Base + 0x08AF
GPIO pin data input register 176	SIU_GPDI176	8-bits	Base + 0x08B0

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data input register 177	SIU_GPDI177	8-bits	Base + 0x08B1
GPIO pin data input register 178	SIU_GPDI178	8-bits	Base + 0x08B2
GPIO pin data input register 179	SIU_GPDI179	8-bits	Base + 0x08B3
GPIO pin data input register 180	SIU_GPDI180	8-bits	Base + 0x08B4
GPIO pin data input register 181	SIU_GPDI181	8-bits	Base + 0x08B5
GPIO pin data input register 182	SIU_GPDI182	8-bits	Base + 0x08B6
GPIO pin data input register 183	SIU_GPDI183	8-bits	Base + 0x08B7
GPIO pin data input register 184	SIU_GPDI184	8-bits	Base + 0x08B8
GPIO pin data input register 185	SIU_GPDI185	8-bits	Base + 0x08B9
GPIO pin data input register 186	SIU_GPDI186	8-bits	Base + 0x08BA
GPIO pin data input register 187	SIU_GPDI187	8-bits	Base + 0x08BB
GPIO pin data input register 188	SIU_GPDI188	8-bits	Base + 0x08BC
GPIO pin data input register 189	SIU_GPDI189	8-bits	Base + 0x08BD
GPIO pin data input register 190	SIU_GPDI190	8-bits	Base + 0x08BE
GPIO pin data input register 191	SIU_GPDI191	8-bits	Base + 0x08BF
GPIO pin data input register 192	SIU_GPDI192	8-bits	Base + 0x08C0
GPIO pin data input register 193	SIU_GPDI193	8-bits	Base + 0x08C1
GPIO pin data input register 194	SIU_GPDI194	8-bits	Base + 0x08C2
GPIO pin data input register 195	SIU_GPDI195	8-bits	Base + 0x08C3
GPIO pin data input register 196	SIU_GPDI196	8-bits	Base + 0x08C4
GPIO pin data input register 197	SIU_GPDI197	8-bits	Base + 0x08C5
GPIO pin data input register 198	SIU_GPDI198	8-bits	Base + 0x08C6
GPIO pin data input register 199	SIU_GPDI199	8-bits	Base + 0x08C7
GPIO pin data input register 200	SIU_GPDI200	8-bits	Base + 0x08C8
GPIO pin data input register 201	SIU_GPDI201	8-bits	Base + 0x08C9
GPIO pin data input register 202	SIU_GPDI202	8-bits	Base + 0x08CA
GPIO pin data input register 203	SIU_GPDI203	8-bits	Base + 0x08CB
GPIO pin data input register 204	SIU_GPDI204	8-bits	Base + 0x08CC
GPIO pin data input register 205	SIU_GPDI205	8-bits	Base + 0x08CD
GPIO pin data input register 206	SIU_GPDI206	8-bits	Base + 0x08CE
GPIO pin data input register 207	SIU_GPDI207	8-bits	Base + 0x08CF
GPIO pin data input register 208	SIU_GPDI208	8-bits	Base + 0x08D0

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
GPIO pin data input register 209	SIU_GPDI209	8-bits	Base + 0x08D1
GPIO pin data input register 210	SIU_GPDI210	8-bits	Base + 0x08D2
GPIO pin data input register 211	SIU_GPDI211	8-bits	Base + 0x08D3
GPIO pin data input register 212	SIU_GPDI212	8-bits	Base + 0x08D4
GPIO pin data input register 213	SIU_GPDI213	8-bits	Base + 0x08D5
Reserved	—	—	Base + (0x08D6–0x08FF)
eQADC trigger input select register	SIU_ETISR	32-bits	Base + 0x0900
External IRQ input select register	SIU_EIISR	32-bits	Base + 0x0904
DSPI input select register	SIU_DISR	32-bits	Base + 0x0908
Reserved	—	—	Base + (0x090C–0x097F)
Chip configuration register	SIU_CCR	32-bits	Base + 0x0980
External clock control register	SIU_ECCR	32-bits	Base + 0x0984
Compare A high register	SIU_CARH	32-bits	Base + 0x0988
Compare A low register	SIU_CARL	32-bits	Base + 0x098C
Compare B high register	SIU_CBRH	32-bits	Base + 0x0990
Compare B low register	SIU_CBRL	32-bits	Base + 0x0994
Reserved	—	—	Base + 0x0998–0xC3F9_FFFF
Enhanced Modular Input/Output Subsystem (eMIOS) Chapter 16, “Enhanced Modular Input/Output Subsystem (eMIOS)”			0xC3FA_0000
Module configuration register	EMIOS_MCR	32-bit	Base + 0x0000
Global flag register	EMIOS_GFR	32-bit	Base+ 0x0004
Output update disable register	EMIOS_OUDR	32-bit	Base + 0x0008
Reserved	—	—	Base + (0x000C–0x001F)
Unified channel *n*, where *n* = 0–23	UC base addresses (Acne)		Base + (0x0020 × (n+1))
Channel A data register n	EMIOS_CADRn	32-bit	UCnBase + 0x0000
Channel B data register n	EMIOS_CBDRn	32-bit	UCnBase + 0x0004
Channel counter register n	EMIOS_CCNTRn	32-bit	UCnBase + 0x0008
Channel control register n	EMIOS_CCRn	32-bit	UCnBase + 0x000C
Channel status register n	EMIOS_CSRn	32-bit	UCnBase + 0x0010
Reserved	—	—	UCnBase + 0x0014–0xC3FB_FFFF

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Enhanced Time Processing Unit (eTPU) Chapter 17, "Enhanced Time Processing Unit (eTPU)"			0xC3FC_0000
eTPU module configuration register	ETPU_MCR	32-bit	Base + 0x0000
eTPU coherent dual-parameter controller register	ETPU_CDCR	32-bit	Base + 0x0004
Reserved	—	—	Base + (0x0008–0x000B)
eTPU miscellaneous compare register	ETPU_MISCCMPR	32-bit	Base + 0x000C
eTPU SCM off-range data register	ETPU_SCMOFFDATAR	32-bit	Base + 0x0010
eTPU A engine configuration register	ETPU_ECR_A	32-bit	Base + 0x0014
eTPU B engine Configuration register	ETPU_ECR_B	32-bit	Base + 0x0018
Reserved	—	—	Base + (0x0018C–0x001F)
eTPU A time base configuration register	ETPU_TBCR_A	32-bit	Base + 0x0020
eTPU A time base 1	ETPU_TB1R_A	32-bit	Base + 0x0024
eTPU A time base 2	ETPU_TB2R_A	32-bit	Base + 0x0028
eTPU A STAC bus interface configuration register	ETPU_REDCR_A	32-bit	Base + 0x002C
Reserved	—	—	Base + (0x0030–0x01F03F)
eTPU B time base configuration register	ETPU_TBCR_B	32-bit	Base + 0x0040
eTPU B time base 1	ETPU_TB1R_B	32-bit	Base + 0x0044
eTPU B time base 2	ETPU_TB2R_B	32-bit	Base + 0x0048
eTPU B STAC bus interface configuration register	ETPU_REDCR_B	32-bit	Base + 0x004C
Reserved	—	—	Base + (0x0050–0x01FF)
eTPU A channel interrupt status register	ETPU_CISR_A	32-bit	Base + 0x0200
eTPU B channel interrupt status register	ETPU_CISR_B	32-bit	Base + 0x0204
Reserved	—	—	Base + (0x02048–0x020F)
eTPU A channel data transfer request status register	ETPU_CDTRSR_A	32-bit	Base + 0x0210
eTPU B channel data transfer request status register	ETPU_CDTRSR_B	32-bit	Base + 0x0214
Reserved	—	—	Base + (0x02148–0x021F)
eTPU A channel interrupt overflow status register	ETPU_CIOSR_A	32-bit	Base + 0x0220
eTPU B channel interrupt overflow status register	ETPU_CIOSR_B	32-bit	Base + 0x0224
Reserved	—	—	Base + (0x02248–0x022F)
eTPU A channel data transfer request overflow status register	ETPU_CDTROSR_A	32-bit	Base + 0x0230
eTPU B channel data transfer request overflow status register	ETPU_CDTROSR_B	32-bit	Base + 0x0234

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Reserved	—	—	Base + (0x02348–0x023F)
eTPU A channel interrupt enable register	ETPU_CIER_A	32-bit	Base + 0x0240
eTPU B channel interrupt enable register	ETPU_CIER_B	32-bit	Base + 0x0244
Reserved	—	—	Base + (0x02448–0x024F)
eTPU A channel data transfer request enable register	ETPU_CDTRER_A	32-bit	Base + 0x0250
eTPU B channel data transfer request enable register	ETPU_CDTRER_B	32-bit	Base + 0x0254
Reserved	—	—	Base + (0x02548–0x027F)
eTPU A channel pending service status register	ETPU_CPSSR_A	32-bit	Base + 0x0280
eTPU B channel pending service status register	ETPU_CPSSR_B	32-bit	Base + 0x0284
Reserved	—	—	Base + (0x02848–0x028F)
eTPU A channel service status register	ETPU_CSSR_A	32-bit	Base + 0x0290
eTPU B channel service status register	ETPU_CSSR_B	32-bit	Base + 0x0294
Reserved	—	—	Base + (0x02948–0x03FF)
eTPU A channel 0 configuration register	ETPU_C0CR_A	32-bit	Base + 0x0400
eTPU A channel 0 status and control register	ETPU_C0SCR_A	32-bit	Base + 0x0404
eTPU A channel 0 host service request register	ETPU_C0HSRR_A	32-bit	Base + 0x0408
Reserved	—	—	Base + (0x040C–0x040F)
eTPU A channel 1 configuration register	ETPU_C1CR_A	32-bit	Base + 0x0410
eTPU A channel 1 status and control register	ETPU_C1SCR_A	32-bit	Base + 0x0414
eTPU A channel 1 host service request register	ETPU_C1HSRR_A	32-bit	Base + 0x0418
Reserved	—	—	Base + (0x041C–0x041F)
eTPU A channel 2 configuration register	ETPU_C2CR_A	32-bit	Base + 0x0420
eTPU A channel 2 status and control register	ETPU_C2SCR_A	32-bit	Base + 0x0424
eTPU A channel 2 host service request register	ETPU_C2HSRR_A	32-bit	Base + 0x0428
Reserved	—	—	Base + (0x042C–0x042F)
eTPU A channel 3 configuration register	ETPU_C3CR_A	32-bit	Base + 0x0430
eTPU A channel 3 status and control register	ETPU_C3SCR_A	32-bit	Base + 0x0434
eTPU A channel 3 host service request register	ETPU_C3HSRR_A	32-bit	Base + 0x0438
Reserved	—	—	Base + (0x043C–0x043F)
eTPU A channel 4 configuration register	ETPU_C4CR_A	32-bit	Base + 0x0440
eTPU A channel 4 status and control register	ETPU_C4SCR_A	32-bit	Base + 0x0444
eTPU A channel 4 host service request register	ETPU_C4HSRR_A	32-bit	Base + 0x0448

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Reserved	—	—	Base + (0x044C–0x044F)
eTPU A channel 5 configuration register	ETPU_C5CR_A	32-bit	Base + 0x0450
eTPU A channel 5 status and control register	ETPU_C5SCR_A	32-bit	Base + 0x0454
eTPU A channel 5 host service request register	ETPU_C5HSRR_A	32-bit	Base + 0x0458
Reserved	—	—	Base + (0x045C–0x045F)
eTPU A channel 6 configuration register	ETPU_C6CR_A	32-bit	Base + 0x0460
eTPU A channel 6 status and control register	ETPU_C6SCR_A	32-bit	Base + 0x0464
eTPU A channel 6 host service request register	ETPU_C6HSRR_A	32-bit	Base + 0x0468
Reserved	—	—	Base + (0x046C–0x046F)
eTPU A channel 7 configuration register	ETPU_C7CR_A	32-bit	Base + 0x0470
eTPU A channel 7 status and control register	ETPU_C7SCR_A	32-bit	Base + 0x0474
eTPU A channel 7 host service request register	ETPU_C7HSRR_A	32-bit	Base + 0x0478
Reserved	—	—	Base + (0x047C–0x047F)
eTPU A channel 8 configuration register	ETPU_C8CR_A	32-bit	Base + 0x0480
eTPU A channel 8 status and control register	ETPU_C8SCR_A	32-bit	Base + 0x0484
eTPU A channel 8 host service request register	ETPU_C8HSRR_A	32-bit	Base + 0x0488
Reserved	—	—	Base + (0x048C–0x048F)
eTPU A channel 9 configuration register	ETPU_C9CR_A	32-bit	Base + 0x0490
eTPU A channel 9 status and control register	ETPU_C9SCR_A	32-bit	Base + 0x0494
eTPU A channel 9 host service request register	ETPU_C9HSRR_A	32-bit	Base + 0x0498
Reserved	—	—	Base + (0x049C–0x049F)
eTPU A channel 10 configuration register	ETPU_C10CR_A	32-bit	Base + 0x04A0
eTPU A channel 10 status and control register	ETPU_C10SCR_A	32-bit	Base + 0x04A4
eTPU A channel 10 host service request register	ETPU_C10HSRR_A	32-bit	Base + 0x04A8
Reserved	—	—	Base + (0x04AC–0x04AF)
eTPU A channel 11 configuration register	ETPU_C11CR_A	32-bit	Base + 0x04B0
eTPU A channel 11 status and control register	ETPU_C11SCR_A	32-bit	Base + 0x04B4
eTPU A channel 11 host service request register	ETPU_C11HSRR_A	32-bit	Base + 0x04B8
Reserved	—	—	Base + (0x04BC–0x04BF)
eTPU A channel 12 configuration register	ETPU_C12CR_A	32-bit	Base + 0x04C0
eTPU A channel 12 status and control register	ETPU_C12SCR_A	32-bit	Base + 0x04C4
eTPU A channel 12 host service request register	ETPU_C12HSRR_A	32-bit	Base + 0x04C8

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Reserved	—	—	Base + (0x04CC–0x04CF)
eTPU A channel 13 configuration register	ETPU_C13CR_A	32-bit	Base + 0x04D0
eTPU A channel 13 status and control register	ETPU_C13SCR_A	32-bit	Base + 0x04D4
eTPU A channel 13 host service request register	ETPU_C13HSRR_A	32-bit	Base + 0x04D8
Reserved	—	—	Base + (0x04DC–0x04DF)
eTPU A channel 14 configuration register	ETPU_C14CR_A	32-bit	Base + 0x04E0
eTPU A channel 14 status and control register	ETPU_C14SCR_A	32-bit	Base + 0x04E4
eTPU A channel 14 host service request register	ETPU_C14HSRR_A	32-bit	Base + 0x04E8
Reserved	—	—	Base + (0x04EC–0x04EF)
eTPU A channel 15 configuration register	ETPU_C15CR_A	32-bit	Base + 0x04F0
eTPU A channel 15 status and control register	ETPU_C15SCR_A	32-bit	Base + 0x04F4
eTPU A channel 15 host service request register	ETPU_C15HSRR_A	32-bit	Base + 0x04F8
Reserved	—	—	Base + (0x04FC–0x04FF)
eTPU A channel 16 configuration register	ETPU_C16CR_A	32-bit	Base + 0x0500
eTPU A channel 16 status and control register	ETPU_C16SCR_A	32-bit	Base + 0x0504
eTPU A channel 16 host service request register	ETPU_C16HSRR_A	32-bit	Base + 0x0508
Reserved	—	—	Base + (0x050C–0x050F)
eTPU A channel 17 configuration register	ETPU_C17CR_A	32-bit	Base + 0x0510
eTPU A channel 17 status and control register	ETPU_C17SCR_A	32-bit	Base + 0x0514
eTPU A channel 17 host service request register	ETPU_C17HSRR_A	32-bit	Base + 0x0518
Reserved	—	—	Base + (0x051C–0x051F)
eTPU A channel 18 configuration register	ETPU_C18CR_A	32-bit	Base + 0x0520
eTPU A channel 18 status and control register	ETPU_C18SCR_A	32-bit	Base + 0x0524
eTPU A channel 18 host service request register	ETPU_C18HSRR_A	32-bit	Base + 0x0528
Reserved	—	—	Base + (0x052C–0x052F)
eTPU A channel 19 configuration register	ETPU_C19CR_A	32-bit	Base + 0x0530
eTPU A channel 19 status and control register	ETPU_C19SCR_A	32-bit	Base + 0x0534
eTPU A channel 19 host service request register	ETPU_C19HSRR_A	32-bit	Base + 0x0538
Reserved	—	—	Base + (0x053C–0x053F)
eTPU A channel 20 configuration register	ETPU_C20CR_A	32-bit	Base + 0x0540
eTPU A channel 20 status and control register	ETPU_C20SCR_A	32-bit	Base + 0x0544
eTPU A channel 20 host service request register	ETPU_C20HSRR_A	32-bit	Base + 0x0548

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Reserved	—	—	Base + (0x054C–0x054F)
eTPU A channel 21 configuration register	ETPU_C21CR_A	32-bit	Base + 0x0550
eTPU A channel 21 status and control register	ETPU_C21SCR_A	32-bit	Base + 0x0554
eTPU A channel 21 host service request register	ETPU_C21HSRR_A	32-bit	Base + 0x0558
Reserved	—	—	Base + (0x055C–0x055F)
eTPU A channel 22 configuration register	ETPU_C22CR_A	32-bit	Base + 0x0560
eTPU A channel 22 status and control register	ETPU_C22SCR_A	32-bit	Base + 0x0564
eTPU A channel 22 host service request register	ETPU_C22HSRR_A	32-bit	Base + 0x0568
Reserved	—	—	Base + (0x056C–0x056F)
eTPU A channel 23 configuration register	ETPU_C23CR_A	32-bit	Base + 0x0570
eTPU A channel 23 status and control register	ETPU_C23CR_A	32-bit	Base + 0x0574
eTPU A channel 23 host service request register	ETPU_C23HSRR_A	32-bit	Base + 0x0578
Reserved	—	—	Base + (0x057C–0x057F)
eTPU A channel 24 configuration register	ETPU_C24CR_A	32-bit	Base + 0x0580
eTPU A channel 24 status and control register	ETPU_C24SCR_A	32-bit	Base + 0x0584
eTPU A channel 24 host service request register	ETPU_C24HSRR_A	32-bit	Base + 0x0588
Reserved	—	—	Base + (0x058C–0x058F)
eTPU A channel 25 configuration register	ETPU_C25CR_A	32-bit	Base + 0x0590
eTPU A channel 25 status and control register	ETPU_C25SCR_A	32-bit	Base + 0x0594
eTPU A channel 25 host service request register	ETPU_C25HSRR_A	32-bit	Base + 0x0598
Reserved	—	—	Base + (0x059C–0x059F)
eTPU A channel 26 configuration register	ETPU_C26CR_A	32-bit	Base + 0x05A0
eTPU A channel 26 status and control register	ETPU_C26SCR_A	32-bit	Base + 0x05A4
eTPU A channel 26 host service request register	ETPU_C26HSRR_A	32-bit	Base + 0x05A8
Reserved	—	—	Base + (0x05AC–0x05AF)
eTPU A channel 27 configuration register	ETPU_C27CR_A	32-bit	Base + 0x05B0
eTPU A channel 27 status and control register	ETPU_C27SCR_A	32-bit	Base + 0x05B4
eTPU A channel 27 host service request register	ETPU_C27HSRR_A	32-bit	Base + 0x05B8
Reserved	—	—	Base + (0x05BC–0x05BF)
eTPU A channel 28 configuration register	ETPU_C28CR_A	32-bit	Base + 0x05C0
eTPU A channel 28 status and control register	ETPU_C28SCR_A	32-bit	Base + 0x05C4
eTPU A channel 28 host service request register	ETPU_C28HSRR_A	32-bit	Base + 0x05C8

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Reserved	—	—	Base + (0x05CC–0x05CF)
eTPU A channel 29 configuration register	ETPU_C29CR_A	32-bit	Base + 0x05D0
eTPU A channel 29 status and control register	ETPU_C29SCR_A	32-bit	Base + 0x05D4
eTPU A channel 29 host service request register	ETPU_C29HSRR_A	32-bit	Base + 0x05D8
Reserved	—	—	Base + (0x05DC–0x05DF)
eTPU A channel 30 configuration register	ETPU_C30CR_A	32-bit	Base + 0x05E0
eTPU A channel 30 status and control register	ETPU_C30SCR_A	32-bit	Base + 0x05E4
eTPU A channel 30 host service request register	ETPU_C30HSRR_A	32-bit	Base + 0x05E8
Reserved	—	—	Base + (0x05EC–0x05EF)
eTPU A channel 31 configuration register	ETPU_C31CR_A	32-bit	Base + 0x05F0
eTPU A channel 31 status and control register	ETPU_C31SCR_A	32-bit	Base + 0x05F4
eTPU A channel 31 host service request register	ETPU_C31HSRR_A	32-bit	Base + 0x05F8
Reserved	—	—	Base + (0x05FC–0x07FF)
eTPU B channel 0 configuration register	ETPU_C0CR_B	32-bit	Base + 0x0800
eTPU B channel 0 status and control register	ETPU_C0SCR_B	32-bit	Base + 0x0804
eTPU B channel 0 host service request register	ETPU_C0HSRR_B	32-bit	Base + 0x0808
Reserved	—	—	Base + (0x080C–0x080F)
eTPU B channel 1 configuration register	ETPU_C1CR_B	32-bit	Base + 0x0810
eTPU B channel 1 status and control register	ETPU_C1SCR_B	32-bit	Base + 0x0814
eTPU B channel 1 host service request register	ETPU_C1HSRR_B	32-bit	Base + 0x0818
Reserved	—	—	Base + (0x081C–0x081F)
eTPU B channel 2 configuration register	ETPU_C2CR_B	32-bit	Base + 0x0820
eTPU B channel 2 status and control register	ETPU_C2SCR_B	32-bit	Base + 0x0824
eTPU B channel 2 host service request register	ETPU_C2HSRR_B	32-bit	Base + 0x0828
Reserved	—	—	Base + (0x082C–0x082F)
eTPU B channel 3 configuration register	ETPU_C3CR_B	32-bit	Base + 0x0830
eTPU B channel 3 status and control register	ETPU_C3SCR_B	32-bit	Base + 0x0834
eTPU B channel 3 host service request register	ETPU_C3HSRR_B	32-bit	Base + 0x0838
Reserved	—	—	Base + (0x083C–0x083F)
eTPU B channel 4 configuration register	ETPU_C4CR_B	32-bit	Base + 0x0840
eTPU B channel 4 status and control register	ETPU_C4SCR_B	32-bit	Base + 0x0844
eTPU B channel 4 host service request register	ETPU_C4HSRR_B	32-bit	Base + 0x0848

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Reserved	—	—	Base + (0x084C–0x084F)
eTPU B channel 5 configuration register	ETPU_C5CR_B	32-bit	Base + 0x0850
eTPU B channel 5 status and control register	ETPU_C5SCR_B	32-bit	Base + 0x0854
eTPU B channel 5 host service request register	ETPU_C5HSRR_B	32-bit	Base + 0x0858
Reserved	—	—	Base + (0x085C–0x085F)
eTPU B channel 6 configuration register	ETPU_C6CR_B	32-bit	Base + 0x0860
eTPU B channel 6 status and control register	ETPU_C6SCR_B	32-bit	Base + 0x0864
eTPU B channel 6 host service request register	ETPU_C6HSRR_B	32-bit	Base + 0x0868
Reserved	—	—	Base + (0x086C–0x086F)
eTPU B channel 7 configuration register	ETPU_C7CR_B	32-bit	Base + 0x0870
eTPU B channel 7 status and control register	ETPU_C7SCR_B	32-bit	Base + 0x0874
eTPU B channel 7 host service request register	ETPU_C7HSRR_B	32-bit	Base + 0x0878
Reserved	—	—	Base + (0x087C–0x087F)
eTPU B channel 8 configuration register	ETPU_C8CR_B	32-bit	Base + 0x0880
eTPU B channel 8 status and control register	ETPU_C8SCR_B	32-bit	Base + 0x0884
eTPU B channel 8 host service request register	ETPU_C8HSRR_B	32-bit	Base + 0x0888
Reserved	—	—	Base + (0x088C–0088F)
eTPU B channel 9 configuration register	ETPU_C9CR_B	32-bit	Base + 0x0890
eTPU B channel 9 status and control register	ETPU_C9SCR_B	32-bit	Base + 0x0894
eTPU B channel 9 host service request register	ETPU_C9HSRR_B	32-bit	Base + 0x0898
Reserved	—	—	Base + (0x081C–0x081F)
eTPU B channel 10 configuration register	ETPU_C10CR_B	32-bit	Base + 0x08A0
eTPU B channel 10 status and control register	ETPU_C10SCR_B	32-bit	Base + 0x08A4
eTPU B channel 10 host service request register	ETPU_C10HSRR_B	32-bit	Base + 0x08A8
Reserved	—	—	Base + (0x08AC–0x08AF)
eTPU B channel 11 configuration register	ETPU_C11CR_B	32-bit	Base + 0x08B0
eTPU B channel 11 status and control register	ETPU_C11SCR_B	32-bit	Base + 0x08B4
eTPU B channel 11 host service request register	ETPU_C11HSRR_B	32-bit	Base + 0x08B8
Reserved	—	—	Base + (0x08BC–0x08BF)
eTPU B channel 12 configuration register	ETPU_C12CR_B	32-bit	Base + 0x08C0
eTPU B channel 12 status and control register	ETPU_C12SCR_B	32-bit	Base + 0x08C4
eTPU B channel 12 host service request register	ETPU_C12HSRR_B	32-bit	Base + 0x08C8

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Reserved	—	—	Base + (0x08CC–0x08CF)
eTPU B channel 13 configuration register	ETPU_C13CR_B	32-bit	Base + 0x08D0
eTPU B channel 13 status and control register	ETPU_C13SCR_B	32-bit	Base + 0x08D4
eTPU B channel 13 host service request register	ETPU_C13HSRR_B	32-bit	Base + 0x08D8
Reserved	—	—	Base + (0x08DC–0x08DF)
eTPU B channel 14 configuration register	ETPU_C14CR_B	32-bit	Base + 0x08E0
eTPU B channel 14 status and control register	ETPU_C14SCR_B	32-bit	Base + 0x08E4
eTPU B channel 14 host service request register	ETPU_C14HSRR_B	32-bit	Base + 0x08E8
Reserved	—	—	Base + (0x08EC–0x08EF)
eTPU B channel 15 configuration register	ETPU_C15CR_B	32-bit	Base + 0x08F0
eTPU B channel 15 status and control register	ETPU_C15SCR_B	32-bit	Base + 0x08F4
eTPU B channel 15 host service request register	ETPU_C15HSRR_B	32-bit	Base + 0x08F8
Reserved	—	—	Base + (0x08FC–0x08FF)
eTPU B channel 16 configuration register	ETPU_C16CR_B	32-bit	Base + 0x0900
eTPU B channel 16 status and control register	ETPU_C16SCR_B	32-bit	Base + 0x0904
eTPU B channel 16 host service request register	ETPU_C16HSRR_B	32-bit	Base + 0x0908
Reserved	—	—	Base + (0x090C–0x090F)
eTPU B channel 17 configuration register	ETPU_C17CR_B	32-bit	Base + 0x0910
eTPU B channel 17 status and control register	ETPU_C17SCR_B	32-bit	Base + 0x0914
eTPU B channel 17 host service request register	ETPU_C17HSRR_B	32-bit	Base + 0x0918
Reserved	—	—	Base + (0x091C–0x091F)
eTPU B channel 18 configuration register	ETPU_C18CR_B	32-bit	Base + 0x0920
eTPU B channel 18 status and control register	ETPU_C18SCR_B	32-bit	Base + 0x0924
eTPU B channel 18 host service request register	ETPU_C18HSRR_B	32-bit	Base + 0x0928
Reserved	—	—	Base + (0x092C–0x092F)
eTPU B channel 19 configuration register	ETPU_C19CR_B	32-bit	Base + 0x0930
eTPU B channel 19 status and control register	ETPU_C19SCR_B	32-bit	Base + 0x0934
eTPU B channel 19 host service request register	ETPU_C19HSRR_B	32-bit	Base + 0x0938
Reserved	—	—	Base + (0x093C–0x093F)
eTPU B channel 20 configuration register	ETPU_C20CR_B	32-bit	Base + 0x0940
eTPU B channel 20 status and control register	ETPU_C20SCR_B	32-bit	Base + 0x0944
eTPU B channel 20 host service request register	ETPU_C20HSRR_B	32-bit	Base + 0x0948

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Reserved	—	—	Base + (0x094C–0x094F)
eTPU B channel 21 configuration register	ETPU_C21CR_B	32-bit	Base + 0x0950
eTPU B channel 21 status and control register	ETPU_C21SCR_B	32-bit	Base + 0x0954
eTPU B channel 21 host service request register	ETPU_C21HSRR_B	32-bit	Base + 0x0958
Reserved	—	—	Base + (0x095C–0x095F)
eTPU B channel 22 configuration register	ETPU_C22CR_B	32-bit	Base + 0x0960
eTPU B channel 22 status and control register	ETPU_C22SCR_B	32-bit	Base + 0x0964
eTPU B channel 22 host service request register	ETPU_C22HSRR_B	32-bit	Base + 0x0968
Reserved	—	—	Base + (0x096C–0x096F)
eTPU B channel 23 configuration register	ETPU_C23CR_B	32-bit	Base + 0x0970
eTPU B channel 23 status and control register	ETPU_C23SCR_B	32-bit	Base + 0x0974
eTPU B channel 23 host service request register	ETPU_C23HSRR_B	32-bit	Base + 0x0978
Reserved	—	—	Base + (0x097C–0x097F)
eTPU B channel 24 configuration register	ETPU_C24CR_B	32-bit	Base + 0x0980
eTPU B channel 24 status and control register	ETPU_C24SCR_B	32-bit	Base + 0x0984
eTPU B channel 24 host service request register	ETPU_C24HSRR_B	32-bit	Base + 0x0988
Reserved	—	—	Base + (0x098C–0x098F)
eTPU B channel 25 configuration register	ETPU_C25CR_B	32-bit	Base + 0x0990
eTPU B channel 25 status and control register	ETPU_C25SCR_B	32-bit	Base + 0x0994
eTPU B channel 25 host service request register	ETPU_C25HSRR_B	32-bit	Base + 0x0998
Reserved	—	—	Base + (0x099C–0x099F)
eTPU B channel 26 configuration register	ETPU_C26CR_B	32-bit	Base + 0x09A0
eTPU B channel 26 status and control register	ETPU_C26SCR_B	32-bit	Base + 0x09A4
eTPU B channel 26 host service request register	ETPU_C26HSRR_B	32-bit	Base + 0x09A8
Reserved	—	—	Base + (0x09AC–0x09AF)
eTPU B channel 27 configuration register	ETPU_C27CR_B	32-bit	Base + 0x09B0
eTPU B channel 27 status and control register	ETPU_C27SCR_B	32-bit	Base + 0x09B4
eTPU B channel 27 host service request register	ETPU_C27HSRR_B	32-bit	Base + 0x09B8
Reserved	—	—	Base + (0x09BC–0x09BF)
eTPU B channel 28 configuration register	ETPU_C28CR_B	32-bit	Base + 0x09C0
eTPU B channel 28 status and control register	ETPU_C28SCR_B	32-bit	Base + 0x09C4
eTPU B channel 28 host service request register	ETPU_C28HSRR_B	32-bit	Base + 0x09C8

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Reserved	—	—	Base + (0x09CC–0x09CF)
eTPU B channel 29 configuration register	ETPU_C29CR_B	32-bit	Base + 0x09D0
eTPU B channel 29 status and control register	ETPU_C29SCR_B	32-bit	Base + 0x09D4
eTPU B channel 29 host service request register	ETPU_C29HSRR_B	32-bit	Base + 0x09D8
Reserved	—	—	Base + (0x09DC–0x09DF)
eTPU B channel 30 configuration register	ETPU_C30CR_B	32-bit	Base + 0x09E0
eTPU B channel 30 status and control register	ETPU_C30SCR_B	32-bit	Base + 0x09E4
eTPU B channel 30 host service request register	ETPU_C30HSRR_B	32-bit	Base + 0x09E8
Reserved	—	—	Base + (0x09EC–0x09EF)
eTPU B channel 31 configuration register	ETPU_C31CR_B	32-bit	Base + 0x09F0
eTPU B channel 31 status and control register	ETPU_C31SCR_B	32-bit	Base + 0x09F4
eTPU B channel 31 host service request register	ETPU_C31HSRR_B	32-bit	Base + 0x09F8
Reserved	—	—	Base + (0x09FC–0x7FFF)
Shared data memory (parameter RAM)	SDM	3 KB	Base + (0x8000–0x8BFF)
Reserved	—	—	Base + (0x8C00–0xBFFF)
SDM PSE mirror			Base + (0xC000–0xCBFF)
Reserved	—	—	Base + (0xCC00–0xFFFF)
Shared code memory	SCM	12 KB 20 KB	Base + (0x0001_0000–0x0001_2FFF) (0x0001_0000–0x0001_4FFF)
Reserved	—	—	Base + (0x0001_4000–FFEF_FFFF)
Peripheral Bridge B (PBRIDGEB) Chapter 5, “Peripheral Bridge (PBRIDGE A and PBRIDGE B)”			0xFFF0_0000
Peripheral bridge B master privilege control register	PBRIDGEB_MPCR	32-bit	Base + 0x0000
Reserved	—	—	Base + (0x0004–0x001F)
Peripheral bridge B peripheral access control register 0	PBRIDGEB_PACR0	32-bit	Base + 0x0020
Reserved	—	—	Base + (0x0024–0x0027)
Peripheral bridge B peripheral access control register 2	PBRIDGEB_PACR2	32-bit	Base + 0x0028
Reserved	—	—	Base + (0x002C–0x003F)
Peripheral bridge B off-platform peripheral access control register 0	PBRIDGEB_OPACR0	32-bit	Base + 0x0040

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Peripheral bridge B off-platform peripheral access control register 1	PBRIDGEB_OPACR1	32-bit	Base + 0x0044
Peripheral bridge B off-platform peripheral access control register 2	PBRIDGEB_OPACR2	32-bit	Base + 0x0048
Peripheral bridge B off-platform peripheral access control register 3	PBRIDGEB_OPACR3	32-bit	Base + 0x004C
Reserved	—	—	(Base + 0x0050)–0xFFF0_3FFF
System Bus Crossbar Switch (XBAR) Chapter 7, “Crossbar Switch (XBAR)”			0xFFF0_4000
Master priority register 0	XBAR_MPR0	32-bit	Base + 0x0000
Reserved	—	—	Base + (0x0004–0x000F)
Slave general purpose control register 0	XBAR_SGPCR0	32-bit	Base + 0x0010
Reserved	—	—	Base + (0x0014–0x00FF)
Master priority register 1	XBAR_MPR1	32-bit	Base + 0x0100
Reserved	—	—	Base + (0x0104–0x010F)
Slave general purpose control register 1	XBAR_SGPCR1	32-bit	Base + 0x0110
Reserved	—	—	Base + (0x0114–0x02FF)
Master priority register 3	XBAR_MPR3	32-bit	Base + 0x0300
Reserved	—	—	Base + (0x0304–0x030F)
Slave general purpose control register 3	XBAR_SGPCR3	32-bit	Base + 0x0310
Reserved	—	—	Base + (0x0314–0x05FF)
Master priority register 6	XBAR_MPR6	32-bit	Base + 0x0600
Reserved	—	—	Base + (0x0604–0x060F)
Slave general purpose control register 6	XBAR_SGPCR6	32-bit	Base + 0x0610
Reserved	—	—	Base + (0x0614–0x06FF)
Master priority register 7	XBAR_MPR7	32-bit	Base + 0x0700
Reserved	—	—	Base + (0x0704–0x070F)
Slave general purpose control register 7	XBAR_SGPCR7	32-bit	Base + 0x0710
Reserved	—	—	(Base + 0x0714)–0xFFF4_3FFF
Chapter 8, “Error Correction Status Module”			0xFFF4_0000
Reserved	—	—	Base + (0x0000–0x0015)
Software watchdog timer control register	ECSM_SWTCR [1]	16-bit	Base + 0x0016
Reserved	—	—	Base + (0x0018–0x001A)
Software watchdog timer service register	ECSM_SWTSR [1]	8-bit	Base + 0x001B

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Reserved	—	—	Base + (0x001C–0x001E)
Software watchdog timer interrupt register	ECSM_SWTIR [1]	8-bit	Base + 0x001F
Reserved	—		Base + (0x0020–0x0023)
FEC Burst Optimization Master Control register	FBOMCR	32-bit	Base + 0x0024
Reserved	—	—	Base + (0x0028–0x0042)
ECC configuration register	ECSM_ECR	8-bit	Base + 0x0043
Reserved	—	—	Base + (0x0044–0x0046)
ECC status register	ECSM_ESR	8-bit	Base + 0x0047
Reserved	—	—	Base + (0x0048–0x0049)
ECC error generation register	ECSM_EEGR	16-bit	Base + 0x004A
Reserved	—	—	Base + (0x004C–0x004F)
Flash ECC address register	ECSM_FEAR	32-bit	Base + 0x0050
Reserved	—	—	Base + (0x0054–0x0055)
Flash ECC master number register	ECSM_FEMR	8-bit	Base + 0x0056
Flash ECC attributes register	ECSM_FEAT	8-bit	Base + 0x0057
Flash ECC data register high	ECSM_FEDRH	32-bit	Base + 0x0058
Flash ECC data register low	ECSM_FEDRL	32-bit	Base + 0x005C
RAM ECC address register	ECSM_REAR	32-bit	Base + 0x0060
Reserved	—	—	Base + (0x0064–0x0065)
RAM ECC master number register	ECSM_REMR	8-bit	Base + 0x0066
RAM ECC attributes register	ECSM_REAT	8-bit	Base + 0x0067
RAM ECC data register high	ECSM_REDRH	32-bit	Base + 0x0068
RAM ECC data register low	ECSM_REDRL	32-bit	Base + 0x006C
Reserved	—	—	(Base + 0x0070)–0xFFF4_3FFF
Enhanced Direct Memory Access (eDMA) Chapter 9, “Enhanced Direct Memory Access (eDMA)”			0xFFF4_4000
Control register	EDMA_CR	32-bit	Base + 0x0000
Error status register	EDMA_ESR	32-bit	Base + 0x0004
Reserved	—	—	Base + (0x0008)
Enable request register low	EDMA_ERQRL	32-bit	Base + 0x000C
Reserved	—	—	Base + (0x0010)
Enable error interrupt register low	EDMA_EEIRL	32-bit	Base + 0x0014

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Set enable request register	EDMA_SERQR	8-bit	Base + 0x0018
Clear enable request register	EDMA_CERQR	8-bit	Base + 0x0019
Set enable error interrupt register	EDMA_SEEIR	8-bit	Base + 0x001A
Clear enable error interrupt request register	EDMA_CEEIR	8-bit	Base + 0x001B
Clear interrupt request register	EDMA_CIRQR	8-bit	Base + 0x001C
Clear error register	EDMA_CER	8-bit	Base + 0x001D
Set START bit register	EDMA_SSBR	8-bit	Base + 0x001E
Clear DONE status bit register	EDMA_CDSBR	8-bit	Base + 0x001F
Reserved	—	—	Base + 0x0020
Interrupt request register low	EDMA_IRQRL	32-bit	Base + 0x0024
Reserved	—	—	Base + 0x0028
Error register low	EDMA_ERL	32-bit	Base + 0x002C
Reserved	—	—	Base + (0x0030–0x00FF)
Channel priority register 0	EDMA_CPR0	8-bit	Base + 0x0100
Channel priority register 1	EDMA_CPR1	8-bit	Base + 0x0101
Channel priority register 2	EDMA_CPR2	8-bit	Base + 0x0102
Channel priority register 3	EDMA_CPR3	8-bit	Base + 0x0103
Channel priority register 4	EDMA_CPR4	8-bit	Base + 0x0104
Channel priority register 5	EDMA_CPR5	8-bit	Base + 0x0105
Channel priority register 6	EDMA_CPR6	8-bit	Base + 0x0106
Channel priority register 7	EDMA_CPR7	8-bit	Base + 0x0107
Channel priority register 8	EDMA_CPR8	8-bit	Base + 0x0108
Channel priority register 9	EDMA_CPR9	8-bit	Base + 0x0109
Channel priority register 10	EDMA_CPR10	8-bit	Base + 0x010A
Channel priority register 11	EDMA_CPR11	8-bit	Base + 0x010B
Channel priority register 12	EDMA_CPR12	8-bit	Base + 0x010C
Channel priority register 13	EDMA_CPR13	8-bit	Base + 0x010D
Channel priority register 14	EDMA_CPR14	8-bit	Base + 0x010E
Channel priority register 15	EDMA_CPR15	8-bit	Base + 0x010F
Channel priority register 16	EDMA_CPR16	8-bit	Base + 0x0110
Channel priority register 17	EDMA_CPR17	8-bit	Base + 0x0111
Channel priority register 18	EDMA_CPR18	8-bit	Base + 0x0112

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Channel priority register 19	EDMA_CPR19	8-bit	Base + 0x0113
Channel priority register 20	EDMA_CPR20	8-bit	Base + 0x0114
Channel priority register 21	EDMA_CPR21	8-bit	Base + 0x0115
Channel priority register 22	EDMA_CPR22	8-bit	Base + 0x0116
Channel priority register 23	EDMA_CPR23	8-bit	Base + 0x0117
Channel priority register 24	EDMA_CPR24	8-bit	Base + 0x0118
Channel priority register 25	EDMA_CPR25	8-bit	Base + 0x0119
Channel priority register 26	EDMA_CPR26	8-bit	Base + 0x011A
Channel priority register 27	EDMA_CPR27	8-bit	Base + 0x011B
Channel priority register 28	EDMA_CPR28	8-bit	Base + 0x011C
Channel priority register 29	EDMA_CPR29	8-bit	Base + 0x011D
Channel priority register 30	EDMA_CPR30	8-bit	Base + 0x011E
Channel priority register 31	EDMA_CPR31	8-bit	Base + 0x011F
Channel priority register 32	EDMA_CPR32	8-bit	Base + 0x0120
Channel priority register 33	EDMA_CPR33	8-bit	Base + 0x0121
Channel priority register 34	EDMA_CPR34	8-bit	Base + 0x0122
Channel priority register 35	EDMA_CPR35	8-bit	Base + 0x0123
Channel priority register 36	EDMA_CPR36	8-bit	Base + 0x0124
Channel priority register 37	EDMA_CPR37	8-bit	Base + 0x0125
Channel priority register 38	EDMA_CPR38	8-bit	Base + 0x0126
Channel priority register 39	EDMA_CPR39	8-bit	Base + 0x0127
Channel priority register 40	EDMA_CPR40	8-bit	Base + 0x0128
Channel priority register 41	EDMA_CPR41	8-bit	Base + 0x0129
Channel priority register 42	EDMA_CPR42	8-bit	Base + 0x012A
Channel priority register 43	EDMA_CPR43	8-bit	Base + 0x012B
Channel priority register 44	EDMA_CPR44	8-bit	Base + 0x012C
Channel priority register 45	EDMA_CPR45	8-bit	Base + 0x012D
Channel priority register 46	EDMA_CPR46	8-bit	Base + 0x012E
Channel priority register 47	EDMA_CPR47	8-bit	Base + 0x012F
Channel priority register 48	EDMA_CPR48	8-bit	Base + 0x0130
Channel priority register 49	EDMA_CPR49	8-bit	Base + 0x0131
Channel priority register 50	EDMA_CPR50	8-bit	Base + 0x0132

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Channel priority register 51	EDMA_CPR51	8-bit	Base + 0x0133
Channel priority register 52	EDMA_CPR52	8-bit	Base + 0x0134
Channel priority register 53	EDMA_CPR53	8-bit	Base + 0x0135
Channel priority register 54	EDMA_CPR54	8-bit	Base + 0x0136
Channel priority register 55	EDMA_CPR55	8-bit	Base + 0x0137
Channel priority register 56	EDMA_CPR56	8-bit	Base + 0x0138
Channel priority register 57	EDMA_CPR57	8-bit	Base + 0x0139
Channel priority register 58	EDMA_CPR58	8-bit	Base + 0x013A
Channel priority register 59	EDMA_CPR59	8-bit	Base + 0x013B
Channel priority register 60	EDMA_CPR60	8-bit	Base + 0x013C
Channel priority register 61	EDMA_CPR61	8-bit	Base + 0x013D
Channel priority register 62	EDMA_CPR62	8-bit	Base + 0x013E
Channel priority register 63	EDMA_CPR63	8-bit	Base + 0x013F
Reserved	—	—	Base + (0x0140–0x0FFF)
Transfer control descriptor register 0	TCD0	256-bit	Base + 0x1000
Transfer control descriptor register 1	TCD1	256-bit	Base + 0x1020
Transfer control descriptor register 2	TCD2	256-bit	Base + 0x1040
Transfer control descriptor register 3	TCD3	256-bit	Base + 0x1060
Transfer control descriptor register 4	TCD4	256-bit	Base + 0x1080
Transfer control descriptor register 5	TCD5	256-bit	Base + 0x10A0
Transfer control descriptor register 6	TCD6	256-bit	Base + 0x10C0
Transfer control descriptor register 7	TCD7	256-bit	Base + 0x10E0
Transfer control descriptor register 8	TCD8	256-bit	Base + 0x1100
Transfer control descriptor register 9	TCD9	256-bit	Base + 0x1120
Transfer control descriptor register 10	TCD10	256-bit	Base + 0x1140
Transfer control descriptor register 11	TCD11	256-bit	Base + 0x1160
Transfer control descriptor register 12	TCD12	256-bit	Base + 0x1180
Transfer control descriptor register 13	TCD13	256-bit	Base + 0x11A0
Transfer control descriptor register 14	TCD14	256-bit	Base + 0x11C0
Transfer control descriptor register 15	TCD15	256-bit	Base + 0x11E0
Transfer control descriptor register 16	TCD16	256-bit	Base + 0x1200
Transfer control descriptor register 17	TCD17	256-bit	Base + 0x1220

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Transfer control descriptor register 18	TCD18	256-bit	Base + 0x1240
Transfer control descriptor register 19	TCD19	256-bit	Base + 0x1260
Transfer control descriptor register 20	TCD20	256-bit	Base + 0x1280
Transfer control descriptor register 21	TCD21	256-bit	Base + 0x12A0
Transfer control descriptor register 22	TCD22	256-bit	Base + 0x12C0
Transfer control descriptor register 23	TCD23	256-bit	Base + 0x12E0
Transfer control descriptor register 24	TCD24	256-bit	Base + 0x1300
Transfer control descriptor register 25	TCD25	256-bit	Base + 0x1320
Transfer control descriptor register 26	TCD26	256-bit	Base + 0x1340
Transfer control descriptor register 27	TCD27	256-bit	Base + 0x1360
Transfer control descriptor register 28	TCD28	256-bit	Base + 0x1380
Transfer control descriptor register 29	TCD29	256-bit	Base + 0x13A0
Transfer control descriptor register 30	TCD30	256-bit	Base + 0x13C0
Transfer control descriptor register 31	TCD31	256-bit	Base + 0x13E0
Transfer control descriptor register 32	TCD32	256-bit	Base + 0x1400
Transfer control descriptor register 33	TCD33	256-bit	Base + 0x1420
Transfer control descriptor register 34	TCD34	256-bit	Base + 0x1440
Transfer control descriptor register 35	TCD35	256-bit	Base + 0x1460
Transfer control descriptor register 36	TCD36	256-bit	Base + 0x1480
Transfer control descriptor register 37	TCD37	256-bit	Base + 0x14A0
Transfer control descriptor register 38	TCD38	256-bit	Base + 0x14C0
Transfer control descriptor register 39	TCD39	256-bit	Base + 0x14E0
Transfer control descriptor register 40	TCD40	256-bit	Base + 0x1500
Transfer control descriptor register 41	TCD41	256-bit	Base + 0x1520
Transfer control descriptor register 42	TCD42	256-bit	Base + 0x1540
Transfer control descriptor register 43	TCD43	256-bit	Base + 0x1560
Transfer control descriptor register 44	TCD44	256-bit	Base + 0x1580
Transfer control descriptor register 45	TCD45	256-bit	Base + 0x15A0
Transfer control descriptor register 46	TCD46	256-bit	Base + 0x15C0
Transfer control descriptor register 47	TCD47	256-bit	Base + 0x15E0
Transfer control descriptor register 48	TCD48	256-bit	Base + 0x1600
Transfer control descriptor register 49	TCD49	256-bit	Base + 0x1620

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Transfer control descriptor register 50	TCD50	256-bit	Base + 0x1640
Transfer control descriptor register 51	TCD51	256-bit	Base + 0x1660
Transfer control descriptor register 52	TCD52	256-bit	Base + 0x1680
Transfer control descriptor register 53	TCD53	256-bit	Base + 0x16A0
Transfer control descriptor register 54	TCD54	256-bit	Base + 0x16C0
Transfer control descriptor register 55	TCD55	256-bit	Base + 0x16E0
Transfer control descriptor register 56	TCD56	256-bit	Base + 0x1700
Transfer control descriptor register 57	TCD57	256-bit	Base + 0x1720
Transfer control descriptor register 58	TCD58	256-bit	Base + 0x1740
Transfer control descriptor register 59	TCD59	256-bit	Base + 0x1760
Transfer control descriptor register 60	TCD60	256-bit	Base + 0x1780
Transfer control descriptor register 61	TCD61	256-bit	Base + 0x17A0
Transfer control descriptor register 62	TCD62	256-bit	Base + 0x17C0
Transfer control descriptor register 63	TCD63	256-bit	Base + 0x17E0
Reserved	—	—	(Base + 0x1800)–0xFFF4_7FFF
Interrupt Controller (INTC) Chapter 10, “Interrupt Controller (INTC)”			0xFFF4_8000
Module configuration register	INTC_MCR	32-bit	Base + 0x0000
Reserved	—	—	Base + (0x0004–0x0007)
Current priority register	INTC_CPR	32-bit	Base + 0x0008
Reserved	—	—	Base + (0x000C–0x000F)
interrupt acknowledge register	INTC_IACKR	32-bit	Base + 0x0010
Reserved	—	—	Base + (0x0014–0x0017)
End of interrupt register	INTC_EOIR	32-bit	Base + 0x0018
Reserved	—	—	Base + (0x001C–0x001F)
Software set/clear interrupt register 0	INTC_SSCIR0	8-bit	Base + 0x0020
Software set/clear interrupt register 1	INTC_SSCIR1	8-bit	Base + 0x0021
Software set/clear interrupt register 2	INTC_SSCIR2	8-bit	Base + 0x0022
Software set/clear interrupt register 3	INTC_SSCIR3	8-bit	Base + 0x0023
Software set/clear interrupt register 4	INTC_SSCIR4	8-bit	Base + 0x0024
Software set/clear interrupt register 5	INTC_SSCIR5	8-bit	Base + 0x0025
Software set/clear interrupt register 6	INTC_SSCIR6	8-bit	Base + 0x0026

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Software set/clear interrupt register 7	INTC_SSCIR7	8-bit	Base + 0x0027
Reserved	—	—	Base + (0x0028–0x003F)
Priority select register 0	INTC_PSR0	8-bit	Base + 0x0040
Priority select register 1	INTC_PSR1	8-bit	Base + 0x0041
Priority select register 2	INTC_PSR2	8-bit	Base + 0x0042
Priority select register 3	INTC_PSR3	8-bit	Base + 0x0043
Priority select register 4	INTC_PSR4	8-bit	Base + 0x0044
Priority select register 5	INTC_PSR5	8-bit	Base + 0x0045
Priority select register 6	INTC_PSR6	8-bit	Base + 0x0046
Priority select register 7	INTC_PSR7	8-bit	Base + 0x0047
Priority select register 8	INTC_PSR8	8-bit	Base + 0x0048
Priority select register 9	INTC_PSR9	8-bit	Base + 0x0049
Priority select register 10	INTC_PSR10	8-bit	Base + 0x004A
Priority select register 11	INTC_PSR11	8-bit	Base + 0x004B
Priority select register 12	INTC_PSR12	8-bit	Base + 0x004C
Priority select register 13	INTC_PSR13	8-bit	Base + 0x004D
Priority select register 14	INTC_PSR14	8-bit	Base + 0x004E
Priority select register 15	INTC_PSR15	8-bit	Base + 0x004F
Priority select register 16	INTC_PSR16	8-bit	Base + 0x0050
Priority select register 17	INTC_PSR17	8-bit	Base + 0x0051
Priority select register 18	INTC_PSR18	8-bit	Base + 0x0052
Priority select register 19	INTC_PSR19	8-bit	Base + 0x0053
Priority select register 20	INTC_PSR20	8-bit	Base + 0x0054
Priority select register 21	INTC_PSR21	8-bit	Base + 0x0055
Priority select register 22	INTC_PSR22	8-bit	Base + 0x0056
Priority select register 23	INTC_PSR23	8-bit	Base + 0x0057
Priority select register 24	INTC_PSR24	8-bit	Base + 0x0058
Priority select register 25	INTC_PSR25	8-bit	Base + 0x0059
Priority select register 26	INTC_PSR26	8-bit	Base + 0x005A
Priority select register 27	INTC_PSR27	8-bit	Base + 0x005B
Priority select register 28	INTC_PSR28	8-bit	Base + 0x005C
Priority select register 29	INTC_PSR29	8-bit	Base + 0x005D

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Priority select register 30	INTC_PSR30	8-bit	Base + 0x005E
Priority select register 31	INTC_PSR31	8-bit	Base + 0x005F
Priority select register 32	INTC_PSR32	8-bit	Base + 0x0060
Priority select register 33	INTC_PSR33	8-bit	Base + 0x0061
Priority select register 34	INTC_PSR34	8-bit	Base + 0x0062
Priority select register 35	INTC_PSR35	8-bit	Base + 0x0063
Priority select register 36	INTC_PSR36	8-bit	Base + 0x0064
Priority select register 37	INTC_PSR37	8-bit	Base + 0x0065
Priority select register 38	INTC_PSR38	8-bit	Base + 0x0066
Priority select register 39	INTC_PSR39	8-bit	Base + 0x0067
Priority select register 40	INTC_PSR40	8-bit	Base + 0x0068
Priority select register 41	INTC_PSR41	8-bit	Base + 0x0069
Priority select register 42	INTC_PSR42	8-bit	Base + 0x006A
Priority select register 43	INTC_PSR43	8-bit	Base + 0x006B
Priority select register 44	INTC_PSR44	8-bit	Base + 0x006C
Priority select register 45	INTC_PSR45	8-bit	Base + 0x006D
Priority select register 46	INTC_PSR46	8-bit	Base + 0x006E
Priority select register 47	INTC_PSR47	8-bit	Base + 0x006F
Priority select register 48	INTC_PSR48	8-bit	Base + 0x0070
Priority select register 49	INTC_PSR49	8-bit	Base + 0x0071
Priority select register 50	INTC_PSR50	8-bit	Base + 0x0072
Priority select register 51	INTC_PSR51	8-bit	Base + 0x0073
Priority select register 52	INTC_PSR52	8-bit	Base + 0x0074
Priority select register 53	INTC_PSR53	8-bit	Base + 0x0075
Priority select register 54	INTC_PSR54	8-bit	Base + 0x0076
Priority select register 55	INTC_PSR55	8-bit	Base + 0x0077
Priority select register 56	INTC_PSR56	8-bit	Base + 0x0078
Priority select register 57	INTC_PSR57	8-bit	Base + 0x0079
Priority select register 58	INTC_PSR58	8-bit	Base + 0x007A
Priority select register 59	INTC_PSR59	8-bit	Base + 0x007B
Priority select register 60	INTC_PSR60	8-bit	Base + 0x007C
Priority select register 61	INTC_PSR61	8-bit	Base + 0x007D

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Priority select register 62	INTC_PSR62	8-bit	Base + 0x007E
Priority select register 63	INTC_PSR63	8-bit	Base + 0x007F
Priority select register 64	INTC_PSR64	8-bit	Base + 0x0080
Priority select register 65	INTC_PSR65	8-bit	Base + 0x0081
Priority select register 66	INTC_PSR66	8-bit	Base + 0x0082
Priority select register 67	INTC_PSR67	8-bit	Base + 0x0083
Priority select register 68	INTC_PSR68	8-bit	Base + 0x0084
Priority select register 69	INTC_PSR69	8-bit	Base + 0x0085
Priority select register 70	INTC_PSR70	8-bit	Base + 0x0086
Priority select register 71	INTC_PSR71	8-bit	Base + 0x0087
Priority select register 72	INTC_PSR72	8-bit	Base + 0x0088
Priority select register 73	INTC_PSR73	8-bit	Base + 0x0089
Priority select register 74	INTC_PSR74	8-bit	Base + 0x008A
Priority select register 75	INTC_PSR75	8-bit	Base + 0x008B
Priority select register 76	INTC_PSR76	8-bit	Base + 0x008C
Priority select register 77	INTC_PSR77	8-bit	Base + 0x008D
Priority select register 78	INTC_PSR78	8-bit	Base + 0x008E
Priority select register 79	INTC_PSR79	8-bit	Base + 0x008F
Priority select register 80	INTC_PSR80	8-bit	Base + 0x0090
Priority select register 81	INTC_PSR81	8-bit	Base + 0x0091
Priority select register 82	INTC_PSR82	8-bit	Base + 0x0092
Priority select register 83	INTC_PSR83	8-bit	Base + 0x0093
Priority select register 84	INTC_PSR84	8-bit	Base + 0x0094
Priority select register 85	INTC_PSR85	8-bit	Base + 0x0095
Priority select register 86	INTC_PSR86	8-bit	Base + 0x0096
Priority select register 87	INTC_PSR87	8-bit	Base + 0x0097
Priority select register 88	INTC_PSR88	8-bit	Base + 0x0098
Priority select register 89	INTC_PSR89	8-bit	Base + 0x0099
Priority select register 90	INTC_PSR90	8-bit	Base + 0x009A
Priority select register 91	INTC_PSR91	8-bit	Base + 0x009B
Priority select register 92	INTC_PSR92	8-bit	Base + 0x009C
Priority select register 93	INTC_PSR93	8-bit	Base + 0x009D

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Priority select register 94	INTC_PSR94	8-bit	Base + 0x009E
Priority select register 95	INTC_PSR95	8-bit	Base + 0x009F
Priority select register 96	INTC_PSR96	8-bit	Base + 0x00A0
Priority select register 97	INTC_PSR97	8-bit	Base + 0x00A1
Priority select register 98	INTC_PSR98	8-bit	Base + 0x00A2
Priority select register 99	INTC_PSR99	8-bit	Base + 0x00A3
Priority select register 100	INTC_PSR100	8-bit	Base + 0x00A4
Priority select register 101	INTC_PSR101	8-bit	Base + 0x00A5
Priority select register 102	INTC_PSR102	8-bit	Base + 0x00A6
Priority select register 103	INTC_PSR103	8-bit	Base + 0x00A7
Priority select register 104	INTC_PSR104	8-bit	Base + 0x00A8
Priority select register 105	INTC_PSR105	8-bit	Base + 0x00A9
Priority select register 106	INTC_PSR106	8-bit	Base + 0x00AA
Priority select register 107	INTC_PSR107	8-bit	Base + 0x00AB
Priority select register 108	INTC_PSR108	8-bit	Base + 0x00AC
Priority select register 109	INTC_PSR109	8-bit	Base + 0x00AD
Priority select register 110	INTC_PSR110	8-bit	Base + 0x00AE
Priority select register 111	INTC_PSR111	8-bit	Base + 0x00AF
Priority select register 112	INTC_PSR112	8-bit	Base + 0x00B0
Priority select register 113	INTC_PSR113	8-bit	Base + 0x00B1
Priority select register 114	INTC_PSR114	8-bit	Base + 0x00B2
Priority select register 115	INTC_PSR115	8-bit	Base + 0x00B3
Priority select register 116	INTC_PSR116	8-bit	Base + 0x00B4
Priority select register 117	INTC_PSR117	8-bit	Base + 0x00B5
Priority select register 118	INTC_PSR118	8-bit	Base + 0x00B6
Priority select register 119	INTC_PSR119	8-bit	Base + 0x00B7
Priority select register 120	INTC_PSR120	8-bit	Base + 0x00B8
Priority select register 121	INTC_PSR121	8-bit	Base + 0x00B9
Priority select register 122	INTC_PSR122	8-bit	Base + 0x00BA
Priority select register 123	INTC_PSR123	8-bit	Base + 0x00BB
Priority select register 124	INTC_PSR124	8-bit	Base + 0x00BC
Priority select register 125	INTC_PSR125	8-bit	Base + 0x00BD

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Priority select register 126	INTC_PSR126	8-bit	Base + 0x00BE
Priority select register 127	INTC_PSR127	8-bit	Base + 0x00BF
Priority select register 128	INTC_PSR128	8-bit	Base + 0x00C0
Priority select register 129	INTC_PSR129	8-bit	Base + 0x00C1
Priority select register 130	INTC_PSR130	8-bit	Base + 0x00C2
Priority select register 131	INTC_PSR131	8-bit	Base + 0x00C3
Priority select register 132	INTC_PSR132	8-bit	Base + 0x00C4
Priority select register 133	INTC_PSR133	8-bit	Base + 0x00C5
Priority select register 134	INTC_PSR134	8-bit	Base + 0x00C6
Priority select register 135	INTC_PSR135	8-bit	Base + 0x00C7
Priority select register 136	INTC_PSR136	8-bit	Base + 0x00C8
Priority select register 137	INTC_PSR137	8-bit	Base + 0x00C9
Priority select register 138	INTC_PSR138	8-bit	Base + 0x00CA
Priority select register 139	INTC_PSR139	8-bit	Base + 0x00CB
Priority select register 140	INTC_PSR140	8-bit	Base + 0x00CC
Priority select register 141	INTC_PSR141	8-bit	Base + 0x00CD
Priority select register 142	INTC_PSR142	8-bit	Base + 0x00CE
Priority select register 143	INTC_PSR143	8-bit	Base + 0x00CF
Priority select register 144	INTC_PSR144	8-bit	Base + 0x00D0
Priority select register 145	INTC_PSR145	8-bit	Base + 0x00D1
Priority select register 146	INTC_PSR146	8-bit	Base + 0x00D2
Priority select register 147	INTC_PSR147	8-bit	Base + 0x00D3
Priority select register 148	INTC_PSR148	8-bit	Base + 0x00D4
Priority select register 149	INTC_PSR149	8-bit	Base + 0x00D5
Priority select register 150	INTC_PSR150	8-bit	Base + 0x00D6
Priority select register 151	INTC_PSR151	8-bit	Base + 0x00D7
Priority select register 152	INTC_PSR152	8-bit	Base + 0x00D8
Priority select register 153	INTC_PSR153	8-bit	Base + 0x00D9
Priority select register 154	INTC_PSR154	8-bit	Base + 0x00DA
Priority select register 155	INTC_PSR155	8-bit	Base + 0x00DB
Priority select register 156	INTC_PSR156	8-bit	Base + 0x00DC
Priority select register 157	INTC_PSR157	8-bit	Base + 0x00DD

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Priority select register 158	INTC_PSR158	8-bit	Base + 0x00DE
Priority select register 159	INTC_PSR159	8-bit	Base + 0x00DF
Priority select register 160	INTC_PSR160	8-bit	Base + 0x00E0
Priority select register 161	INTC_PSR161	8-bit	Base + 0x00E1
Priority select register 162	INTC_PSR162	8-bit	Base + 0x00E2
Priority select register 163	INTC_PSR163	8-bit	Base + 0x00E3
Priority select register 164	INTC_PSR164	8-bit	Base + 0x00E4
Priority select register 165	INTC_PSR165	8-bit	Base + 0x00E5
Priority select register 166	INTC_PSR166	8-bit	Base + 0x00E6
Priority select register 167	INTC_PSR167	8-bit	Base + 0x00E7
Priority select register 168	INTC_PSR168	8-bit	Base + 0x00E8
Priority select register 169	INTC_PSR169	8-bit	Base + 0x00E9
Priority select register 170	INTC_PSR170	8-bit	Base + 0x00EA
Priority select register 171	INTC_PSR171	8-bit	Base + 0x00EB
Priority select register 172	INTC_PSR172	8-bit	Base + 0x00EC
Priority select register 173	INTC_PSR173	8-bit	Base + 0x00ED
Priority select register 174	INTC_PSR174	8-bit	Base + 0x00EE
Priority select register 175	INTC_PSR175	8-bit	Base + 0x00EF
Priority select register 176	INTC_PSR176	8-bit	Base + 0x00F0
Priority select register 177	INTC_PSR177	8-bit	Base + 0x00F1
Priority select register 178	INTC_PSR178	8-bit	Base + 0x00F2
Priority select register 179	INTC_PSR179	8-bit	Base + 0x00F3
Priority select register 180	INTC_PSR180	8-bit	Base + 0x00F4
Priority select register 181	INTC_PSR181	8-bit	Base + 0x00F5
Priority select register 182	INTC_PSR182	8-bit	Base + 0x00F6
Priority select register 183	INTC_PSR183	8-bit	Base + 0x00F7
Priority select register 184	INTC_PSR184	8-bit	Base + 0x00F8
Priority select register 185	INTC_PSR185	8-bit	Base + 0x00F9
Priority select register 186	INTC_PSR186	8-bit	Base + 0x00FA
Priority select register 187	INTC_PSR187	8-bit	Base + 0x00FB
Priority select register 188	INTC_PSR188	8-bit	Base + 0x00FC
Priority select register 189	INTC_PSR189	8-bit	Base + 0x00FD

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Priority select register 190	INTC_PSR190	8-bit	Base + 0x00FE
Priority select register 191	INTC_PSR191	8-bit	Base + 0x00FF
Priority select register 192	INTC_PSR192	8-bit	Base + 0x0100
Priority select register 193	INTC_PSR193	8-bit	Base + 0x0101
Priority select register 194	INTC_PSR194	8-bit	Base + 0x0102
Priority select register 195	INTC_PSR195	8-bit	Base + 0x0103
Priority select register 196	INTC_PSR196	8-bit	Base + 0x0104
Priority select register 197	INTC_PSR197	8-bit	Base + 0x0105
Priority select register 198	INTC_PSR198	8-bit	Base + 0x0106
Priority select register 199	INTC_PSR199	8-bit	Base + 0x0107
Priority select register 200	INTC_PSR200	8-bit	Base + 0x0108
Priority select register 201	INTC_PSR201	8-bit	Base + 0x0109
Priority select register 202	INTC_PSR202	8-bit	Base + 0x010A
Priority select register 203	INTC_PSR203	8-bit	Base + 0x010B
Priority select register 204	INTC_PSR204	8-bit	Base + 0x010C
Priority select register 205	INTC_PSR205	8-bit	Base + 0x010D
Priority select register 206	INTC_PSR206	8-bit	Base + 0x010E
Priority select register 207	INTC_PSR207	8-bit	Base + 0x010F
Priority select register 208	INTC_PSR208	8-bit	Base + 0x0110
Priority select register 209	INTC_PSR209	8-bit	Base + 0x0111
Priority select register 210	INTC_PSR210	8-bit	Base + 0x0112
Priority select register 211	INTC_PSR211	8-bit	Base + 0x0113
Priority select register 212	INTC_PSR212	8-bit	Base + 0x0114
Priority select register 213	INTC_PSR213	8-bit	Base + 0x0115
Priority select register 214	INTC_PSR214	8-bit	Base + 0x0116
Priority select register 215	INTC_PSR215	8-bit	Base + 0x0117
Priority select register 216	INTC_PSR216	8-bit	Base + 0x0118
Priority select register 217	INTC_PSR217	8-bit	Base + 0x0119
Priority select register 218	INTC_PSR218	8-bit	Base + 0x011A
Priority select register 219	INTC_PSR219	8-bit	Base + 0x011B
Priority select register 220	INTC_PSR220	8-bit	Base + 0x011C
Priority select register 221	INTC_PSR221	8-bit	Base + 0x011D

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Priority select register 222	INTC_PSR222	8-bit	Base + 0x011E
Priority select register 223	INTC_PSR223	8-bit	Base + 0x011F
Priority select register 224	INTC_PSR224	8-bit	Base + 0x0120
Priority select register 225	INTC_PSR225	8-bit	Base + 0x0121
Priority select register 226	INTC_PSR226	8-bit	Base + 0x0122
Priority select register 227	INTC_PSR227	8-bit	Base + 0x0123
Priority select register 228	INTC_PSR228	8-bit	Base + 0x0124
Priority select register 229	INTC_PSR229	8-bit	Base + 0x0125
Priority select register 230	INTC_PSR230	8-bit	Base + 0x0126
Priority select register 231	INTC_PSR231	8-bit	Base + 0x0127
Priority select register 232	INTC_PSR232	8-bit	Base + 0x0128
Priority select register 233	INTC_PSR233	8-bit	Base + 0x0129
Priority select register 234	INTC_PSR234	8-bit	Base + 0x012A
Priority select register 235	INTC_PSR234	8-bit	Base + 0x012B
Priority select register 236	INTC_PSR236	8-bit	Base + 0x012C
Priority select register 237	INTC_PSR237	8-bit	Base + 0x012D
Priority select register 238	INTC_PSR238	8-bit	Base + 0x012E
Priority select register 239	INTC_PSR239	8-bit	Base + 0x012F
Priority select register 240	INTC_PSR240	8-bit	Base + 0x0130
Priority select register 241	INTC_PSR241	8-bit	Base + 0x0131
Priority select register 242	INTC_PSR242	8-bit	Base + 0x0132
Priority select register 243	INTC_PSR243	8-bit	Base + 0x0133
Priority select register 244	INTC_PSR244	8-bit	Base + 0x0134
Priority select register 245	INTC_PSR245	8-bit	Base + 0x0135
Priority select register 246	INTC_PSR246	8-bit	Base + 0x0136
Priority select register 247	INTC_PSR247	8-bit	Base + 0x0137
Priority select register 248	INTC_PSR248	8-bit	Base + 0x0138
Priority select register 249	INTC_PSR249	8-bit	Base + 0x0139
Priority select register 250	INTC_PSR250	8-bit	Base + 0x013A
Priority select register 251	INTC_PSR251	8-bit	Base + 0x013B
Priority select register 252	INTC_PSR252	8-bit	Base + 0x013C
Priority select register 253	INTC_PSR253	8-bit	Base + 0x013D

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Priority select register 254	INTC_PSR254	8-bit	Base + 0x013E
Priority select register 255	INTC_PSR255	8-bit	Base + 0x013F
Priority select register 256	INTC_PSR256	8-bit	Base + 0x0140
Priority select register 257	INTC_PSR257	8-bit	Base + 0x0141
Priority select register 258	INTC_PSR258	8-bit	Base + 0x0142
Priority select register 259	INTC_PSR259	8-bit	Base + 0x0143
Priority select register 260	INTC_PSR260	8-bit	Base + 0x0144
Priority select register 261	INTC_PSR261	8-bit	Base + 0x0145
Priority select register 262	INTC_PSR262	8-bit	Base + 0x0146
Priority select register 263	INTC_PSR263	8-bit	Base + 0x0147
Priority select register 264	INTC_PSR264	8-bit	Base + 0x0148
Priority select register 265	INTC_PSR265	8-bit	Base + 0x0149
Priority select register 266	INTC_PSR266	8-bit	Base + 0x014A
Priority select register 267	INTC_PSR267	8-bit	Base + 0x014B
Priority select register 268	INTC_PSR268	8-bit	Base + 0x014C
Priority select register 269	INTC_PSR269	8-bit	Base + 0x014D
Priority select register 270	INTC_PSR270	8-bit	Base + 0x014E
Priority select register 271	INTC_PSR271	8-bit	Base + 0x014F
Priority select register 272	INTC_PSR272	8-bit	Base + 0x0150
Priority select register 273	INTC_PSR273	8-bit	Base + 0x0151
Priority select register 274	INTC_PSR274	8-bit	Base + 0x0152
Priority select register 275	INTC_PSR275	8-bit	Base + 0x0153
Priority select register 276	INTC_PSR276	8-bit	Base + 0x0154
Priority select register 277	INTC_PSR277	8-bit	Base + 0x0155
Priority select register 278	INTC_PSR278	8-bit	Base + 0x0156
Priority select register 279	INTC_PSR279	8-bit	Base + 0x0157
Priority select register 280	INTC_PSR280	8-bit	Base + 0x0158
Priority select register 281	INTC_PSR281	8-bit	Base + 0x0159
Priority select register 282	INTC_PSR282	8-bit	Base + 0x015A
Priority select register 283	INTC_PSR283	8-bit	Base + 0x015B
Priority select register 284	INTC_PSR284	8-bit	Base + 0x015C
Priority select register 285	INTC_PSR285	8-bit	Base + 0x015D

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Priority select register 286	INTC_PSR286	8-bit	Base + 0x015E
Priority select register 287	INTC_PSR287	8-bit	Base + 0x015F
Priority select register 288	INTC_PSR288	8-bit	Base + 0x0160
Priority select register 289	INTC_PSR289	8-bit	Base + 0x0161
Priority select register 290	INTC_PSR290	8-bit	Base + 0x0162
Priority select register 291	INTC_PSR291	8-bit	Base + 0x0163
Priority select register 292	INTC_PSR292	8-bit	Base + 0x0164
Priority select register 293	INTC_PSR293	8-bit	Base + 0x0165
Priority select register 294	INTC_PSR294	8-bit	Base + 0x0166
Priority select register 295	INTC_PSR295	8-bit	Base + 0x0167
Priority select register 296	INTC_PSR296	8-bit	Base + 0x0168
Priority select register 297	INTC_PSR297	8-bit	Base + 0x0169
Priority select register 298	INTC_PSR298	8-bit	Base + 0x016A
Priority select register 299	INTC_PSR299	8-bit	Base + 0x016B
Priority select register 300	INTC_PSR300	8-bit	Base + 0x016C
Fast Ethernet Controller (FEC) Chapter 15, “Fast Ethernet Controller (FEC)”			0xFFF4_C000
Interrupt event register	EIR	32-bit	Base + 0x0004
Interrupt mask register	EIMR	32-bit	Base + 0x0008
Receive descriptor active register	RDAR	32-bit	Base + 0x0010
Transmit descriptor active register	TDAR	32-bit	Base + 0x0014
Ethernet control register	ECR	32-bit	Base + 0x0024
MII management frame register	MMFR	32-bit	Base + 0x0040
MII speed control register	MSCR	32-bit	Base + 0x0044
MIB control/status register	MIBC	32-bit	Base + 0x0064
Receive control register	RCR	32-bit	Base + 0x0084
Transmit control register	TCR	32-bit	Base + 0x00C4
MAC address low register	PALR	32-bit	Base + 0x00E4
MAC address upper register and type field	PAUR	32-bit	Base + 0x00E8
Opcode and pause duration	OPD	32-bit	Base + 0x00EC
Upper 32 bits of individual hash table	IAUR	32-bit	Base + 0x0118
Lower 32 Bits of individual hash table	IALR	32-bit	Base + 0x011C

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Upper 32 bits of group hash table	GAUR	32-bit	Base + 0x0120
Lower 32 bits of group hash table	GALR	32-bit	Base + 0x0124
Transmit FIFO watermark	TFWR	32-bit	Base + 0x0144
FIFO receive bound register	FRBR	32-bit	Base + 0x014C
FIFO receive FIFO start registers	FRSR	32-bit	Base + 0x0150
Pointer to receive descriptor ring	ERDSR	32-bit	Base + 0x0180
Pointer to transmit descriptor ring	ETDSR	32-bit	Base + 0x0184
Maximum receive buffer size	EMRBR	32-bit	Base + 0x0188
MIB block counters	MIB		FFF4_C200
Reserved	—	—	Base + 0xFFF0_8000
Reserved	—	—	Base + 0xFFF1_0000
Enhanced Queued Analog-to-Digital Converter (eQADC) Chapter 18, “Enhanced Queued Analog-to-Digital Converter (eQADC)”			0xFFF8_0000
Module configuration register	EQADC_MCR	32-bit	Base + 0x0000
Reserved	—	—	Base + (0x0004–0x0007)
Null message send format register	EQADC_NMSFR	32-bit	Base + 0x0008
External trigger digital filter register	EQADC_ETDFR	32-bit	Base + 0x000C
CFIFO push register 0	EQADC_CFPR0	32-bit	Base + 0x0010
CFIFO push register 1	EQADC_CFPR1	32-bit	Base + 0x0014
CFIFO push register 2	EQADC_CFPR2	32-bit	Base + 0x0018
CFIFO push register 3	EQADC_CFPR3	32-bit	Base + 0x001C
CFIFO push register 4	EQADC_CFPR4	32-bit	Base + 0x0020
CFIFO push register 5	EQADC_CFPR5	32-bit	Base + 0x0024
Reserved	—	—	Base + (0x0028–0x002F)
Result FIFO pop register 0	EQADC_RFPR0	32-bit	Base + 0x0030
Result FIFO pop register 1	EQADC_RFPR1	32-bit	Base + 0x0034
Result FIFO pop register 2	EQADC_RFPR2	32-bit	Base + 0x0038
Result FIFO pop register 3	EQADC_RFPR3	32-bit	Base + 0x003C
Result FIFO pop register 4	EQADC_RFPR4	32-bit	Base + 0x0040
Result FIFO pop register 5	EQADC_RFPR5	32-bit	Base + 0x0044
Reserved	—	—	Base + (0x0048–0x004F)

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
CFIFO control register 0	EQADC_CFCR0	16-bit	Base + 0x0050
CFIFO control register 1	EQADC_CFCR1	16-bit	Base + 0x0052
CFIFO control register 2	EQADC_CFCR2	16-bit	Base + 0x0054
CFIFO control register 3	EQADC_CFCR3	16-bit	Base + 0x0056
CFIFO control register 4	EQADC_CFCR4	16-bit	Base + 0x0058
CFIFO control register 5	EQADC_CFCR5	16-bit	Base + 0x005A
Reserved	—	—	Base + (0x005C–0x005F)
Interrupt and DMA control register 0	EQADC_IDCR0	16-bit	Base + 0x0060
Interrupt and DMA control register 1	EQADC_IDCR1	16-bit	Base + 0x0062
Interrupt and DMA control register 2	EQADC_IDCR2	16-bit	Base + 0x0064
Interrupt and DMA control register 3	EQADC_IDCR3	16-bit	Base + 0x0066
Interrupt and DMA control register 4	EQADC_IDCR4	16-bit	Base + 0x0068
Interrupt and DMA control register 5	EQADC_IDCR5	16-bit	Base + 0x006A
Reserved	—	—	Base + (0x006C–0x006F)
FIFO and interrupt status register 0	EQADC_FISR0	32-bit	Base + 0x0070
FIFO and interrupt status register 1	EQADC_FISR1	32-bit	Base + 0x0074
FIFO and interrupt status register 2	EQADC_FISR2	32-bit	Base + 0x0078
FIFO and interrupt status register 3	EQADC_FISR3	32-bit	Base + 0x007C
FIFO and interrupt status register 4	EQADC_FISR4	32-bit	Base + 0x0080
FIFO and interrupt status register 5	EQADC_FISR5	32-bit	Base + 0x0084
Reserved	—	—	Base + (0x0088–0x008F)
CFIFO transfer counter register 0	EQADC_CFTCR0	16-bit	Base + 0x0090
CFIFO transfer counter register 1	EQADC_CFTCR1	16-bit	Base + 0x0092
CFIFO transfer counter register 2	EQADC_CFTCR2	16-bit	Base + 0x0094
CFIFO transfer counter register 3	EQADC_CFTCR3	16-bit	Base + 0x0096
CFIFO transfer counter register 4	EQADC_CFTCR4	16-bit	Base + 0x0098
CFIFO transfer counter register 5	EQADC_CFTCR5	16-bit	Base + 0x009A
Reserved	—	—	Base + (0x009C–0x009F)
CFIFO status snapshot register 0	EQADC_CFSSR0	32-bit	Base + 0x00A0
CFIFO status snapshot register 1	EQADC_CFSSR1	32-bit	Base + 0x00A4
CFIFO status snapshot register 2	EQADC_CFSSR2	32-bit	Base + 0x00A8
CFIFO status register	EQADC_CFSR	32-bit	Base + 0x00AC

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Reserved	—	—	Base + (0x00B0–0x00B3)
SSI control register	EQADC_SSICR	32-bit	Base + 0x00B4
SSI receive data register	EQADC_SSIRDR	32-bit	Base + 0x00B8
Reserved	—	—	Base + (0x00BC–0x00FF)
CFIFO 0 register 0	EQADC_CF0R0	32-bit	Base + 0x0100
CFIFO 0 register 1	EQADC_CF0R1	32-bit	Base + 0x0104
CFIFO 0 register 2	EQADC_CF0R2	32-bit	Base + 0x0108
CFIFO 0 register 3	EQADC_CF0R3	32-bit	Base + 0x010C
Reserved	—	—	Base + (0x0110–0x013F)
CFIFO 1 register 0	EQADC_CF1R0	32-bit	Base + 0x0140
CFIFO 1 register 1	EQADC_CF1R1	32-bit	Base + 0x0144
CFIFO 1 register 2	EQADC_CF1R2	32-bit	Base + 0x0148
CFIFO 1 register 3	EQADC_CF1R3	32-bit	Base + 0x014C
Reserved	—	—	Base + (0x0150–0x017F)
CFIFO 2 register 0	EQADC_CF2R0	32-bit	Base + 0x0180
CFIFO 2 register 1	EQADC_CF2R1	32-bit	Base + 0x0184
CFIFO 2 register 2	EQADC_CF2R2	32-bit	Base + 0x0188
CFIFO 2 register 3	EQADC_CF2R3	32-bit	Base + 0x018C
Reserved	—	—	Base + (0x0190–0x01BF)
CFIFO 3 register 0	EQADC_CF3R0	32-bit	Base + 0x01C0
CFIFO 3 register 1	EQADC_CF3R1	32-bit	Base + 0x01C4
CFIFO 3 register 2	EQADC_CF3R2	32-bit	Base + 0x01C8
CFIFO 3 register 3	EQADC_CF3R3	32-bit	Base + 0x01CC
Reserved	—	—	Base + (0x01D0–0x01FF)
CFIFO 4 register 0	EQADC_CF4R0	32-bit	Base + 0x0200
CFIFO 4 register 1	EQADC_CF4R1	32-bit	Base + 0x0204
CFIFO 4 register 2	EQADC_CF4R2	32-bit	Base + 0x0208
CFIFO 4 register 3	EQADC_CF4R3	32-bit	Base + 0x020C
Reserved	—	—	Base + (0x0210–0x023F)

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
CFIFO 5 register 0	EQADC_CF5R0	32-bit	Base + 0x0240
CFIFO 5 register 1	EQADC_CF5R1	32-bit	Base + 0x0244
CFIFO 5 register 2	EQADC_CF5R2	32-bit	Base + 0x0248
CFIFO 5 register 3	EQADC_CF5R3	32-bit	Base + 0x024C
Reserved	—	—	Base + (0x0250–0x02FF)
RFIFO 0 register 0	EQADC_RF0R0	32-bit	Base + 0x0300
RFIFO 0 register 1	EQADC_RF0R1	32-bit	Base + 0x0304
RFIFO 0 register 2	EQADC_RF0R2	32-bit	Base + 0x0308
RFIFO 0 register 3	EQADC_RF0R3	32-bit	Base + 0x030C
Reserved	—	—	Base + (0x0310–0x033F)
RFIFO 1 register 0	EQADC_RF1R0	32-bit	Base + 0x0340
RFIFO 1 register 1	EQADC_RF1R1	32-bit	Base + 0x0344
RFIFO 1 register 2	EQADC_RF1R2	32-bit	Base + 0x0348
RFIFO 1 register 3	EQADC_RF1R3	32-bit	Base + 0x034C
Reserved	—	—	Base + (0x0350–0x037F)
RFIFO 2 register 0	EQADC_RF2R0	32-bit	Base + 0x0380
RFIFO 2 register 1	EQADC_RF2R1	32-bit	Base + 0x0384
RFIFO 2 register 2	EQADC_RF2R2	32-bit	Base + 0x0388
RFIFO 2 register 3	EQADC_RF2R3	32-bit	Base + 0x038C
Reserved	—	—	Base + (0x0390–0x03BF)
RFIFO 3 register 0	EQADC_RF3R0	32-bit	Base + 0x03C0
RFIFO 3 register 1	EQADC_RF3R1	32-bit	Base + 0x03C4
RFIFO 3 register 2	EQADC_RF3R2	32-bit	Base + 0x03C8
RFIFO 3 register 3	EQADC_RF3R3	32-bit	Base + 0x03CC
Reserved	—	—	Base + (0x03D0–0x03FF)
RFIFO 4 register 0	EQADC_RF4R0	32-bit	Base + 0x0400
RFIFO 4 register 1	EQADC_RF4R1	32-bit	Base + 0x0404
RFIFO 4 register 2	EQADC_RF4R2	32-bit	Base + 0x0408
RFIFO 4 register 3	EQADC_RF4R3	32-bit	Base + 0x040C
Reserved	—	—	Base + (0x0410–0x043F)

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
RFIFO 5 register 0	EQADC_RF5R0	32-bit	Base + 0x0440
RFIFO 5 register 1	EQADC_RF5R1	32-bit	Base + 0x0444
RFIFO 5 register 2	EQADC_RF5R2	32-bit	Base + 0x0448
RFIFO 5 register 3	EQADC_RF5R3	32-bit	Base + 0x044C
Reserved	—	—	Base + (0x0450–0x07FF)
ADC0 control register	ADC0_CR		No memory mapped access
ADC1 control register	ADC1_CR		
ADC time stamp control register	ADC_TSCR		
ADC time base counter register	ADC_TBCR		
ADC0 gain calibration constant register	ADC0_GCCR		
ADC1 gain calibration constant register	ADC1_GCCR		
ADC0 offset calibration constant register	ADC0_OCCR		
ADC1 offset calibration constant register	ADC1_OCCR		
Reserved	—	—	(Base + 0x0800)–0xFFF8_FFFF
Deserial / Serial Peripheral Interface (DSPIx) Chapter 19, “Deserial Serial Peripheral Interface (DSPI)			0xFFF9_0000 (DSPI A) 0xFFF9_4000 (DSPI B) 0xFFF9_8000 (DSPI C) 0xFFF9_C000 (DSPI D)
Module configuration register	DSPIx_MCR	32-bit	Base + 0x0000
Reserved	—	—	Base + (0x0004–0x0007)
Transfer count register	DSPIx_TCR	32-bit	Base + 0x0008
Clock and transfer attribute register 0	DSPIx_CTAR0	32-bit	Base + 0x000C
Clock and transfer attribute register 1	DSPIx_CTAR1	32-bit	Base + 0x0010
Clock and transfer attribute register 2	DSPIx_CTAR2	32-bit	Base + 0x0014
Clock and transfer attribute register 3	DSPIx_CTAR3	32-bit	Base + 0x0018
Clock and transfer attribute register 4	DSPIx_CTAR4	32-bit	Base + 0x001C
Clock and transfer attribute register 5	DSPIx_CTAR5	32-bit	Base + 0x0020
Clock and transfer attribute register 6	DSPIx_CTAR6	32-bit	Base + 0x0024
Clock and transfer attribute register 7	DSPIx_CTAR7	32-bit	Base + 0x0028
DSPI Status register	DSPIx_SR	32-bit	Base + 0x002C
DMA/interrupt request select and enable register	DSPIx_RSER	32-bit	Base + 0x0030
Push TX FIFO register	DSPIx_PUSHR	32-bit	Base + 0x0034
Pop RX FIFO register	DSPIx_POPR	32-bit	Base + 0x0038

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Transmit FIFO registers 0	DSPIx_TXFR0	32-bit	Base + 0x003C
Transmit FIFO registers 1	DSPIx_TXFR1	32-bit	Base + 0x0040
Transmit FIFO registers 2	DSPIx_TXFR2	32-bit	Base + 0x0044
Transmit FIFO registers 3	DSPIx_TXFR3	32-bit	Base + 0x0048
Reserved	—	—	Base + (0x004C–0x007B)
Receive FIFO registers 0	DSPIx_RXFR0	32-bit	Base + 0x007C
Receive FIFO registers 1	DSPIx_RXFR1	32-bit	Base + 0x0080
Receive FIFO registers 2	DSPIx_RXFR2	32-bit	Base + 0x0084
Receive FIFO registers 3	DSPIx_RXFR3	32-bit	Base + 0x0088
Reserved	—	—	Base + (0x008C–0x00BB)
DSI configuration register	DSPIx_DSICR	32-bit	Base + 0x00BC
DSI serialization data register	DSPIx_SDR	32-bit	Base + 0x00C0
DSI alternate serialization data register	DSPIx_ASDR	32-bit	Base + 0x00C4
DSI transmit comparison register	DSPIx_COMPR	32-bit	Base + 0x00C8
DSI deserialization data register	DSPIx_DDR	32-bit	Base + 0x00CC
Reserved	—	—	(Base + 0x00D0) 0xFFF9_3FFF (DSPI A) 0xFFF9_7FFF (DSPI B) 0xFFF9_BFFF (DSPI C) 0xFFFA_FFFF (DSPI D)
Enhanced Serial Communication Interface (eSCIx) Chapter 20, “Enhanced Serial Communication Interface (eSCI)”			0xFFFB_0000 (A) 0xFFFB_4000 (B)
Control register 1	ESCIx_CR1	32-bit	Base + 0x0000
Control register 2	ESCIx_CR2	16-bit	Base + 0x0004
Data register	ESCIx_DR	16-bit	Base + 0x0006
Status register	ESCIx_SR	32-bit	Base + 0x0008
LIN control register	ESCIx_LCR	32-bit	Base + 0x000C
LIN transmit register	ESCIx_LTR	32-bit	Base + 0x0010
LIN receive register	ESCIx_LRR	32-bit	Base + 0x0014
LIN CRC polynomial register	ESCIx_LPR	32-bit	Base + 0x0018
Reserved	—	—	(Base + 0x001C)–0xFFFB_3FFF (A) (Base + 0x001C)–0xFFFB_7FFF (B)
FlexCAN2 Controller Area Network (CANx) Chapter 21, “FlexCAN2 Controller Area Network”			0xFFFC_0000 (FlexCAN A) 0xFFFC_4000 (FlexCAN B) 0xFFFC_8000 (FlexCAN C) 0xFFFF_C000 (FlexCAN D)

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Module configuration register	CANx_MCR	32-bit	Base + 0x0000
Control register	CANx_CR	32-bit	Base + 0x0004
Free running timer register	CANx_TIMER	32-bit	Base + 0x0008
Reserved	—	—	Base + (0x000C–0x000F)
Receive global mask register	CANx_RXGMASK	32-bit	Base + 0x0010
Receive buffer 14 mask register	CANx_RX14MASK	32-bit	Base + 0x0014
Receive buffer 15 mask register	CANx_RX15MASK	32-bit	Base + 0x0018
Error counter register	CANx_ECR	32-bit	Base + 0x001C
Error and status register	CANx_ESR	32-bit	Base + 0x0020
Interrupt mask register high	CANx_IMRH	32-bit	Base + 0x0024
Interrupt mask register low	CANx_IMRL	32-bit	Base + 0x0028
Interrupt flag register high	CANx_IFRH	32-bit	Base + 0x002C
Interrupt flag register low	CANx_IFRL	32-bit	Base + 0x0030
Reserved	—	—	Base + (0x0034–0x007F)
Boot Assist Module (BAM) Chapter 15, “Boot Assist Module (BAM)”			0xFFFF_C000
Reserved			
Message buffer 0	MB0	16-bit	Base + 0x0080
Message buffer 1	MB1	16-bit	Base + 0x0090
Message buffer 2	MB2	16-bit	Base + 0x00A0
Message buffer 3	MB3	16-bit	Base + 0x00B0
Message buffer 4	MB4	16-bit	Base + 0x00C0
Message buffer 5	MB5	16-bit	Base + 0x00D0
Message buffer 6	MB6	16-bit	Base + 0x00E0
Message buffer 7	MB7	16-bit	Base + 0x00F0
Message buffer 8	MB8	16-bit	Base + 0x0100
Message buffer 9	MB9	16-bit	Base + 0x0110
Message buffer 10	MB10	16-bit	Base + 0x0120
Message buffer 11	MB11	16-bit	Base + 0x0130
Message buffer 12	MB12	16-bit	Base + 0x0140
Message buffer 13	MB13	16-bit	Base + 0x0150
Message buffer 14	MB14	16-bit	Base + 0x0160

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Message buffer 15	MB15	16-bit	Base + 0x0170
Message buffer 16	MB16	16-bit	Base + 0x0180
Message buffer 17	MB17	16-bit	Base + 0x0190
Message buffer 18	MB18	16-bit	Base + 0x01A0
Message buffer 19	MB19	16-bit	Base + 0x01B0
Message buffer 20	MB20	16-bit	Base + 0x01C0
Message buffer 21	MB21	16-bit	Base + 0x01D0
Message buffer 22	MB22	16-bit	Base + 0x01E0
Message buffer 23	MB23	16-bit	Base + 0x01F0
Message buffer 24	MB24	16-bit	Base + 0x0200
Message buffer 25	MB25	16-bit	Base + 0x0210
Message buffer 26	MB26	16-bit	Base + 0x0220
Message buffer 27	MB27	16-bit	Base + 0x0230
Message buffer 28	MB28	16-bit	Base + 0x0240
Message buffer 29	MB29	16-bit	Base + 0x0250
Message buffer 30	MB30	16-bit	Base + 0x0260
Message buffer 31	MB31	16-bit	Base + 0x0270
Message buffer 32	MB32	16-bit	Base + 0x0280
Message buffer 33	MB33	16-bit	Base + 0x0290
Message buffer 34	MB34	16-bit	Base + 0x02A0
Message buffer 35	MB35	16-bit	Base + 0x02B0
Message buffer 36	MB36	16-bit	Base + 0x02C0
Message buffer 37	MB37	16-bit	Base + 0x02D0
Message buffer 38	MB38	16-bit	Base + 0x02E0
Message buffer 39	MB39	16-bit	Base + 0x02F0
Message buffer 40	MB40	16-bit	Base + 0x0300
Message buffer 41	MB41	16-bit	Base + 0x0310
Message buffer 42	MB42	16-bit	Base + 0x0320
Message buffer 43	MB43	16-bit	Base + 0x0330
Message buffer 44	MB44	16-bit	Base + 0x0340
Message buffer 45	MB45	16-bit	Base + 0x0350
Message buffer 46	MB46	16-bit	Base + 0x0360

Table A-2. MPC5566 Detailed Register Map (continued)

Register Description	Register Name	Used Size	Address
Message buffer 47	MB47	16-bit	Base + 0x0370
Message buffer 48	MB48	16-bit	Base + 0x0380
Message buffer 49	MB49	16-bit	Base + 0x0390
Message buffer 50	MB50	16-bit	Base + 0x03A0
Message buffer 51	MB51	16-bit	Base + 0x03B0
Message buffer 52	MB52	16-bit	Base + 0x03C0
Message buffer 53	MB53	16-bit	Base + 0x03D0
Message buffer 54	MB54	16-bit	Base + 0x03E0
Message buffer 55	MB55	16-bit	Base + 0x03F0
Message buffer 56	MB56	16-bit	Base + 0x0400
Message buffer 57	MB57	16-bit	Base + 0x0410
Message buffer 58	MB58	16-bit	Base + 0x0420
Message buffer 59	MB59	16-bit	Base + 0x0430
Message buffer 60	MB60	16-bit	Base + 0x0440
Message buffer 61	MB61	16-bit	Base + 0x0450
Message buffer 62	MB62	16-bit	Base + 0x0460
Message buffer 63	MB63	16-bit	Base + 0x0470
Reserved	—	—	Base + (0x0500–end)

[1] The registers mapped in the ECSM module (0xFFF4_0014–0xFFF4_001F) can control and configure the software watchdog timer in the standard Freescale ECSM block incorporated in the device. The e200z6 core also provides this functionality and is the preferred method for watchdog implementation. To optimize code portability to other members of the MPC55XX family, use of the watchdog registers in the ECSM is not recommended.

Table A-3. e200z6 Core SPR Numbers (Supervisor Mode)

Register	Description	SPR (decimal)
General Registers		
XER	Integer Exception Register	1
LR	Link Register	8
CTR	Count Register	9
GPR0–GPR31	General Purpose Registers	N/A
Special Purpose Registers		
SPRG0	Special Purpose Register 0	272
SPRG1	Special Purpose Register 1	273

Table A-3. e200z6 Core SPR Numbers (Supervisor Mode) (continued)

Register	Description	SPR (decimal)
SPRG2	Special Purpose Register 2	274
SPRG3	Special Purpose Register 3	275
SPRG4	Special Purpose Register 4	276
SPRG5	Special Purpose Register 5	277
SPRG6	Special Purpose Register 6	278
SPRG7	Special Purpose Register 7	279
USPRG0	User Special Purpose Register	256
BUCSR	Branch Unit Control and Status Register	1013
Exception Handling / Control Registers		
SRR0	Save and Restore Register 0	26
SRR1	Save and Restore Register 1	27
CSRR0	Critical Save and Restore Register 0	58
CSRR1	Critical Save and Restore Register 1	59
DSRR0	Debug Save and Restore Register 0	574
DSRR1	Debug Save and Restore Register 1	575
ESR	Exception Syndrome Register	62
MCSR	Machine Check Syndrome Register	572
DEAR	Data Exception Address Register	61
IVPR	Interrupt Vector Prefix Register	63
IVOR1	Interrupt Vector Offset Register 1	401
IVOR2	Interrupt Vector Offset Register 2	402
IVOR3	Interrupt Vector Offset Register 3	403
IVOR4	Interrupt Vector Offset Register 4	404
IVOR5	Interrupt Vector Offset Register 5	405
IVOR6	Interrupt Vector Offset Register 6	406
IVOR7	Interrupt Vector Offset Register 7	407
IVOR8	Interrupt Vector Offset Register 8	408
IVOR9	Not Supported	—
IVOR10	Interrupt Vector Offset Register 10	410
IVOR11	Interrupt Vector Offset Register 11	411
IVOR12	Interrupt Vector Offset Register 12	412
IVOR13	Interrupt Vector Offset Register 13	413
IVOR14	Interrupt Vector Offset Register 14	414

Table A-3. e200z6 Core SPR Numbers (Supervisor Mode) (continued)

Register	Description	SPR (decimal)
IVOR15	Interrupt Vector Offset Register 15	415
IVOR32	Interrupt Vector Offset Register 32	528
IVOR33	Interrupt Vector Offset Register 33	529
IVOR34	Interrupt Vector Offset Register 34	530
Processor Control Registers		
MSR	Machine State Register	N/A
PVR	Processor Version Register	287
PIR	Processor ID Register	286
SVR	System Version Register	1023
HID0	Hardware Implementation Dependent Register 0	1008
HID1	Hardware Implementation Dependent Register 1	1009
Timer Registers		
TBL	Time Base Lower Register	284
TBU	Time Base Upper Register	285
TCR	Timer Control Register	340
TSR	Timer Status Register	336
DEC	Decrementer Register	22
DECAR	Decrementer Auto-reload Register	54
Debug Registers		
DBCR0	Debug Control Register 0	308
DBCR1	Debug Control Register 1	309
DBCR2	Debug Control Register 2	310
DBCR3	Debug Control Register 3	561
DBSR	Debug Status Register	304
DBCNT	Debug Counter Register	562
IAC1	Instruction Address Compare Register 1	312
IAC2	Instruction Address Compare Register 2	313
IAC3	Instruction Address Compare Register 3	314
IAC4	Instruction Address Compare Register 4	315
DAC1	Data Address Compare Register 1	316
DAC2	Data Address Compare Register 2	317
Memory Management Registers		
MAS0	MMU Assist Register 0	624

Table A-3. e200z6 Core SPR Numbers (Supervisor Mode) (continued)

Register	Description	SPR (decimal)
MAS1	MMU Assist Register 1	625
MAS2	MMU Assist Register 2r	626
MAS3	MMU Assist Register 3	627
MAS4	MMU Assist Register 4	628
MAS6	MMU Assist Register 6	630
PID0	Process ID Register	48
MMUCSR0	MMU Control and Status Register 0	1012
MMUCFG	MMU Configuration Register	1015
TLB0CFG	TLB 0 Configuration Register	688
TLB1CFG	TLB 1 Configuration Register	689
Cache Registers		
L1CFG0	L1 Cache Configuration Register	515
L1CSR0	L1 Cache Control and Status Register 0	1010
L1FINV0	L1 Cache Flush and Invalidate Control Register 0	1016
APU Registers		
SPEFSCR	SPE APU Status and Control Register	512

Table A-4. e200z6 Core SPR Numbers (User Mode)

Register	Description	SPR (decimal)
General Registers		
CTR	Count Register	9
LR	Link Register	8
XER	Integer Exception Register	1
GPR0–GPR31	General Purpose Registers	N/A
Special Purpose Registers		
SPRG4	Special Purpose Register 4	260
SPRG5	Special Purpose Register 5	261
SPRG6	Special Purpose Register 6	262
SPRG7	Special Purpose Register 7	263
USPRG0	User Special Purpose Register	256
Timer Registers		
TBL	Time Base Lower Register	268

Table A-4. e200z6 Core SPR Numbers (User Mode) (continued)

Register	Description	SPR (decimal)
TBU	Time Base Upper Register	269
Cache Registers		
L1CFG0	L1 Cache Configuration Register	515
APU Registers		
SPEFSCR	SPE APU Status and Control Register	512

Appendix B
Calibration

B.1 Overview

The MPC5500 family of microcontrollers includes various specialized features to support automotive calibration. Many of these calibration features are not available to the final application software, and some MPC5500 devices support calibration signals that are not available in the standard 208, 324, and 416 BGA packages. Special calibration assembled devices with increased signal bond-out provide full access to all calibration resources for all MPC5500 variants.

Calibration hardware that uses the calibration assembled devices is detailed in Figure B-1. Freescale-produced VertiCal bases use the calibration-assembled MPC5500 device mounted on a small circuit board with a footprint which is compatible with that of the production BGA packaged MPC5500 device. A 156-way VertiCal connector on the top-side of the VertiCal base allows you to attach VertiCal compliant top-board hardware. Various types of top-board hardware to support calibration and debug are available from Freescale and commercial companies.

The VertiCal connector standard defines the set of signals used to communicate between the microcontroller on the VertiCal base board and the attached calibration development tools, called top-boards. Signal availability or sourcing for the VertiCal connector differs depending on the MPC5500 device used.

The calibration system is illustrated in Figure B-1 and the VertiCal Base is illustrated in Figure B-2.

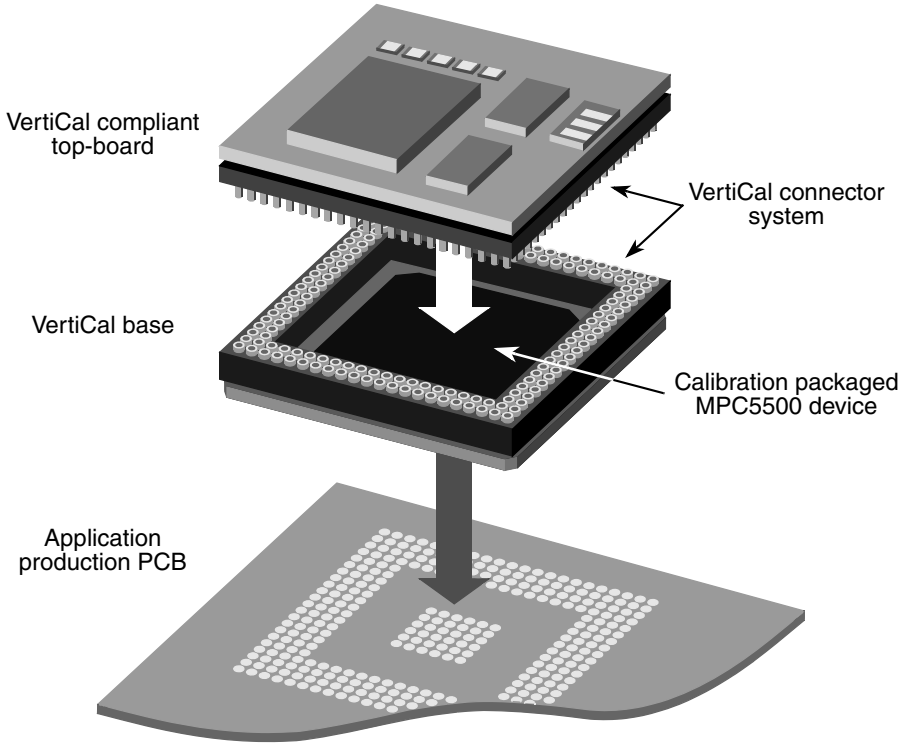


Figure B-1. Calibration Assembly

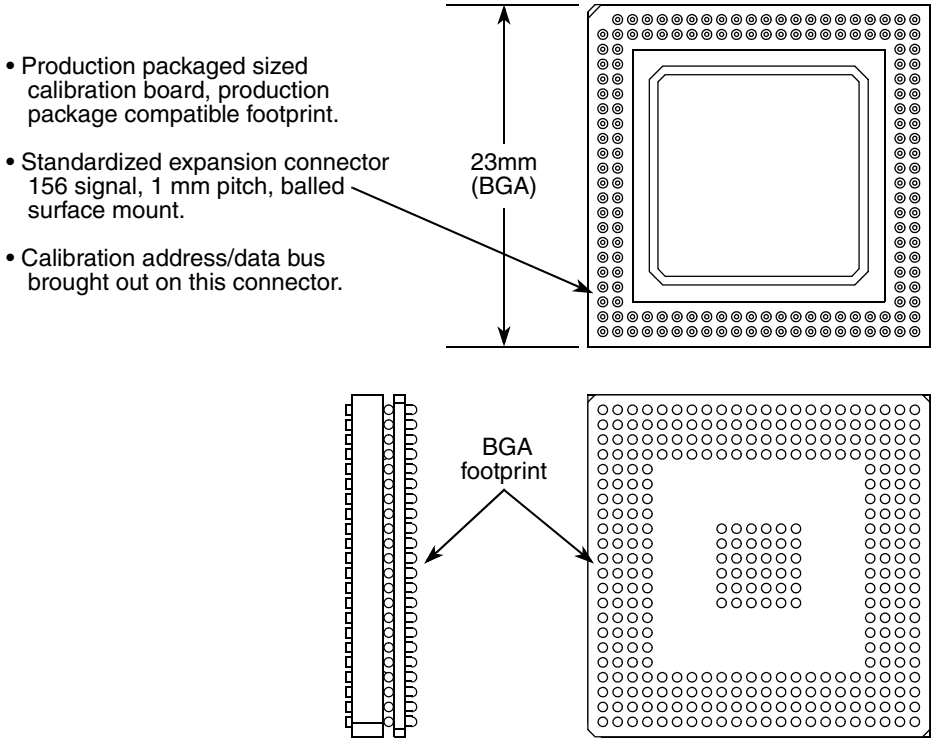


Figure B-2. VertiCal Base

B.2 Calibration Bus

The calibration bus is made up of address bus, data bus, bus control and clock signals. The calibration bus is used by tools that include memory for calibration data or other code in development. Refer to Table B-1 for calibration bus signals. A 16-bit data bus and 19-bit address bus gives a basic addressing range of 1 MB. Alternatively, the maximum memory addressable using just one chip select is four MB. Refer to Table B-2.

The VertiCal connector supports up to 4 chip select signals, although the actual number of chip selects available depends on the device and package. Use the CAL_$\overline{CS}$[0] chip select as the default calibration chip select to ensure maximum portability of calibration tools across devices. The four calibration chip select signals CAL_$\overline{CS}$[0:3] are configured and function like the external chip select signals $\overline{CS}$[0:3], except the calibration chip selects have a higher priority in address decoding than the external chip selects, $\overline{CS}$[0:3]. Refer to Section B.8, "Application Information," for application information on the number of calibration chip selects.

The CAL_$\overline{CS}$[0:3] chip selects have multiplexed signal functions to provide additional addressing bits that allows the flexibility of increasing the addressing range or the number of chip selects. The calibration functionality provides a calibration bus with pads that are in addition to the pads for the 416 pin package part. Therefore, the calibration functionality does not use any I/O available in the 416 pin production package for a calibration bus interface.

The P/A/G column in the following table differentiates each signal function that is multiplexed to the same pin assignment. The P/A/G value is set in the PA field of the SIU_PCR registers and determines which multiplexed signal function controls the pin. For more information on how to set the PA field, read the Signals Chapter.

Table B-1. MPC5566 Calibration Bus Signals

496 VertiCal Signal Name	Signal Function	Signal Name	P/A/G
Calibration Bus			
CAL_$\overline{CS}$[0]	Calibration chip select 0	CAL_$\overline{CS}$[0]	P
CAL_$\overline{CS}$[1:3]	Calibration chip select 1–3 Calibration address	CAL_$\overline{CS}$[1:3]_ CAL_ADDR[9:11]	P A
CAL_ADDR[12:30]	Calibration address bus	CAL_ADDR[12:30]	P
CAL_DATA[0:15]	Calibration data bus	CAL_DATA[0:15]	P
CAL_RD_$\overline{WR}$	Calibration read/write	CAL_RD_$\overline{WR}$	P
CAL_$\overline{WE}$/$\overline{BE}$[0:1]	Calibration write/byte enable	CAL_$\overline{WE}$/$\overline{BE}$[0:1]	P
CAL_$\overline{OE}$	Calibration output enable	CAL_$\overline{OE}$	P
CAL_$\overline{TS}$	Calibration transfer start	CAL_$\overline{TS}$	P
Clock Synthesizer			
CLKOUT	System Clock Output	CLKOUT	P

B.3 Device-Specific Information

The various address bus, data bus and bus control signals are sourced from different signals depending on the MPC5500 device used, as detailed in the following sections.

B.3.1 MPC5566 Calibration Bus Implementation

The MPC5566 device has a set of external bus signals that are only used by the calibration bus. These device signals are prefixed by CAL, and their use does not affect the usage modes and electrical loading on the equivalent signals for the EBI.

B.4 Signals and Pads

The following sections detail the signal descriptions for the calibration bus.

B.4.1 CAL_$\overline{CS}$[0:3] — Calibration Chip Selects 0 through 3

CAL_$\overline{CS}$[*n*] is asserted by the master to indicate that this transaction is targeted for a particular calibration memory bank.

The calibration chip selects are driven by the EBI. CAL_$\overline{CS}$[*n*] is driven in the same clock as the assertion of $\overline{TS}$ and valid address, and is kept valid until the cycle is terminated. Bus timing is identical to standard EBI timing.

B.4.1.1 Number of Chip Selects and Maximum Memory Size

The trade-off between calibration chip selects and address lines is the same as the trade-off between non-calibration chip selects and address lines for the 324 pin package.

Table B-2. Maximum Memory Size According to Calibration Chip Selects

	Maximum Memory Allocated for Calibration		
	Device 0	**Device 2**	**Device 3**
CAL_$\overline{CS}$[0] only	4 MB	—	—
CAL_$\overline{CS}$[0] and CAL_$\overline{CS}$[2]	2 MB	2 MB	—
CAL_$\overline{CS}$[0] and CAL_$\overline{CS}$[2:3]	1 MB	1 MB	1 MB

B.4.2 Pad Ring

This section provides a list of the calibration pins and associated pad configuration registers (PCRs), including links to the detailed PCR information for each pin or pin group.

Refer to Table B-1 for device signal names.

The drive strength of the calibration pins is configured in the PCR registers. In some cases, multiple pads have their drive strengths controlled by one PCR by grouping the pins:

- CAL_ADDR[12:30]
- CAL_DATA[0:15]
- CAL_RD_$\overline{WR}$, CAL_$\overline{WE}$/$\overline{BE}$[0:1], CAL_$\overline{OE}$, CAL_$\overline{TS}$

The SIU_PCR registers control whether the CAL_$\overline{CS}$[2:3] pins are used for CAL_$\overline{CS}$[2:3] or for CAL_ADDR[10:11]. Refer to Table B-2 for the pin assignments. Selecting between CAL_$\overline{CS}$[2:3] and CAL_ADDR[10:11] allows you to maximize the amount of calibration memory size by limiting the number of calibration chip selects to $\overline{CS}$[0]. Refer to Section B.4.1.1, "Number of Chip Selects and Maximum Memory Size."

B.4.3 CLKOUT

CLKOUT is supplied by the clock control block, not the EBI. Nevertheless, the same CLKOUT is used for both the non-calibration and calibration bus.

A drawback of having just one CLKOUT is that while the difference in board timing can be compensated by the adjustment in the drive strength, the CLKOUT timing, and hence the timing of the non-calibration bus, can have minor differences with a calibration tool from the production package.

B.5 Packaging

The addition of the calibration bus means that the device has more pads than can be connected to the balls on a 416 pin package. Therefore, the die is assembled in a 496 pin chip scale package (CSP) and this package is used in the VertiCal base assembly.

B.6 Power Supplies

The signals that make up the calibration bus have their own power supply segment (V_{DDE12}). The V_{DDE12} power supply balls are not connected to any other power supply segment from the standard package ball-out but are routed on the VertiCal base to pins on the VertiCal connector. The VertiCal top board must provide voltage to the V_{DDE12} power supply pins to power up the calibration bus.

B.7 Integration Logic Functionality

The EBI connects to both the non-calibration and calibration buses. The integration logic on MPC5566 selects between the data input from both buses to the EBI.

The MPC5566 integration logic also suppresses the reflections of the outputs of the calibration bus onto the non-calibration bus. For the non-calibration bus pins that do not have a negated state to which the pins return at the end of the access, this reflection suppression is enabled by the SIU_CCR[CRSE] bit. SIU_CCR[CRSE] does not enable reflection suppression for the non-calibration bus pins that have a negated state to which the pins return at the end of an access. Those reflections always are suppressed. Furthermore, the suppression of reflections from the non-calibration bus onto the calibration bus is not enabled by CRSE. Those reflections are also always suppressed.

Refer to Section B.8.1, “Enabling Calibration Reflection Suppression,” for when to set SIU_CCR[CRSE] or leave it in its reset negated state.

B.8 Application Information

B.8.1 Enabling Calibration Reflection Suppression

Set SIU_CCR[CRSE] to suppress reflections when calibrating. The calibration reflection suppression logic for an output that does not return to a negated state at the end of an access can introduce a small glitch on the output at the end of the access. The glitch does not interfere with the output valid or hold times. However, keep SIU_CCR[CRSE] in its reset negated state when not calibrating to prevent a glitch on the non-calibration bus outputs.

B.8.2 Communication With Development Tool Using I/O

The development tool can require some I/Os for communication between the MCU and the development tool on the VertiCal connector. ETRIG[0:1] and GPIO[205] are available only in the 416 pin package. Because the application can not use these pins in the 208 and 324 pin packages, they can be used for development tool use in a VertiCal connector. Using ETRIG[1] and GPIO[205] still leaves ETRIG[0] for the application in the 416 package.

B.8.3 Matching Access Delay to Internal Flash With Calibration Memory

One use of VertiCal in the Automotive environment is engine calibration. For this application, an SRAM Top Board is added onto the VertiCal connector. This allows the engine calibrator to modify settings in SRAM, possibly using the Nexus interface or even by using the SCI port or a CAN interface.

Refer to Table 13-3“Internal Flash External Emulation Mode.”

After the data is calibrated, it can be copied into the internal flash. The internal flash can be accessed faster than the calibration memory, and the change in calibration data access time can change the overall system performance. To mitigate this change in system performance, the internal flash memory includes a feature that allows accesses to portions of the flash to be slowed down by adding extra wait states. This is done by multiply mapping the internal flash at different locations with different number of wait states. For example, the physical address of the flash array is 0x0000_0000 to 0x00FF_FFFF (depending on array size). That same flash data can be accessed at address 0x0100_0000 to 0x01FF_FFFF but accesses are one clock cycle slower. That same flash data can be accessed at addresses 0x0200_0000 to 0x02FF_FFFF but accesses are two clock cycles slower. This pattern is repeated through the memory map to addresses 0x1F00_0000 to 0x1FFF_FFFF where accesses are 31 clock cycles slower.

The application can use this feature by mapping the calibration data to a region of the flash memory that has access timing to match the timing of the calibration RAM used when calibrating the data. This remapping of calibration data can be achieved by either using the translation feature of the MMU or rebuilding the code with a modified link file.

Appendix C
MPC5566 Reference Manual Revision History

This appendix describes corrections incorporated to the *MPC5566 Microcontroller Reference Manual, Rev. 1* to create *revision 2*. The corrections are listed chronologically, from changes to the first revision published to the most recent changes located at the end of this appendix.

Each section details the changes between the last published revision and this published revision. Revision changes are listed in sequential order by chapter, as shown in the following table:

C.1 Changes Between Revisions 1 and 2

Table C-1. MPC5566 Changes Between Revisions 1 and 2

Chapter	Description
Chapter 1	Section 1.2, “Features”: • Changed “Parallel programming mode to support rapid end of line programming” to “Page programming mode to support rapid end of line programming” • Added page footnote to read: Although this device has a maximum of 329 interrupts, the logic requires that the total number of interrupts be divisible by four. Therefore, the total number of interrupts specified for this device is 332. Table 1-3 MPC5500 Product Family Comparison: • Changed to comply with the changes submitted for the marketing document. Section 1.5, “MPC5500 Family Memory Map”: • Added the following text about reserved bits and memory: Reserved register bits are allocated for future products and have a default value of zero. When writing to a register, the reserved bits default values must be written as well. Most device features are activated by writing a non-zero value to them. Reserved memory is allocated for future products, therefore do not write to memory segments that are designated as reserved.
	Section 1.2 Features: Under Operating Parameters: Changed to Fully static operation, up to 144 MHz. Figure 1-1. Block Diagram: Changed 1 eQADC to 2 eQADC.

Table C-1. MPC5566 Changes Between Revisions 1 and 2 (continued)

Chapter	Description
Chapter 2 “Signal Description”	Table 2-4. Signal Description table: Changed footnote 3 to 1.3–3.3 V supplies are ±10%. Changed footnote 16 to: The function of the MDO[11:4]_GPIO[82:75] pins is selected during a debug port reset by the $\overline{\text{EVTI}}$ pin or by selecting FPM in the NPC_PCR.
	Added the following to Section 2.1, “Block DiagramRev. 2 To provide an extensive feature set as well as compatibility between the MPC5500 family of devices, the majority of balls are assigned multiplexed signal functions. Figure 2-1 shows only the signals that are available on the device. Signal functions that are not available on this device are not shown in the diagram.
	Table 2-1 includes the primary signal functions that are not available on the device but are used as pin labels in the Ball Grid Array (BGA) map. Read the last two columns in Table 2-1 for a comparison of available signals on the package compared to the VertiCal assembly. NOTE The Vertical assembly has ball connections for all the available signals on the device.
	Added to Table 2-1 MPC5566 Signal Properties, a footnote to PLLCFG[2]: “PLLCFG[2] must be tied to ground.”
	Added TXDA as an alternate signal to CNTXA_GPIO[83]; and RXDA as an alternate signal to CNRXA_GPIO[84]. Added to graphic 2-2, table 2-3, and the signal description section.
	Changed in Figure MPC5566 Signals: From: GPIO[4:27]_ADDR[6:7]_ADDR[8:31] To: GPIO[4:25]_ADDR[8:29] Added: GPIO[26:27]_ADDR[6:7]_ADDR[30:31]

Chapter 3
“e200z6 Core Complex”
	Change to Table 3-11. Interrupts and Conditions, IVOR3:
	• Access control.
	• Precise external termination error and MSR[EE] = 1.
	• Byte ordering due to:
	  • misaligned access across page boundary to pages with mismatched VLE bits
	  • access to pages with VLE set
	with E indicating little-endian.
	• Misaligned instruction fetch due to a change of flow to an odd halfword instruction boundary on a Book E (non-VLE) instruction page as a result of the value in LR, CTR, or SRR0.
	Additional description added to Table 3-11. Interrupts and Conditions for the following interrupts:
	• Machine check
	• Data Storage
	• Instruction Storage

Chapter 4 “Reset”	Section “Watchdog Timer/Debug Reset” reworded.

Table C-1. MPC5566 Changes Between Revisions 1 and 2 (continued)

Chapter	Description
Chapter 5 “Peripheral Bridge”	Added footnote 2 to register figures 5-3 and 5-4 for the SP0 and TP0 bits: The SP0 and TP0 bits default values are always used, even though the bits are writeable. Added Notes to table 5-5 for the SP0 bit: **Note:** For PBRIDGE_A_PACR0 and PBRIDGE_B_PACR0, you must have supervisor privileges to access PBRIDGE registers. **Note:** Even though the SP0 bit (1) is writeable, the reset value for SP0 is always used. Added Notes to table 5-5 for the TP0 bit: **Note:** For PBRIDGE_A_PACR0 and PBRIDGE_B_PACR0, you must have trusted master privileges to access PBRIDGE registers. **Note:** Even though the TP0 bit (1) is writeable, the reset value for TP0 is always used.
	Added to Section 5.3.1.1Master Privilege Control Register: Although these registers are read/write, the reserved fields shown do not apply to this device and must remain at the reset value, therefore only write the fields’ reset value to the reserved fields of these registers. Also changed the read value of the reserved fields to 0111.
Chapter 6 “System Integration Unit”	Added PCR71 TEA_GPIO.
	Corrected the pin numbers in the PA tables for the following pad configuration registers (PCRs): PCR57, PCR58, PCR59, PCR84, PCR95.
	Corrected register addresses in register diagrams for the following PCRs: PCR122–PCR124, PCR127–PCR133, PCR199–PCR200. Reversed register addresses in register diagrams for PCR225–PCR220.
Chapter 7 “Crossbar Switch”	Added to Register Descriptions section: “Please note the difference in numerical values of XBAR Master Port and Master ID as shown in Table 7-3 XBAR Switch Ports.” Changed wording of reserved fields in registers: From: “Reserved” To: “Reserved, must be cleared.”
	Table 7-4 *XBAR_MPRn Descriptions*: Added text for MPR3 and MPR6 fields that all other values than those stated are invalid. Changed ‘Reserved’ to ‘Invalid value”. Figure 7-2 *XBAR_MPRn Register*: Made MPR3 (not included) and MPR6 (not included) fields visible and read/write. Table 7-5 *XBAR_SCPCRn Field Descriptions*: Changed ‘Reserved’ values for the Park field to ‘Invalid value’.
Chapter 8 “Error Correction Status Module”	• Added to section *Initialization and Application*, several paragraphs on precise exception requirements. • Added tables ‘Non-correctable Data ECC States’ and ‘MSR[EE] and MSR[ME] Bit Settings.
	• Added footnote numeral 1 to the RESET rows of all figures that have undefined values upon reset.
	Changed Step 2 in the ECC procedure in Section 8.1.1 Overview to: 2. If the access is a write, then: a. Merger new byte / halfword / word or doubleword into the 64 bits and calculate a new ECC value. b. Write the 64 bits and the ECC are to SRAM.
	Section 8.3 Initialization and Application Information expanded to include exception processing.

Table C-1. MPC5566 Changes Between Revisions 1 and 2 (continued)

Chapter	Description
Chapter 9 “Enhanced Direct Memory Access”	In the section on DMA Performance, made this change: • FROM: removed eDMA Peak Transfer Rate table • TO: Added an eDMA Peak Transfer Rates table (Table 9-22) with columns that show the effect of buffering enabled and disabled.
	To the TCD Structure diagram, added this footnote to the CITER and BITER fields: “If channel linking on minor link completion is disabled, TCD bits [161:175] are used to form a 15-bit CITER field; if channel-to-channel linking is enabled, CITER becomes a 9-bit field.”
	Removed the Note: referring to bit 2 in the following tables: EDMA_SERQR, EDMA_CERQR, EDMA_SEEIR, EDMA_CEEIR, EDMA_CER, EDMA_SSBR, EDMA_CDSBR.
Chapter 10 “Interrupt Controller”	**NOTE** Reading the INTC_IACKR acknowledges the interrupt request to the processor and updates the INTC_CPR[PRI] with the priority of the preempting interrupt request. If the processor recognition of interrupts is disabled during the LIFO restoration, interrupt requests to the processor can go undetected. However, since the peripheral or software settable interrupt requests are not cleared, the peripheral interrupt request to the processor re-asserts when INTC_CPR[PRI] is lower than the priorities of those peripheral or software settable interrupt requests.
	Section 10.5.6, “Selecting Priorities According to Request Rates and Deadlines Added the acronyms RMS and DMS for ‘rate monotonic scheduling’ and ‘deadline monotonic scheduling.’ • From: “Reducing the number of priorities does cause some priority inversion which reduces the processor's ability to meet its deadlines. It also allows easier management of ISRs with similar deadlines that share a resource. They can be placed at the same priority without any further priority inversion, and they do not need to use the PCP to access the shared resource” • To: “Reducing the number of priorities does reduce the processor's ability to meet its deadlines. However, it also allows easier management of ISRs with similar deadlines that share a resource. They do not need to use the PCP to access the shared resource.
	Throughout the chapter, replaced “priority inversion” with “scheduling inefficiencies”
	Added this sentence to “Scheduling a Lower Priority ...” section: “After generating a software settable interrupt request, the higher priority ISR completes. The lower priority ISR is scheduled according to its priority. Execution of the higher priority ISR is not resumed after the completion of the lower priority ISR”
	Table 10-9 Combined adjacent reserved areas of memory.
	Figure 10-1 *INT Block Diagram*: Changed key for diagram from: ‘Non-memory mapped logic’ To: Logic not memory-mapped. Changed footnote 1 from: The total number of interrupt sources is 332, which includes 26 reserved source and 8 software sources To: Although N = 329, the total number of interrupts must be a multiple of four. Therefore, the total number of interrupts is 332: 208 peripheral IRQs, 8 software-configurable IRQs, and 26 reserved IRQs
	Figure 10-3 *Program Flow–Software Vector Mode*: Added footnote 1 in text frame inside figure that reads: N is the maximum number of usable interrupt vectors. which equals 329, and includes 26 reserved IRQ vectors and eight software-settable IRQ vectors. Because the memory is mapped in four-byte words, the total number of interrupt vectors must be a multiple of four, therefore one more interrupt vector exists to complete the word. This results in a total of 332 interrupt vectors. However, interrupt vector 332 is reserved and not available.

Table C-1. MPC5566 Changes Between Revisions 1 and 2 (continued)

Chapter	Description
	Figure 10-4 *Program Flow–Hardware Vector Mode*: Added two notes that read: Address IVPR + 0x1480 contains the 329 interrupt vector and is the last usable interrupt vector address in the interrupt memory map for this device. and N is the maximum number of usable interrupt vectors. which equals 329(address is IVPR + 0x1480), and includes 26 reserved IRQ vectors and eight software-settable IRQ vectors. Because the memory is mapped in four-byte words, the total number of interrupt registers must be a multiple of four, therefore another interrupt vector exists in memory to complete the word for a total of 332 interrupt vectors. However, the 332 interrupt vector is reserved and is not available.
Chapter 10 “Interrupt Controller” (continued)	Table *Interrupt Sources*: Added to column one heading ‘Hardware Vector Mode’ before ‘Offset’. Added to column two heading ‘Number” after ‘vector’ and table footnote 1 that reads: The vector number is used to identify the interrupt and does not indicate the maximum number of usable interrupt sources.
	Added the following sentence to the second paragraph in section 10.5.5.2: ‘Interrupts must be enabled before executing the GetResource code sequence.’ Added a blank line between the GetResource code and the ReleaseResource code sequence for clarity and readability,
	Added another row at the end of Table 10-9: MPC5566 Interrupt Sources: 0x1490–0x14B0; 329–331; Reserved; 32-bit.
	Section 10.5.2.1 Software Vector Mode: Corrected the comment code for the mtlr r3 code line to: `move the INTC_IACKR address into the link register`
Chapter 11 “Frequency Modulated Phase Locked Loop and System Clock”	Section FMPLL Calibration Routine: Corrected the equation at the end of the third paragraph: changed value of M from 640 to 480.
Chapter 12 “External Bus Interface”	Added the following introductory sentence to Figure 12-1 EBI Block Diagram: The following figure shows the MPC5566 EBI block diagram on the 416 package. The $\overline{BR}$, $\overline{BG}$, and $\overline{BB}$ signals are used for arbitration on the external bus:
	Added the following calibration bus signals to Figure 12-1 EBI Block Diagram: CAL_$\overline{OE}$, CAL_RD_$\overline{WR}$, CAL_$\overline{TS}$, CAL_$\overline{WE}$/$\overline{BE}$[0:1], CAL_ADDR[12:30], CAL_DATA[0:15].
	• Added the following introductory sentence to section External Signal Description: The EBI signal pinouts depend on the type of package. • Removed the 324 package column in Signal Properties table.
	Added footnote to the 496 BGA package column in the Signals Properties table: All EBI and calibration signals designed for this device are available on the 496 VertiCal assembly.
	Moved the following paragraph from the Detailed Signal Description section to the Calibration Signal section: ‘During a calibration bus access, the non-calibration bus signals (other than DATA) are held in a negated state, with the exception of RD_$\overline{WR}$ and ADDR, which reflect the same values shown on the calibration version of those signals. Because the $\overline{TS}$ and $\overline{CS}$ signals are held negated on the EBI (non-calibration bus) during calibration accesses, no transfer occurs on the EBI. During an EBI bus access, the calibration bus signals (other than CAL_DATA) are held in a negated state. CAL_DATA is not driven during non-calibration accesses.

Table C-1. MPC5566 Changes Between Revisions 1 and 2 (continued)

Chapter	Description
	Section Separate Input Clock for Registers, For readability, changed from: • The clock signal dedicated to the registers, however, allows access to the registers even while the EBI is in the module disable mode. to: • The dedicated clock signal allows access to the registers even while the EBI module is in disable mode.
Chapter 12 “External Bus Interface” (continued)	Table Signal Function According to EBI Mode Settings: • Combined two rows labelled Data[16:31] into one row labelled Data[0:21]. Combined three WE/BE rows: one WE[0:]/BE[0:1] and two WE[2:3]/BE[2:3] to WE/BE[0:3]. • Added the calibration signals: CAL_DATA[0:15], CAL_ADDR[12:30], CAL_$\overline{OE}$, CAL_$\overline{TS}$, CAL_RD_$\overline{WR}$, CAL_$\overline{WE}$/$\overline{BE}$[0:1] • Added footnote: These signals are muxed with the chip select ($\overline{CS}$) signals on this device. Use the pad configuration registers (PCR) in the system integration module (SIU) to configure the balls to use the address signals *or* chip select signals–not both. • Added footnote: This device is designed to support a 32-bit EBI data bus (DATA[0:31]) and four write/byte enable signals ($\overline{WE}$/$\overline{BE}$[0:3]) using the VertiCal assembly.
	Renamed the table title from ‘Transaction Sizes Supported by EBI’ to ‘Valid EBI Transaction Sizes (Number of Bytes)’
	Section Size, Alignment, and Packaging on Transfers: Changed first paragraph from: • Table 12-18 shows the allowed sizes that an internal or external master can request from the EBI. The behavior of the EBI for request sizes not shown below is undefined. No error signal is asserted for these erroneous cases. To: • Table 12-18 shows the allowed sizes that an internal or external master can request from the EBI. EBI transfer request sizes not listed in the table are undefined. No error signal is asserted for these invalid cases.
	Changed text in Section Booting from External Memory from: If code in external memory must write EBI registers, avoid modifying EBI registers while external accesses are in progress by using the following method: • Copy to internal SRAM the code that writes to the EBI registers (plus a return branch) • Branch to internal SRAM to run the code, ending with a branch back to external flash To: If code in external memory must write EBI registers, avoid modifying EBI registers while external accesses are in progress by using the following method: 1. Copy to internal SRAM the code that writes to the EBI registers (plus a return branch) 2. Branch to internal SRAM to run the code, ending with a branch back to external flash
	Added section 12.4.1.18 Misaligned Access Support.
Chapter 13 “Flash Memory”	No changes.
Chapter 14 “Internal Static RAM”	Removed L2 designation from the sample code.
Chapter 15 “Fast Ethernet Controller”	Added footnote: “w1c” signifies the bit is cleared by writing 1 to it.” to Figure 15-4, Ethernet Interrupt Event Register.

Table C-1. MPC5566 Changes Between Revisions 1 and 2 (continued)

Chapter	Description
Chapter 16 “Boot Assist Module”	In the Serial Boot Mode section: From: “This mode of operation is intended to load a user program into internal SRAM using either the eSCI or CAN serial interface, then to execute that program” To: “This mode of operation can load a user program into internal SRAM using either the eSCI or FlexCAN serial interface, then execute the downloaded program”
Chapter 17 “Enhanced Modular Input/Output Subsystem”	In Section Pulse Edge/Accumulation Mode: changed the following text From: Triggering of the counter clock (an input event) is done by a rising or falling edge or both edges on the on the input pin. To: The counter clock (an input event) is triggered by a rising or falling edge, or by both the rising and falling edges on the input pin.
Chapter 18 “Enhanced Time Processing Unit”	• Duplicate sentence removed: Each function can require a different number of parameters. During eTPU initialization the host has to program channel base addresses, allocating proper parameters for each channel according to its selected function. • Changes to Table 18-11, ETPU_TBCR Field Descriptions: TCR2CTL field, AM=0 column: 101 Peripheral time base clock source, 110 Do not use with AM=1. Moved table note into AM=1 column.
	In Section “eTPU Operation Overview”, changed: • FROM: “A thread be interrupted only by resetting the entire eTPU module.” • TO: “The core can terminate the thread by writing 1 to the FEND bit in the ETPUECR register.”
	Figure 18-3: changed title from SDM Write to SDM PSE Area Write.
	In Section “Time Bases” removed the words “or be driven by” from the sentence • FROM: “The TCRs drive or be driven by an eMIOS time base through the shared time and counter (STAC) bus, or they be written by eTPU function software.” • TO: It now reads ““The TCRs can also drive an eMIOS time base through the shared time and counter (STAC) bus, or they be written by eTPU function software.”
	In Section “Features” changed: • FROM: “The first time base be clocked by the system clock with programmable prescaler division from 2 to 512 (in steps of 2), or by the output of the second time base prescaler.” • TO: “The first time base can be clocked by the system clock with programmable prescaler division from 2 to 512 (in steps of 2) Added this bullet: • “The second time base has a programmable prescaler that applies to all TCR2 clock inputs except the angle counter.” Changed: • FROM: “32-bit microengine registers and 24-bit resolution ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands: single bit manipulation, shift operations, sign extension and conditional execution.” • TO: “24-bit registers and ALU, plus one 32-bit register for full-width SDM access” Added these bullets: • Hardware breakpoints on data access, qualified by address and/or data values. • Hardware breakpoints on instruction address.
	In Section “External Signal Description” corrected the number of external signals to 65 from 69. The four output disable input signals are now designated as internal signals. Changed wording in SCMMISF bit: • FROM: “This bit is automatically cleared when SCMMISEN changes from 0 to 1, or when global exception is cleared by writing 1 to GEC.” • TO: "This bit is cleared by writing 1 to GEC."
	In Section “eTPU SCM Off-Range Data Register (ETPU_SCMOFFDATAR)” added a NOTE.

Table C-1. MPC5566 Changes Between Revisions 1 and 2 (continued)

Chapter	Description
	In Section “eTPU Operation Overview”, changed: • FROM: “A thread be interrupted only by resetting the entire eTPU module.” • TO: “The core can terminate the thread by writing 1 to the FEND bit in the ETPUECR register.”
Chapter 18 “Enhanced Time Processing Unit” (continued)	In Section “eTPU Engine Configuration Register (ETPU_ECR)”: • In the MDIS bit, changed the Note to read: “After MDIS has been switched from 1 to 0 or vice-versa, do not switch its value again until STF switches to the same value.” • In the STF bit, removed the words “or after the STAC but stop has been asserted” from the STF bit description.
	In Table, “ETPU_TBR Field Descriptions, in the TCR2CTL field, removed the phrase: “TCR2 can also be clocked by an internal peripheral timebase signal.”
Chapter 19 “Enhanced Queued Analog-to-Digital Converter	Changes to Table 18-11, ETPU_TBCR Field Descriptions: TCR2CTL field, AM=0 column: 101 Peripheral time base clock source, 110 Do not use with AM=1. Moved table note into AM=1 column.
Chapter 20 “Deserial Serial Peripheral Interface”	Changed the NOTE in the DSPI_PUSHR register: From: “Only the TXDATA field is used for slaves.” To: “TXDATA is used in master and slave modes.”
	Section 19.5.5.2, “Address Calculation for the First-in Entry and Last-in Entry in the RX FIFO” Changed from: First-in entry address = TX FIFO base + [4 x (POPNXTPTR)] to: First-in entry address = RX FIFO base + [4 x (POPNXTPTR)]
	Numbered and edited the steps in section ‘How to Change Queues.” Changed the following section titles: • From: Modified SPI/DSI Transfer Format (MTFE = 1, CPHA = 0) To: Modified Transfer Format Enabled (MTFE = 1) and Classic SPI Transfer Format Cleared (CPHA = 0) for SPI and DSI • From: Modified SPI/DSI Transfer Format (MTFE = 1, CPHA = 1) To: Modified Transfer Format Enabled (MTFE = 1) with Classic SPI Transfer Format Set (CPHA = 1) for SPI and DSI
Chapter 21 “Enhanced Serial Communication Interface”	No changes.
Chapter 22 “FlexCAN2 Controller Area Network”	No changes.
Chapter 23 “Voltage Regulator Controller and POR”	No changes.
Chapter 24 “IEEE 1149.1 Test Access Port Controller”	No changes.
Chapter 25 “Nexus Development Interface”	No changes.

Table C-1. MPC5566 Changes Between Revisions 1 and 2 (continued)

Chapter	Description
Appendix A “MPC5566 Register Map”	No changes.
Appendix B “Calibration”	Added footnote to the following signals in the Calibration Bus Signals table: $\overline{WE}/\overline{BE}$[2,3] ADDR[8:11] $\overline{TEA}$ The footnote reads: Not available on the 324 package.
	Removed the reference to the 324 package in figures 1 and 2: Calibration Assembly and Vertical Base.