UM12208

RDGD3162MITEVM three-phase inverter reference design

Rev. 1.0 — 15 January 2025 User manual

Document information

Information	Content
Keywords	GD3162, gate driver, power, inverter, automotive
Abstract	The RDGD3162MITEVM three-phase inverter is a functional hardware power inverter reference design, which can be used as a foundation to develop a complete ASIL D compliant high-voltage, high-power traction motor inverter for electric vehicles. This inverter is compatible with the Mitsubishi CTF700CJ3D130 SiC power module.

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1 Introduction

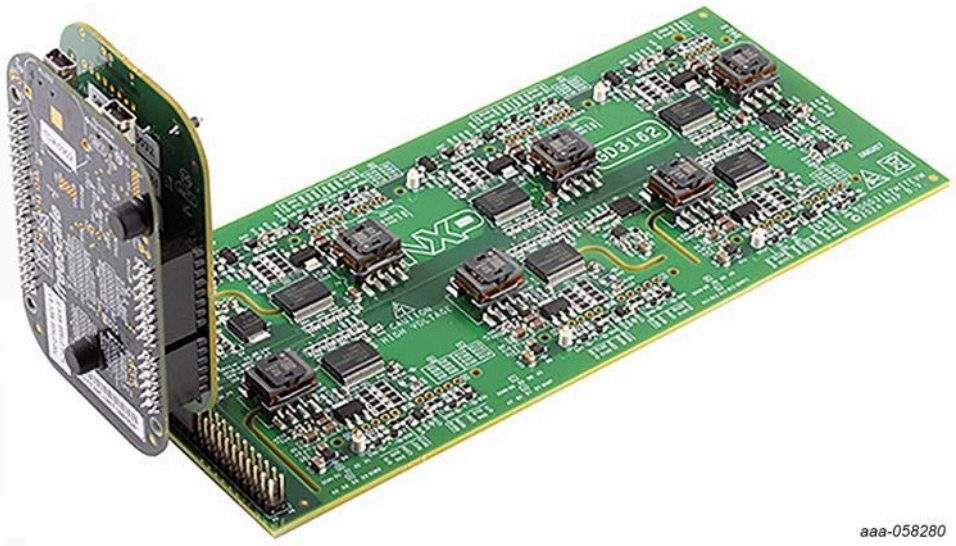

Figure 1. RDGD3162MITEVM

This document is the user manual for the RDGD3162MITEVM reference design. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of the GD3162 single-channel gate driver for insulated gate bipolar transistor (IGBT)/SiC metal-oxide-semiconductor field-effect transistor (MOSFET).

The scope of this document is to provide the user with information to evaluate the GD3162 single-channel gate driver for IGBT/SiC. This document covers connecting the hardware, installing the software and tools, configuring the environment, and using the kit.

The RDGD3162MITEVM is a fully functional three-phase inverter evaluation board populated with six GD3162 gate drivers with fault management and supporting circuitry. This board supports serial peripheral interface (SPI) daisy-chain communication for programming and communication with three high-side gate drivers and three low-side gate drivers independently, or all six gate drivers at the same time.

This board has low-voltage isolation and high-voltage isolation with gate-drive integrated galvanic signal isolation. Other supporting features on the board include desaturation short-circuit detection, IGBT/SiC temperature sensing, onboard isolated flyback supplies, DC-link bus-voltage monitoring, phase-current sensing, DC-link bus-current sense, and motor-resolver excitation/processing. Refer to the GD3162 data sheet https://www.nxp.com/GD3162#documentation for more gate drive features. The data sheet requires a secure access rights request to download the document.

2 Finding kit resources and information on the NXP website

NXP Semiconductors provides online resources for this reference design and its supported devices on http://www.nxp.com.

The information page for the RDGD3162MITEVM reference design is at http://www.nxp.com/RDGD3162MITEVM. The information page provides overview information, documentation, software and tools, ordering information and a Getting Started tab. The Getting Started tab provides quick reference information applicable to using the RDGD3162MITEVM reference design, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, asking and answering technical questions, and receiving input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 Getting ready

Working with the RDGD3162MITEVM requires the kit contents and a Windows PC workstation with the FlexGUI 2 for GD3162 software installed.

3.1 Kit contents

- Assembled and tested RDGD3162MITEVM (three-phase inverter populated with 5 V compatible gate-driver devices) board in an antistatic bag
- KITGD316xTREVB 3.3 V to 5.0 V translator with FRDM-KL25Z MCU board with micro-USB cable
- Quick start guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is beneficial when working with this reference board.

- Microcontroller for SPI communication
- Compatible Mitsubishi CTF700CJ3D130 SiC MOSFET module
- DC-link capacitor compatible with SiC MOSFET module
- HV power supply with protection shield and hearing protection
- Current sensors for monitoring each phase current
- 12 V, 1.0 A DC power supply
- Four-channel oscilloscope with appropriate isolated probes

3.3 Windows PC workstation

This reference design requires a Windows PC workstation. Meeting these minimum specifications produces great results when working with this evaluation board.

- USB-enabled computer with Windows 10 or higher operating system.

3.4 Software

Installing software is necessary to work with this reference design. All listed software is available on the information page at http://www.nxp.com/RDGD3162MITEVM.

- FlexGUI 2 for GD3162 software for using with KITGD316xTREVB MCU/translator board
- S32S Design Studio IDE for power architecture
- Automotive Math and Motor Control Library (AMMCLib)
- FreeMASTER 2.0 runtime debugging tool
- Motor control application tuning (MCAT)
- Example code, GD3162 device driver notes, and GD31xx device driver reference

4 Getting to know the hardware

4.1 RDGD3162MITEVM features

- Capability to perform double-pulse and short-circuit tests on phase W using KITGD316xTREVB and FlexGUI 2; see phase W schematics and FlexGUI 2 pulse tab (Figure 25 and Figure 27)
- Evaluation board designed for and populated with GD3162 gate drivers and protection circuitry
- Capability to connect to Mitsubishi SiC specific modules for full three-phase evaluation and development
- Daisy-chain SPI communication × 3 - 2 channel (three high-side gate drivers and three low-side gate drivers)
- Flyback VCC power supply with GND reference negative VEE supply

4.2 Kit featured components

4.2.1 Voltage domains, GD3162 pinout, logic header, and IGBT pinout

Low-voltage domain is an externally supplied 12 V DC (VPWR) primary supply for non-isolated circuits, typically supplied by a vehicle battery. A 5 V regulator supplies VDD to GD3162 gate drive devices. The low-voltage domain includes the interface between the MCU and the GD3162 control registers and logic control.

Low-side driver and high-side driver domains are isolated high-voltage driver control domains for SiC MOSFET or IGBT single-phase connections and control circuits. Mounting holes on the bottom of the board are designed to connect easily to a compatible three-phase SiC MOSFET module.

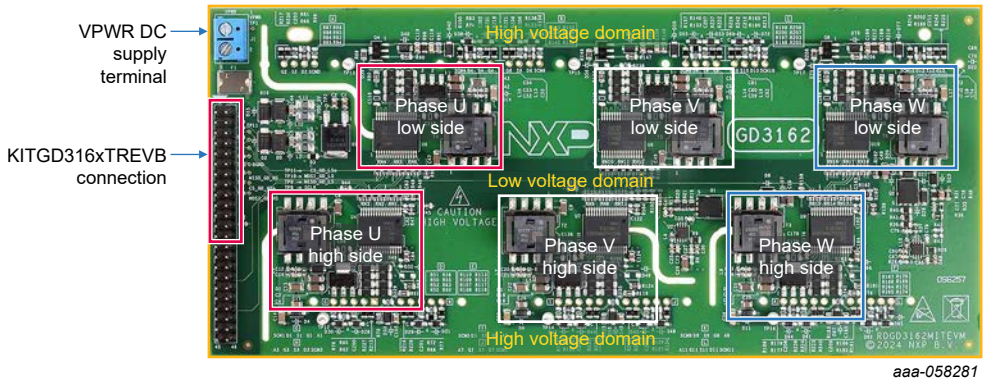

Figure 2. RDGD3162 three-phase inverter board voltage domains and interfaces

4.2.2 GD3162 pinout and MCU interface pinout

Refer to the GD3162 advanced IGBT/SiC gate-driver data sheet for specific information about pinout, pin descriptions, specifications, and operating modes. The VPWR DC supply terminal is a low-voltage input connection for supplying power to the low-voltage non-isolated die and related circuitry. Power is typically supplied by the vehicle battery (12 V DC).

The KITGD316xTREVB included with the kit (MCU and translator) can be attached to this board at the top of the dual-row header pin interface. All gate drivers can be accessed via SPI control using FlexGUI 2 software.

Note: *Double-pulse and short-circuit tests can be conducted on phase W only. See FlexGUI pulse tab Figure 26 and Figure 27.*

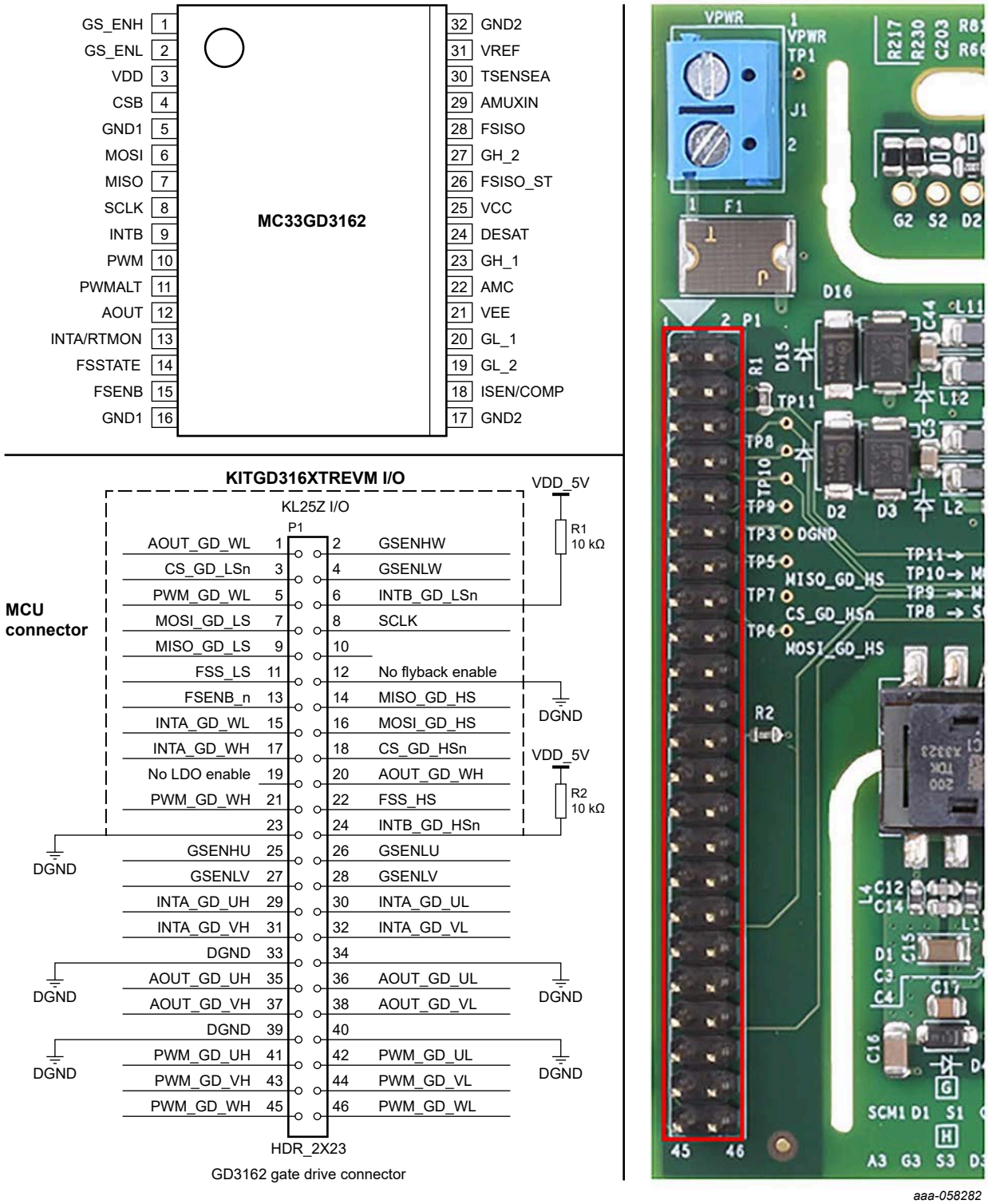

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Figure 3. Gate driver pinout and board interface connection dual row header

Table 1. Dual-row MCU connector P1 pin definitions

Pin	Name	Function
1	AOUT_GD_WL	Analog output phase W low-side
2	GSENHW	Gate-strength enable phase W high-side
3	CS_GD_LS	Chip select all phases low-side
4	GSENLW	Gate-strength enable phase W low-side
5	PWM_GD_WL	Pulse width modulation (PWM) signal phase W low-side
6	INTB_GD_LS	Fault reporting for low-side gate-drive devices
7	MOSI_GD_LS	SPI input signal low-side
8	SCLK	SPI clock
9	MISO_GD_LS	SPI output signal low-side
10	n.c.	Not connected
11	FSS_LS	Fail-safe state low-side
12	DGND	Digital ground
13	FSENB	Fail-safe enable
14	MISO_GD_HS	SPI output high-side
15	INTA_GD_WL	Fault reporting and real-time monitoring low-side phase W
16	MOSI_GD_HS	SPI input high-side
17	INTA_GD_WH	INTA output phase W high-side
18	CS_GD_HS	Chip select all phases high-side
19	n.c.	Not connected
20	AOUT_GD_WH	Analog output phase W high-side
21	PWM_GD_WH	PWM signal phase W high-side
22	FSS_HS	Fail-safe state high-side
23	DGND	Digital ground
24	INTB_GD_HS	Fault reporting for high-side gate drive devices
25	GSENHU	Gate-strength enable high-side phase U
26	GSENLU	Gate-strength enable low-side phase U
27	GSENHV	Gate-strength enable high-side phase V
28	GSENLV	Gate-strength enable low-side phase V
29	INTA_GD_UH	Fault reporting and real-time monitoring high-side phase U
30	INTA_GD_UL	Fault reporting and real-time monitoring low-side phase U
31	INTA_GD_VH	Fault reporting and real-time monitoring high-side phase V
32	INTA_GD_VL	Fault reporting and real-time monitoring low-side phase V
33	DGND	Digital ground
34	DGND	Digital ground
35	AOUT_GD_UH	Analog output phase U high-side
36	AOUT_GD_UL	Analog output phase U low-side
37	AOUT_GD_VH	Analog output phase V high-side
38	AOUT_GD_VL	Analog output phase V low-side
39	DGND	Digital ground
40	DGND	Digital ground

Table 1. Dual-row MCU connector P1 pin definitions*...continued*

Pin	Name	Function
41	PWM_GD_UH	PWM signal phase U high-side
42	PWM_GD_UL	PWM signal phase U low-side
43	PWM_GD_VH	PWM signal phase V high-side
44	PWM_GD_VL	PWM signal phase V low-side
45	PWM_GD_WH	PWM signal phase W high-side
46	PWM_GD_WL	PWM signal phase W low-side

4.2.3 Test points

All test points are clearly marked on the board. Figure 4 shows the location of various test points.

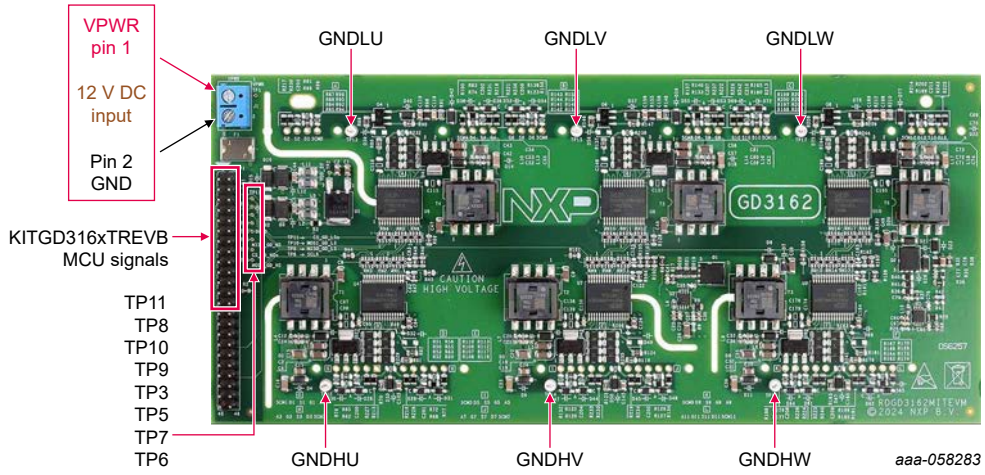


Figure 4. RDGD3162MITEVM test points and isolated grounding points

Table 2. Test points and isolated grounding points

Test point name	Function
VPWR terminal pin 1	Low-voltage power supply connection 12 V DC
GND terminal pin 2	Low-voltage power supply ground connection
TP11	SPI chip select (CS) low-side
TP8	SPI clock (SCLK)
TP10	SPI input (MOSI) low-side
TP9	SPI output (MISO) low-side
TP3	Digital ground
TP5	SPI output (MISO) high-side
TP7	SPI CS high-side
TP6	SPI input (MOSI) high-side
GNDLU	Isolated ground phase U low-side
GNDLV	Isolated ground phase V low-side
GNDLW	Isolated ground phase W low-side
GNDHU	Isolated ground phase U high-side
GNDHV	Isolated ground phase V high-side

Table 2. Test points and isolated grounding points...*continued*

Test point name	Function
GNDHW	Isolated ground phase W high-side

4.2.4 Gate drive resistors

- **RGH_1:** Gate-high resistor in series with the GH_1 pin at the output of the GD3162 high-side driver and IGBT/SiC gate that controls the strong turn-on current for IGBT/SiC gate.
- **RGH_2:** Gate-high resistor in series with the GH_2 pin at the output of the GD3162 high-side driver and IGBT/SiC gate that controls the weak turn-on current for IGBT/SiC gate.
- **RGL_1:** Gate-low resistor in series with the GL_1 pin at the output of the GD3162 low-side driver and IGBT/SiC gate that controls the strong turn-off current for IGBT/SiC gate.
- **RGL_2:** Gate-low resistor in series with the GL_2 pin at the output of the GD3162 low-side driver and IGBT/SiC gate that controls the weak turn-off current for IGBT/SiC gate.
- **RAMC:** Series resistor between IGBT/SiC gate and active Miller clamp (AMC) input pin of the GD3162 high-side/low-side driver for gate sensing and active Miller clamping.

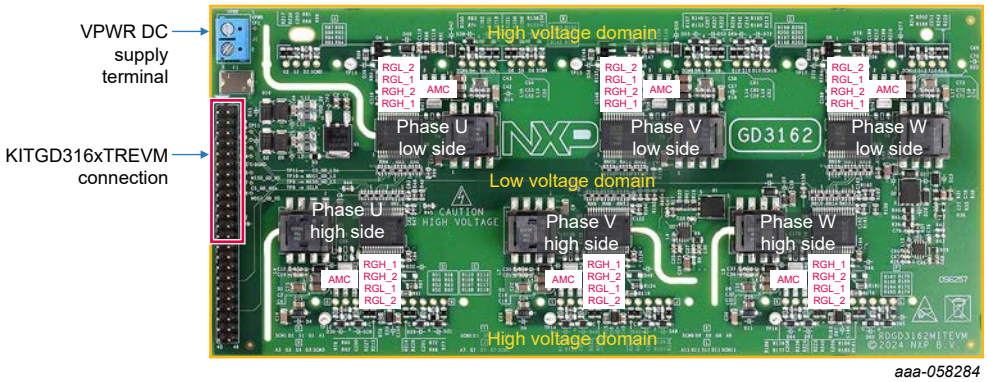


Figure 5. Gate-driver resistors for each phase high side and low side

Note: *Gate resistors installed on the hardware are initial set values and are not optimized for reducing switching energy losses. A characterization would need to be performed at targeted DC link bus voltage and switching current to optimize for switching losses and to maintain the safe operating area of the SiC MOSFET to avoid overshoot.*

4.2.5 Mitsubishi CTF700CJ3D130 (SiC) module pin connections

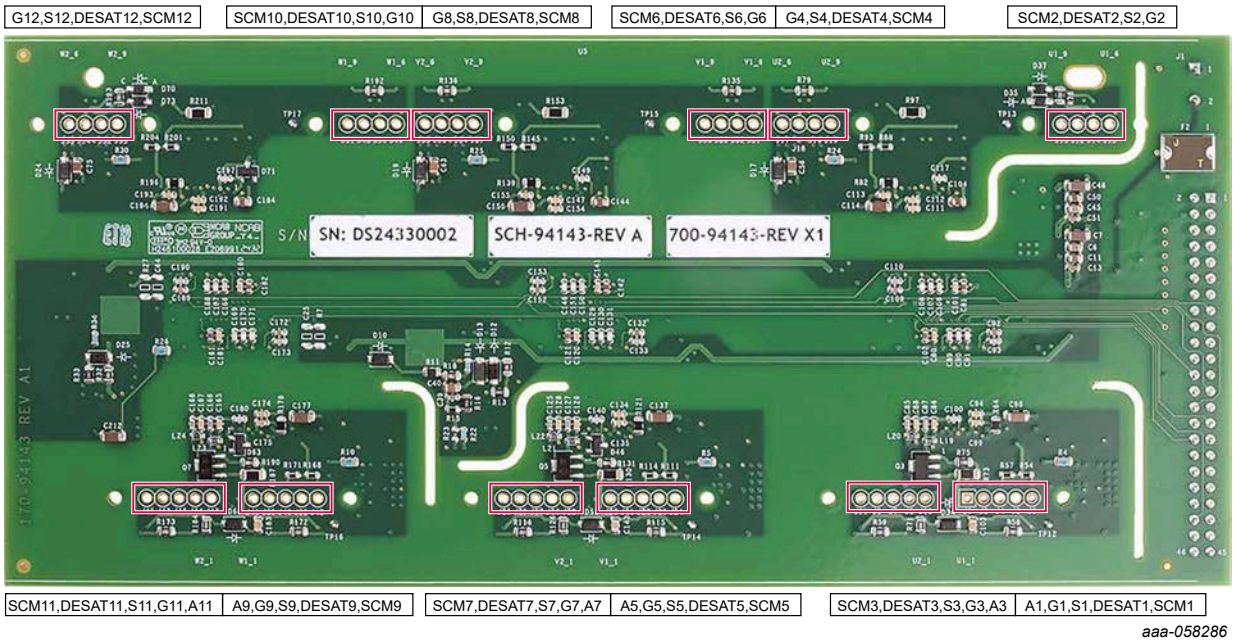


Figure 6. SiC module pin connections

4.2.5.1 Power module connections

These 54 connectors connect the RDGD3162MITEVM board to the corresponding pins on the surface of the CTF700CJ3D130 SiC module [gate, desat, source, short circuit monitor] for each phase. These connectors align with the power module pins so that the RDGD3162MITEVM board can be mounted directly on top of the power module.

Socket pins (not included) can be used to attach the RDGD3162MITEVM board to the SiC MOSFET power module to easily attach and de-attach board from power module if desired. **Mill-Max part# 0405-0-15-15-34-27-04-0**.

Table 3. SiC module pin connections

Connection name	Pin description
DESAT1	Desat diode drain high-side phase U1
G1	Gate high-side phase U1
S1	Source high-side phase U1
A1	Temperature sense diode high-side phase U1
SCM1	Short-circuit monitor high-side phase U1
DESAT2	Desat diode drain low-side phase U1
G2	Gate low-side phase U1
S2	Source low-side phase U1
SCM2	Short-circuit monitor low-side phase U1
DESAT3	Desat diode drain high-side phase U2
G3	Gate high-side phase U2
S3	Source high-side phase U2
A3	Temperature sense diode high-side phase U2

Table 3. SiC module pin connections*...continued*

Connection name	Pin description
SCM3	Short-circuit monitor high-side phase U2
DESAT4	Desat drain low-side phase U2
G4	Gate low-side phase U2
S4	Source low-side phase U2
SCM4	Short-circuit monitor low-side phase U2
DESAT5	Desat diode drain high-side phase V1
G5	Gate high-side phase V1
S5	Source high-side phase V1
A5	Temperature sense diode high-side phase V1
SCM5	Short-circuit monitor high-side phase V 1
DESAT6	Desat diode drain low-side phase V1
G6	Gate low-side phase V1
S6	Source low-side phase V1
SCM6	Short-circuit monitor low-side phase V1
DESAT7	Desat diode drain high-side phase V2
G7	Gate high-side phase V2
S7	Source high-side phase V2
A7	Temperature sense diode high-side phase V2
SCM7	Short-circuit monitor high-side phase V2
DESAT8	Desat diode drain low-side phase V2
G8	Gate low-side phase V2
S8	Source low-side phase V2
SCM8	Short-circuit monitor low-side phase V2
DESAT9	Desat diode drain high-side phase W1
G9	Gate high-side phase W1
S9	Source high-side phase W1
A9	Temperature sense diode high-side phase W1
SCM9	Short-circuit monitor high-side phase W1
DESAT10	Desat diode drain low-side phase W1
G10	Gate low-side phase W1
S10	Source low-side phase W1
SCM10	Short-circuit monitor low-side phase W1
DESAT11	Desat diode drain high-side phase W2
G11	Gate high-side phase W2
S11	Source high-side phase W2
A11	Temperature sense diode high-side phase W2
SCM11	Short-circuit monitor high-side phase W2
DESAT12	Desat diode drain low-side phase W2
G12	Gate low-side phase W2
S12	Source low-side phase W2

Table 3. SiC module pin connections...*continued*

Connection name	Pin description
SCM12	Short-circuit monitor low-side phase W2

4.3 Kinetis KL25Z Freedom board

The Kinetis KL25Z Freedom board is a development platform for the Kinetis L series MCU built on Arm Cortex-M0+ processor.

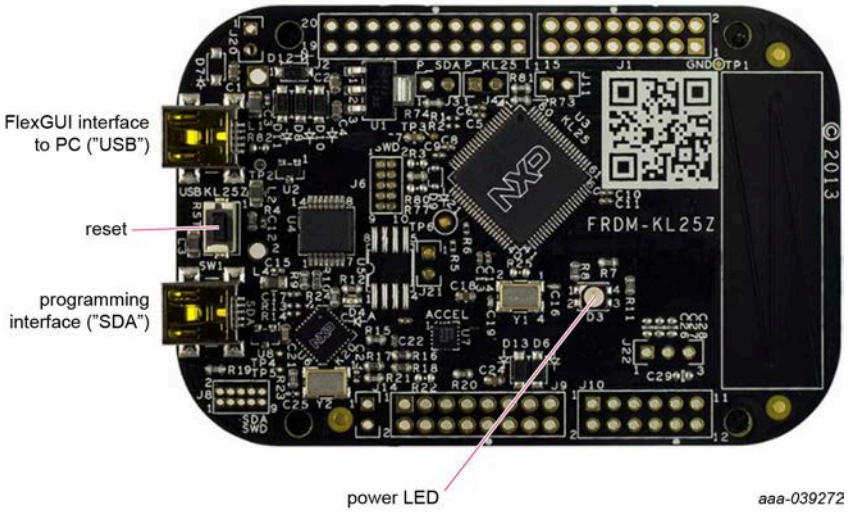


Figure 7. Freedom development platform

4.4 3.3 V to 5.0 V translator board

The KITGD316xTREVB translator enables level shifting of signals from the MCU 3.3 V to 5.0 V SPI communication.

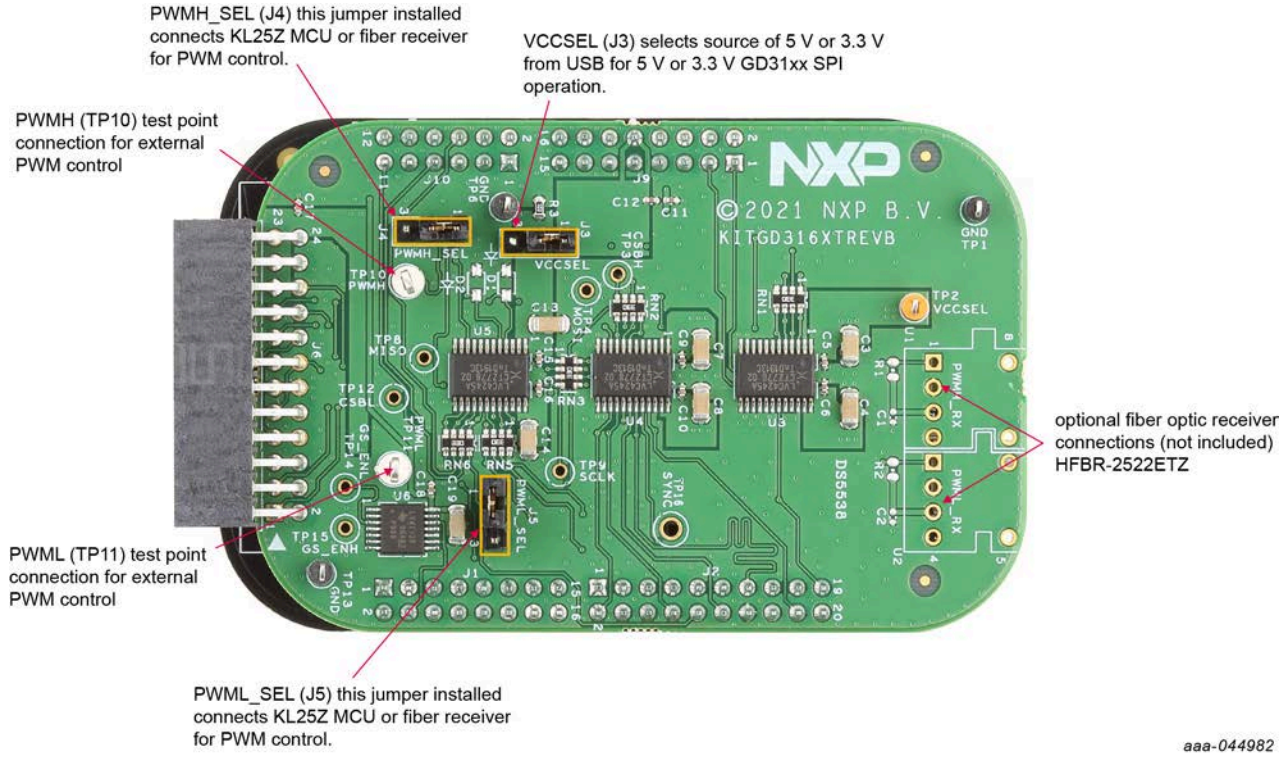


Figure 8. Translator board

Table 4. Translator board jumper definitions

Jumper	Position	Function
VCCSEL (J3)	1-2	Selects 5.0 V for 5.0 V compatible gate drive
	2-3	Selects 3.3 V for 3.3 V compatible gate drive
PWMH_SEL (J4)	1-2	Selects PWM high-side control from KL25Z MCU
	2-3	Selects PWM high-side control from fiber optic receiver inputs
PWML_SEL (J5)	1-2	Selects PWM low-side control from KL25Z MCU
	2-3	Selects PWM low-side control from fiber optic receiver inputs

5 Installing and configuring software tools

Software for the RDGD3162MITEVM is distributed with the FlexGUI 2 for GD3162 software tool (available on nxp.com). Necessary firmware comes preinstalled on the FRDM-KL25Z with the kit.

If the user intends to test with other software or PWM, it is recommended to install this software as a backup or to help debugging.

5.1 Installing FlexGUI 2 for the GD3162 on a computer

The latest version of FlexGUI supports the GD3162 gate driver. It is designed to run on any Windows 10 or higher operating system. To install the software, do the following:

1. Go to www.nxp.com/FlexGUI and click **Download**.
2. When the FlexGUI 2 software page appears, click **Download FlexGUI 2 for GD3162 Advanced Gate Driver Evaluation Software**.
3. The FlexGUI 2 for GD3162 Wizard creates a shortcut. An NXP FlexGUI 2 icon appears on the desktop. Installing the device drivers overwrites any previous FlexGUI 2 installation and replaces it with a current version containing the GD3162 drivers. However, configuration files (.spi) from the previous version remain intact.

5.2 Configuring the FRDM-KL25Z microcode

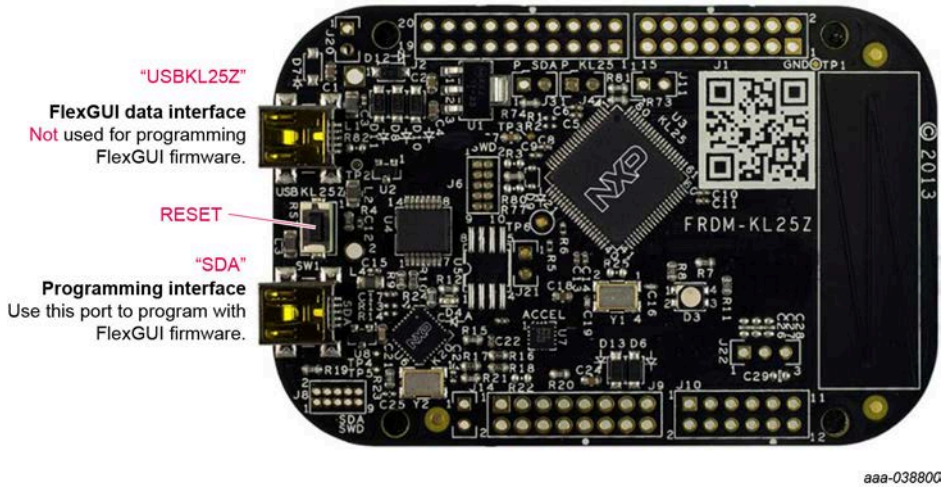


Figure 9. FRDM-KKL25Z setup and interface

By default, the FRDM-KL25Z delivered with this kit is preprogrammed with the most up-to-date firmware available for the kit.

A way to check that the microcode is programmed and the board is functioning properly is to plug the KL25Z into a computer using a USB cable to the USBKL25Z port, open FlexGUI 2, and verify that the software version at the bottom is 1.8 or later (see Figure 9).

If a loss of functionality occurs after a board reset, reprogramming, or a corrupted data issue, the microcode is rewritten per the following steps:

1. To clear the memory and place the board in Bootloader mode, hold down the reset button while plugging a USB cable into the OpenSDA USB port.
2. Verify that the board appears as a BOOTLOADER device and continue with step 3. If the board appears as KL25Z, go to step 6.

3. Download the Firmware Apps.zip archive from the PEmicro OpenSDA webpage (http://www.pemicro.com/opensda/). Validate the user email address to access the files.
4. Find the most recent MDS-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA and copy/drag-and-drop into the BOOTLOADER device.
5. Reboot the board by unplugging and replugging the connection to the OpenSDA port. Verify now that the device appears as a KL25Z device to continue.
6. Locate the most recent KL25Z firmware, which is distributed as part of the FlexGUI package.
   a. The FlexGUI download file is named in the form “flexgui2-fw-KL25Z_gd3162_public_vx.x.x.bin”.
   b. This .bin file is a product/family specific configuration file for FRDM-KL25Z containing the pin definitions, SPI/PWM generation code, and pin-mapping assignments necessary to interface with the translator board as part of RDGD3162MITEVM.
7. With the KL25Z still plugged through the OpenSDA port, copy/drag-and-drop the .bin file into the KL25Z device memory. Once done, disconnect the USB and it plug into the other USB port, labeled KL25Z.
   a. The device does not appear as a distinct device to the computer while connected through the KL25Z USB port, which is normal.
8. The FRDM-KL25Z board is now fully set up to work with RDGD3162MITEVM and the FlexGUI 2.
   a. There is no software stored or present on either the driver or translator boards, only on the FRDM-KL25Z MCU board.

All uploaded firmware is stored in nonvolatile memory until **Reset** is hit on the FRDM-KL25Z. There is no need to repeat this process during every power up, and there is no loss of data associated with a single unplug event.

5.3 Using FlexGUI 2 for GD3162

FlexGUI 2 is available from http://www.nxp.com/FlexGUI as an evaluation tool demonstrating GD3162-specific functionality, configuration, and fault reporting. FlexGUI 2 includes basic capacity for the RDGD3162MITEVM to control an IGBT or SiC module, enabling double-pulse and short-circuit testing.

SPI messages can be generated graphically or in hexadecimal format. See Figure 10 through Figure 26 for FlexGUI 2 for GD3162 internal register read and write access.

Starting FlexGUI 2 for GD3162

- FlexGUI install program (NXP_GD316x_GUI_public-1.8.x.msi)
- Download FlexGUI 2 for GD3162 and run the install program on a PC
- When the application starts, Figure 10 allows the user to select the target application board, feature set (standard or daisy chain), target MCU, and USB interface; leave all settings as shown
- Daisy-chain GD3162 (x3-2 channels) must be used for RDGD3162MITEVM board

Once the kit is selected, press **OK** and **Connect** FlexGUI 2 on the following GUI page. The proper USB COM port may need to be selected. Scan for COM ports with the micro-USB cable that must be attached from the PC and KL25Z port on the KL25Z MCU board.

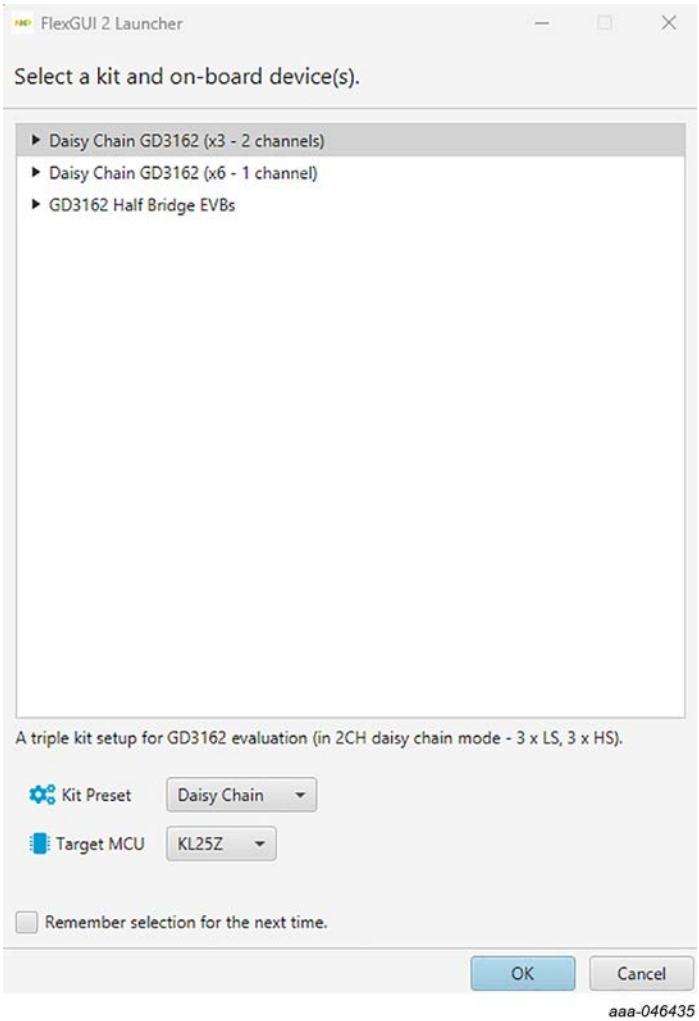


Figure 10. Kit selection

FlexGUI_2 connection

- Select FRDM-KL25Z COM port from the drop-down menu and select Connect to establish USB connection
  - If connection is not established, check USB cable connection between PC and KL25Z port and or scan again and select an alternate COM port for FRDM-KL25Z
  - If connection is not established, ensure that proper firmware is installed on FRDM-KL25Z MCU for FlexGUI 2 (refer to step 6 in Section 5.2)

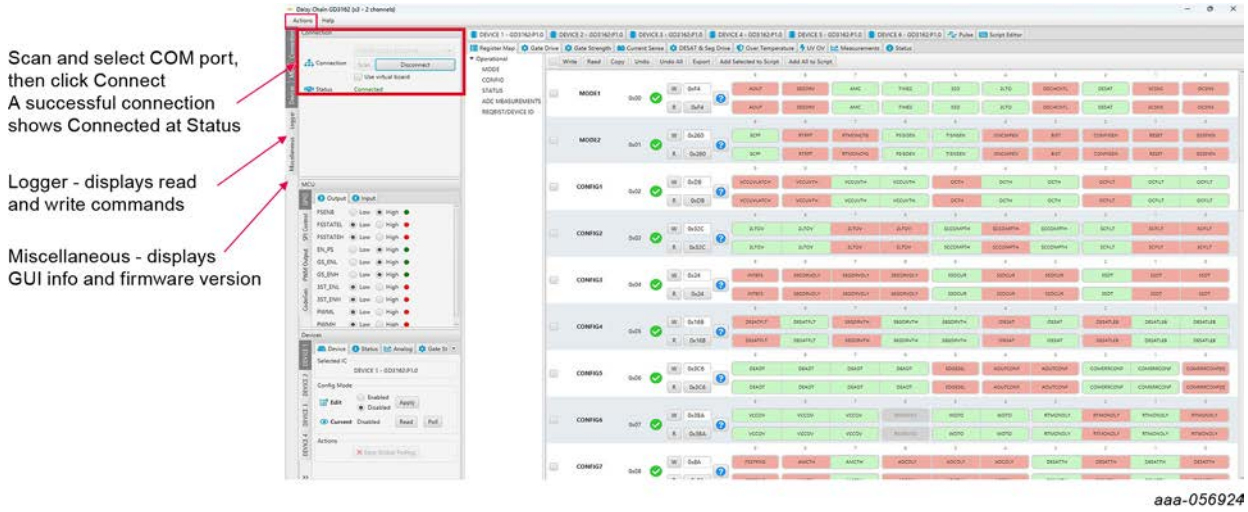
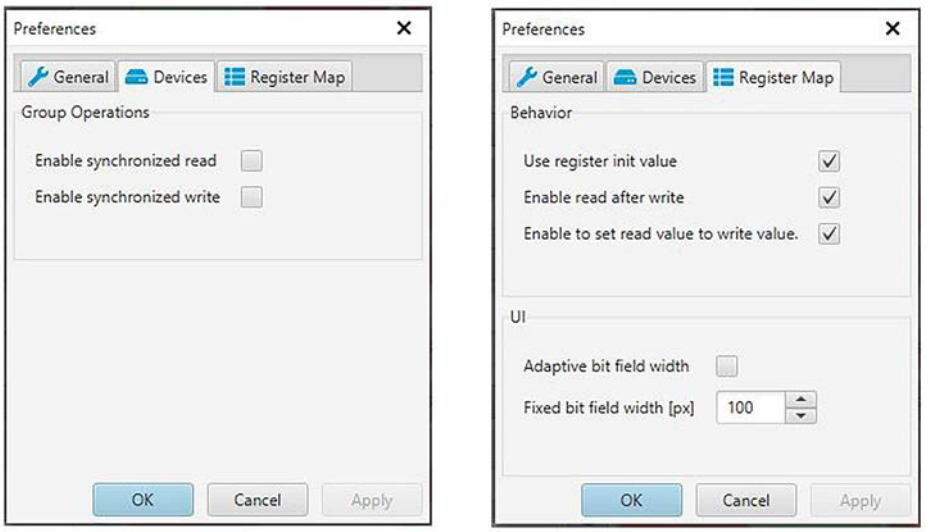


Figure 11. FlexGUI 2 connection

Set GUI actions and preferences

Access preferences from Actions menu at top left of GUI



Enable synchronized read and write to set both HS and LS devices simultaneously with same settings if desired

Enable Use register init value and Enable read after write and Enable to set read value to write value if desired (recommended)

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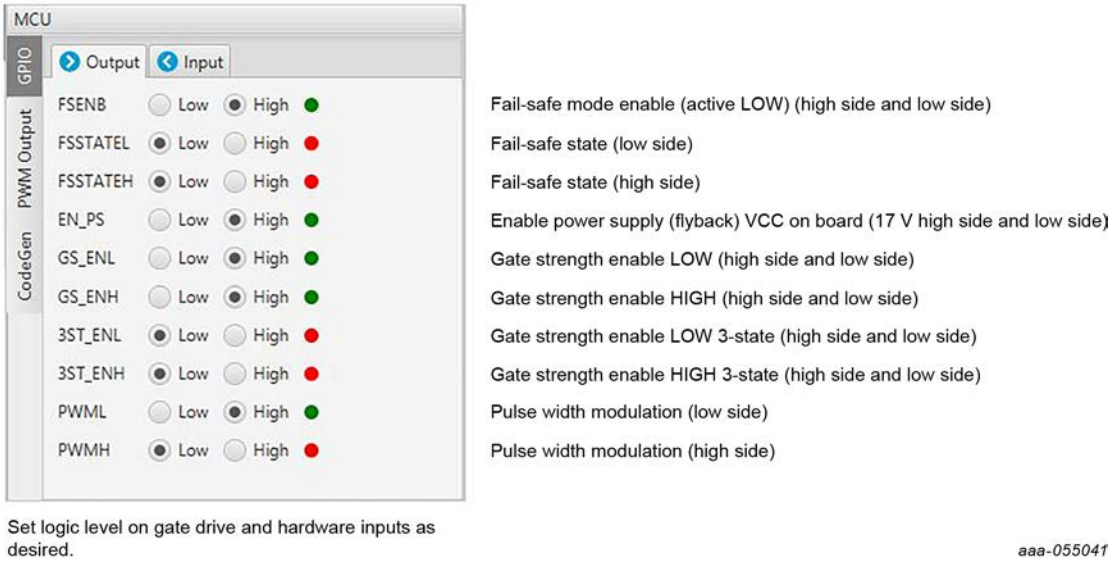
Figure 12. Actions and preferences settings



Set logic level on gate drive and hardware inputs as desired.

aaa-055041

Figure 13. MCU GPIO output control

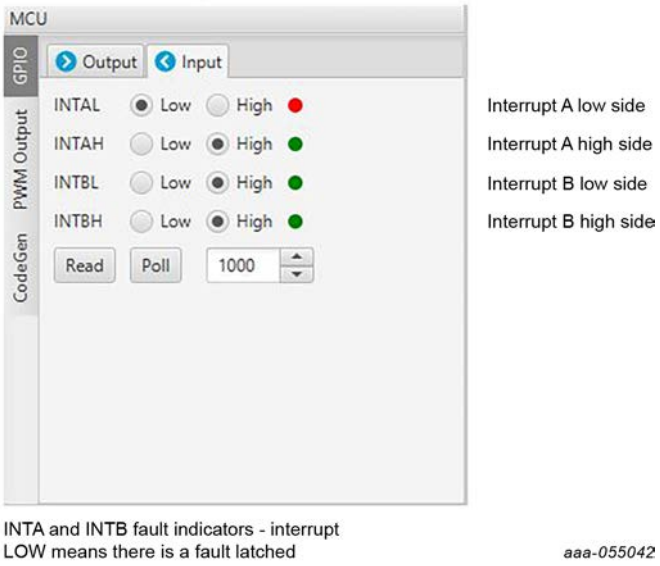


Figure 14. MCU GPIO input

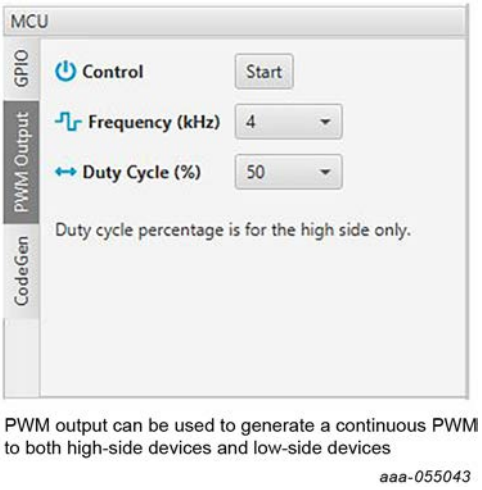


Figure 15. MCU PWM output

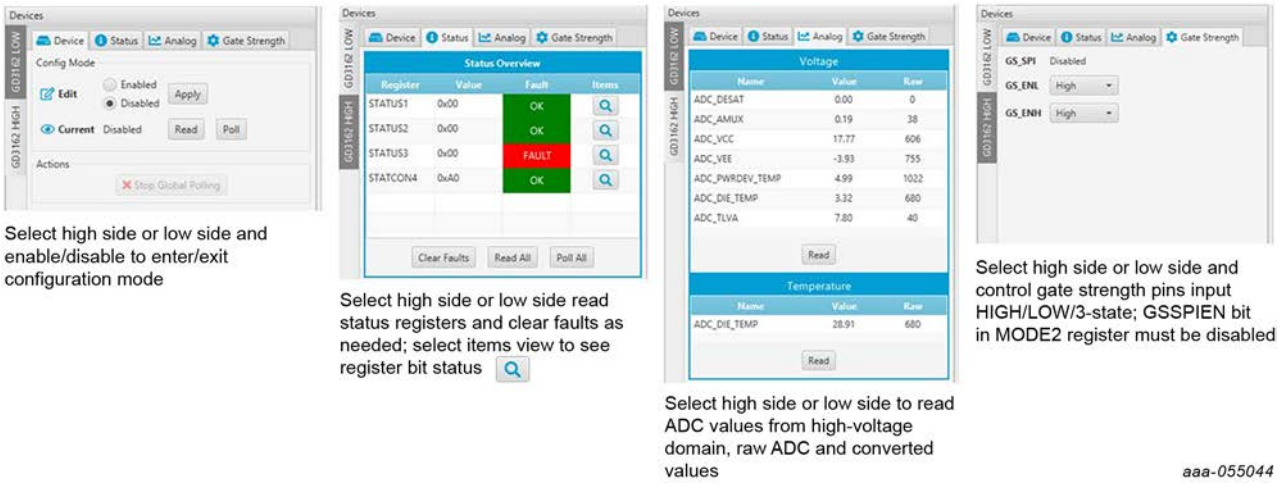


Figure 16. Devices

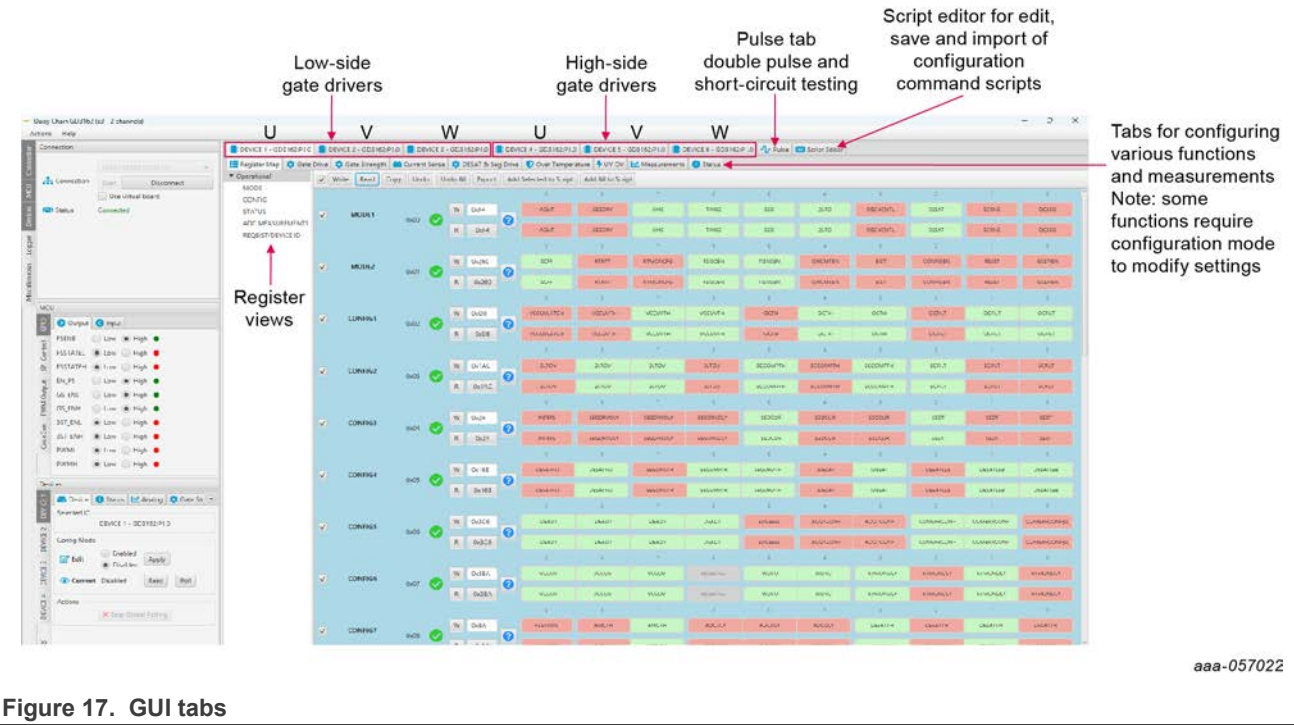


Figure 17. GUI tabs

- Registers are grouped according to function; independent lines to read and write the registers
- Individual registers can be read by clicking **R** and can be written by clicking **W**
- **Copy** to copy the read values to the write line; can be set to copy automatically
- Global register controls perform the selected command on all registers with the checkbox selected
- **Add to Script** adds current and selected register values to a script in the script editor window

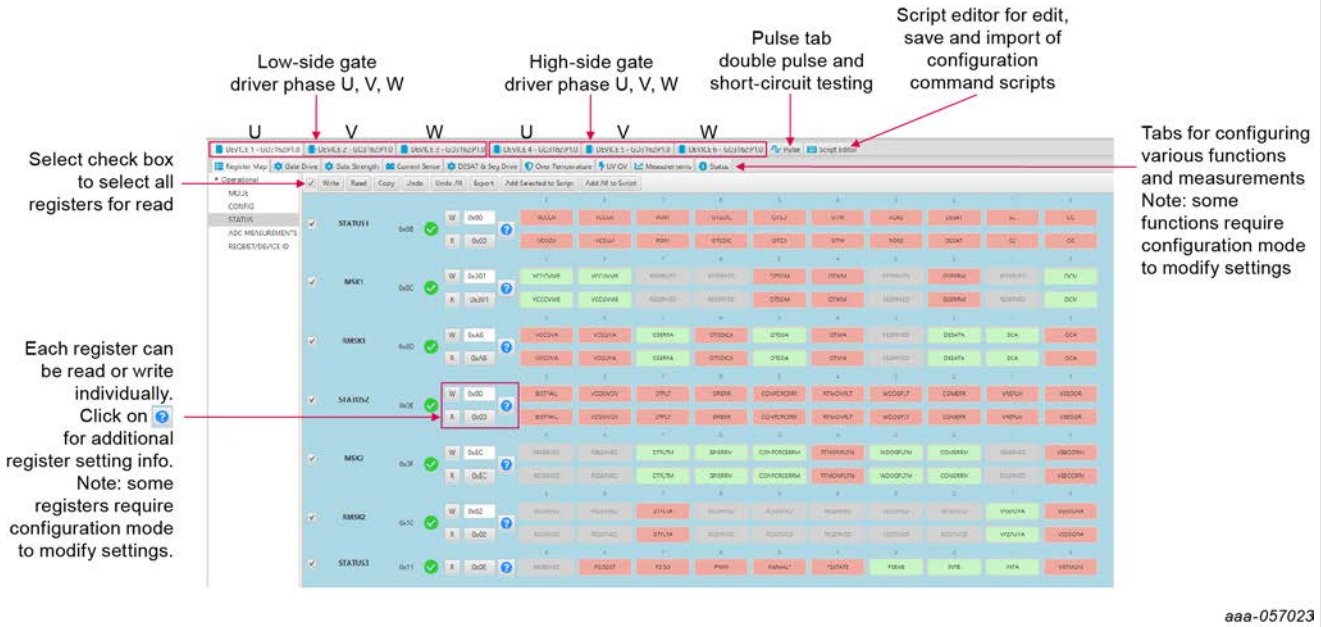


Figure 18. GUI tabs continued

Gate Drive tab

- Allows setting of parameters related to the gate drive; controls are disabled when not in config mode
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls

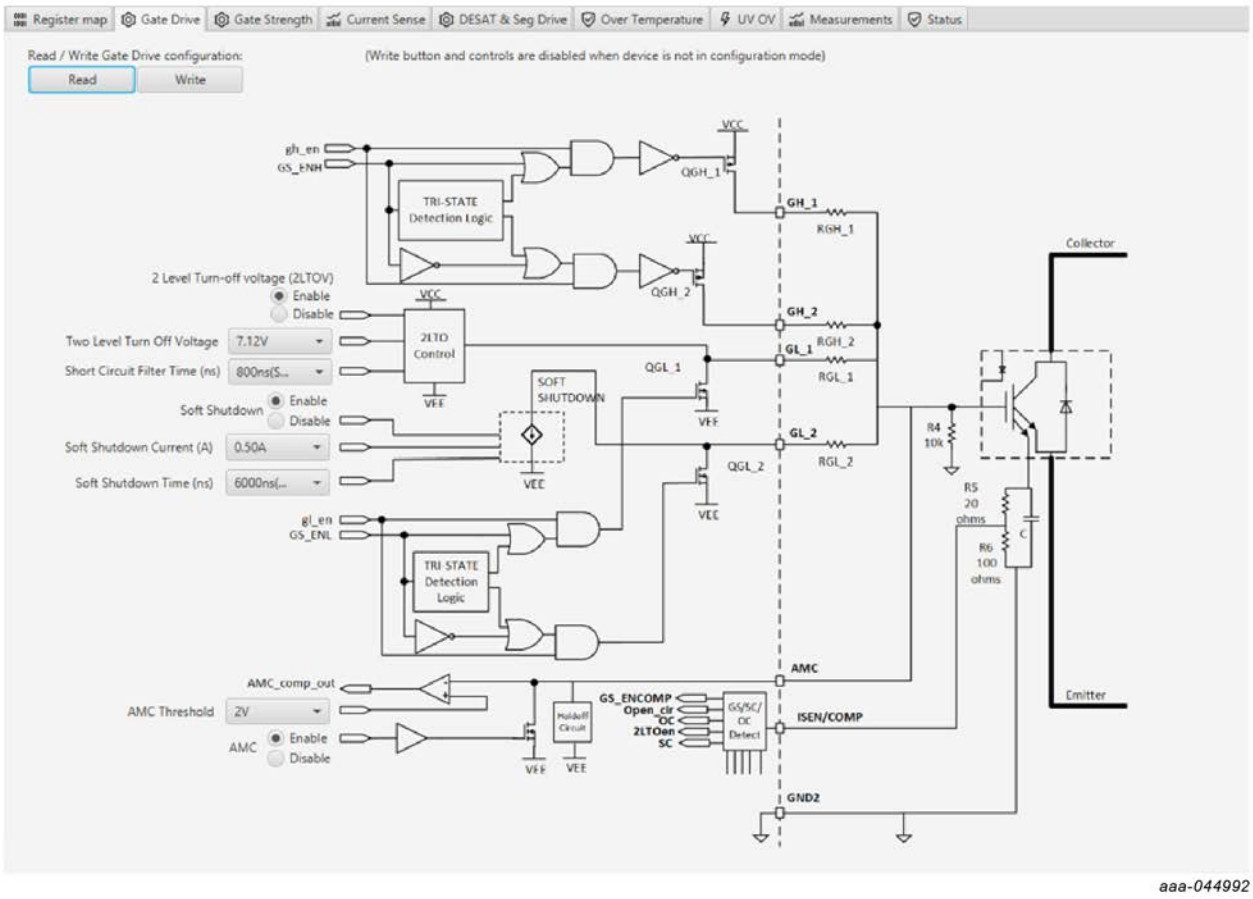


Figure 19. Gate Drive tab

Current Sense tab

- Allows setting of parameters related to current sense
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls

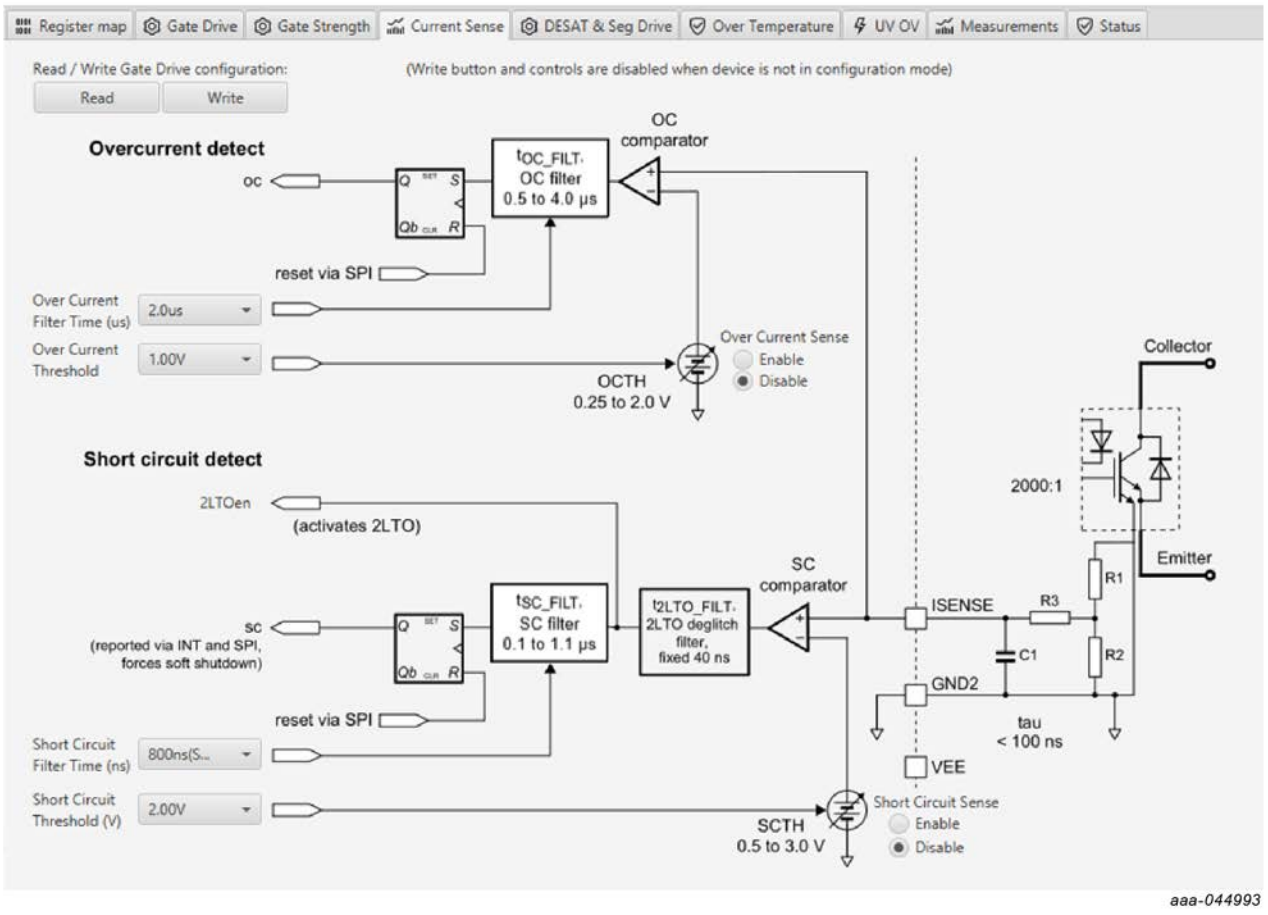


Figure 20. Current Sense tab

DESAT & Seg Drive tab

- Allows setting of parameters related to desat and segmented drive
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls

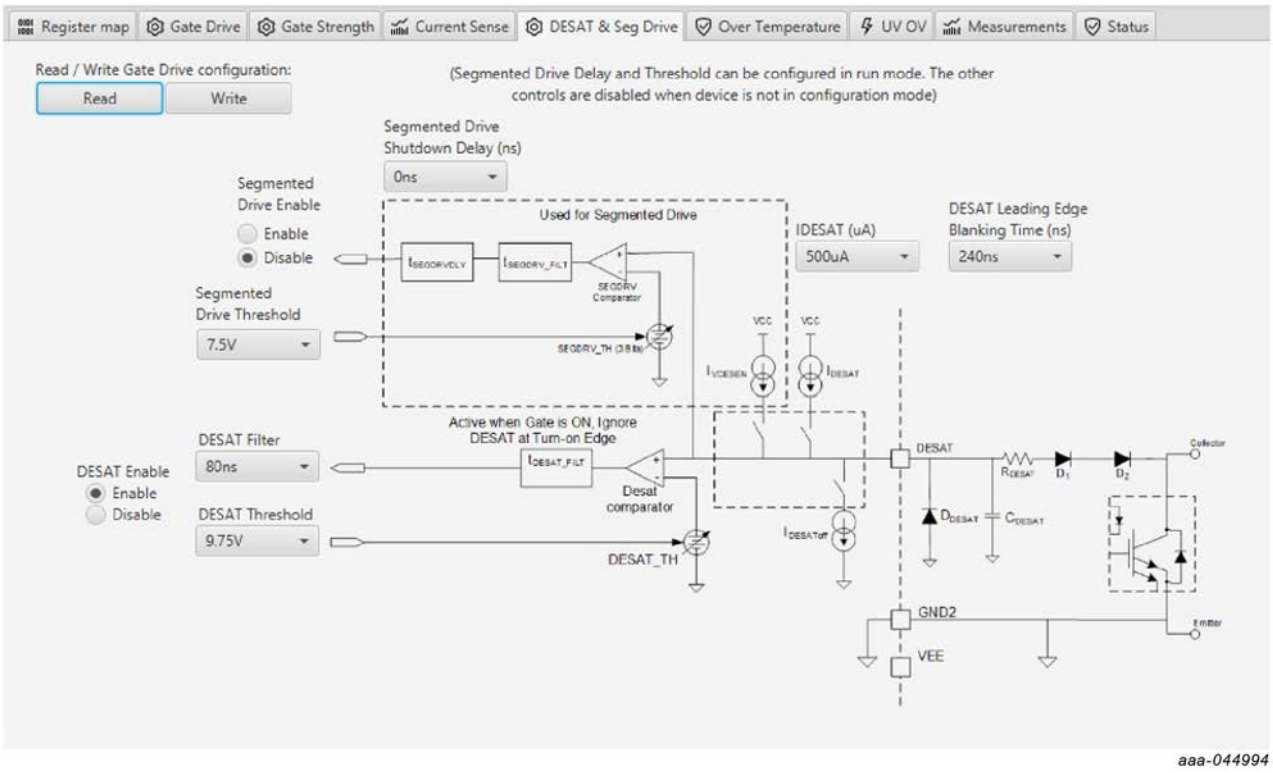


Figure 21. DESAT & Seg Drive tab

Over Temperature tab

- Allows setting of parameters related to overtemperature and overtemperature warning thresholds
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls

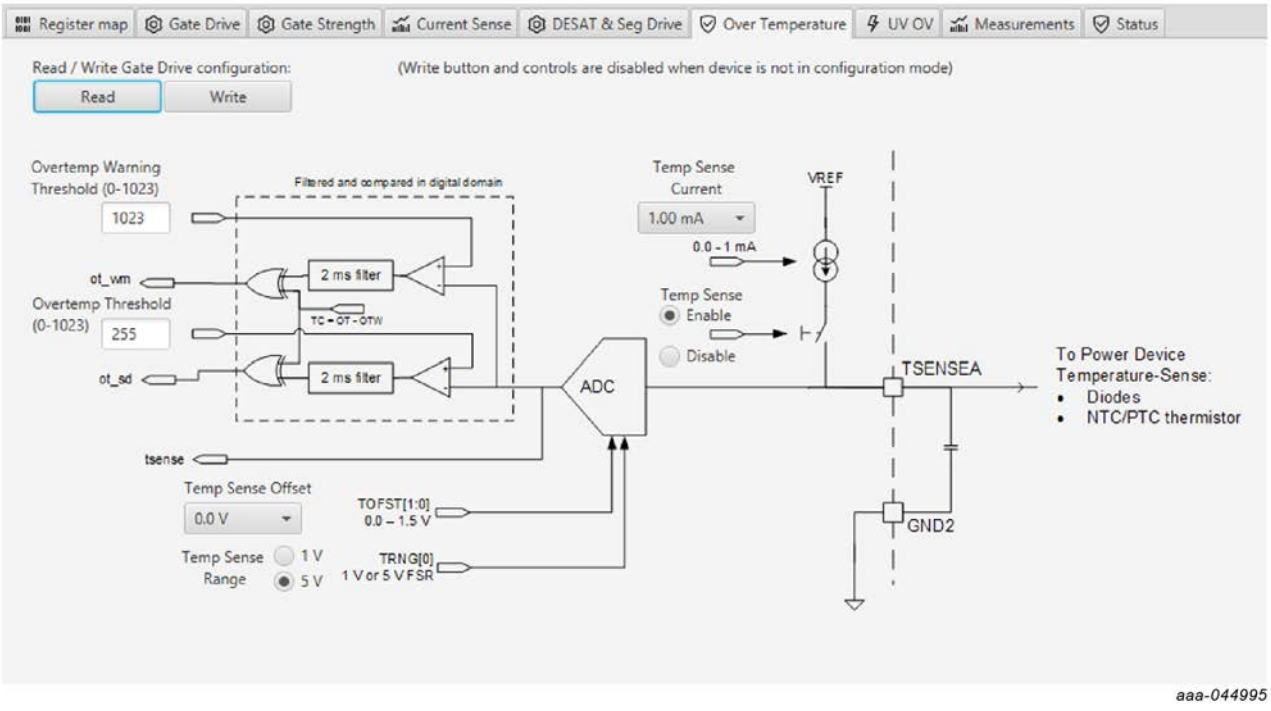


Figure 22. Over Temperature tab

Undervoltage and overvoltage threshold tab

- Allows setting of parameters related to undervoltage and overvoltage threshold
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls

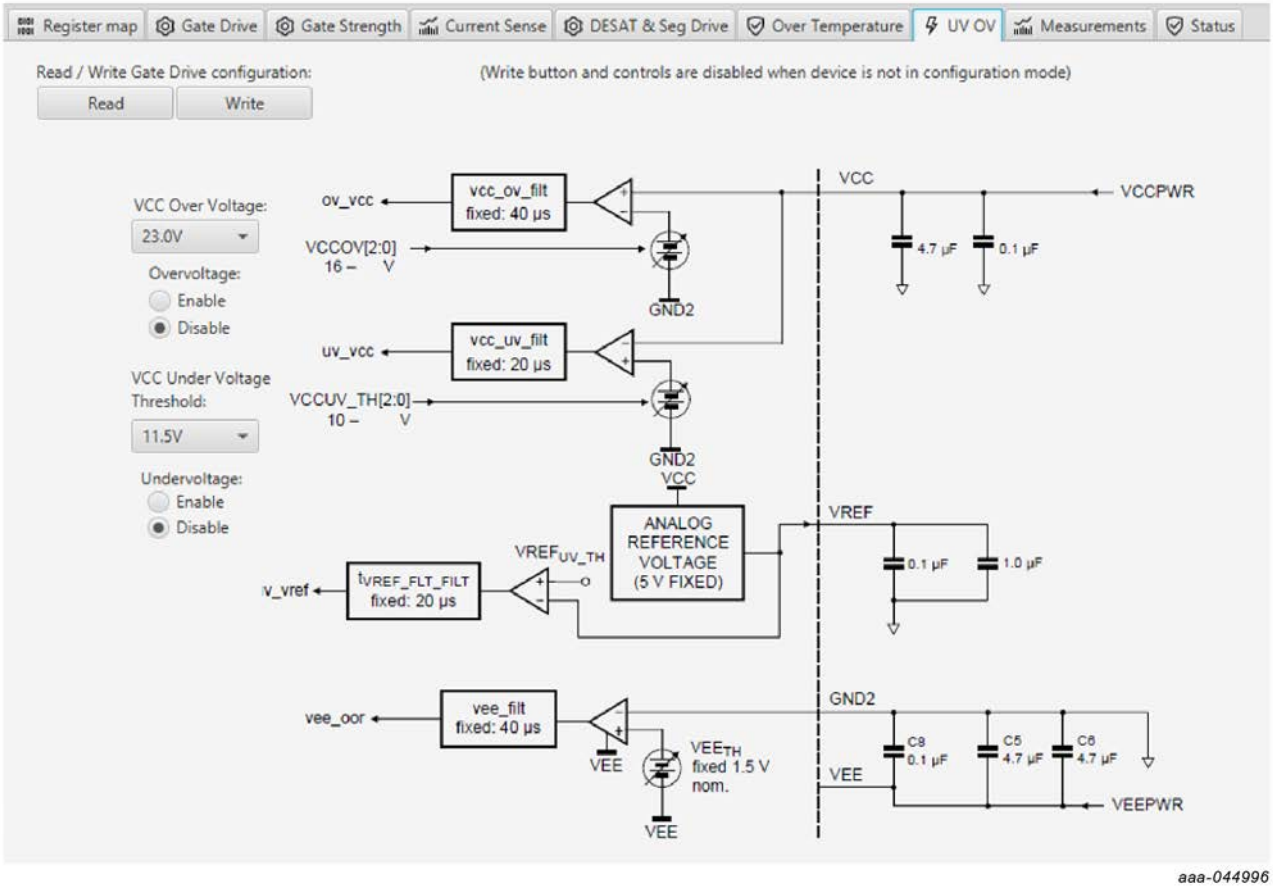


Figure 23. Undervoltage and overvoltage threshold tab

Measurements tab

- Allows monitoring and graphing of ADC and temperature values

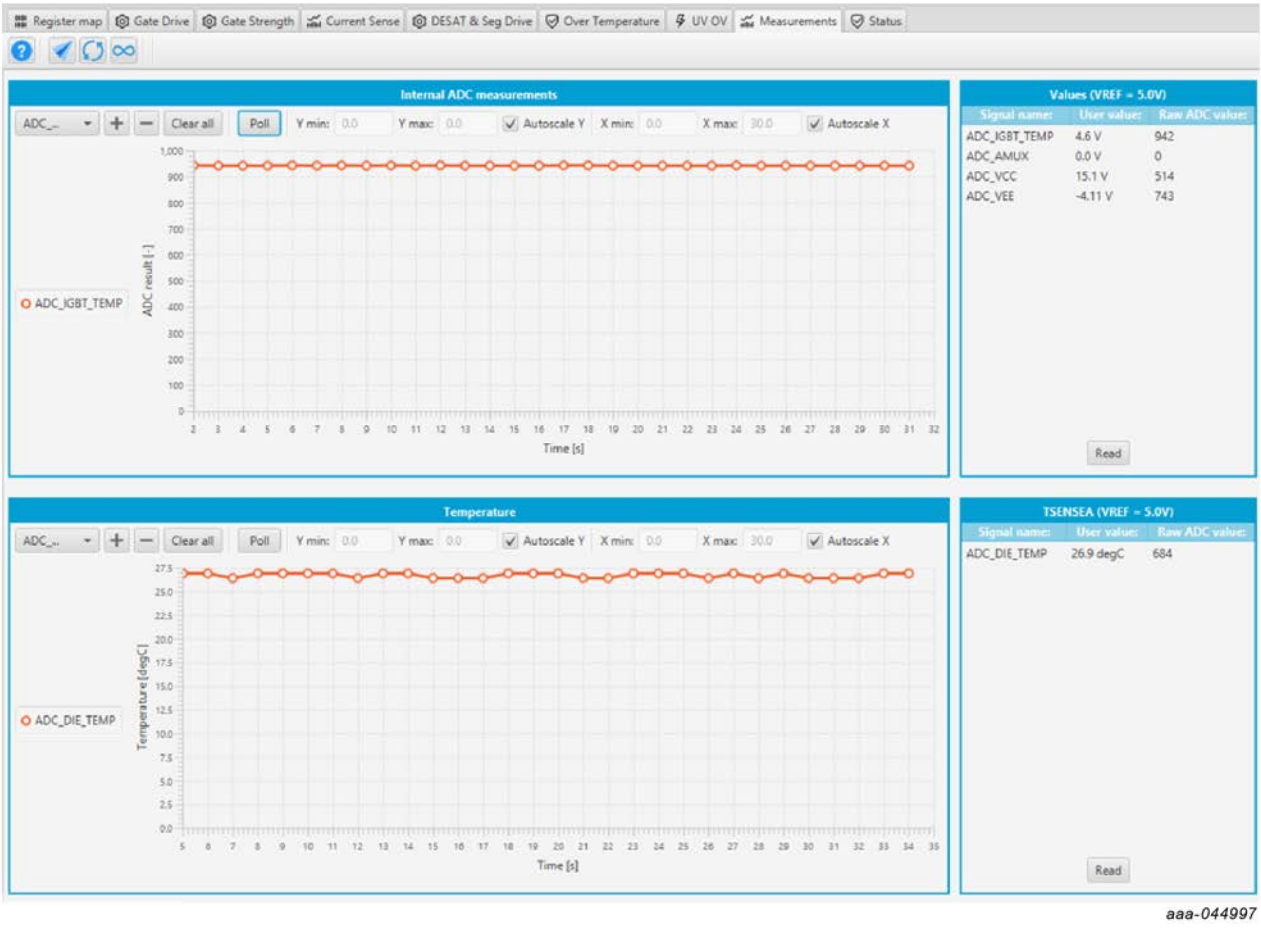


Figure 24. Measurements tab

Pulse tab

- Used for double pulse, short circuit, and PWM testing
- Select desired t1, t2, and t3 timings for each test type; select enable then generate pulses

Note: *Phase W can be used for double-pulse and short-circuit tests. To enable short-circuit testing, resistors on PWMALT signals must be removed to disable dead time control on gate drivers. PWMALT signals should also be tied to GND1 for short-circuit testing.*

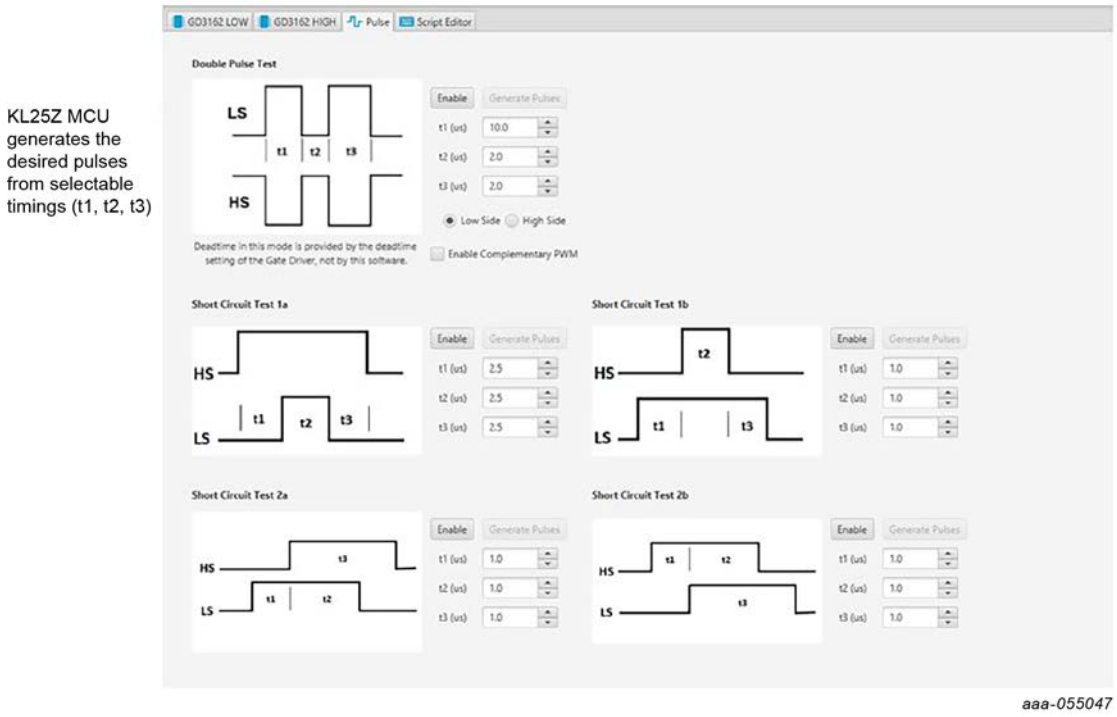


Figure 25. Pulse tab

Script Editor tab

- Scripts can be used for setting up configurations on all devices and saved for reuse

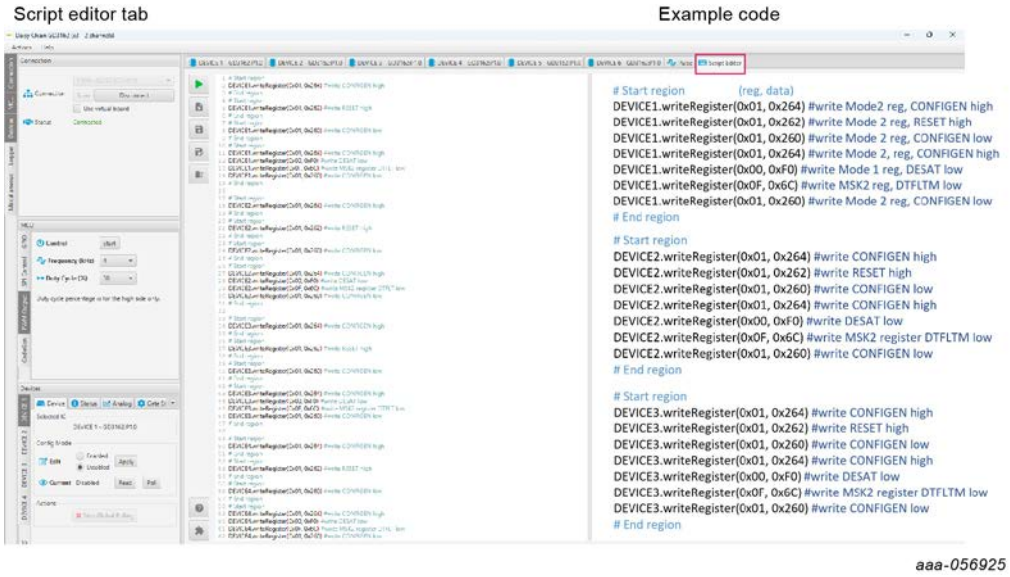


Figure 26. Script Editor tab

5.4 Troubleshooting

Some common issues and troubleshooting procedures are detailed below. This is not an exhaustive list by any means, and additional debug may be needed:

Problem	Evaluation	Explanation	Corrective action(s)
Unable to establish COM port connection	Check USB cable is connected to KL25Z port on FRDM-KL25Z MCU	If the USB cable is not connected to PC USB and KL25Z port GUI will not be able to establish USB connection	Plug in USB cable to PC USB port and FRDM-KL25Z KL25Z port
	Incorrect firmware installed on FRDM-KL25Z MCU	If the incorrect firmware is installed on the FRDM-KL25Z MCU board GUI will not be able to establish USB connection	Go to step 5 in this user guide for installing FlexGUI 2 on your computer to locate firmware file in GUI download package and copy to FRDM-KL25Z through OpenSDA port on MCU board.
	Check the COM port setting on FlexGUI 2. The drop-down menu will show the various COM ports available.	Selecting the incorrect COM port in the COM port drop-down menu will not be able to establish USB connection.	Select an alternative COM in the COM port drop-down menu on FlexGUI 2.
No PWM output (no fault reported)	Check PWM jumper position on translator board	Incorrect PWM jumpers obstruct signal path but not report fault	Set PWMH_SEL (J4) and PWML_SEL (J5) jumpers properly, for desired control method: • 3.3 V to 5.0 V translator board reviewed in Section 4.4
	Check PWM control signal	Ensure that proper PWM signal is reaching GD3162	Monitor PWML (TP11) and PWMH (TP10) on translator board for commanded PWM state. Check position of jumpers J4 and J5 on translator board.
	Check FSENB status (see GD3162 pin 15, STATUS3)	PWM is disabled when FSENB = LOW	Set pin FSENB = HIGH (pin 15) to continue
	Check CONFIG_EN bit (MODE2)	PWM is disabled when CONFIG_EN is logic 1	Write CONFIG_EN = logic 0 to continue

Problem	Evaluation	Explanation	Corrective action(s)
No PWM output (fault reported)	Check VGE fault (VGE_FLT)	A short on IGBT or SiC module gate, or too low of VGEMON delay setting causes VGE fault, locking out PWM control of the gate.	Clear VGE_FLT bit (STATUS2) to continue. Increase VGEMON delay setting (CONFIG6). If safe operating condition can be guaranteed, set VGE_FLTM (MSK2) bit to logic 0, to mask fault.
	Check for short-circuit fault (SC) in STATUS1 register	SC is a severe fault that disables PWM. SC fault cannot be masked	Clear SC fault to continue. Consider adjusting SC fault settings on GD3162: • Adjust short-circuit threshold setting (CONFIG2) • Adjust short-circuit filter setting (CONFIG2)
PWM output is good, but with persistent fault reported	Check for dead time fault (DTFLT) in STATUS2 register	Dead time is enforced, but fault indicates that PWM controls signals are in violation	Clear DTFLT fault bit (STATUS2). Check PWMHSEL (J10) and PWMLSEL (J14) are configured to bypass dead time faults. Consider adjusting dead time settings on GD3162: • Change mandatory PWM dead time setting (CONFIG5) • Mask dead time fault (MSK2)
	Check for overcurrent (OC) fault in STATUS1 register	OC fault latches, but does not disable PWM. OC fault cannot be masked.	Clear OC fault bit (STATUS1). Adjust OC fault detection settings on GD3162: • Adjust overcurrent threshold setting (CONFIG1) • Adjust overcurrent filter setting (CONFIG1)
PWM or FSSTATE rising edge has longer delay than falling edge	Check translator output voltage versus GD3162 VDD voltage	Low translator output voltage (compared with correct VDD at GD3162) causes the high threshold at the GD3162 pin to be crossed later than commanded	Check translator output voltage selection (J3) is configured to the same level as the GD3162 VDD Check VCCSEL supply or translator outputs on the translator board for excessive loading or supply droop/pulldown
WDOG_FLT reported on startup	Check VSUP and VCC are powered	On initialization, watchdog fault is reported when one die is powered up before the other	Check VSUP and VCC both have power applied. Clear WDOG_FLT bit (STATUS2) to continue.
SPIERR reported on startup	Check KL25Z/translator connection	On initialization, SPIERR can occur when the SPI bus is open, or when GD3162 IC is powered up before the translator (which provides CSB).	Clear SPIERR fault to continue. Reinitialize power to GD3162 after translator is powered (over USB).
SPIERR reported after SPI message	Check bit length of message sent	There is SPIERR if SCLK does not see a n*24 multiple of cycles	Use 24-bit message length for SPI messages
	Check CRC	SPIERR faults if CRC provided in sent message is not good	Use FlexGUI to generate commands with valid CRC. The command can be copied in binary or hexadecimal and sent from another program.
	Check for sufficient dead time between SPI messages	SPIERR fault bit is set when the time between SPI messages (txfer_delay) received is too short. Minimum required delay time is 19 µs.	Check time between CSB rising edge (old message end) and CSB falling edge (new message start) during normal SPI read, and ensure transfer delay dead time check. SPIERR can also be cleared in BIST.
VCCREGUV reported on startup	Check VCCREG potential	Caused by low VCC	Clear VCCREGUV fault bit (STATUS1). Tune VCC-GNDISO potential with power supply set resistor (R51).

Problem	Evaluation	Explanation	Corrective action(s)
VREFUV reported on startup	Check HV domain is powered correctly	Related to slow rise time of VCC supply on HV domain, or failed VREF regulator	Clear VREFUV bit (STATUS2). Reset HV domain supply if fault bit does not clear.
	Check VCC for undervoltage condition	Low VCC is visible indirectly through other HV domain faults	Check onboard the flyback power supply circuit. VCC-GNDISO set to ~19 V.
VCCOV fault reported on startup	Check VEE level on suspect domain.	If VEE level is not at desired negative voltage it could cause excessive VCC level.	Check Zener diode in power supply circuit for proper value in setting VEE level. Clear VCCOV bit (STATUS1) to continue.
	Check VCC-GNDISO potential	PWM is disabled during a VCC overvoltage (23 V nom.)	VCC-GNDISO potential level should be ~19 V. Clear VCCOV bit (STATUS1) to continue.
No PWM during short circuit test	Check PWMxSEL jumpers	Incorrect configuration of PWMALT pins prevent short-circuit test by enforcing dead time	PWMALT resistors must be unpopulated to disable dead time control for short circuit testing. See Pulse tab in Section 5.3.
Bad SPI data, appears to repeat previous response	Check VSUP/VDD for undervoltage condition	VDD_UV latches SPI buffer contents, preventing updated fault reporting.	Check voltage provided at VDD pin (pin 3). On each read, compare the address from the sent command and response (a difference indicates that the SPI response is latched due to inactive). Read multiple addresses to ensure a good comparison.
	Check EN_PS is set to HIGH in FlexGUI 2; see Figure 13	VCC/VEE can be enabled/disabled in software.	EN_PS in GPIO output tab on FlexGUI 2; see Section 5.3
	Check VCC for undervoltage	Unpowered VCC prevents HV domain from updating data	Tune VCC-GNDISO using R51 feedback

6 Configuring the hardware

The RDGD3162MITEVM with the KITGD316xTREVM attached is shown in Figure 27 using Windows-based PC and FlexGUI 2 for GD3162 software.

Note: *Double-pulse and short-circuit testing can be conducted on phase W only. See Section 5.3.*

Suggested equipment needed for test:

- Rogowski coil high-current probe
- High-voltage differential voltage probes
- High sample rate digital oscilloscope with probes
- DC-link capacitor compatible with Mitsubishi CTF700CJ3D130 power module.
- Mitsubishi CTF700CJ3D130 SiC power module
- Windows-based PC
- High-voltage DC power supply for DC link voltage
- Low-voltage 12 V DC power supply for VPWR
- Voltmeter for monitoring high-voltage DC-link supply
- Load coil for double-pulse testing (phase W only)

Note: *To enable short-circuit testing on phase W only, two resistors must be removed from PWMALT phase U signals to disable dead-time control on phase W gate drivers.*

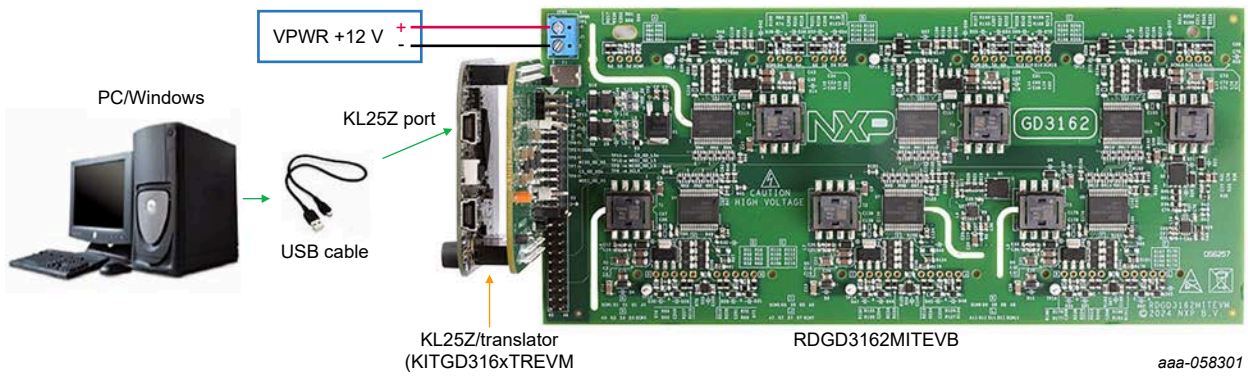


Figure 27. Evaluation setup using KITGD316xTREVM and FlexGUI 2

7 Schematic, board layout, and bill of materials

The schematic, board layout, and bill of materials for the RDGD3162MITEVM reference design are available at http://www.nxp.com/RDGD3162MITEVM.

8 References

1. RDGD3162MITEVM detailed information on this board, including documentation, downloads, and software and tools http://www.nxp.com/RDGD3162MITEVM
2. GD3162 product information on advanced single-channel gate driver for IGBT/SiC http://www.nxp.com/GD3162
3. MPC5777C ultra-reliable MCU for automotive and industrial engine management http://www.nxp.com/MPC5777C
4. MPC5744P ultra-reliable MCU for automotive and industrial safety applications http://www.nxp.com/MPC574xP
5. MPC5775B/E-EVB low-cost development board for battery management and inverter http://www.nxp.com/MPC5775B-E-EVB

9 Revision history

Table 5. Revision history

Document ID	Release date	Description
UM12208 v.1.0	15 January 2025	Initial version

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