UM11900

Hardware user manual for KIT-PC2TPLEVB

Rev. 1 — 20 April 2023 User manual

Document information

Information	Content
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Abstract	User manual for KIT-PC2TPLEVB.

Revision history

Rev	Date	Description
v.1	20230420	Initial version

1 Important notice

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2 Introduction

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal, and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

3 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for the KIT-PC2TPLEVB evaluation board is at http://www.nxp.com/KITPC2TPLEVB. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a Getting Started tab. The Getting Started tab provides quick-reference information applicable to using the KIT-PC2TPLEVB evaluation board, including the downloadable assets referenced in this document.

4 Getting ready

The purpose of the KIT-PC2TPLEVB is to interface NXP PC software (that is, Device Evaluation GUI) to TPL attached NXP devices (that is, MC33775A).

This document guides the user through the process of using the KIT-PC2TPLEVB.

4.1 Kit contents

The KIT-PC2TPLEVB kit includes:

- KIT-PC2TPLEVB - personal computer (PC) to electrical transport protocol link (ETPL) gateway board
- TTL-232R-5V - USB to RS232 cable (1.8 m)
- ETPL cable - two-wire twisted pair TPL cable (50 cm)
- Quick start guide

5 Getting to know the hardware

5.1 Kit overview

Figure 1 an overview of the KIT-PC2TPLEVB.

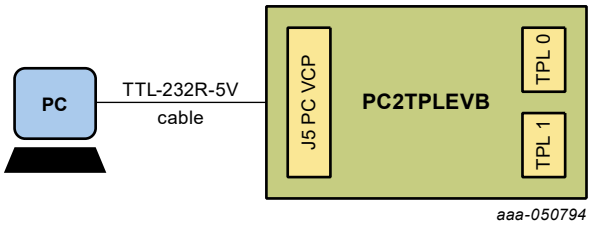

Figure 1. KIT-PC2TPLEVB overview

5.2 Board features

The main features of the KIT-PC2TPLEVB are:

- Direct control from a PC via USB connection (VCP)
- VCP communication speed 2 MBd
- Supply of the KIT-PC2TPLEVB from USB
- Two galvanically isolated ETPL ports
- Supports TPL3 and TPL2 protocol versions
- Four status LEDs

The KIT-PC2TPLEVB serves as a hardware tool supporting evaluation of ETPL devices with software running on a PC. This board can be directly connected to a USB port of a PC and interfaced via a virtual COM port (VCP).

Figure 2. KIT-PC2TPLEVB overview

5.3 Block diagram

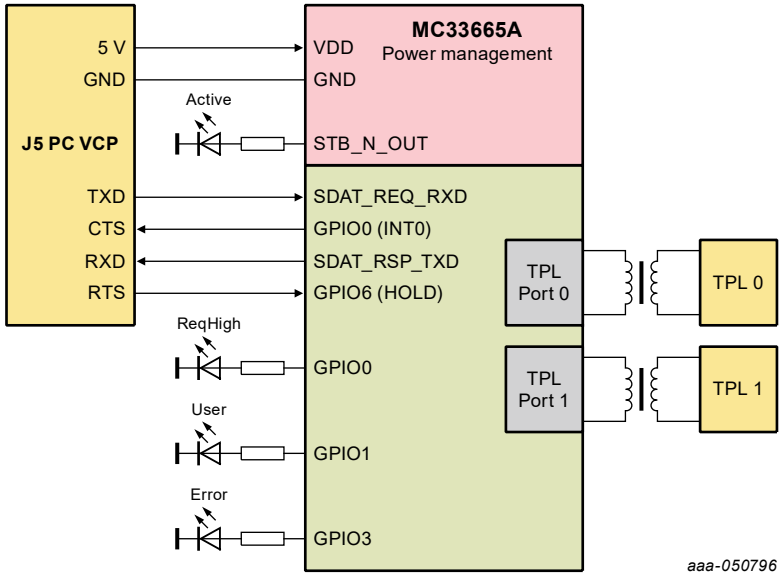

Figure 3. KIT-PC2TPLEVB block diagram

5.4 Kit featured components

The KIT-PC2TPLEVB allows the user to interface ETPL chains/devices with software running on a PC.

The kit includes a UART-to-USB translator cable (TTL-232R-5V) and an ETPL cable. The UART-to-USB translator cable interfaces with the UART-based MC33665A gateway and provides the 5 V supply. The two ETPL ports allow connection to NXP evaluation boards or customer boards having the NXP ETPL interface.

The KIT-PC2TPLEVB has the following LEDs to indicate information to the user. The D13 indicates the operating mode (active) of the MC33665A. The D14, D15, and D16 LEDs are connected to GPIOs of the MC33665A and depend on the configuration of the MC33665A device. The default use is listed in Table 1.

Table 1. Status LEDs

LED	Description	MC33665A signal
D13 - green	Active: Indicates the MC33665A operating state	STB_OUT_N
D16 - orange	ReqHigh (default use): Indicates Request Queue High status	GPIO0
D15 - orange	User (default use): optional for User purpose	GPIO1
D14 - red	Error (default use): optional indicating error status	GPIO3

5.4.1 Connectors

The KIT-PC2TPLEVB has one connector to interface to a PC and two TPL ports.

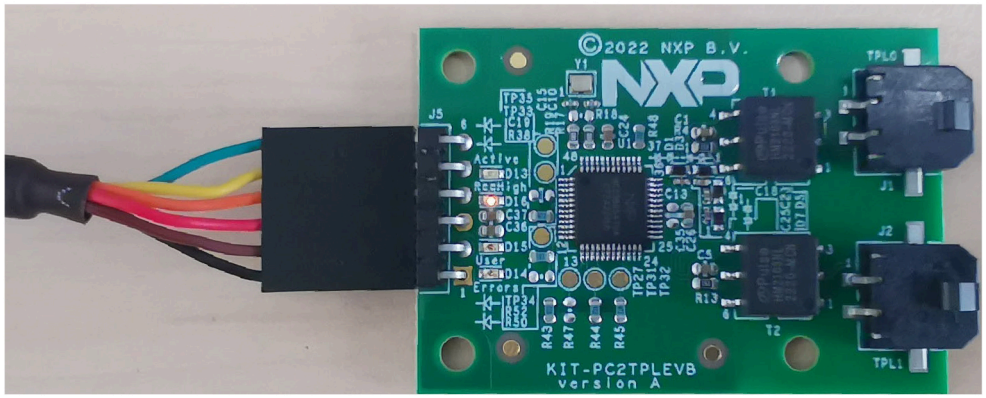

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Figure 4. KIT-PC2TPLEVB connectors

Connector J5 connects the KIT-PC2TPLEVB to the UART-to-USB translator cable. Pin 1 of the TTL-232R-5V (black wire) must be connected to the J5 Pin 1 as shown in Figure 4.

Table 2. Interface - J5

Pin number	Connection	Description
1	GND	Ground
2	ReqHigh	Request Queue High output (connect to PC UART CTS input)
3	VDD5V	5 V supply input
4	ReqData	Request Data input (connect to PC UART TXD output)
5	RspData	Response Data output (connect to PC UART RXD input)
6	Hold	Hold input (optional connect to PC UART RTS output)

Connectors J1 and J2 connects to the KIT-PC2TPLEVB TPL ports 0 and 1.

Table 3. TPL port 0 - J1

Pin number	Connection	Description
1	TPL0_P	TPL port 0 (positive)
2	TPL0_N	TPL port 0 (negative)

Table 4. TPL port 1 - J2

Pin number	Connection	Description
1	TPL1_P	TPL port 1 (positive)
2	TPL1_N	TPL port 1 (negative)

5.5 Schematic, board layout, and bill of materials

The schematic, board layout and bill of materials for the KIT-PC2TPLEVB evaluation board are available at http://www.nxp.com/KITPC2TPLEVB.

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