UM10607

BGA7350 performance at IF=230 MHz

Rev. 1 — 14 November 2012 **User manual**

Document information

Info	Content
Keywords	Dual VGA. 28 dB attenuator range IF=230 MHz NXP
Abstract	This User Manual describes the functionality and performance of the single ended BGA7350 evaluation board, tuned for a IF of 230 MHz

Revision history

Rev	Date	Description
1	20121114	First publication

Contact information

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1. Introduction

The BGA7350 is a Silicon MMIC (Monolithic Microwave Integrated Circuit) processed in NXP's mainstream Si QuBIC4+ BiCmos process. This process intrinsic inhibits high F_T figures (up to 28 GHz), while not compromising ruggedness (breakdown voltage) and noise figures. These characteristics make this device suitable for versatile IF applications like in Base station receive path. The BGA7350 exhibits a logic-level shutdown control to reduce supply current. The BGA7350 is packed in the leadless HVQFN (5 x 5 mm^2), and in combination with the optimized die design, gives excellent thermal performance,

To ensure optimal ESD protections, all pins are ESD protected.

All above mentioned highlight makes the BGA7350 and extreme attractive device with optimal performance/cost ratio, as compared to other devices in the market.

The single ended 230 MHz evaluation board (EVB) is designed for optimal performance in the 230 MHz frequency ranges, with a bandwidth of 28 MHz, suitable for base station Rx applications, as shown in Fig. 1.

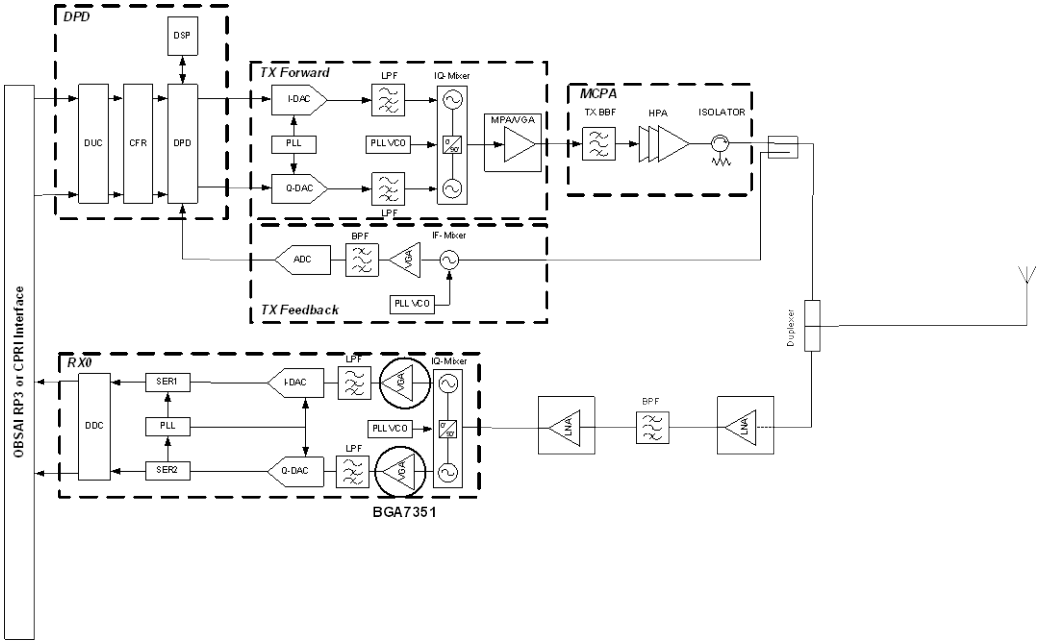


Fig 1. Generic Base station architecture

2. Product Profile

2.1 General description

The BGA7350 MMIC is a dual independently digitally controlled IF Variable Gain Amplifier (VGA) operating from 50 MHz to 250 MHz Each IF VGA amplifies with a gain range of 24 dB and at its maximum gain setting delivers 17 dBm output power at 1 dB gain compression and a superior linear performance.

The BGA7350 Dual IF VGA is optimized for a differential gain error of less than ±0.1 dB for accurate gain control and has a total integrated gain error of less than ±0.3 dB.

The gain controls of each amplifier are separate digital gain-control word, which is provided externally through two sets of 5 bits.

The BGA7350 is housed in a 32 pins 5 × 5 mm2 leadless HVQFN package.

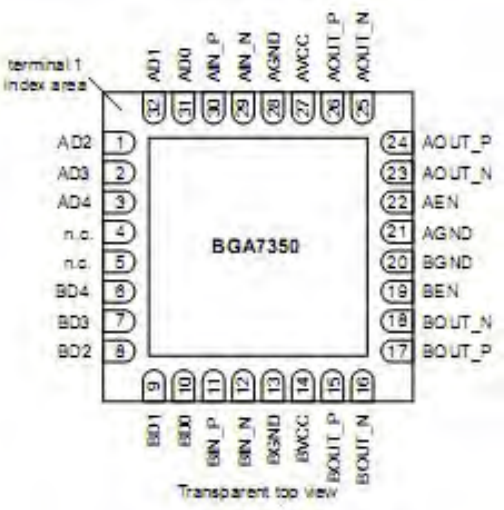
2.2 Features and benefits

- Dual independent digitally controlled 28 dB gain range VGAs, with 5-bit control interface
- 50 MHz to 250 MHz frequency operating range
- Gain step size: 1 dB ± 0.1 dB
- 18.5 dB small signal gain
- Fast gain stage switching capability
- 17 dBm output power at 1 dB gain compression
- 5 V single supply operation with power-down control
- Logic-level shutdown control pin reduces supply current
- Excellent ESD protection at all pins
- Moisture sensitivity level 2
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)
- Unconditionally stable
- Excellent differential and integrated gain error

2.3 Applications

- Compatible with GSM / W-CDMA carrier/ WiMAX / LTE base-station infrastructure / multi systems carrier
- Multi channel receivers
- General use for DAC driver applications

3. Pinning information



Transparent top view

Fig 2. SOT617-1 Pin configuration

3.1 Pin description

Table 2. Pin description

Symbol	Pin	Description
AD2	1	MSB – 2 for gain control interface of channel A
AD3	2	MSB – 1 for gain control interface of channel A
AD4	3	MSB for gain control interface of channel A
n.c.	4	not connected [1]
n.c.	5	not connected [1]
BD4	6	MSB for gain control interface of channel B
BD3	7	MSB – 1 for gain control interface of channel B
BD2	8	MSB – 2 for gain control interface of channel B
BD1	9	LSB + 1 for gain control interface of channel B
BD0	10	LSB for gain control interface of channel B
BIN_P	11	channel B positive input [2]
BIN_N	12	channel B negative input [2]
GNDB	13, 20	ground for channel B
V_{CCB}	14	supply voltage for channel B [3]
BOUT_P	15, 17	channel B positive output [2]
BOUT_N	16, 18	channel B negative output [2]
BEN	19	power enable pin for channel B
GNDA	21, 28	ground for channel A
AEN	22	power enable pin for channel A
AOUT_N	23, 25	channel A negative output [2]
AOUT_P	24, 26	channel A positive output [2]
V_{CCA}	27	supply voltage for channel A [3]
AIN_N	29	channel A negative input [2]
AIN_P	30	channel A positive input [2]
AD0	31	LSB for gain control interface of channel A
AD1	32	LSB + 1 for gain control interface of channel A
GND	GND paddle	RF ground and DC ground [4]

[1] Pin to be left open.

[2] Each channel should be independently enabled with logic HIGH and disabled with logic LOW.

[3] RF decoupled.

[4] The center metal base of the SOT617-1 also functions as heatsink for the VGA.

4. Functional Diagram

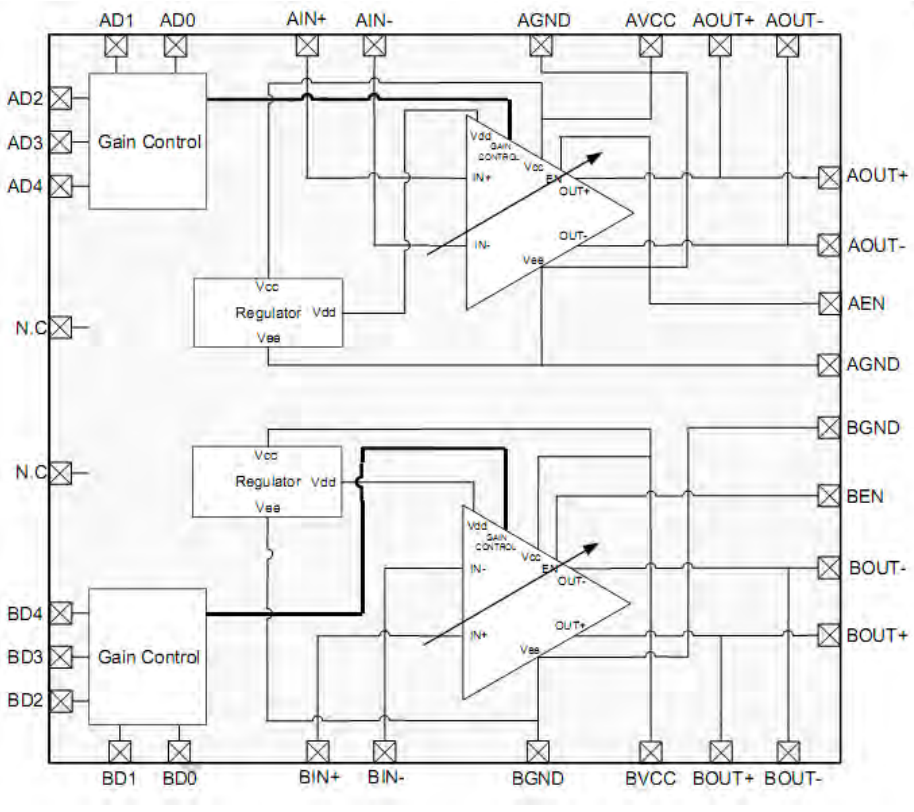


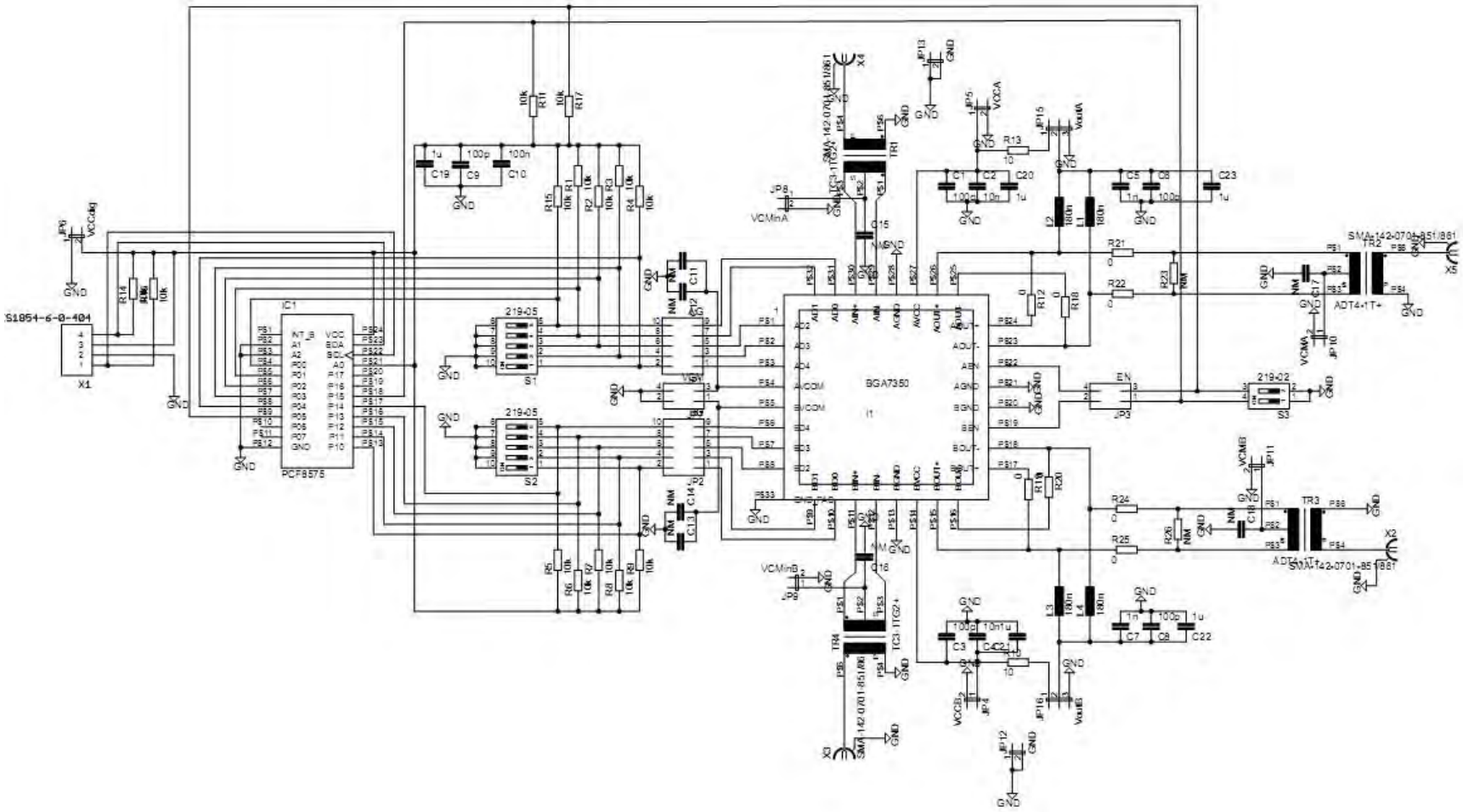
Fig 3. Functional diagram

5. Gain control Range

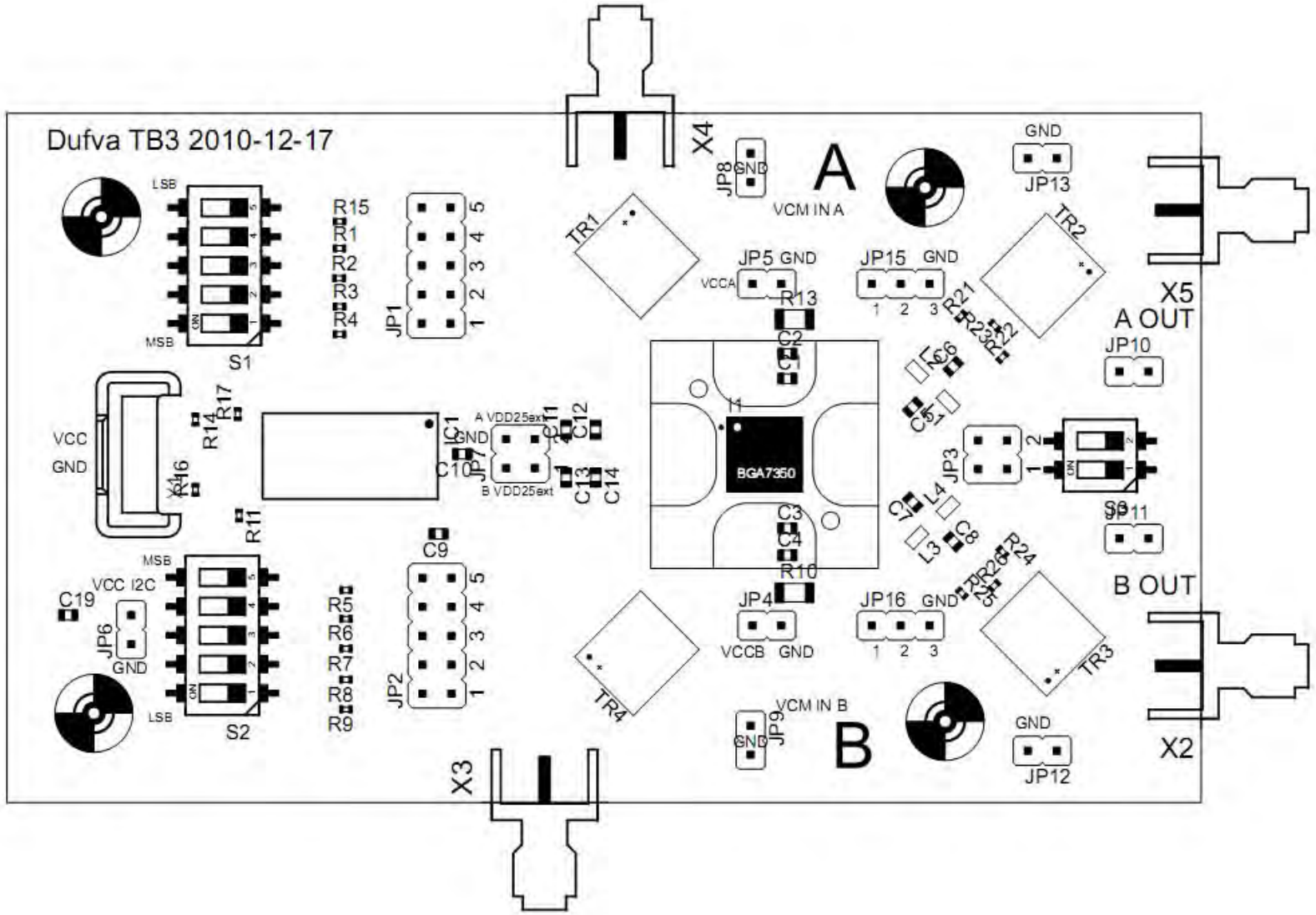
Input to all 0 to 4 gain control pins	nominal power gain [dB]
00000	22
00001	21
00010	20
00011	19
00100	18
00101	17
00110	16
00111	15
01000	14
01001	13
01010	12
01011	11
01100	10
01101	9
01110	8
01111	7
10000	6
10001	5
10010	4
10011	3
10100	2
10101	1
10110	0
10111	−1
11000	−2
11001	−3
11010	−4
11011	−5
11100	−6
> 11100	-6

Table 3 Gain control range

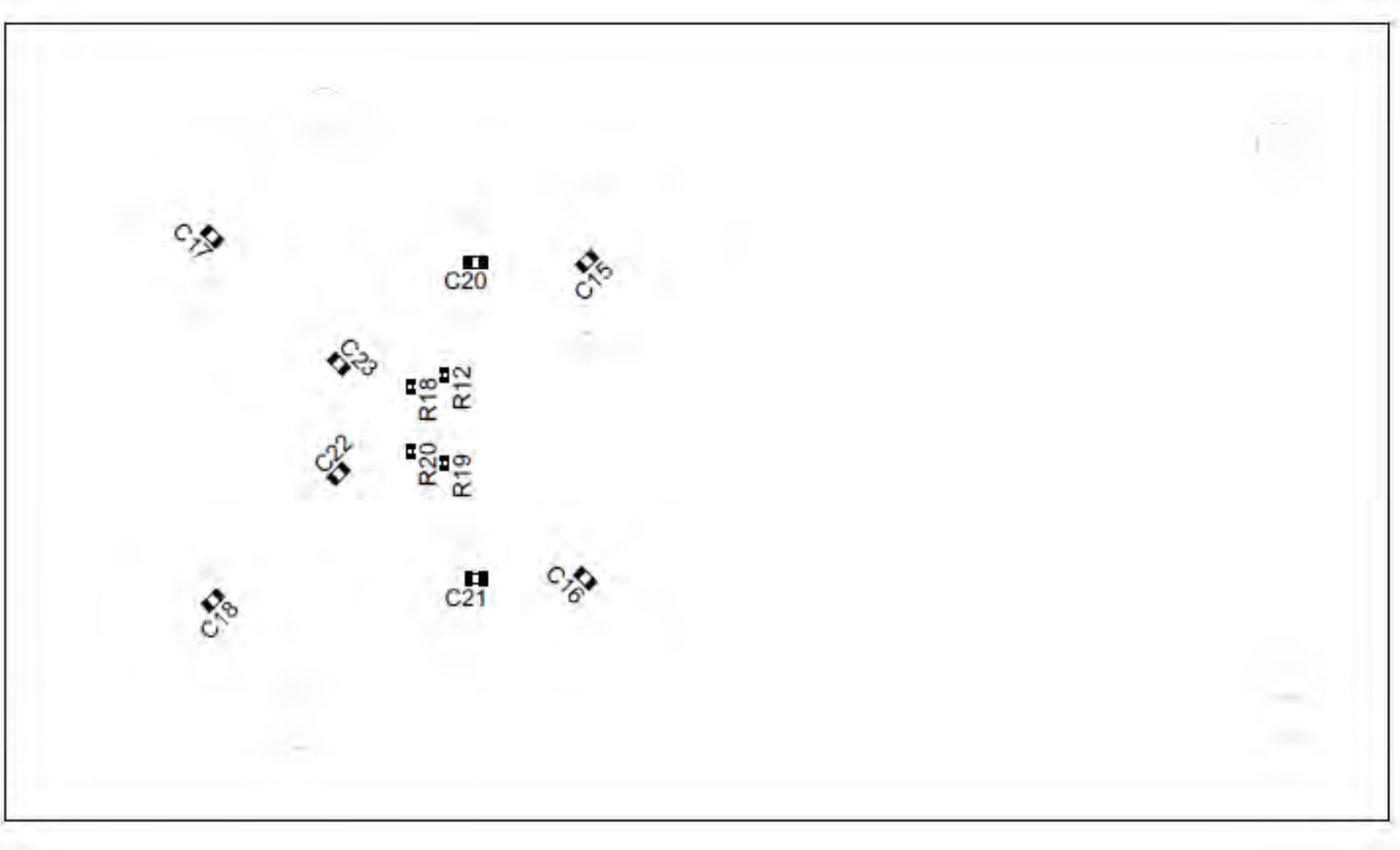
6. EVB circuit diagram



7. Evaluation Board top layout



8. Evaluation board bottom layout



9. Bill of Materials (BOM)

Part	Value	Device	Package	Description
C1	100p		C0603	CAPACITOR
C2	10n		C0603	CAPACITOR
C3	100p		C0603	CAPACITOR
C4	10n		C0603	CAPACITOR
C5	1n		C0603	CAPACITOR
C6	100p		C0603	CAPACITOR
C7	1n		C0603	CAPACITOR
C8	100p		C0603	CAPACITOR
C9	100p		C0603	CAPACITOR
C10	100n		C0603	CAPACITOR
C11	NM		C0603	CAPACITOR
C12	NM		C0603	CAPACITOR
C13	NM		C0603	CAPACITOR
C14	NM		C0603	CAPACITOR
C15	100n		C0603	CAPACITOR
C16	100n		C0603	CAPACITOR
C17	100n		C0603	CAPACITOR
C18	100n		C0603	CAPACITOR
C19	100n		C0603	CAPACITOR
C20	100n		C0603	CAPACITOR
C25	1u		C0603	CAPACITOR
C26	1u		C0603	CAPACITOR
C27	1u		C0603	CAPACITOR
C28	1u		C0603	CAPACITOR
C29	1u		C0603	CAPACITOR
I1	BGA7350		SOT617-1	BGA7350
JP1	AG	2 x 5pins	JP5	JUMPER
JP2	BG	2 x 5pins	JP5	JUMPER
JP3	EN	2 x 2pins	JP2	JUMPER
JP4	VCCB	1 x2pins	JP1	JUMPER
JP5	VCCA	1 x2pins	JP1	JUMPER
JP6	VCCdig	1 x2pins	JP1	JUMPER
JP7	VCM	2 x 2pins	JP2	JUMPER
JP8	VCMinA	1 x2pins	JP1	JUMPER
JP9	VCMinB	1 x2pins	JP1	JUMPER
JP10	VCMA	1 x2pins	JP1	JUMPER
JP11	VCMB	1 x2pins	JP1	JUMPER
JP12	GND	1 x2pins	JP1	JUMPER
JP13	GND	1 x2pins	JP1	JUMPER
JP15	VoutA	1 x3pins	JP3	JUMPER
JP16	VoutB	1 x3pins	JP3	JUMPER
L1	56n	0603LS	0603LS	Coilcraft
L2	56n	0603LS	0603LS	Coilcraft
L3	56n	0603LS	0603LS	Coilcraft
L4	56n	0603LS	0603LS	Coilcraft

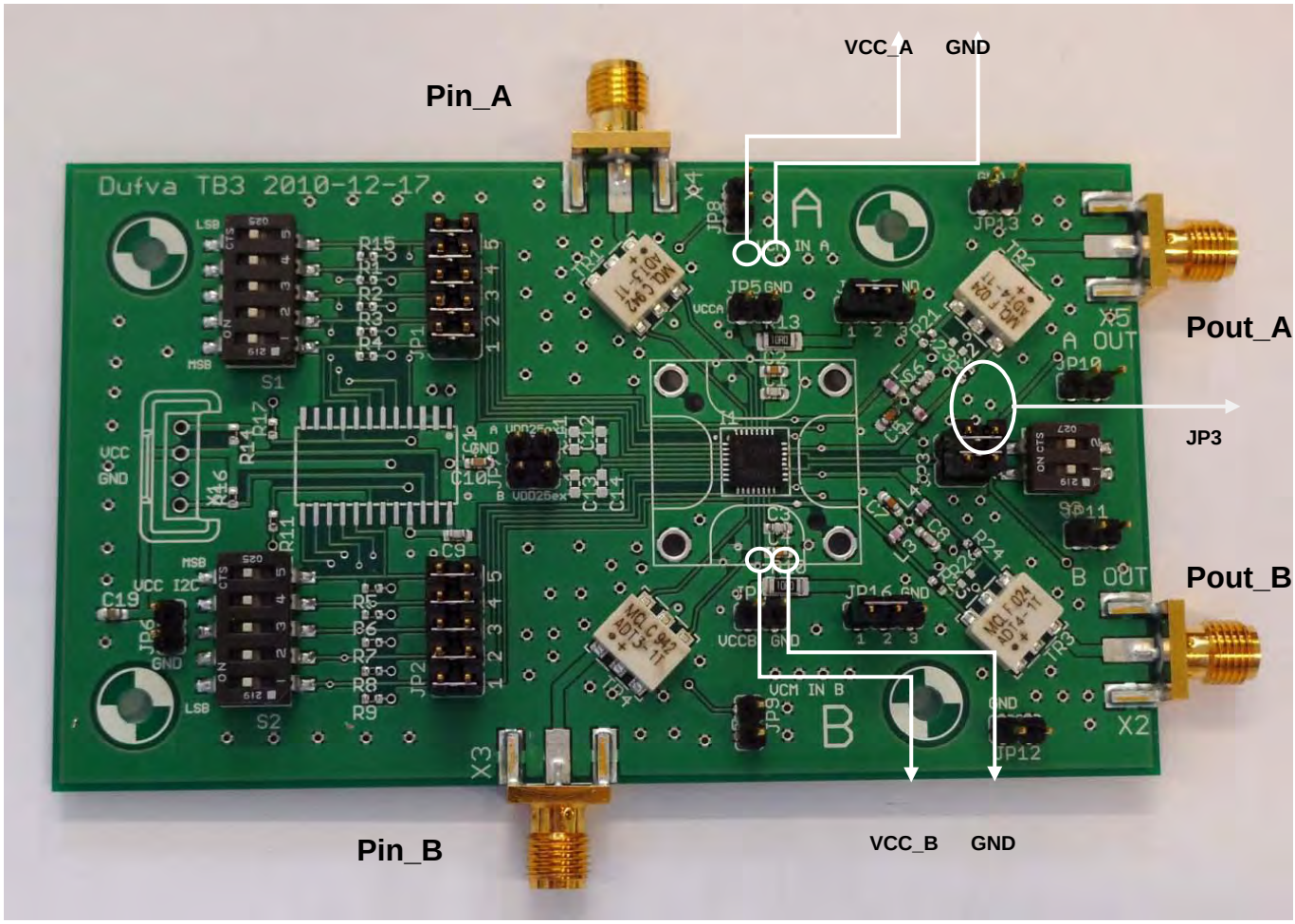
Part	Value	Device	Package	Description
R1	10k	R-EU_R0402	R0402	RESISTOR
R2	10k	R-EU_R0402	R0402	RESISTOR
R3	10k	R-EU_R0402	R0402	RESISTOR
R4	10k	R-EU_R0402	R0402	RESISTOR
R5	10k	R-EU_R0402	R0402	RESISTOR
R6	10k	R-EU_R0402	R0402	RESISTOR
R7	10k	R-EU_R0402	R0402	RESISTOR
R8	10k	R-EU_R0402	R0402	RESISTOR
R9	10k	R-EU_R0402	R0402	RESISTOR
R10	10	R-EU_R1206	R1206	RESISTOR
R11	10k	R-EU_R0402	R0402	RESISTOR
R12	0	R-EU_R0402	R0402	RESISTOR
R13	10	R-EU_R1206	R1206	RESISTOR
R14	10k	R-EU_R0402	R0402	RESISTOR
R15	10k	R-EU_R0402	R0402	RESISTOR
R16	10k	R-EU_R0402	R0402	RESISTOR
R17	10k	R-EU_R0402	R0402	RESISTOR
R18	0	R-EU_R0402	R0402	RESISTOR
R19	NM	R-EU_R0402	R0402	RESISTOR
R20	NM	R-EU_R0402	R0402	RESISTOR
R21	0	R-EU_R0402	R0402	RESISTOR
R22	0	R-EU_R0402	R0402	RESISTOR
R23	NM	R-EU_R0402	R0402	RESISTOR
R24	0	R-EU_R0402	R0402	RESISTOR
R25	0	R-EU_R0402	R0402	RESISTOR
R26	NM	R-EU_R0402	R0402	RESISTOR
R27	0	R-EU_R0402	R0402	RESISTOR
R28	NM	R-EU_R0402	R0402	RESISTOR
R29	0	R-EU_R0402	R0402	RESISTOR
R30	NM	R-EU_R0402	R0402	RESISTOR
R31	NM	R-EU_R0402	R0402	RESISTOR
R32	0	R-EU_R0402	R0402	RESISTOR
R33	NM	R-EU_R0402	R0402	RESISTOR
R34	NM	R-EU_R0402	R0402	RESISTOR
R35	0	R-EU_R0402	R0402	RESISTOR
R36	0	R-EU_R0402	R0402	RESISTOR
R37	NM	R-EU_R0402	R0402	RESISTOR
R38	0	R-EU_R0402	R0402	RESISTOR
S1	DIP	219-05	CTS-219-05	Surface
S2	DIP	219-05	CTS-219-05	Surface
S3	DIP	219-02	CTS-219-02	Surface
TR1	ADT3-1T+	transformer		Mini-Circuits
TR2	ADT4-1T+	transformer		Mini-Circuits
TR3	ADT4-1T+	transformer		Mini-Circuits
TR9	ADT3-1T+	transformer		Mini-Circuits
X1	NM	con		
X2	BOUT_P	SMA connector		SMA
X3	BIN_P	SMA connector		SMA
X4	AIN_P	SMA connector		SMA
X5	AOUT_P	SMA connector		SMA
X10	NM	BU-SMA-V		FEMALE
X11	NM	SMA connector		SMA
X12	NM	SMA connector		SMA
X13	NM	SMA connector		SMA
X14	NM	BU-SMA-V		FEMALE
X15	NM	SMA connector		SMA

10. Operation of the BGA7350 EVB

10.1 Applying bias

The EVB, as shown in Fig. 4, should be connected to 5V supply, according the following connections:

1. Leave jumpers JP3 in their current position, as shown in Fig. 4
2. Apply +5V to VCC_A and/or VCC_B to the pins, as shown in Fig. 4
3. Apply ground to GND_A and/or GND_B pins



26.

Fig 4. BGA7350 EVB picture

10.2 Mode of operation

The EVB of the BGA7350 can either be operated in the manual mode or ‘automatic’ mode. The BGA7350 can be enabled/disabled by switch3 (see Fig.5)

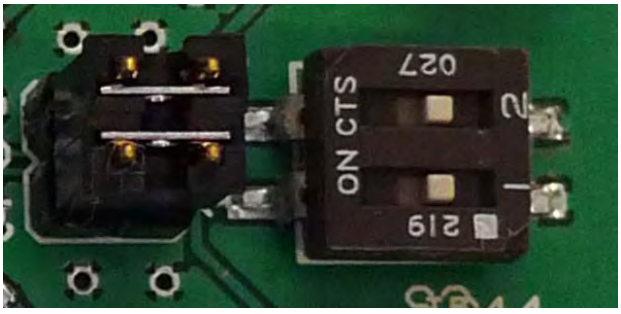


Fig 5. Enable/disable switch S3

10.2.1 Manual mode.

For manual mode operation, all jumpers, as shown in Fig. 5 must be in place. Also a 5V pull-up voltage and ground should be applied, as indicated as 5V/GND pull-up in Fig. 6.

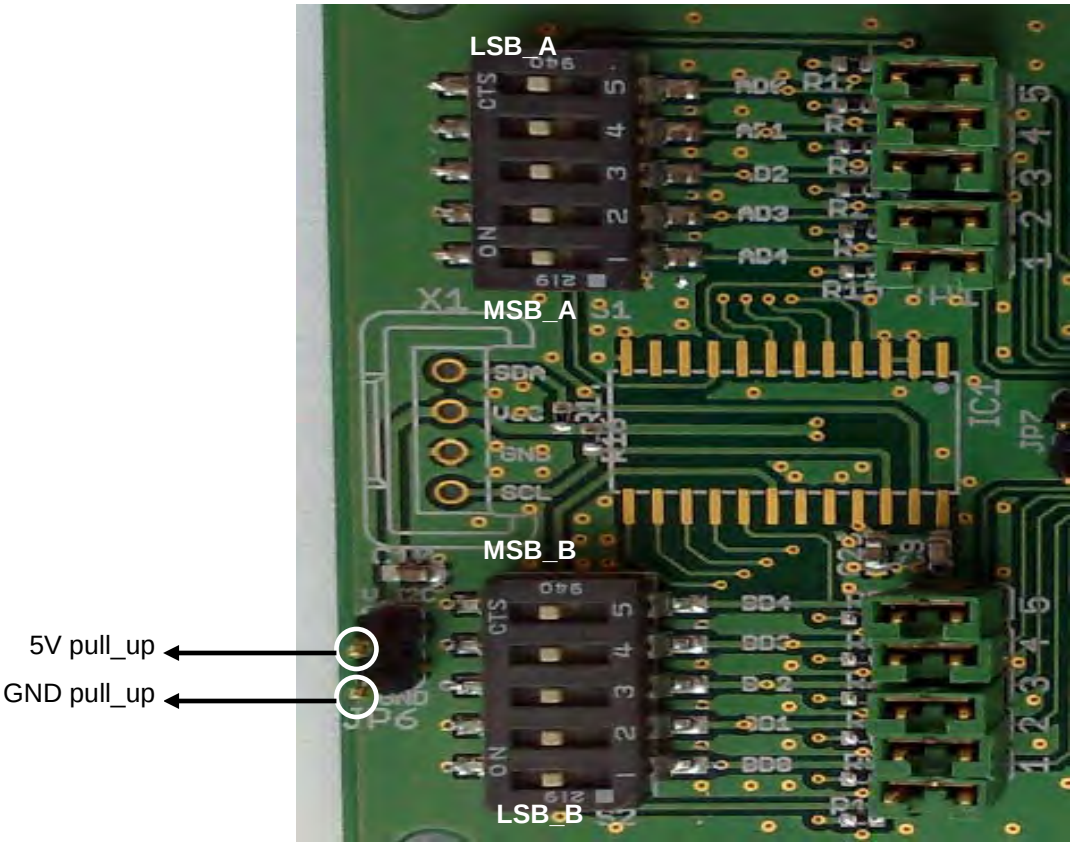


Fig. 6 Manual gain settings by switches S1 and S2

With the positions of S1 and S2, the gain range can be adjusted according the values in Table.3.

10.3 Mode of operation

The EVB of the BGA7350 can either be operated in the manual mode or ‘automatic’ mode. The BGA7350 can be enabled/disabled by switch3 (see Fig.5)

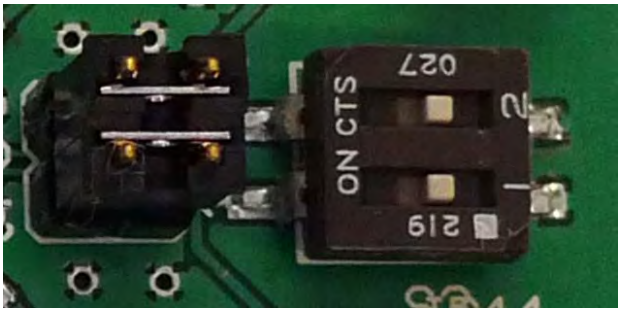


Fig 5. Enable/disable switch S3

10.3.1 Manual mode.

For manual mode operation, all jumpers, as shown in Fig. 5 must be in place. Also a 5V pull-up voltage and ground should be applied, as indicated as 5V/GND pull-up in Fig. 6.

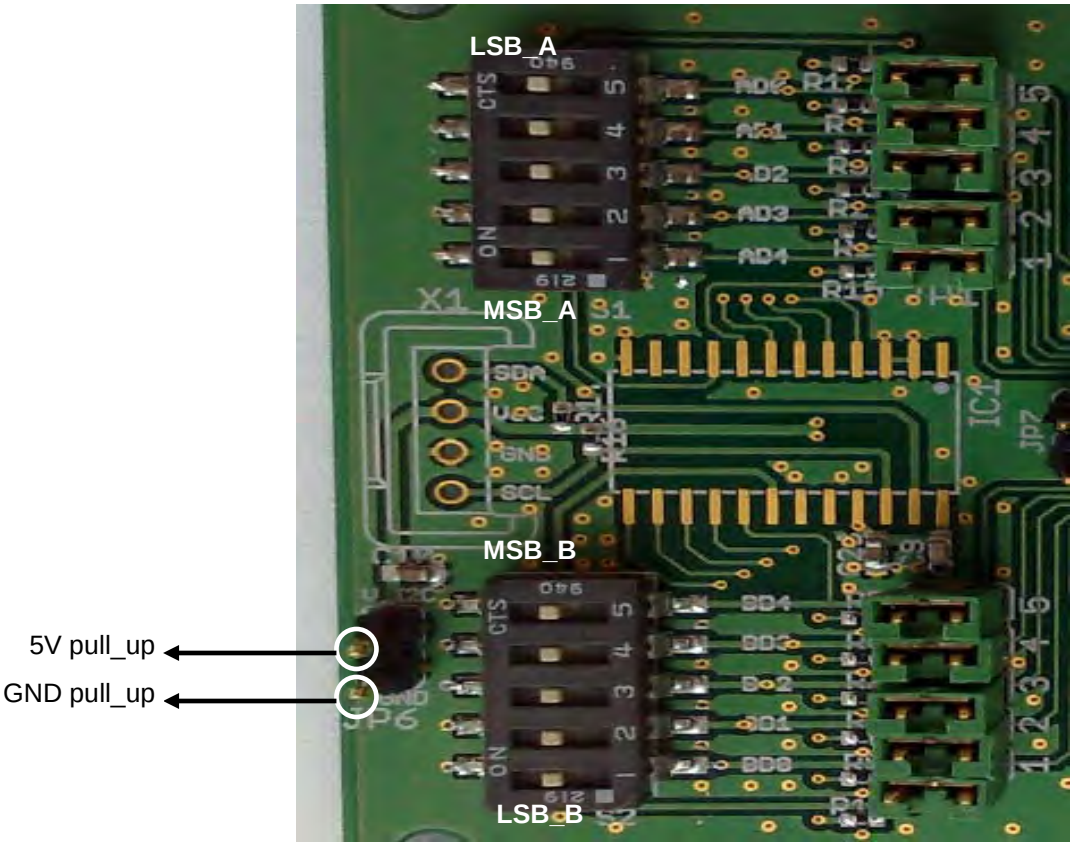


Fig. 6 Manual gain settings by switches S1 and S2

With the positions of S1 and S2, the gain range can be adjusted according the values in Table.3.

10.3.2 'Automatic' mode

For 'automatic' mode of operations the jumpers according Fig. 6 should be removed, and logic levels should be applied to the rows (also I^2C operation is possible, but not functional on this EVB), as indicated by the white circles (see Fig. 7). The logic levels applied to the pins should be within the following range:

0V < '0' < 0.8V

1.6V < '1' < 5V

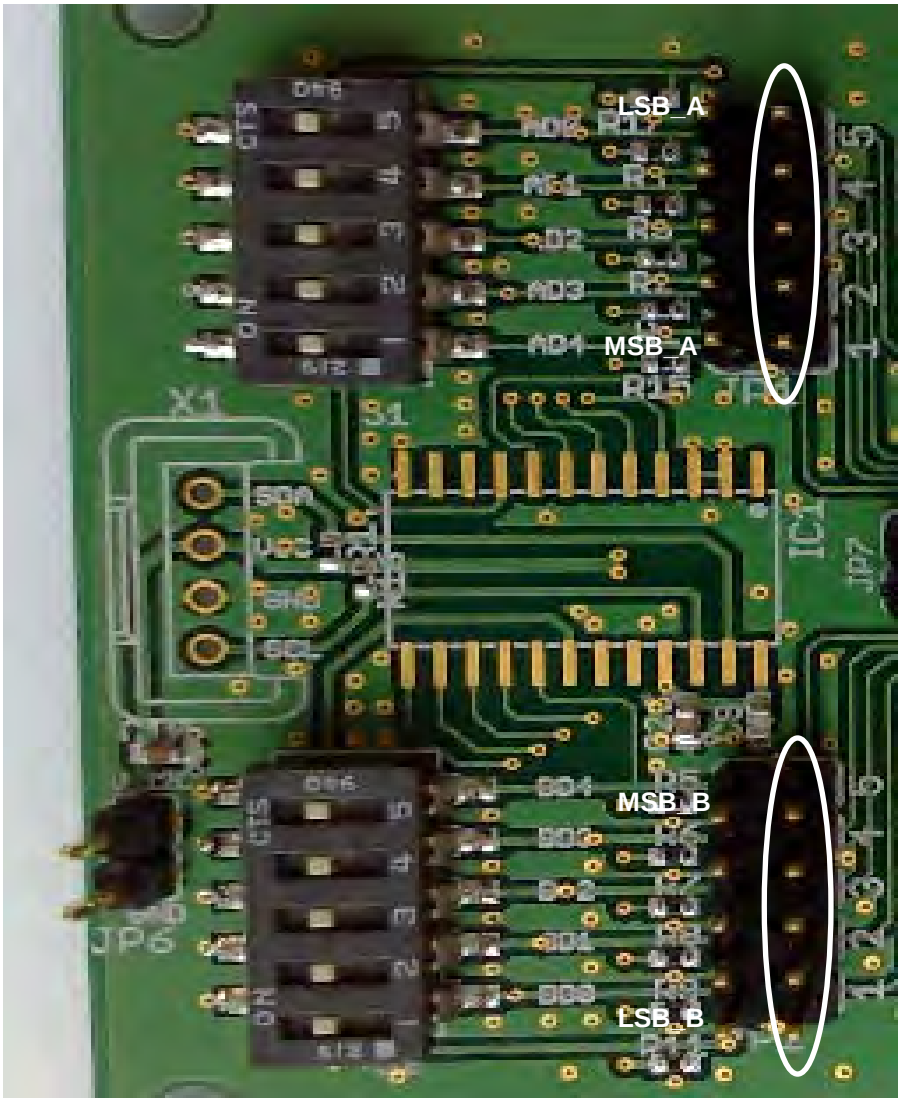


Fig. 7 Gain setting control by logic levels, according table 3

11. Measurements

On the BGA7350, the following measurements have been performed:

1. S-parameters. From the S-parameter measurements the following data can be deducted:
   a. S-parameters (Spar)
   b. Power gain (G_p)
   c. Gain adjustment range (Δg_{adj})
   d. Gain step (G_{step})
   e. Gain Flatness (G_{flat})
   f. Differential gain error (Eg_{diff})
   g. Integrated gain error (Eg_{itg})
   h. Isolation (ISL)
   i. Output power at 1dB compression (P_{1dB})

2. Harmonic Measurements. From the Harmonic measurements the following data can be deducted:
   a. Output third order intercept point ($IP3_O$)
   b. Second harmonic (H_2)
3. Noise Measurements. From the Noise measurements the following data can be deducted:
   a. Noise Figure (NF)
4. Timing measurement. From the Timing measurements the following data can be deducted:
   a. Gain step settling time (min/max) ($t_{s(step)G}$)

11.1 Measurement definitions

11.1.1 Differential input and output impedance

$|Zi| = |((1+S_{11}(F)) / (1-S_{11}(F)))| * 50Ohm$, with F = 160MHz … 300MHz

$|Zo| = |((1+S_{22}(F)) / (1-S_{22}(F)))| * 50Ohm$, with F = 160MHz … 300MHz

11.1.2 Absolute gain accuracy

Absolute gain accuracy (230Mhz) = $20log(|S_{21}(230MHz)|)$ – 22dB (=typical max gain)

11.1.3 Gain flatness

Gain flatness (F) = Max (Gain(F + ½ Fd … F – ½ Fd)) – Min (Gain(F + ½ Fd … F – ½ Fd))

with Gain(F) = $20*log(|S_{21}(F)|)$

11.1.4 Differential gain errors

Differential gain error = max | Gain(x) – Gain (x-1) –1dB |, with

Gain(x) = $20log(|S_{21}(x)|)$ measured at 230 MHz and x = gain setting (1…24)

Differential gain error (upper 12dB) = | Gain(0) – Gain (12) –12dB |, with

Gain(x) = $20log(|S_{21}(x)|)$ measured at 230 MHz and x = gain setting

Differential gain error (full range) = | Gain(0) – Gain (24) –24dB |, with

Gain(x) = $20log(|S_{21}(x)|)$ measured at 230 MHz and x = gain setting

11.1.5 Differential phase errors

Differential phase error (consecutive gain steps) = $arg(S_{21}(x)) – arg(S_{21}(x-1))$

with x = gain setting (0…24), measured 230 MHz

Differential phase error (any two steps upper 12dB) = $max(arg(S_{21}(x;x-12))) – min(arg(S_{21}(x;x-12)))$

with x = gain setting, measured at 230 MHz

Differential phase error (any two steps) = $max(arg(S_{21}(x))) – min(arg(S_{21}(x)))$

with x = gain setting (0…24), measured at 230 MHz

11.1.6 OPI3

OIP3low = Po(F_1)+ ½ (Po(F_1)-Po(F_1-2MHz)), with F_1=230 MHz F_2 = F_1+2MHz

OIP3high = Po(F_2)+ ½ (Po(F_2)-Po(F_2-2MHz)), with F_1=230 MHz F_2 = F_1+2MHz

OIP3 = Min (OIP3low, OIP3high)

11.1.7 H2

2^{nd} order harm (F) = 20log(|S21(2*F)|) – 20log((|S21(F)|)

11.2 S-parameter measurements

The S-parameters (and the above mentioned derivative measurements) are measured with a full two-port calibrated network analyzer; over the frequency range 160 –300 MHz Also the output power compression point (P_{1dB}) has been measured with the network analyzer. In the latter case, a calibrated power sweep has been performed, in order to obtain the P_{1dB}.

All gain and phase measurements have been performed with a constant output power of +5 dBm, meaning that for every 1 dB increase of attenuation, the input power also have to increase by +1 dBm.

The non-used port's of the dual VGA (channel A or B) has been terminated with a 50-Ohm load.

The isolation measurement (ISL) have been performed by injecting the signal to the input of channel A, and measuring the response at the output of channel B (and vice versa), with the remaining input and output terminated with 50 Ohm.

11.3 Harmonic measurements.

The harmonic measurements (OIP_2, OIP_3 and H_2) have been measured with a set-up, as described in Fig. 8.

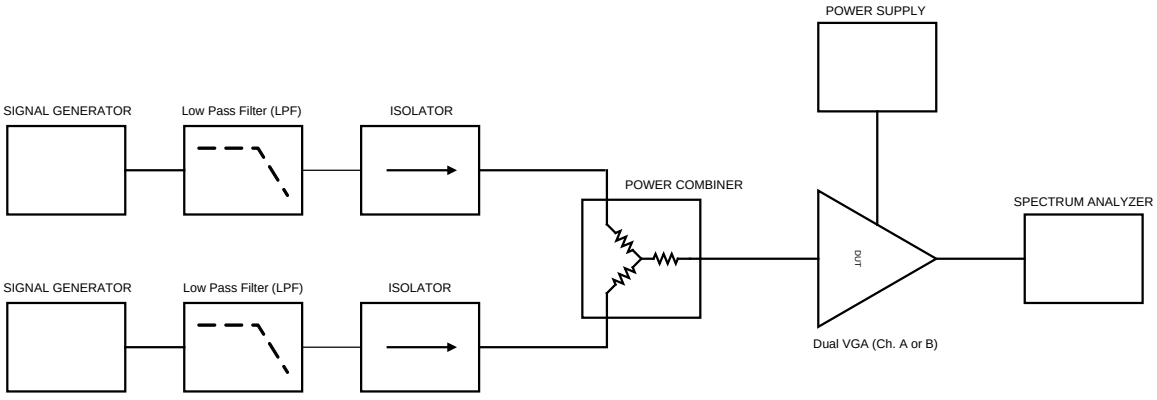


Fig. 8 Harmonic measurement set-up

A low-pass filter at the output of the signal generators guaranties suppression of the H_2 generated by the generator itself.

11.4 Noise Figure measurements

The Noise Figure (NF) has been measured with a noise source (Excess Noise Ratio ENR=15.3 dB), in combination with a spectrum analyzer with a noise measurement option. (See Fig.9)

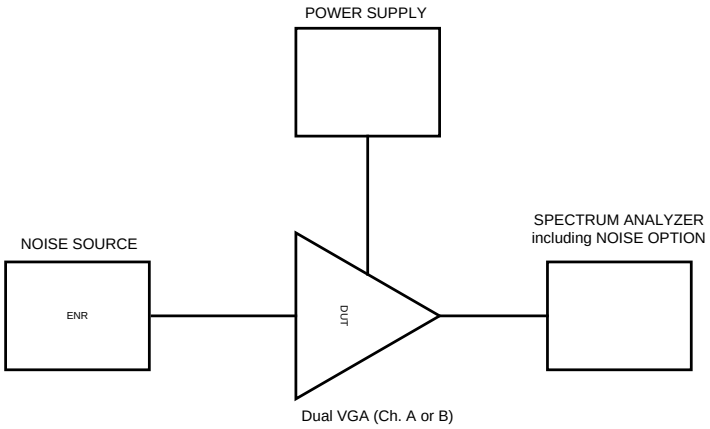


Fig. 9 Noise Figure Measurements

11.5 Timing Measurement.

In order to determine the gain step settling time, the set-up as shown in Fig. 10 has been used. A pulse generator (preferably a pulse generator that can supply the proper logic levels) is connected to the disable/enable pin of the EVB. The input (Pin_A or Pin_B) is connected to a signal generator (or network analyzer) to supply the RF input signal. The response (Pout_A or Pout_B) is measured with a digital sampling scope, triggered by the pulse generator. The 50-Ohm input of the sampling scope is used, in order to terminate the output of the dual VGA properly.

With the pulse generator, the gain settings are switch from minimum (00000) to maximum (11000) attenuation.

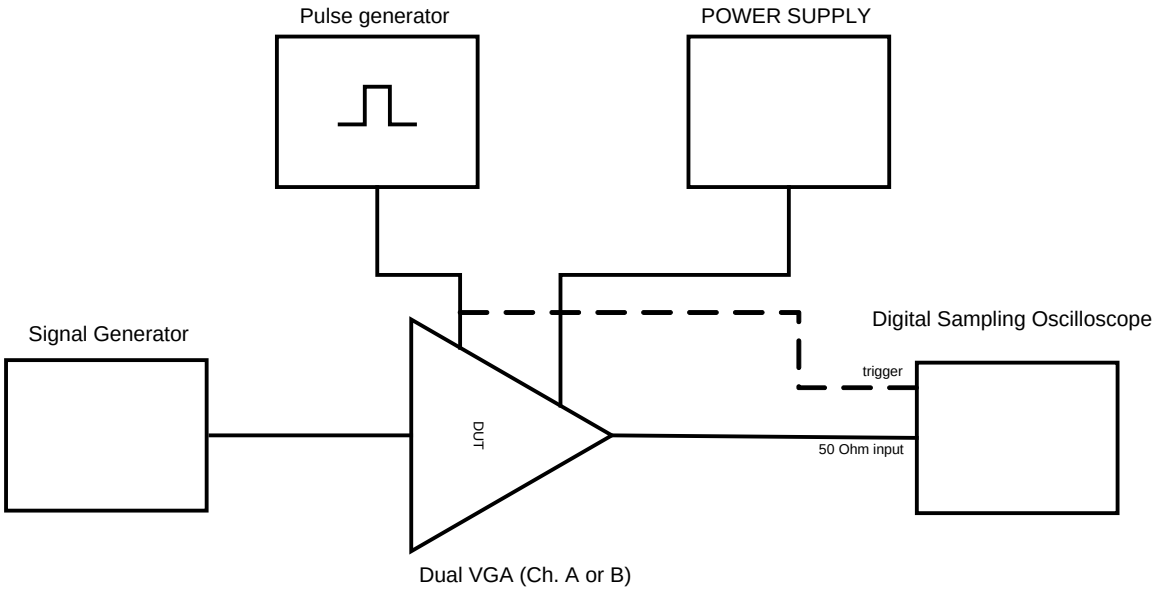


Fig. 10 Timing measurements

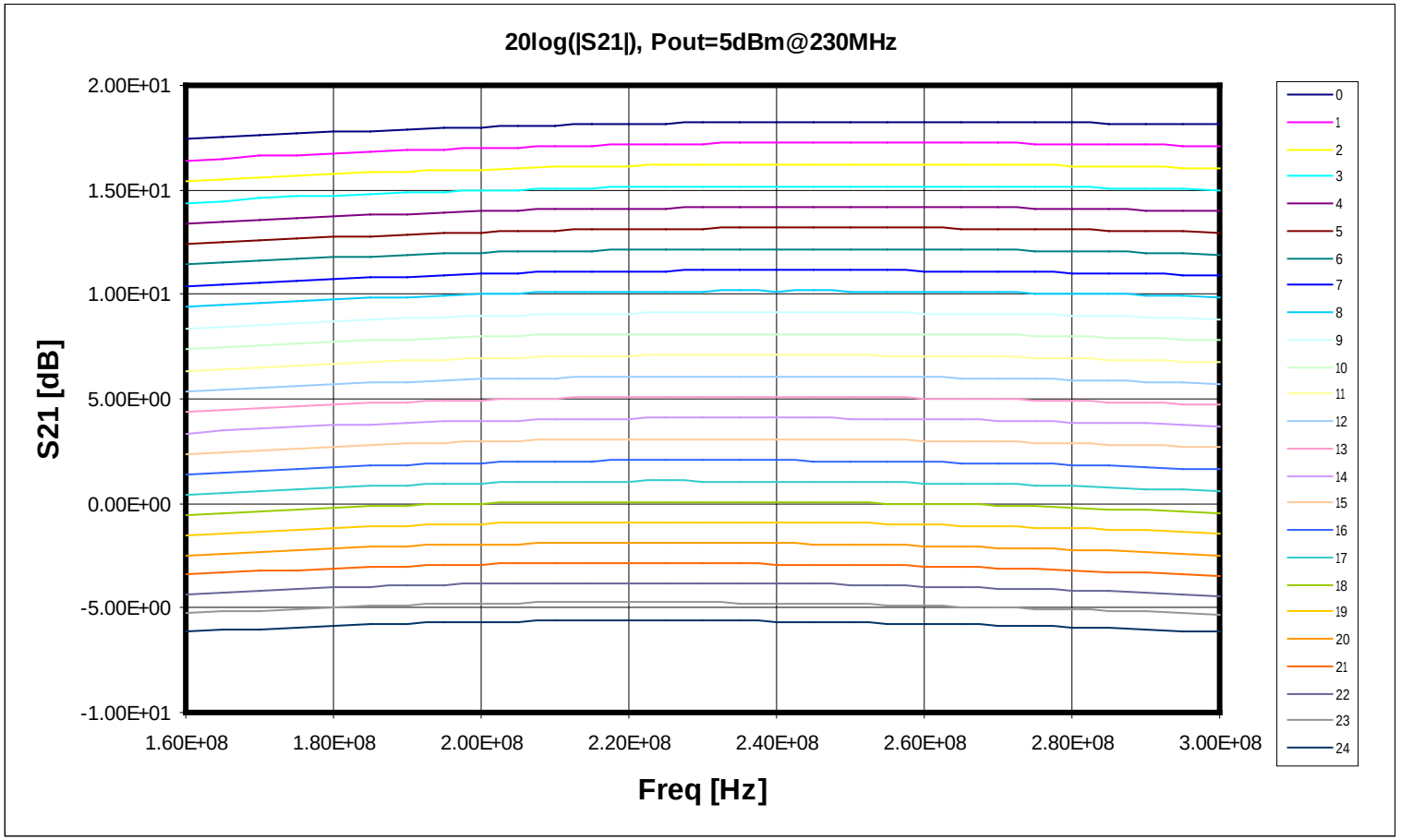
11.6 Measurement results

The section following below shows performance measurements of the BGA7350 EVB in single-ended operations.

The EVB has been measured under the following conditions:

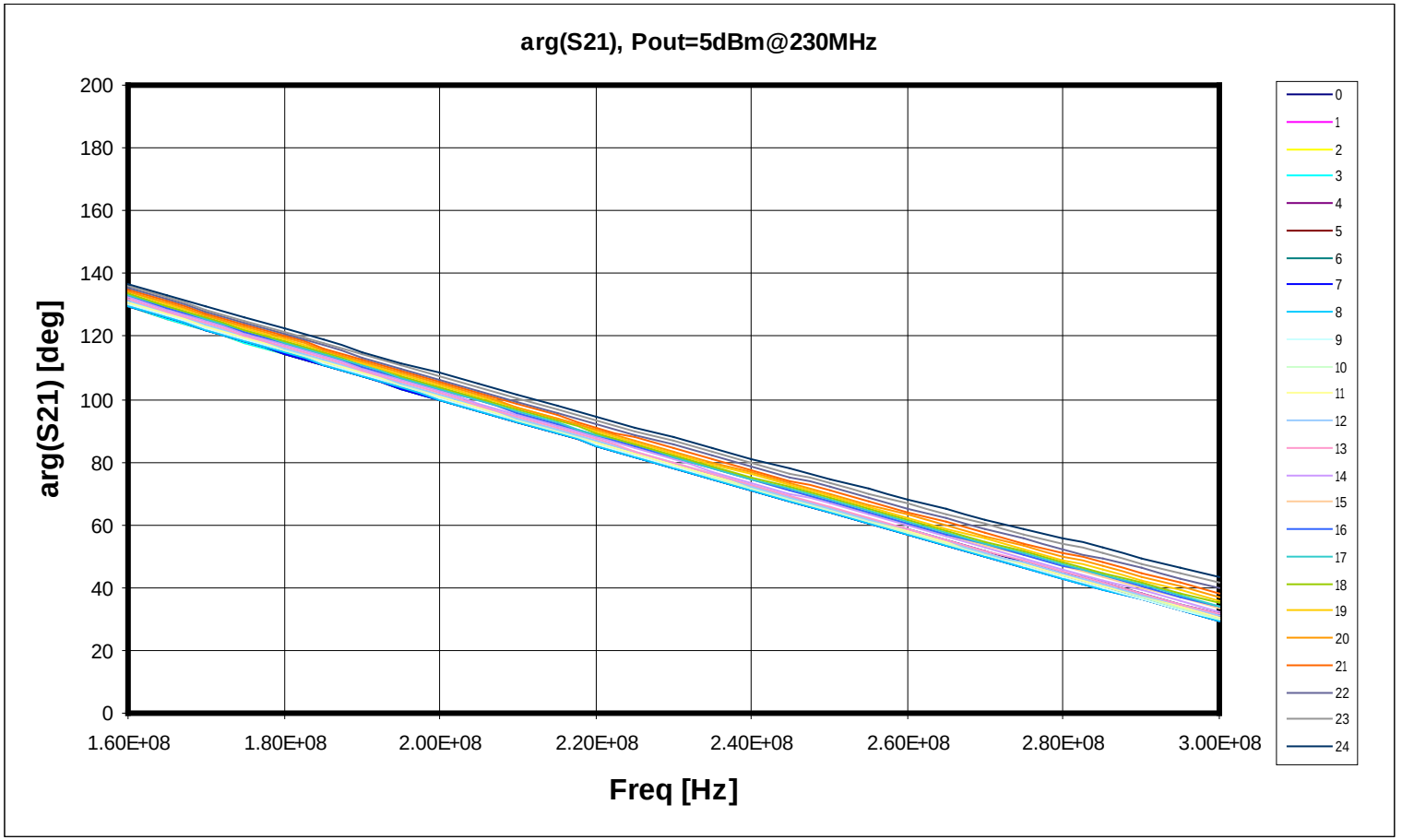
- Measurement data corrected for input-and output transformer losses
  - Input transformer; losses 0.55 dB, transformer ratio 1:3
  - Output transformer; losses 0.6 dB, transformer ratio 1:4
- EVB optimized for 230 MHz operation (other frequency ranges can be easily optimized by changing L1 .. L4, see also circuit diagram.
- 5V supply
- 25 deg. Ambient temperature

11.6.1 Gain as function of frequency and attenuator range



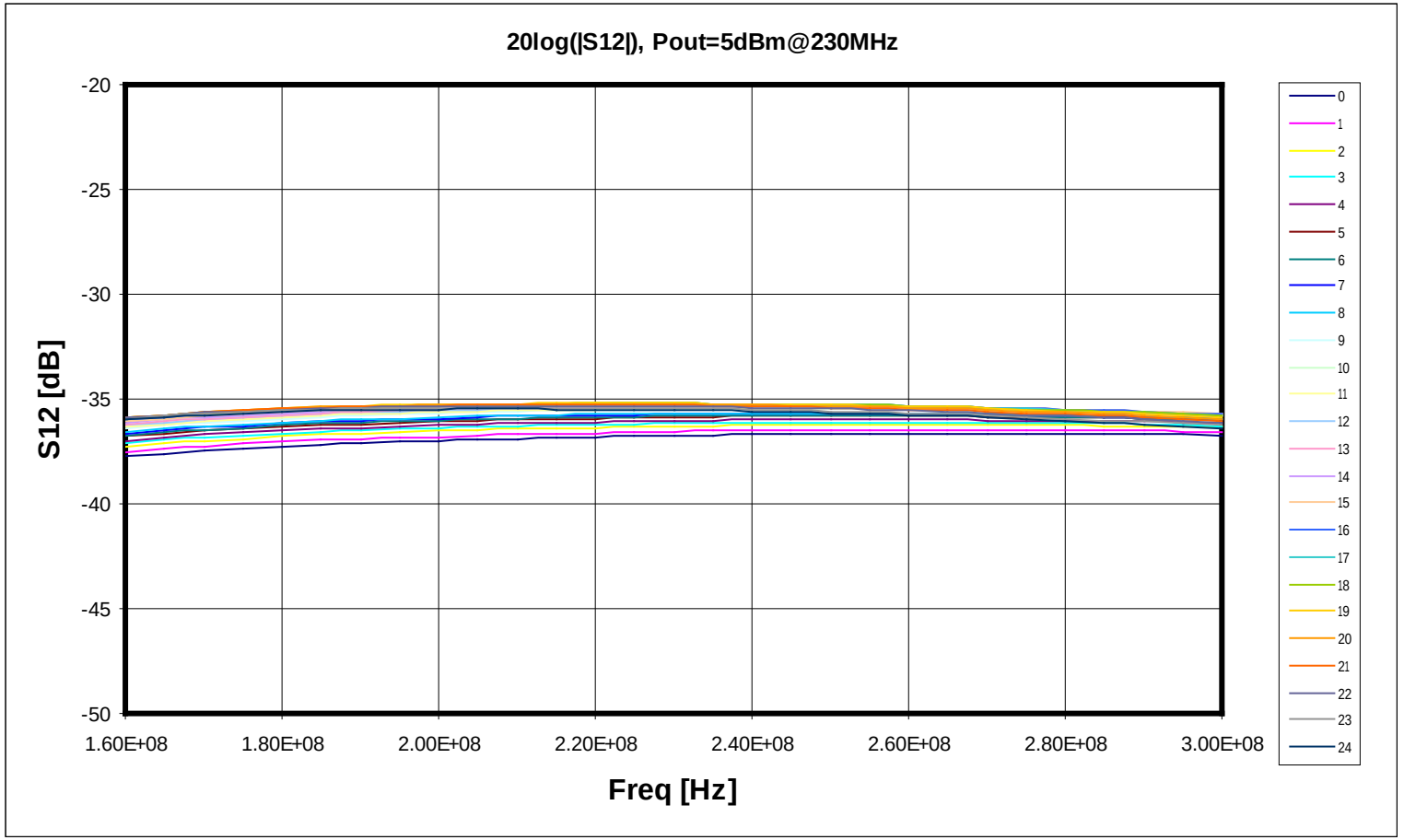
Note: every gain step measured @Pout= 5dBm

11.6.2 Phase of S21 as function of frequency and attenuator range



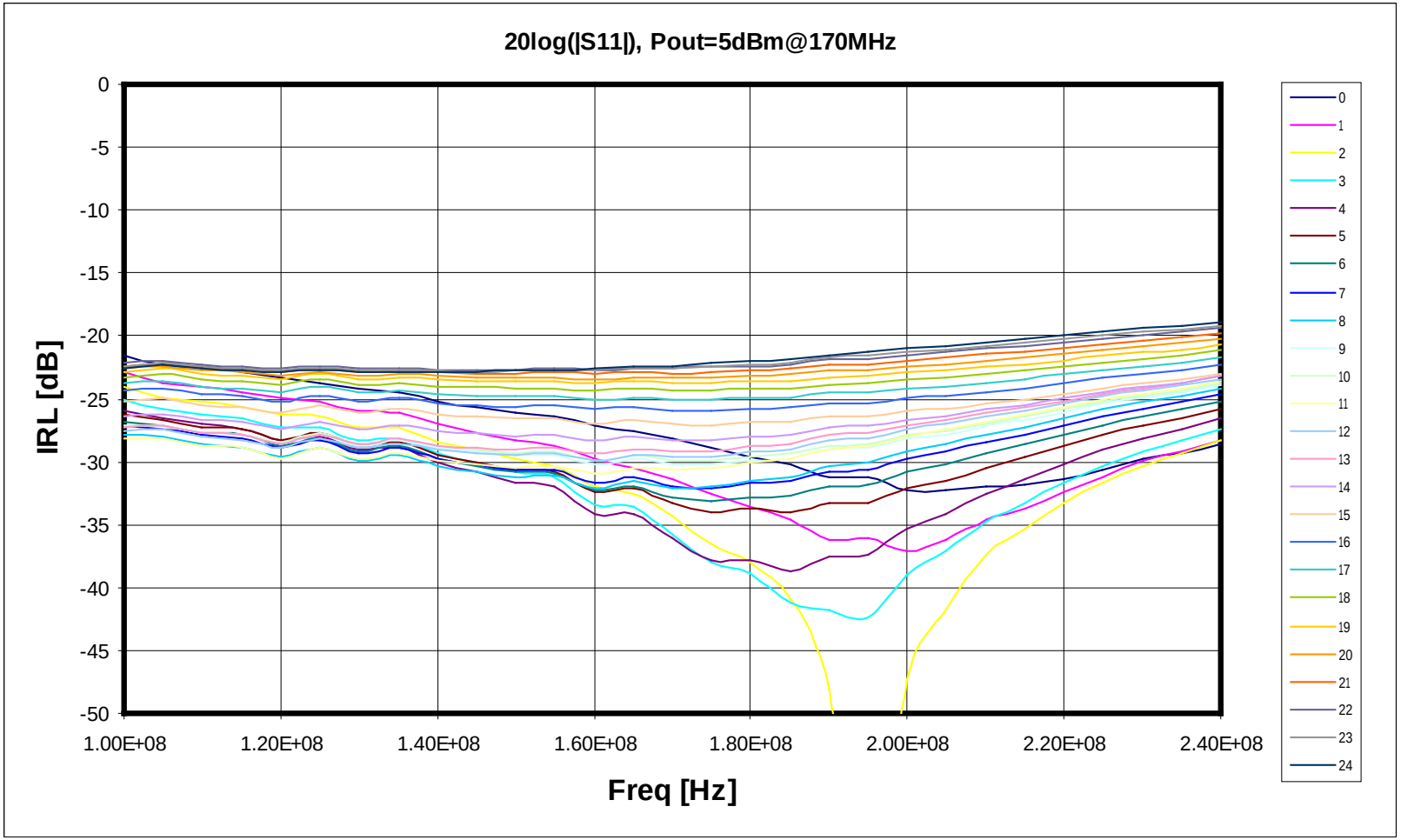
Note: every gain step measured @Pout= 5dBm

11.6.3 S-parameters; S12



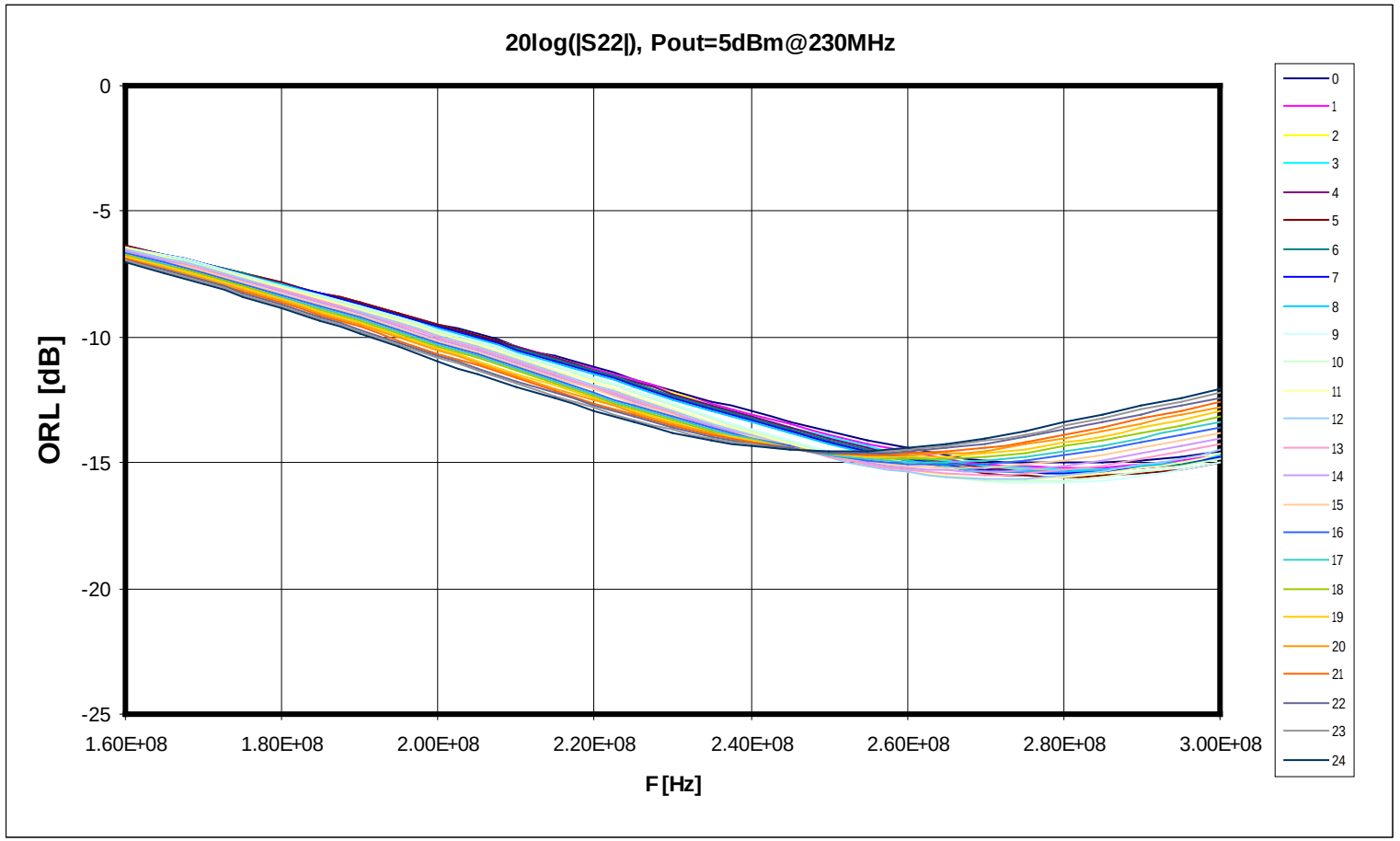
Note: every gain step measured @Pout= 5dBm

11.6.4 S-parameters; S11



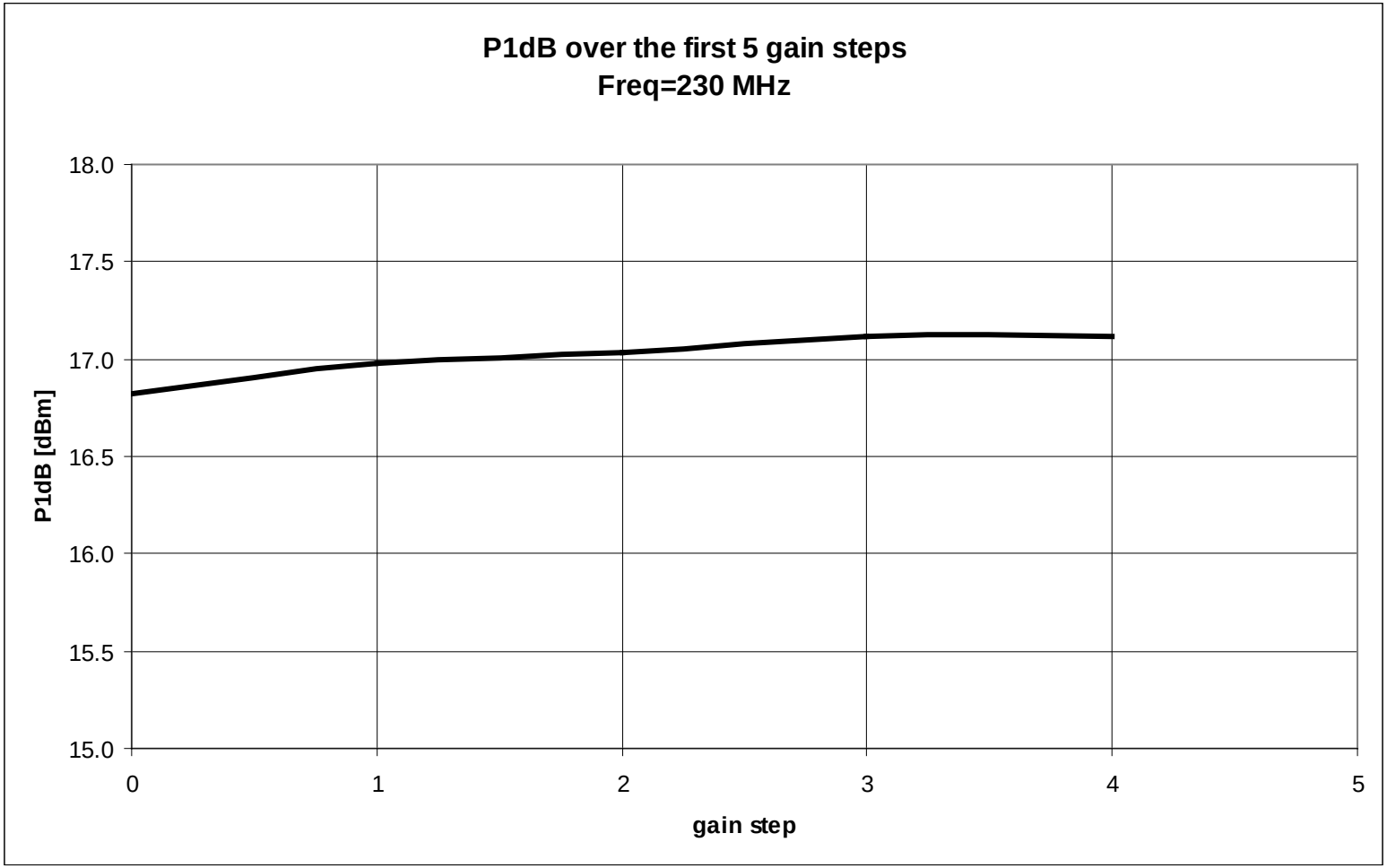
Note: every gain step measured @Pout= 5dBm

11.6.5 S-parameters; S22

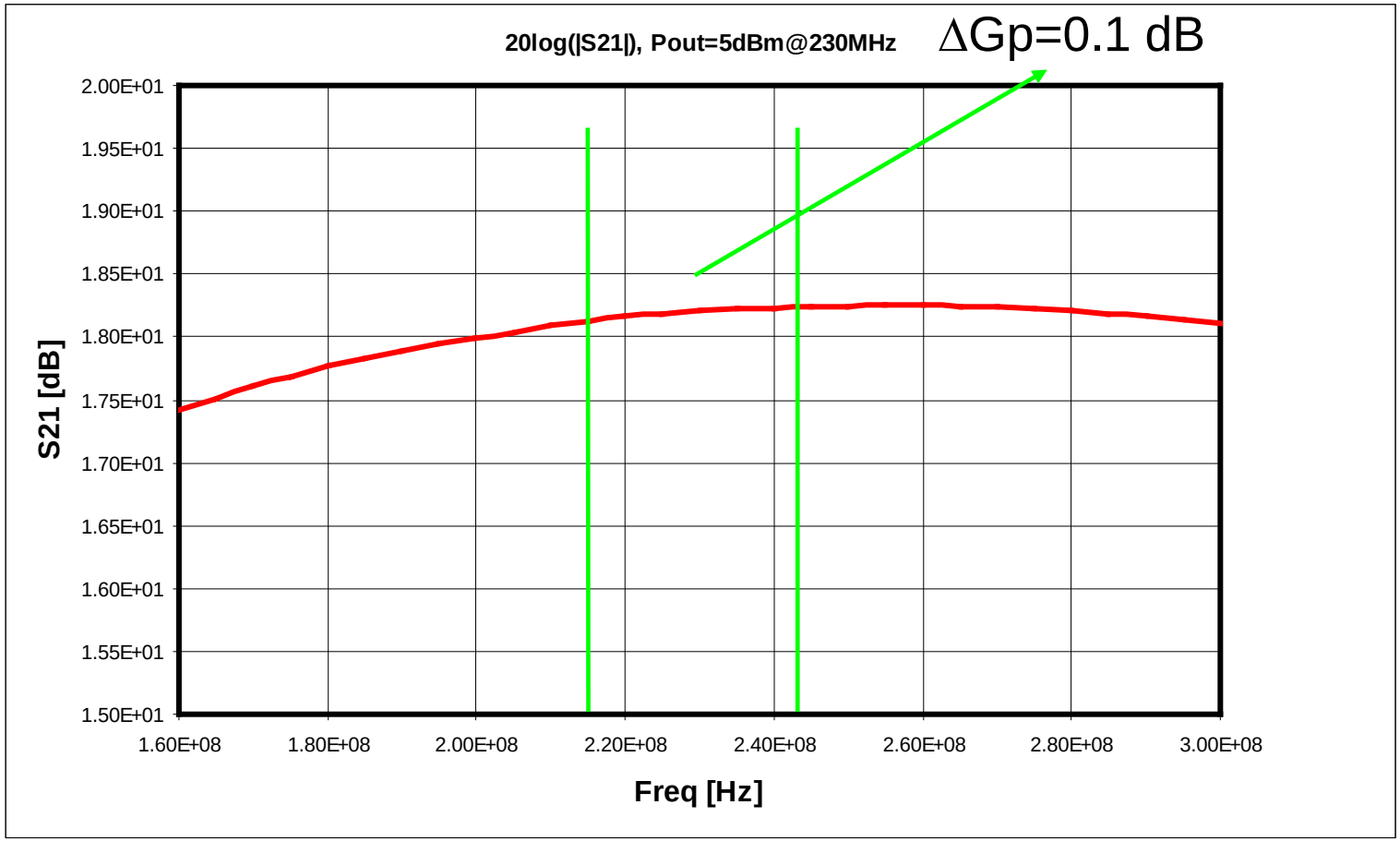


Note: every gain step measured @Pout= 5dBm

11.6.6 P1dB over first 5 gain steps

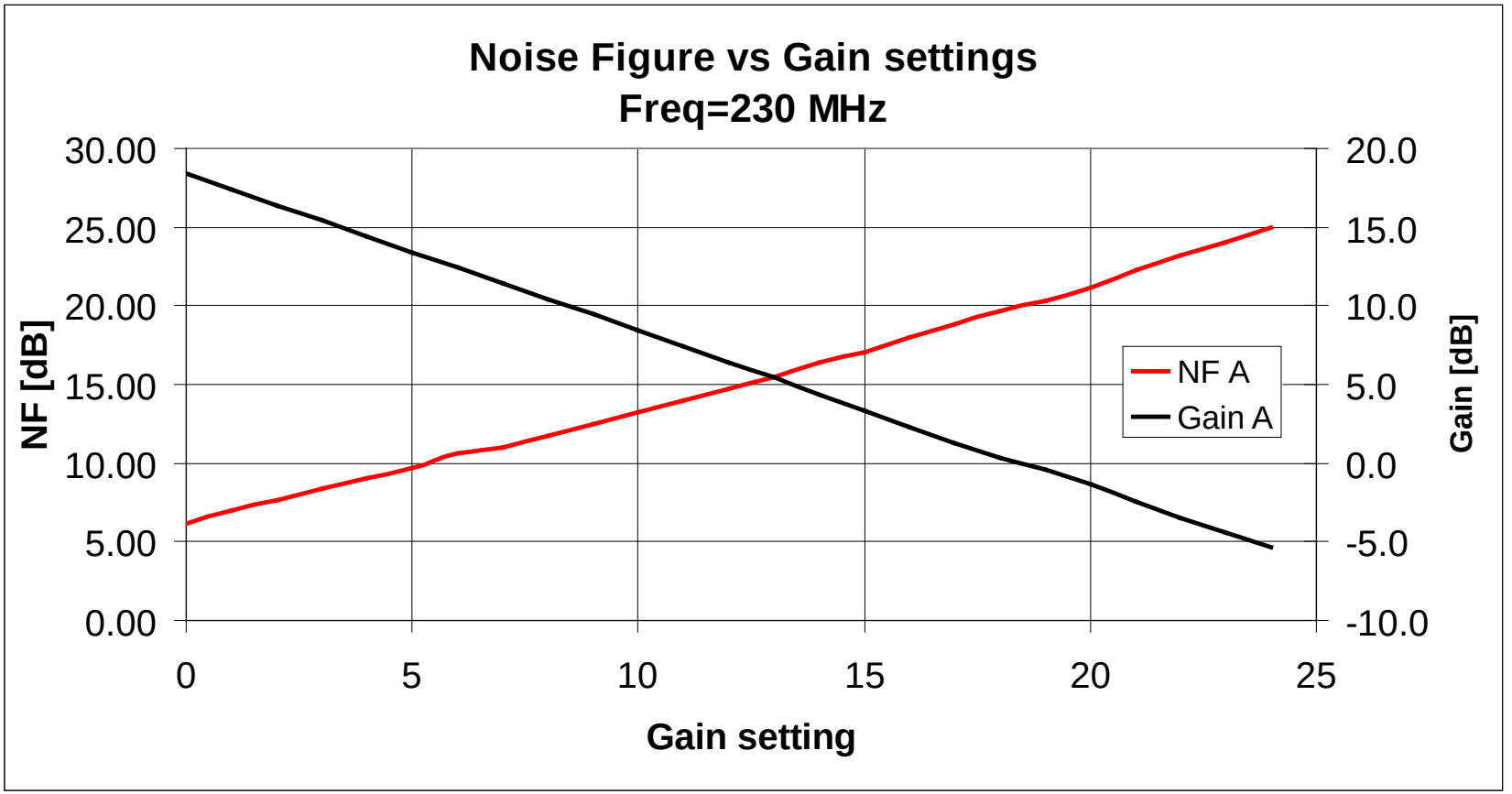


11.6.7 Gain Flatness @maximum gain



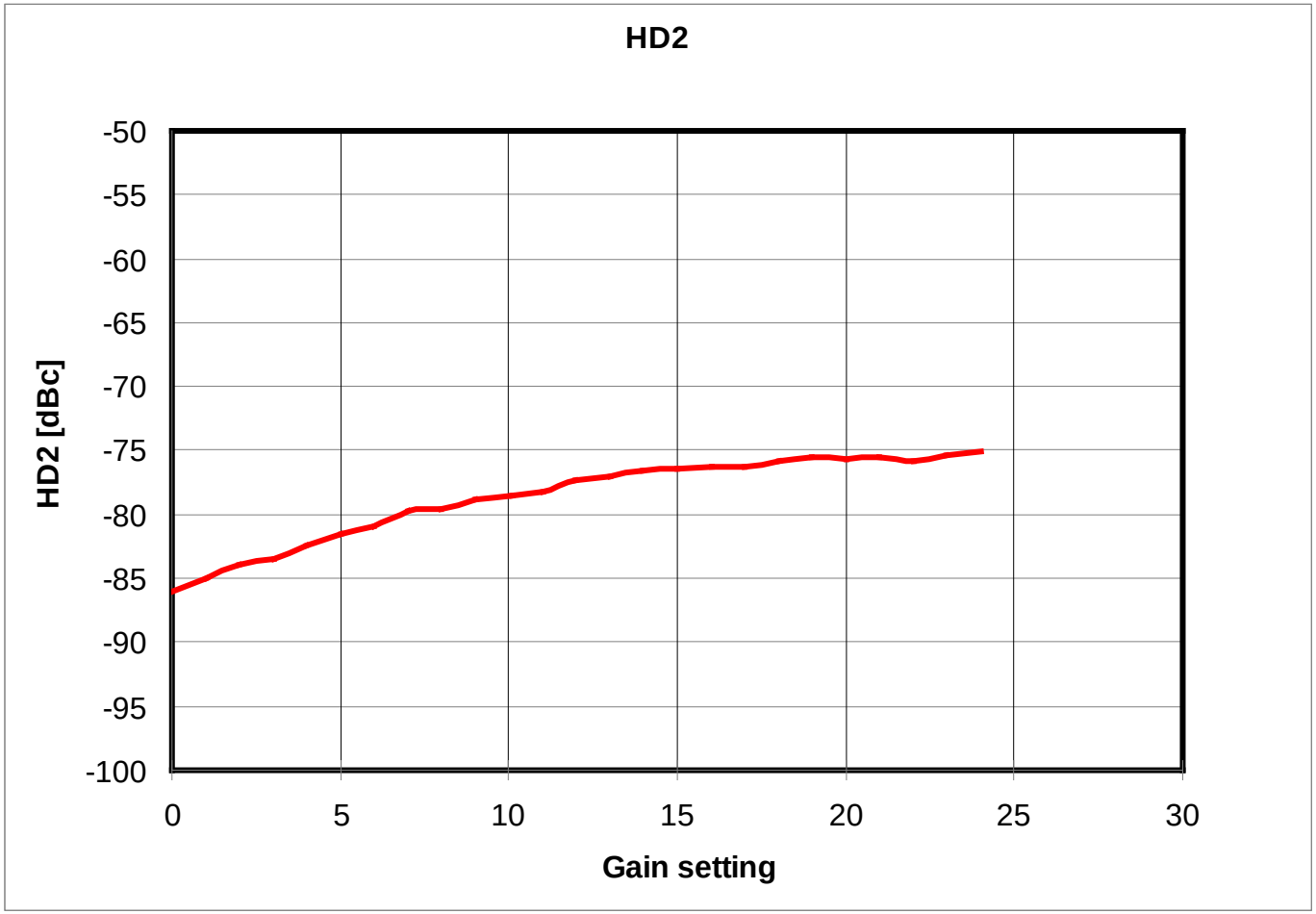
ΔGp=0.1 dB over operating frequency band

11.6.8 Noise Figure versus gain settings



Fmin=6.2 dB (@minimum attenuation, noise step = 0.8dB/dB

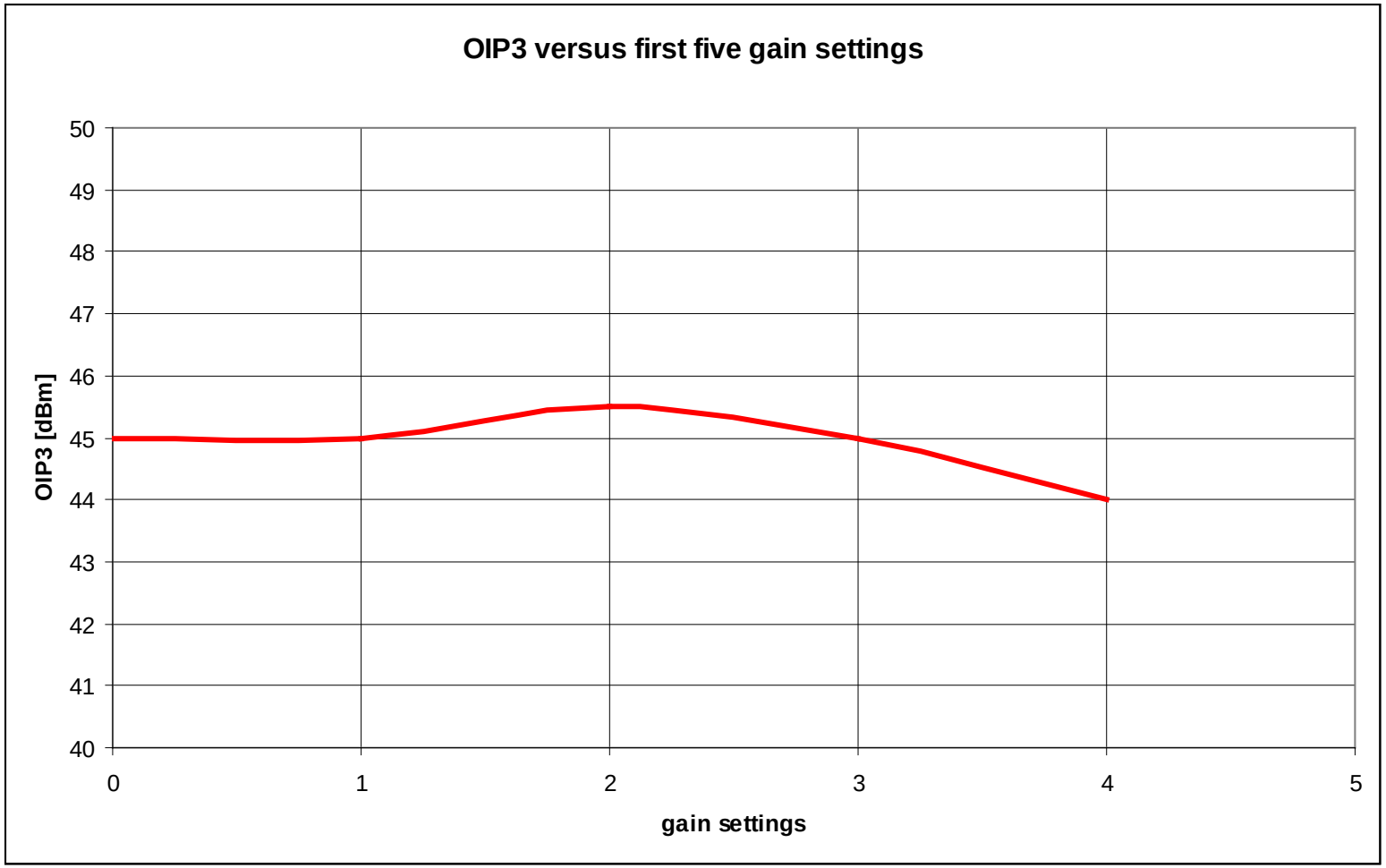
11.6.9 Harmonic Distortion (HD2) versus gain steps



Note: Pout=+5 dBm for every gain step

Freq_in=130 MHz

11.6.10 OIP3 over first 5 gain steps



Note: Pout per tone =+2 dBm
Freq1=170 MHz ; Freq2= 172 MHz

11.6.11 Summary of the gain errors

Measurement	Unit	Value	Conditions
Temperature	C	25 deg	
Power supply voltage	V	6	Definition
Power supply current	mA	125.8	Maximum supply current for all gain steps
Standby current	mA	2.72	Maximum standby current (for all gain steps)
Absolute gain	dB	18.21	Gain measured at F=230MHz
Differential gain error per 1dB consecutive steps	|dB|	0.13	Measured at F=230MHz
Integrated gain error upper 12dB	dB	0.13	Measured at F=230MHz
Integrated gain error full range	dB	-0.18	Measured at F=230MHz
Gain flatness over 30MHz bandwidth at maximum gain	dB	0.12	pk-pk over 30MHz bandwidth at gain=0
Gain flatness over 30MHz bandwidth at minimum gain	dB	0.06	pk-pk over 30MHz bandwidth at gain=24
Maximum gain flatness over 30MHz	dB	0.03	Maximum flatness over 30MHz for all gain steps
Minimum gain flatness over 30MHz	dB	0.24	Minimum flatness over 30MHz for all gain steps

11.6.12 Isolation (between channel A and channel B)

Gain settings @170 MHz	isolation [dB]
min	-59.8
max	-60

Measured @Pout=5dBm for both min and max gain

11.6.13 Impedance summary

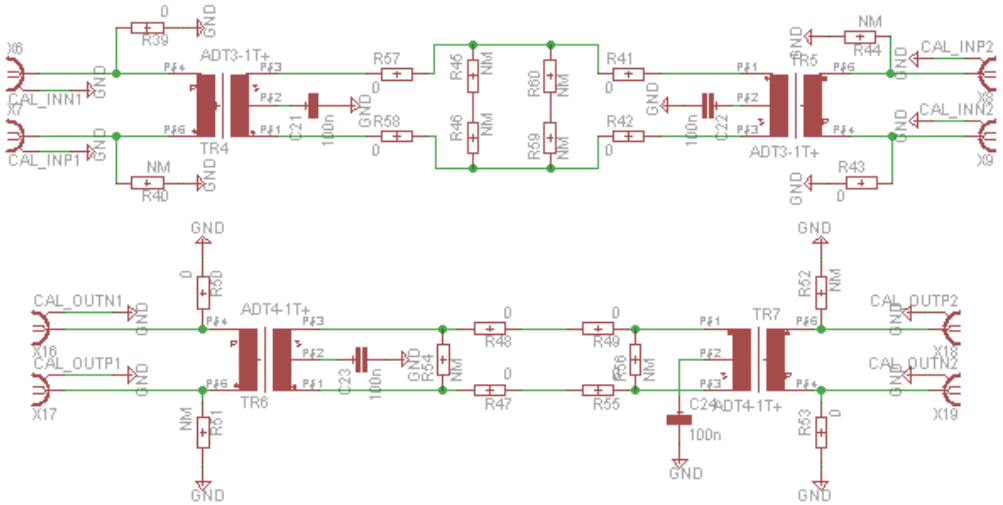
Measurement	Unit	Value	Conditions
Maximum input impedance (BW=30 all gainsteps)	|Ohm|	57.7	Maximum absolute value measured over 30MHz bandwidth, for all gain steps
Minimum input impedance (BW=30 all gainsteps)	|Ohm|	43.8	Minimum absolute value measured over 30MHz bandwidth, for all gain steps
Maximum output impedance (BW=30 all gainsteps)	|Ohm|	66.4	Maximum absolute value measured over 30MHz bandwidth, for all gain steps
Minimum output impedance (BW=30 all gainsteps)	|Ohm|	53.2	Minimum absolute value measured over 30MHz bandwidth, for all gain steps
Maximum input impedance (BW=30 all gainsteps)	Ohm	57.5	Maximum real value measured over 30MHz bandwidth, for all gain steps
Minimum input impedance (BW=30 all gainsteps)	Ohm	43.5	Minimum real value measured over 30MHz bandwidth, for all gain steps
Maximum output impedance (BW=30 all gainsteps)	Ohm	59.0	Maximum real value measured over 30MHz bandwidth, for all gain steps
Minimum output impedance (BW=30 all gainsteps)	Ohm	49.6	Minimum real value measured over 30MHz bandwidth, for all gain steps

12. Balun Characterization

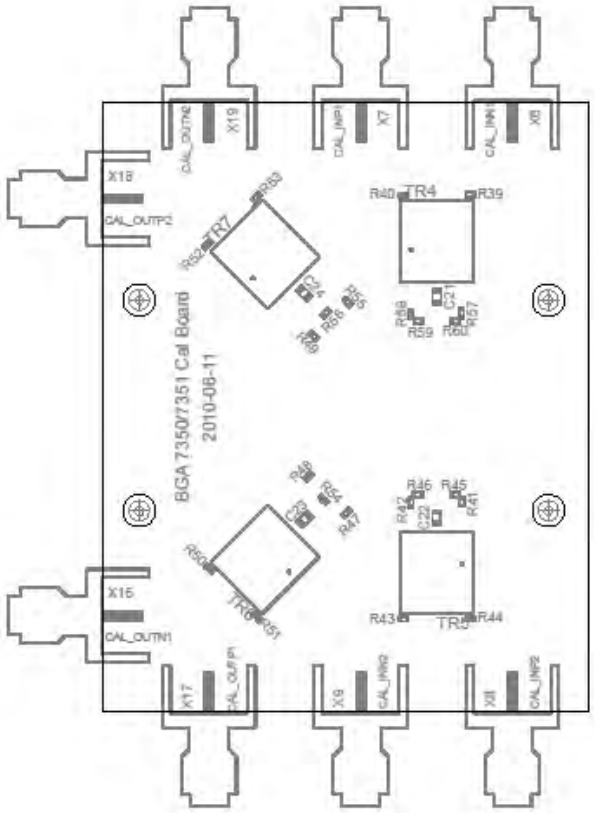
In order to determine the BGA7350 performance only, the input-and output balun characteristics (losses) must be determined for correction. This has been done by measuring the baluns (both input and output) back-to-back, and assuming that both transformers are identical, the measured losses can be divided by two, to determine the losses per balun.

The measurements have been performed on the (calibration) boards, as described below)

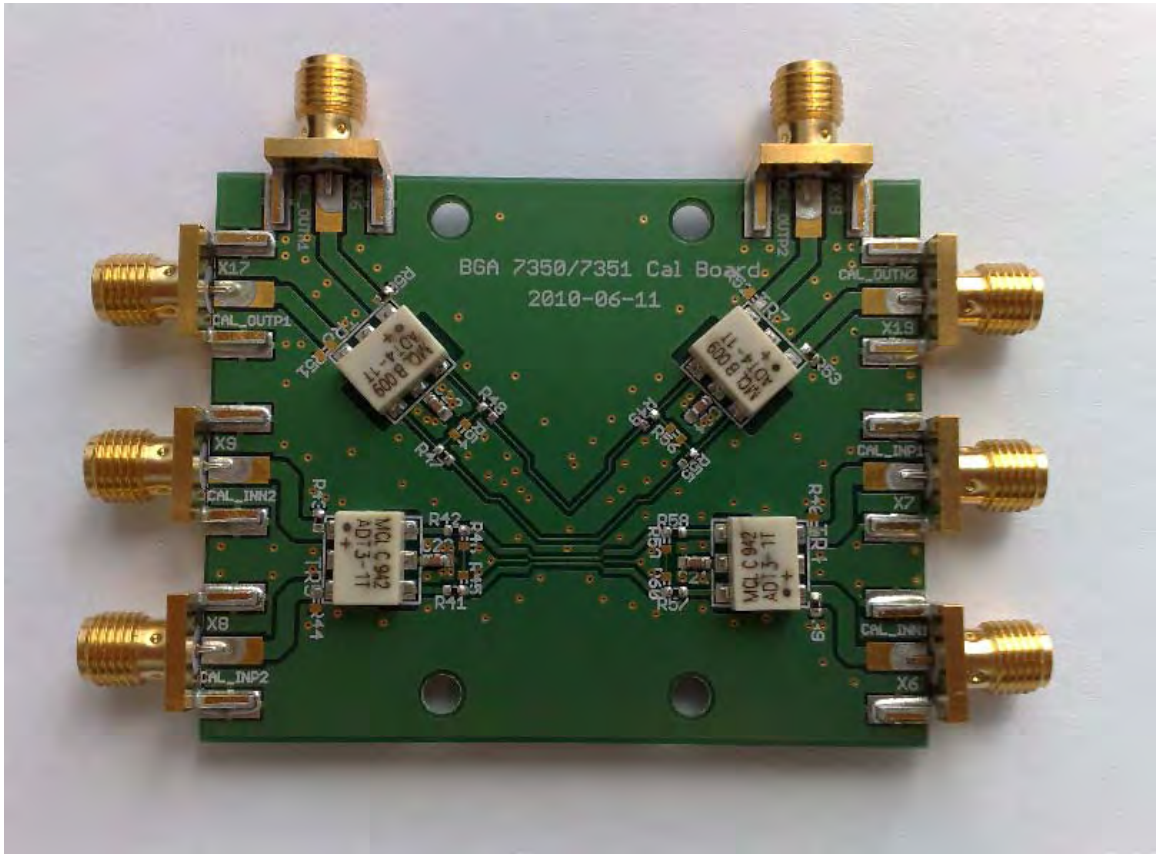
12.1 Calibration EVB schematics



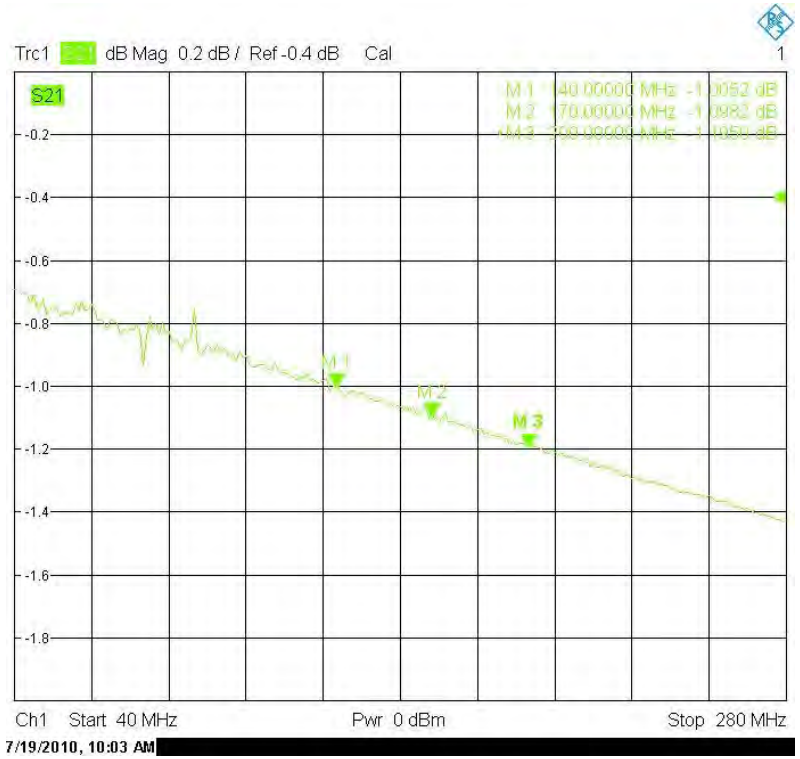
12.2 Calibration EVB layout



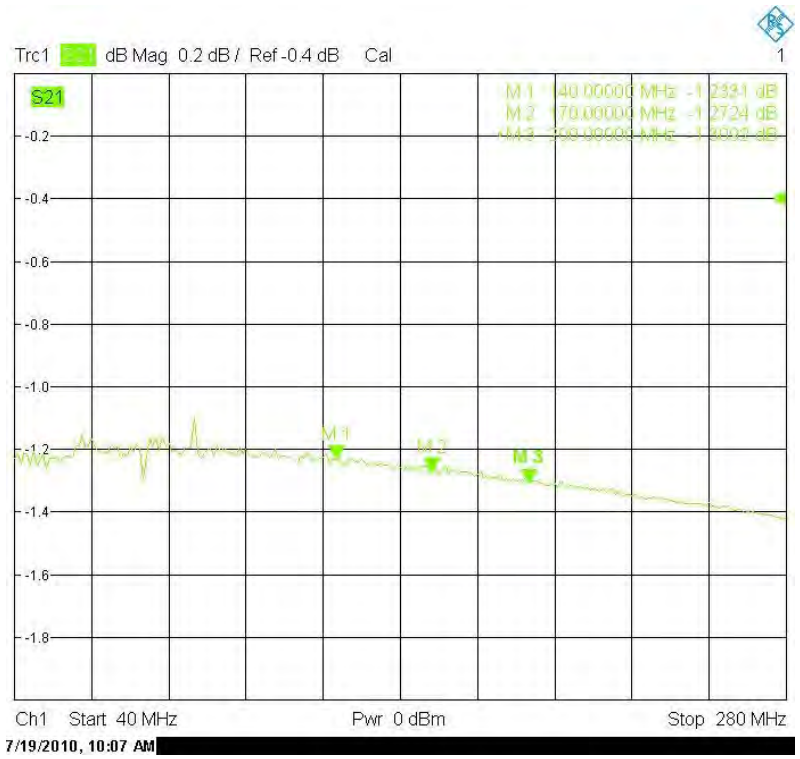
12.3 Calibration EVB picture



12.4 Calibration measurement results



Input Balun, back-to-back



Output Balun, back-to back

The losses of the input balun is about 0.55 dB

The losses of the output balun is about 0.6 dB

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