UG10151

MCXA14x/15x Hardware Design Guide

Rev. 1.0 — 22 August 2024 **User guide**

Document information

Information	Content
Keywords	UG10151, MCX, MCXA14x/15x, MCXA156, MCXA155, MCXA154, MCXA153, MCXA152, MCXA146, MCXA145, MCXA144, MCXA143, MCXA142
Abstract	This document provides guidelines and recommendations for creating hardware designs based on the NXP MCXA14x/15x MCU.

1 Introduction

This document provides guidelines and recommendations for creating hardware designs based on the NXP MCXA14x/15x MCU. It provides guidelines for designing the board schematics and the board layout. It aims to help hardware engineers achieve first-pass success with board design and testing and avoid board bring-up problems.

For relevant device-specific hardware documentation, visit MCX A Series Microcontrollers.

2 MCXA14x/15x family overview

The MCXA14x/15x family is a new NXP general-purpose MCU family that further extends the highly scalable MCU portfolio for industrial and IoT applications. It builds on the legacy LPC and Kinetis families, while introducing higher memory options along with a richer peripheral set.

With support for a voltage range from 1.71 V to 3.6 V and focus on low-power performance, the MCXA14x/15x devices are well suited for a wide range of industrial and IoT applications. The MCXA14x/15x family offers low-pin-count options and is optimized for cost-sensitive applications.

To address varying customer needs, 30+ MCXA14x/15x parts are already available, and more parts are planned for the future. It provides scalability in terms of memory set and performance. Most of these parts are fully pin-to-pin compatible and all of them are software compatible. You can start your hardware design now with already available parts. You get the flexibility to upgrade or downgrade the part in the future within the whole MCXA14x/15x family.

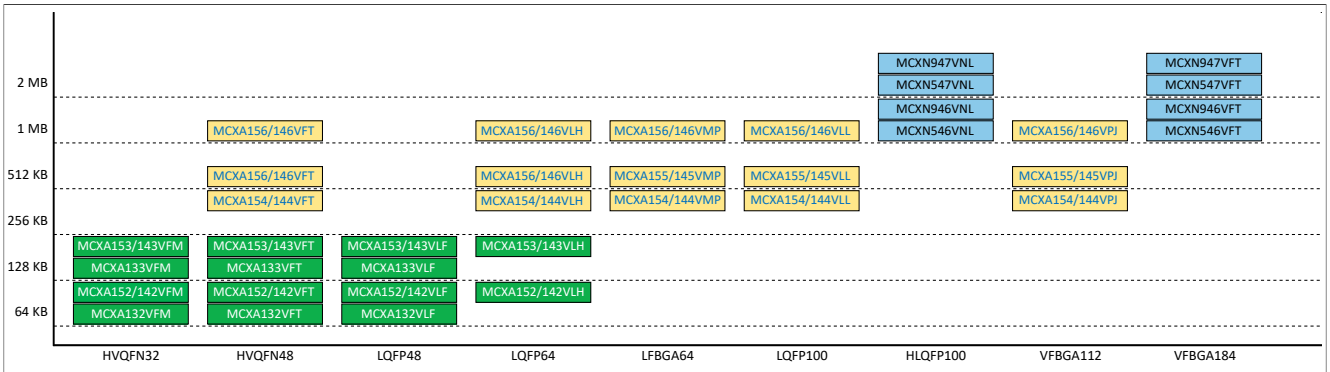

Figure 1. MCXA14x/15x part number scalability

Figure 2 explains how to decode an MCXA14x/15x part number.

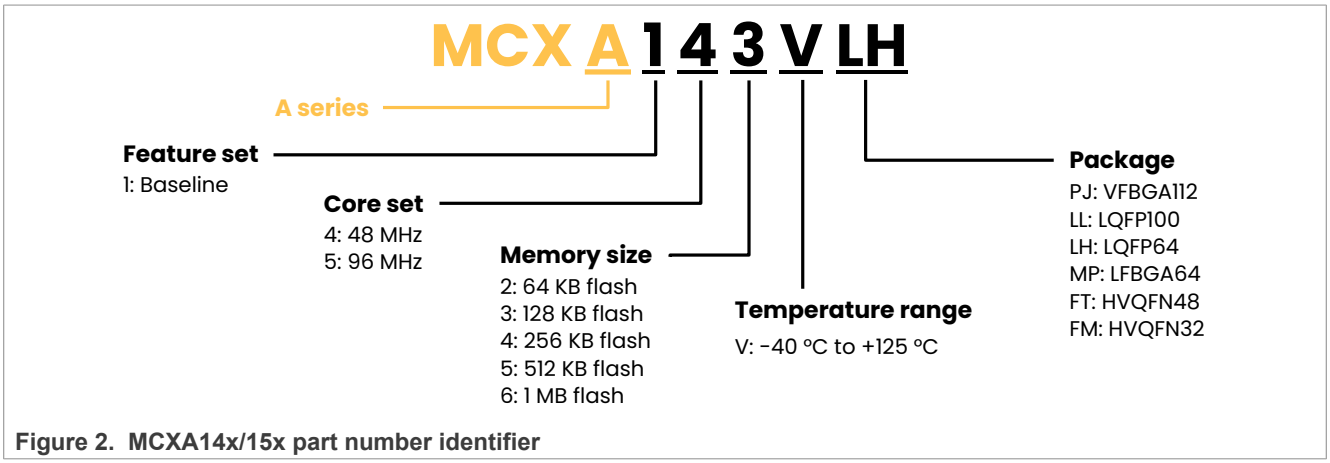

Figure 2. MCXA14x/15x part number identifier

In the MCXA14x/15x part number:

- 'A' indicates the device part number series.
- '1' indicates the baseline feature set, which also indicates that the part is relatively cost effective.
- The next character ('4' or '5') indicates core speed — 48 MHz for MCXA14x and 96 MHz for MCXA15x.
- The next character indicates the memory size, for example, '2' represents 64 KB flash memory.
- 'V' represents a temperature range from -40 °C to 125 °C.
- The last two characters indicate the package option, for example, "PJ" indicates the VFBGA112 package.

2.1 MCXA14x/15x features

The MCXA14x/15x MCU features are summarized below:

- 32-bit Arm Cortex-M33 core, running at speeds of up to 96 MHz
- Scalable memory footprints — up to 1 MB flash memory and up to 128 KB static random-access memory (SRAM)
- High-precision, mixed-signal capability with on-chip analog comparators, 16-bit ADCs, 12-bit DAC, OpAmp, and integrated temperature sensor
- Powerful timers for a broad range of applications, including motor control and lighting control applications
- Serial communication interfaces, such as LPUART, LPSPI, LPI2C, I3C, FlexCAN with CAN FD, and FlexIO
- Operating junction temperature range from -40 °C to +125 °C

Note: *For more details on the MCXA14x/15x MCU features, refer to the MCXA14x/15x data sheet corresponding to the device part.*

The subsections below provide comparisons of features across the MCXA14x/15x family devices.

2.1.1 Core platform

All MCXA14x/15x family devices are based on the Arm Cortex-M33 core with 48 MHz or 96 MHz core frequency. Table 1 compares the core features across the MCXA14x/15x family devices.

Table 1. MCXA14x/15x family core feature comparison

Core feature	MCXA146	MCXA145	MCXA144	MCXA143	MCXA142	MCXA156	MCXA155	MCXA154	MCXA153	MCXA152
Core — Arm Cortex-M33	48 MHz					96 MHz				
Cache	4 KB									
Direct memory access (DMA)	8 channels			4 channels		8 channels			4 channels	
Wake-Up Unit (WUU)	Yes									
Peripheral input multiplexing (INPUTMUX)	Yes									

2.1.2 Clock

Table 2 compares the clock features across the MCXA14x/15x family devices.

Table 2. MCXA14x/15x family clock feature comparison

Clock feature	MCXA146	MCXA145	MCXA144	MCXA143	MCXA142	MCXA156	MCXA155	MCXA154	MCXA153	MCXA152
Fast internal reference clock (FRO192M)	48 MHz					192 MHz				
Slow internal reference clock (FRO12M)	12 MHz									
Low-power internal reference clock (FRO16K)	16.384 kHz									
System oscillator (SOSC)	8–50 MHz									

2.1.3 Memory

Table 3 compares the memory features across the MCXA14x/15x family devices.

Table 3. MCXA14x/15x family memory comparison

Memory	MCXA146	MCXA145	MCXA144	MCXA143	MCXA142	MCXA156	MCXA155	MCXA154	MCXA153	MCXA152
Flash	1024 KB	512 KB	256 KB	128 KB	64 KB	1024 KB	512 KB	256 KB	128 KB	64 KB
SRAM	128 KB including 8 KB with ECC	96 KB including 8 KB with ECC	64 KB including 8 KB with ECC	32 KB including 8 KB with ECC	16 KB including 8 KB with ECC	128 KB including 8 KB with ECC	96 KB including 8 KB with ECC	64 KB including 8 KB with ECC	32 KB including 8 KB with ECC	16 KB including 8 KB with ECC
Error injection module (EIM)	Yes									
Error recording module (ERM)	Yes									

Cache

MCXA14x/15x features 4 KB Low-Power Cache Controller (LPCAC) RAM, which provides low-latency access to the instructions or data. The LPCAC RAM is placed on the core code bus. It can be configured as code tightly coupled memory (TCM) SRAM when LPCAC is disabled.

Flash

MCXA14x/15x features up to 1 MB flash array, which is implemented as a single array. The flash array supports ECC on every 128 bits. It also supports the flash swapping feature. The size of the smallest flash programming phrase is 16 bytes.

The flash subsystem also includes Memory Block Checker (MBC), Flash Memory Controller (FMC), and Flash Memory Module (FMU).

FMC implements a 128-bit entry buffer and a 128-bit prefetch buffer. These buffers allow program code execution at a higher clock frequency than the frequency supported by flash memory. It accelerates flash memory transfers.

SRAM

MCXA14x/15x features up to 128 KB SRAM, which is divided into several SRAM sections, including SRAM X0, X1, A0, A1, A2, A3, B0, B1, and B2. Therefore, different SRAM sections can be retained independently in a low-power mode to reduce power consumption.

On every 32-bit aligned field, the 8 KB SRAM A0 section supports 2-bit error correction code (ECC) detection and 1-bit ECC correction. In addition, for functional safety diagnostic (self-test) purposes, MCXA14x/15x offers the Error Injection Module (EIM). The EIM module can be used to induce artificial errors in the RAM ECC. It can inject single-bit or multi-bit inversions on the data.

To get 128 KB continuous SRAM addressing, the SRAM remap feature can be enabled, by remapping SRAM X0 right after SRAM B2.

2.1.4 Communication interfaces

Table 4 compares the communication interfaces across the MCXA14x/15x family devices.

Table 4. MCXA14x/15x family communication interface comparison

Communication interface	MCXA146	MCXA145	MCXA144	MCXA143	MCXA142	MCXA156	MCXA155	MCXA154	MCXA153	MCXA152
LPUART	5			3		5			3	
LPSPI	2									
LPI2C	4			1		4			1	
I3C	1									
USB FS Device	1									
FlexCAN[1]	1			-		1 (CAN FD)			-	

Table 4. MCXA14x/15x family communication interface comparison...*continued*

Communication interface	MCXA146	MCXA145	MCXA144	MCXA143	MCXA142	MCXA156	MCXA155	MCXA154	MCXA153	MCXA152
Flexible I/O (FlexIO)[2]	1			-		1			-	

[1] MCXA156/A155/A154 supports CAN flexible data rate (CAN FD), which is an important feature for industrial applications.
[2] FlexIO can simulate various communication interfaces, such as UART, I²C, camera, and LCD driver.

2.1.5 Analog modules

Table 5 compares the analog modules across the MCXA14x/15x family devices.

Table 5. MCXA14x/15x family analog module comparison

Analog module	MCXA146	MCXA145	MCXA144	MCXA143	MCXA142	MCXA156	MCXA155	MCXA154	MCXA153	MCXA152
Analog comparator (LPCMP)	2									
ADC	2			1		2			1	
DAC	-					1	1	1	-	
OpAmp	-					1	1	1	-	

For ADC configuration and sample rate calculation, refer to *MCXA14x/15x ADC Usage and Calculator Tool* (AN14390).

2.1.6 Timers

Table 6 compares the motor control timers across the MCXA14x/15x family devices.

Table 6. MCXA14x/15x family motor control timer comparison

Motor control timer	MCXA146	MCXA145	MCXA144	MCXA143	MCXA142	MCXA156	MCXA155	MCXA154	MCXA153	MCXA152
FlexPWM[1][2]	1					2			1	
AND/OR/INVERT (AOI)	2			1		2			1	
Quadrature Decoder (eQDC)[3]	1					2			1	

[1] FlexPWM0 is available in all MCXA14x/15x devices, whereas FlexPWM1 is only available in MCXA156/A155/A154.
[2] Each FlexPWM module has three submodules.
[3] QDC0 is available in all MCXA14x/15x devices, whereas QDC1 is only available in MCXA156/A155/A154.

Table 7 compares the general-purpose timers across the MCXA14x/15x family devices.

Table 7. MCXA14x/15x family general-purpose timer comparison

General-purpose timer	MCXA146	MCXA145	MCXA144	MCXA143	MCXA142	MCXA156	MCXA155	MCXA154	MCXA153	MCXA152
32-bit timer (CTimer)	5			3		5			3	
Low-Power Timer (LPTMR)	1									
Micro-Tick Timer (UTICK)	1									
OS Event Timer (OSTIMER)	1									
Windowed Watchdog Timer (WWDT)	1									
Frequency Measurement (FREQME)	1									
Wake Timer	1									

2.1.7 GPIOs

Table 8 compares the inputs/outputs (I/Os) across the MCXA14x/15x family devices.

Table 8. MCXA14x/15x family I/O comparison

I/O	MCXA146	MCXA145	MCXA144	MCXA143	MCXA142	MCXA156	MCXA155	MCXA154	MCXA153	MCXA152
Independent I/O supply[1]	VDD_P3			-		VDD_P3			-	
5 V tolerant I/O[2]	2									
High-drive I/O (20 mA)[3]	Up to 8									
50 MHz I/O[4]	Up to 21									

[1] MCXA146/MCXA145/MCXA144/MCXA156/MCXA155/MCXA154 supports 1.2 V I/O power supply on P3 port.
[2] The P3_27 and P3_28 pins are 5 V tolerant I/Os.
[3] The P0_16, P0_17, P1_8, P1_9, P1_30, P1_31, P3_0, and P3_1 pins are high-drive I/Os.
[4] 50 MHz I/Os are available on P1, P3, and P4 ports.

Table 9 shows the number of general-purpose inputs/outputs (GPIOs) available in different packages of the MCXA14x/15x family devices.

Table 9. MCXA14x/15x family GPIO comparison

Package	Number of GPIOs									
	MCXA146	MCXA145	MCXA144	MCXA143	MCXA142	MCXA156	MCXA155	MCXA154	MCXA153	MCXA152
VFBGA112 (PJ)	82			-		82			-	
LQFP100 (LL)	81			-		81			-	
LQFP64 (LH)	-			52		-			52	
LFBGA64 (MP)	50			-		50			-	
HVQFN48 (FT)	-			41		-			41	
HVQFN32 (FM)	-			26		-			26	

2.2 Package options

The MCXA14x/15x devices are available in different package options, including:

- Traditional leaded packages (QFP) and non-leaded packages (QFN)
- Advanced ball grid array (BGA) packages

The variety of package options help customers achieve reliable mechanical and thermal performance for their hardware designs.

Table 10 shows the package options available for the MCXA14x/15x devices.

Table 10. MCXA14x/15x package options

Package	Pin count	Number of GPIOs	Dimensions (length x width x thickness)	Pitch	Package drawing document number
VFBGA112 (PJ)	112	82	7 x 7 x 0.86 mm	0.5 mm	98ASA02081D
LQFP100 (LL)	100	81	14 x 14 x 1.4 mm	0.5 mm	98ASS23308W
LQFP64 (LH)	64	52	10 x 10 x 1.4 mm	0.5 mm	98ASS23234W
LFBGA64 (MP)	64	50	5 x 5 x 1.2 mm	0.5 mm	98ASA02085D
HVQFN48 (FT)	48	41	7 x 7 x 0.9 mm	0.5 mm	98ASA01637D
HVQFN32 (FM)	32	26	5 x 5 x 0.9 mm	0.5 mm	98ASA02110D

As shown in Table 10, the MCXA14x/15x devices are available in packages with pin count as low as 32 (HVQFN32) to as high as 112 (VFBGA112). The low-pin-count packages allow the devices to be used for simple, low-cost PCB designs.

2.2.1 BGA packages

Ball grid array (BGA) is a popular packaging option for devices with high I/O requirements, especially for devices used in small form factor designs. The MCXA14x/15x device is available in the following two BGA packages:

- Very thin, fine pitch, ball grid array (VFBGA112)
- Low-profile, fine pitch, ball grid array (LFBGA64)

Figure 3 shows the MCXA156 device in a 5x5 mm, 0.5 mm pitch LFBGA64 package.

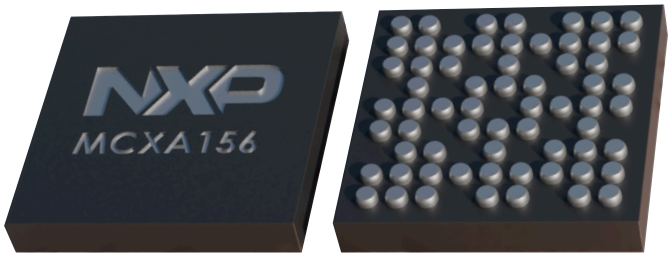

Figure 3. MCXA156 device in 5x5 mm, 0.5 mm pitch LFBGA64 package

The ball pattern has been designed in such a manner that vias can be placed in the depopulated regions for easier fanout. The VDD and VSS signals are grouped conveniently, providing several options for fanning out the chip without requiring the via-in-pad technology. The MCXA14x/15x device in the LFBGA64 package can be used easily with low-cost 2-layer technology. Figure 4 shows an example layout for the MCXA14x/15x device in the LFBGA64 package.

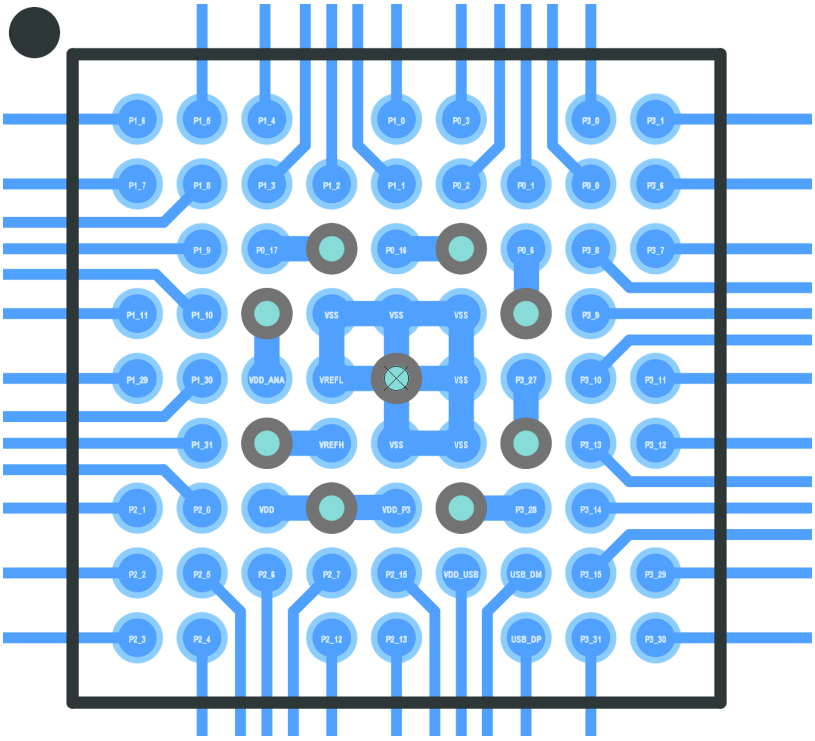

Figure 4. Example MCXA14x/15x LFBGA64 layout

2.2.2 LQFP packages

A low-profile, quad flat package (LQFP) is a QFP package with reduced body thickness. The MCXA14x/15x device is available in the following two LQFP packages:

- LQFP100
- LQFP64

An MCXA14x/15x LQFP package does not have an exposed pad underneath the package that could act as a ground connection and/or heat sink.

2.2.3 HVQFN packages

A heat sink, very thin, quad flat package, non-leaded (HVQFN) is equipped with electrode contacts (instead of leads) around all four sides of the chip. It allows an HVQFN package to have a smaller mounting area and lower height, as compared to a QFP package. An exposed thermal pad on the bottom side of a QFN package can be soldered directly to the system PCB to increase heat emission from the die.

The MCXA14x/15x device is available in the following two HVQFN packages:

- HVQFN48
- HVQFN32

The MCXA14x/15x HVQFN48 package has some inner exposed leads, as shown in Figure 5. While designing the hardware, do not solder these exposed leads to the PCB. Cover this area with solder mask for easier signal routing.

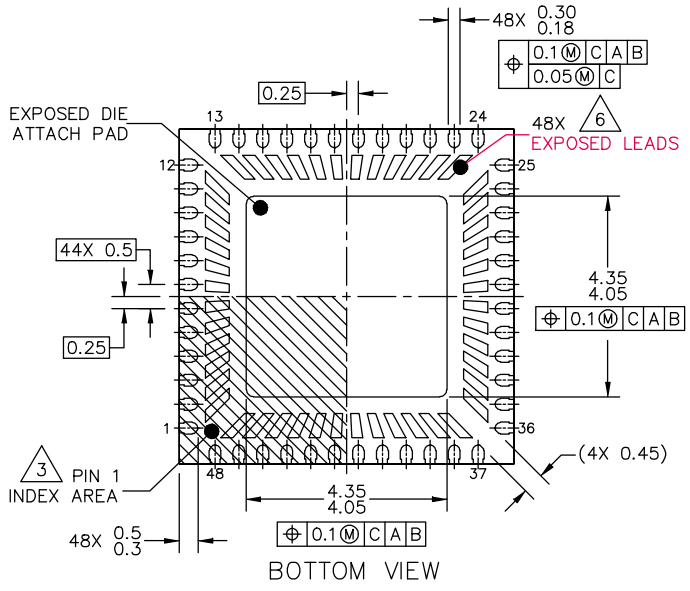

Figure 5. MCXA14x/15x HVQFN48 package drawing

To find a package drawing, go to nxp.com and perform a search operation using the package drawing document number as the search keyword. To find the document number of a package drawing, see Table 10.

2.3 Pin compatibility

The MCXA14x/15x family devices are mostly pin-to-pin compatible except for a few pins, such as ISP (ISPMODE_N). The ISP pin determines whether to boot from the internal flash memory or to run into ISP mode, after reset.

Table 11 compares the ISP pin assignment across the MCXA14x/15x family devices.

Table 11. MCXA14x/15x family ISP pin assignment comparison

Package	ISP pin assignment									
	MCXA146	MCXA145	MCXA144	MCXA143	MCXA142	MCXA156	MCXA155	MCXA154	MCXA153	MCXA152
VFBGA112 (PJ)	P0_6			-		P0_6			-	
LQFP100 (LL)	P0_6			-		P0_6			-	
LFBGA64 (MP)	P0_6			-		P0_6			-	
LQFP64 (LH)	P3_29									
HVQFN48 (FT)	P3_29									
HVQFN32 (FM)	-			P3_29		-			P3_29	

3 Minimum system

While designing the hardware, one of the initial steps is to determine the minimum system components required to run the MCU. For the MCXA14x/15x family devices, the key system components include reset, ISP, debug, power, and optionally, clock.

The state of the ISP pin at reset determines the boot source of the MCXA14x/15x MCU. If the ISP pin is pulled down, the MCU enters ISP boot mode; otherwise, it boots from the internal flash memory.

Figure 6 shows the minimum system for an MCXA14x/15x device.

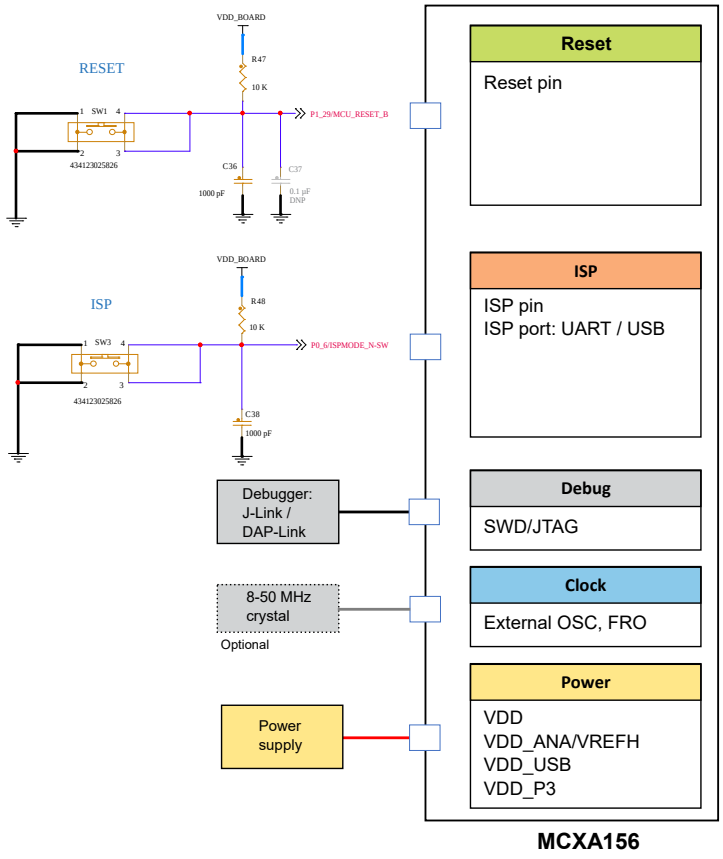

Figure 6. MCXA14x/15x minimum system

4 Power supplies

MCXA14x/15x operates in the power supply range from 1.71 V to 3.6 V. It has multiple power domains that can be put into different power modes independent of each other, for power efficiency. Multiple power supplies are available to supply power to the power domains and I/O ports. Figure 7 shows the MCXA14x/15x power supply scheme.

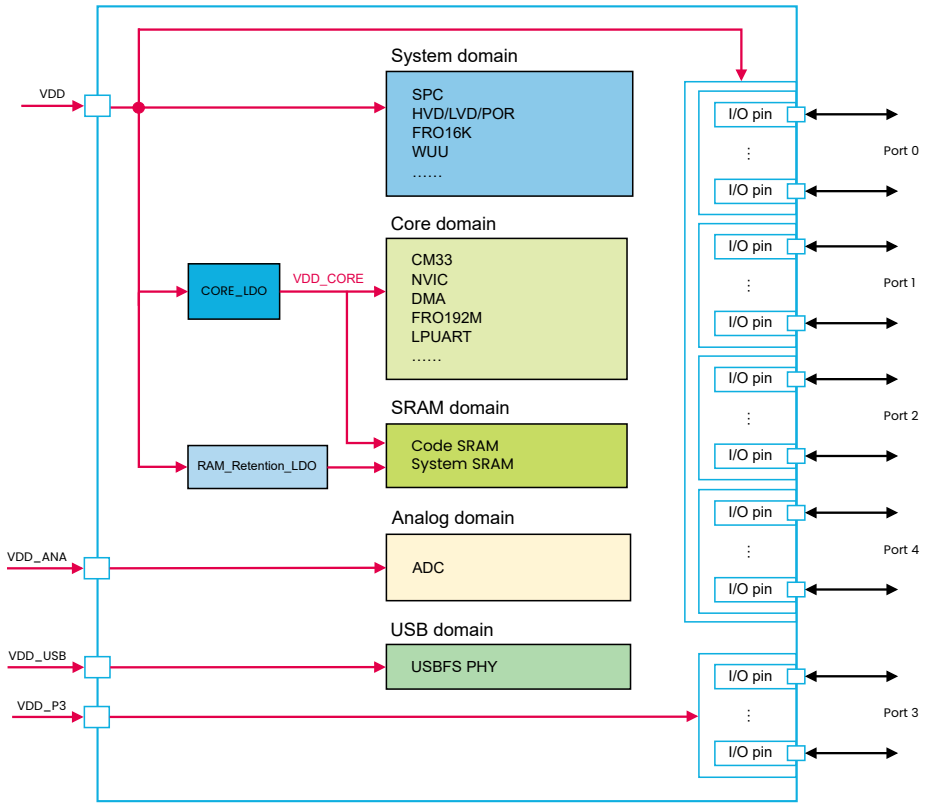

Figure 7. MCXA14x/15x power supply scheme

The input power supplies shown in Figure 7 are explained below:

- Digital power supply (VDD): The VDD supply is used for the following purposes:
  - It supplies power to the system power domain and I/O ports except port 3. The system power domain mainly includes System Power Control (SPC), High-Voltage Detect (HVD) / Low-Voltage Detect (LVD), Wake-Up Unit (WUU), and Low-Power Timer (LPTMR).
  - It supplies power to the core power domain through an internal LDO. The core power domain supports the dynamic voltage and frequency scaling (DVFS) feature. This feature allows you to scale up/down the voltage depending on the desired MCU core frequency. For example, if you want to run the core clock at the maximum frequency (96 MHz), the core voltage must be kept at 1.1 V. However, if your application can tolerate running at a lower frequency (even for a short period), decrease the core voltage. Decreasing the core voltage reduces the power consumption.
- Analog power supply (VDD_ANA): The VDD_ANA supply is used to power up the analog power domain, including the ADC module. Usually in hardware designs, VDD_ANA is connected to VDD. If you want to improve ADC accuracy, you can use an independent power supply to power up VDD_ANA. However, ensure that the voltage difference between VDD_ANA and VDD is within ±0.1 V, as specified in the MCXA14x/15x data sheets.

- USB power supply (VDD_USB): The VDD_USB supply is used to power up the USB domain. For VDD_USB, the voltage must be kept within the range from 3 V to 3.6 V. If the USB domain is not used, VDD_USB can be tied to the ground through a 10 kΩ resistor.
- Optional (independent) port 3 power supply (VDD_P3): On some MCXA14x/15x parts, an independent power supply VDD_P3 is used to power up I/O port 3 for 1.2 V I/Os. VDD_P3 operates in the voltage range from 1.14 V to 3.6 V.

4.1 Bulk and decoupling capacitors

Bulk and decoupling capacitors help the MCU chip operate properly:

- A bulk capacitor is used to provide a local power supply to an MCU pin.
- A decoupling capacitor, if shorted to the ground, helps in preventing noise from entering into the MCU chip.

Figure 8 shows an example circuit diagram with bulk and decoupling capacitors.

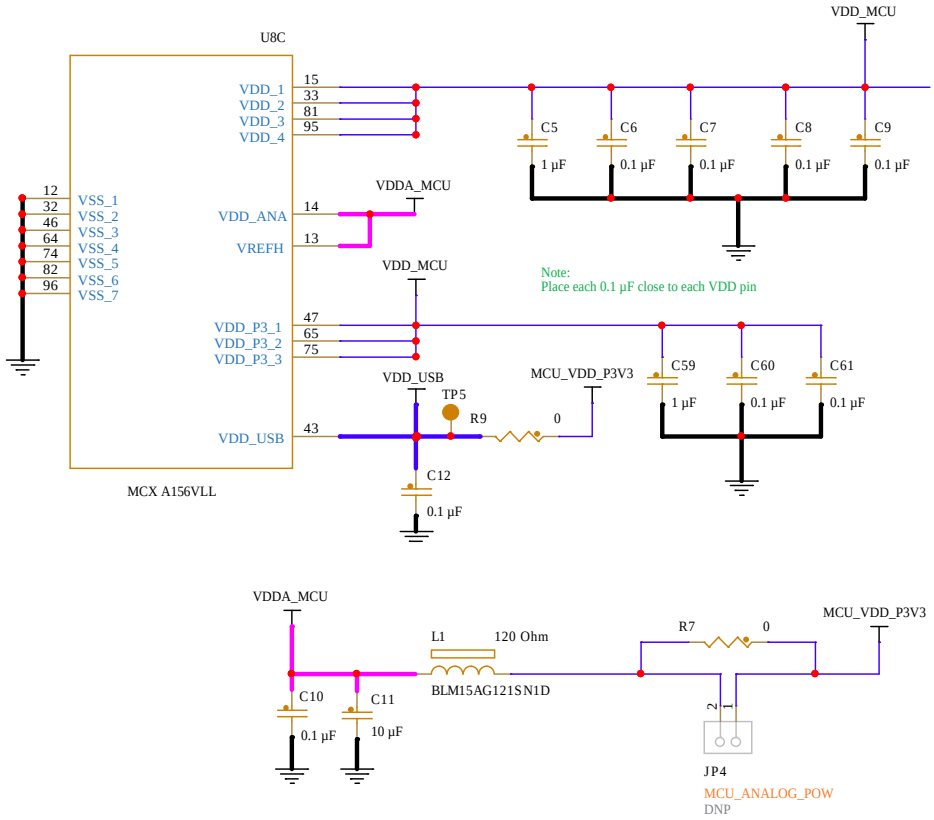

Figure 8. Bulk and decoupling capacitors

Follow these recommendations when using bulk and decoupling capacitors in your hardware design:

- Use decoupling capacitors that exhibit low reactance in the desired frequency ranges.
- For each power pin, use a decoupling capacitor with a capacitance value of 0.1 µF.
- For each power domain, use a bulk capacitor with a capacitance value in the range from 2.2 µF to 10 µF.
- Place the decoupling and bulk capacitors as near as possible to their respective MCU pins.

4.2 Power supply considerations

While designing the hardware, follow these power supply considerations:

- The VDD_ANA supply must be at the same voltage level as the VDD supply, and both supplies must be ramped up together.
- The VDD_P3 supply (I/O supply of port 3) must be ramp up together with or after VDD. If you want to shut down VDD_P3, assert the isolation in the SPC EVD_CFG register before shutting down VDD_P3 in active mode.

5 Clock

The MCXA14x/15x MCU includes an external oscillator module — a system oscillator (SOSC) with an external 8–50 MHz crystal. Figure 9 shows an example system oscillator circuit diagram.

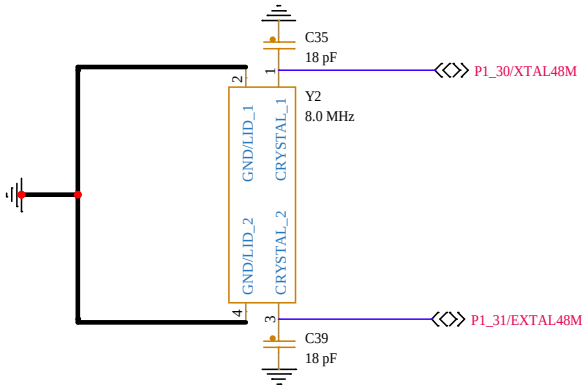

Figure 9. Example SOSC circuit diagram

6 Debug and programming interface

This section contains the following subsections:

- Section 6.1 "Reset system"
- Section 6.2 "JTAG/SWD interface"
- Section 6.3 "ISP programming"

6.1 Reset system

Resetting the MCU provides a way to start processing from a known set of initial conditions. When a system reset begins:

- The on-chip regulator gets full control over the power supplies
- The system clock gets generated from an internal reference clock

6.1.1 External reset pin (RESET_B)

The RESET_B pin is a bidirectional open-drain pin with an internal pull-up resistor. Asserting RESET_B wakes the MCU from any mode. In MCXA14x/15x, the RESET_B function is multiplexed on the GPIO pin P1_29, and this function is the default function of the pin.

The RESET_B pin works in the following two manners:

- During active and low-power modes, the RESET_B pin can be asserted externally to force the chip into pin reset condition.

- During reset, the RESET_B pin drives low until the chip has completed hardware initialization. At this point, the RESET_B pin is released. If the pin is asserted externally, the MCU remains in reset until the RESET_B input is pulled high.

The RESET_B pin implements a digital filter for filtering out glitches from the pin. You can configure the filter through software to filter out glitches that are less than 1–32 cycles of the Core Mode Controller (CMC) clock. The filter is bypassed in low-power modes, if the CMC clock is disabled.

6.2 JTAG/SWD interface

The MCXA14x/15x MCU supports a JTAG / serial wire debug (SWD) debug interface using a low-cost, 10-pin, 0.05" connector. Because the connector supports both JTAG and SWD signals; therefore, you can configure an external debugger in either JTAG or SWD mode to debug an MCXA14x/15x MCU. The JTAG/SWD connector offers Instruction Trace Macrocell (ITM) and Data Watchpoint and Trace (DWT) trace information.

In SWD mode, the following two pins are used for debugging:

- Bidirectional SWDIO pin, which is used for data transfer
- SWDCLK pin, which is used for clocking the data

A third pin SWO delivers the trace data at a low system cost. The JTAG and SWD pins are shared.

Table 12 shows the MCXA14x/15x debug pin assignments.

Table 12. MCXA14x/15x debug pin assignments

Signal name		Description	MCU port	Internal pull resistor
JTAG mode	SWD mode			
TCK	SWDCLK	Clock into the core	P0_1	Pull-down
TDI	-	JTAG test data input	P0_3	Pull-up
TDO	SWO	JTAG test data output / serial wire debug trace data output	P0_2	-
TMS	SWDIO	JTAG test mode select / serial wire debug data I/O	P0_0	Pull-up
RESET	RESET	Reset MCU	P1_29	Pull-up
GND	GND	Ground	VSS	-

As shown in Table 12, the MCXA14x/15x debug pins have internal pull-up/down resistors, by default. To make the debugger connection more robust, you can add external pull-up/down resistors for the JTAG/SWD signals. NXP also recommends adding electrostatic discharge (ESD) diodes for critical pin connections.

Figure 10 shows an example debug interface circuit diagram.

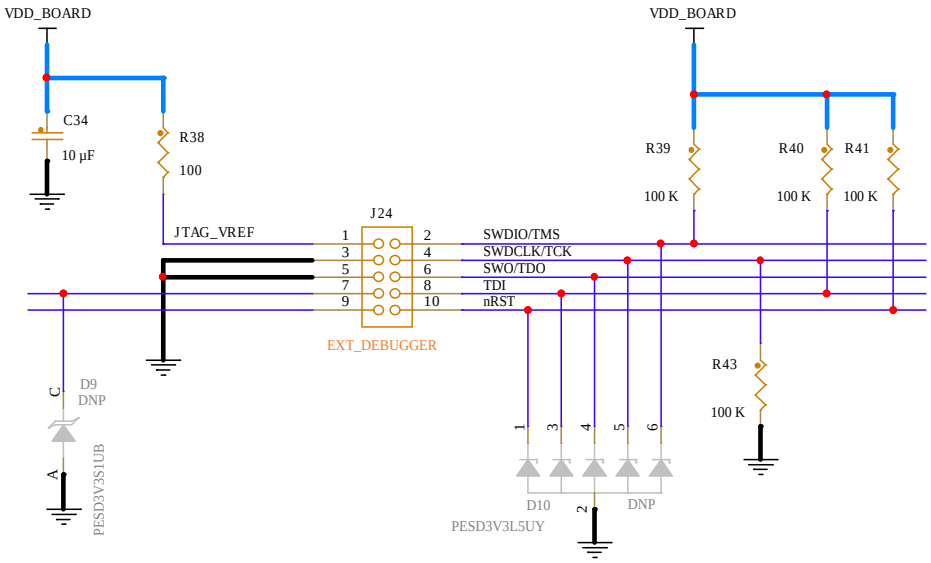

Figure 10. JTAG/SWD interface circuit diagram

MCXA14x/15x also allows using JTAG and boundary scan for performing probe-less device connectivity test. For details, refer to *How To Perform Boundary Scan On MCXA Series Using µTrace And Trace32* (AN14209).

6.3 ISP programming

Besides an external JTAG/SWD debugger, you can also use in-system programming (ISP) to program the MCXA14x/15x MCU. During MCU reset, the state of the MCU ISP pin (ISPMODE_N) determines whether to enter normal boot flow or enter ISP mode. In ISP mode, you can program the MCU through the ISP boot peripherals.

Depending on the device part, the default ISP pin is P0_6 or P3_29. For more details on ISP pin assignment, see Table 11.

Table 13 shows the default ISP boot peripherals and corresponding pin assignments.

Table 13. MCXA14x/15x ISP boot peripherals

ISP boot peripheral	Signal name	MCU pin
LPUART0	LPUART0_RXD	P0_2
	LPUART0_TXD	P0_3
USB0	USB0_DM	USB0_DM
	USB0_DP	USB0_DP

Figure 11 shows an example circuit diagram for the MCXA156 MCU with an ISP push button SW3 for entering ISP mode. Pressing the ISP button asserts the MCXA156 MCU pin P0_6 (ISPMODE_N), which forces the MCU extended bootloader to run in ISP mode.

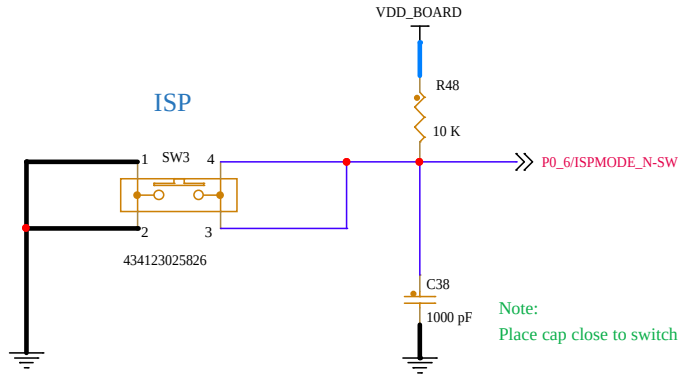

Figure 11. ISP button circuit diagram

7 Unused pins

Table 14 provides recommendations for terminating the unused pins of the MCXA14x/15x MCU.

Table 14. Recommendations for terminating unused pins

Pins	Default state	Recommended way for terminating unused pins
Digital/analog pins	Disabled	Leave unconnected. Configuring the multiplexing mode of a pin as disabled or analog (PCRn[MUX] = 0) disables the input buffer of the pin. It results in reduced power consumption.
P1_29/RESET_B	Input with default internal pull-up resistor	If the RESET_B pin is not used, it can be left unconnected and: • Configured as GPIO by setting PCR9[MUX] = 0 • Disabled by setting PCR9[IBE] = 0
P3_29/ISPMODE_N, P0_6/ISPMODE_N	Input with default internal pull-up resistor	Leave unconnected. Configuring the multiplexing mode of a pin as disabled or analog (PCRn[MUX] = 0) disables the input buffer of the pin. It results in reduced power consumption.
P1_30/XTAL48M, P1_31/EXTAL48M	Disabled	Leave unconnected
VDD_USB		Tie the unused VDD_USB pin to the ground through a 10 kΩ resistor.
USB_DP		Leave unconnected
USB_DM		Leave unconnected

8 EMC recommendations

To find electromagnetic compatibility (EMC) recommendations for the MCXA14x/15x family devices, refer to *EMC Guidelines for MCXA14x/15x MCU Designs* (AN14395).

9 References

Following are some additional documents that you can refer to for more information on the MCXA14x/15x family devices:

- *MCXA156, A155, A154, A146, A145, A144 Data Sheet* (MCXAP100M96FS6)
- *MCXA156, A155, A154, A146, A145, A144 Reference Manual* (MCXAP100M96FS6RM)
- *MCXA153, A152, A143, A142 Data Sheet* (MCXAP64M96FS3)
- *MCX A153, A152, A143, A142 Reference Manual* (MCXAP64M96FS3RM)
- *FRDM-MCXA156 Board User Manual* (UM12121)
- *FRDM-MCXA153 Board User Manual* (UM12012)
- *EMC Guidelines for MCXA14x/15x MCU Designs* (AN14395)
- *MCXNx4x Hardware Design Guide* (UG10092)
- *MCXA14x/15x ADC Usage and Calculator Tool* (AN14390)
- *Hardware Design Guidelines for LPC55(S)xx Microcontrollers* (AN13033)
- *How To Perform Boundary Scan On MCXA Series Using µTrace And Trace32* (AN14209)
- *MCX A Series: The All-Purpose MCU for Embedded Innovation* White Paper

Note: *Some of these documents may only be available under a non-disclosure agreement (NDA). To access such a document, contact a local NXP field applications engineer (FAE) or sales representative.*

10 Acronyms

Table 15 lists the acronyms used in this document.

Table 15. Acronyms

Acronym	Description
ADC	Analog-to-Digital Converter
AOI	AND/OR/INVERT
BGA	Ball grid array
CAN	Controller Area Network
CMC	Core Mode Controller
DAC	Digital-to-Analog Converter
DMA	Direct memory access
DVFS	Dynamic voltage and frequency scaling
DWT	Data Watchpoint and Trace
ECC	Error correction code
EIM	Error Injection Module
EMC	Electromagnetic compatibility
ERM	Error recording module
ESD	Electrostatic discharge
FD	Flexible data rate
FlexCAN	Flexible Data Rate Controller Area Network
FlexIO	Flexible Input/Output
FlexPWM	Flexible Pulse Width Modulator
FMC	Flash Memory Controller
FMU	Flash Memory Module
FS	Full speed

Table 15. Acronyms...*continued*

Acronym	Description
GPIO	General-purpose input/output
HVD	High-Voltage Detect
HVQFN	Heat sink, very thin, quad flat package, non-leaded
I/O	Input/output
I^2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
ISP	In-system programming
ITM	Instruction Trace Macrocell
JTAG	Joint Test Action Group
LCD	Liquid-crystal display
LFBGA	Low-profile, fine pitch, ball grid array
LPCAC	Low-Power Cache Controller
LPI2C	Low-Power Inter-Integrated Circuit
LPSPI	Low-Power Serial Peripheral Interface
LPUART	Low-Power Universal Asynchronous Receiver/Transmitter
LQFP	Low-profile, quad flat package
LVD	Low-Voltage Detect
MBC	Memory Block Checker
MCU	Microcontroller unit
OpAmp	Operational amplifier
OS	Operating system
QDC	Quadrature Decoder
QFN	Quad flat package, non-leaded
QFP	Quad flat package
RAM	Random-access memory
SOSC	System oscillator
SPC	System Power Control
SRAM	Static random-access memory
SWD	Serial wire debug
SWO	Serial wire debug trace data output
TCM	Tightly coupled memory
TDI	Test data input
TDO	Test data output
TMS	Test mode select
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Table 15. Acronyms...*continued*

Acronym	Description
VFBGA	Very thin, fine pitch, ball grid array
WUU	Wake-Up Unit

11 Revision history

Table 16 summarizes the revisions to this document.

Table 16. Revision history

Document ID	Release date	Description
UG10151 v.1.0	22 August 2024	Initial public release

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