QorIQ T4240 Reference Design Board User Guide

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Chapter 1
Introduction

The The QorIQ T4240 reference design board (T4240RDB) is a flexible system that supports a 24-virtual core T4240 processor. The T4240RDB main board is mounted in a 1U rack-mounted chassis. The T4240 supports clocking configuration flexibility for frequent configuration modifications. Two expansion slots are also provided for the addition of standard PCIe expansion cards. The T4240RDB comes with a Linux® board support package (BSP) that provides a comprehensive starting point for Linux development efforts.

The part no. of the T4240 reference design board (RDB) system is T4240RDB-16GPA (for a board based upon T4240 Rev 1.0 silicon) and T4240RDB-PB (for a board based upon T4240 Rev 2.0 silicon).

This document is applicable for PCBA Rev 4.0 and PLD Rev 4.1. The revision information is available in the U-Boot log.

1.1 Related documentation

Some of the documents below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1-1. Related documentation

Document name	Description
T4240 QorIQ Integrated Multicore Communications Processor Family Reference Manual (document T4240RM)	Provides details about the features and functionalities of the T4240 QorIQ Integrated Multicore Communications Processor Family. Link: http://www.nxp.com/products/microcontrollers-and-processors/power-architecture-processors/qoriq-power-architecture-processors/qoriq-t4240-t4160-t4080-multicore-communications-processors:T4240?fpsp=1&tab=Documentation_Tab

Table continues on the next page...

Table 1-1. Related documentation (continued)

Document name	Description
T4240 QorIQ Integrated Multicore Communications Processor Family Data Sheet (document T4240)	Provides specific data regarding DC characteristics, power sequencing, input clocks, interfaces, as well as other design considerations. Link: http://www.nxp.com/products/microcontrollers-and-processors/power-architecture-processors/qoriq-power-architecture-processors/qoriq-t4240-t4160-t4080-multicore-communications-processors:T4240?fpsp=1&tab=Documentation_Tab
QorIQ T4240 Reference Design Board Quick Start (document T4240RDBQS)	Provides information about the features of the T4240 Reference Design Board. Link: http://www.nxp.com/products/microcontrollers-and-processors/power-architecture-processors/qoriq-power-architecture-processors/qoriq-t4240-reference-design-board:T4240RDB?fpsp=1&tab=Documentation_Tab
QorIQ SDK 1.9 Documentation	Provides detailed information about the Freescale Linux-Oriented Software Development Kit. Link: https://freescale.sdlproducts.com/LiveContent/content/en-US/QorIQ_SDK_1.9

1.2 Acronyms and abbreviations

Table 1-2. Acronyms and abbreviations

Usage	Description
ATX	Advanced Technology eXtended
AVD	Address Valid Signal
COP	Common On-chip Processor
CTS	Clear-to-send
DDR	Double Data Rate
DIMM	Dual In-line Memory Module
DUART	Dual Universal Asynchronous Receiver-Transmitter
ECC	Error Checking and Correction
EPPROM	Electrically Erasable Programmable Read-Only Memory
eSDHC	Enhanced SD Host Controller
eSPI	Enhanced Serial peripheral interface
IEEE	Institute of Electrical and Electronic Engineers
IFC	Integrated Flash Controller
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
L2	Level 2 caching
LED	Light-Emitting Diode

Table continues on the next page...

Table 1-2. Acronyms and abbreviations (continued)

Usage	Description
MDIO	Management Data Input/Output
PCIe	Peripheral Component Interconnect Express
PHY	Physical Layer
PLD	Programmable Logic Device
POR	Power-On Reset
RDIMM	Registered DIMM
RJ45	Registered Jack-45
RS	Series Resistor
RT	Termination Resistor
RTS	Ready-to-send
SATA	SerialATA
SD	Secure Digital
SDRAM	Synchronous DRAM
SerDes	Serializer/Deserializer
SFP	Small Form-factor Pluggable
SGMII	Serial Gigabit Media Independent Interface
SLC	Single-Level Cell
SoC	System-on-a-chip
SPD	Serial presence detect
SSTL	Stub Series Terminated Logic
UART	Universal Asynchronous Receiver-Transmitter
UDIMM	Unbuffered DIMM
USB	Universal Serial Bus

Chapter 2
T4240RDB Hardware

This section covers the features, block diagram, specifications, and mechanical data of the RDB.

2.1 T4240RDB features

The board features are as follows:

- Freescale QorIQ T4240 communications processor with 24-virtual cores running at 1.8 GHz
  - 12 e6500 cores built on Power Architecture® technology and arranged as clusters of four e6500 cores each sharing a 2 MB L2 cache
- Memory subsystem:
  - SDRAM
    - 3 DIMM slots, supports 2 GB per DIMM
    - Supports DDR3 1866 UDIMM/RDIMM
  - NOR flash memory
    - 128 MB, 16-bit width NOR flash memory
  - NAND flash memory
    - 2 GB SLC NAND flash, MICRON:MT29F16G08ABABAWP:B
    - 2 Kbit 24C02 I2C EEPROM
    - SD connector to interface
- PCIe:
  - PCIe x4 connector
  - PCIe x8 connector
- USB 2.0:
  - One dual USB slot, connected to USB PHY, Type A Host mode
- Networking subsystem:
  - 10G PHY 4-port SFP+Cortina CS4340
  - 1G PHY SGMII, two Vitesse VSC8664
- Ethernet interfaces
  - ETH0 - ETH7: Connected to SGMII PHY - VSC8664
  - ETH8 - ETH11: Connected to XFI Quad SFP+ PHY CS4340

NOTE

For Rev 1.0 silicon, two 10 Gbit /s (ETH10, ETH11) ports are not working, however other two 10 Gbit /s (ETH8, ETH9) ports are working fine.

- UART:
  - UART interface: supports two UARTs up to 115200 bit/s for console display; dual RJ45 slot is used for the two UART ports
- Transceiver (SFP+)
  - Finisar's FTLX8571D3BCL 10 Gbit/s SFP+ optical transceiver (as shown in Figure A-1)
- Miscellaneous:
  - LED:
    - Power LED (green indicates power ON; yellow indicates stand by)
    - Link LED (green indicates 1 Gbit/s and yellow indicates 10/100 Mbit/s) on each RJ-45 ethernet connector
    - Active LED (green) on each RJ45 Ethernet connector
  - JTAG for debugging
  - Reset: hardware reset
  - One Serial ATA (SATA 2.0) controller
  - Enhanced secure digital host controller (eSDHC)
  - Enhanced Serial peripheral interface (eSPI)
  - Three I2C controllers
  - Two 4-pin DUARTs
  - Power
    - ATX power supply, 300 W

Figure 2-1 shows a high-level block diagram of the T4240RDB board.

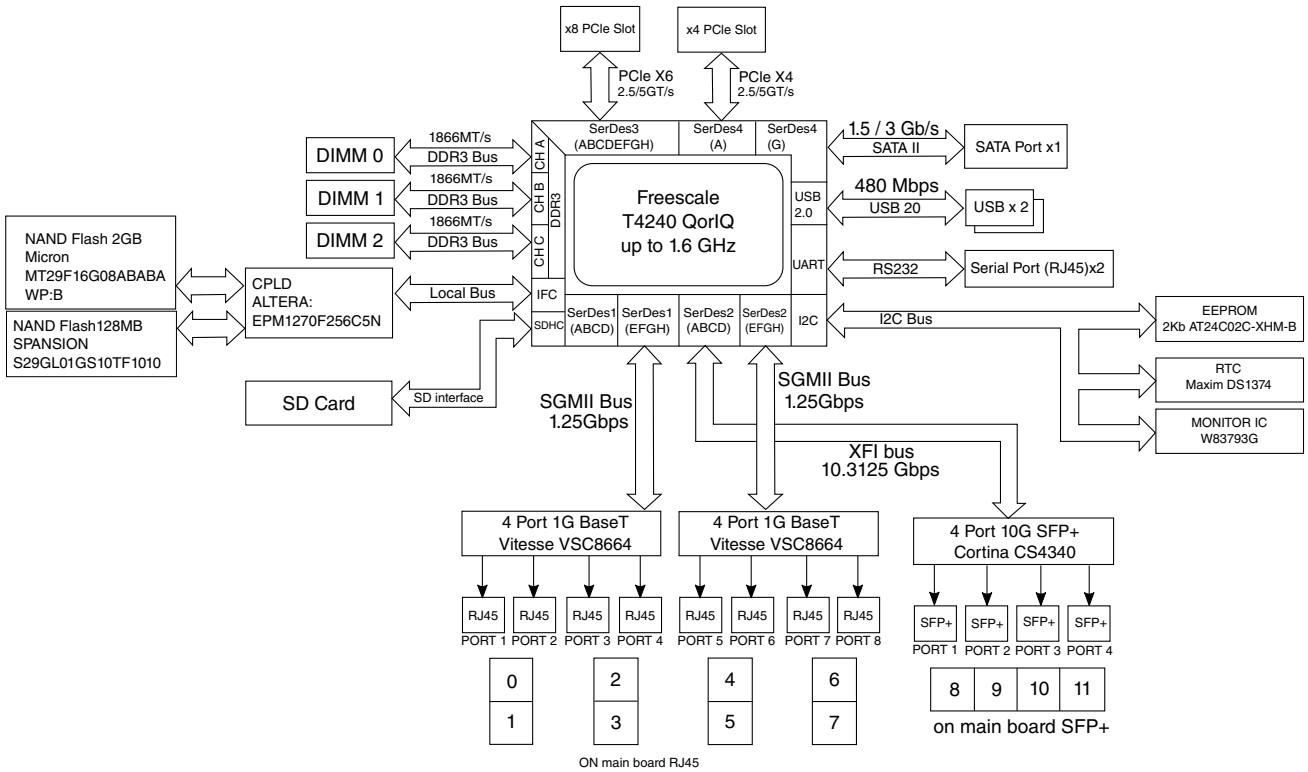


Figure 2-1. T4240RDB block diagram

2.2 Specifications

The table below lists the specifications for the T4240RDB board.

Table 2-1. T4240RDB specifications

Characteristics	Specifications
Chassis power requirements	ATX power supply: 300 W
Communication processor	Freescale QorIQ T4240
Operating temperature	0° C to 70° C (room temperature)
Storage temperature	–25° C to 85° C
Relative humidity	5% to 90% (noncondensing)

Chapter 3
Memory Interface

The three fully programmable DDR SDRAM controllers support most JEDEC standards x4, x8, x16, or x32 DDR3 memories available. Only x32 DRAMs that use 1 data strobe per data byte are supported. In addition, unbuffered and registered DIMMs are also supported. However, mixing different memory types or unbuffered and registered DIMMs in the same system is not supported. Built-in error checking and correction (ECC) ensures very low bit-error rates for reliable high-frequency operation. Dynamic power management and auto-precharge modes simplify the memory system design.

Table 3-1. Supported DDR3 SDRAM device configurations

SDRAM device	Device configuration	Row x Column x Subbank bits	64-Bit bank size	Three banks of memory
512 Mbit/s	128 Mbit/s x 4	13 x 11 x 3	1 GB	4 GB
512 Mbit/s	64 Mbit/s x 8	13 x 10 x 3	512 MB	2 GB
512 Mbit/s	32 Mbit/s x 16	12 x 10 x 3	256 MB	1 GB
1 Gbit/s	256 Mbit/s x 4	14 x 11 x 3	2 GB	8 GB
1 Gbit/s	128 Mbit/s x 8	14 x 10 x 3	1 GB	4 GB
1 Gbit/s	64 Mbit/s x 16	13 x 10 x 3	512 MB	2 GB
2 Gbit/s	512 Mbit/s x 4	15 x 11 x 3	4 GB	16 GB
2 Gbit/s	256 Mbit/s x 8	15 x 10 x 3	2 GB	8 GB
2 Gbit/s	128 Mbit/s x 16	14 x 10 x 3	1 GB	4 GB
4 Gbit/s	1 Gbit/s x 4	16 x 11 x 3	8 GB	32 GB
4 Gbit/s	512 Mbit/s x 8	16 x 10 x 3	4 GB	16 GB
4 Gbit/s	256 Mbit/s x 16	15 x 10 x 3	2 GB	8 GB

The DDR3 interface uses the SSTL driver/receiver and 1.5 V power. A VREF 1.5/2 V is needed for all SSTL receivers in the DDR3 interface. For details on DDR3 timing design and termination, see Application Note AN3940, *Hardware and Layout Design Considerations for DDR3 SDRAM Memory Interfaces*.

Signal integrity test results show that this design does not require terminating resistors (Series Resistor (RS) and Termination Resistor (RT)) for the discrete DDR3 devices used. DDR3 supports on-die termination, the DDR3 chips and the T4240 are connected directly.

The interface is 1.5 V and is provided by an onboard voltage regulator. VREF, which is half of the interface voltage, or 0.75 V, is supplied by the same voltage regulator. The DDR3 parameters are stored in the I2C EEPROM. An SPD binary file is preloaded in the EEPROM.

Figure 3-1 shows the DDR3 SDRAM block diagram.

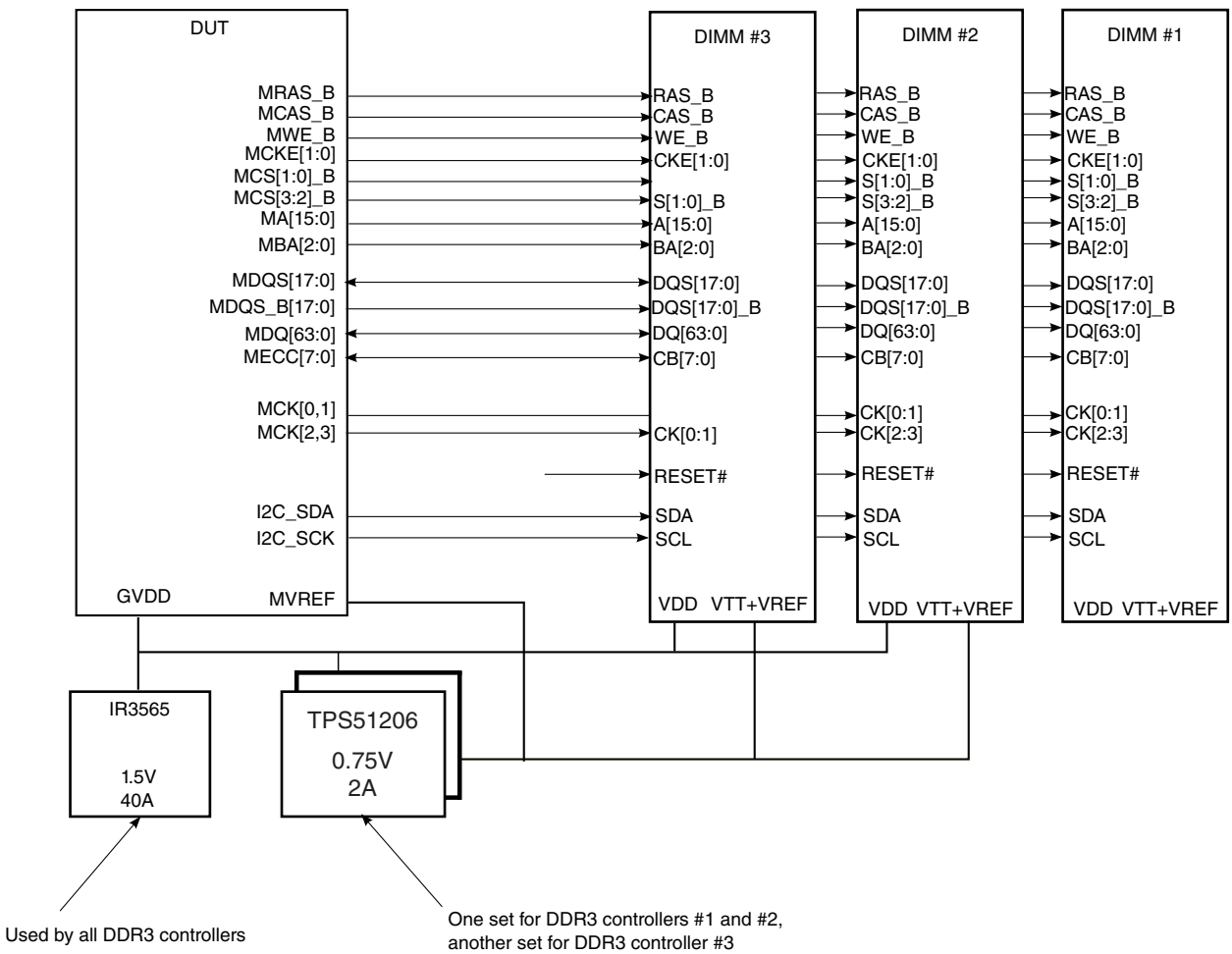


Figure 3-1. DDR3 SDRAM block diagram

Chapter 4
High-Speed Serial Interfaces (HSSI)

The T4240RDB board features a serializer/deserializer (SerDes) interface for high speed interconnected applications. The SerDes interface supports PCI Express, SATA II, and XFI data transfers.

The T4240RDB supports 32 configurable SerDes interfaces:

- SerDes 1 lane E to lane H is configured as SGMII.
- SerDes 2 lane A to lane D is configured to support XFI and lane E to lane H is configured to support SGMII (for 10 Gbit /s and 1 Gbit /s speed).
- SerDes 3 lane A to lane H is configured as x8 PCIe port.
- SerDes 4 lane A to lane D is configured as x4 PCIe port.
- SerDes 4 lane 6 is configured as a SATA interface.

4.1 SATA II

The SoC SATA controller is compliant with the Serial ATA 2.6 specification. The SATA controller supports speed of 1.5 Gbit /s (first-generation SATA) and 3 Gbit /s (second-generation SATA).

4.2 SGMII

The Serial Gigabit Media Independent Interface (SGMII) is a high speed interface linking the Ethernet controller with an Ethernet PHY. SGMII use differential signalling for electrical robustness, which includes four signals:

- Receive data and its inverse
- Send data and its inverse

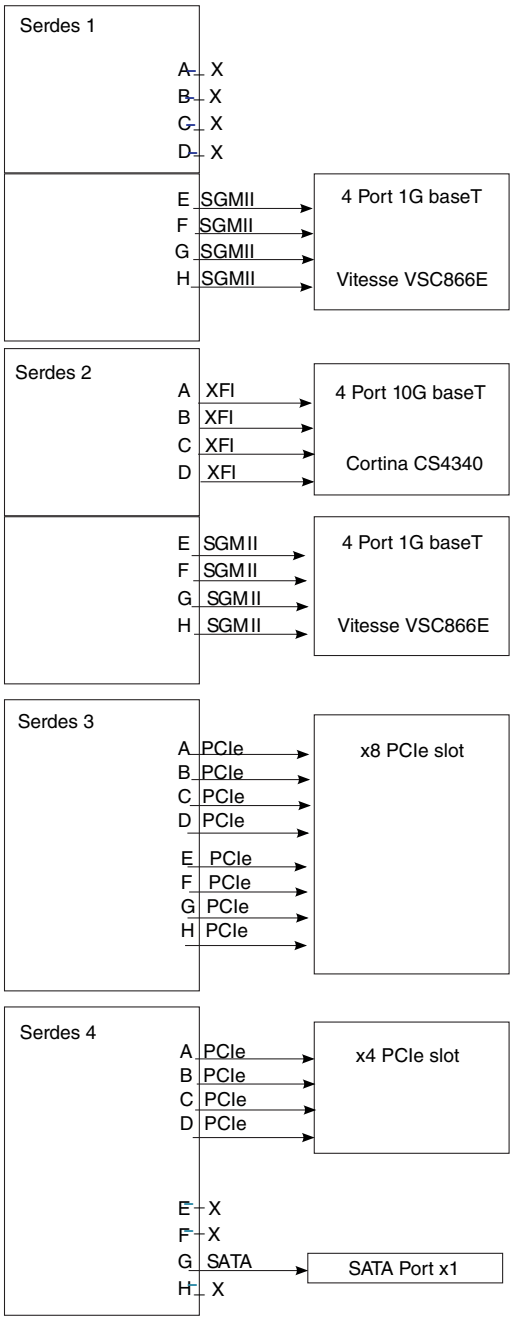


Figure 4-1. SerDes lanes at up to 10 GHz

4.3 Protocol reference clocks

Each SerDes protocol allows a finite set of valid SerDes-related RCW fields and reference clock frequencies, as shown in the table below.

Table 4-1. Valid SerDes reference clocks and RCW encoding

SerDes protocol (Given lane)	Valid reference clock frequency	Valid setting as determined by SRDS_PRTCL_S n	Valid setting as determined by SRDS_PLL_REF_CLK_SEL_S n	Valid setting as determined by SRDS_DIV_[prot]_S n
Networking Protocols (SerDes 1 and SerDes 2)				
SGMII (1.25 Gbit /s)	100 MHz	SGMII @ 1.25 Gbit /s	0: 100	Not applicable
	125 MHz		1: 125 MHz	
XFI (10.3125 Gbit /s)	156.25 MHz	XFI @ 10.3125 Gbit /s	0: 156.25 MHz	Not applicable
Non-networking Protocols (SerDes 3 and SerDes 4)				
PCI2 2.5 Gbit /s (doesn't negotiate upwards)	100 MHz [1]	Any PCIe	0: 100 MHz	2'b10:2.5 G
	125 MHz[1]		1: 125 MHz	
PCI Express 5 Gbit /s (can negotiate up to 5 Gbit /s)	100 MHz[1]	Any PCIe	0: 100 MHz	2'b01:5.0 G
	125 MHz[1]		1: 125 MHz	
SATA (1.5 or 3 Gbit /s)	100 MHz	Any SATA	0: 100 MHz	Not applicable[2]
	125 MHz		1: 125 MHz	

1. A spread-spectrum reference clock is permitted for PCIe. However, if any other high-speed interfaces such as sRIO, Interlaken, SATA, SGMII, SGMII 2.5x, QSGMII, XAUI, XFI, 10GBase-KR, HiGig/HiGig2, or Aurora are used concurrently on the same SerDes bank, the spread-spectrum clocking is not permitted.
2. SerDes lanes configured as SATA operates at 3.0 Gbit /s. 1.5 Gbit /s operation is later enabled through the SATA IP itself. It is possible for software to set each SATA at different rates.

Chapter 5
Integrated Flash Controller (IFC)

The Integrated Flash Controller (IFC) is used to connect with an external asynchronous NAND flash, asynchronous NOR flash, and EPROM.

It has two chip-selects, only one accessible at a time.

The IFC handles pin multiplexing to the internal system bus based on the selected controller (NAND or NOR). To save pins at the chip level, multiplexing of address pins can be done on the data bus using an external address valid signal (AVD). The BCH error-correction algorithm is used to correct the error bits while reading from a NAND device. The following figure shows a block diagram of the IFC.

NOR flash boot bank

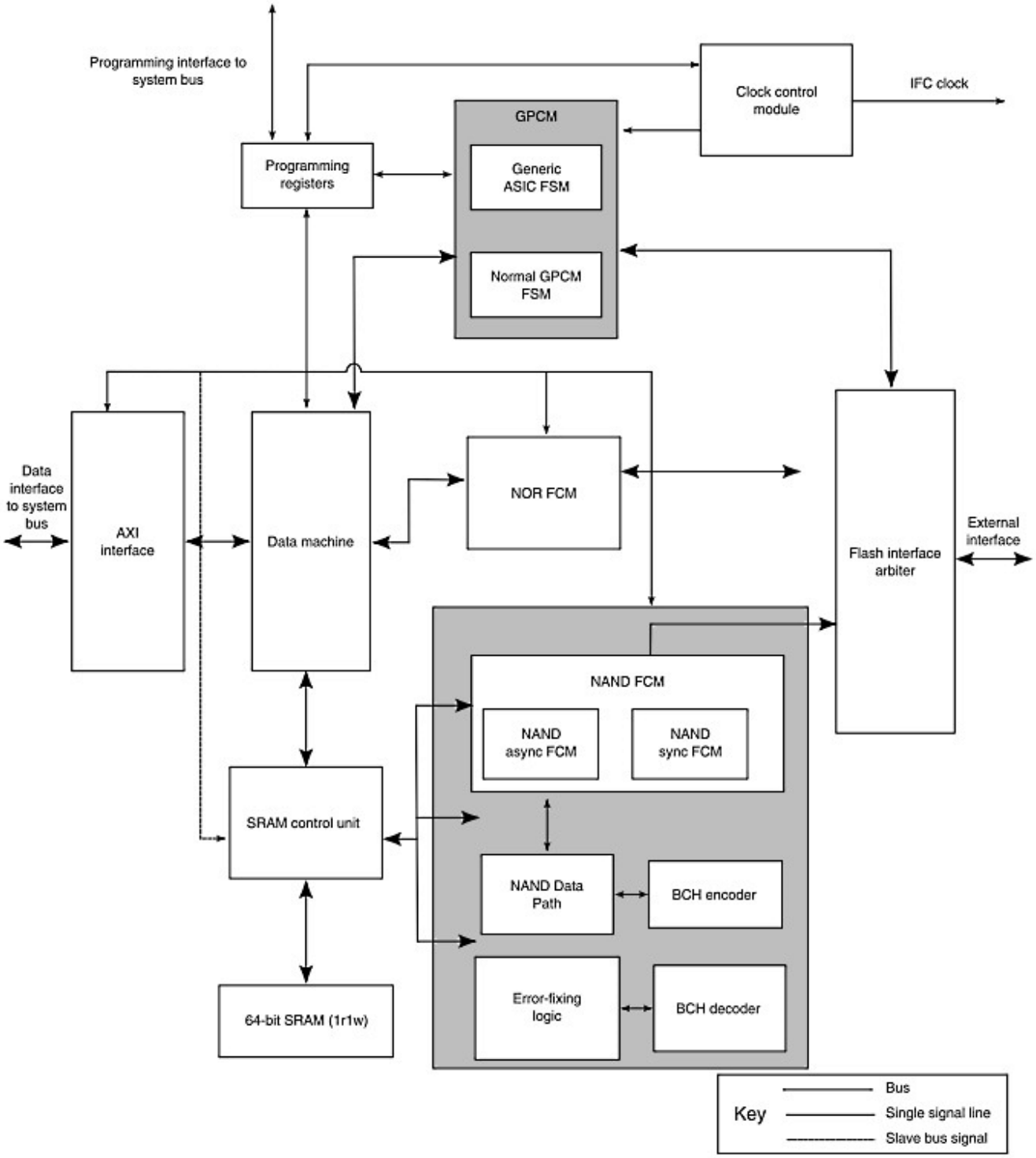


Figure 5-1. IFC block diagram

5.1 NOR flash boot bank

The IFC provides up to 128 MB NOR flash memory, compatible with asynchronous NOR flash (synchronous burst-read is not supported) function. The T4240RDB provides 128 MB of flash memory. The flash memory used is configured in a 16-bit port size.

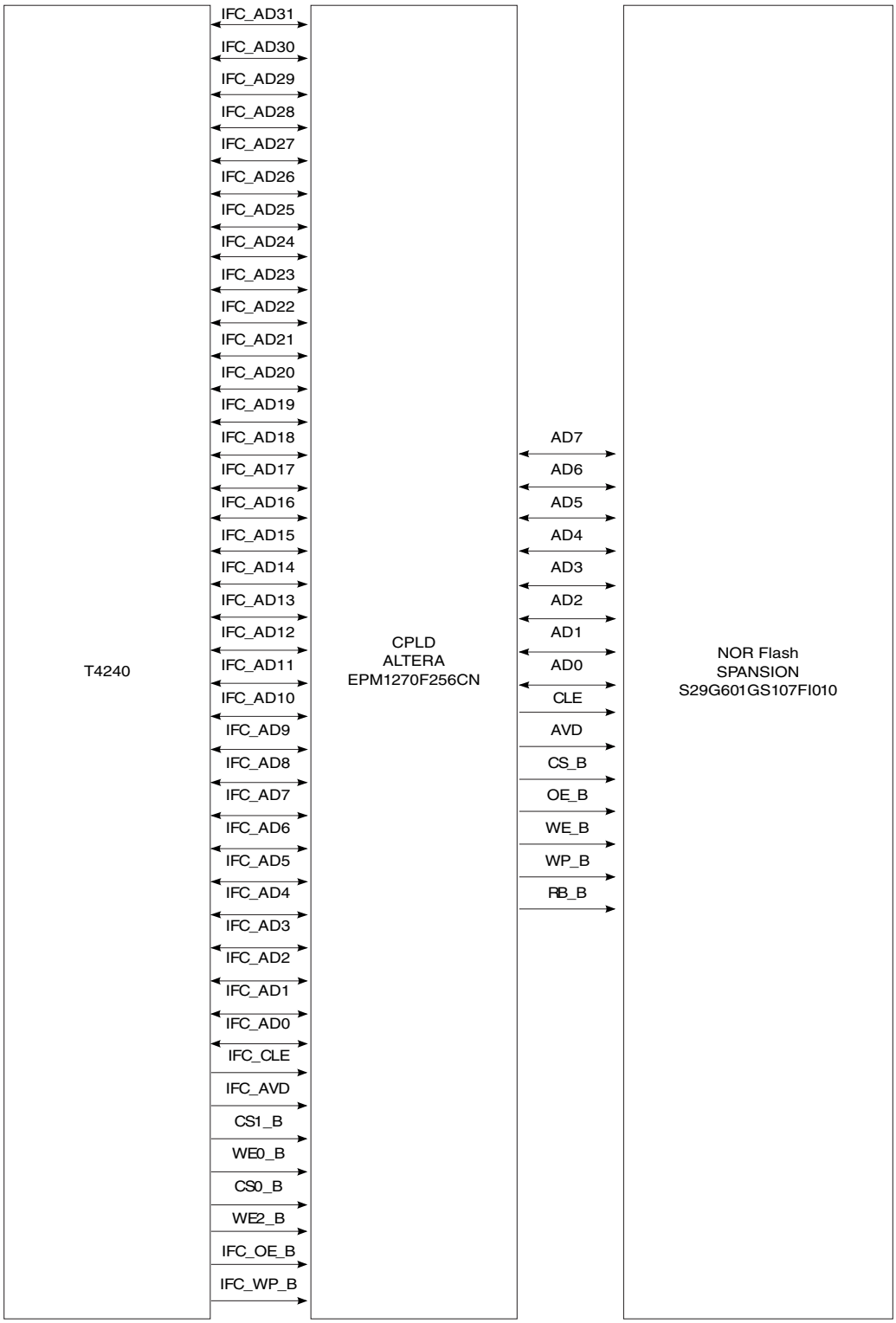


Figure 5-2. NOR flash memory

There are eight virtual banks in the NOR flash memory. SW3(3:1) defines the starting location of each bank.

Table 5-1. NOR flash image layout

SW3(3:1)	Location	Nor flash address
000	vBank0	0xef000000 ~ 0xefffffff
001	vBank1	0xee000000 ~ 0xeeffffff
010	vBank2	0xed000000 ~ 0xedffffff
011	vBank3	0xec000000 ~ 0xecffffff
100	vBank4	0xeb000000 ~ 0xebffffff
101	vBank5	0xea000000 ~ 0xeaffffff
110	vBank6	0xe9000000 ~ 0xe9ffffff
111	vBank7	0xe8000000 ~ 0xe8ffffff

There are two default images in both vBank0 and vBank4 location. If the image in vBank0 is corrupted, adjust SW3(3:1) into (100) position, to boot up from vBank4.

Chapter 6
Ethernet

- Up to eight 1 GHz Ethernet MACs
- Up to four 10 GHz MACs

6.1 Ethernet management

This section explains the electrical characteristics for the EMI1 and EMI2 interfaces. Frame Manager 2's external GE MDIO configures external GE PHYs connected to EMI1 pins.

Frame Manager 2's external 10GE MDIO configures external XAUI, XFI, and HiGig/ HiGig2 PHYs connected to EMI2 pins.

The EMI1 interface timing is compatible with IEEE Std 802.3™ clause 22 and EMI2 interface timing is compatible with IEEE Std 802.3™ clause 45.

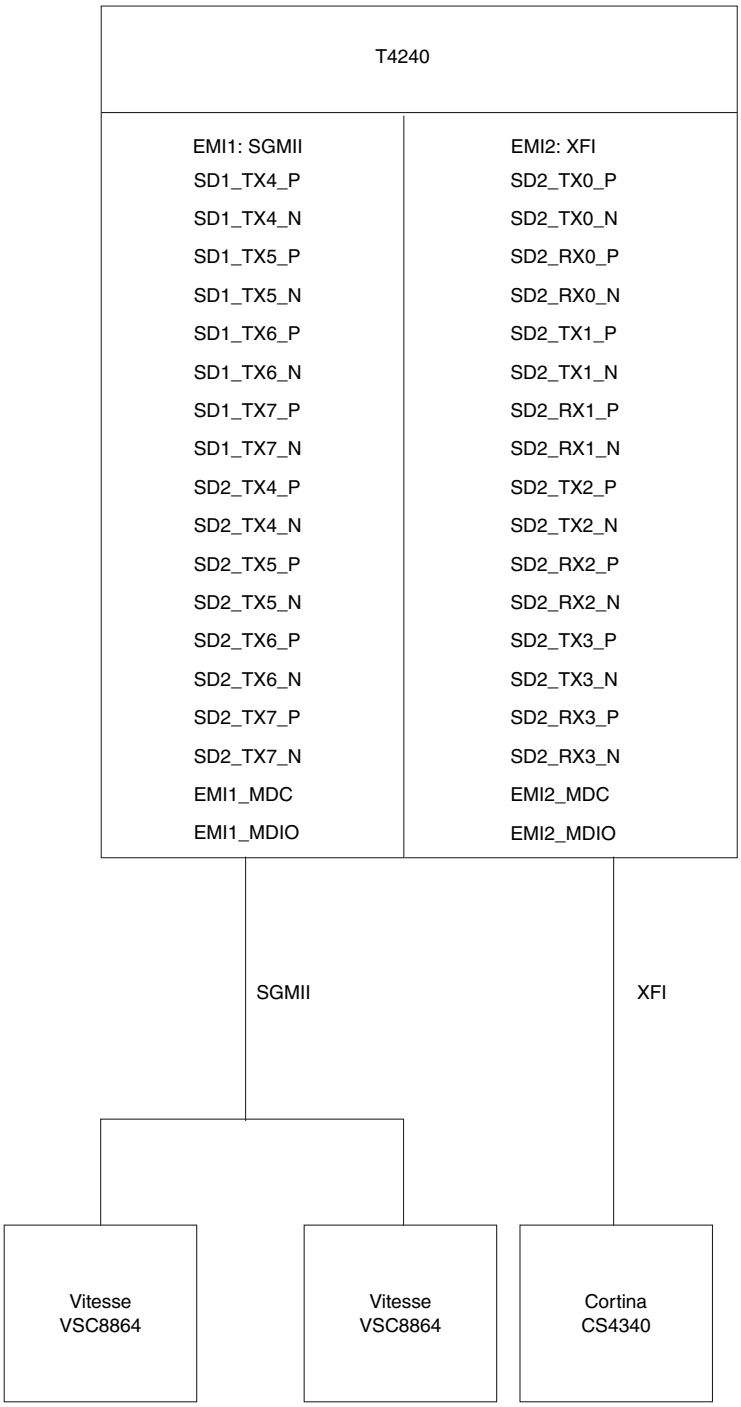


Figure 6-1. EMI1: SGMII

Table 6-1. MDC/MDIO connectivity

Device	Package pin number	Signal description
Interface 1	G13	Management Data Clock
Interface 2	H13	Management Data In/Out

Chapter 7
eSPI

The eSPI is a full-duplex, synchronous, and character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The T4240 has the ability to boot from an SPI serial flash device in addition to supporting other peripheral devices conforming to the SPI standard.

On the RDB, a spansion SPI flash memory is supported (optional).

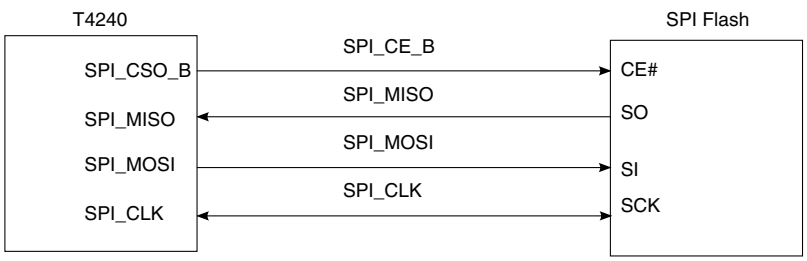


Figure 7-1. SPI

Chapter 8
eSDHC Interface

The enhanced SD host controller (eSDHC) provides an interface between host system and SD cards. The secure digital (SD) card is specifically designed to meet the security, capacity, and performance. Booting from the eSDHC interface is supported using the processor's on-chip ROM.

On the T4240RDB, a single connector is used for both SD memory cards.

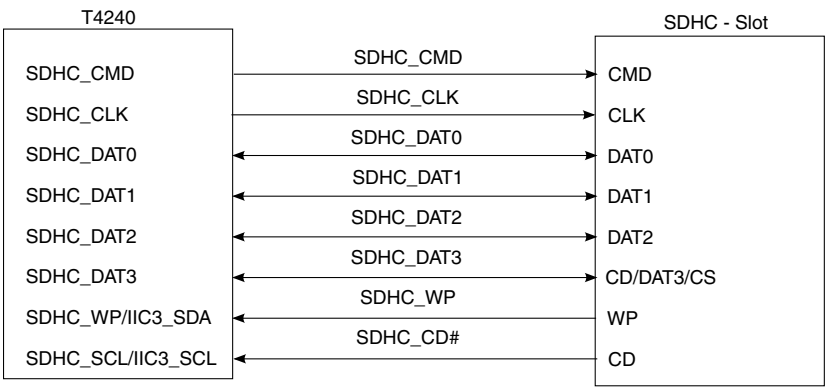


Figure 8-1. eSDHC interface

Chapter 9
I2C

The T4240RDB uses 3 onboard I2C interfaces, which are connected to EEPROM (2Kb AT24C02C-XHM-B), RTC (Maxim DS1374), and Windbond (W83793G).

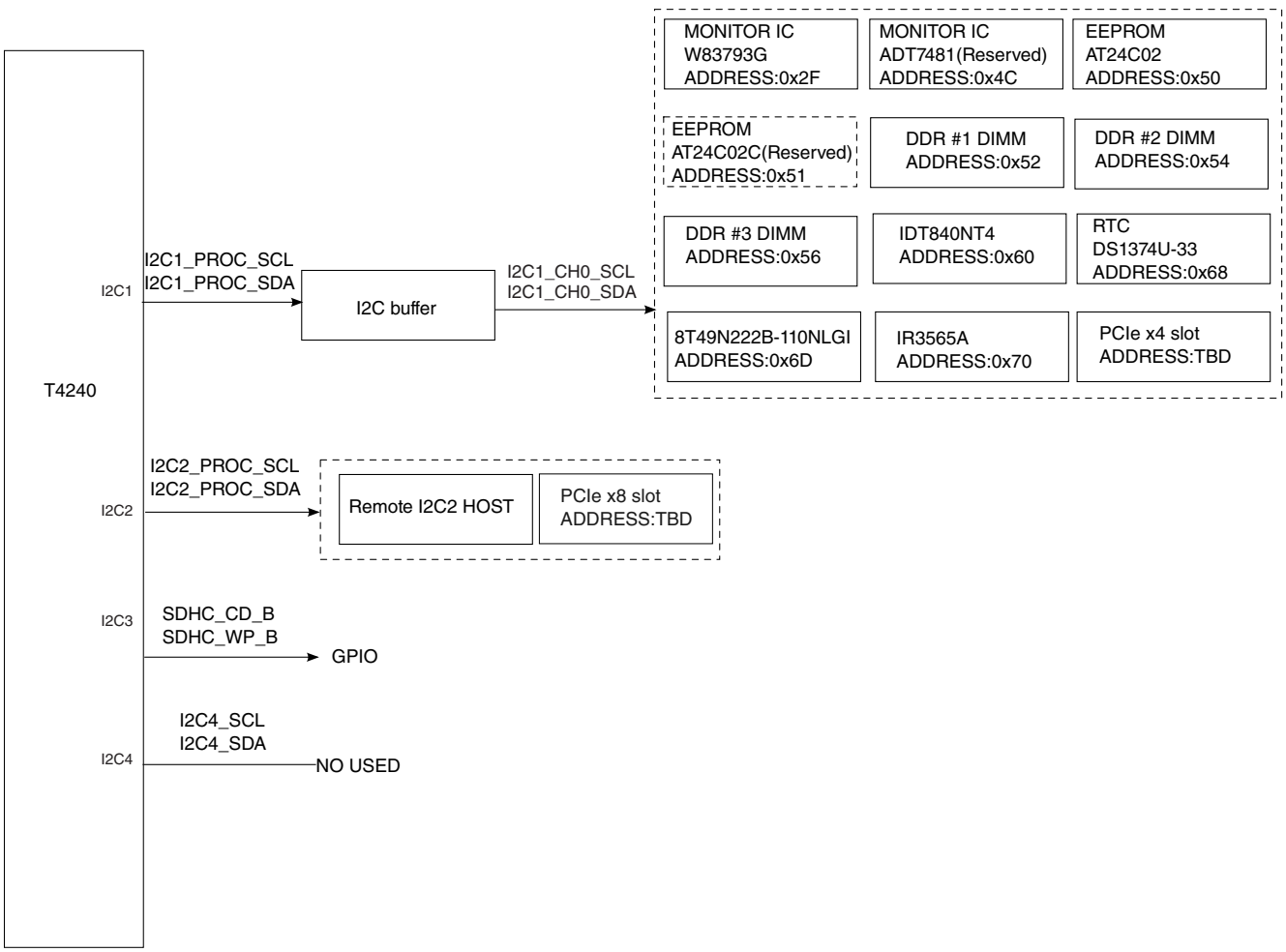


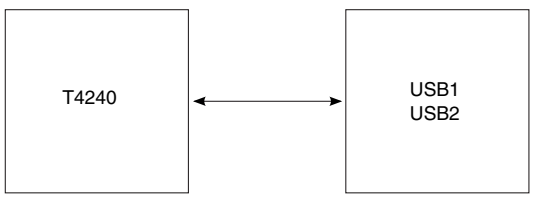
Figure 9-1. I2C block diagram

Chapter 10
USB Interface

The USB interface is configured to operate as a standalone host.

The board features are:

- High-speed (480 MB/s), full-speed (12 MB/s), and low-speed (1.5 MB/s) operations
- Host mode
- Dual stacked Type A connection



USB1_DP	T4240	USB1
USB1_DN	T4240	USB1
USB2_DP	T4240	USB2
USB2_DN	T4240	USB2

Figure 10-1. USB interface

Chapter 11
Serial Interface, UART, and Console Port

Serial interface 1 is a RS232 level serial interface in a RJ45 form factor and is used as the console port for the Appliance. The default setting for this port are:

- Baud rate: 115200
- Data: 8 bit
- Parity: No
- Stop: 1 bit
- No flow control

Each UART supports:

- Full-duplex operation
- Software-programmable baud generators:
  - Divide the input clock by 1 to (216 – 1)
  - Generate a 16x clock for the transmitter and receiver engines
- Clear-to-send (CTS) and ready-to-send (RTS) modem control functions
- Software-selectable serial interface data format that includes:
  - Data length
  - Parity
  - 1/1.5/2 stop bit
  - Baud rate
- Overrun, parity, and framing error detection

The UART ports are routed to dual stacked RJ45 connectors.

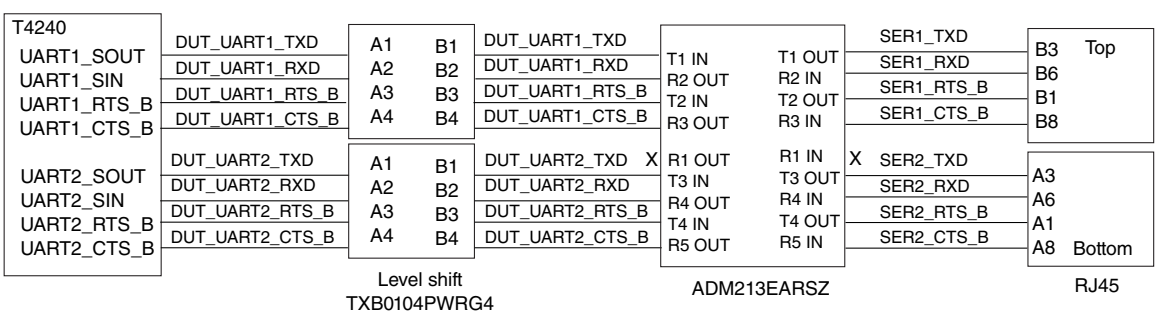


Figure 11-1. Serial interface, UART, and console port

Chapter 12
Power-On Reset Configuration

This section explains:

- POR configuration PLD
- POR configuration resistors

12.1 POR configuration PLD

The Power-On Reset (POR) configuration PLD drives the appropriate configuration signals to the processor. When hard reset (HRESET) is asserted, the POR config PLD begins to drive the POR config signals to the processor. The config signals remain asserted until the POR config signals are latched by the processor. The POR configuration PLD does not drive all POR configuration pins, it drives only those which needs boot location.

12.2 POR configuration resistors

The Power-On Reset (POR) settings that are not set by the POR configuration PLD are controlled using the on-board resistors.

Chapter 13
JTAG/COP

The JTAG connection is provided by a direct connection to the appropriate header connector.

13.1 COP/JTAG port

The common on-chip processor (COP) is a part of the T4240's JTAG module and is implemented as a set of additional instructions and logic. This port can connect to a dedicated emulator for extensive system debugging.

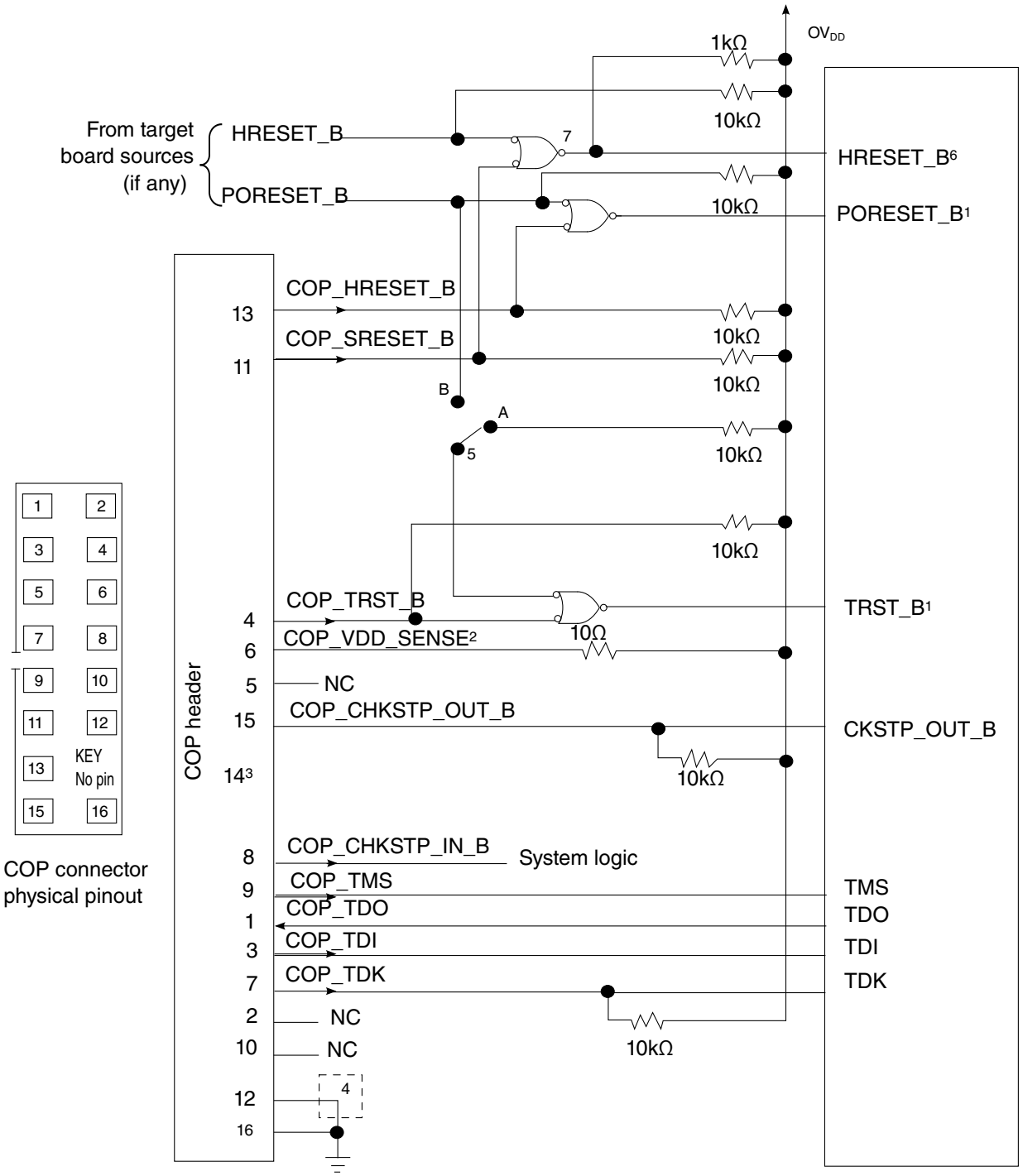


Figure 13-1. JTAG

Chapter 14
Interface Connector Pinout and Switch Settings

This section explains:

- Interface connector pinout
- Switch settings

14.1 Interface connector pinout

Figure 14-1 shows the top view of the T4240RDB board.

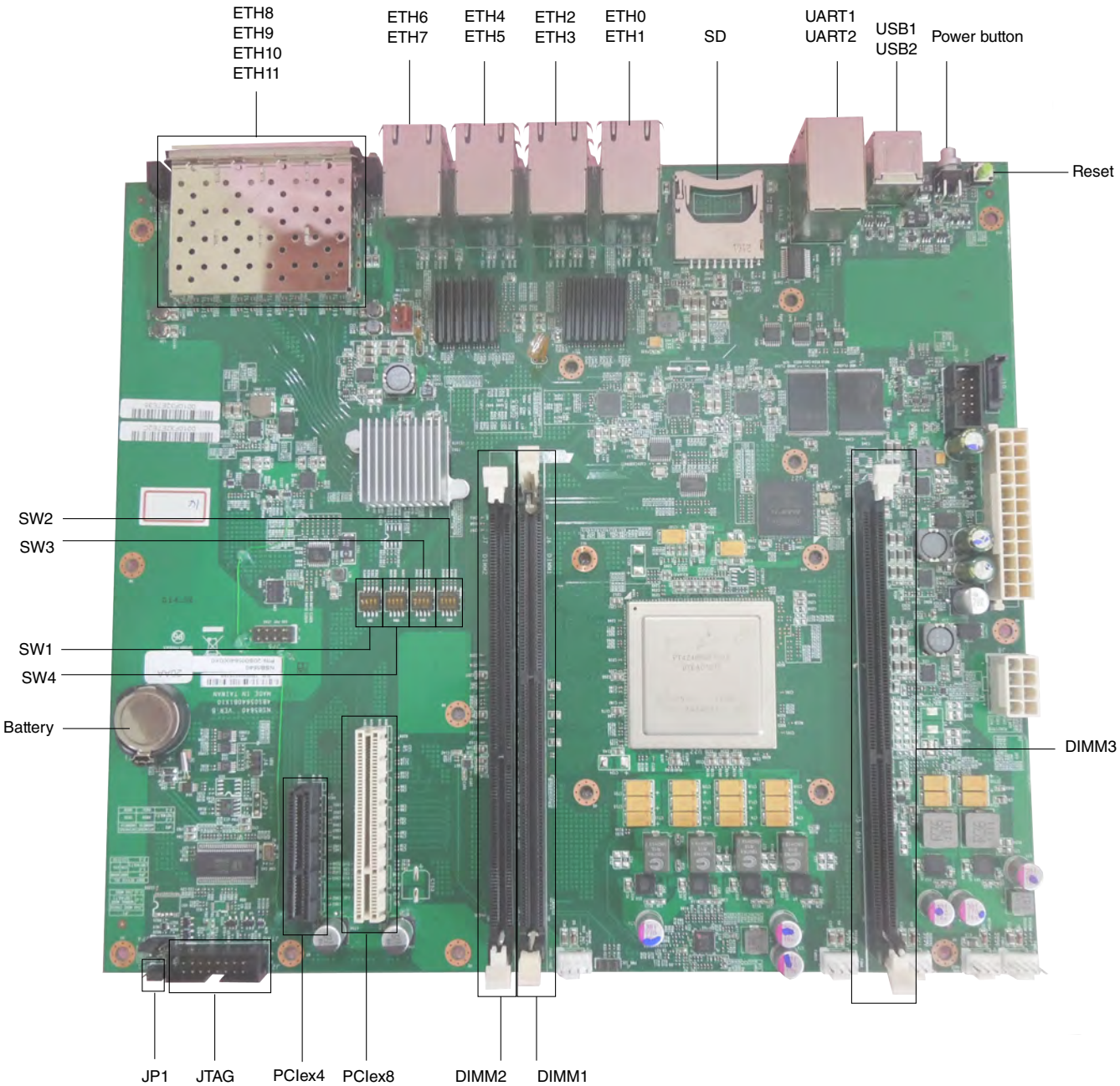


Figure 14-1. T4240RDB top view

The following section shows the connector figures and pinouts of the T4240RDB board connectors.

14.1.1 CN3

The figure below shows the CN3 SD card connector.

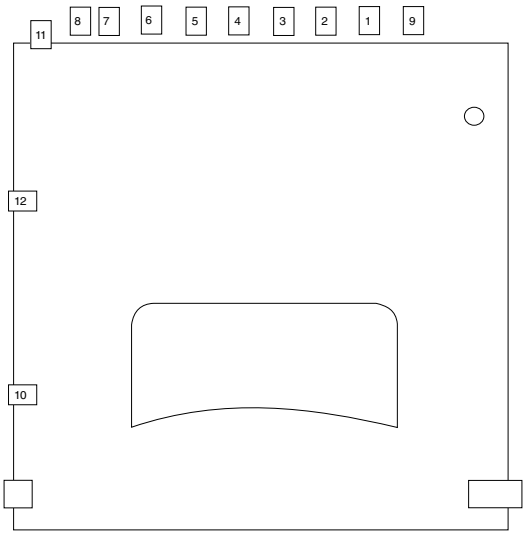


Figure 14-2. CN3 SD card connector

Table 14-1. CN3 SD card connector interface

Pin	Description
1	DAT3
2	CMD
3	GND
4	VCC_3.3
5	CLK
6	GND
7	DAT0
8	DAT1
9	DAT2
10	WRITE PROTECTION
11	CARD DETECTION
12	COMMON PIN

14.1.2 CN4

CN4 shows the USB ports that are present on the board.

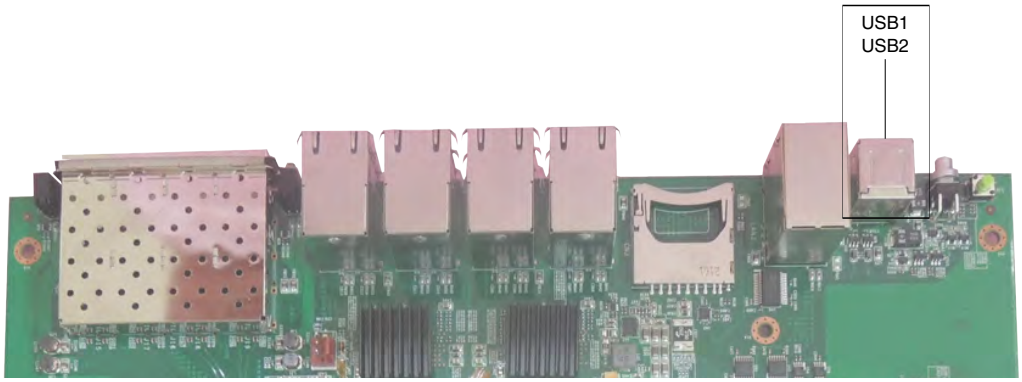


Figure 14-3. CN4 USB connector

Table 14-2. CN4 USB connector interface

Pin	Description
1	USB2_VCC5
2	USB2_DATA-
3	USB2_DATA+
4	USB_GND
5	USB1_VCC5
6	USB1_DATA-
7	USB1_DATA+
8	USB_GND

14.1.3 FAN1 to FAN6

The figure below shows the FAN connectors.

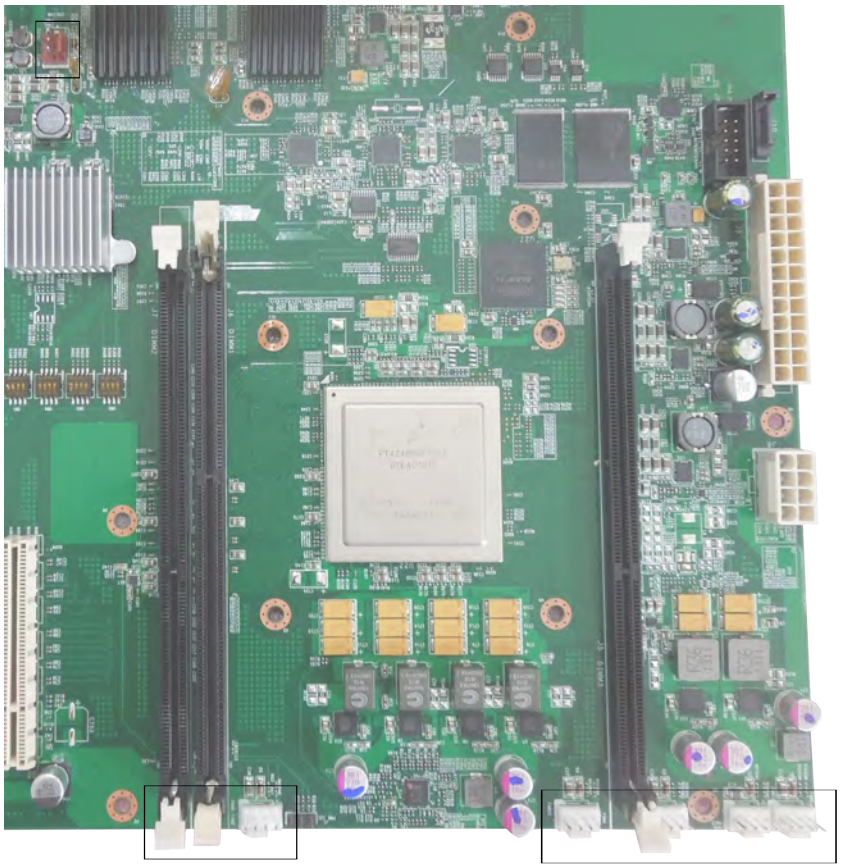


Figure 14-4. FAN1 to FAN6 connectors

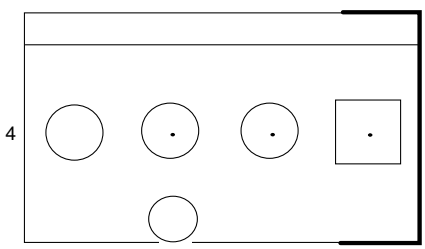


Figure 14-5. FAN connector

Table 14-3. FAN connector interface

Pin	Description
1	GND
2	+12V
3	Fan speed sensor
4	Fan speed control

14.1.4 FAN7 to FAN12

The figure below shows the FAN7 to FAN12 connectors.

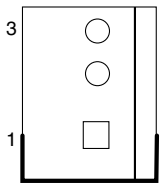


Figure 14-6. FAN7 to FAN12 connectors

14.1.5 J1

J1 refers to Power IC programing connector and I2C for power IC IR3565A.

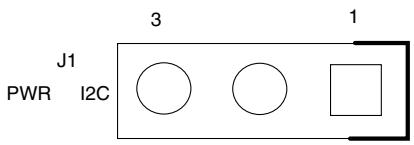


Figure 14-7. J1 connector

Table 14-4. J1 connector interface

Pin	Description
1	GND
2	Power_SDA
3	Power_SCL

14.1.6 J2

J2 refres to the T4240 JTAG debug port.

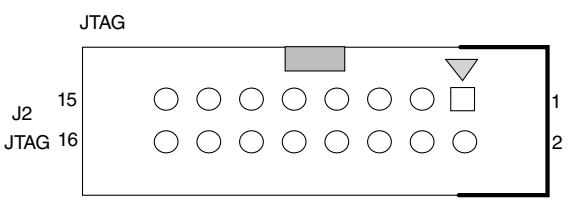


Figure 14-8. J2 connector

Table 14-5. J2 connector interface

Pin	Description
1	COP_TDO
2	NC
3	COP_TDI
4	COP_TRST_N
5	NC
6	OVDD
7	COP_TCK
8	NC
9	COP_TMS
10	NC
11	COP_SRST_B
12	GND
13	COP_HRST_B
14	NC
15	DUT_CKSTP_OUT_B
16	GND

14.1.7 J3: PCIe connector

J3 refers to the PCIe x8 connector.

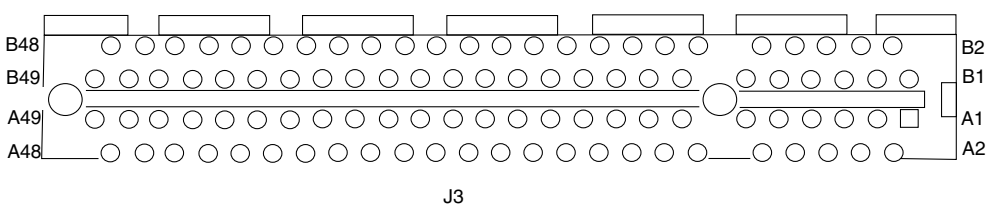


Figure 14-9. PCIe x8 connector

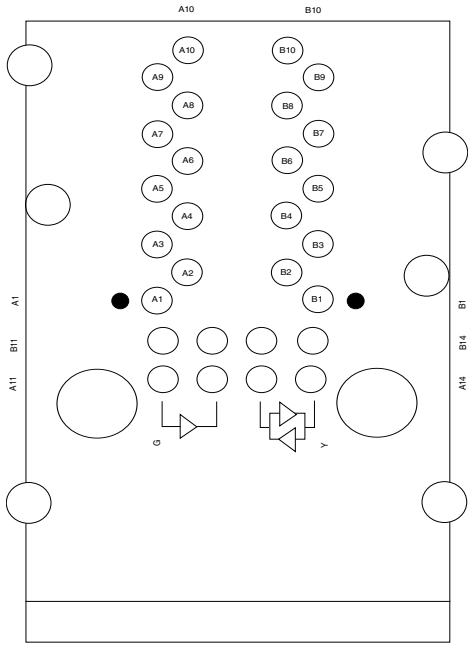


Figure 14-10. J3 connector

Table 14-6. J3

Pin Number	Net Name	Pin Function Description	Direction
B1	VCC_12	+12V	POWER
B2	VCC_12	+12V	POWER
B3	VCC_12	+12V	POWER
B4	GND	GND	
B5	12C1_CH2_SCL	SMbus CLK	I/O
B6	12C1_CH2_SDA	SMbus DATA	I/O
B7	GND	GND	
B8	VCC_3.3	+3.3V	POWER
B9	SLOT6_TRST_B	TRST#	OUT
B10	VCC_P3V3SB	+3.3V Standby power	POWER
B11	PCIEX8_WAKE_B	PCIe WAKE	OUT
B12	NC	Reserved	
B13	GND	GND	
B14	SD3_TXC0_P	PCI Express Transmit Differential Pair	OUT
B15	SD3_TXC0_N	PCI Express Transmit Differential Pair	OUT
B16	GND	GND	
B17	HOT_PLUG_DETECT_B	PLUG DETECT	OUT
B18	GND	GND	
B19	SD3_TXC1_P	PCI Express Transmit Differential Pair	OUT
B20	SD3_TXC1_N	PCI Express Transmit Differential Pair	OUT
B21	GND		
B22	GND		

Table continues on the next page...

Table 14-6. J3 (continued)

Pin Number	Net Name	Pin Function Description	Direction
B23	SD3_TXC2_P	PCI Express Transmit Differential Pair	OUT
B24	SD3_TXC2_N	PCI Express Transmit Differential Pair	OUT
B25	GND		
B26	GND		
B27	SD3_TXC3_P	PCI Express Transmit Differential Pair	OUT
B28	SD3_TXC3_N	PCI Express Transmit Differential Pair	OUT
B29	GND		
B30	NC		
B31	HOT_PLUG_DETECT_B		OUT
B32	GND		
B33	SD3_TXC4_P	PCI Express Transmit Differential Pair	OUT
B34	SD3_TXC4_N	PCI Express Transmit Differential Pair	OUT
B35	GND		
B36	GND		
B37	SD3_TXC5_P	PCI Express Transmit Differential Pair	OUT
B38	SD3_TXC5_N	PCI Express Transmit Differential Pair	OUT
B39	GND		
B40	GND		
B41	GNDSD3_TXC6_P	PCI Express Transmit Differential Pair	OUT
B42	SD3_TXC6_N	PCI Express Transmit Differential Pair	OUT
B43	GND		
B44	GND		
B45	SD3_TXC7_P	PCI Express Transmit Differential Pair	OUT
B46	SD3_TXC7_N	PCI Express Transmit Differential Pair	OUT
B47	GND		
B48	HOT_PLUG_DETECT_B	PLUG_DETECT	OUT
B49	GND		
A1	PRSNT1	PLUG DETECT	OUT
A2	VCC_12	+12v	POWER
A3	VCC_12	+12v	POWER
A4	GND		
A5	SLOT6_TCK	SLOT TCK	OUT
A6	SLOT6_TDI	SLOT TDI	OUT
A7	NC		
A8	SLOT6_TMS	SLOT TMS	OUT
A9	VCC_3.3	+3.3V	POWER
A10	VCC_3.3	+3.3V	POWER
A11	RST_PCIE_B	RESET	IN
A12	GND		

Table continues on the next page...

Table 14-6. J3 (continued)

Pin Number	Net Name	Pin Function Description	Direction
A13	PCIE_REFCLK_P	PCIE CLOCK P	IN
A14	PCIE_REFCLK_N	PCIE CLOCK N	IN
A15	GND		
A16	SD3_RX0_P	PCI Express Receive Differential Pair	IN
A17	SD3_RX0_N	PCI Express Receive Differential Pair	IN
A18	GND		
A19	NC		
A20	GND		
A21	SD3_RX1_P	PCI Express Receive Differential Pair	IN
A22	SD3_RX1_N	PCI Express Receive Differential Pair	IN
A23	GND		
A24	GND		
A25	SD3_RX2_P	PCI Express Receive Differential Pair	IN
A26	SD3_RX2_N	PCI Express Receive Differential Pair	IN
A27	GND		
A28	GND		
A29	SD3_RX3_P	PCI Express Receive Differential Pair	IN
A30	SD3_RX3_N	PCI Express Receive Differential Pair	IN
A31	GND		
A32	NC		
A33	NC		
A34	GND		
A35	SD3_RX4_P	PCI Express Receive Differential Pair	IN
A36	SD3_RX4_N	PCI Express Receive Differential Pair	IN
A37	GND		
A38	GND		
A39	SD3_RX5_P	PCI Express Receive Differential Pair	IN
A40	SD3_RX5_N	PCI Express Receive Differential Pair	IN
A41	GND		
A42	GND		
A43	SD3_RX6_P	PCI Express Receive Differential Pair	IN
A44	SD3_RX6_N	PCI Express Receive Differential Pair	IN
A45	GND		
A46	GND		
A47	SD3_RX7_P	PCI Express Receive Differential Pair	IN
A48	SD3_RX7_N	PCI Express Receive Differential Pair	IN
A49		GND	

U55: PCI-e x4 connector

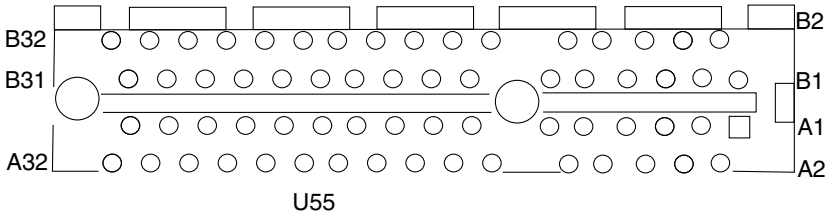


Figure 14-11. U55 connector

Table 14-7. J3

Pin Number	Net Name	Pin Function Description	Direction
B1	VCC_12	+12V	POWER
B2	VCC_12	+12V	POWER
B3	VCC_12	+12V	POWER
B4	GND	GND	
B5	I2C1_CH2_SCL	SMbus CLK	I/O
B6	I2C1_CH2_SCL	SMbus DATA	I/O
B7	GND	GND	
B8	VCC_3.3	+3.3V	POWER
B9	SLOT6_TRST_B	TRST#	OUT
B10	VCC_P3V3SB	+3.3V Standby power	POWER
B11	PCIEX8_WKE_B	PCIE WAKE#	OUT
B12	NC	Reserved	
B13	GND	GND	
B14	SD3_TXC0_P	PCI Express Transmit Differential Pair	I/O
B15	SD3_TXC0_N	PCI Express Transmit Differential Pair	I/O
B16	GND	GND	
B17	HOT_PLUG_DETECT_B	PLUT DETECT	OUT
B18	GND	GND	
B19	SD3_TXC1_P	PCI Express Transmit Differential Pair	OUT
B20	SD3_TXC1_N	PCI Express Transmit Differential Pair	OUT
B21	GND	GND	
B22	GND	GND	
B23	SD3_TXC2_P	PCI Express Transmit Differential Pair	I/O
B24	SD3_TXC2_N	PCI Express Transmit Differential Pair	I/O
B25	GND	GND	
B26	GND	GND	
B27	SD3_TXC3_P	PCI Express Transmit Differential Pair	I/O
B28	SD3_TXC3_N	PCI Express Transmit Differential Pair	I/O
B29	GND	GND	
B30	NC		
B31	HOT_PLUG_DETECT_B		OUT

Table continues on the next page...

Table 14-7. J3 (continued)

Pin Number	Net Name	Pin Function Description	Direction
B32	GND	GND	
A1	PRSNT1	PLUG DETECT	OUT
A2	VCC_12	+12v	POWER
A3	VCC_12	+12v	POWER
A4	GND	GND	
A5	SLOT6_TCK	SLOT TCK	OUT
A6	SLOT6_TDI	SLOT TDI	OUT
A7	NC		
A8	SLOT6_TMS	SLOT TMS	OUT
A9	VCC_3.3	+3.3V	POWER
A10	VCC_3.3	+3.3V	POWER
A11	RST_PCIE_B	RESET	IN
A12	GND		
A13	PCIE_REFCLK_P	PCIE CLOCK P	IN
A14	PCIE_REFCLK_N	PCIE CLOCK N	IN
A15	GND		
A16	SD3_RX0_P	PCIE Express Receive Differential Pair	IN
A17	SD3_RX0_N	PCIE Express Receive Differential Pair	IN
A18	GND		
A19	NC		
A20	GND		
A21	SD3_RX1_P	PCIE Express Receive Differential Pair	IN
A22	SD3_RX1_N	PCIE Express Receive Differential Pair	IN
A23	GND		
A24	GND		
A25	SD3_RX2_P	PCIE Express Receive Differential Pair	IN
A26	SD3_RX2_N	PCIE Express Receive Differential Pair	IN
A27	GND		
A28	GND		
A29	SD3_RX3_P	PCIE Express Receive Differential Pair	IN
A30	SD3_RX3_N	PCIE Express Receive Differential Pair	IN
A31	GND		
A32	NC		

14.1.8 J4

J4 refers to the T4240 I2C bus connector.

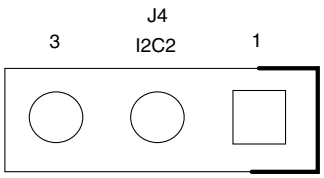


Figure 14-12. J4 connector

Table 14-8. J4 connector interface

Pin	Description
1	I2C2_SDA
2	GND
3	I2C2_SCL

14.1.9 J8

J8 refers to the ATX power connector.

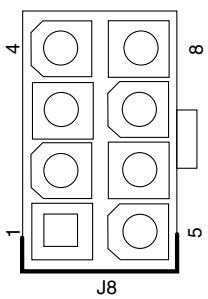


Figure 14-13. J8 connector

Table 14-9. J8 connector interface

Pin	Description
1	GND
2	GND
3	GND
4	GND
5	P12V
6	P12V
7	P12V
8	P12V

14.1.10 J9

J9 refers to the ATX power connector for main power.

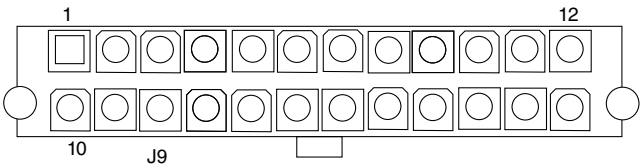


Figure 14-14. J9 connector

Table 14-10. J9 connector interface

Pin	Description
1	P3V3
2	P3V3
3	GND
4	P5V
5	GND
6	P5V
7	GND
8	PWROK
9	P5V_SB
10	P12V
11	P12V
12	P3V3
13	P3V3
14	N12V
15	GND
16	PSON#
17	GND
18	GND
19	GND
20	NC
21	P5V
22	P5V
23	P5V
24	GND

14.1.11 J10

J10 refers to the SATA port/connector.

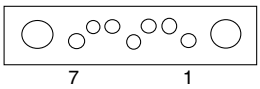


Figure 14-15. J10 SATA connector

Table 14-11. J10 SATA connector interface

Pin	Description
1	GND
2	TXP
3	TXN
4	GND
5	RXN
6	RXP
7	GND

14.1.12 J11, J12, J13, and J14

J11, J12, J13, and J14 refers to the gigabit Ethernet (GbE) ports.

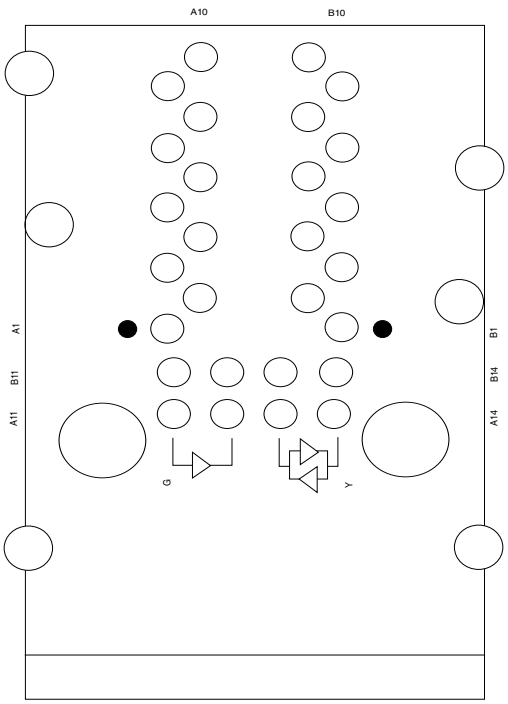


Figure 14-16. J11, J12, J13, and J14 connector

Table 14-12. J11, J12, J13, and J14 connector interface

Pin	Description
A1	A_MDX1+
A2	A_MDX1-
A3	A_MDX2+
A4	A_MDX2-
A5	A_MDX3+
A6	A_MDX3-
A7	A_MDX4+
A8	A_MDX4-
B1	B_MDX1+
B2	B_MDX1-
B3	B_MDX2+
B4	B_MDX2-
B5	B_MDX3+
B6	B_MDX3-
B7	B_MDX4+
B8	B_MDX4-

14.1.13 JP1

The jumper, JP1, is used to toggle between Normal mode and JTAG debug mode. Figure 14-18 shows the JP1 pins.

- **Normal mode**: when in this mode, the system will go directly to the Kernel. Place the jumper on pin 1 and 2 to use this mode. This is also the default mode.
- **JTAG mode**: when in this mode, before entering to the Kernel, there is an option to select **CodeWarrior IDE**, as a debugging tool. Place the jumper on pin 2 and 3 to use this mode.

JP1 is shown in the figure below.

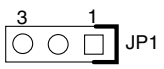


Figure 14-17. JP1 connector

Table 14-13. JP1 connector interface

JTAG mode	Choose
1-2	Normal mode (default)
2-3	JTAG mode

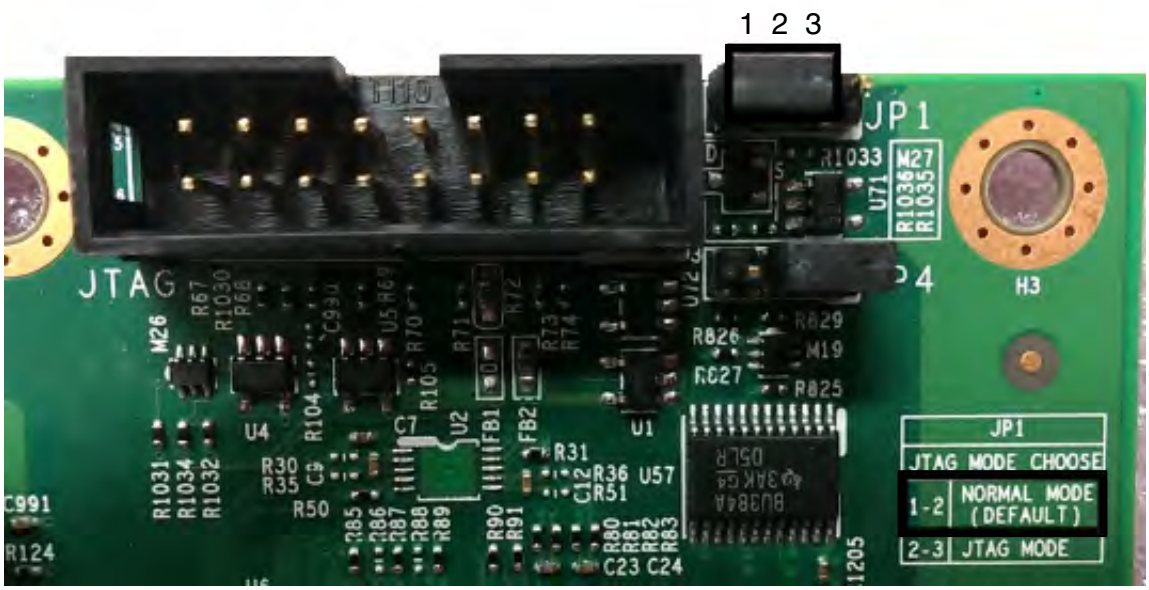


Figure 14-18. JP1 pins

14.1.14 JP3: JTAG connector

The jumper, JP3, refers to the CPLD programming connector.

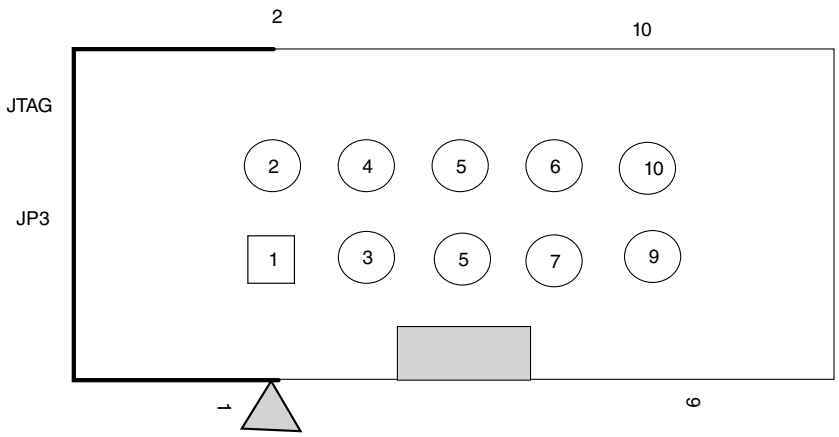


Figure 14-19. JP3 connector

Table 14-14. JP3 connector interface

Pin	Description
1	TCK
2	GND
3	TDO
4	P3V3
5	TMS
6	JTAG
7	NC
8	NC
9	TDI
10	GND

14.1.15 J15, J17, J18, and J19: 10G SFP+

The jumpers, J15, J17, J18, and J19 (10G SFP+), refers to the 10 gigabit Ethernet (GbE) ports.

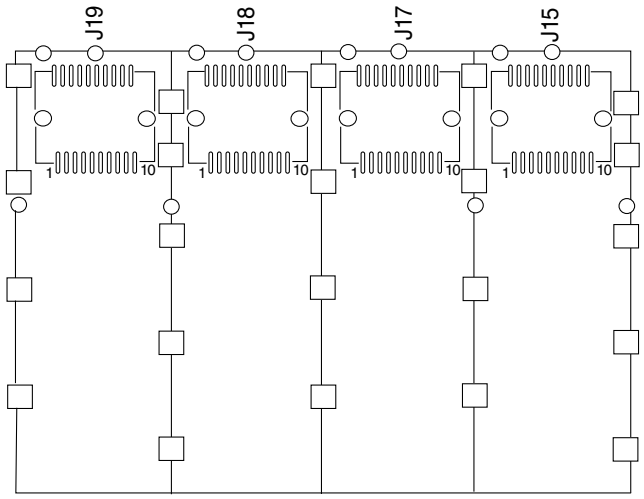


Figure 14-20. 15, J17, J18, and J19: 10G SFP+

Table 14-15. J15, J17, J18, and J19 connector interface

Pin	Description
1	VEET
2	TXFAULT
3	TX_DISABLE
4	SDA
5	SCL
6	MOD-ABS
7	RS0
8	RX_LOS
9	RS1
10	VEER
11	VEER
12	RD-
13	RD+
14	VEER
15	VCCR
16	CCT
17	VEET
18	TD+
19	TD-
20	VEET

14.1.16 LAN1

LAN1 refers to the console ports.

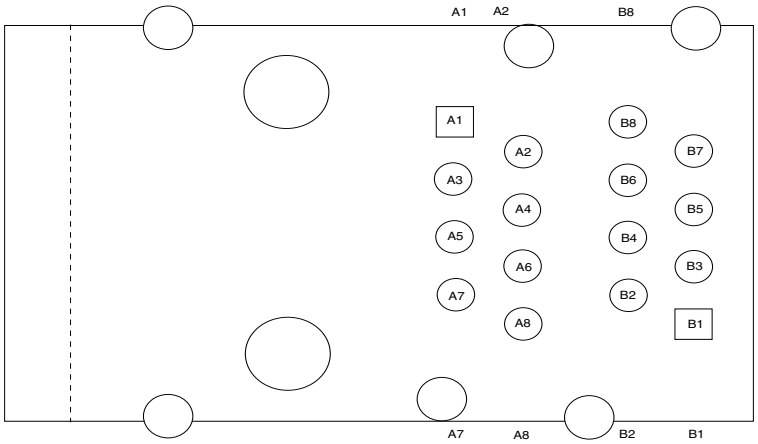


Figure 14-21. LAN1 console connector

Table 14-16. LAN1 console connector interface

Pin	Description
A1	SER2_RTS_B
A2	NC
A3	SER2_TXD
A4	GND
A5	NC
A6	SER2_RSD
A7	NC
A8	SER2 CTS B
B1	SER1_RTS_B
B2	NC
B3	SER1_TXD
B4	GND
B5	NC
B6	SER1_RXD
B7	NC
B8	SER1 CTS B

14.1.17 Cortina PHY to 10G

The figure below shows the 10G SPF+ cage.

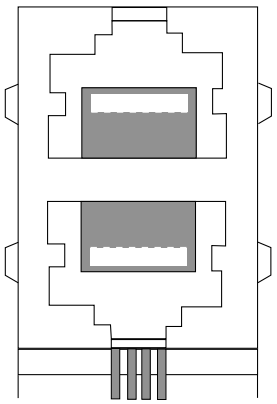


Figure 14-22. 10G SPF+ cage

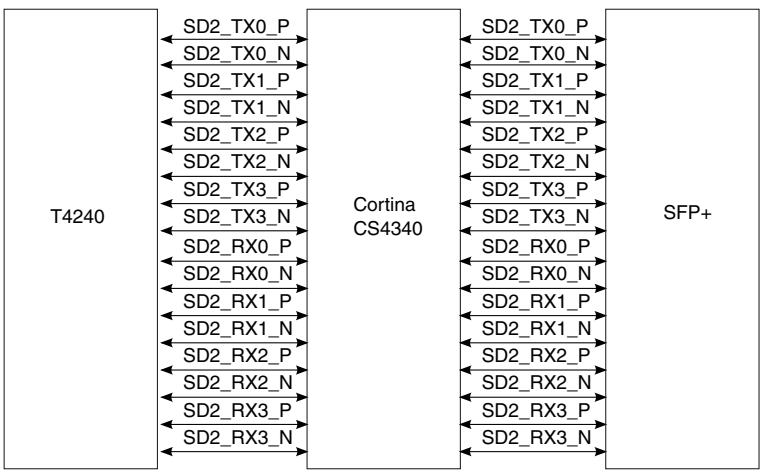


Figure 14-23. Cortina PHY to 10G

14.2 Switch settings

This section explains:

- SW1 switch
- SW2 switch
- SW3 switch
- SW4 switch

14.2.1 SW1 switch

The switch SW1 is used to select the frequency of the system clock (SYSCLK) and the DDR reference clock (DDRCLK).

Default SW1 settings are:

- SW1(4:1): 0011

- SYSCLK: 66 MHz
- DDRCLK: 133.33 MHz

Table 14-17. SW1 settings

SW1(4:1)	SYSCLK (MHz)	DDRCLK (MHz)
0000	66.67	66.67
0001	66.67	100
0010	66.67	125
0011 (Default)	66.67	133.33
0100	100	66.67
0101	100	100
0110	100	125
0111	100	133.33
1000	125	66.67
1001	125	100
1010	125	125
1011	125	133.33
1100	133.33	66.67
1101	133.33	100
1110	133.33	125
1111	133.33	133.33

For SW1(4:1) values in the above table, 0 indicates ON and 1 indicates OFF.

14.2.2 SW2 switch

The SW2(3:4) are reserved pins for future use. For an SW2 value, 0 indicates ON and 1 indicates OFF.

The SW2 and SW3 are the selection of the RCW location.

Table 14-18. SW2 switch settings

Switches	Pin	Description
SW2	1	ON: RCW source located in NOR/ NAND OFF: RCW source located in SD/ EEPROM
SW2	2	ON: RCW in NAND OFF: RCW in NOR
SW3	4	ON: RCW source located in SD OFF: RCW source located in EEPROM

Default is to have the RCW in the NOR flash location.

NOTE

- RCW in NOR, SW2(4:1) will be XX10.
- RCW in NAND, SW2(4:1) will be XX00.

14.2.3 SW3 switch

The SW3 switch defines eight virtual banks starting and ending location. There are eight virtual bank in the NOR flash and Table 5-1 lists those bank locations. SW3(3:1) is used to select the virtual bank location. The default SW3(4:1) value is X000.

Table 14-19. SW3 settings

3:1	NOR flash virtual bank selector
4	RCW_SRC_SELECT 1: RCW source from EEPROM 0: RCW source from SD card

For an SW3 value, 0 indicates ON and 1 indicates OFF.

14.2.4 SW4 switch

The table below shows the SW4 settings, where value 0 indicates ON and value 1 indicates OFF.

Table 14-20. SW4 settings

P1	Auto power mode 0: Power always ON 1: Normal power ON/ OFF (default)
P2	CFG_TESTSEL_B 0: T4160 mode 1: T4240 mode (default)
P3	Reserved
P4	Reserved

Chapter 15
Updating the RCW

Follow these steps for updating the RCW under U-Boot:

1. Use UART to 10-pin connector cable to connect the host computer to the T4240RDB board, as shown in Figure 15-3 .

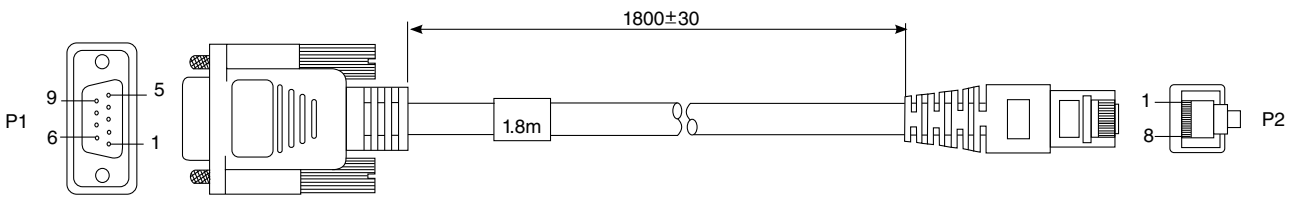


Figure 15-1. UART to 10-Pin connector cable

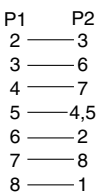


Figure 15-2. Console cable - pin assignment

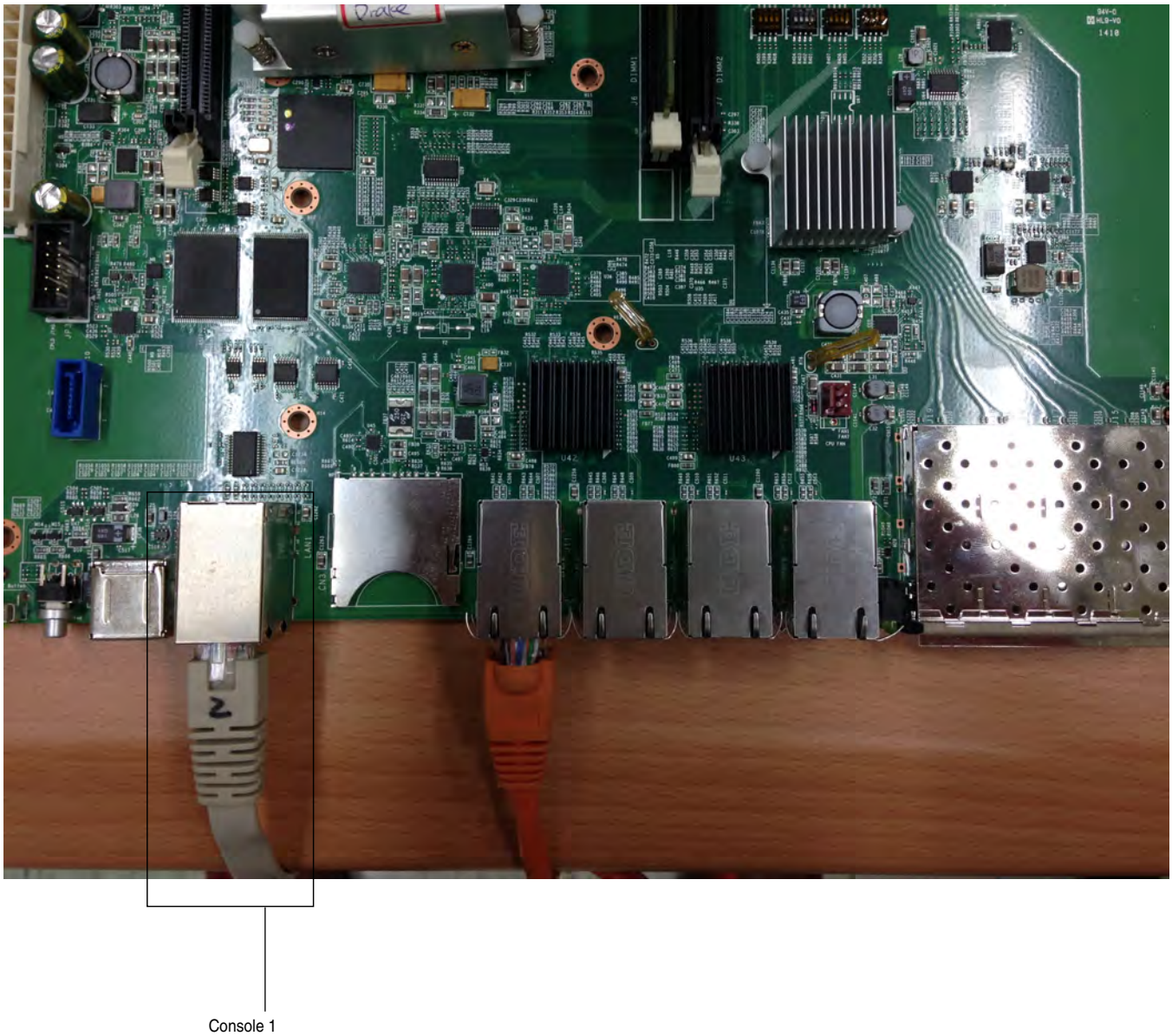


Figure 15-3. Connecting the 10-Pin connector cable

Table 15-1. Connecting the 10-Pin connector cable

DB9	RJ45	Function
8	1	RTS
6	2	X
2	3	TXD
5	4	GND
5	5	X
3	6	RXD

Table continues on the next page...

Table 15-1. Connecting the 10-Pin connector cable (continued)

DB9	RJ45	Function
4	7	X
7	8	CTS

2. Open the Hyper Terminal or applications with similar functions on the host computer, for example Tera Term.
   a. Open **Tera Term** from the programs menu.
   b. Select **Serial** and confirm the correct **Port**.
   c. Select **OK**, as shown in Figure 15-4.

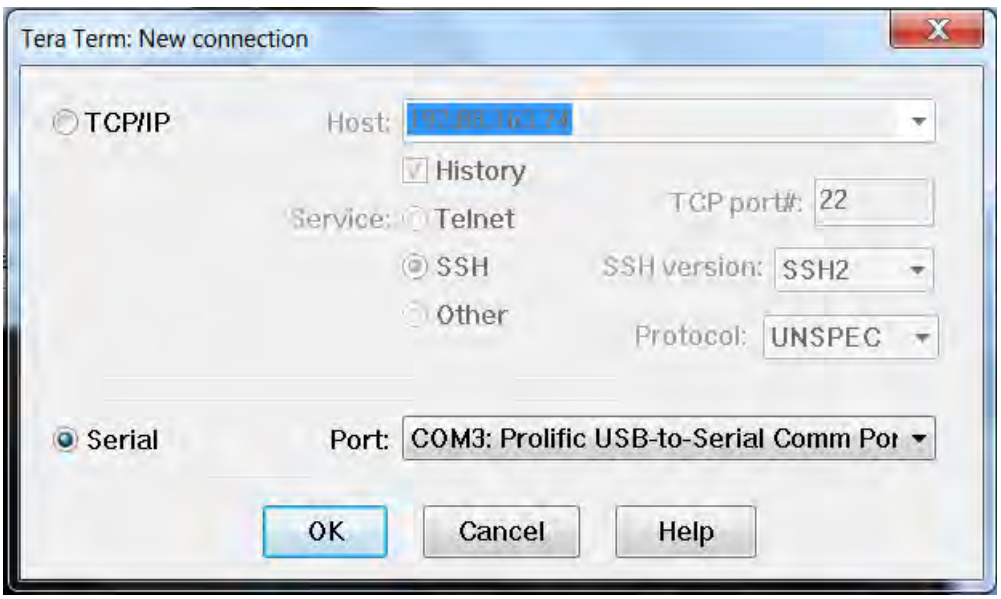


Figure 15-4. Selecting serial port

   d. Select Setup/serial port …, and prepare setup as shown in Figure 15-5.
      - Port: COM1
      - Baud rate: 115200
      - Data: 8 bit
      - Parity: none
      - Stop:1 bit
      - Flow control: none

Figure 15-5. Setting-up serial port

3. Turn ON and select any key to stop autoboot on U-boot, for example, RCW binary filename *rcw_28_56_2_10_1666MHz_1600MHz.bin*. BIN file is located in SW image (USB drive).

NOTE

- File name is only for reference, actual name may vary based on project requirements.
- Use Kermit for downloading files.

```
loadb 1000000

## Ready for binary (kermit) download to 0x01000000 at 115200 bps...
## Total Size = 0x00000078 = 120 Bytes
## Start Addr = 0x01000000
```

I2C write 1000000 50 0.1 78 (Length: 78; refers to the total size value)

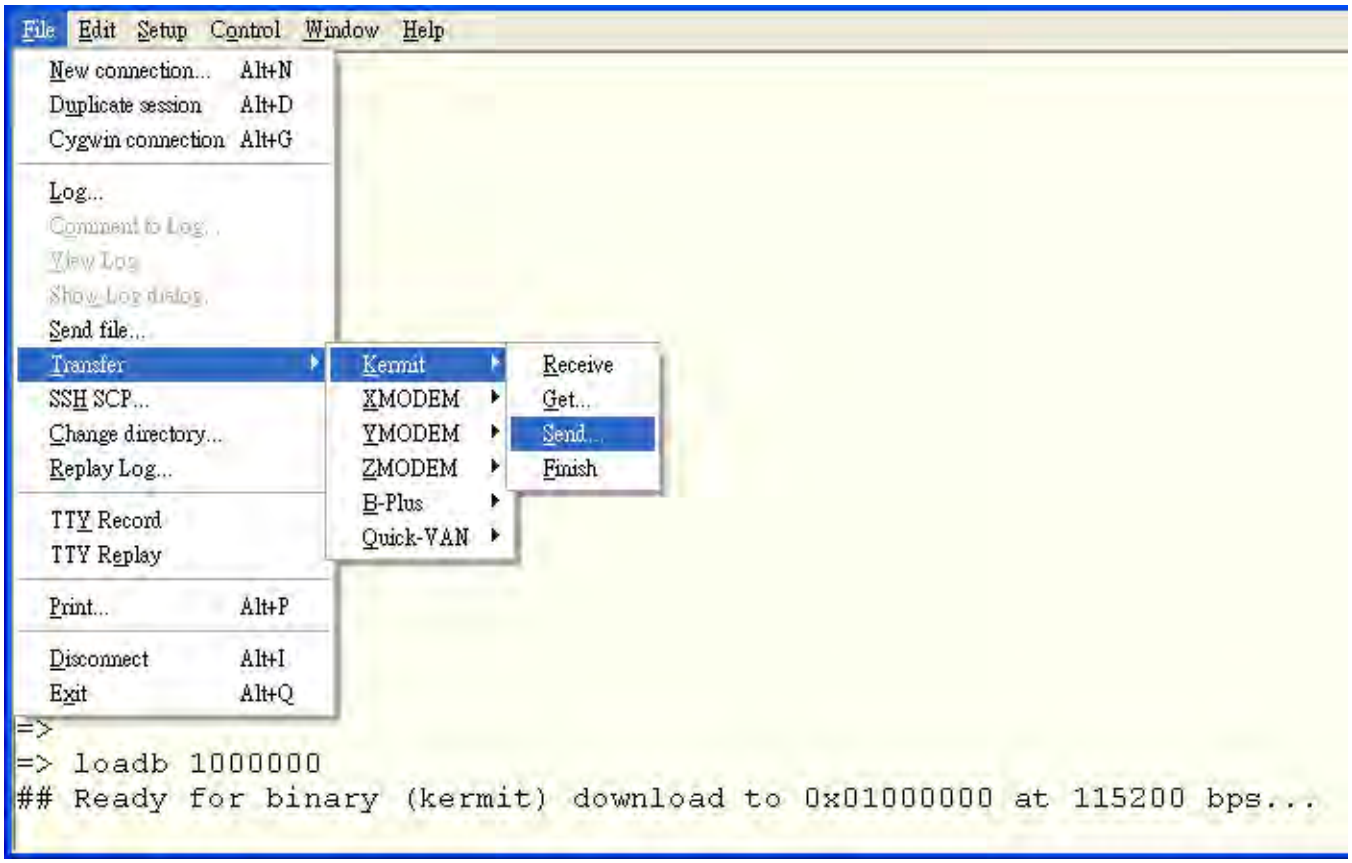


Figure 15-6. Transferring through Kermit

Power up the board once completed.

Appendix A
10G interface testing steps

The T4240RDB board has four 10G interfaces. The table below shows how ETH matches to Linux.

Table A-1. Port map

Label in Linux	Label on the front panel
fm1-mac9	eth11
fm1-mac10	eth10
fm2-mac9	eth8
fm2-mac10	eth9

Follow these steps to test the 10G interface performance by connecting two RDB boards:

1. Choose the correct interface you want to test and connect the SFP.
2. After connecting the SFP, connect the optical fiber cable to both ends of the board, as shown in Figure A-2.
3. In this scenario, the interface is fm2-mac9. So, you need to make the interface up, by using the following commands on both the boards:
   - Board 1: `Ifconfig fm2-mac9 192.168.1.10 up`
   - Board 2: `Ifconfig fm2-mac9 192.168.1.20 up`
4. Now you can ping between the boards and test if the connection is working fine:
   - Board 1: `ping 192.168.1.20`
   - Board 2: `ping 192.168.1.10`

Figure A-1. SFP+ module

Figure A-2. 10G interface (ETH8-ETH11)

Execute these commands to run iperf on the board to check the throughput performance:

- Board 1 (server): `iperf -s`
- Board 2 (client): `iperf -c 192.168.1.10 -P24`

Iperf is a client server communication benchmark, which is used to measure the network performance. Following are the features of ipref:

- TCP:
  - Measure bandwidth.
  - Report MSS/MTU size and observed read sizes.
  - Support for TCP window size via socket buffers.
  - Multi-threaded if pthreads or Win32 threads are available. Client and server can have multiple simultaneous connections.
- UDP:
  - Client can create UDP streams of specified bandwidth.
  - Measure packet loss
  - Measure delay jitter

- Multicast capable
- Multi-threaded if pthreads are available. Client and server can have multiple simultaneous connections.

Listing A-1. Synopsis

```
iperf [-s|-c host] [options]

iperf  [-h|--help] [-v|--version]
```

Listing A-2. Description Client/Server

```
-f, --format
          [kmKM] format to report: Kbits, Mbits, KBytes, MBytes

-i, --interval
          # seconds between periodic bandwidth reports

-l, --len
          # [KM]length of buffer to read or write (default 8 KB)

-m, --print_mss
          print TCP maximum segment size (MTU - TCP/IP header)

-p, --port
          # server port to listen on/connect to

-u, --udp
          use UDP rather than TCP

-w, --window
          #[KM] TCP window size (socket buffer size)

-B, --bind
          <host> bind to <host>, an interface or multicast address

-C, --compatibility
          for use with older versions does not sent extra msgs

-M, --mss
          # set TCP maximum segment size (MTU - 40 bytes)

-N, --nodelay
          set TCP no delay, disabling Nagle's Algorithm

-V, --IPv6Version
          Set the domain to IPv6
```

Listing A-3. Server specific

```
-s, --server
          run in server mode

-U, --single_udp
          run in single threaded UDP mode

-D, --daemon
          run the server as a daemon
```

Listing A-4. Client specific

```
-b, --bandwidth #[KM]
          for  UDP,  bandwidth to send at in bits/sec (default 1 Mbit/sec, implies -u)

-c, --client
          <host> run in client mode, connecting to <host>

-d, --dualtest
```

```
          Do a bidirectional test simultaneously

-n, --num
          #[KM] number of bytes to transmit (instead of -t)

-r, --tradeoff
          Do a bidirectional test individually

-t, --time
          # time in seconds to transmit for (default 10 secs)

-F, --fileinput <name>
          input the data to be transmitted from a file

-I, --stdin
          input the data to be transmitted from stdin

-L, --listenport #
          port to recieve bidirectional tests back on

-P, --parallel
          # number of parallel client threads to run

-T, --ttl
          # time-to-live, for multicast (default 1)
```

Appendix B
Booting from SD card

Follow these steps to boot up the board from SD card:

1. Insert the SD card into another working board.
2. Download the U-Boot image and program into the SD card.

```
tftp 1000000 $your_dir_path/u-boot-with-spl-pbl.bin
mmc write 1000000 8 0x800
```

NOTE

`u-boot-with-Spi-pbl.bin` file is inside the software folder in the USB stick.

3. Set the T4240RDB's board Switch 3 as:

```
SW3[4-1] = 0000
```

NOTE

- 0 represents ON.
- SW2[1] should be OFF to load RCW from SD card.

4. Insert the SD card into the SD card slot and power up the board to boot from SD card.

NOTE

For more information on the system recovery, see QorIQ SDK 1.9 Documentation.

- For SD card deployment, see, https://freescale.sdlproducts.com/LiveContent/content/en-US/QorIQ_SDK_1.9/GUID-09A9C9B5-F47B-4FA3-912E-8682C033B6BF
- When both NOR flash memory banks are corrupted, you can use the CodeWarrior IDE to flash the image to NOR flash memory. See, https://freescale.sdlproducts.com/LiveContent/content/en-US/QorIQ_SDK_1.9/GUID-6E44B664-2DFD-4695-9801-701AD8CB0B9D

Appendix C
Revision History

Table C-1 summarizes revisions to this document.

Table C-1. Revision history

Revision	Date	Topic cross-reference	Description
Rev. 1	01/2016	SW2 switch	Updated table Table 14-18.
Rev. 0	06/2015	-	Initial public release.

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Revision 1, 01/2016