M68EML08QBLTYUM
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M68EML08QBLTY
Emulation Module

User's Manual

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M68EML08QBLTY Quick Start Guide

Make sure that power is disconnected from your M68EML08QBLTY Emulator Module and from your target system. Then follow these quick-start steps to make your M68EML08QBLTY ready for use as quickly as possible.

1 - Set Jumpers W4 and W5

Set jumper headers W4 and W5 to specify the MCU you wish to emulate:

- Jumper W4 specifies the MCU suffix (ex. 1, 2, 3, 4, 5 or 8)
- Jumper W5 specifies the MCU family (QT/QY, QL or QB)

2 - Set Jumper W3

Set 6-pin header W3 to specify the clock source for the EM MCU when external clock is enabled (you must switch from internal clock to external clock in your software):

- Jumper between pins 1 and 2 = Replaceable EM 32.768 kHz oscillator Y1
- Jumper between pins 3 and 4 = Debugger-controlled PFB oscillator (factory default)
- Jumper between pins 5 and 6 = XTAL, 4.9152 MHz crystal at Y2

3 - Install the emulation module into your development system

To use the M68EML08QBLTY in an MMDS0508 Motorola Modular Development System (MMDS) or MMEVS0508 Motorola Modular Evaluation System (MMEVS):

- Remove the access panel of the station-module enclosure if using an MMDS
- Insert the M68EML08QBLTY through the access-panel opening
- Fit together M68EML08QBLTY connectors P1 and P2 (on the bottom of the board) to connectors P11 and P12, respectively, of the MMDS or MMEVS control board
- Snap the corners of the M68EML08QBLTY onto the plastic standoffs

4 - Connect the emulation module to your target system

Use a target flex A cable, appropriate target head adapter, and surface mount adapter. Plug the appropriate end of the flex cable into M68EML08QBLTY connector J1.

- If the M68EML08QBLTY is in an MMDS station module, run the flex cable through the slit in the station-module enclosure, then replace the access panel.
- Plug the other end of the flex cable into the target head. Solder the appropriate surface mount adapter to your target if necessary. Then plug the target head into the surface mount adapter on your target system.

5 - Install the development software

Refer to your development software installation or user guide.

6 - Copy personality files to your computer

The factory ships M68EML08QBLTY MCU personality files on the documentation CD-ROM.

- If you're using the CodeWarrior IDE, find the installation directory and copy the personality files named 00C75Vxx.mem, 00C76Vxx.mem, and 00C7EVxx.mem from the documentation CD-ROM to the `...\prog\reg` subdirectory of the CodeWarrior IDE main directory.

- If you're using the P&E debugger, copy these files to the installation directory that contains MMDS08.EXE or MMEVS08.EXE and rename them from 00C75Vxx.mem, 00C76Vxx.mem, and 00C7EVxx.mem to 00475Vxx.mem, 00476Vxx.mem, and 0047EVxx.mem respectively.

7 - Connect MMDS or MMEVS to your computer and apply power

When you make sure that the serial cable connections between your development system and your computer are sound, you are ready to apply power and use your M68EML08QBLTY.

This completes the quick start for your M68EML08QBLTY.

7 - Connect MMDS or MMEVS to your computer and apply power

User's Manual — M68EML08QBLTY Emulation Module

Section 1. General Information

1.1 Introduction

This user's manual explains connection and configuration of the Motorola M68EML08QBLTY Emulator Module. The M68EML08QBLTY makes possible emulation and debugging of target systems based on MC68HC908QL2 (alpha version only), MC68HC908QL3 (alpha version only), MC68HC908QL4 (alpha version only), MC68HC908QT1/QY1, MC68HC908QT2/QY2, MC68HC908QT4/QY4, MC68HC908QT8/QY8, MC68HC908QB4, or MC68HC908QB8 microcontroller units (MCU).

The M68EML08QBLTY can be part of two development systems. This section describes those systems and explains the layout of the M68EML08QBLTY.

1.2 Development Systems

Your M68EML08QBLTY can be part of two Motorola HC08 processor family development systems: the MMDS0508 Motorola Modular Development System (MMDS) or the MMEVS0508 Evaluation System (MMEVS). Refer to the specific development system user's manual for more information.

1.2.1 Motorola Modular Development System (MMDS0508)

The MMDS is an emulator system that provides a bus state analyzer and real-time memory windows for designing and debugging a target system. A complete MMDS consists of:

- **a Station Module** — the metal MMDS enclosure, containing the platform board and the internal power supply. Most system cables connect to the MMDS station module.
- **an Emulator Module (EM)** — such as the M68EML08QBLTY, a separately- purchased printed circuit board that enables system functionality for a specific set of MCUs. The EM fits into the station module through a removable panel in the enclosure top. The EM has

connectors for a target cable and for cables to a logic analyzer. The cable runs to an optional target system through an aperture in the station-module enclosure, to connect directly to the emulator module.

- **Two logic clip cable assemblies** — twisted-pair cables that connect the station module to your target system, a test fixture, an oscillator, or any other circuitry useful for evaluation or analysis. One end of each cable assembly has a molded connector, which fits into station-module pod A or pod B. Leads at the other end of each cable terminate in female probe tips. Ball clips come with the cable assemblies and may be attached to the female probe tips.
- **a 9-lead RS-232 Serial Cable** — the cable that connects the MMDS to the host computer RS-232 port.
- **System Software** — development software, on CD-ROM.
- **MMDS0508 Documentation** — an MMDS operations manual (MMDS0508OM/D) and the appropriate EM user's manual.

You select the MMDS baud rate: 1200, 2400, 4800, 9600, 19200, 38400, 57600, or 115200.

Substituting a different EM enables your MMDS to emulate target systems based on different MCUs or MCU families. (Your Motorola representative can explain all the EMs available.)

1.2.2 Motorola Modular Evaluation System (MMEVS0508)

An MMEVS is an economical tool for designing, debugging, and evaluating target systems. A complete MMEVS consists of:

- **a Platform Board (PFB)** — the bottom board, which supports the emulator module. The platform board has connectors for power and the the terminal or host computer.
- **an Emulator Module (EM)** — such as the M68EML08QBLTY, a separately purchased printed circuit board that enables system functionality for a specific set of MCUs. The EM fits onto the PFB. The EM has connectors for the target cable and for cables to a logic analyzer.
- **a 9-to-25-pin Adapter** — a molded assembly that lets you connect the 9-pin cable to a 25-pin serial port.

- **a 9-lead RS-232 Serial Cable** — the cable that connects the station module to the host computer RS-232 port.
- **System Software** — development software, supplied on CD-ROM.
- **MMEVS0508 Documentation** — an MMEVS operations manual (MMEVSOM/D) and the appropriate EM user's manual.

An MMEVS features automatic baud rate selection: 2400, 4800, 9600, 19200, 38400, or 57600.

Substituting a different EM enables your MMEVS to emulate target systems based on different MCUs or MCU families. (Your Motorola representative can explain all the EMs available.).

1.3 System Requirements

An IBM PC or compatible running Windows® 98, Windows 2000, Windows NT® (version 4.0), or Windows® XP with at least 32MB of RAM and an RS-232 serial port.

1.4 EM Layout

Figure 1-1 shows the layout of the M68EML08QBLTY. Jumper header W1 specifies the operating voltage. Jumper header W2 is a programming header that selects between the QB8 and the QL4. Jumper header W3 specifies the clock signal source. Jumper headers W4 and W5 specify the MCU to be emulated.

Target interface connector J1 connects the M68EML08QBLTY to a target system, via the included target cable assembly. If you use your M68EML08QBLTY as part of an MMDS, run the target cable assembly through the slit in the station module enclosure.
Connectors J2 and J13 connect to an external logic analyzer. Connector J11 is the source for an inverted clock signal. DIN connectors P1 and P2, on the bottom of the board connect the M68EML08QBLTY to the platform board.
The emulation MCU (MC68HC908GZ60) is at location U4. An MC68HC908QB8 is located at U19 and an MC68HC908QL4 is at location U25. These two processors are used only to generate the emulation clock. The Connector E3 provides the A/D reference voltages. Connectors J12 and J14 are for EM board design and factory use only.

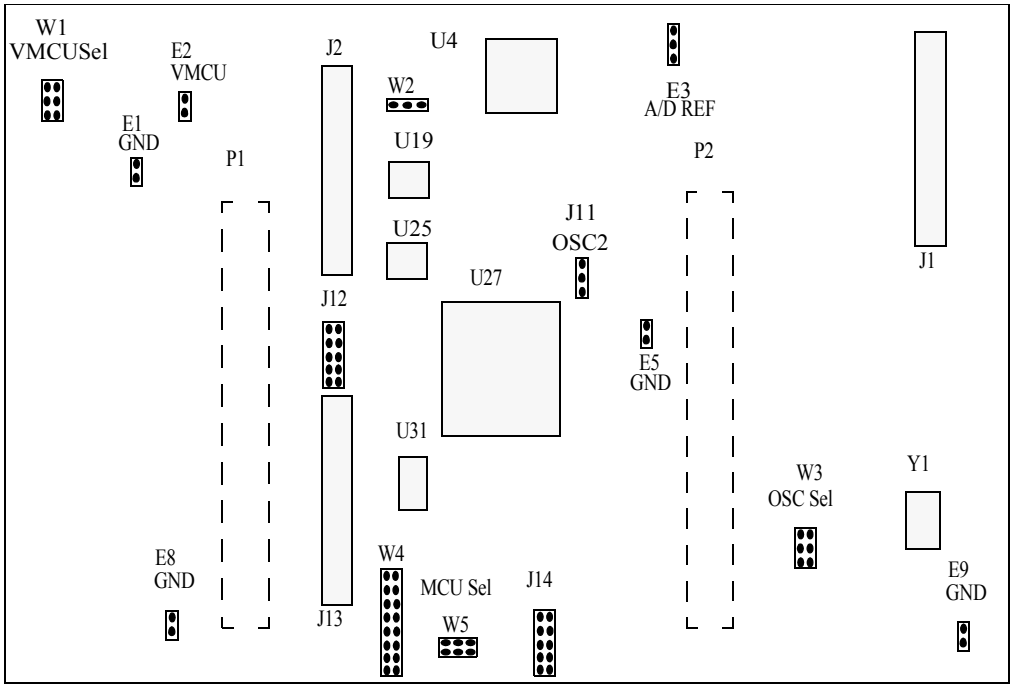


Figure 1-1 M68EML08QBLTY Emulator Module

1.5 Specifications

Table 1-1 lists M68EML08QBLTY specifications

Table 1-1 Specifications

Characteristic	Specifications
Maximum Clock speed	32-MHz at 5V (8-MHz bus), 16-MHz at 3V (4-MHz bus)
Temperature operating storage	 -10° to +50° C -40° to +85° C
MCU Extension I/O	HCMOS Compatible at Vmcu (5V or 3V)
Relative humidity	0 to 90% (noncondensing)
Power requirements	5VDC supplied from the MMDS or MMEVS
Dimensions	5.5 X 8.0 X 0.75 inches (139.7 x 203.2 x 19.1 mm)

1.6 Target Cable Assemblies

To connect your M68EML08QBLTY to a target system, you need a target cable and a target head adapter and footprint for the package you are using. See Figure 1-2.

The cable assembly consists of: a flex cable, a target head adapter, a male-to-male socket-saver and depending on your package, a surface mount adapter. One end of the target cable plugs onto M68EML08QBLTY connector J1. The other end of the flex cable plugs onto the target head adapter, which plugs onto a DIP MCU socket or a surface mount adapter. You should solder the surface mount adapter directly onto the target-system board in place of the MCU. The socket-saver goes between the target head adapter and MCU socket or surface mount adapter. If you use it, it will reduce wear on the target head adapter. After many insertions, you can replace the socket-saver without replacing the entire target head adapter.

Table 1-2 lists target cable and head part numbers appropriate for the M68EML08QBLTY.

Table 1-2 M68EML08QBLTY Target Cable and Head Assemblies

MCU Package	Flex Cable Part Number	Target Head Adapter Part Number	Surface Mount Adapter Part Number	Socket-Saver Part Number
8-pin PDIP (QT)	M68CBL05A	M68TA08QTP8	User-Supplied Thru-Hole DIP Socket	Samtec APA-308-G-A1
8-pin SOIC (QT)	M68CBL05A	M68TA08QTP8	M68DIP8SOIC	Samtec APA-308-G-A1
8-pin DFN (QT)	M68CBL05A	M68TA08QTDFN8	M68DIP8DFN	Samtec APA-308-G-A1
16-pin PDIP (QY, QB)	M68CBL05A	M68TA08QYP16	User-Supplied Thru-Hole DIP Socket	Samtec APA-316-G-A1
16-pin SOIC (QY, QB)	M68CBL05A	M68TA08QYP16	M68DIP16SOIC	Samtec APA-316-G-A1
16-pin TSSOP (QY, QB)	M68CBL05A	M68TA08QYT16	M68DIP16TSSOP	Samtec APA-316-G-A1
16-pin PDIP (QL)	M68CBL05A	M68TA08QLP16	User-Supplied Thru-Hole DIP Socket	Samtec APA-316-G-A1
16-pin SOIC (QL)	M68CBL05A	M68TA08QLP16	M68DIP16SOIC	Samtec APA-316-G-A1
16-pin TSSOP (QL)	M68CBL05A	M68TA08QLDT16	M68DIP16TSSOP	Samtec APA-316-G-A1

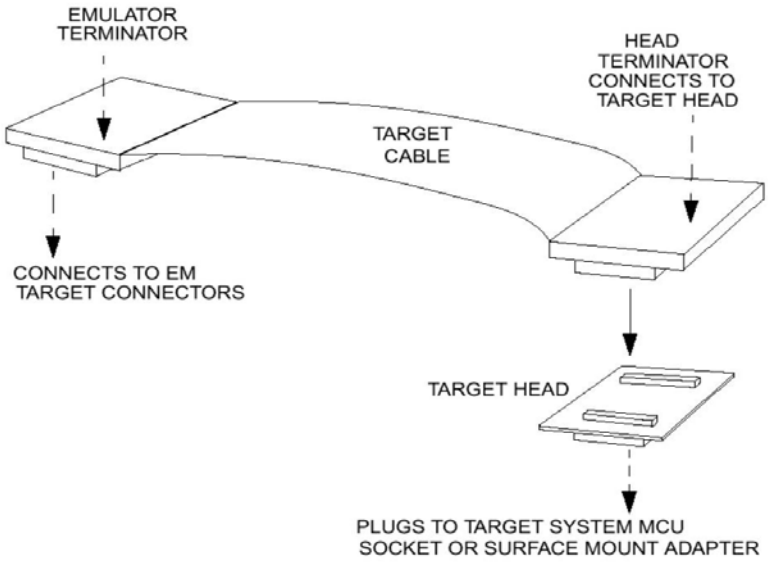


Figure 1-2 Target Cable Assembly

Section 2. Preparation and Operation

2.1 Introduction

This section explains M68EML08QBLTY preparation: how to set board jumpers and how to make system connections.

Note that you can reconfigure an M68EML08QBLTY already installed in an MMDS0508 station module enclosure. To do so, switch off station-module power and target power, remove the panel, then follow the guidance of this section. Similarly, you can reconfigure an M68EML08QBLTY already installed on the MMEVS platform board, provided that you disconnect platform-board power and target power.

CAUTION: ESD Protection

Motorola development systems include open-construction printed circuit boards that contain static-sensitive components. These boards are subject to damage from electrostatic discharge (ESD). To prevent such damage, you must use static-safe work surfaces and grounding straps, as defined in ANSI/EOS/ESD S6.1 and ANSI/EOS/ESD S4.1. All handling of these boards must be in accordance with ANSI/EAI 625.

2.2 Configuring Board Components

Table 2-1 is a summary of configuration settings.

Table 2-1 Configuration Components

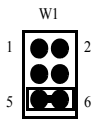
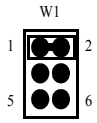
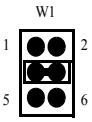
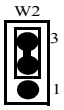
Component	Position	Effect
Voltage Select Header, W1 **Note:** The tracking function is enabled out of the factory. This header is not populated on factory boards. You must remove resistor R2 and solder a 2x3 header onto the board if you wish to use forced 3V or 5V operation. (Use only one jumper in this header.)		**TRCK:** Specifies that the voltage tracks the target voltage (2.7V to 5.5V). **Note:** This is the factory setting. You must remove resistor R2 to turn off this setting.
		**5V:** Specifies 5.0-volt operating power.
		**3V:** Specifies 3.0-volt operating power.
MON08 MCU Header, W2 (Use only one jumper in this header.)		**QB:** Sets the board up for programming the QB part **NOTE:** This header is only used in the factory. Customers should not use this header or attempt to reprogram the MCUs
		**QL:** Sets the board up for programming the QL part **NOTE:** This header is only used in the factory. Customers should not use this header or attempt to reprogram the MCUs

Table 2-1 Configuration Components (Continued)

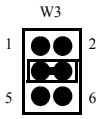
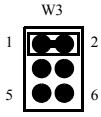
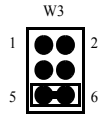
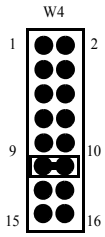
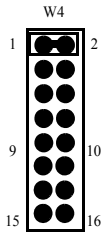
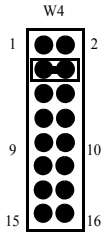
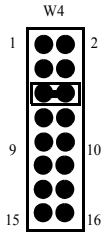
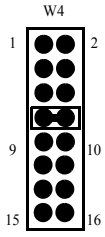
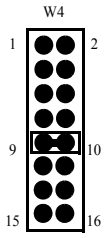
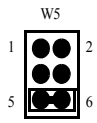
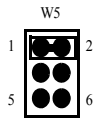
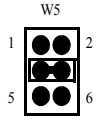
Component	Position	Effect
Oscillator Select Header, W3 (Use only one jumper in this header.)		**PFB:** Specifies the oscillator clock signal from the platform board (PFB). **Factory setting**
		**EM:** Specifies the clock signal from the removable 32.768-kilohertz oscillator on the EM board installed at Y1 (EM).
		**XTAL:** Specifies the clock signal from a 4.9152-megahertz crystal on the EM board installed at Y2 (XTAL).
MCU Suffix Select Header, W4 Settings other than those described here are not currently supported. (Use only one jumper in this header.)		**8:** Specifies an MCU suffix of 8 (ex., QT8, QY8 or QB8). **Factory setting**
		**1:** Specifies an MCU suffix of 1 (ex., QT1 or QY1).
		**2:** Specifies an MCU suffix of 2 (ex., QL2, QT2 or QY2).

Table 2-1 Configuration Components (Continued)

Component	Position	Effect
		**3:** Specifies an MCU suffix of 3 (ex., QL3).
		**4:** Specifies an MCU suffix of 4 (ex., QL4, QT4, QY4 or QB4).
		**5:** Specifies an MCU suffix of 5 (Not Supported).
MCU Family Select Header, W5		**QB:** Specifies emulation of a QB family MCU **Factory setting**
		**QTQY:** Specifies emulation of a QT or QY family MCU.
		**QL:** Specifies emulation of a QL family MCU. Note: Eemulation is only valid for the alpha version of the QL family MCUs.

2.3 Remaining System Installation

When you have configured jumper headers, you are ready to complete M68EML08QBLTY installation:

- To install the M68EML08QBLTY in an MMDS0508 station module, remove the panel from the station module top. Fit together EM connectors P1 and P2 (on the bottom of the board) and platform-board connectors P11 and P12, respectively. Snap the corners of the EM onto the plastic standoffs. Connect the target cable, if appropriate, then replace the panel.
- If your M68EML08QBLTY already is installed in the station module, reconnect the target cable (if necessary). Replace the panel.
- To install the M68EML08QBLTY on an MMEVS platform board, fit together EM connectors P1 and P2 (on the bottom of the board) and platform-board connectors P11 and P12, respectively. Snap the corners of the EM onto the plastic standoffs.
- *If you will use the P&E development software*, copy personality files 00C75Vxx.mem, 00C76Vxx.mem, and 00C7EVxx.mem from the documentation CD-ROM to the installation directory that contains file `MMDS08.EXE or MMEVS08.EXE`. Then rename these files to 00475Vxx.mem, 00476Vxx.mem, and 0047EVxx.mem respectively.
- *If you will use the CodeWarrior IDE development software*, copy personality files 00C75Vxx.mem, 00C76Vxx.mem, and 00C7EVxx.mem from the documentation CD-ROM to the `...\prog\mem` subdirectory of the CodeWarrior IDE installation directory.

  Additionally, if you will use CodeWarrior IDE development software, you will need to copy the M68EML08QBLTY register files MCU0C75.reg, MCU0C76.reg, and MCU0C7E.reg from the documentation CD-ROM to the `...\prog\reg` subdirectory of the CodeWarrior IDE installation directory. The CodeWarrior IDE uses these files to implement optional functionality such as letting you view or modify register contents by name rather than by address. A register file is an ASCII text file, which you may customize. (The CodeWarrior IDE user's manual explains how to create and use such files.)

At this point, you are ready to make any remaining cable connections and apply power. For instructions, consult the MMDS or MMEVS operations manual.

2.4 Limitations

Limitations listed here apply to using your M68EML08QBLTY versus using the actual MCU in your target system:

Limitation 1 - Port A Data Register (PORTA): If you set PORT A Data Direction register bit 6, then PORT A Data register (DDRA) bit 6, indicating and auto-wakeup interrupt, will not read correctly. You should always clear DDRA bit 6..

Limitation 2 - Data Direction Register A (DDRA): It is possible to set bit 2 of DDRA as an output. This will cause PORT A bit 2 not to read as an input, but as what you set in the data register. You should always clear DDRA bit 2.

Limitation 3 - Port A and B Input Pullup Enable Register (PTAPUE and PTBPUE): All bits of PTAPUE are write-only and their values will not be displayed correctly when read. Bits 6 and 7 of PTBPUE are write only and their values are 0 when read. You should not use read-modify-write operations on these registers (such as BCLR or BSET instructions). When emulating QB4, QB8, or QT/QY8 the Port A Pullup register (PTAPUE) is located at $0D instead of $0B.

Limitation 4 - Configuration Register 2 (CONFIG2): Out of reset, bit 0 will always read 1. Once you modify this register it will read correctly. All other bits read and write as expected. All bit functionality is as expected.

Limitation 5 - Configuration Register 2 (CONFIG2): When emulating QB4 or QB8 the RST_B Pin Function Selection bit (RSTEN) and the ESCI Baud Rate Clock Source bit (ESCIBDSRC) of the CONFIG2 register should be swapped such that RSTEN is programmed at bit 2 and ESCIBDSRC is programmed at bit 0.

Limitation 6 - Oscillator Status, Control and Trim Registers (OSCSTAT, OSCTRIM, and OSCSC): When emulating a QT/QY family MCU, out of reset OSCSTAT will read 0x20 instead of 0x00 at address 0x36. Bit 0 (EGCST) will not reflect the status of the external clock at address 0x36. At address 0x36, bits 0 thru 2 will not always read back what was written. When emulating a QL family MCU (alpha version only), this register will also exist and be fully functional in all respects for reading and writing at address 0x51, but will have the above limitations at location 0x36. If using it at address 0x36, you should not use read-modify-write operations (such as BSET or BCLR instructions). When emulating a QB family MCU, this register is the OSCSC register and you can not write 01 to ICFS1 and ICFS0 directly. You must first clear these bits and then you can write the value 01.

The OSCTRIM register will always read 0x00 at address 0x38 but can be written. When emulating a QL family MCU, this register will also exist and be fully functional in all respects for reading and writing at address 0x52, but will have the above limitations at location 0x38. If using it at address 0x38, you should not use read-modify-write operations (such as BSET or BCLR instructions).

Limitation 7 - ADC Input Clock Register (ADICLK): When emulating a QT or QY family MCU, out of reset the emulator will use a 10-bit A/D instead of 8-bit as expected in those parts. You must explicitly change to 8-bit mode to correctly emulate those MCUs. See the QL chip data book for more details on how to change from 10-bit to 8-bit mode.

Limitation 8 - Crystals: You should not change the value of crystal Y2. You may change the oscillator at Y1 to any value within the range specified for the external clock in the data book.

Limitation 9 - TCLK: The TCLK timer clock function on PTA2 is not functional on the emulator. When this function is enabled, the pin on the emulator has no function.

Limitation 10 - Factory Trimming: There is a factory trim value located at address 0xFFC0 when you first power on the emulator. You may overwrite this value as if it were flash. After a normal reset it will maintain the value you have set. This value can be copied to the trim register and used if you are operating at 5V and you are using the default internal bus frequency option. Other modes of operation will require other unprovided trim values to have a trimmed internal clock frequency.

Limitation 11 - QL Emulation: Only the alpha version of the QL is supported. This emulator will not support the clock options of the final version of the QL. In the OSCSTAT register, ICFS bits are not supported. The BFS bit is supported.

Limitation 12 - SPI Registers and Vectors: When emulating the QB/QY MCUs, the SPI registers and vectors are located in the following locations which does not match the actual silicon:

$10 - SPCR
$11 - SPSCR
$12 - SPDR

$FFE8 - SPI TX Vector High
$FFE9 - SPI TX Vector Low
$FFEA - SPI RX Vector High
$FFEB - SPI RX Vector Low

Limitation 13 - ESCI Registers and Vectors: When emulating the QB/QY MCUs, the ESCI registers and vectors are located in the following locations which does not match the actual silicon:

$13 - SCC1
$14 - SCC2
$15 - SCC3
$16 - SCS1
$17 - SCS2
$18 - SCDR
$19 - SCBR
$09 - SCPSC
$0A - SCIACTL
$0B - SCIADAT

$FFE2 - ESCI TX Vector High
$FFE3 - ESCI TX Vector Low
$FFE4 - ESCI RX Vector High
$FFE5 - ESCI RX Vector Low
$FFE6 - ESCI Error Vector High
$FFE7 - ESCI Error Vector Low

Limitation 14 - TIMER Registers and Vectors: When emulating the QB/QY MCUs, the TIMER registers and vectors are located in the following locations which does not match the actual silicon:

$2B - TSC
$2C - TCNTH
$2D - TCNTL
$2E - TMODH
$2F - TMODL
$30 - TSC0
$31 - TCH0H
$32 - TCH0L
$33 - TSC1
$34 - TCH1H
$35 - TCH1L
$456 - TSC2
$457 - TCH2H
$458 - TCH2L
$459 - TSC3
$45A - TCH3H
$45B - TCH3L

$FFD0 - TIM CH3 Vector High
$FFD1 - TIM CH3 Vector Low
$FFD2 - TIM CH2 Vector High
$FFD3 - TIM CH2 Vector Low
$FFEC - TIM Overflow Vector High
$FFED - TIM Overflow Vector Low
$FFEE - TIM CH1 Vector High
$FFEF - TIM CH1 Vector Low
$FFF0 - TIM CH0 Vector High
$FFF1 - TIM CH0 Vector Low

Limitation 15 - Keyboard Polarity Register (KBIPR): The keyboard polarity register (KBIPR) is located at $08.

2.5 Running the Automated Board Test

This section explains how to test the EML08QBLTY emulation module using test software located on the included documentation CD-ROM. This test allow you to verify the proper operation of your board.

2.5.1 Set up the hardware

Follow the setup steps outlined in the Quickstart section of this user's manual. You must have the CodeWarrior IDE for HC08V3.0 or later installed on your computer to run this test. Do not connect the emulator board to your target system during this test.

2.5.2 Install the test software

The factory ships the EML08QBLTY with the test software. Double-click the file EML08QBLTY_Test.exe on the included documentation CD-ROM to run the setup program and follow the installation instructions. You must install this softare in the default location.

2.5.3 Run the test

Run the test by choosing Programs -> EML08QBLTY -> EML08QBLTY in the Windows Start Menu. Then follow the steps below:

- Click on the *Setup* button and verify that your hardware is connected as shown in the diagram. Click *Hide* to close the diagram.
- Click on the *Initial/Final Jumper Configuration* button and verify that the jumper setting on your board match the diagram. Verify that you have the factory installed 32.768kHz oscillator in location Y2. Click *Hide* to close the diagram.
- Apply power to the emulator.
- Click on the *Test* button.
- Click *OK* when you are ready to run the test.
- Move the jumpers as directed during the test.
- When the test is complete, you can verify that each item tested passed by checking that its box is green. The message window also displays the results of each test.

- You may now either run the test again or exit this program by clicking on the *Exit* button.

Section 3. Support Information

3.1 Introduction

This section consists of connector pin assignments, connector signal descriptions, and other information that may be useful in your development activities.

3.2 Target Connector J1

Connector J1 is the M68EML08QBLTY target connector. Figure 3-1 and Table 3-1 give the pin assignments and signal descriptions for connector J1.

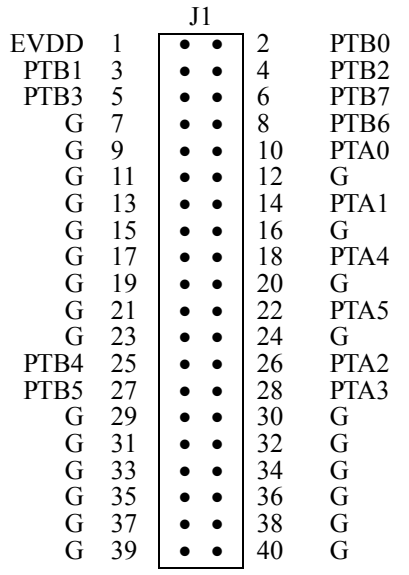


Figure 3-1 Target Connector (J1) Pin Assignments

Table 3-1 Target Connector (J1) Signal Descriptions

Pin	Label	Signal
1	EVDD	EXTERNAL VOLTAGE DETECT — Input signal that detects target-system power-up.
7, 9, 11, 12, 13, 15, 16, 17, 19, 20, 21, 23, 24, 29 — 40	G	GROUND
2 — 6, 8, 25, 27	PB0 — PB7	PORT B (lines 0—7) — General-purpose I/O lines controlled by software via data direction and data registers.
10, 14, 18, 22, 26, 28	PA0 — PA5 (not in exact order)	PORT A (lines 0—5) — General-purpose I/O lines controlled by software via data direction and data registers.

3.3 Logic Analyzer Connectors J2 and J13

Connectors J2 and J13 are the M68EML08QBLTY logic analyzer connectors. Figure 3-2 and Table 3-2 give pin assignments and signal descriptions for connector J2, which has pod 1 signals. Figure 3-3 and Table 3-3 give pin assignments and signal descriptions for connector J13, which has pod 2 signals.

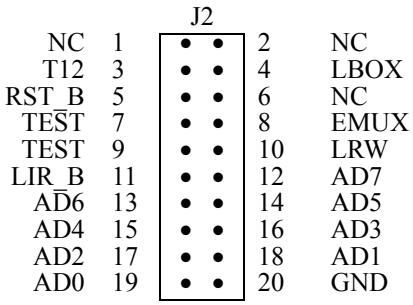


Figure 3-2 Logic Analyzer Connector J2 Pin Assignments

Table 3-2 Logic Analyzer Connector J2 Signal Descriptions

Pin	Label	Signal
1, 2, 6	NC	No connection
3	T12	SYSTEM BUS CLOCK — Clock that matches the internal emulation MCU bus clock
4	LBOX	LAST BUS CYCLE — Output signal that the emulator asserts to indicate that the target system MCU is in the last bus cycle of an instruction.
5	RST_B	COP RESET — Active-low output signal indicating (1) the target driving its reset pin, or (2) the platform board driving a reset to the emulator module.
7, 9	TEST	Test pins are used only during system development and factory test.
8	EMUX	EMLMUX - Muxed versions of R/W, LIR, and LAST.
10	LRW	LATCHED READ/WRITE — Output signal from the target MCU. If high, the target MCU is reading. If low, the target MCU is writing.
11	LIR_B	LOAD INSTRUCTION REGISTER — Active-low output signal indicating that the target MCU is fetching an instruction.
12 — 19	AD7 — AD0	PFB DATA BUS (lines 7—0) — Outputs the data lines going to the platform board.
20	GND	GROUND

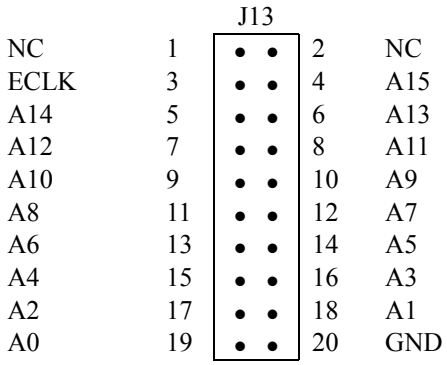


Figure 3-3 Logic Analyzer Connector J13 Pin Assignments

Table 3-3 Logic Analyzer Connector J13 Signal Descriptions

Pin	Label	Signal
1, 2	NC	No connection
3	ECLK	EM CLOCK — Output clock signal for the emulator module.
4 — 19	A15 — A0	LATCHED ADDRESS BUS (lines 15—0) — Output showing the address of the current bus cycle.
20	GND	GROUND

3.4 Inverted Clock Connector J11

Connector J11 is the source for an inverted clock signal. Figure 3-4 and Table 3-4 give the pin assignments and signal descriptions for this connector. You can connect this signal to your target system if you will use the OSC2 signal.

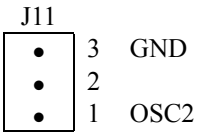


Figure 3-4 Connector J11 Pin Assignments

Table 3-4 Connector J11 Signal Descriptions

Pin	Label	Signal
3	GND	Ground
2		No connection
1	OSC2	OSC2 OUTPUT — Inversion of the clock signal that jumper header W2 specifies if you select the external clock. Inversion of the ICR clock if you select the internal clock (default). This signal behaves like the OSC2 pin function, meaning you must set the OSC2EN bit in the PTAPUE register and not have selected external clock in the CONFIG2 for the clock to be available on this header.

3.5 Analog-to-Digital Converter Reference Voltage Connector E3

Connector E3 is the source for the filtered A/D reference voltages. Figure 3-5 and Table 3-5 give the pin assignments and signal descriptions for this connector. The factory test uses this connection.

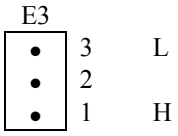


Figure 3-5 Connector E3 Pin Assignments

Table 3-5 Connector E3 Signal Descriptions

Pin	Label	Signal
3	L	LOW REFERENCE VOLTAGE
2	A/D REF	No connection (label only)
1	H	HIGH REFERENCE VOLTAGE

3.6 Board Factory Test Connectors J12 and J14

These connectors are used in the factory and during product development. They may not be populated.

3.7 Clock oscillator Y2

When you select the EM option on jumper W3 (jumper on pins 1-2), the clock signal generated by Y2 is supplied to the external inputs of the MCU. You can replace Y2 with another compatible clock oscillator to provide a different clock frequency (see the schematic on the user documentation CD-ROM, page 6).

3.8 EM Board Socket Connectors P1 and P2

Connectors P1 and P2 connect the M68EML08QBLTY to the platform board. Figure 3-6 and Table 3-6 give pin assignments and signal descriptions for connector P1. Figure 3-7 and Table 3-7 give pin assignments and signal descriptions for connector P2.

P1

A			B			C		
•	A1	LA[14]	•	B1	PFB_AD[7]	•	C1	GND
•	A2	LA[13]	•	B2	PFB_AD[6]	•	C2	GND
•	A3	LA[12]	•	B3	PFB_AD[5]	•	C3	GND
•	A4	LA[11]	•	B4	PFB_AD[4]	•	C4	GND
•	A5	LA[10]	•	B5	PFB_AD[3]	•	C5	GND
•	A6	LA[9]	•	B6	PFB_AD[2]	•	C6	GND
•	A7	LA[8]	•	B7	PFB_AD[1]	•	C7	GND
•	A8	LA[7]	•	B8	PFB_AD[0]	•	C8	GND
•	A9	LA[6]	•	B9	LIR_B	•	C9	GND
•	A10	LA[5]	•	B10	LRW	•	C10	GND
•	A11	LA[4]	•	B11	SCLK	•	C11	GND
•	A12	LA[3]	•	B12	T12CLK	•	C12	GND
•	A13	LA[2]	•	B13	NC	•	C13	GND
•	A14	LA[1]	•	B14	NC	•	C14	GND
•	A15	LA[0]	•	B15	NC	•	C15	GND
•	A16	LA[15]	•	B16	NC	•	C16	GND
•	A17	NC	•	B17	INTERNAL_B	•	C17	GND
•	A18	NC	•	B18	NC	•	C18	GND
•	A19	PFB_IRQ_B	•	B19	SWITCH_B	•	C19	GND
•	A20	CHRGPMP	•	B20	NC	•	C20	GND
•	A21	NC	•	B21	NC	•	C21	GND
•	A22	NC	•	B22	NC	•	C22	GND
•	A23	PFB_OSC	•	B23	NC	•	C23	GND
•	A24	NC	•	B24	LBOX	•	C24	GND
•	A25	NC	•	B25	BREAK_B	•	C25	GND
•	A26	NC	•	B26	NC	•	C26	GND
•	A27	NC	•	B27	NC	•	C27	GND
•	A28	NC	•	B28	NC	•	C28	GND
•	A29	NC	•	B29	NC	•	C29	GND
•	A30	NC	•	B30	NC	•	C30	GND
•	A31	PFB_VCC	•	B31	PFB_VCC	•	C31	GND
•	A32	GND	•	B32	GND	•	C32	GND

Figure 3-6 EM Connector P1 Pin Assignments

Table 3-6 EM Connector P1 Signal Descriptions

Pin	Mnemonic	Signal
A1 — A16	LA[15] — LA[0] (not in exact order)	LATCHED ADDRESS BUS (lines 15—0) — Output lines for addressing external devices.
A17, A18, A21, A22, A24 — A30	NC	No connection
A19	PFB_IRQ_B	PFB INTERRUPT — Active-low signal that requests an interrupt of the platform board.
A20	CHRGPMP	CHARGE PUMP — 12-volt signal (from the platform board).
A23	PFB_OSC	PFB OSCILLATOR — Oscillator clock signal from the platform board.
A31	PFB_VCC	PFB POWER — Operating voltage signal from the platform board.
A32	GND	GROUND
B1 — B8	PFB_AD[7] — PFB_AD[0]	PFB ADDRESS (lines 7—0) — Address of the current bus cycle.
B9	LIR_B	LOAD INSTRUCTION REGISTER — Active-low signal that the target MCU is fetching an instruction.
B10	LRW	LATCHED READ/WRITE — Input signal from the target MCU. If high, the target MCU is reading. If low, the target MCU is writing.
B11	SCLK	SERIAL CLOCK — Output clock signal to the platform board.
B12	T12CLK	T12 CLOCK — Matches the internal bus clock of the emulation MCU.
B13 — B16, B18, B20 — B23, B26 — B30	NC	No connection
B17	INTERNAL_B	INTERNAL RESOURCE — Active-low input signal indicating (1) that the current address is a target-MCU internal resource, or (2) that the EM board recreated the current address.
B19	SWITCH_B	SWITCH CONTROL — Active-low input signal that controls switches into the foreground map.
B24	LBOX	LAST BUS CYCLE — Input signal that the emulator asserts to indicate that the target system MCU is in the last bus cycle of an instruction.
B25	BREAK_B	BREAK REQUEST — Active-low output signal that requests a switch to background logic.
B31	PFB_VCC	PFB POWER — Operating voltage signal from the platform board.
B32	GND	GROUND
C1 — C32	GND	GROUND

P2

A			B			C		
•	A1	GND	•	B1	GND	•	C1	GND
•	A2	GND	•	B2	VCC	•	C2	VCC
•	A3	GND	•	B3	PTC[0]	•	C3	PTA[0]
•	A4	GND	•	B4	PTC[1]	•	C4	PTA[1]
•	A5	GND	•	B5	PTC[2]	•	C5	PTA[2]
•	A6	GND	•	B6	PTC[3]	•	C6	PTA[3]
•	A7	GND	•	B7	PTC[4]	•	C7	PTA[4]
•	A8	GND	•	B8	NC	•	C8	PTA[5]
•	A9	GND	•	B9	NC	•	C9	PTA[6]
•	A10	GND	•	B10	NC	•	C10	NC
•	A11	GND	•	B11	LOCKOUT_B	•	C11	PTB[7]
•	A12	GND	•	B12	T_RESET_5V_B	•	C12	PTB[6]
•	A13	GND	•	B13	NC	•	C13	PTB[5]
•	A14	GND	•	B14	PORTS_B	•	C14	PTB[4]
•	A15	GND	•	B15	NC	•	C15	PTB[3]
•	A16	GND	•	B16	PFB_RST_B	•	C16	PTB[2]
•	A17	GND	•	B17	COP_RST_B	•	C17	PTB[1]
•	A18	GND	•	B18	NC	•	C18	PTB[0]
•	A19	GND	•	B19	NC	•	C19	ID9
•	A20	GND	•	B20	NC	•	C20	ID8
•	A21	GND	•	B21	NC	•	C21	ID7
•	A22	GND	•	B22	NC	•	C22	ID6
•	A23	GND	•	B23	NC	•	C23	NC
•	A24	GND	•	B24	NC	•	C24	NC
•	A25	GND	•	B25	NC	•	C25	ID3
•	A26	GND	•	B26	NC	•	C26	ID2
•	A27	GND	•	B27	NC	•	C27	MCU_ID1
•	A28	GND	•	B28	VPRU	•	C28	MCU_ID0
•	A29	GND	•	B29	NC	•	C29	NC
•	A30	GND	•	B30	EVDD	•	C30	DAVINCI
•	A31	GND	•	B31	PFB_VCC	•	C31	PFB_VCC
•	A32	GND	•	B32	GND	•	C32	GND

Figure 3-7 EM Connector P2 Pin Assignments

Table 3-7 EM Connector P2 Signal Descriptions

Pin	Mnemonic	Signal
A1 — A32	GND	GROUND
B1, B32	GND	GROUND
B2	VCC	POWER — Operating voltage.
B3 — B7	PTC[0] — PTC[4]	PORT C (lines 0—4) — General-purpose I/O lines controlled by software via data direction and data registers.
B8 — B10, B13, B15, B18 — B27, 29	NC	No connection
B11	LOCKOUT_B	Used by the platform board to block the IRQ_B signal during reset recovery.
B12	T_RESET_5V_B	Target reset used to sense and drive resets to and from the target.
B14	PORTS_B	Indicates a port-related register access, which is routed to the PRU on the platform board.
B16	PFB_RST_B	PFB RESET — Active-low signal that requests a reset of the platform board.
B17	COP_RST_B	COP RESET — Active-low signal that resets the EM board.
B28	VPRU	Emulation MCU voltage used by the port replacement unit on the platform board.
B31	PFB_VCC	PFB POWER — Operating voltage signal from the platform board.
C1, C32	GND	GROUND
C2	VCC	POWER — Operating voltage.
C3 — C9	PTA[0] — PTA[7]	PORT A (lines 0—7) — General-purpose I/O lines controlled by software via data direction and data registers.
C10, C23, C24, C29	NC	No connection
C11 — C18	PTB[7] — PTB[0]	PORT B (lines 0—7) — General-purpose I/O lines controlled by software via data direction and data registers.
C19 — C22, C25 — C28	ID9 — ID6, ID3, ID2, MCU_ID1, MCU_ID0	MCU identification signals used by the platform board to detect which EM board is inserted.
C30	DAVINCI	Used to indicate HC05 or HC08 EM boards.
C31	PFB_VCC	PFB POWER — Operating voltage signal from the platform board.

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