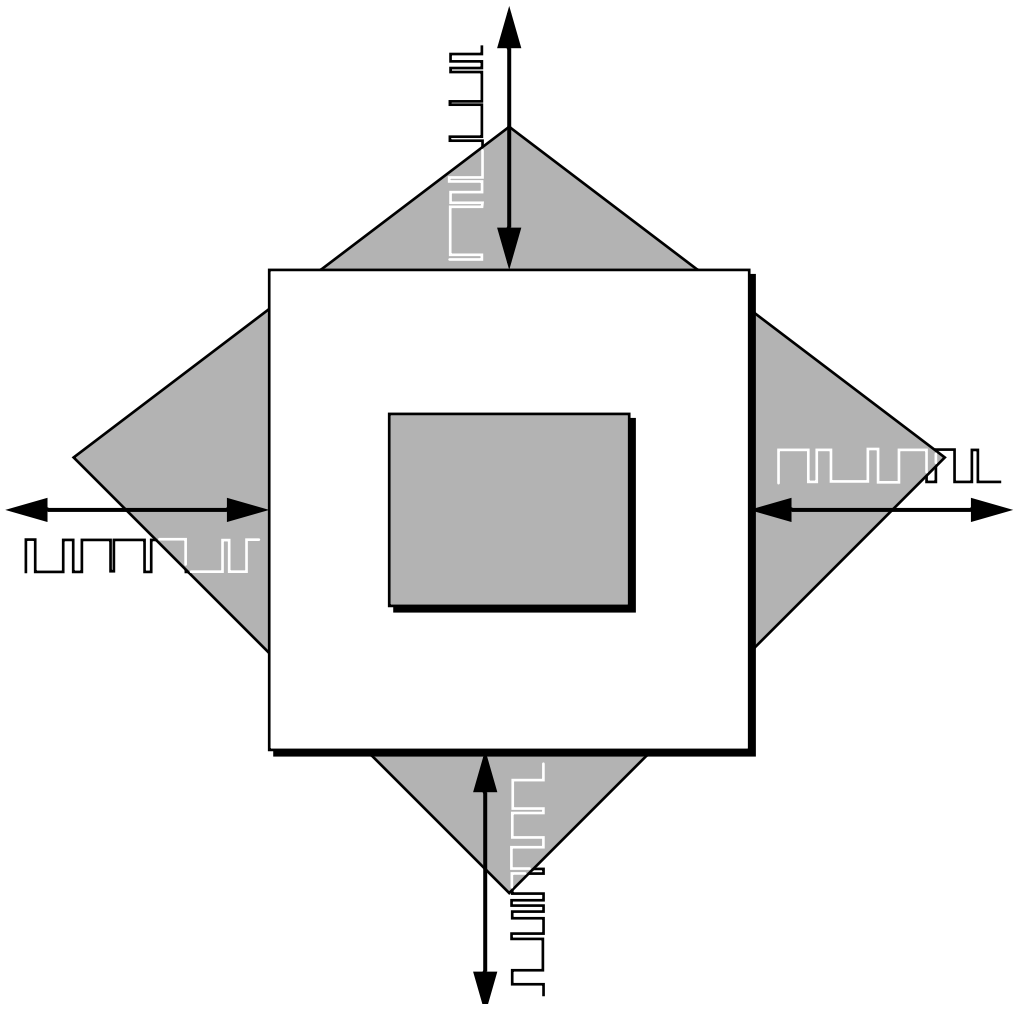
SECTION 8

SYNCHRONOUS SERIAL INTERFACE



8.1 INTRODUCTION

This section presents the Synchronous Serial Interface (SSI) and discusses its architecture, programming model, operating modes, and initialization. The capabilities of the SSI include:

- Independent (asynchronous) or shared (synchronous) transmit and receive sections with separate or shared internal / external clocks and frame syncs
- Normal mode operation using frame sync
- Network mode operation with as many as 32 time slots
- Programmable word length (8, 12, or 16 bits)
- Program options for frame synchronization and clock generation

The DSP56602 provides two independent, identical SSIs. (For simplicity, a single SSI is described in this section.) Each SSI provides a full-duplex serial port for communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals that implement the Motorola Serial Peripheral Interface (SPI). The SSI consists of independent transmitter and receiver sections and a common SSI clock generator. SSI pins can also be configured for use as General Purpose I / O (GPIO) pins when not used by the SSI. **Figure 8-1** shows a block diagram of the SSI.

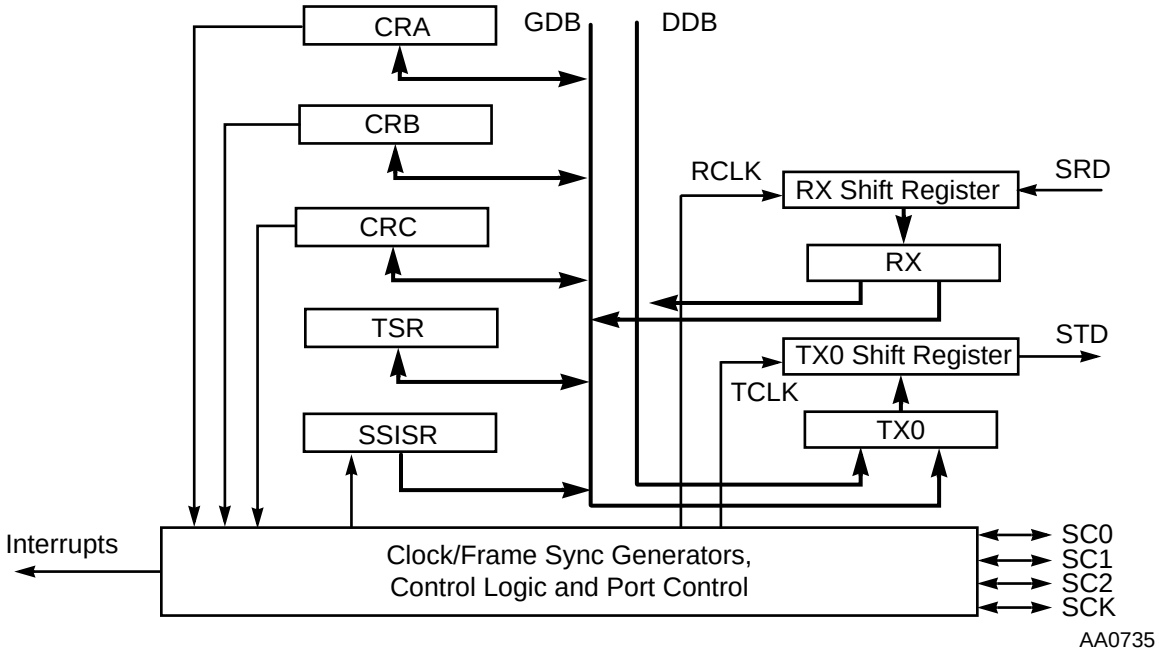


Figure 8-1 SSI Block Diagram

8.2 SSI DATA AND CONTROL PINS

Each SSI provides the following signal connections:

- SC0—Serial Control Pin 0
- SC1—Serial Control Pin 1
- SC2—Serial Control Pin 2
- SCK—Serial Clock Pin
- SRD—Serial Receive Data Pin
- STD—Serial Transmit Data Pin

8.2.1 Serial Control 0 (SC0)

The function of the Serial Control 0 (SC0) pin is determined by the selection of either Synchronous or Asynchronous mode (see **Table 8-3** on page 8-11). In Asynchronous mode, this pin is used for the receive clock I/O. In Synchronous mode, this pin is used for Serial I/O Flag 0. A typical application of flag I/O would be multiple device selection for addressing in codec systems. When this pin is configured as a serial flag pin, its direction is determined by the SCD0 bit in the SSI Control Register C (CRC) (see **Serial Control 0 Direction (SCD0)—Bit 2** on page 8-14). When configured as an output, this pin functions either as Serial Output Flag 0, based on control bit OF0 in the SSI Control Register B (CRB), or as a receive shift register clock output. When configured as an input, this pin is used either as Serial Input Flag 0, which controls the IF1 flag bit in the SSI Status Register (SSISR), or as a receive shift register clock input.

The SC0 pin can be programmed as a GPIO pin (PC0 on SSI0, and PD0 on SSI1) when the SSI SC0 function is not being used.

8.2.2 Serial Control 1 (SC1)

The function of the Serial Control 1 (SC1) pin is determined by the selection of either Synchronous or Asynchronous mode (see **Table 8-3** on page 8-11). In Asynchronous mode (such as a single codec with asynchronous transmit and receive), this pin provides the receiver frame sync I/O. In Synchronous mode, this pin is used for Serial I/O Flag 1 and operates like the previously described SC0. The SC0 and SC1 pins provide independent serial I/O flags, but can be used together for multiple serial device selection. The SC0 and SC1 pins can be used unencoded to select either one or two

codecs, or can be decoded externally to select as many as four codecs. If this pin is configured as a serial flag pin, its direction is determined by the SCD1 bit in the CRC (see **Serial Control 1 Direction (SCD1)—Bit 3** on page 8-14). When configured as an output, this pin provides either Serial Output Flag 1 (based on control bit OF1) or the receive frame sync signal. When configured as an input, this pin can be used as Serial Input Flag 1, which controls the IF1 flag bit in the SSI Status Register (SSISR), or as a receive frame sync from an external source.

The SC1 pin can be programmed as a GPIO pin (PC1 on SSI0, or PD1 on SSI1) when the SSI SC1 function is not being used.

8.2.3 Serial Control 2 (SC2)

The Serial Control 2 (SC2) pin is used for frame sync I/O. The SC2 pin provides frame synchronization for both the transmitter and receiver in Synchronous mode, and frame synchronization for the transmitter only in Asynchronous mode (see **Table 8-3** on page 8-11). The direction of this pin is determined by the SCD2 bit in the CRC (described in **Serial Control 2 Direction (SCD2)—Bit 4** on page 8-15). When configured as an output, this pin provides the internally generated frame sync signal. When configured as an input, this pin receives an external frame sync signal for the transmitter and the receiver in Synchronous mode, and for the transmitter only in Asynchronous mode.

The SC2 pin can be programmed as a GPIO pin (PC2 on SSI0, or PD2 on SSI1) when the SSI SC2 function is not being used.

8.2.4 Serial Clock (SCK)

The Serial Clock (SCK) pin is a bidirectional pin that provides the serial bit rate clock for the SSI. The SCK pin is a clock input or output used by the transmitter and receiver in Synchronous mode, or by only the transmitter in Asynchronous mode (see **Table 8-1**).

The SCK pin can be programmed as a GPIO pin (PC3 on SSI0, and PD3 on SSI1) when the SSI SCK function is not being used.

Table 8-1 SSI Clock Sources

SYN	SCKD	SCD0	Receive Clock Source	Receive Clock Out	Transmit Clock Source	Transmit Clock Out
Asynchronous Clock						
0	0	0	EXT, SC0	—	EXT, SCK	—
0	0	1	INT	SC0	EXT, SCK	—
0	1	0	EXT, SC0	—	INT	SCK
0	1	1	INT	SC0	INT	SCK
Synchronous Clock						
1	0	d.c.	EXT, SCK	—	EXT, SCK	—
1	1	d.c.	INT	SCK	INT	SCK

Note: Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (i.e., the system clock frequency must be at least three times the external SSI clock frequency). The SSI needs at least three DSP phases (DSP phase equals T) inside each half of the serial clock.

8.2.5 Serial Receive Data (SRD)

The Serial Receive Data (SRD) pin receives serial data and transfers the data to the Receive Shift Register. The SRD pin can be programmed as a GPIO pin (PC4 on SSI0, and PD4 on SSI1) when the SSI SRD function is not being used.

8.2.6 Serial Transmit Data (STD)

The Serial Transmit Data (STD) pin is used for transmitting data from the Transmit Shift Register. The STD pin is an output when data is being transmitted from the Transmit Shift Register. When using an internally generated bit clock, the STD pin is tri-stated after transmitting the last data bit when another data word does not follow immediately. If a data word follows immediately (within a full clock cycle), the STD pin is not tri-stated. The STD pin can be programmed as a GPIO pin (PC5 on SSI0, and PD5 on SSI1) when the SSI STD function is not being used.

8.3 SSI PROGRAMMING MODEL

The SSI contains the following registers:

- Interface control registers
  - CRA—Control Register A
  - CRB—Control Register B
  - CRC—Control Register C
- SSISR—SSI Status Register
- Data registers
  - TX—Transmit Data Register
  - RX—Receive Data Register
- Time Slot Register
- GPIO port registers
  - PCR—Port Control Register
  - PRR—Port Direction Register
  - PDR—Port Data Register

The registers described in this section represent one SSI. The DSP56602 chip has two identical SSIs. When programming the SSI, the user must ensure that the correct set of registers is used for the desired SSI. The following paragraphs describe the SSI registers.

8.3.1 SSI Control Register A (CRA)

The SSI Control Register A (CRA) is one of three 16-bit read / write control registers used to direct the operation of the SSI. The CRA controls the SSI clock generator bit and frame sync rates, word length, and number of words per frame for the serial data. **Figure 8-2** shows the programming model for the CRA. Hardware and software reset clear all the bits in the CRA.

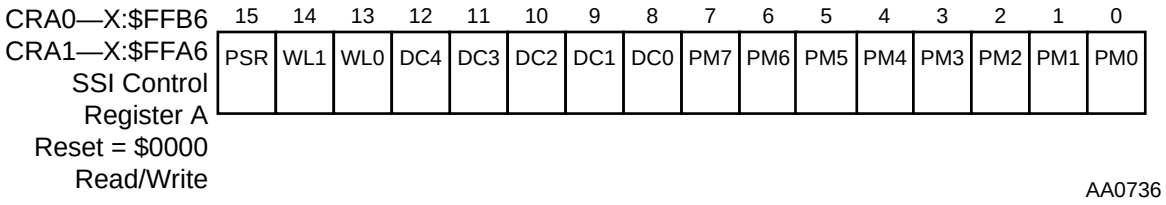


Figure 8-2 SSI Control Register A Programming Model

8.3.1.1 Prescale Modulus Select (PM[7:0])—Bits 0–7

The Prescale Modulus Select (PM[7:0]) bits specify the divide ratio of the prescale divider in the SSI clock generator. A divide ratio from 1 to 256 (PM[7:0] = 0 to $FF) can be selected. The bit clock output is available on the SCK pin or the SC0 pin. The bit clock output is also available internally for use as the bit clock to shift the Transmit Shift Register and the Receive Shift Register. Careful choice of the crystal oscillator frequency and the prescaler modulus allows the industry-standard codec master clock frequencies of 2.048 MHz, 1.544 MHz, and 1.536 MHz to be generated. Hardware and software reset clear the PM[7:0] bits.

Note: The combination PSR = 1 and PM[7:0] = $00 is reserved, and may cause synchronization problems if used.

8.3.1.2 Frame Rate Divider Control (DC[4:0])—Bits 8–12

The Frame Rate Divider Control (DC[4:0]) bits control the divide ratio for the programmable frame rate dividers used to generate the frame clocks. In Network mode, this ratio can be interpreted as the number of words per frame minus one. In Normal mode, this ratio determines the word transfer rate. The divide ratio ranges from 1 to 32 (DC[4:0] = 00000 to 11111) for Normal mode, and from 2 to 32 (DC[4:0] = 00001 to 11111) for Network mode.

In Network mode, a divide ratio of 1 (DC[4:0] = 00000) is a special case (On-Demand mode). In Normal mode, a divide ratio of 1 (DC[4:0] = 00000) provides continuous periodic data word transfers. In this case, a bit-length sync must be used. Hardware and software reset clear the DC[4:0] bits.

8.3.1.3 Word Length Control (WL[1:0])—Bits 13–14

The Word Length Control (WL[1:0]) bits are used to select the length of the data words being transferred via the SSI. Word lengths of 8, 12, or 16 bits can be selected according to the assignment described in **Table 8-2**. Hardware and software reset clear the WL1 and WL0 bits.

Table 8-2 SSI Word Length Selection

WL1	WL0	Number of Bits Per Word
0	0	8
0	1	12
1	0	16
1	1	Reserved

8.3.1.4 Prescaler Range (PSR)—Bit 15

The Prescaler Range (PSR) bit controls a fixed divide-by-eight prescaler in series with the variable prescaler. This bit extends the prescaler range for those cases in which a slower bit clock is desired. The minimum internally generated bit clock frequency is:

fosc / 2 / 8 / 256 = fosc / 4096

The maximum internally generated bit clock frequency is fosc / 4. When the PSR bit is set, the fixed prescaler is bypassed. When the PSR bit is cleared, the fixed divide-by-eight prescaler is used. Hardware and software reset clear the PSR bit.

Note: The combination PSR = 1 and PM[7:0] = $00 is reserved, and may cause synchronization problems if used.

8.3.2 SSI Control Register B (CRB)

The SSI Control Register B (CRB) is one of three 16-bit read / write control registers used to direct the operation of the SSI. The CRB controls the serial output flag, the SSI interrupts enables, and transmitter and receiver enable. The CRB bits are described in the following paragraphs. **Figure 8-3** shows the programming model for the CRB. Hardware and software reset clear all the bits in the CRB.

CRB0—X:$FFB7
CRB1—X:$FFA7
SSI Control Register B
Reset = $0000
Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REIE	TEIE	RLIE	TLIE	RIE	TIE	RE	TE	*	*	*	*	*	*	OF1	OF0

* Indicates reserved bits, read as 0 and should be written with 0 for future compatibility

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Figure 8-3 SSI Control Register B Programming Model

8.3.2.1 Serial Output Flag 0 (OF0)—Bit 0

When the SSI is in the Synchronous mode (the SYN bit in the CRC is set) the SC0 pin is configured as Serial I/O Flag 0. When the SCD0 bit in the CRC is set, the SC0 pin is an output, and data present in the OF0 bit is written to the SC0 pin either at the beginning of the frame in Normal mode, or at the beginning of the next time slot in Network mode. Hardware and software reset clear the OF0 bit.

8.3.2.2 Serial Output Flag 1 (OF1)—Bit 1

When the SSI is in the Synchronous mode (the SYN bit in the CRC is set) the SC1 pin is configured as Serial I/O Flag 1. When the SCD1 bit in the CRC is set, the SC1 pin is an output, and data present in the OF1 bit is written to the SC1 pin either at the beginning of the frame in Normal mode, or at the beginning of the next time slot in Network mode. Hardware and software reset clear the OF1 bit. Hardware and software reset clear the OF1 bit.

The normal sequence for setting output flags when transmitting data is:

1. Wait for the TDE bit to be set, indicating the TX register is empty.
2. Write the OF0 and OF1 bits flags.
3. Write the transmit data to the TX register.

The OF0 and OF1 bits are double-buffered so that the flag states appear on the pins when the TX data is transferred to the transmit shift register (i.e., the flags are synchronous with the data).

Note: The optional serial output pins timing (SC0 and SC1) are controlled by the frame timing and are not affected by the TE or RE bits.

8.3.2.3 Reserved Bits—Bits 2–7

Bits 2–7 in the CRB are reserved bits. They read as 0 and must be written with 0 for future compatibility.

8.3.2.4 Transmit Enable (TE)—Bit 8

The Transmit Enable (TE) bit enables the transfer of data from the Transmit Data (TX) register to the Transmit Shift Register. When the TE bit is set and a frame sync is detected, the transmit portion of the SSI is enabled for that frame. When the TE bit is cleared, the transmitter is disabled after completing transmission of data currently in the Transmit Shift Register. The STD output pin is tri-stated, and any data present in the TX register is not transmitted. Data can be written to the TX register when the TE bit is cleared, but no data is transferred to the Transmit Shift Register.

The Normal mode transmit enable sequence is to write data to the TX register (or Transmit Shift Register) before setting the TE bit. The normal transmit disable sequence is to clear the TE, TIE, and TEIE bits after the TDE flag bit in the SSI Status Register (SSISR) is set.

In the Network mode, the operation of clearing and then resetting the TE bit disables the transmitter after completing transmission of the current data word until the beginning of the next frame. During that time period, the STD pin remains in the high-impedance state. Hardware reset and software reset clear the TE bit.

The On-Demand mode transmit enable sequence can be the same as the Normal mode, or TE can be left enabled.

Note: The TE bit does not affect the generation of frame sync or output flags.

Table 8-3 Mode and Pin Definition Table

Control Bits			SSI Pins					
SYN	**TE**	**RE**	**SC0**	**SC1**	**SC2**	**SCK**	**STD**	**SRD**
0	0	0	—	—	—	—	—	—
0	0	1	RXC	FSR	—	—	—	RD
0	1	0	—	—	FST	TXC	TD	—
0	1	1	RXC	FSR	FST	TXC	TD	RD
1	0	0	F0/U	F1/U	FS	XC	—	—
1	0	1	F0/U	F1/U	FS	XC	—	RD
1	1	0	F0/U	F1/U	FS	XC	TD	—
1	1	1	F0/U	F1/U	FS	XC	TD	RD

Table 8-3 Mode and Pin Definition Table (continued)

Control Bits			SSI Pins					
SYN	**TE**	**RE**	**SC0**	**SC1**	**SC2**	**SCK**	**STD**	**SRD**

Legend:

TXC	Transmitter Clock	FS	Transmitter/Receiver Frame Sync (Synchronous Operation)
RXC	Receiver Clock		
XC	Transmitter/Receiver Clock (Synchronous Operation)	TD	Transmit Data
		RD	Receive Data
FST	Transmitter Frame Sync	F0/U	Flag 0 / Unused
FSR	Receiver Frame Sync	F1/U	Flag 1 / Unused
		—	Unused (can be used as GPIO pin)

Note: A pin can be used for GPIO if its corresponding bit in the Port Control Register is cleared.

8.3.2.5 Receive Enable (RE)—Bit 9

The Receive Enable (RE) bit controls the receive portion of the SSI. When the RE bit is set, the receive portion of the SSI is enabled. When the RE bit is cleared, the receiver is disabled by inhibiting data transfer into the Receive Data (RX) register. If data is being received while the RE bit is cleared, the remainder of the word is shifted in and transferred to the RX register. The RE bit must be set in the Normal mode and On-Demand mode to receive data. In Network mode, the operation of clearing RE and then resetting it disables the receiver after reception of the current data word until the beginning of the next data frame. Hardware and software reset clear the RE bit.

Note: The RE bit does not affect the generation of a frame sync.

8.3.2.6 Transmit Interrupt Enable (TIE)—Bit 10

The Transmit Interrupt Enable (TIE) control bit enables transmit interrupts. When the TIE control bit and the TDE flag bit in the SSISR are set, the DSP is interrupted. When the TIE bit is cleared, the transmit interrupt is disabled. Writing to the TX register or to the Transmit Shift Register clears the TDE bit, thus clearing the interrupt.

Transmit interrupts with exception have higher priority than normal transmit data interrupts. Therefore, if an exception occurs (the TUE bit is set) and the TEIE bit is set, the SSI requests an SSI Transmit Data with Exception interrupt from the interrupt controller. Hardware and software reset clear the TIE bit.

8.3.2.7 Receive Interrupt Enable (RIE)—Bit 11

The Receive Interrupt Enable (RIE) bit enables the receive interrupt. When the RIE bit is set, the DSP is interrupted when the RDF bit in the SSISR is set. When the RIE bit is

cleared, this interrupt is disabled. Reading the RX register clears the RDF bit, thus clearing the pending interrupt.

Receive interrupts with exception have higher priority than normal receive data interrupts. Therefore, if an exception occurs (the ROE bit is set) and REIE is set, the SSI requests an SSI Receive Data with Exception interrupt from the interrupt controller. Hardware and software reset clear the RIE bit.

8.3.2.8 Transmit Last Slot Interrupt Enable (TLIE)—Bit 12

The Transmit Last Slot Interrupt Enable (TLIE) control bit enables an interrupt at the beginning of last slot of a frame in Network mode. When the TLIE bit is set, the DSP is interrupted at the start of the last slot in a frame in Network mode. When the TLIE bit is cleared, the Transmit Last Slot interrupt is disabled. The TLIE function is disabled when DC[4:0] = $0 (On-Demand mode). Hardware and software reset clear the TLIE bit. The use of the Transmit Last Slot interrupt is described in **SSI Exceptions** on page 8-23.

8.3.2.9 Receive Last Slot Interrupt Enable (RLIE)—Bit 13

The Receive Last Slot Interrupt Enable (RLIE) control bit enables an interrupt after the last slot of a frame ended in Network mode only. When the RLIE bit is set, the DSP is interrupted after the last slot in a frame has ended. When the RLIE bit is cleared, the Receive Last Slot interrupt is disabled. The RLIE bit is disabled when DC[4:0] = $0 (On-Demand mode). Hardware and software reset clear the RLIE bit. The use of the Receive Last Slot interrupt is described in **SSI Exceptions** on page 8-23.

8.3.2.10 Transmit Exception Interrupt Enable (TEIE)—Bit 14

When the Transmit Exception Interrupt Enable (TEIE) control bit is set, the DSP is interrupted when both the TDE and TUE bits in the SSISR are set. When the TEIE bit is cleared, this interrupt is disabled. Reading the SSISR followed by writing to the transmitter data registers clears the TUE bit, thus clearing the pending interrupt. Hardware and software reset clear the TEIE bit.

8.3.2.11 Receive Exception Interrupt Enable (REIE)—Bit 15

When the Receive Exception Interrupt Enable (REIE) control bit is set, the DSP is interrupted when both the RDF and ROE bits in the SSISR are set. When the REIE bit is cleared, this interrupt is disabled. Reading the SSISR followed by reading the receive data register clears the ROE bit, thus clearing the pending interrupt. Hardware and software reset clear the REIE bit.

8.3.3 SSI Control Register C (CRC)

The SSI Control Register C (CRC) is one of three 16-bit read / write control registers used to direct the operation of the SSI. The CRC controls the SSI multifunction pins, SC2, SC1,

and SC0, which can be used as clock inputs or outputs, frame synchronization pins or serial I/O flag pins. The direction control bits for the serial control pins are in the CRC. Operating modes are also selected in this register. Hardware and software reset clear all the bits in the CRC. The SSI CRC bits are described in the following paragraphs.
Figure 8-4 shows the programming model for the CRC. Hardware and software reset clear all the bits in the CRC.

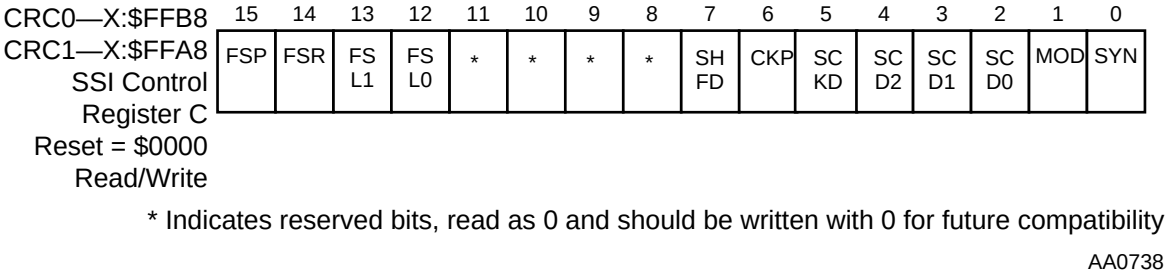

Figure 8-4 SSI Control Register C Programming Model

8.3.3.1 Asynchronous /Synchronous (SYN)—Bit 0

The Asynchronous/Synchronous (SYN) control bit selects whether the receive and transmit functions of the SSI occur synchronously or asynchronously with respect to each other. When the SYN bit is set, Synchronous mode is chosen and the transmit and receive sections use common clock and frame sync signals. When the SYN bit is cleared, Asynchronous mode is chosen and separate clock and frame sync signals are used for the transmit and receive sections. Hardware reset and software reset clear the SYN bit.

8.3.3.2 SSI Mode Select (MOD)—Bit 1

The SSI Mode Select (MOD) control bit selects the operational mode of the SSI. When the MOD bit is cleared, Normal mode is selected. When the MOD bit is set, Network mode is selected. In Normal mode, the Frame Rate Divider Control (DC4–DC0) bits determine the word transfer rate. One word can be transferred per frame sync during the frame sync time slot. In Network mode, a word can be transferred during every time slot. Hardware and software reset clear the MOD bit.

8.3.3.3 Serial Control 0 Direction (SCD0)—Bit 2

The Serial Control 0 Direction (SCD0) control bit selects the direction of the SC0 pin. When the SCD0 bit is set, the SC0 pin is an output. When the SCD0 bit is cleared, the SC0 pin is an input. Hardware and software reset clear the SCD0 bit.

8.3.3.4 Serial Control 1 Direction (SCD1)—Bit 3

The Serial Control 1 Direction (SCD1) control bit selects the direction of the SC1 pin. When the SCD1 bit is cleared, the SC1 pin is an input. When the SCD bit 1 is set, the SC1 pin is an output. Hardware and software reset clear the SCD1 bit.

8.3.3.5 Serial Control 2 Direction (SCD2)—Bit 4

The Serial Control 2 Direction (SCD2) control bit selects the direction of the SC2 pin. When the SCD2 bit is cleared, the SC2 pin is an input. When the SCD2 bit is set, the SC2 pin is an output. Hardware and software reset clear the SCD2 bit.

8.3.3.6 Clock Source Direction (SCKD)—Bit 5

The Clock Source Direction (SCKD) control bit selects the source of the clock signal used to clock the Transmit Shift register in the Asynchronous mode and the Transmit Shift register and the Receive Shift register in the Synchronous mode. When the SCKD bit is set in Asynchronous mode, the internal clock source becomes the bit clock for the Transmit Shift register and word length divider, and is the output on the SCK pin. When the SCKD bit is cleared, the clock source is external, the internal clock generator is disconnected from the SCK pin, and an external clock source can drive the SCK pin. Hardware and software reset clear the SCKD bit.

8.3.3.7 Clock Polarity (CKP)—Bit 6

The Clock Polarity (CKP) control bit controls on which bit the clock edge data and frame sync are clocked out and latched in. When the CKP bit is cleared, the data and the frame sync are clocked out on the rising edge of the transmit bit clock and latched in on the falling edge of the receive bit clock.When the CKP bit is set, the falling edge of the transmit clock is used to clock the data out and frame sync, and the rising edge of the receive clock is used to latch the data and frame sync in. Hardware and software reset clear the CKP bit.

8.3.3.8 Shift Direction (SHFD)—Bit 7

The Shift Direction (SHFD) control bit causes the Transmit Shift register to shift data out MSB first when SHFD is cleared, and LSB first when SHFD is set to 1. Received data is shifted in MSB first when SHFD is cleared or LSB first when SHFD equals 1. Hardware and software reset clear the SHFD bit.

8.3.3.9 Reserved Bits—Bits 8–11

Bits 8–11 in the CRC are reserved bits. They are read as 0 and should be written with 0 to ensure future compatibility.

8.3.3.10 Frame Sync Length (FSL[1:0])—Bits 12–13

The Frame Sync Length (FSL[1:0]) control bits select the length of frame sync to be generated or recognized. If FSL1 and FSL0 are both cleared, a word-length frame sync is selected for both TX and RX that is the length of the data word defined by bits WL1 and WL0. If the FSL1 bit is set and the FSL0 bit is cleared, a 1-bit clock period frame sync is selected for both TX and RX. When the FSL0 bit is set, the TX and RX frame syncs are different lengths. The FSL0 bit is ignored when the SYN bit is set. Encoding of the FSL1 and FSL0 bits is described in **Table 8-4**. Hardware reset and software reset clear FSL0 and FSL1.

Table 8-4 FSL[1:0] Encoding

FSL1	FSL0	Frame Sync Length
0	0	Word-length bit clock for both TX/RX
0	1	One-bit clock for TX and Word-length bit clock for RX
1	0	One-bit clock for both TX/RX
1	1	One-bit clock for RX and Word-length bit clock for TX

8.3.3.11 Frame Sync Relative Timing (FSR)—Bit 14

The Frame Sync Relative Timing (FSR) control bit determines the relative timing of the receive and transmit frame sync signal as referred to the serial data lines, for a word length frame sync only. When the FSR bit is set, the word length frame sync occurs one serial clock cycle earlier (i.e., together with the last bit of the previous data word). When the FSR bit is cleared, the word length frame sync occurs together with the first bit of the data word of the first slot. Hardware reset and software reset clear the FSR bit.

8.3.3.12 Frame Sync Polarity (FSP)—Bit 15

The Frame Sync Polarity (FSP) bit determines the polarity of the receive and transmit frame sync signals. When FSP is set, the frame sync signal polarity is negative (i.e., the frame start is signaled by the low level of the frame sync pin). When the FSP bit is cleared, the frame sync signal polarity is positive (i.e., the frame start is signaled by the high level of the frame sync pin). Hardware reset and software reset clear the FSP bit.

8.3.4 SSI Status Register (SSISR)

The SSI Status Register (SSISR) is an 8-bit read-only status register used by the DSP to read the status and serial input flags of the SSI. When the SSISR is read to the internal data bus, the register contents occupy the low-order byte of the data bus, and the remaining bits are read as 0. **Figure 8-5** shows the programming model for the SSISR.

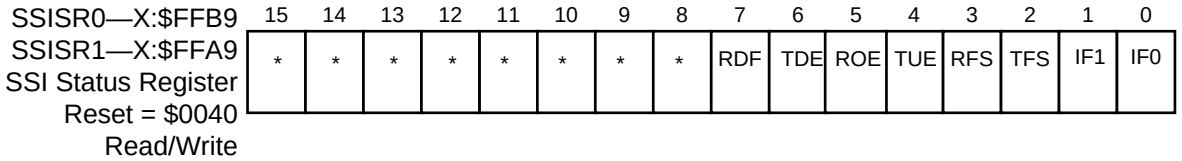

Figure 8-5 SSI Status Register Programming Model

8.3.4.1 Serial Input Flag 0 (IF0)—Bit 0

The SSI latches data present on the SC0 pin during reception of the first received bit after frame sync is detected. The IF0 bit is updated with this data when the Receive Shift Register is transferred into the RX register. The IF0 bit is enabled only when the SC0 pin is programmed as SSI in the PCR, the SYN bit is set, and the SCD0 bit (in the CRC) is cleared, indicating that SC0 is an input flag and the Synchronous mode is selected. Otherwise, the IF0 bit reads as a 0 when it is not enabled. Hardware, software, SSI individual, and STOP reset clear IF0.

8.3.4.2 Serial Input Flag 1 (IF1)—Bit 1

The SSI latches data present on the SC1 pin during reception of the first received bit after frame sync is detected.The IF1 bit is updated with this data when the Receive Shift Register is transferred into the RX register. The IF1 bit is enabled only when the SC1 pin is programmed as SSI in the PCR, the SYN bit is set, and the SCD1 bit (in the CRC) is cleared, indicating that SC1 is an input flag and Synchronous mode is selected. Otherwise, the IF1 bit is read as 0 when it is not enabled. Hardware, software, SSI individual, and STOP reset clear the IF1 bit.

8.3.4.3 Transmit Frame Sync Flag (TFS)—Bit 2

The Transmit Frame Sync Flag (TFS) bit indicates whether a transmit frame sync has occurred in the current time slot. The TFS bit is set at the start of the first time slot in the frame, and cleared during all other time slots. In Network mode, data written to a transmit data register during the time slot when the TFS bit is set is transmitted(if the transmitter is enabled) during the second time slot in the frame. The TFS bit is useful in Network mode to identify the start of a frame. The TFS bit is cleared by hardware, software, SSI individual, or STOP reset. The TFS bit is valid only if the transmitter is enabled (the TE bit in the CRB is set).

Note: In Normal mode, the TFS bit is always read as 1 when transmitting data because there is only one time slot per frame—the “frame sync” time slot.

8.3.4.4 Receive Frame Sync Flag (RFS)—Bit 3

When set, the Receive Frame Sync Flag (RFS) bit indicates that a receive frame sync occurred during reception of the word in the serial receive data register. This indicates that the data word is from the first time slot in the frame. In Network mode, when the RFS bit is cleared and a word is received, it indicates that the frame sync did not occur during reception of that word.

The RFS bit is cleared by hardware, software, SSI individual, or STOP reset. The RFS bit is valid only if the receiver is enabled by setting the RE bit in the CRB.

Note: In Normal mode, the RFS bit is always read as 1 when reading data because there is only one time slot per frame—the “frame sync” time slot.

8.3.4.5 Transmitter Underrun Error Flag (TUE)—Bit 4

The Transmitter Underrun Error Flag (TUE) bit indicates whether a transmit underrun error has occurred. The TUE bit is set when the Transmit Shift Register is empty (no new data is available to be transmitted) and a transmit time slot occurs. When a transmit underrun error occurs, the previous data, which is still present in the TX register that was not written, is retransmitted.

In Normal mode, a frame contains only one transmit time. In Network mode, a frame can contain as many as 32 transmit time slots.

If the TEIE bit is set, a DSP Transmit Underrun Error Interrupt request is issued when the TUE bit is set. Hardware, software, SSI individual, and STOP reset clear the TUE bit. The TUE bit is also cleared by reading the SSISR with this bit set, followed by writing to the transmit data registers or to TSR.

8.3.4.6 Receiver Overrun Error Flag (ROE)—Bit 5

The Receiver Overrun Error Flag (ROE) bit indicates that a receive overrun error has occurred. The ROE bit is set when the Receive Shift Register is filled and ready to transfer to the RX register and RX is already full (i.e., RDF = 1). If the REIE bit is set, a DSP Receiver Overrun Error Interrupt request is issued when the ROE bit is set. Hardware, software, SSI individual, and STOP reset clear the ROE bit. The ROE bit is also cleared by reading the SSISR with this bit set, followed by reading the RX register.

8.3.4.7 Transmit Data Register Empty (TDE)—Bit 6

The Transmit Data Register Empty (TDE) bit is set when the contents of the Transmit Data (TX) register is transferred to the Transmit Shift Register. This bit is also set for a TSR disabled time slot period in Network mode (as if data were being transmitted after the TSR was written). When set, the TDE bit indicates that data should be written to the TX register or to the Time Slot Register (TSR). The TDE bit is cleared when the DSP writes to the transmit data register, or when the DSP writes to the TSR to disable transmission of the next time slot. If the TIE bit is set, a DSP transmit data interrupt request is issued when the TDE bit is set. Hardware, software, SSI individual, and STOP reset set the TDE bit.

8.3.4.8 Receive Data Register Full (RDF)—Bit 7

The Receive Data Register Full (RDF) bit is set when the contents of the receive shift register are transferred to the receive data register. The RDF bit is cleared when the DSP reads the SSI Receive Data Register (RX) or cleared by hardware, software, SSI individual, or STOP reset. If the RIE bit (in the CRB) is set, a DSP receive data interrupt request is issued when the RDF bit is set.

8.3.4.9 Reserved Bits—Bits 8–15

Bits 8–15 are reserved for future use. They are read as 0 and should be written with 0 for future compatibility.

8.3.5 Receive Shift Register

The Receive Shift Register is a 16-bit shift register that receives the incoming data from the SRD pin. Data is shifted in by the selected bit clock (internal or external) when the associated frame sync I/O is asserted. Data is received LSB first if the SHFD bit (in the CRC) is set, and MSB first if the SHFD bit is cleared. Data is transferred to the Receive Data Register after 8, 12, or 16 serial clock cycles are counted, depending on the Word Length (WL1–0) bits in the CRA.

8.3.6 Receive Data Register (RX)

The Receive Data Register (RX) is a 16-bit read-only register that accepts data from the Receive Shift Register as it becomes full. The data read occupies the Most Significant Portion of the RX register. The unused bits (Least Significant Portion) are read as 0. If the associated interrupt is enabled, the DSP is interrupted whenever the RX register becomes full.

8.3.7 Transmit Shift Register

The Transmit Shift Register is a 16-bit shift register that contain the data being transmitted. Data is shifted out to the Serial Transmit Data (STD) pin by the selected bit clock (internal or external) when the associated frame sync I/O is asserted. Depending on the Word Length (WL1–0) bits in the CRA, the number of bits shifted out before the Transmit Shift Register is considered empty and can be written to again is 8, 12, or 16 bits. The data to be transmitted occupies the Most Significant Portion of the shift register. The unused portion of the register is ignored. Data is shifted out of this register LSB first if the SHFD bit (in the CRC) is set, and MSB first if the SHFD bit is cleared. (This is the same direction as the Receive Shift Register.)

8.3.8 Transmit Data Register (TX)

The Transmit Data (TX) register is a 16-bit write-only register. Data to be transmitted is written into this register and is automatically transferred to the transmit shift register. The data written (8, 12 or 16 bits) should occupy the Most Significant Portion of the TX. The unused bits (Least Significant Portion) of the TX register are don't care bits. If the TEIE bit has been enabled, the DSP is interrupted when the TX register becomes empty.

8.3.9 Time Slot Register (TSR)

The Time Slot Register (TSR) is effectively a null data register that is used when the data is not to be transmitted in the available transmit time slot. For the purposes of timing, the TSR is a write-only register that behaves like an alternative transmit data register, except that, rather than transmitting data, the transmit data pin is in the high-impedance state for that time slot.

8.3.10 Port Control Register (PCR)

The Port Control Register (PCR) is a 16-bit read / write register that controls the functionality of the SSI GPIO pins. The PCRC is associated with SSI0. The PCRD is associated with SSI1. **Figure 8-6** shows the programming model for the PCR. Hardware and software reset clear all PCR bits.

PCRC—X:$FFBF
PCRD—X:$FFAF
SSI Port Control Register
Reset = $0000
Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	PEN	*	PC5	PC4	PC3	PC2	PC1	PC0

* Indicates reserved bits, read as 0 and should be written with 0 for future compatibility

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Figure 8-6 SSI Port Control Register Programming Model

8.3.10.1 Port Control (PC[5:0])—Bits 0–5

The Port Control (PC[5:0]) bits control the functionality of a corresponding port pin. When a PC bit is set, the corresponding port pin is configured as a SSI pin. When a PC bit is cleared, the corresponding port pin is configured as GPIO pin.

8.3.10.2 Port Enable (PEN)—Bit 7

When the Port Enable (PEN) control bit is set, all SSI pins are activated as defined by all other settings. When the PEN bit is cleared, all SSI pins are tri-stated, ignoring all other settings.

8.3.10.3 Reserved Bits—Bits 6, 8–15

Bit 6 and bits 8–15 are reserved. They are read as 0 and should be written as 0 to ensure future compatibility.

8.3.11 Port Direction Register (PRR)

The Port Direction Register (PRR) is a 16-bit read / write register that controls the direction of SSI GPIO pins. The PRRC is associated with SSI0. The PRRD is associated with SSI1. When a port pin is configured as GPIO, the PDC bit controls the port pin direction. When the PDC bit is set, the GPIO port pin is configured as output. When the PDC bit is cleared the GPIO port pin is configured as input. Hardware and software reset clear all PRR bits.

PRRC—X:$FFBE
PRRD—X:$FFAE
SSI GPIO Direction Control Register
Reset = $0000
Read/Write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0

* Indicates reserved bits, read as 0 and should be written with 0 for future compatibility

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Figure 8-7 SSI GPIO Direction Control Register Programming Model

Table 8-5 describes the port pin configurations.

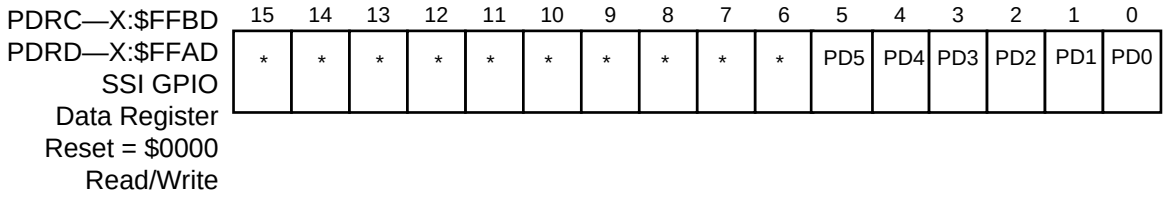
Table 8-5 PCR and PRR Register Bits Functionality

PC	PDC	Port Pin Function
1	0 or 1	SSI
0	0	GPIO input
0	1	GPIO output

Note: When the PEN bit in the PCR is cleared, the port is disabled and all the pins are at high impedance regardless of the values of the PC and PDC bits.

8.3.12 Port Data Register (PDR)

The read / write 16-bit Port Data Register (PDR) is used to read or write data to or from the SSI GPIO pins. The PDRC is associated with SSI0, and the PDRD is associated with SSI1. Bits PD[5:0] are used to read or write data to or from the corresponding port pins if they are configured as GPIO (by PC[5:0] bits in the PCR). If a port pin is configured as a GPIO input, then the corresponding PD bit reflects the value present on this pin. If a port pin is configured as a GPIO output, then the value written into the corresponding PD bit is reflected on the this pin. Hardware and software reset clear all PDR bits.



* Indicates reserved bits, read as 0 and should be written with 0 for future compatibility

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Figure 8-8 SSI GPIO Data Register Programming Model

8.4 OPERATING MODES

SSI operating modes are selected by the SSI Control Registers CRA, CRB, and CRC. The main operating modes are described in the following paragraphs.

Hardware or software reset clears the Port Control Register (PCR) and the Port Direction Control Register (PRR), which configure all SSI pins to be at high impedance. The SSI is reset while all SSI pins are programmed as GPIO and is active only when at least one of the SSI I / O pins is programmed as an SSI pin.

The correct way to initialize the SSI is as follows:

1. Hardware, software, SSI individual, or STOP reset
2. Program SSI control according to the desired functionality

During program execution, the PC[5:0] bits in the PCR can be cleared, causing the SSI to stop serial activity and enter the individual reset state. All status bits of the interface are then set to their reset state. However, the contents of CRA, CRB, and CRC are not affected. This procedure allows the DSP program to reset each interface separately from the other internal peripherals. During individual reset, internal accesses to the data

registers of the SSI are not valid and any data read will not be valid. To ensure proper operation of the interface, the DSP program must reset the SSI before changing any of its control registers except for the CRB.

8.4.1 SSI Exceptions

The SSI generates the following exceptions**,** ordered from highest to lowest priority:

1. SSI Receive Data with Exception Status—This exception occurs when the receive exception interrupt is enabled, the receive data register is full, and a receiver overrun error has occurred. ROE is cleared by first reading the SSISR and then reading RX.
2. SSI Receive Data—This exception occurs when the receive interrupt is enabled, the receive data register is full, and no receive error conditions exist. Reading RX clears the pending interrupt. This error-free interrupt can use a fast interrupt service routine for minimum overhead.
3. SSI Receive Last Slot Interrupt—This exception occurs after the last slot of the frame ended (in Network mode only). Using the Receive Last Slot interrupt guarantees that the previous frame was serviced with the previous setting and the new frame is to be serviced with the new setting without synchronization problems. The maximum Receive Last Slot interrupt service time should not exceed N – 1 SSI bits service time, where N is the number of bits in a slot.
4. SSI Transmit Data with Exception Status—This exception occurs when the transmit exception interrupt is enabled, the transmit data register is empty, and a transmitter underrun error has occurred. TUE is cleared by first reading the SSISR and then writing to the transmit data register, or to the TSR to clear the pending interrupt.
5. SSI Transmit Last Slot Interrupt—This exception occurs at the start of the last slot of the frame in Network mode. Using the Transmit Last Slot interrupt guarantees that the previous frame was serviced with the previous setting and the new frame is to be serviced with the new setting without synchronization problems. Note that the maximum Transmit last slot interrupt service time should not exceed N – 1 SSI bits service time, where N is the number of bits in a slot.
6. SSI Transmit Data—This exception occurs when the transmit interrupt is enabled, and the transmit data register is empty, and no transmitter error conditions exist. Writing to the TX registers or to the TSR clears this interrupt. This error-free interrupt can use a fast interrupt service routine for minimum overhead.

8.4.2 Operating Modes–Normal, Network, and On-Demand

The SSI has three basic operating modes and many data/operation formats selectable by programming control bits in the CRA and CRC. These control bits are DC[4:0], WL1, WL0, MOD, SYN, FSL1, FSL0, FSR, FSP, CKP, and SHFD.

8.4.2.1 Operating Mode Selection

Selecting between the Normal mode and Network mode is accomplished by clearing or setting the MOD bit in the CRC. In Normal mode, the SSI functions with one data word of I/O per frame. In Network mode, two to 32 time slots per frame can be selected. During each frame, 0 to 32 data words of I/O can be received or transmitted. In either case, the transfers are periodic. Normal mode is typically used to transfer data to or from a single device. Network mode is typically used in Time Division Multiplexed (TDM) networks of codecs or DSPs with multiple words per frame.

Setting the MOD bit in the CRC, as for Network mode, and setting the frame rate divider to 0 (DC[4:0] = 00000) selects the On-Demand mode. This special case does not generate a periodic frame sync. Instead, a frame sync pulse is generated only when data is available to transmit. The frame sync signal indicates the first time slot in the frame. The On-Demand mode requires that the transmit frame sync be internal (output) and the receive frame sync be external (input). Therefore, for simplex operation, the Synchronous mode could be used; however, for full-duplex operation, the Asynchronous mode must be used. Data transmission that is data driven is enabled by writing data into the TX register. Although the SSI is double-buffered, only one word can be written to the TX register, even if the transmit shift register is empty. The receive and transmit interrupts function as usual using the TDE and RDF flag bits. However, transmit underruns are impossible for on-demand transmission and are disabled. This mode is useful for interfacing to codecs that require a continuous clock.

8.4.2.2 Synchronous/Asynchronous Operating Modes

The transmit and receive sections of this interface can be synchronous or asynchronous—the transmitter and receiver can use common clock and synchronization signals (Synchronous mode) or they can have their own separate clock and sync signals (Asynchronous mode). The SYN bit in the CRC selects synchronous or asynchronous operation. Since the SSI is designed to operate either synchronously or asynchronously, separate receive and transmit interrupts are provided.

When the SYN bit is cleared, the Asynchronous mode is selected and the SSI TX and RX clocks and frame sync sources are independent. When the SYN bit is set, the SSI TX and RX clocks and frame sync come from the same source (either external or internal).

Data clock and frame sync signals can be generated internally by the DSP or can be obtained from external sources. If internally generated, the SSI clock generator is used to

derive bit clock and frame sync signals from the DSP internal system clock. The SSI clock generator consists of a selectable fixed prescaler and a programmable prescaler for bit rate clock generation and also a programmable frame-rate divider and a word-length divider for frame-rate sync-signal generation.

8.4.2.3 Frame Sync Selection

The transmitter and receiver can operate independently of each other. The transmitter can have either a bit-long or word-long frame-sync signal format, and the receiver can have the same or opposite format. The selection is made by programming the FSL0 and FSL1 bits in the CRC.

1. If the FSL1 bit is cleared, the RX frame sync is asserted during the entire data transfer period. This frame sync length is compatible with Motorola codecs, SPI serial peripherals, serial A/D and D/A converters, shift registers, and telecommunication PCM serial I/O.
2. If FSL1 is set, the RX frame sync pulse is active for one bit clock immediately before the data transfer period. This frame sync length is compatible with Intel and National components, codecs, and telecommunication PCM serial I/O.

The ability to mix frame sync lengths is useful in configuring systems in which data is received from one type device (e.g., codec) and transmitted to a different type device.

The FSL0 bit controls whether RX and TX have the same frame sync length. If FSL0 equals 0, RX and TX have the same frame sync length, which is selected by FSL1. If FSL0 equals 1, RX and TX have different frame sync lengths, which are selected by FSL1. FSL0 is ignored when the SYN bit is set.

The FSR bit controls the relative timing of the word length frame sync as referred to the data word. When the FSR bit is cleared, the word length frame sync is generated (or expected) with the first bit of the data word. When the FSR bit is set, the word length frame sync is generated (or expected) with the last bit of the previous word. The FSR bit is ignored when a bit length frame sync is selected.

The FSP bit controls the polarity of the frame sync. When FSP is cleared the polarity of the frame sync is positive (i.e., the frame sync signal is asserted high). When FSP is set the polarity of the frame sync is negative (i.e., the frame sync is asserted low.)

The SSI receiver looks for a receive frame sync leading edge (or trailing edge, if FSP is set) only when the previous frame is completed. If the frame sync goes high before the frame is completed (or before the last bit of the frame is received in the case of a bit frame sync or a word length frame sync with FSR set), the current frame sync is not recognized, and the receiver is internally disabled until the next frame sync. Frames do not have to be adjacent—that is, a new frame sync does not have to immediately follow the previous

frame. Gaps of arbitrary periods can occur between frames. The transmitter is tri-stated during these gaps.

8.4.2.4 Shift Direction Selection

Some data formats, such as those used by codecs, specify MSB first. Other data formats, such as the AES-EBU digital audio, specify LSB first. To interface with devices from both systems, the shift registers in the SSI are bidirectional. The MSB/LSB selection is made by programming the SHFD bit in the CRC. When the SHFD bit is cleared, data is shifted into the Receive Shift Register and shifted out of the Transmit Shift Register MSB first. If the SHFD bit is set, data is shifted into the Receive Shift Register and shifted out of the Transmit Shift Register LSB first.

8.4.3 Serial I/O Flags

Two SSI pins (SC1 and SC0) are available as serial I/O flags. Their operation is controlled by the SYN, SCD0, and SCD1 bits in the CRC. The control bits (OF1 and OF0) and status bits (IF1 and IF0) are double-buffered to and from the SC1 and SC0 pins. Double-buffering the flags keeps them synchronized with TX and RX registers.

The flags are only available in the Synchronous mode (when the SYN bit is set). Each flag can be separately programmed. When flag 0 is enabled, its direction is selected by SCD0, SCD0 = 1 as output and SCD0 = 0 as input. In the same way when flag1 is enabled, its direction is selected by SCD1, SCD1 = 1 as output and SCD1 = 0 as input.

When programmed as input, the SC0 and SC1 pins are latched at the same time the first bit of the receive data word is sampled. Since the input is latched, the signal on the input flag pins SC0 and SC1 can change without affecting the input flag until the first bit of the next received data word. When the received data word is latched by the RX register, the latched values are then latched by the IF0 and IF1 bits (in the SSISR) and can be read by software.

When programmed as output, the SC0 and SC1 pins are driven by the value from the OF0 and OF1 bits (in the CRB) and latched when the contents of the TX register is transferred to the transmit shift register. The values on the SC0 and SC1 pins are stable from the same time the first bit of the transmit data word is transmitted until the first bit of the next transmit data word is transmitted. Software can change the values of the OF0 and OF1 bits (in the CRB), thus controlling the SC0 and SC1 pin values for each transmitted word.