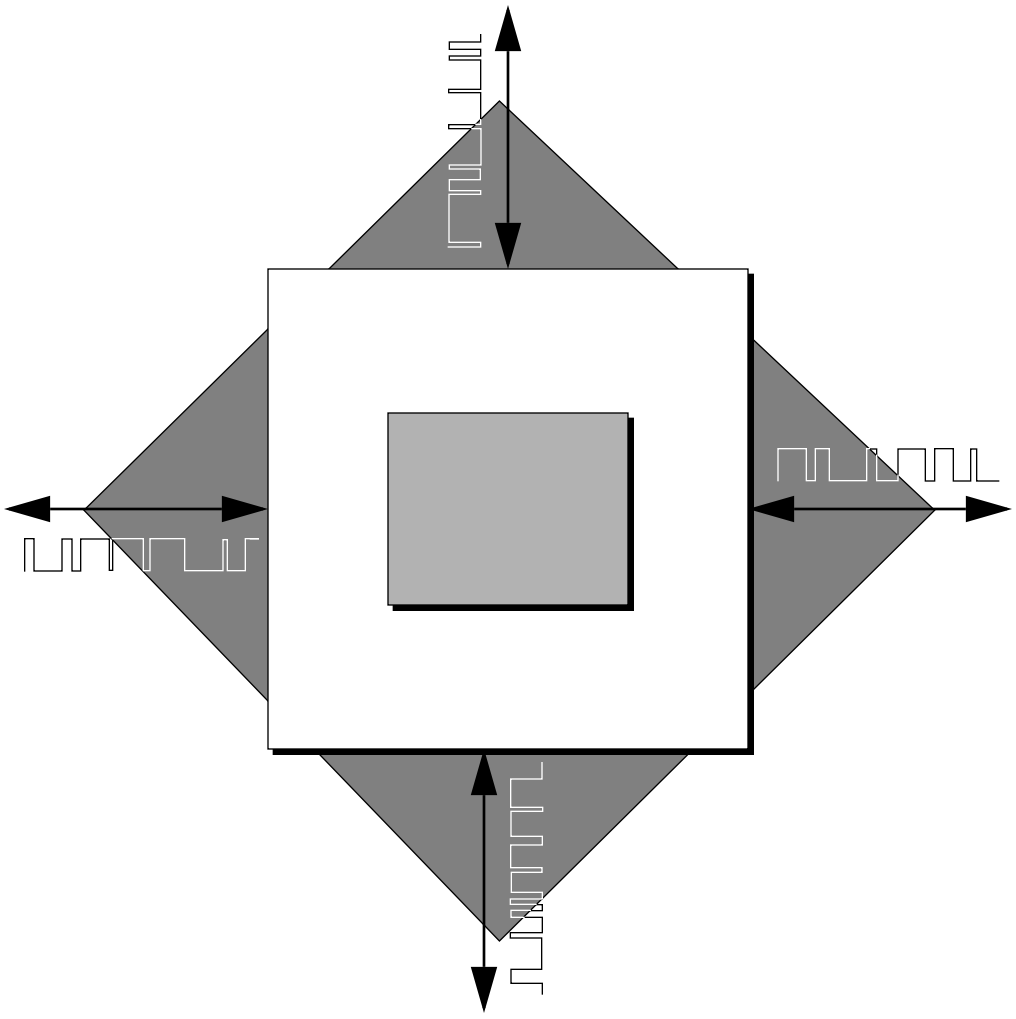
SECTION 4

DSP56166 I/O INTERFACE



SECTION CONTENTS

4.1 INTRODUCTION

The DSP56166 provides 16 pins for an external address bus, 16 pins for an external data bus, and 10 pins for bus control. These pins are grouped to form the Port A bus interface. The DSP56166 also provides 25 programmable I/O pins. These pins may be used as general purpose I/O pins or allocated to on-chip peripherals. Four digital on-chip peripherals are provided on the DSP56166: an 8 bit parallel Host MPU/DMA Interface, a 16-bit timer, and two Reduced Synchronous Serial Interfaces (RSSI0 and RSSI1). These 25 pins are separate from the DSP56166 address and data buses and are grouped as two I/O ports (B and C). Figure 4-1 shows the I/O block diagram.

Port B is a 15-bit I/O interface which may be used either as general purpose I/O pins or as Host MPU/DMA Interface pins. The Host MPU/DMA Interface provides a dedicated 8-bit parallel port to a host microprocessor or DMA controller and can provide debugging facilities via host exceptions.

Port C is a 10-bit I/O interface which may be used as general purpose I/O pins or as Timer and Serial Interface pins. The 16-bit timer can generate periodic interrupts based on a multiple of the internal or external clock. The two Reduced Synchronous Serial Interfaces, RSSI0 and RSSI1, are identical. They provide high speed synchronous serial data communication capability between the DSP56166 and other serial devices. Support for TDM network configurations allows communication among up to eight devices.

These I/O interfaces are intended to minimize system chip count and “glue” logic in many DSP applications. Each I/O interface has its own control, status, and data registers and is treated as memory-mapped I/O by the DSP56166 (see Figure 4-2 and Figure 4-3). Each interface has several dedicated interrupt vector addresses and control bits to enable/disable interrupts. This minimizes the overhead associated with servicing the device since each interrupt source may have its own service routine.

4.2 I/O PORT SET-UP AND PROGRAMMING

Port A Bus Control Registers BCR and BCR2, located respectively at X:$FFDE and X:$FFDA, may be programmed to insert wait states in a bus cycle during external data and program memory accesses for BCR and during external peripheral accesses for BCR2. Five bits are available in each control register for each type of external memory access. Each 5 bit field can specify up to 31 wait states. On processor reset, these five bits for both P and X memories are preset to all ones so that 31 wait states are inserted allowing slow, inexpensive memory to be used immediately after reset. All other Port Control Register bits are cleared on processor reset; i.e., reset sets the BCR to $03FF and BCR2 to $001F.

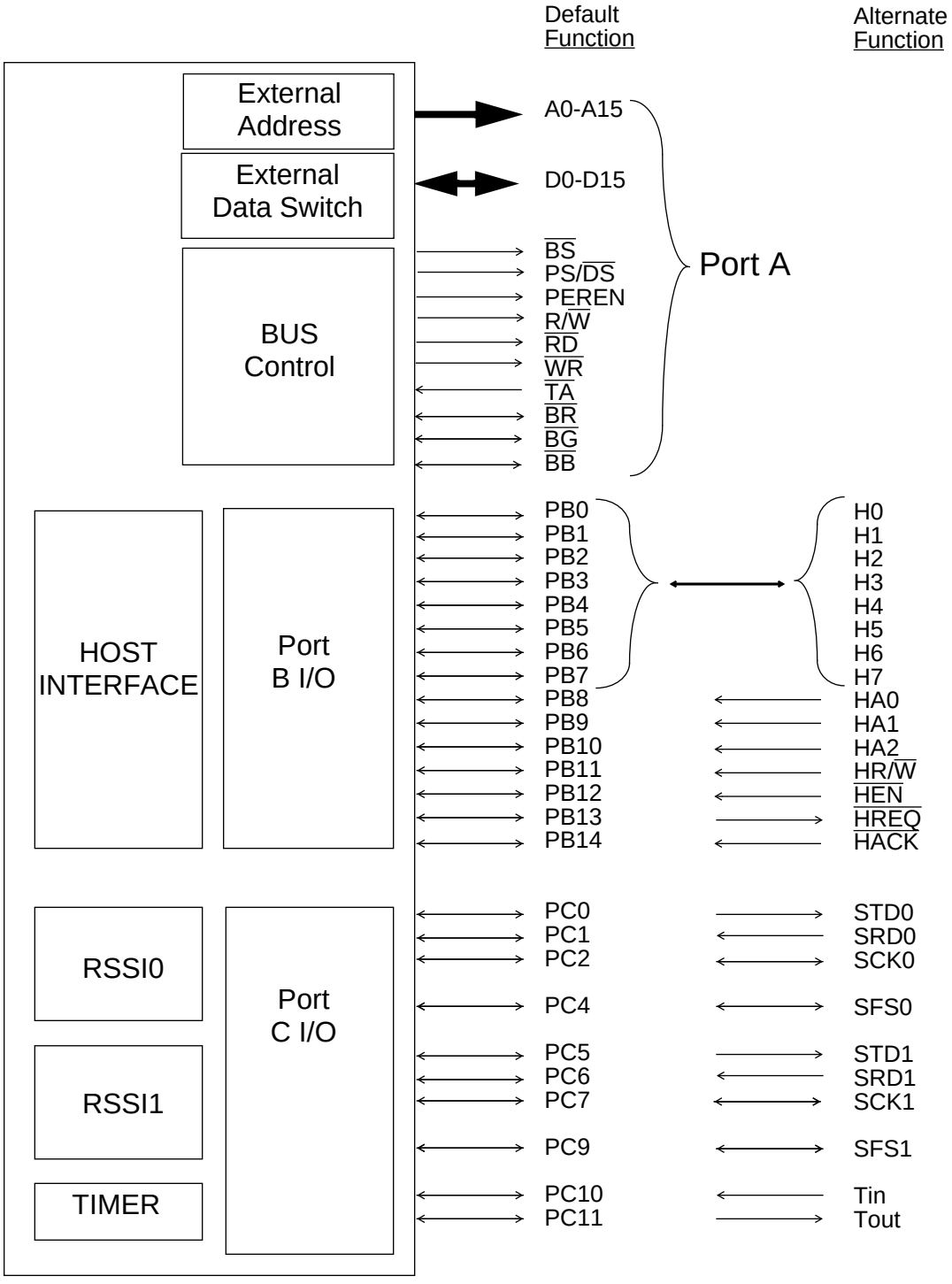


Figure 4-1 DSP56166 Input/Output Block Diagram

$FFFF	Reserved for on-chip emulation	$FFDF	IPR: Interrupt Priority Register
$FFFE		$FFDE	BCR: Bus Control Register
$FFFD		$FFDD	IPR2: Interrupt Priority Register 2
$FFFC		$FFDC	PCR1
$FFFB		$FFDB	PCR0
$FFFA		$FFDA	BCR2: Bus Control Register 2
$FFF9	TX/RX RSSI1 TX/RX Registers	$FFD9	CRB-RSSI1 Control Register B
$FFF8	SR/TSR RSSI1 Status Register	$FFD8	CRA-RSSI1 Control Register A
$FFF7		$FFD7	
$FFF6		$FFD6	
$FFF5		$FFD5	
$FFF4		$FFD4	
$FFF3		$FFD3	
$FFF2		$FFD2	
$FFF1	TX/RX RSSI0 TX/RX Registers	$FFD1	CRB-RSSI0 Control Register B
$FFF0	SR/TSR RSSI0 Status Register	$FFD0	CRA-RSSI0 Control Register A
$FFEF	Timer Preload Register(TPR)	$FFCF	
$FFEE	Timer Compare Register(TCPR)	$FFCE	
$FFED	Timer Count Register(TCTR)	$FFCD	
$FFEC	Timer Control Register(TCR)	$FFCC	
$FFEB		$FFCB	
$FFEA		$FFCA	
$FFE9	CRX/CTX	$FFC9	reserved
$FFE8	COSR	$FFC8	CCR1
$FFE7		$FFC7	CCR0
$FFE6		$FFC6	
$FFE5	HTX/HRX: Host TX/RX Register	$FFC5	
$FFE4	HSR: Host Status Register	$FFC4	HCR: Host Control Register
$FFE3	Port C Data Register (PCD)	$FFC3	Port C Data Direction Register
$FFE2	Port B Data Register (PBD)	$FFC2	Port B Data Direction Register
$FFE1		$FFC1	Port C Control Register (PCC)
$FFE0		$FFC0	Port B Control Register (PBC)

Figure 4-2 DSP56166 I/O and On-Chip Peripheral Memory Map

Ports B and C pins may be programmed under software control as general purpose I/O pins or as dedicated on-chip peripheral pins. A Port Control Register is associated with each port which allows the port pins to be selected for one of these two functions. All port B pins are collectively configured as general purpose I/O pins if the corresponding Port Control Register bit is cleared and all are configured as HI pins if the corresponding Port Control Register bit is set. In contrast, each Port C pin is independently configured as a general purpose I/O pin if the corresponding Port Control Register bit is cleared and is configured as an RSSI pin or Timer pin if the corresponding Port Control Register bit is set. If a port pin is selected as a general purpose I/O pin, the direction of that pin is determined by a corresponding control bit in the Port Data Direction Register. The port pin is configured as an input if the corresponding Data Direction Register bit is cleared and is configured as an output if the corresponding Data Direction Register bit is set. All Port Control Register bits and Data Direction Register bits are cleared on processor reset, configuring all port pins as general purpose input pins. If the port pin is selected as an on-chip peripheral pin, the corresponding data direction bit is ignored and the direction of that pin is determined by the operating mode of the on-chip peripheral.

A port pin configured as a general purpose I/O pin is accessed through an associated Port Data Register B or C. Data written to the Port Data Register is stored in an output latch. If the port pin is configured as an output, the output latch data is driven out on the port pin. When the Port Data Register is read, the logic value on the output port pin is read. If the port pin is configured as an input, data written to the Port Data Register is still stored in the output latch but is not gated to the port pin. When the Port Data Register is read, the state of the port pin is read. That is, reading the port data register will reflect the state of the pins regardless of how they were configured.

When a port pin is configured as a dedicated on-chip peripheral pin, the port data register will read the state of the input pin or output driver.

4.2.1 Port Registers

Ports A, B and C are controlled by programmable registers. Port A is controlled by the Bus Control Registers which control memory wait states. Ports B and C each have registers that select the peripheral to be available and control that peripheral. See Figure 4-3.

4.2.1.1 Bus Control Registers (BCR and BCR2)

Port A Bus Control Registers (BCR and BCR2) are 16-bit read/write registers. They can be programmed to insert wait states in a bus cycle during external memory accesses and external peripheral accesses.

In the BCR, 5 bit wait control fields specify between 0 and 31 wait states for an external X memory and P memory access.Wait state fields are set to $1F during hardware reset.

Bit 15 of the BCR, the Bus Request Hold bit, (RH), can be used for direct software control of the $\overline{BR}$ pin. When this bit is set, the $\overline{BR}$ pin is asserted even though the DSP does not need the bus. If RH is cleared, the $\overline{BR}$ pin will only be asserted if an external access is being attempted or pending. RH is cleared by hardware reset.

Bit 14 of the BCR, the Bus State status bit (BS), is set if the DSP is currently the bus master. If the DSP is not the bus master, BS is cleared. In the slave mode, the BS bit is set when the $\overline{BG}$ output pin is high and cleared when $\overline{BG}$ is low. In the master mode, BS is cleared when the $\overline{BG}$ input pin is high and set when both pins ($\overline{BG}$ and BB) are low. This bit is set by hardware reset.

128 locations of the external data space (X:$FF00-FF7F) are reserved for off-chip peripheral accesses. The external bus access time on this external peripheral space is controlled by 5 bits of BCR2 located at X:$FFDA. Between 0 and 31 software programmable wait states can be generated. A special pin, $\overline{PEREN}$, is asserted low during accesses to the memory mapped external peripheral registers. Wait state fields are set to $1F during hardware reset.

4.2.1.2 Port B and Port C Registers

Port B consists of three read/write registers — a 1-bit Port B Control Register (PBC), a 15-bit Port B Data Direction Register (PBDDR), and a 15-bit Port B Data Register (PBD).

Port C consists of three read/write registers — a 12-bit Port C Control Register (PCC), a 12-bit Port C Data Direction Register (PCDDR), and a 12 bit Port C Data Register (PCD). Only ten bits in these three registers have pins and are available for GPIO. Bits 3 and 8 are not connected to pins. These registers are shown in Figure 4-3. All registers are read/write. Bit manipulation instructions can be used to access individual bits.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RH	BS	**	**	**	**	External X Memory					External P Memory				

PORT A BUS CONTROL REGISTER (BCR) X:$FFDE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
**	**	**	**	**	**	**	**	**	**	**	External Peripherals				

PORT A BUS CONTROL REGISTER (BCR2) X:$FFDA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
**	**	**	**	**	**	**	**	**	**	**	**	**	**	**	BC 0

PORT B CONTROL REGISTER (PBC) X:$FFC0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
**	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0

PORT B DATA DIRECTION REGISTER (PBDDR) X:$FFC2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
**	PB 14	PB 13	PB 12	PB 11	PB 10	PB 9	PB 8	PB 7	PB 6	PB 5	PB 4	PB 3	PB 2	PB 1	PB 0

PORT B DATA REGISTER (PBD) X:$FFE2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
**	**	**	**	CC 11	CC 10	CC 9	**	CC 7	CC 6	CC 5	CC 4	**	CC 2	CC 1	CC 0

PORT C CONTROL REGISTER (PCC) X:$FFC1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
**	**	**	**	DC 11	DC 10	DC 9	**	DC 7	DC 6	DC 5	DC 4	**	DC 2	DC 1	DC 0

PORT C DATA DIRECTION REGISTER (PCDDR) X:$FFC3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
**	**	**	**	PC 11	PC 10	PC 9	**	PC 7	PC 6	PC 5	PC 4	**	PC 2	PC 1	PC 0

PORT C DATA REGISTER (PCD) X:$FFE3

**: reserved

Figure 4-3 DSP56166 I/O Port B and C Programming Models