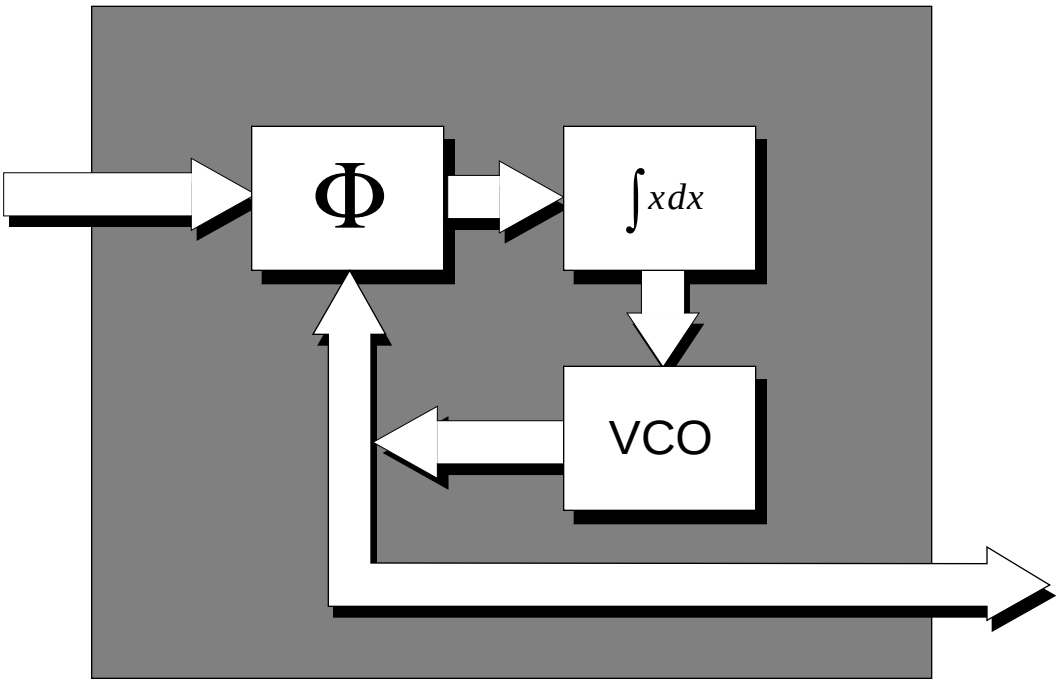
## SECTION 9

# DSP56166 ON-CHIP PLL



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## 9.1 INTRODUCTION

The DSP56166 does not contain an on-chip oscillator. An external system clock must be provided through the EXTAL input pin. The on-chip phase locked loop (PLL) can be used to generate the DSP5616 core system clock or it can be bypassed allowing the DSP5616 core to directly use the clock provided on the EXTAL pin.

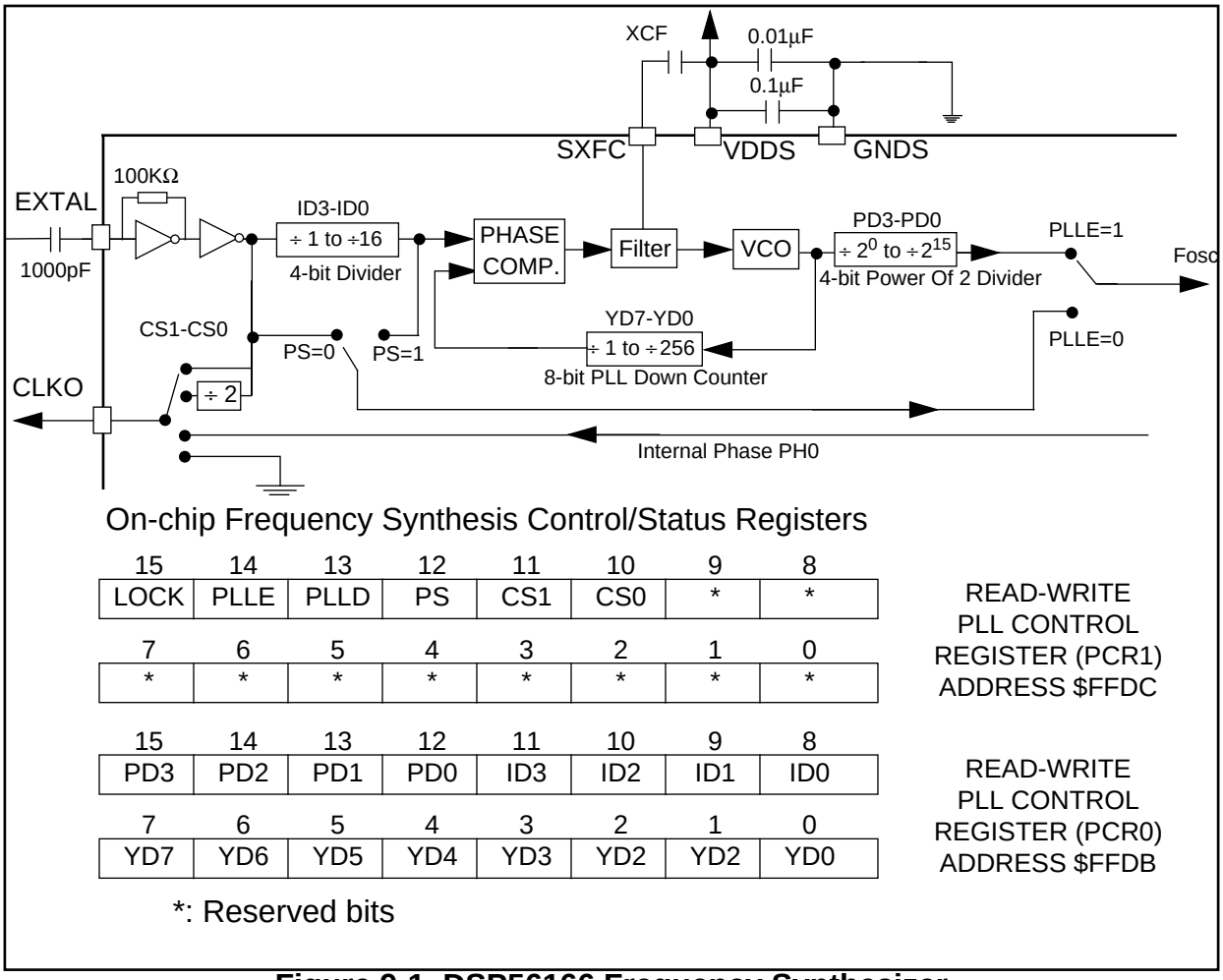
Figure 9-1 shows the general block diagram of the on-chip frequency synthesizer.

The 4-bit divider ID3-ID0 defines the resolution of the PLL and divides the incoming clock rate fed to the PLL. The eight down counter bits YD7-YD0 control down counting in the PLL feedback loop causing it to divide by the value YD+1 (any number between 1 and 256) which effectively multiplies the frequency out of the PLL. The VCO output can be divided down by any power of 2 between $2^0$ and $2^{15}$ before entering the core using the 4-bits PD3-PD0 of the control register PCR1. The system frequency on the DSP core is controlled by the frequency control bits of the PLL control register PCR0 as follows:

$$Fosc = \{Fext \div [ID+1]\} x [YD+1] \div (2^{PD})$$

where ID is the value contained in ID3-ID0, YD is the value contained in YD7-YD0, and PD is the value contained in PD3-PD0. Fext is a squared and delayed version of the clock signal applied to the EXTAL input pin.

**Note:** The STOP instruction does not power down the PLL if the PLL is enabled (PLLD=0) when entering the STOP mode. STOP will power down the ID register if the PLL is disabled (PLLD=1) when entering the STOP mode. (see Section 9.3.4).




On-chip Frequency Synthesis Control/Status Registers

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| LOCK | PLLE | PLLD | PS | CS1 | CS0 | * | * |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| * | * | * | * | * | * | * | * |

READ-WRITE PLL CONTROL REGISTER (PCR1) ADDRESS $FFDC

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| PD3 | PD2 | PD1 | PD0 | ID3 | ID2 | ID1 | ID0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| YD7 | YD6 | YD5 | YD4 | YD3 | YD2 | YD2 | YD0 |

READ-WRITE PLL CONTROL REGISTER (PCR0) ADDRESS $FFDB

*: Reserved bits

**Figure 9-1 DSP56166 Frequency Synthesizer Block Diagram and Control Registers**

## 9.2 ON-CHIP CLOCK SYNTHESIS CONTROL REGISTER PCR0

The Clock Synthesis Control Register PCR0 is a 16-bit read/write register used to direct the operation of the on-chip clock synthesis. The PCR0 controls the frequency programming of the PLL. The PCR0 control bits are described in the following sections.

All PCR0 bits of are cleared by DSP hardware. Software reset does not affect this register.

### 9.2.1 PCR0 Feedback Divider Bits (YD7-YD0) Bits 0-7

The eight feedback divider bits YD7-YD0 control the down counter in the feedback loop, causing it to divide by the value YD+1 where YD is the value contained in the eight bits. Changing these bits requires a time delay for the Voltage Controlled Oscillator (VCO) to lock again.

The LOCK bit is cleared any time a new value is written to the YD bits.

The resulting DSP core system clock must be within the limits specified by the DSP56166 Technical Data Sheet (order number DSP56166/D). The frequency of the VCO should also remain higher than the minimum value specified in this data sheet.

### 9.2.2 PCR0 Input Divider Bits (ID3-ID0) Bits 8-11

The four input divider bits are used to divide the input clock frequency by any number between 1 and 16. The output of the divider is used as input for the phase comparator of the PLL. If ID is the value contained in the four bits, the input clock to the PLL is divided by ID+1.

Any time a new value is written to the ID bits, the LOCK bit is cleared.

### 9.2.3 PCR0 Power Divider Bits (PD3-PD0) Bits 12-15

The four power divider bits are used to divide the VCO output clock frequency by any power of two between $2^0$ and $2^{15}$ (i.e., 1, 2, 4, 8, 16, 32, …, 16384, or 32768). The output of the divider can be used as the operating clock for the DSP core, as shown in Figure 9-1. Writing to the PD bits does not affect the LOCK condition of the PLL.

The PD bits can be used to switch the DSP core back and forth from a high MIPS rate to a very low speed, low power mode without having to wait and check for the PLL to lock on a new frequency.

## 9.3 ON-CHIP CLOCK SYNTHESIS CONTROL REGISTER PCR1

The Clock Synthesis Control Register PCR1 is a 16-bit read/write register used to direct the operation of the on-chip clock synthesizer. The PCR1 control bits are described in the following sections.

All PCR1 bits are cleared by DSP hardware. Software reset does not affect this register.

### 9.3.1 PCR1 Reserved Bits — Bits 0-9

These bits are reserved and should be written as zero by the user.

### 9.3.2 PCR1 CLKO Select Bits (CS1-CS0) Bits 10 and 11

The two CLKO Select bits CS1-CS0 enable one of three possible clocks to be output to the CLKO pin when the CD bit in the OMR register is cleared (see Figure 9-1). After hardware reset, the internal DSP core clock PH0 (phase zero) is output to the CLKO pin. PH0 is a delayed version of the DSP core master clock, Fosc. Changing the value of the two bits CS1-CS0 according to Table 9-1, Fext or Fext/2 can be selected to be output on CLKO. Fext is a squared and delayed version of the signal applied to the EXTAL input pin.

**Table 9-1 CLKOUT Pin Control**

| CS1 | CS0 | CLKO |
|---|---|---|
| 0 | 0 | PH0 |
| 0 | 1 | Reserved |
| 1 | 0 | Fext |
| 1 | 1 | Fext/2 |

### 9.3.3 PCR1 Phase Select Bit (PS) Bit 12

This bit is used to select the DSP core clock when the PLL output is not selected (PLLE=0). When this bit is cleared, a squared version of EXTAL is selected as Fosc. When this bit is set, the output of the ID divider is selected as Fosc.

### 9.3.4 PCR1 PLL Power Down Bit (PLLD) Bit 13

When the PLLD bit is set, the on-chip PLL is powered down. When this control bit is cleared, the on-chip PLL is turned on. This bit should not be set when the PLLE bit is set.

If the PLL has to be turned off before entering the STOP mode, the following sequence will have to be executed before the STOP instruction:

- Clear the PLLE bit (switch back to EXTAL)
- Set the PLLD bit (power down the PLL)
- Execute the STOP instruction.

Setting the PLLD bit clears the LOCK bit. Setting the PLLD bit powers down the complete PLL block including the PD and YD registers.

### 9.3.5 PCR1 PLL Enable Bit (PLLE) Bit 14

When the PLLE bit is set, the DSP5616 core system clock is generated by the on-chip PLL. Table 9-2 summarizes the function of the three bits — PLLE, PLLD and PS. The state of the PLL is defined by the PLLD bit. When the PLLD bit is set, the PLL is in the power down mode. When the PLLD bit is cleared, the PLL is in the active mode. Before turning the PLL off, the PLLE bit should be cleared in order to by-pass the PLL. The PLL can then be put in power down mode by setting PLLD.

If the output frequency of the PLL has to be changed by re-programming the YD bits while the PLL output is used by the core (PLLE=1; PLLD=0), the following sequence of operations should be performed:

- Clear the PLLE bit to switch back to EXTAL

- Program the YD bits (only after clearing PLLE)
- Wait for the LOCK bit to be set
- Set PLLE after the LOCK bit is tested high.

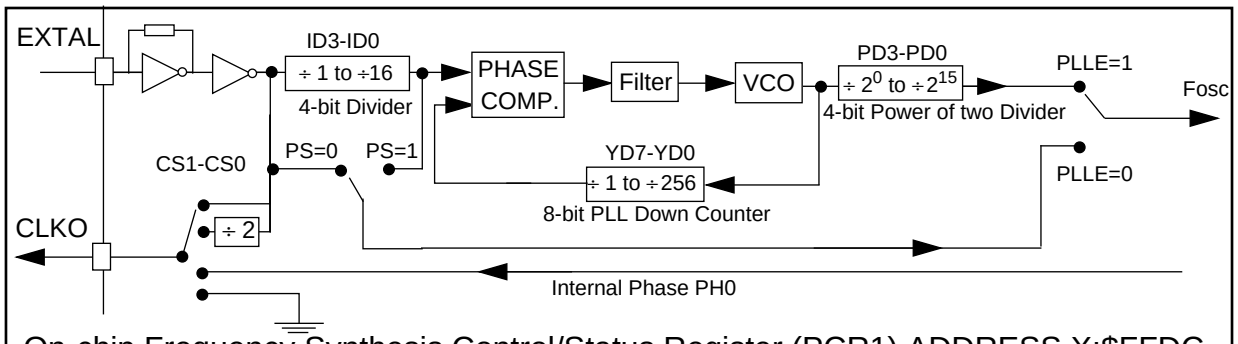
**Table 9-2 PLL Operations**

| PLLE | PLLD | PS | Fosc | PLL Mode |
|---|---|---|---|---|
| 0 | 0 | 0 | Fext | Active |
| 0 | 1 | 0 | Fext | Power Down |
| 0 | 0 | 1 | Fext÷[ID+1] | Active |
| 0 | 1 | 1 | Fext÷[ID+1] | Power Down |
| 1 | 0 | x | {Fext÷[ID+1]}x[YD+1]÷ ($2^{PD}$) | Active |
| 1 | 1 | x | Reserved | — |

### 9.3.6 PCR1 Voltage Controlled Oscillator Lock Bit (LOCK) Bit 15

This status bit shows whether the Voltage Controlled Oscillator (VCO) has locked on the desired frequency or not. When the LOCK bit is set, the VCO has locked; when the LOCK bit is cleared, the VCO has not locked yet. This bit is cleared when setting the PLLD bit and when changing the value of ID or YD bits. The LOCK bit is not cleared when clearing the PLLE bit without changing the values of PLLD, YD, or ID.

This bit is read-only and cannot be written by the DSP core.




On-chip Frequency Synthesis Control/Status Register (PCR1) ADDRESS X:$FFDC

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LOCK | PLLE | PLLD | PS | CS1 | CS0 | ** | ** | ** | ** | ** | ** | ** | ** | ** | ** |

| | | |
|---|---|---|
| LOCK | 0 | PLL unlocked |
| | 1 | PLL locked |
| PLLE PLLD | 00 | PLL active but not used as Fosc |
| | 01 | PLL powered down |
| | 10 | PLL active and used as Fosc |
| | 11 | Reserved |
| PHASE SELECT | 0 | Squared EXTAL selected as Fosc if PLLE=0 |
| | 1 | Squared EXTAL/ID selected as Fosc if PLLE=0 |
| CS1-CS0 CLKO Select | 00 | PH0 output to CLKO when enabled by the CD bit (bit 7) of the OMR |
| | 01 | reserved |
| | 10 | Fext output to CLKO when enabled by the CD bit (bit 7) of the OMR |
| | 11 | Fext/2 output to CLKO when enabled by the CD bit (bit 7) of the OMR |

On-chip Frequency Synthesis Control/Status Register (PCR0) ADDRESS X:$FFDB

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PD3 | PD2 | PD1 | PD0 | ID3 | ID2 | ID1 | ID0 | YD7 | YD6 | YD5 | YD0 | YD3 | YD2 | YD1 | YD0 |

| | | | | | |
|---|---|---|---|---|---|
| PD3-PD0 Clock Output Divider | $0 | Divide the VCO output clock by 1 ($2^0$) | 8 | Divide the VCO output clock by 256 ($2^8$) |
| | $1 | Divide the VCO output clock by 2 ($2^1$) | 9 | Divide the VCO output clock by 512 ($2^9$) |
| | $2 | Divide the VCO output clock by 4 ($2^2$) | A | Divide the VCO output clock by 1024 ($2^{10}$) |
| | $3 | Divide the VCO output clock by 8 ($2^3$) | B | Divide the VCO output clock by 2048 ($2^{11}$) |
| | $4 | Divide the VCO output clock by 16 ($2^4$) | C | Divide the VCO output clock by 4096 ($2^{12}$) |
| | $5 | Divide the VCO output clock by 32 ($2^5$) | D | Divide the VCO output clock by 8192 ($2^{13}$) |
| | $6 | Divide the VCO output clock by 64 ($2^6$) | E | Divide the VCO output clock by 16384 ($2^{14}$) |
| | $7 | Divide the VCO output clock by 128 ($2^7$) | F | Divide the VCO output clock by 32768 ($2^{15}$) |
| ID3-ID0 Input Clock Divider | $0 | Divide the input clock by 1 | 8 | Divide the input clock by 9 |
| | $1 | Divide the input clock by 2 | 9 | Divide the input clock by 10 |
| | $2 | Divide the input clock by 3 | A | Divide the input clock by 11 |
| | $3 | Divide the input clock by 4 | B | Divide the input clock by 12 |
| | $4 | Divide the input clock by 5 | C | Divide the input clock by 13 |
| | $5 | Divide the input clock by 6 | D | Divide the input clock by 14 |
| | $6 | Divide the input clock by 7 | E | Divide the input clock by 15 |
| | $7 | Divide the input clock by 8 | F | Divide the input clock by 16 |
| YD7-YD0 VCO Down Counter value | $YD | Multiplies by YD+1 | | |

**Figure 9-2 On-Chip Frequency Synthesizer Programming Model Summary.**