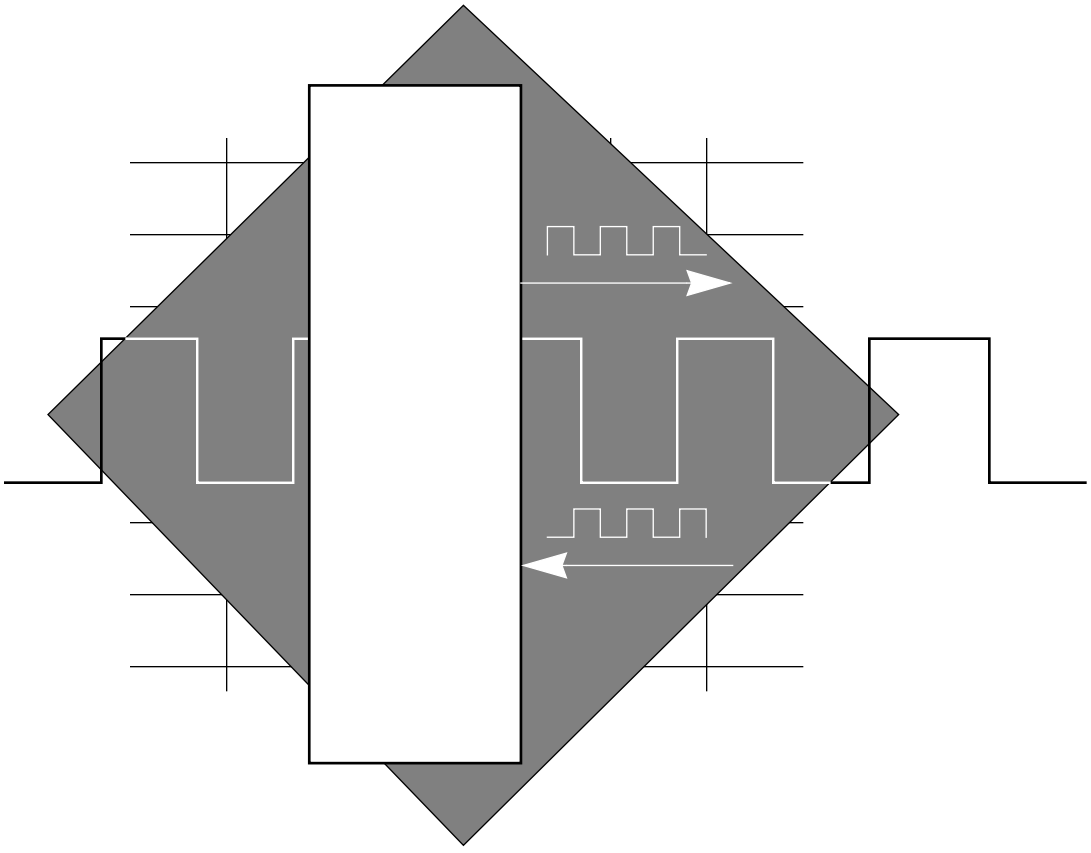
SECTION 8

REDUCED SSI (RSSI0 and RSSI1)



SECTION CONTENTS

8.1 INTRODUCTION

The Reduced Synchronous Serial Interface (RSSI) is a full duplex serial port which allows the DSP to communicate with a variety of serial devices including one or more industry standard codecs, other DSPs, microprocessors, and peripherals. The RSSI interface consists of independent transmitter and receiver sections with a common RSSI clock generator and frame synchronization.

8.2 RSSI OPERATING MODES

The RSSI has several basic operating modes. These modes can be programmed by several bits in the RSSI control registers.Table 8-1. lists these operating modes and some of the typical applications in which they may be used:

Table 8-1. RSSI Operating Modes

TX, RX Sections	Serial Clock	Protocol	Typical Applications
Synchronous	Continuous	Normal	Multiple Synchronous Codecs
Synchronous	Continuous	Network	TDM Codec or DSP Networks
Synchronous	Gated	Normal	SPI-Type Devices; DSP to MCU
Synchronous	Gated	Network	DSP to SPI peripherals

The transmit and receive sections of this interface are synchronous; that is, the transmitter and the receiver use a common clock and frame synchronization signal. Continuous or gated mode may be selected. For continuous mode, the clock is continuously running and for gated mode the clock is only functioning during transmission. Normal or network protocol may also be selected. For normal protocol, the RSSI functions with one data word of I/O per frame. For network protocol, any number from two to eight data words of I/O may be used per frame. These distinctions result in the basic operating modes which allow the RSSI to communicate with a wide variety of devices.

8.3 RSSI CLOCK AND FRAME SYNC GENERATION

Data clock and frame sync signals can be generated internally by the DSP or may be obtained from external sources. If internally generated, the RSSI clock generator is used to derive bit clock and frame sync signals from the DSP internal system clock. The RSSI clock generator consists of a selectable, fixed prescaler and a programmable prescaler for bit rate clock generation. For gated clock mode, the data clock will be valid only when data is to be transmitted, otherwise the clock pin will be three-stated. A programmable frame rate divider and a word length divider are used for frame rate sync signal generation. For gated mode, no frame sync signal is used.

8.4 RSSI DATA AND CONTROL PINS

The RSSI has four dedicated I/O pins:

- Transmit data STDx (PC0 for RSSI0 and PC5 for RSSI1)
- Receive data SRDx (PC1 for RSSI0 and PC6 for RSSI1)
- Serial clock SCKx (PC2 for RSSI0 and PC7 for RSSI1)
- Serial frame sync SFS (PC4 for RSSI0 and PC9 for RSSI1)

Figure 8-1 through Figure 8-4 show the main RSSI configurations and the following paragraphs describe the uses of these pins for each of the RSSI operating modes.

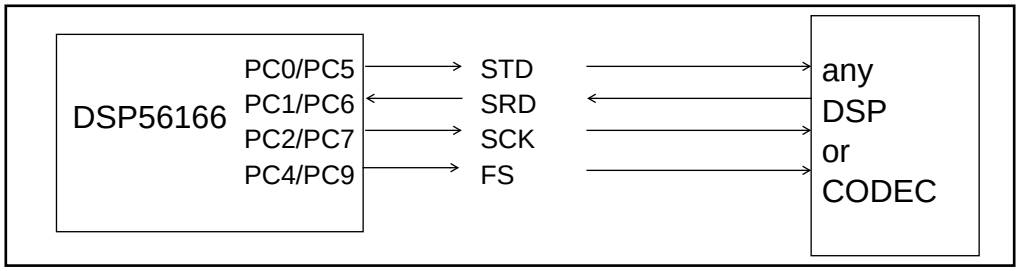


Figure 8-1 RSSI Internal Continuous Clock

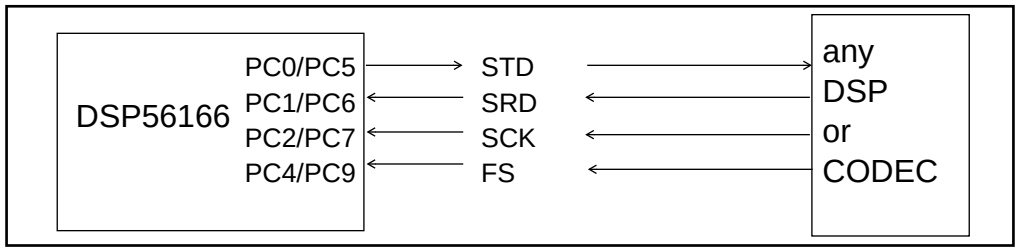


Figure 8-2 RSSI External Continuous Clock

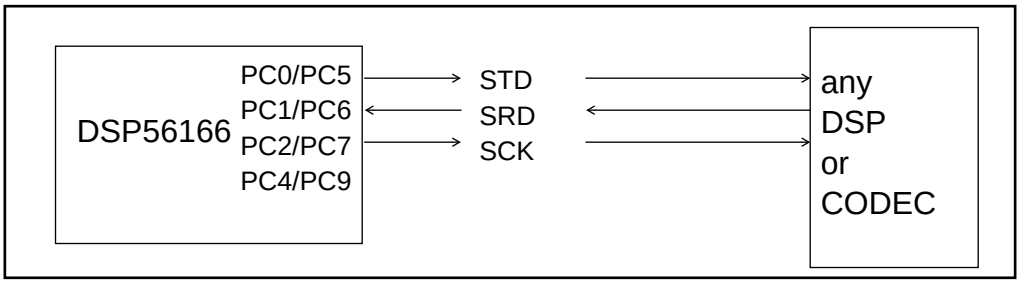


Figure 8-3 RSSI Internal Gated Clock

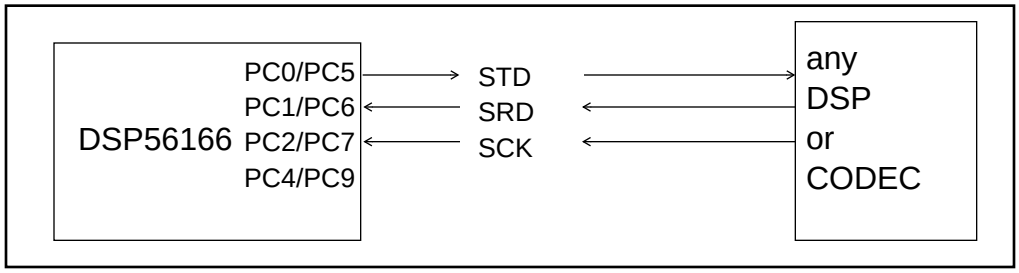


Figure 8-4 RSSI External Gated Clock

Figure 8-5 shows the internal clock path connections in block diagram form. The serial bit clock can be internal or external depending on the SCKD bit in the control register.

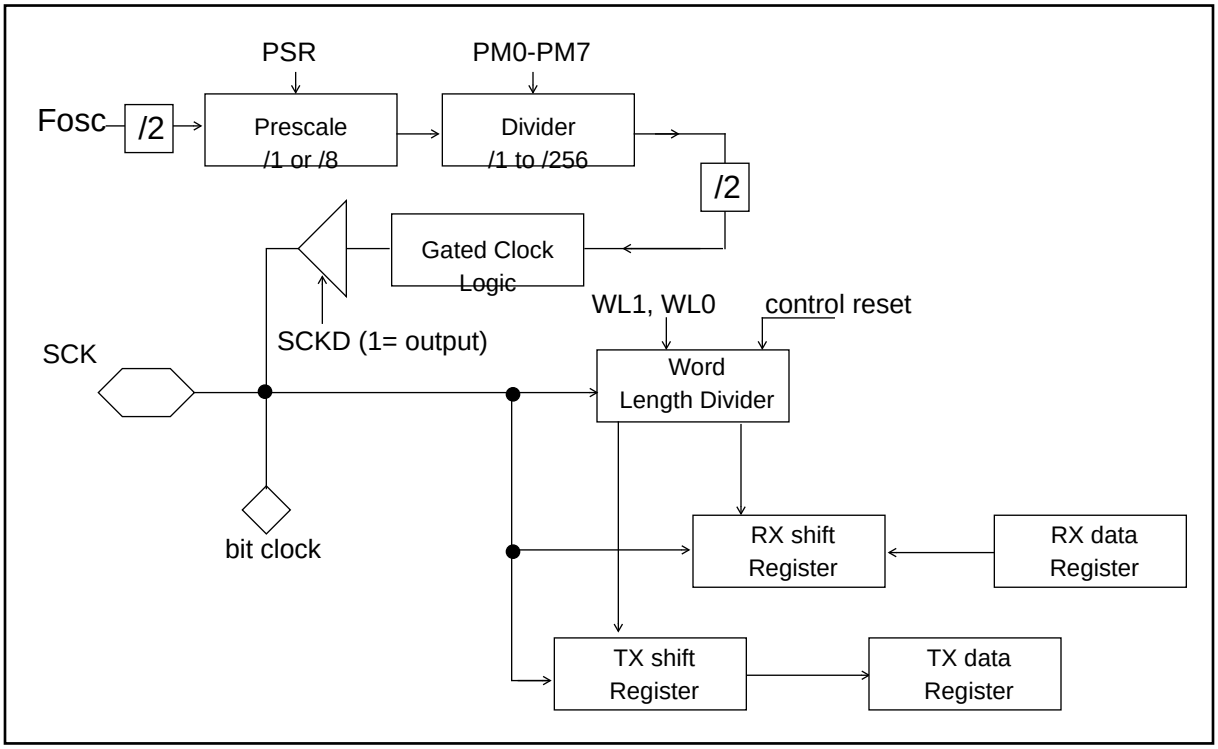


Figure 8-5 RSSI Clock Generator Functional Block Diagram

Figure 8-6 shows frame sync generation. When internally generated, both receive and transmit frame sync are generated from the word clock and are defined by the frame rate divider (DC2-DC0) bit and the word length (WL1-WL0) bits of CRA.

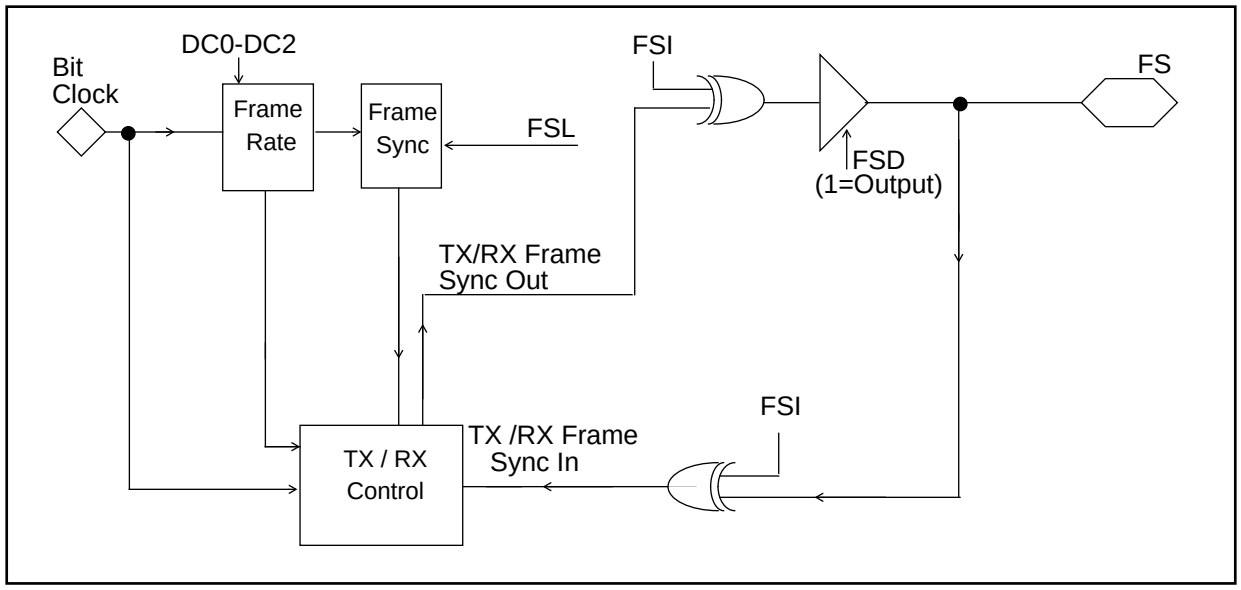


Figure 8-6 RSSI Frame Sync Generator Functional Block Diagram

8.4.1 Serial Transmit Data Pin — STD

The Serial Transmit Data Pin (STD) is used to transmit data from the Serial Transmit Shift Register. STD is an output when data is being transmitted and is three-stated between data word transmissions and on the trailing edge of the bit clock after the last bit of a word is transmitted.

8.4.2 Serial Receive Data Pin — SRD

The Serial Receive Data Pin (SRD) is used to bring serial data into the Receive Data Shift Register.

8.4.3 Serial Clock — SCK

The Serial Clock (SCK) pin can be used as either an input or an output. This clock signal is used by both the transmitter and receiver and can be either continuous or gated. During gated mode, SCK is valid only during the transmission of data, otherwise it is three-stated.

8.4.4 Serial Frame Sync — SFS

The Serial Frame Sync (FS) pin can be used as either an input or an output. The frame sync is used by both the transmitter and receiver to synchronize the transfer of data. The frame sync signal can be one bit or one word in length and can occur one bit before the transfer of data or right at the transfer of data. In the gated clock mode, frame sync signals are not used.

The pin signals are shown in Figure 8-7. Continuous and gated clock signals are shown as well as the bit length and word length frame sync signals.

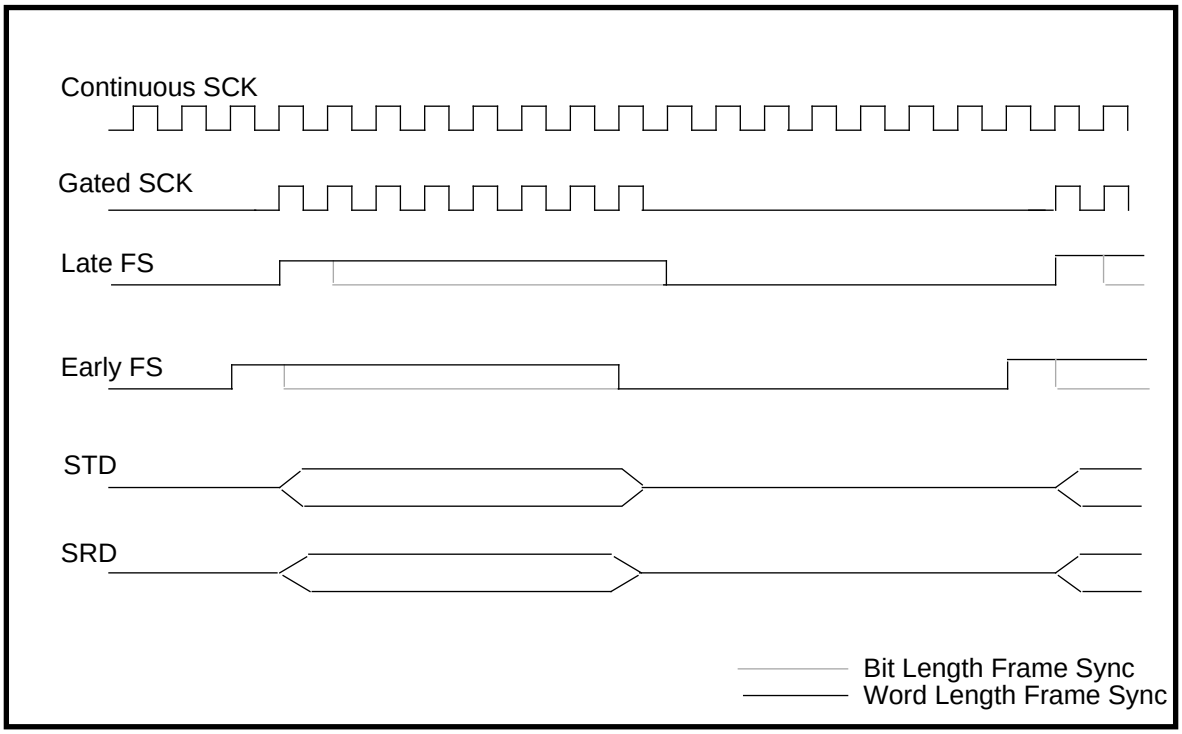


Figure 8-7 Serial Clock and Frame Sync Timing

8.5 RSSI RESET AND INITIALIZATION PROCEDURE

The RSSI is affected by three types of reset:

DSP Reset The DSP hardware reset is generated by asserting the $\overline{\text{RESET}}$ pin or the software reset is generated by executing the RESET instruction. The DSP hardware or software reset clears the SSI enable bit (SSIEN) in control register B which disables the RSSI. All other status and control bits in the RSSI are affected as described below.

RSSI Reset The RSSI reset is generated when the SSI enable bit (SSIEN) in control register B is cleared. The RSSI status bits are preset to the same state produced by the DSP reset. The RSSI control bits are unaffected. The RSSI reset is useful for selective reset of the RSSI interface without changing the present RSSI control bits and without affecting the other peripherals.

STOP Reset The STOP reset is caused by executing the STOP instruction. During the stop state no clocks are active in the chip. The RSSI status bits are preset to the same state produced by the DSP reset. The RSSI control bits are unaffected.

The correct sequence to initialize the RSSI interface is as follows:

1. DSP reset or RSSI reset.
2. Program RSSI control registers.
3. Set the SSI enable bit (SSIEN) in control register B.

The DSP programmer should use the DSP or RSSI reset before changing the MOD, FSI, FSL, SHFD, SCKP, SCKD, FSD, GCK, ELFS, WL0, or WL1 control bits to ensure proper operation of the RSSI interface. That is, these control bits should not be changed during RSSI operation.

Note: The RSSI clock must go low for at least one complete period to ensure proper RSSI reset.

8.6 RSSI INTERFACE PROGRAMMING MODEL

The registers comprising the RSSI interface are shown in Figure 8-8. Note that the Codec device labels the MSB as bit 0, whereas the DSP labels the LSB as bit 0. Therefore, when using a standard Codec, the DSP MSB (or Codec bit 0) is shifted out first, and the MSB of CRB should be cleared.

RSSI CONTROL and STATUS REGISTERS

15	14	13	12	11	10	9	8
PSR	WL1	WL0	*	*	DC2	DC1	DC0
7	6	5	4	3	2	1	0
PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

READ-WRITE RSSI CONTROL REGISTER A (CRA) ADDRESS $FFD0/D8

15	14	13	12	11	10	9	8
RIE	TIE	RE	TE	MOD	SSIEN	FSI	FSL
7	6	5	4	3	2	1	0
SHFD	SCKP	SCKD	FSD	GCK	ELFS	*	*

READ-WRITE RSSI CONTROL REGISTER B (CRB) ADDRESS $FFD1/D9

7	6	5	4	3	2	1	0
RDF	TDE	ROE	TUE	TRFS	*	*	*

READ-ONLY RSSI STATUS REGISTER (SR) ADDRESS $FFF0/F8

15 ... 8	7 ... 0
A Dummy Register, No Content Is Actually Written	

WRITE-ONLY RSSI TIME SLOT REGISTER (TSR) ADDRESS $FFF0/F8

15 ... 8	7 ... 0
HIGH BYTE	LOW BYTE

SERIAL RECEIVE SHIFT REGISTER

15 ... 8	7 ... 0
HIGH BYTE	LOW BYTE

READ-ONLY SERIAL RECEIVE REGISTER (Addr X:$FFF1/F9)

15 ... 8	7 ... 0
HIGH BYTE	LOW BYTE

SERIAL TRANSMIT SHIFT REGISTER

15 ... 8	7 ... 0
HIGH BYTE	LOW BYTE

WRITE-ONLY SERIAL TRANSMIT REGISTER (Addr X:$FFF1/F9)

** - Reserved bits, read as zero, should be written with zero for future compatibility.

Figure 8-8 RSSI Programming Model

8.7 RSSI TRANSMIT SHIFT REGISTER

The Transmit Shift Register (TSR) is a 16 bit shift register that contains the data being transmitted. When a continuous clock is used, data is shifted out to the serial transmit data STD pin by the selected (internal/external) bit clock when the associated (internal/external) frame sync is asserted. When a gated clock is used, data is shifted out to the serial transmit data STD pin by the selected (internal/external) gated clock. The Word Length control bits (WL1-WL0), in RSSI Control Register A, determine the number of bits to be shifted out of the TSR before it is considered empty and may be written to again. This word length can be 8, 12, or 16 bits. The data to be transmitted occupies the most significant portion of the shift register. The unused portion of the register is ignored. Data is always shifted out of this register with the most significant bit (MSB) first when the SHFD bit of the control register B is cleared. If this bit is set, the least significant bit (LSB) is shifted out first.

8.8 RSSI TRANSMIT DATA REGISTER (TX)

The Transmit Data Register is a 16-bit write-only register. Data to be transmitted is written into this register and is automatically transferred to the transmit shift register. The data written should occupy the most significant portion of the transmit data register. The unused bits (least significant portion) of the transmit data register are don't care bits. The DSP is interrupted whenever the transmit data register becomes empty provided that the transmit data register empty interrupt has been enabled.

Note: When early frame sync is selected (ELFS=1), if data is written into TX in the time between the frame sync and transmission of the first bit, the data will not be transmitted. TDE and TUE will be set when the first bit is transmitted.

8.9 RSSI RECEIVE SHIFT REGISTER

The Receive Shift Register is a 16 bit shift register that receives incoming data from the serial receive data SRD pin. When a continuous clock is used, data is shifted in by the selected (internal/external) bit clock when the associated (internal/external) frame sync is asserted. When a gated clock is used, data is shifted in by the selected (internal/external) gated clock. Data is assumed to be received most significant bit (MSB) first if the SHFD bit of CRB is cleared. If this bit is set, the data is received least significant bit (LSB) first. Data is transferred to the RSSI Receive Data Register after 8, 12, or 16 bits have been shifted in depending on the Word Length control bits (WL1-WL0) in RSSI Control Register A.

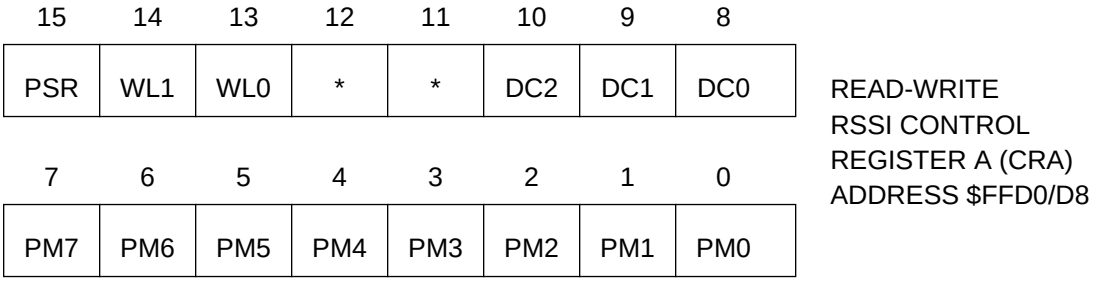
8.10 RSSI RECEIVE DATA REGISTER (RX)

The RSSI Receive Data Register is a 16 bit read-only register that accepts data from the Receive Shift Register as it becomes full. The data read will occupy the most significant portion of the receive data register. The unused bits (least significant portion) will read as

zeros. The DSP is interrupted whenever the receive data register becomes full if the associated interrupt is enabled.

8.11 RSSI CONTROL REGISTER A (CRA)

The RSSI Control Register A (CRA) is one of two 16 bit read/write control registers used to direct the operation of the Synchronous Serial Interface. The CRA controls the RSSI clock generator bit and frame sync rates, word length, and number of words per frame for the serial data. The DSP reset clears all CRA bits. RSSI reset and STOP reset do not affect the CRA bits. The CRA control bits are described in the following paragraphs.



*unused bits should be set to zero

8.11.1 CRA Prescale Modulus Select (PM7-PM0) Bits 0-7

The Prescale Modulus Select bits (PM7 through PM0) specify the divide ratio of the prescale divider in the RSSI clock generator. This prescaler is used only in internal clock mode to divide the internal clock of the core. A divide ratio from 1 to 256 (PM=$00 to $FF) may be selected.The bit clock output is available at the clock SCK. The bit clock output is also available internally for use as the bit clock to shift the transmit and receive shift registers. Careful choice of the crystal oscillator frequency and the prescaler modulus will allow the telecommunication industry standard codec master clock frequencies of 2.048 MHz, 1.544 MHz, and 1.536 MHz to be generated. For example, a 24.576 MHz clock frequency may be used to generate the standard 2.048 MHz and 1.536 MHz rates, and a 24.704 MHz clock frequency may be used to generate the standard 1.544 MHz rate.Table 8-2. gives examples of PM7-PM0 values that can be used in order to generate different bit clocks.

Table 8-2. RSSI bit clock as a function of Fosc and PM7-PM0 (PSR=0)

Fosc (MHz)	Max bit Clock (MHz)	PM7-PM0 Values for different SCK				
		2.048Mhz	1.544Mhz	1.536Mhz	128Khz	64Khz
16.384	4.096	1	—	—	31($1F)	63($3F)
18.432	4.608	—	—	2	35($23)	71($47)
20.480	5.12	—	—	—	39($27)	79($4F)
26.624	6.656	—	—	—	51($33)	103($67)
24.576	6.144	2	—	3	47($2F)	95($5F)
24.704	6.176	—	3	—	—	—
32.768	8.192	3	—	—	63($3F)	127($7F)
36.864	9.216	—	—	5	71($47)	143(8F)
49.152	12.288	5	—	7	95($5F)	191($BF)
49.408	12.352	—	7	—	—	—

The bit clock on the RSSI can be calculated from the Fosc value using the following equation:

$$SCK = Fosc \prod (4 \times [7PSR+1] \times (PM+1))$$

8.11.2 CRA Frame Rate Divider Control (DC2-DC0) Bits 8-10

The Frame Rate Divider Control bits (DC2, DC1, and DC0) control the divide ratio for the programmable frame rate dividers. It operates on the word clock.

In normal mode, this ratio determines the word transfer rate. In network mode this ratio may be interpreted as the number of words per frame. The divide ratio may range from 1 to 8 (DC = 000 to 111) for normal mode and 2 to 8 (DC = 001 to 111) for network mode.

Examples:

In 8 bit word normal mode:

DC2-DC0= 1, PM7-PM0=9, PSR=1, Fosc = 40.96MHz would give a bit clock of 40.96Mhz ÷ [8x4x10] = 128 kHz. The 8-bit word rate being equal to two, the sampling rate (FS rate) would then be 128 kHz ÷ [2x8] = 8kHz.

In 8 bit word network mode:

DC2-DC0= 6, PM7-PM0=80, PSR=0, Fosc = 62.22MHz would give a bit clock of 62.22Mhz ÷ [4x81] = 0.192 MHz for a 7 slot TDM multiplex of 8-bit words. The sampling rate for every word (FS rate) would then be 0.192 MHz ÷ [3x8] = 8kHz.

8.11.3 CRA Word Length Control (WL0, WL1) Bits 13 and 14

The Word Length Control bits (WL1-WL0) are used to select the length of the data words being transferred via the RSSI. Word lengths of 8, 12 or 16 bits may be selected as shown in Table 8-3.

Table 8-3. RSSI Data Word Lengths

WL1	WL0	Number of bits/word
0	0	8
0	1	(Reserved)
1	0	12
1	1	16

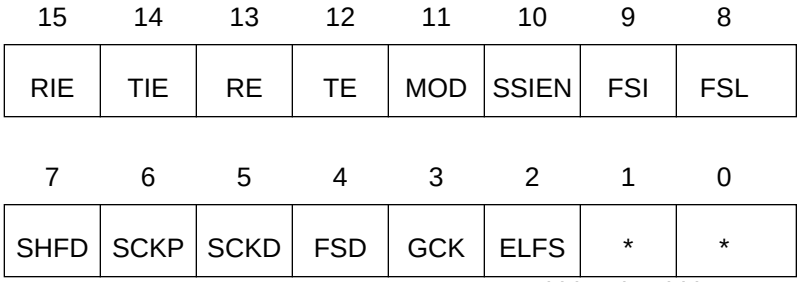
These bits control the Word Length Divider shown in the RSSI Clock Generator. The WL control bits also control the frame sync pulse length when FSL=0.

8.11.4 CRA Prescaler Range (PSR) Bit 15

The Prescaler Range (PSR) controls a fixed divide-by-eight prescaler in series with the variable prescaler. It is used to extend the range of the prescaler for those cases where a slower bit clock is desired. When PSR is cleared, the fixed prescaler is bypassed. When PSR is set, the fixed divide-by-eight prescaler is operational. This allows a 128kHz master clock to be generated for Motorola MC1440X series codecs. The maximum internally generated bit clock frequency is Fosc/4 and the minimum internally generated bit clock frequency is Fosc/(4*8*256).

8.12 RSSI CONTROL REGISTER B (CRB)

The RSSI Control Register B (CRB) is one of two 16 bit read/write control registers used to direct the operation of the RSSI. The RSSI reset is controlled by a bit in the CRB. CRB controls the direction of the bit clock pin SCK and the frame sync pin FS. Interrupt enable bits for each data register interrupt are provided in this control register. RSSI operating modes are also selected in this register. The DSP reset clears all CRB bits. However, RSSI reset and STOP reset do not affect the CRB bits. The RSSI Control Register B bits are described in the following paragraphs.



READ-WRITE
RSSI1 CONTROL
REGISTER B (CRB)
ADDRESS $FFD1/D9

*Unused bits should be set to zero.

8.12.1 CRB Early/Late Frame Sync Bit (ELFS) Bit 2

The early/late frame sync bit (ELFS) controls when the frame sync is initiated for the transmit and receive sections. When ELFS is cleared, the frame sync is initiated as the first bit of data is transmitted and/or received. When ELFS is set, the frame sync is initiated one bit before the data is transmitted and/or received. The frame sync is disabled after one bit for bit length frame sync and after one word for word length frame sync.

8.12.2 CRB Gated Clock (GCK) Bit 3

The gated clock bit (GCK) selects the type of clock signal used to clock the Transmit Shift Register and the Receive Shift Register. When GCK is cleared, the clock signal is a continuous clock. When GCK and SCKD are set, the clock signal is an internally gated clock. The internally gated clock will run only when the transmitter is enabled (TE=1) during a valid time slot. When GCK is set and SCKD is cleared, the clock signal is an externally gated clock. The gated clock signal is useful when interfacing with microcontrollers.

8.12.3 CRB Frame Sync Direction (FSD) Bit 4

The Frame Sync Direction bit (FSD) controls the direction of the FS pin for the transmit and receive sections. When FSD is cleared, the FS pin is an input, meaning that the frame sync is supplied from an external source. When FSD is set, the FS pin is an output, meaning that the frame sync is generated internally.

8.12.4 CRB Clock Source Direction (SCKD) Bit 5

The Clock Source Direction bit (SCKD) selects the source of the clock signal used to clock the Transmit Shift Register and the Receive Shift Register. When SCKD is set, the clock source is internal and is the bit clock output of the RSSI clock generator. This clock will also appear at the SCK pin when SCKD is set. When SCKD is cleared, (1) the clock source is external, (2) the internal clock generator is disconnected from the SCK pin and (3) an external clock source may drive this pin to clock the Transmit Shift Register and the Receive Shift Register.

8.12.5 CRB Clock Polarity Bit (SCKP) Bit 6

The clock polarity bit controls which bit clock edge is used to clock out data and latched in data. If SCKP=0, the data is clocked out on the rising edge of the bit clock and latched in on the falling edge of the clock. If SCKP = 1, the falling edge of the clock is used to clock the data out and the rising edge of the clock is used to latch the data in.

8.12.6 CRB MSB/LSB Position Bit (SHFD) Bit 7

The SHFD bit controls whether the MSB or LSB is transmitted and received first. If SHFD = 0, the data is transmitted and received MSB first. If SHFD = 1, the LSB is transmitted and received first.

8.12.7 CRB Frame Sync Length (FSL) Bit 8

The Frame Sync Length (FSL) bit selects the length of the frame sync signal to be generated or recognized. If FSL=1, then a one clock bit long frame sync is selected. If FSL=0, a one word long frame sync is selected.The length this frame sync is the same as the length of the data word selected by WL0 and WL1.

8.12.8 CRB Frame Sync Invert (FSI) Bit 9

The Frame Sync Invert (FSI) bit selects the logic of frame sync I/O. If FSI=1, the frame sync is active low. If FSL=0, the frame sync is active high.

8.12.9 CRB RSSI Enable Bit (SSIEN) Bit 10

The RSSI enable (SSIEN) bit enables and disables the RSSI. If SSIEN=1, the RSSI is enabled, which causes an output frame sync to be generated (FSD=1) or causes the RSSI to wait for the input frame sync (FSD=0). If SSIEN=0, the RSSI is disabled. When disabled, the output clock and frame sync will be three-stated, the status register bits will be preset to the same state produced by the DSP reset, and the control register bits will not be affected.

8.12.10 CRB RSSI Mode Select (MOD) Bit 11

The Mode select bit (MOD) selects the operational mode of the RSSI. When MOD is cleared, the normal mode is selected. When MOD is set, the network mode is selected.

8.12.11 CRB RSSI Transmit Enable (TE) Bit 12

The RSSI Transmit Enable (TE) bit enables the transfer of TX to the Transmit Shift Register and also enables the internal gated clock. When TE is set and a word boundary is detected, the transmit portion of the RSSI is enabled. When TE is cleared, the transmitter will continue to transmit the data currently in the RSSI Transmit Shift Register and then disable the transmitter. The serial output is three-stated and any data present in

TX will not be transmitted, i.e. data can be written to TX with TE cleared, TDE will be cleared but data will not be transferred to the Transmit Shift Register. If TE is disabled and then re-enabled during the same transmitted word, then the data will continue to be transmitted. If TE is re-enabled during a different word slot, then data will not be transmitted until the next word boundary.**The normal transmit enable sequence for transmit is to write data to TX or to TSR before setting TE. The normal transmit disable sequence is to clear TE and TIE after TDE=1.**

When an internal gated clock is being used, the gated clock will run during valid word slots if the TE bit is set. If TE is disabled, the transmitter will continue to transmit the data currently in the RSSI Transmit Shift Register and then the clock will stop. When TE is re-enabled, the gated clock will start immediately and will run during any valid word slots.

Note: The function of disabling and enabling TE is different from the DSP56156 SSI.

8.12.12 CRB RSSI Receive Enable (RE) Bit 13

When the RSSI Receive Enable (RE) bit is set, the receive portion of the RSSI is enabled. When this bit is cleared, the receiver will be disabled by inhibiting data transfer into RX. If data is being received while this bit is cleared, the rest of the word will not be shifted in and transferred to the RSSI Receive Data Register. If RE is re-enabled during a word slot before the second to last bit then that word will be received.

Note: The function of disabling and enabling RE is different from the DSP56156 SSI.

8.12.13 CRB RSSI Transmit Interrupt Enable (TIE) Bit 14

When the RSSI Transmit Interrupt Enable bit (TIE) is set, the program controller will be interrupted when the RSSI Transmit Data Register Empty flag (TDE) in the RSSI Status Register is set. When TIE is cleared, this interrupt is disabled. However, the TDE bit will always indicate the transmit data register empty condition even when the transmitter is disabled by the TE bit. Writing data to the TX or TSR register will clear TDE thus clearing the interrupt.

There are two transmit data interrupts (these have separate interrupt vectors):

1. Transmit data with exception status.
   This interrupt is generated on the following condition:

   TIE=1 and TDE=1 and TUE=1

2. Transmit data without exceptions.
   This interrupt is generated on the following condition:

   TIE=1 and TDE=1 and TUE=0

8.12.14 CRB RSSI Receive Interrupt Enable (RIE) Bit 15

When the RSSI Receive Interrupt Enable bit (RIE) is set, the program controller will be interrupted when the RSSI Receive Data Register Full flag (RDF) in the RSSI Status Register is set. If RIE is cleared, this interrupt is disabled. However, the RDF bit still indicates the receive data register full condition. Reading the receive data register will clear RDF and thus clear the pending interrupt.

There are two receive data interrupts which have separate interrupt vectors:

1. Receive Data with exception status — This interrupt is generated on the following condition:

   RIE=1 and RDF=1 and ROE=1

2. Receive Data without exceptions — This interrupt is generated on the following condition:

   RIE=1 and RDF=1 and ROE=0

8.13 RSSI STATUS REGISTER

The RSSI Status Register (SR) is a 16-bit read only status register used by the DSP to interrogate the status and serial input flags of the Synchronous Serial Interface. The status bits are described in the following paragraphs.

7	6	5	4	3	2	1	0
RDF	TDE	ROE	TUE	TRFS	*	*	*

READ-ONLY
RSSI STATUS
REGISTER (SR)
ADDRESS $FFF0/F8

*Unused bits should be set to zero.

Note: All the flags in the SR are updated after the first bit of the next SSI word has completed transmission or reception.

8.13.1 RSSISR Transmit/Receive Frame Sync (TRFS) Bit 3

When set, the Transmit/Receive Frame Sync flag (TRFS) indicates that a frame sync occurred during transmission of the last word written to the Tx register or receiving of the next word into the Rx register. Data written to the transmit data register during the time slot when TRFS is set will be transmitted during the second time slot (network mode) or in the next first time slot (normal mode). In network mode, TRFS is set during transmission or receiving of the first slot of the frame. It will then be cleared when starting transmission or receiving of the next slot.

TRFS is cleared by DSP, RSSI or STOP reset.

Note: This bit functions differently than the DSP56156 SSI TFS/RFS bits.

8.13.2 RSSISR Transmitter Underrun Error (TUE) Bit 4

The Transmitter Underrun Error (TUE) flag is set when the Serial Transmit Shift Register is empty (no data to be transmitted) and a transmit time slot occurs. When a transmit underrun error occurs, the previous data will be re-transmitted.

A transmit time slot in the normal mode occurs when the frame sync is asserted. In the network mode, each time slot requires transmit data and is therefore a transmit time slot. (TE=1)

TUE does not cause any interrupts; however, TUE does cause a change in the interrupt vector used for transmit interrupts so that a different interrupt handler may be used for a transmit underrun condition. If a transmit interrupt occurs with TUE set, the Transmit Data With Exception Status interrupt will be generated. If a transmit interrupt occurs with TUE clear, the Transmit Data Without Errors interrupt will be generated.

TUE is cleared by DSP, RSSI, or STOP reset. TUE is cleared by reading the SR with TUE set followed by writing TX or TSR.

8.13.3 RSSISR Receiver Overrun Error (ROE) Bit 5

The Receiver Overrun Error flag (ROE) is set when the serial receive shift register is filled and ready to transfer to the receiver data register (RX) and the RX is already full (i.e. RDF=1). The Receiver Shift Register is not transferred to RX. ROE does not cause any interrupts; however, ROE does cause a change in the interrupt vector used so that a different interrupt handler may be used for a receive overrun condition. If a receive interrupt occurs with ROE set, the Receive Data With Exception Status interrupt will be generated and if a receive interrupt occurs with ROE clear, the Receive Data Without Errors interrupt will be generated.

ROE is cleared by DSP, RSSI, or STOP reset and is cleared by reading the SR with ROE set followed by reading the RX. Clearing RE does not affect ROE.

8.13.4 RSSISR Transmit Data Register Empty (TDE) Bit 6

The RSSI Transmit Data Register Empty flag (TDE) is set when the contents of the Transmit Data Register are transferred to the Transmit Shift Register. When set, TDE indicates that data should be written to the TX or to the time slot register (TSR) before the transmit shift register becomes empty (which would cause an underrun error).

TDE is cleared when the DSP writes to the Transmit Data Register or when the DSP writes to the TSR to disable transmission of the next time slot. If TIE is set, a RSSI Transmit Data interrupt request will be issued when TDE is set. The vector of the interrupt will

depend on the state of the Transmitter Underrun TUE bit. TDE is set by DSP, RSSI, and STOP reset.

8.13.5 RSSISR Receive Data Register Full (RDF) Bit 7

The RSSI Receive Data Register Full flag (RDF) is set when the contents of the Receive Shift Register are transferred to the Receive Data Register. RDF is cleared when the DSP reads the Receive Data Register. If RIE is set, a DSP receive data interrupt request will be issued when RDF is set. The interrupt request vector will depend on the state of the Receiver Overrun ROE bit. RDF is cleared by DSP, RSSI, and STOP reset.

8.14 TIME SLOT REGISTER — TSR

The Time Slot Register (TSR) is used when the data is not to be transmitted in the available transmit time slot. For the purposes of timing, the time slot register is a write-only register that behaves like an alternative transmit data register except that rather than transmitting data, the transmit data pin, STD is three-stated. Using this register is important for avoiding overflow/underflow during inactive time slots.

8.15 NORMAL AND NETWORK OPERATING MODES

In the normal mode, the frame rate divider determines the word transfer rate — one word is transferred per frame sync during the frame sync time slot. In network mode, a word is (possibly) transferred every time slot.

8.15.1 Normal Mode Transmit

The conditions for data transmission from the RSSI are:

1. SSI enabled (SSIEN=1)
2. Transmitter Enabled (TE=1)
3. Frame sync is active (continuous clock only)
4. Bit clock begins (gated clock only)

When the above conditions occur in normal mode, the next data word will be transferred from TX to the transmit shift register, the TDE flag will be set (transmitter empty), and the transmit interrupt will occur if TIE=1 (transmit interrupt is enabled). The new data word will be transmitted immediately.

The transmit data output (STD) is three-stated except during the data transmission period. For a continuous clock, the optional frame sync output and clock outputs are not three-stated even if both receiver and transmitter are disabled.

8.15.2 Normal Mode Receive

If the receiver is enabled, then for a continuous clock, each time the frame sync signal is generated (or detected) a data word will be clocked in, and for a gated clock, each time the clock begins a data word will be clocked in. After receiving the data word it will be transferred from the RSSI Receive Shift Register to the Receive Data Register (RX), the RDF flag will be set (Receiver full), and the Receive Interrupt will occur if it is enabled (RIE=1).

The DSP program has to read the data from RX before a new data word is transferred from the Receive Shift Register, otherwise the Receiver Overrun error will be set (ROE).

The transmitter and receiver timing in normal mode for an eight bit word with two words per time slot is shown in Figure 8-9. Both continuous and gated clock are shown with a late word length frame sync.

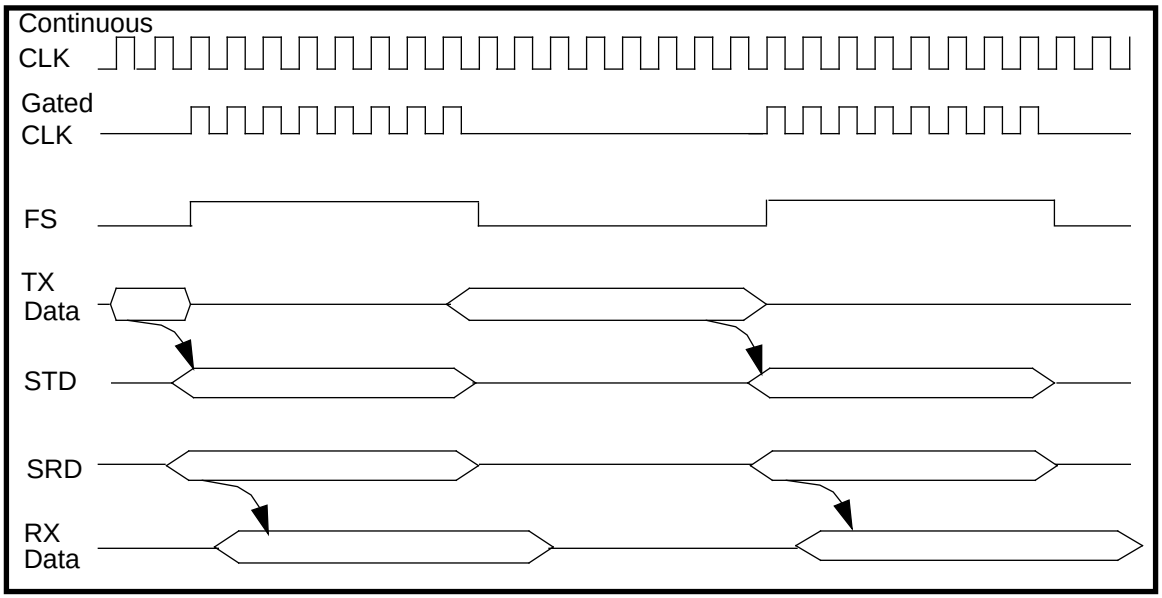


Figure 8-9 Normal Mode Timing

8.15.3 Network Mode

In this mode, the RSSI can be used in TDM networks. It is the typical mode in which the DSP would interface to a TDM codec network or a network of DSPs. The DSP may be a master device that controls its own private network or a slave device that is connected to an existing TDM network and occupies a few time slots. The distinction of the network mode is that it identifies each time slot (data word time) and allows the option of ignoring the time slot by writing to TSR or transmitting data during the time slot. The receiver is treated in the same manner except that data is always being shifted into the Receive Shift

Register and transferred to the RX. The DSP will read the receive data register and either use it or discard it.

The frame sync signal indicates the beginning of a new data frame. Each data frame is divided into time slots and transmission and/or reception can occur in each time slot (rather than in just the frame sync time slot as in normal mode). The frame rate dividers, controlled by DC2, DC1, and DC0 select two to eight time slots per frame.

8.15.3.1 Network Mode Transmit

The transmit portion of RSSI is enabled when SSIEN=1 and TE=1. However, for continuous clock, when TE is set, the transmitter will be enabled only after detection of a new word slot (if TE is enabled during a slot other than the first). This is different from the DSP56156 SSI. **Software will have to find the start of the next frame.** For a gated clock, when TE is set, the transmitter will be enabled as soon as the clock begins.

Normal start up sequence for transmission is to:

1. Write the data to be transmitted to the Transmit Register (TX). This clears the TDE flag.
2. Set TE and TIE to enable the transmitter
   - on the next word boundary (continuous clock)
   - or on the next clock signal (gated clock).
3. Enable transmit interrupts.

Alternatively, the DSP programmer may decide to NOT transmit in a time slot by writing to the Time Slot Register (TSR). This will clear the TDE flag just as if data were going to be transmitted but the STD pin will remain in three-state during the time slot.

When the frame sync is detected or generated (continuous clock) or the first clock signal is detected or generated (gated clock) then the first enabled data word will be transferred from TX to the Transmit Shift Register and will be shifted out (transmitted). TX now being empty will cause TDE to be set which, if TIE is set, will cause a transmitter interrupt. Software can poll TDE or use interrupts to reload the TX register with new data for the next time slot or write to the TSR to prevent transmitting in the next time slot. Failing to reload TX (or writing to the TSR) before the Transmit Shift Register is finished shifting (empty) will cause (1) a transmitter underrun, (2) the TUE error bit to be set and (3) the STD pin will be three-stated for the next time slot.

The operation of clearing TE will disable the transmitter after completion of transmission of the current data word. Setting TE will enable transmission of the next word. During that time the STD pin will be three-stated. TE should be cleared after TDE is set to ensure that all pending data is transmitted.

To summarize, the network mode transmitter generates interrupts every enabled time slot and requires the DSP program to respond to each enabled time slot. These responses may be:

1. Write data register with data to enable transmission in the next time slot.
2. Write the time slot register to disable transmission in the next time slot.
3. Do nothing — transmit underrun will occur at the beginning of the next time slot and the previous data will be transmitted.

8.15.3.2 Network Mode Receive

The receiver portion of the RSSI is enabled when SSIEN=1 and RE =1. However, the receive enable will only take place during that word slot if RE is enabled before the second to last bit of the word. If the RE bit is cleared, the receiver will be disabled immediately. This is different from the DSP56156 SSI. **Software will have to find the start of the next frame.**

When the word is completely received, it is transferred to the RX data register which sets the RDF flag (Receive Data register full). Setting RDF will cause a receive interrupt to occur if the receiver interrupt is enabled (RIE=1).

The second data word (second time slot in the frame), begins shifting in immediately after the transfer of the first data word to the RX data register. The DSP program has to read the data from the RX data register (which clears RDF) before the second data word is completely received (ready to transfer to RX data register) or a receive overrun error will occur (ROE is set).

An interrupt can occur after the reception of each enabled data word or the programmer can poll the RDF flag. The DSP program response can be:

1. Read RX and use the data.
2. Read RX and ignore the data.
3. Do nothing — the receiver overrun exception will occur at the end of the current time slot.

Note: For a continuous clock, the optional frame sync output and clock output signals are not affected even if the transmitter and/or receiver are disabled. TE and RE do not disable the bit clock or the frame sync generation. The only way to disable the bit clock and the frame sync generation is to disable the SSI enable bit (SSIEN) in control register B. However, for a gated clock, no frame sync signals will be output and the clock signal is only enabled when TE is enabled and it is a valid time slot.

The transmitter and receiver timing for an eight bit word with three words per frame sync in network mode is shown in Figure 8-10 and Figure 8-11. A gated clock is shown in Figure 8-10 with the TE and RE bits. A continuous clock is shown in Figure 8-11 with the transmit and receive flags.

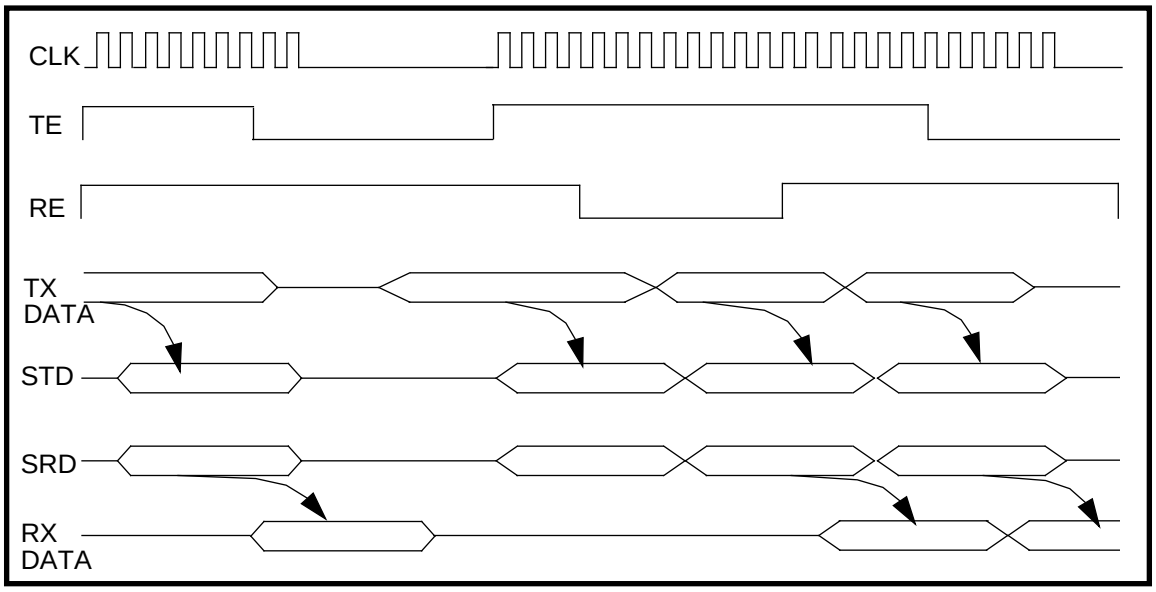


Figure 8-10 Network Mode Timing (Gated Clock)

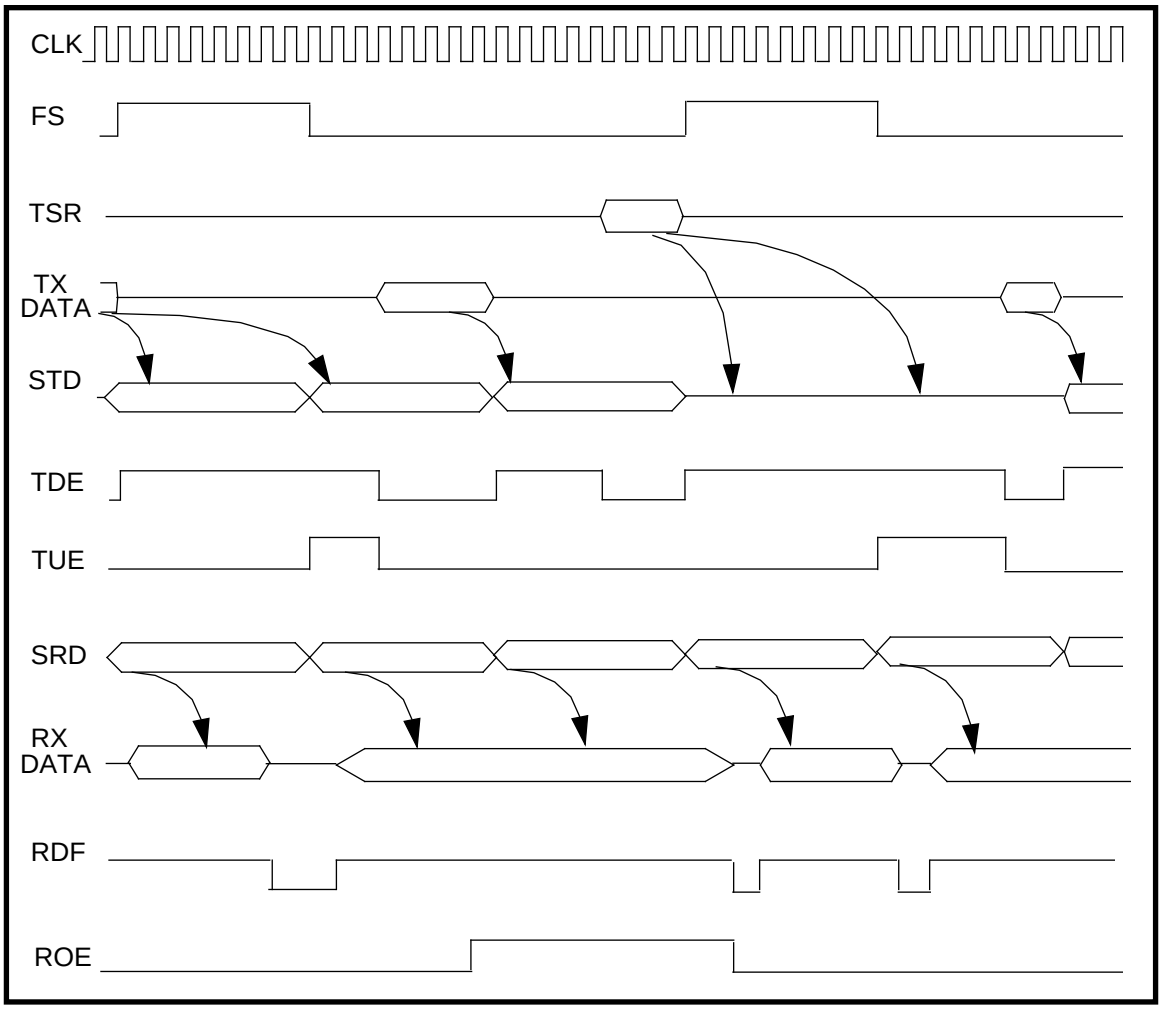


Figure 8-11 Network Mode Timing (Continuous Clock)