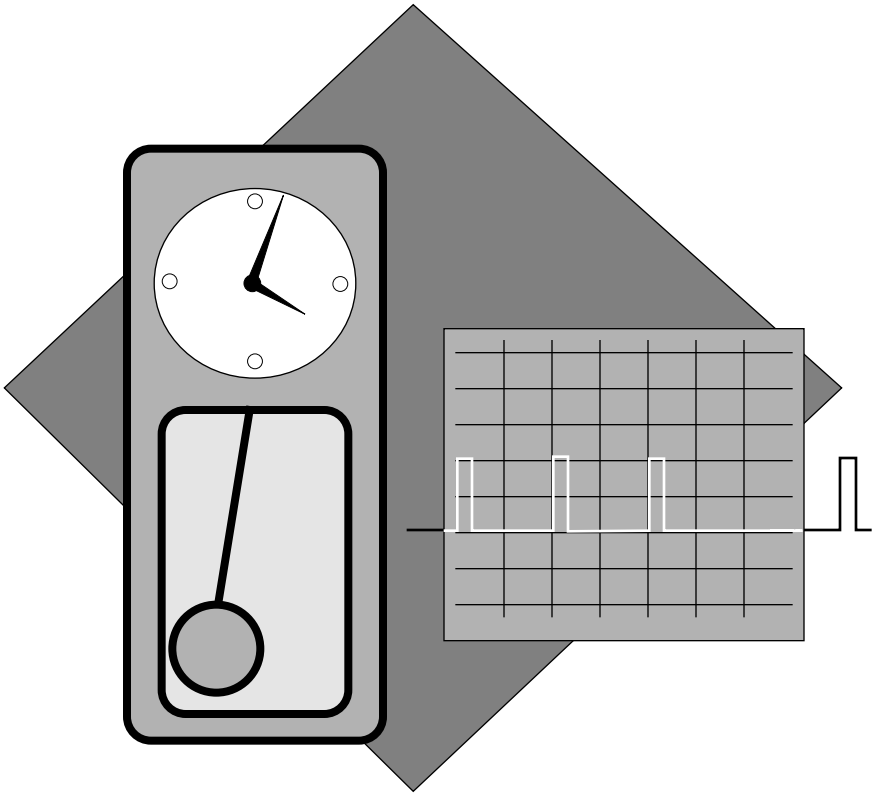
SECTION 7

16-BIT TIMER AND EVENT COUNTER



SECTION CONTENTS

7.1 INTRODUCTION

This section describes a general purpose 16-bit timer/event counter with either internal clocking to count internal events or external clocking to count external events. This timer/event counter can be used to either interrupt the DSP or to signal an external device at periodic intervals. A Timer Input pin (TIN) can be used as an event counter input and a Timer Output pin (TOUT) can be used as a timer pulse or for timer clock generation.

7.2 TIMER ARCHITECTURE

Figure 7-1 shows the general block diagram of the timer. It includes three 16-bit registers: the Timer Count Register (TCTR), the Timer Preload Register (TPR), and the Timer Compare Register (TCPR). An additional Timer Control Register (TCR) controls the timer operations.

A decrement register, programmed by the control register, is not available to the user. All other registers are read/write registers memory mapped as shown in Figure 7-2.

7.3 TIMER COUNT REGISTER (TCTR)

When the timer is enabled (TE=1), the 16-bit timer count register is decremented by one after the decrement register has reached the value zero. On the next event after the count register reaches the value zero, an overflow interrupt will be generated if the Overflow Interrupt Enable bit (OIE) is set in the timer control register. Also, the state of the TOUT pin can then be affected according to the mode selected by the Timer Out Enable bits (TO2-TO0) of the timer control register. If n is the value stored in the count register when the timer is enabled, the overflow interrupt occurs after (n+1)*(DC+1) input events, DC being the preset value of the decrement register. After reaching zero, the count register is reloaded with the contents of the preload register or with a direct value if a direct write to the count register had been executed after the last timer count register reload.

On the next event after the count register reaches the value of the compare register, a compare interrupt is generated if the Compare Interrupt Enable bit (CIE) is set in the timer control register. The state of the TOUT pin may also be affected according to the mode selected by the Timer Out Enable bits (TO2-TO0) of the timer control register.

The user program can write a new value into the count register anytime. If the timer is enabled (TE=1) during the write to the count register, this new value is written to the TCTR on the next count register decrement (next event after the decrement register reaches zero). If the timer is disabled (TE=0) during the write, the value is immediately written to the count register and will not be overwritten by the value stored in the preload register when the timer gets enabled (TE=1). In that case, the value stored or written in the preload reg-

ister will be loaded into the count register on the next event after it reaches zero, unless another write to the count register is performed in between. Refer to Section 7.8, Functional Description of the Timer, for more details.

The count register is initialized to zero on hardware $\overline{\text{RESET}}$ and software reset (RESET instruction).

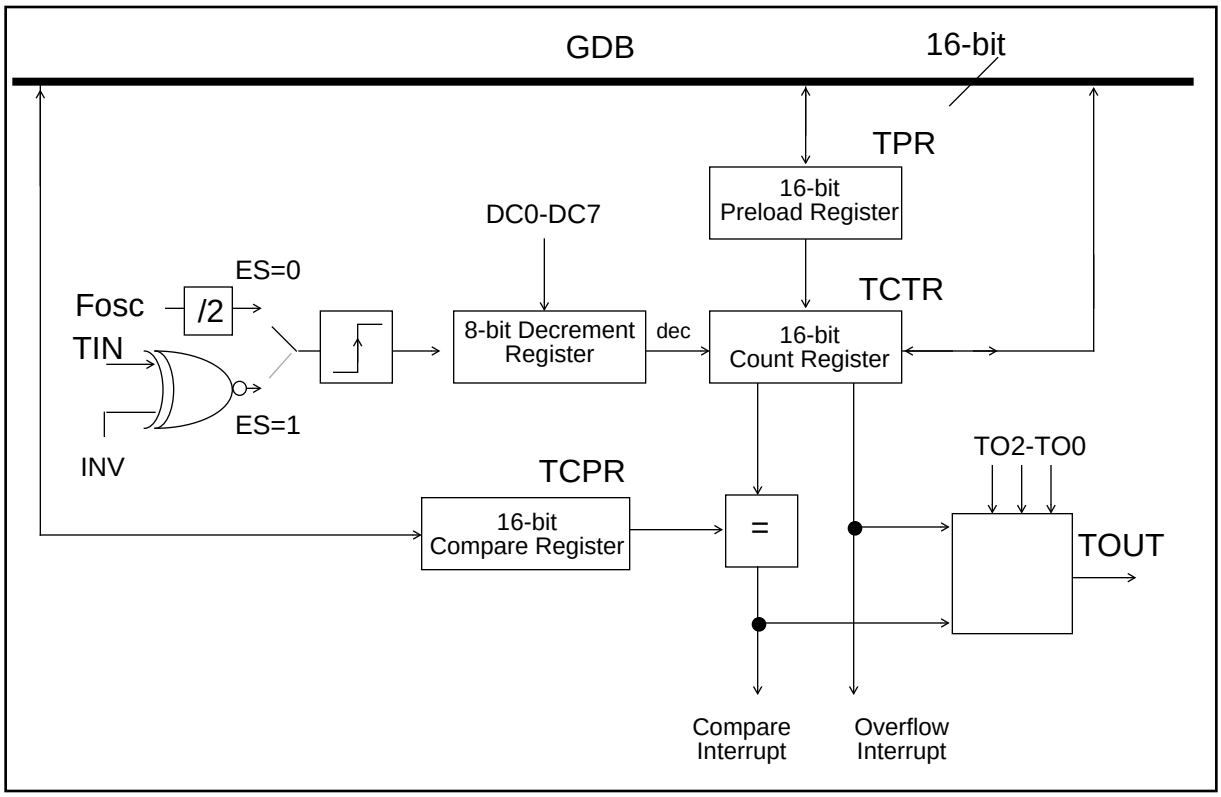


Figure 7-1 16-bit Timer General Block Diagram

7.4 TIMER PRELOAD REGISTER (TPR)

The preload register is a 16-bit read/write register which typically contains the value to be reloaded inside the count register when the timer is enabled and when the timer count register (TCTR) has been decremented to zero.

If the timer is enabled (TE=1) when the user program writes a new value inside the preload register (TPR), this new value is transferred to the count register the next time the count register is loaded (after it reaches zero), unless a direct write to the count register is performed while the TCTR is zero.

If the timer is disabled (TE=0) when the user program writes a new value inside the preload register, this new value transfers immediately into the count register unless a direct write to the TCTR has already been performed.

The preload register is initialized to zero by hardware $\overline{\text{RESET}}$ and software reset (RESET instruction).

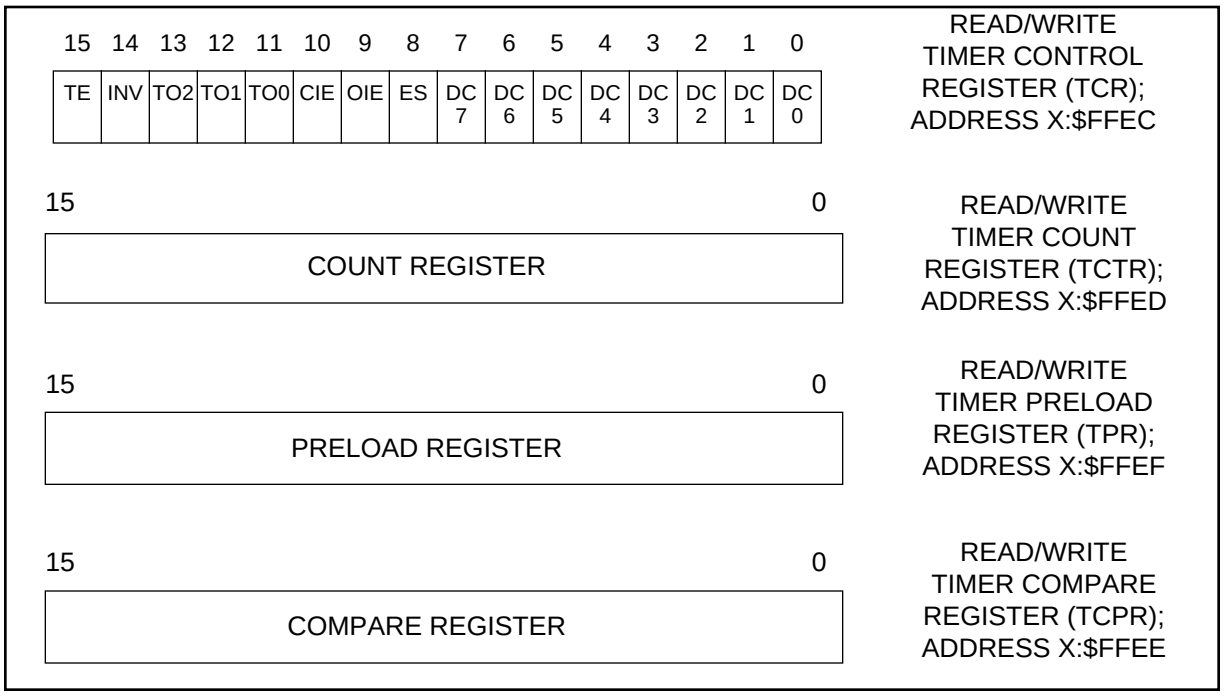


Figure 7-2 Timer Programming Model

7.5 TIMER COMPARE REGISTER (TCPR)

The output compare register is a 16-bit read/write register used to program an action when the value of the count register reaches the value contained in the compare register. The value in the compare register is compared against the value of the count register on every instruction cycle. At the next event after the compare matches, an interrupt is generated if interrupts are enabled (CIE=1) and the state of the TOUT pin changes according to the mode selected by the Timer Out Enable bits (TO2-TO0) of the timer control register. This is useful for providing a pulse width modulated timer output.

The compare register is initialized to zero by hardware $\overline{\text{RESET}}$ and software reset (RESET instruction).

7.6 TIMER CONTROL REGISTER (TCR)

The timer control register is a 16-bit read/write register that contains the control bits for the timer. The control bits are defined in the following paragraphs.

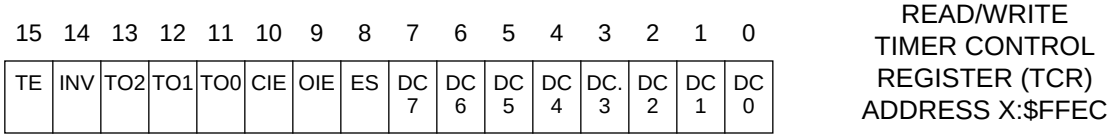


Figure 7-3 Timer Control Register

7.6.1 TCR Decrement Ratio (DC7-DC0) Bits 0-7

DC7-DC0 are eight clock divider bits that are used to preset an 8-bit counter which is decremented at the input clock rate. If DC7-DC0= n, n+1 clock cycles will be counted before decrementing the count register, i.e., the decrement register acts as a prescaler. The 8-bit decrement register is not accessible to the user.

If the timer is disabled (TE=0) when a new value is written to this field, the decrement register will start decrementing with this initial value when the timer is enabled (TE=1). If the timer is enabled (TE=1) when a new value is written to this field, the decrement register will be reloaded with this value after it has reached the value zero. DC7-DC0 are reset to zero on hardware $\overline{\text{RESET}}$ and software reset (RESET instruction).

7.6.2 TCR Event Select (ES) Bit 8

The event select bit (ES) selects the source of the timer clock. If ES is cleared, Fosc/2 is selected as input of the decrement register. If ES is set, an external signal coming from the TIN pin is used as input to the decrement register. The external signal is synchronized to the internal clock and should be lower than the maximum internal frequency Fosc/4. ES is cleared by hardware $\overline{\text{RESET}}$ and software reset (RESET instruction).

7.6.3 TCR Overflow Interrupt Enable (OIE) Bit 9

The overflow interrupt has precedence over the compare interrupt at the same priority level. A compare interrupt will remain pending until all pending overflow interrupts are serviced. When the Overflow Interrupt Enable bit (OIE) is set, the DSP will be interrupted at the next event after the count register reaches zero. When the OIE bit is cleared, this interrupt is disabled. OIE bit is cleared on hardware $\overline{\text{RESET}}$ and software reset (RESET instruction).

7.6.4 TCR Compare Interrupt Enable (CIE) Bit 10

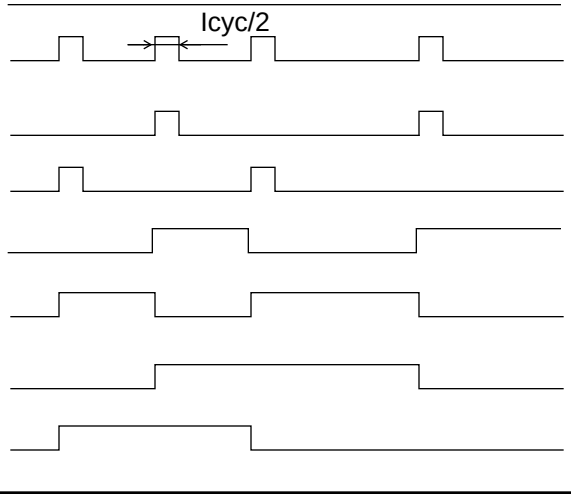
When the Compare Interrupt Enable bit (CIE) is set, the DSP will be interrupted at the next event after the count register reaches the value contained in the compare register. When the CIE bit is cleared, this interrupt is disabled. The CIE bit is cleared on hardware $\overline{\text{RESET}}$ and software reset (RESET instruction).

7.6.5 TCR Timer Output Enable (TO2-TO0) Bits 11-13

The three timer output enable bits (TO2-TO0) are used to program the function of the timer output pin (TOUT). Table 7-1 shows the relationship between the value of TO2-TO0 and the function of the TOUT pin. These bits are cleared on hardware $\overline{\text{RESET}}$ and software reset (RESET instruction).

Table 7-1 TOUT Pin Function

TO2	TO1	TO0	Function of TOUT	Signal on TOUT
0	0	0	TOUT disabled	
0	0	1	Compare/Overflow pulse	
0	1	0	Overflow pulse	
0	1	1	Compare pulse	
1	0	0	Overflow/Compare toggle	
1	0	1	Compare/Overflow toggle	
1	1	0	Overflow toggle	
1	1	1	Compare toggle	



Note: If one of the toggle modes is selected and TE is written as zero while the TOUT pin is either high or low, the pin remains in the same state. If the TO2 bit is written as zero with the TE bit, the pin will remain high and will go low when the timer is re-enabled. Writing the TO2 bit as zero before writing the TE bit as zero will clear the TOUT pin, i.e., in the non-toggle modes, TOUT is normally low.

7.6.6 TCR Inverter Bit (INV) Bit 14

When the inverter bit INV is set, the external signal coming in the TIN pin is inverted before entering the 8-bit decrement register. All 1 to 0 transitions of the TIN pin will then decrement the decrement register. When the INV bit is cleared, the external signal on TIN is not

inverted and the decrement register is decremented on all 0 to 1 transitions. INV is cleared on hardware $\overline{\text{RESET}}$ and software reset (RESET instruction).

7.6.7 TCR Timer Enable (TE) Bit 15

The TE bit is used to enable or disable the timer. Setting the TE bit will enable the timer. The decrement register will start decrementing from its preset value each time an event comes in. Clearing the TE bit will disable the timer. The decrement register will be preset to the value contained in bits DC7-DC0 of the control register and the count register will be loaded with the value of the preload register. However, if a direct write to the count register has happened since the last count register reload, the value written will be loaded into the count register instead of the preload value. TE is cleared by hardware $\overline{\text{RESET}}$ and software reset (RESET instruction).

7.7 TIMER RESOLUTION

Table 7-2 shows the range of timer interrupt rates (overflow interrupt using internal event, Fosc/2) that are provided by the 16-bit count register, the 16-bit preload register, and the 8-bit decrement register.

Table 7-2 Timer Range and Resolution

ICycle Time	DC7-DC0 value	Interrupt Rate (Preload = 2^{16})	Resolution (Preload=0)
33 ns (60MHz-30 MIPS)	0 255	2.162 ms 553.5 ms	33 ns 8.4 µs
51 ns (39 MHz-19.5MIPS))	0 255	3.342 ms 855.6 ms	51 ns 13.06 µs
74 ns (27 MHz-13.5MIPS)	0 255	4.85 ms 1.242 s	74 ns 18.94 µs

The overflow interrupt occurs every (PRELOAD+1)*(DC7-DC0+1) input clock cycles.

7.8 EVENT COUNTER TIMER DIAGRAMS

The figures given in this section illustrate most configurations in which the timer can be enabled, disabled, and used.

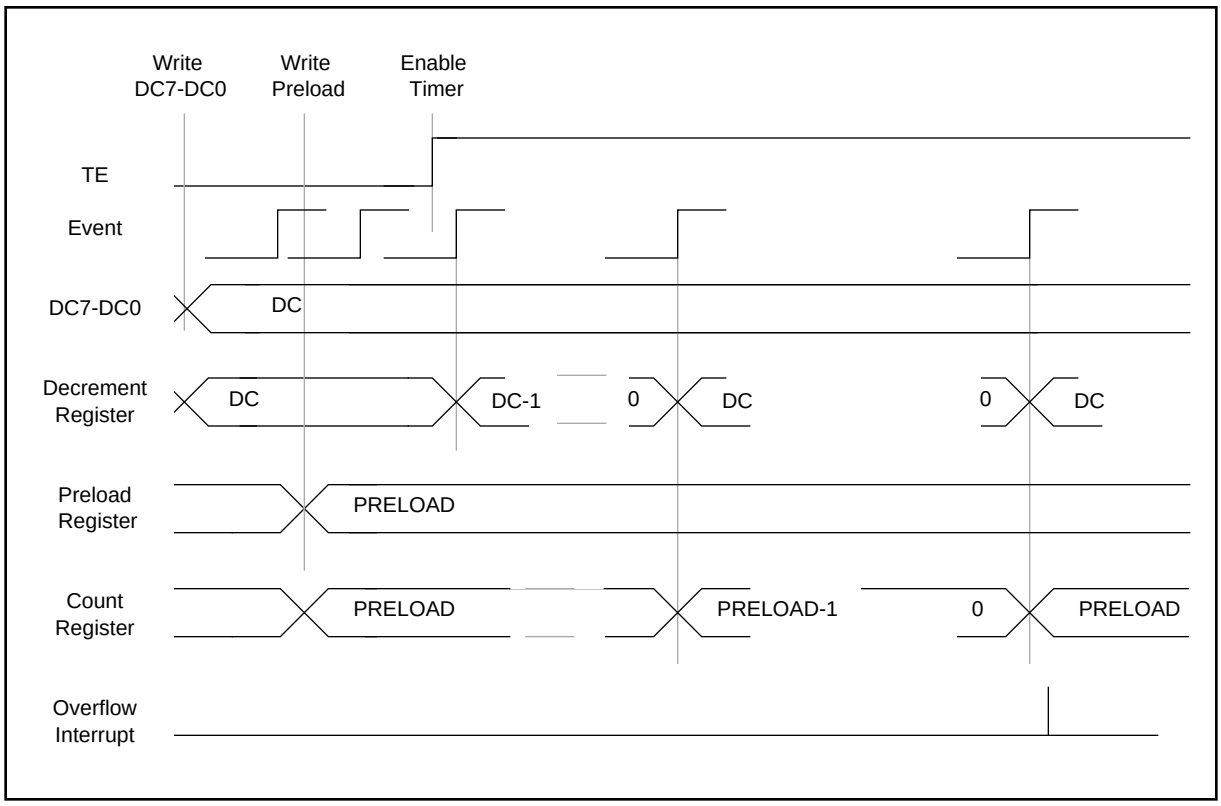


Figure 7-4 Standard Timer Operation with Overflow Interrupt

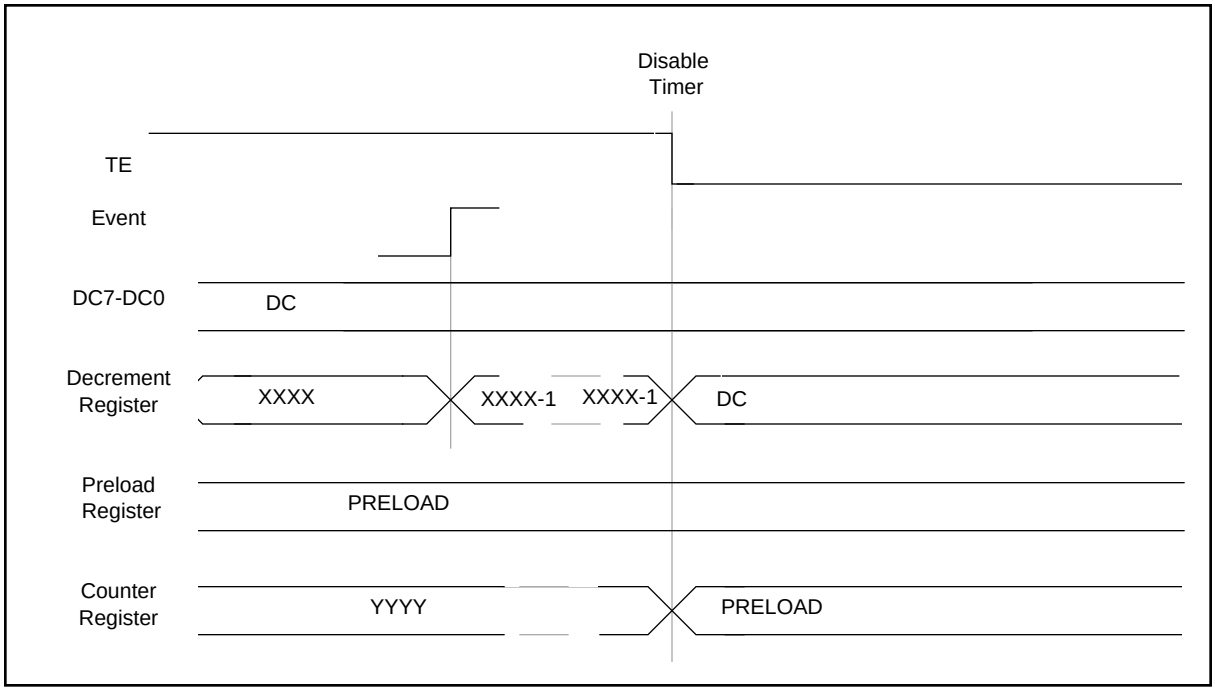


Figure 7-5 Standard Timer Disable

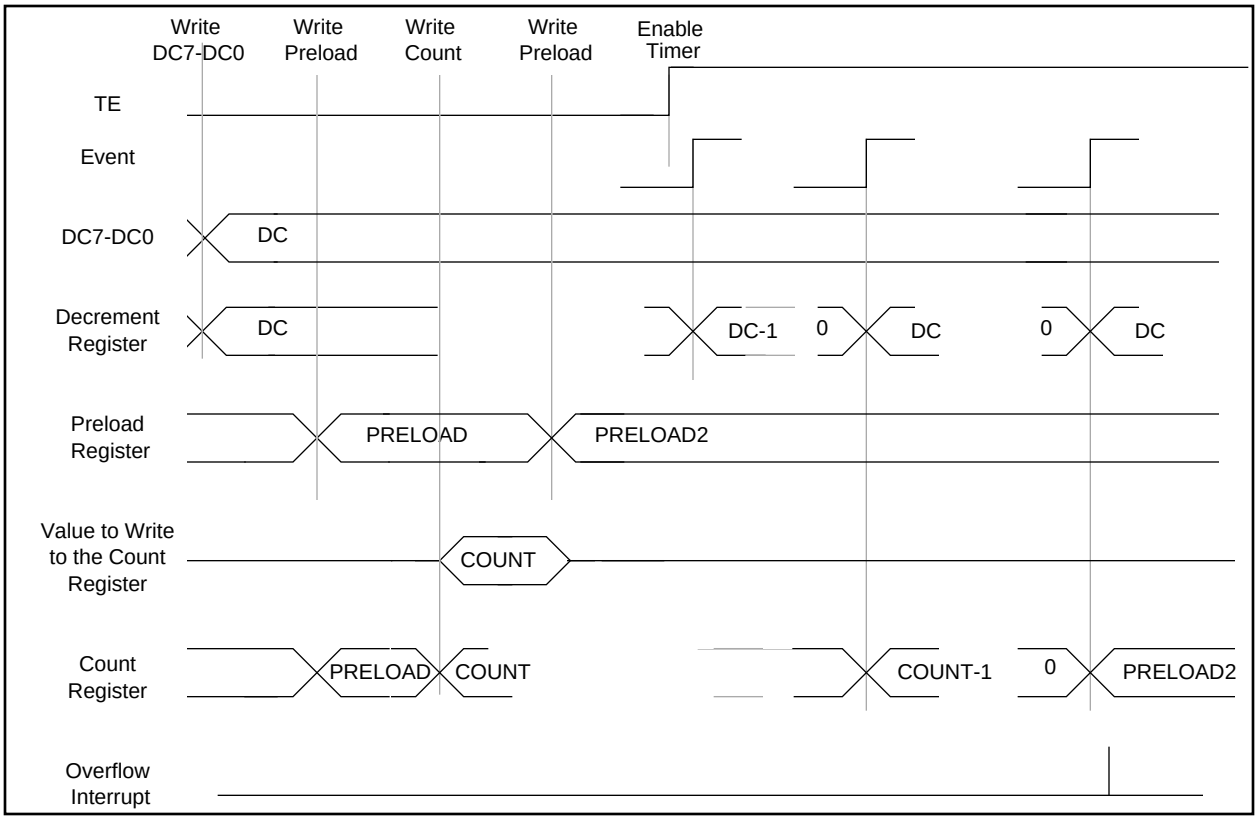


Figure 7-6
Write to the Count Register After Writing to the Preload Register When the Timer is Disabled

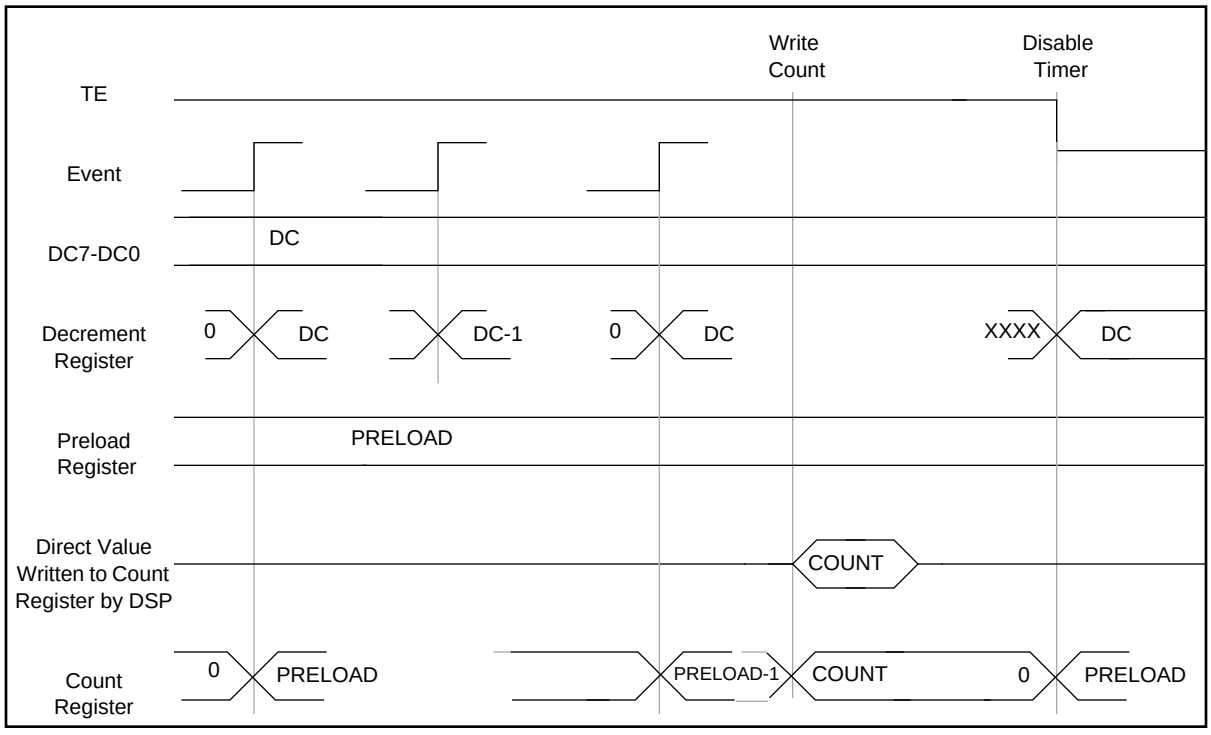


Figure 7-7 Timer Disable After a Write to the Count Register

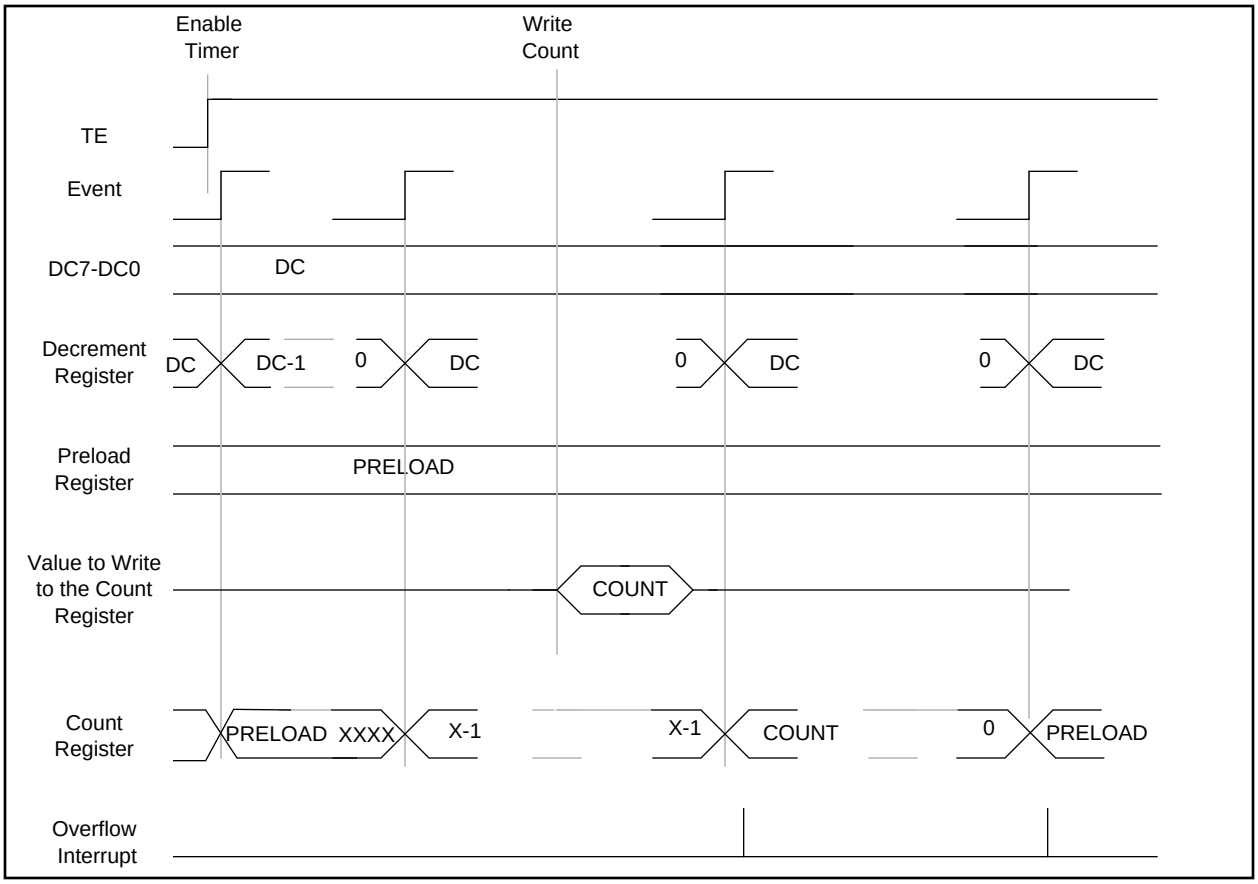


Figure 7-8 Write to the Count Register when the Timer is Enabled

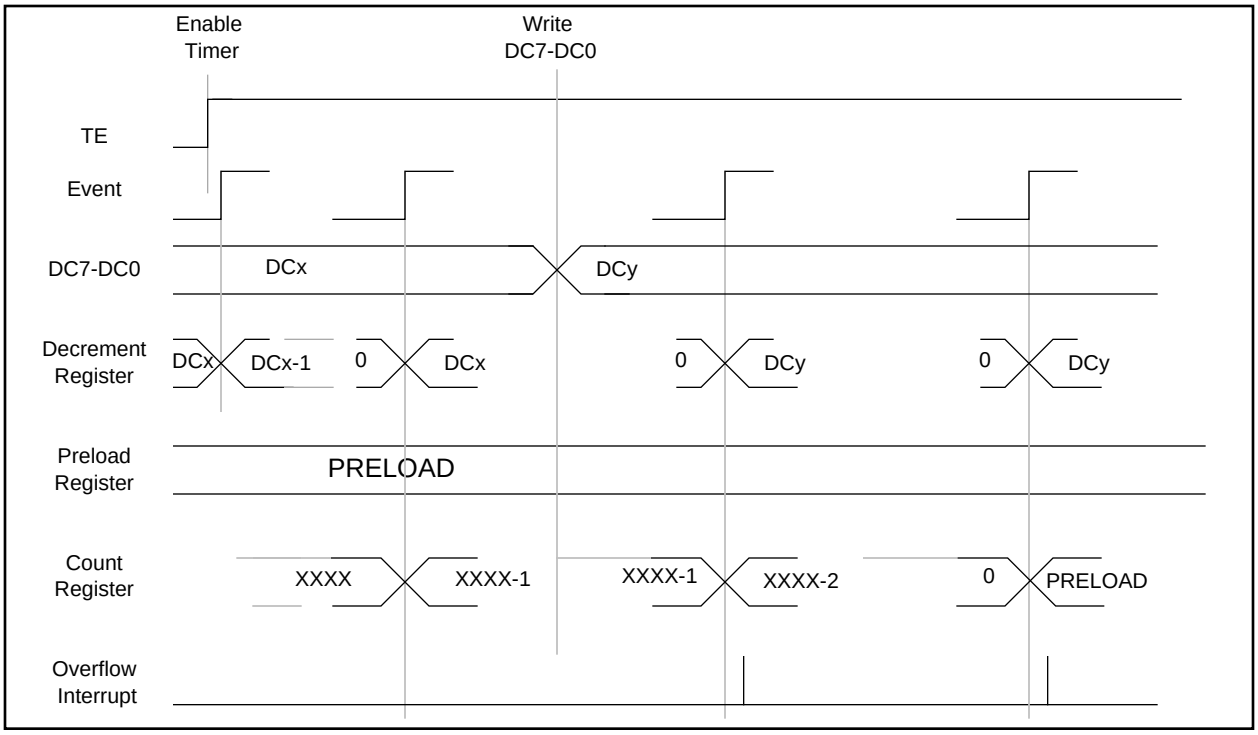


Figure 7-9 Write to DC7-DC0 when the Timer is Enabled

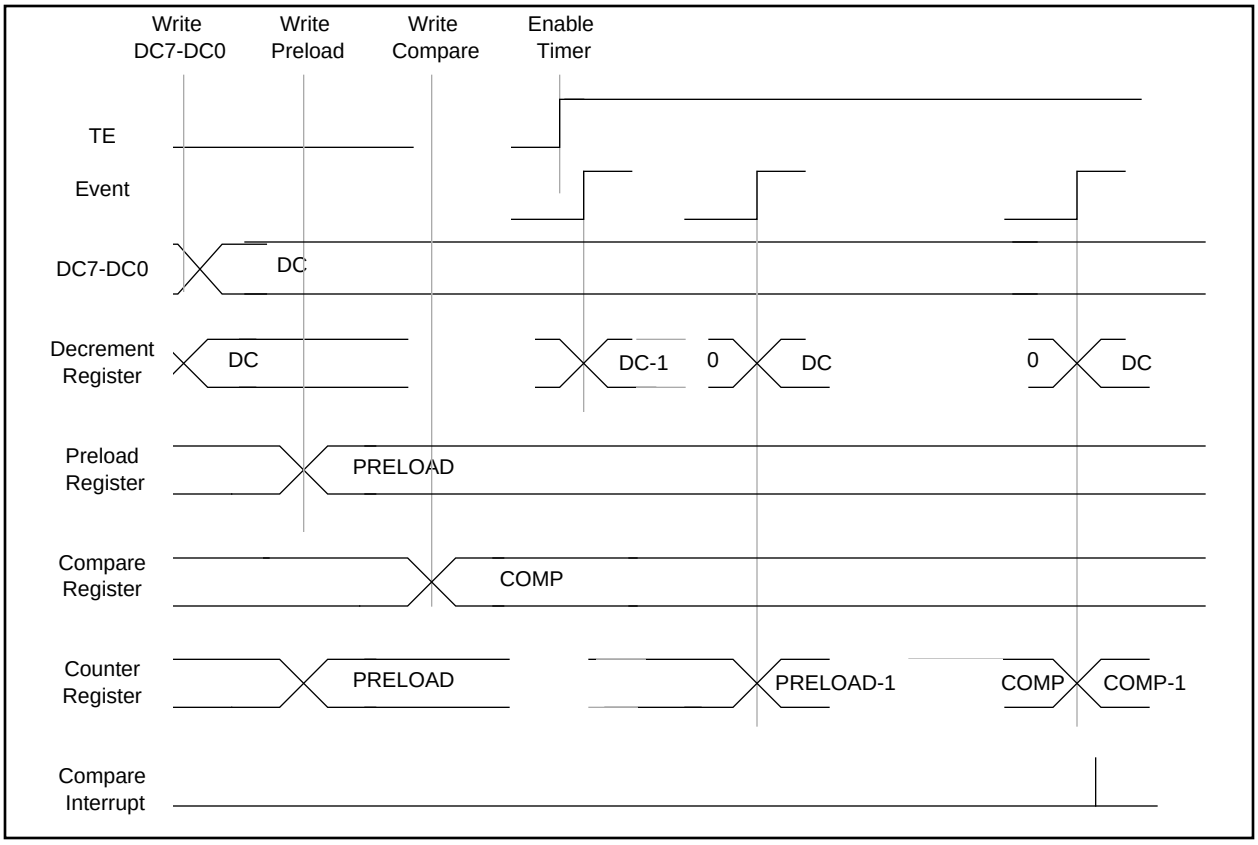


Figure 7-10 Standard Timer Operation with Compare Interrupt