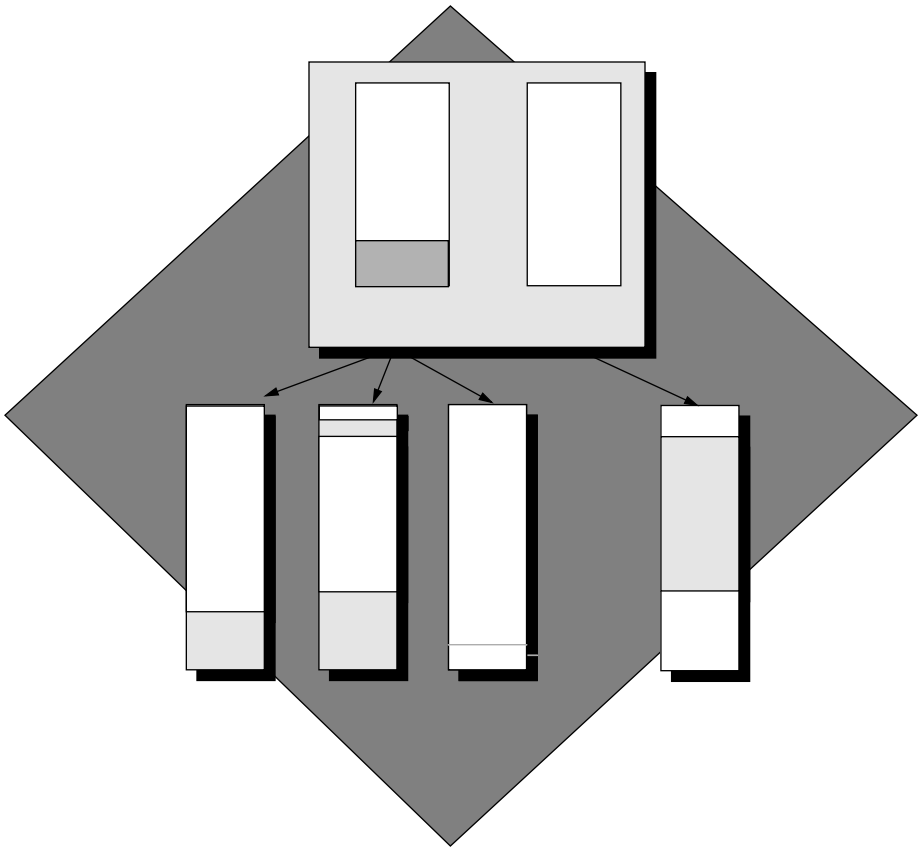
## SECTION 3

# OPERATING MODES AND MEMORY CONFIGURATION



# SECTION CONTENTS

## 3.1 INTRODUCTION

The DSP56166 is available in two different on-chip memory configurations: a RAM based part and a ROM based part. This section describes in detail the on-chip memories and the operating modes of the two versions.

## 3.2 DSP56166 RAM BASED DESCRIPTION

The RAM based DSP56166 uses **RAM** for the on-chip **Program Memory** and for the on-chip **Data Memory**. The two independent memory spaces, X data and program, are shown in Figure 3-2. The memory spaces are configured by control bits in the operating mode register (OMR). The operating mode control bits (MA and MB) in the OMR control the program memory map and select the reset vector address. Both the program and data memories can be expanded off-chip.

### 3.2.1 X Data Memory

The DSP56166 has 4096 words of on-chip data RAM: 128 data memory locations are reserved for on-chip peripheral registers (X:$FF80-FFFF) and 128 additional locations (X:$FF00-FF7F) are reserved for off-chip peripheral accesses. The external bus access time on this external peripheral space is controlled by 5 bits of an additional bus control register, BCR2, located at X:$FFDA (see Figure 3-1). Between 0 and 31 software programmable wait states can be generated. A special pin, $\overline{\text{PEREN}}$, is asserted low during accesses to the memory mapped external peripheral registers.

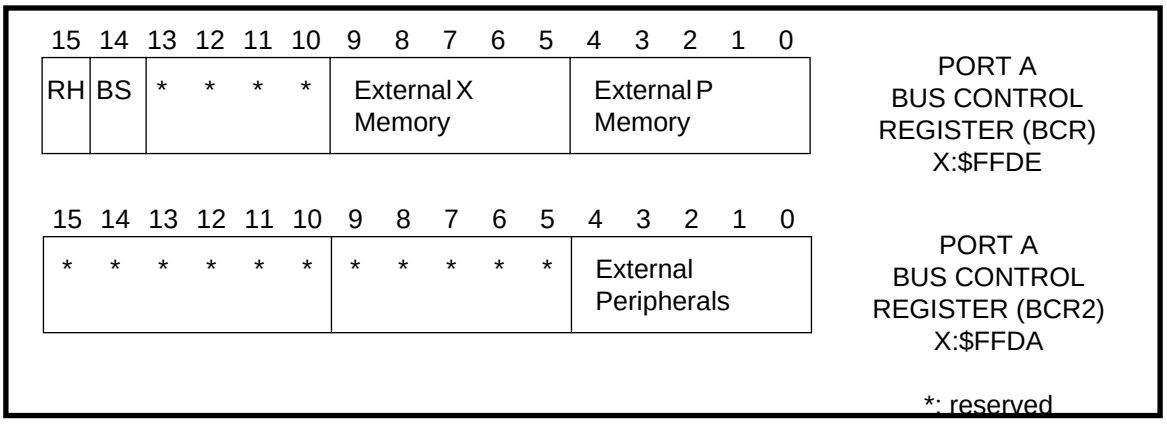



**Figure 3-1 External Peripheral Bus Control Register (BCR2)**

The X memory may be expanded off-chip for a total of 65,280 (65,536-256) addressable locations.The external data memory bus access time is controlled by 5 bits of an additional bus control register (BCR, located at X:$FFDE). This register is described in Figure 3-1.

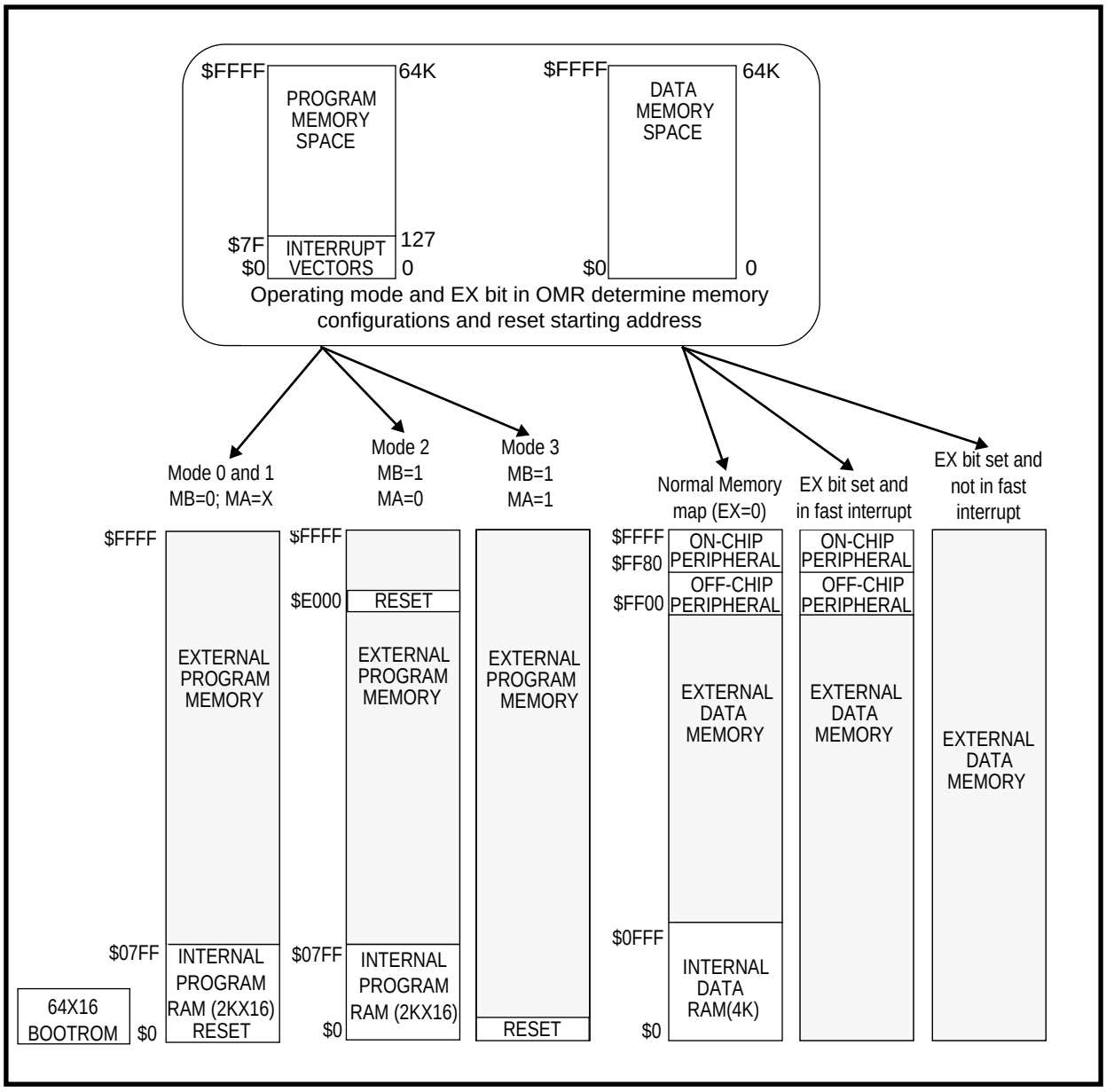



**Figure 3-2 DSP56166 RAM based Memory Map**

The External X memory bit (EXT bit 3) of the OMR determines the mapping of the X memory as shown in Figure 3-2. Setting this bit completely disables the on-chip data memory and enables the full 64 K external memory map. This bit is ignored by the fast interrupt process so that the on-chip peripheral space and off-chip peripheral space can be accessed during fast interrupts. During long interrupts, this bit, if set before the interrupt, can be cleared by the user program inside the interrupt routine in order to access the on-chip peripheral space and the on-chip memory; it can be set again before the RTI instruction.

When the EX bit is set, external data memory access is only controlled by the BCR except during fast interrupts, where BCR2 controls external accesses to the off-chip peripheral space.

### 3.2.2 Program Memory

The RAM based DSP56166 has 2048 words of on-chip program RAM. The first 128 locations of program memory are reserved for interrupt vectors. The program memory may be expanded off-chip for a total of 65,536 addressable locations.The external data memory bus access time is controlled by 5 bits of the bus control register BCR located at X:$FFDE. This register is described in Figure 3-1.

### 3.2.3 Bootstrap ROM

The Bootstrap ROM is a 64 location by 16-bit factory programmed ROM which is used only in the bootstrap modes, Operating Modes 0 and 1, during which the on-chip program RAM is defined as write-only. The bootstrap ROM is not accessible by the user and is disabled in normal operating modes. Refer to **APPENDIX A BOOTSTRAP OPERATING MODE — OPERATING MODE 0 or 1** for a full description of the bootstrap feature of the DSP56166.

The bootstrap program can load from any one of three different sources. Selection of which one of the three is made by reading the mode pins and, if necessary, bit-15 of P:$C000 from the external data bus.

If MB:MA = 00 (Mode 0) then the bootstrap program will load from an external byte-wide memory. This bootstrap program will load 4,096 bytes from the external P: memory space beginning at location P:$C000 (bits 0-7). These will be packed into 2,048 16-bit words and stored in contiguous internal program RAM memory locations starting at P:$0000. The byte-wide data will be packed into the 16-bit memory least significant byte first.

If MB:MA = 01 (Mode 1), the bootstrap program will read bit-15 of P:$C000 from the external data bus. If bit-15 = 0, the bootstrap program will load 4,096 bytes through the host port (the host processor can terminate down-loading early by setting HF0=0). If bit-15 = 1, the bootstrap program will load through RSSI0. Data is packed into program RAM least significant byte of P:$0000 first.

### 3.2.4 RAM Based DSP56166 Operating Modes

The DSP operating modes determine the memory maps for program and data memories and the start-up procedure when the DSP leaves the reset state. The MODA, MODB, and MODC pins are sampled as the DSP leaves the reset state and the initial operating mode of the DSP is set accordingly. After the reset state is exited, the MODA and MODB pins become general-purpose interrupt pins, $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$. One of three initial operating modes is selected: single chip, normal expanded, or development. chip operating modes

**Table 3-1 Operating Mode Summary**
**Program RAM Part**

| Operating Mode | MB | MA | Description |
|---|---|---|---|
| Special Bootstrap 1 | 0 | 0 | Bootstrap from an external byte-wide memory located at P:$C000. Reset at P:$0000 |
| Special Bootstrap 2 | 0 | 1 | Bootstrap from the Host port (P:$C000 bit 15=0) or RSSI0 (P:$C000 bit 15=0) Reset at P:$0000 |
| Normal Expanded | 1 | 0 | Internal PRAM enabled; External reset at P:$E000 |
| Development Expanded | 1 | 1 | Internal program memory disabled; External reset at P:$0000. |

can be changed by writing the operating mode bits (MB, MA) in the OMR. Changing operating modes does not reset the DSP. It is desirable to disable interrupts immediately before changing the OMR to prevent an interrupt from going to the wrong memory location. Also, one no-operation (NOP) instruction should be included after changing the OMR to allow for remapping to occur.

#### 3.2.4.1 Bootstrap Mode (Mode 0).

Mode 0 is one of two single-chip modes which have all internal program memories enabled (see Figure 3-2). This mode can be entered by either grounding both mode pins and resetting the chip or by writing to the OMR and changing the MA and MB bits. When the operating mode is first changed to Mode 0, the DSP56166 executes a bootstrap program which loads program memory from a byte wide memory located at P:$C000 (see Table 3-1). Section 3.2.5.2 describes the bootstrap operation. The memory maps for Mode 0 and Mode 1 are identical. The only difference between the two modes is the location of the reset vector in program memory. The reset vector location in Mode 0 is P:$0000. The reset vector location in Mode 2 is P:$E000 (external memory).

#### 3.2.4.2 Bootstrap Mode (Mode 1).

Mode 1 is one of two single-chip modes which have all internal program and data RAM memories enabled (see Figure 3-2). This mode can be entered by either grounding the MB pin and pulling the MA pin high or by writing to the OMR and changing the MA and MB bits (see Table 3-1). When the operating mode is first changed to Mode 1, the DSP56166 executes a bootstrap program which loads program memory from either the

host port or the RSSI0 depending on whether bit 15 of location P:C000 is a zero (host port) or a one (RSSI0). Section 3.2.5.2 describes the bootstrap operation. The memory maps for Mode 0 and Mode 1 are identical. The memory maps for Mode 1 and Mode 2 are very similar. The memory map difference between Mode 0 and Mode 2 is the location of the reset vector in program memory. The reset vector location in Mode 0 is P:$0000. The reset vector location in Mode 2 is P:$E000.

#### 3.2.4.3 Normal Expanded Mode (Mode 2).

The normal expanded mode (Mode 2) has the same memory map as Mode 0 and Mode 1 (see Figure 3-2). The difference is that entering Mode 2 does not cause the bootstrap program to be executed and the reset vectors to external program memory location P:$C000. This mode can be entered by either grounding the MA pin and pulling the MB pin high or by writing to the OMR and changing the MA and MB bits (see Table 3-1).

#### 3.2.4.4 Development Mode (Mode 3).

The development mode is similar to the normal expanded mode except that internal program memory is disabled (see Figure 3-2). All references to program memory space are directed to external program memory, which is accessed on the external data bus. This mode can be entered by either pulling the MA and MB pins high or by writing to the OMR and changing the MA and MB bits (see Table 3-1). The reset vector location in Mode3 is external program memory location P:$0000.

### 3.2.5 Bootstrap Mode

The bootstrap feature consists of a special on-chip bootstrap ROM containing a bootstrap program and a bootstrap control logic. The bootstrap feature is only available on the program RAM part. It is not available on the program ROM part. Appendix A describes the contents of the boot ROM.

#### 3.2.5.1 Bootstrap ROM

This 64-word on-chip ROM is factory programmed to perform the actual bootstrap operation from the memory expansion port (Port A), from the Host Interface, or from the Reduced Synchronous Serial Interface RSSI0. No access is provided to the bootstrap ROM other than through the bootstrap process. Control logic will disable the bootstrap ROM during normal operations.

#### 3.2.5.2 Bootstrap Control Logic

The bootstrap mode control logic is activated when the DSP is placed in one of the bootstrap modes, Mode 0 or Mode 1. The control logic maps the bootstrap ROM into program

memory space until the bootstrap program changes operating modes when the bootstrap load is completed.

When the DSP exits the reset state in Mode 0 or 1, the following actions occur:

1. The control logic maps the bootstrap ROM into the internal DSP program memory space starting at location P:$0000. All program fetches during the bootstrap operation are from the bootstrap ROM.
2. The control logic forces the entire internal program RAM space to be write-only memory during the bootstrap loading process. All write operations during the bootstrap program execution are to the PRAM.
3. Program execution begins at location $0000 in the bootstrap ROM. The bootstrap ROM program performs the load of the internal program RAM (PRAM) through either the memory expansion port from a byte-wide external memory, through the Host Interface, or through the Reduced Synchronous Serial Interface RSSI0.
4. Upon completing the program RAM load, the bootstrap program terminates the bootstrap operation by entering Operating Mode 2 (writing to the OMR) and by branching to the internal program RAM location P:$0000. During the execution of the branch to P:$0000, the bootstrap ROM is disabled and fetches from the PRAM are re-enabled.

The bootstrap mode may also be selected by setting the OMR bits for Operating Mode 0 or 1. This initiates a timed operation to map the bootstrap ROM into the program address space after a delay to allow execution of a single instruction and a jump to P:$0000 to start executing the bootstrap program. This technique allows the user to reboot the internal PRAM (with a different program if desired).

#### 3.2.5.3 Bootstrap Program

The bootstrap ROM contains the bootstrap firmware program that performs initial loading of the DSP's internal program RAM (see Appendix A for a listing of the bootstrap code). The program is written in DSP5616 core assembly language. It contains three separate methods of initializing the PRAM: loading from a byte-wide memory starting at location P:$C000, loading through the Host Interface, or loading through the Reduced Synchronous Serial Interface RSSI0.

When Mode 0 is selected, the external bus version of the bootstrap is executed. The data contents of the external byte-wide memory must be organized as shown in Table 3-2.

**Table 3-2 Data Mapping for External Bus Bootstrap**

| Address of External Byte-wide Memory | Contents Loaded to Internal PRAM at: |
|---|---|
| P:$C000 | P:$0000 low byte |
| P:$C001 | P:$0000 high byte |
| * | * |
| * | * |
| P:$CFFE | P:$07FF low byte |
| P:$CFFF | P:$07FF high byte |

When Mode 1 is selected, the bootstrap is performed through the Host port or the RSSI0 depending on the level of the most significant bit of P:$C000.

If Bit 15 of P:$C000 is zero (a pull-down resistor can be used in some applications), the host port bootstrap is selected. Typically a host processor will be connected to the 16-bit DSP Host Interface and a host microprocessor will write the Host Interface registers TXH and TXL with the desired contents of PRAM from locations P:$0000 to P:$07FF. If less than 2048 words are to be loaded into the PRAM, the host programmer can terminate the bootstrap process by setting HF0=1 in the Host Interface.

If bit 15 of P:$C000 is set (a pull-up resistor can be used in some applications), the bootstrap is performed through the Reduced Synchronous Serial Interface RSSI0. The bootstrap program sets up the RSSI0 in 8 bit mode, external clock, and synchronous mode.

## 3.3 DSP56166 ROM BASED DESCRIPTION

The RAM DSP56166 uses **a combination of RAM and ROM** for the on-chip **Program Memory** and for the on-chip **Data Memory**. The two independent memory spaces, X data, and program, are shown in Figure 3-3. The memory spaces are configured by control bits in the operating mode register (OMR). The operating mode control bits (MA and MB) in the OMR control the program memory map and select the reset vector address. Both the program and data memories can be expanded off-chip.

### 3.3.1 X Data Memory

DSP56166 has 4096 words of on-chip data RAM and 4096 words of on-chip data ROM. 128 data memory locations are reserved for on-chip peripheral registers (X:$FF80-FFFF) and 128 additional locations (X:$FF00-FF7F) are reserved for off-chip peripheral accesses. The external bus access time on this external peripheral space is controlled by 5 bits of an additional bus control register BCR2 located at X:$FFDA. This register is described in Figure 3-1. Between 0 and 31 software programmable wait states can be generated. A special pin, $\overline{\text{PEREN}}$, is asserted low during accesses to the memory mapped external peripheral registers. The X memory may be expanded off-chip for a total of 65,280 (65,536-256) addressable locations.

The External X memory bit (EXT bit-3) of the OMR determines the mapping of the X memory as shown on Figure 3-3. Setting this bit completely disables the on-chip data memory and enables a full 64 K external memory map. This bit is ignored by the fast interrupt process so that the on-chip peripheral space and off-chip peripheral space can be accessed during fast interrupts. During long interrupts, this bit, if set before the interrupt, can be cleared by the user program inside the interrupt routine in order to access the on-chip peripheral space and the on-chip memory; it can be set again before the RTI instruction.

When the EX bit is set, the external access on the data memory is controlled by the BCR only. Except during fast interrupts, where BCR2 will control external accesses to the off-chip peripheral space.

## NOTICE

**The on-chip XROM on the ROM based part is only connected to the XAB1 address bus**. Therefore, the data located in this ROM is only accessible by the **first** read during **dual** parallel read instructions.

During development using the **RAM** based part, the data to be mapped into the on-chip XROM of the **ROM** based part **should not** be accessed with a **second** read during a **dual** parallel read instruction.

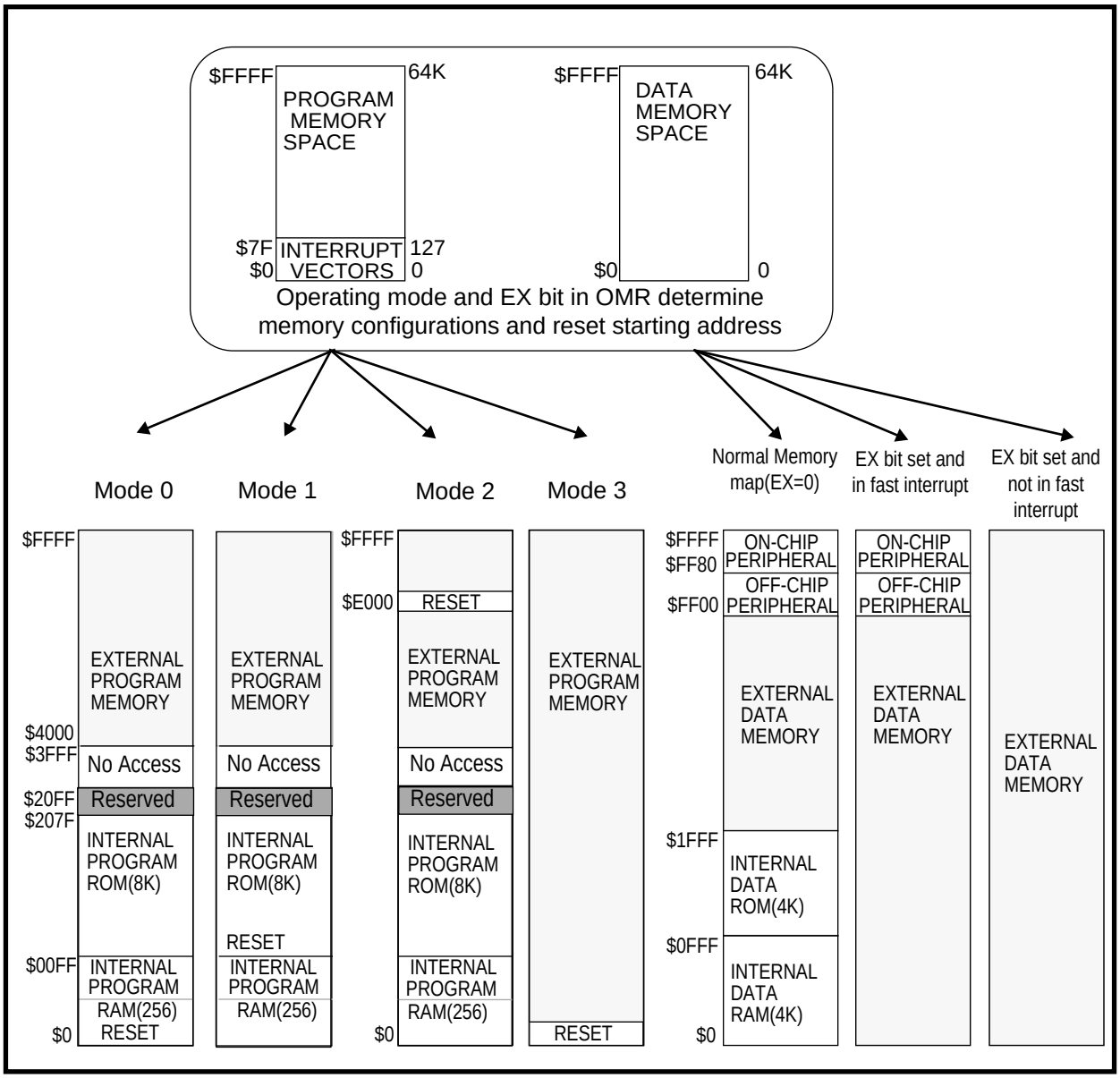



**Figure 3-3 DSP56166 ROM Based Memory Map**

### 3.3.2 Program Memory

DSP56166 has 8192 words of on-chip program ROM and 256 words of on-chip program RAM. Since the DSP5616 core specifies on-chip program memory by blocks of power of two words, there is a non-accessible hole in the program memory between addresses P:$20FF and P:$3FFF (P:8447-P:16383).

External program memory will start at location P:$4000 (P:16384) for mode 0,1 and 2 like shown on Figure 3-3.

When mode 3 is selected, the complete 64 K words of program memory are external.

**Note:** The last 128 locations of the on-chip program ROM are reserved and are not available for use (P:$2080-$20FF).

### 3.3.3 ROM Based DSP56166 Operating Modes

The DSP operating modes determine the memory maps for program and data memories and the start-up procedure when the DSP leaves the reset state. The MODA, MODB, and MODC pins are sampled as the DSP leaves the reset state and the initial operating mode of the DSP is set accordingly. After the reset state is exited, the MODA and MODB pins become general-purpose interrupt pins, $\overline{\text{IRQA}}$, and $\overline{\text{IRQB}}$. One of three initial operating modes is selected: single chip, normal expanded, or development. Chip operating modes can be changed by writing the operating mode bits (MB, MA) in the OMR. Changing operating modes does not reset the DSP. It is desirable to disable interrupts immediately before changing the OMR to prevent an interrupt from going to the wrong memory location. Also, one no-operation (NOP) instruction should be included after changing the OMR to allow for remapping to occur.

**Note:** Since the on-chip X data ROM is connected to the XAB1 address bus, the data located in this ROM is only accessible by the **first** read during **dual** parallel read instructions.

**Table 3-3 DSP56166 ROM Based Operating Modes**

| MB | MA | Chip Operating Mode | Reset Vector | Program Memory Configuration |
|---|---|---|---|---|
| 0 | 0 | Single Chip | Internal PRAM P:$0 | Internal Pmem Enabled |
| 0 | 1 | Single Chip | Internal PROM P:$100 | Internal Pmem Enabled |
| 1 | 0 | Normal Expanded | External Pmem P:$E000 | Internal Pmem Enabled |
| 1 | 1 | Development | External Pmem P:$0 | Internal Pmem Disabled |

#### 3.3.3.1 Single-chip Mode (Mode 0).

Mode 0 is one of two single-chip modes which have all internal program and data memories enabled (see Figure 3-3). This mode can be entered by either grounding both mode pins before resetting the chip or by writing to the OMR and changing the MA and MB bits. The memory maps for Mode 0 and Mode 1 are identical. The only difference between the two modes is the location of the reset vector in program memory. The reset vector location in Mode 0 is P:$0000 in the internal PRAM; whereas, the reset vector location in Mode 1 is P:$100 in the internal PROM.

#### 3.3.3.2 Single-chip Mode (Mode 1).

Mode 1 is one of two single-chip modes which have all internal program and data memories enabled (see Figure 3-3). This mode can be entered by either grounding the MB pin and pulling the MA pin high before resetting the chip, or by writing to the OMR and chang-

ing the MA and MB bits. The memory maps for Mode 0 and 1 are identical. The only difference between these two modes is the reset vector location in program memory. The reset vector location in Mode 0 is P:$0000 in internal PRAM; whereas, the reset vector location in Mode 1 is P:$100 in internal PROM.

#### 3.3.3.3 Normal Expanded Mode (Mode 2).

The normal expanded mode (Mode 2) can be entered by either pulling the MB pin high and grounding the MA pin before resetting the chip, or by writing to the OMR and changing the MA and MB bits. The memory maps for Mode 0,1, and 2 are identical. The only difference between the three modes is the location of the reset vector in program memory. The reset vector location in Mode 2 is located in the external program memory space at location P:$E000.

#### 3.3.3.4 Development Mode (Mode 3).

The development mode is similar to the normal expanded mode except that internal program memory is disabled (see Figure 3-3). All references to program memory space are directed to external program memory, which is accessed on the external data bus. This mode can be entered by either pulling the MA and MB pins high or by writing to the OMR and changing the MA and MB bits (see Table 3-3). DSP56166 ROM based chips with bad or obsolete internal program ROM code can be used with external program memory in the development mode. Reset vectors to external program memory location P:$0000.