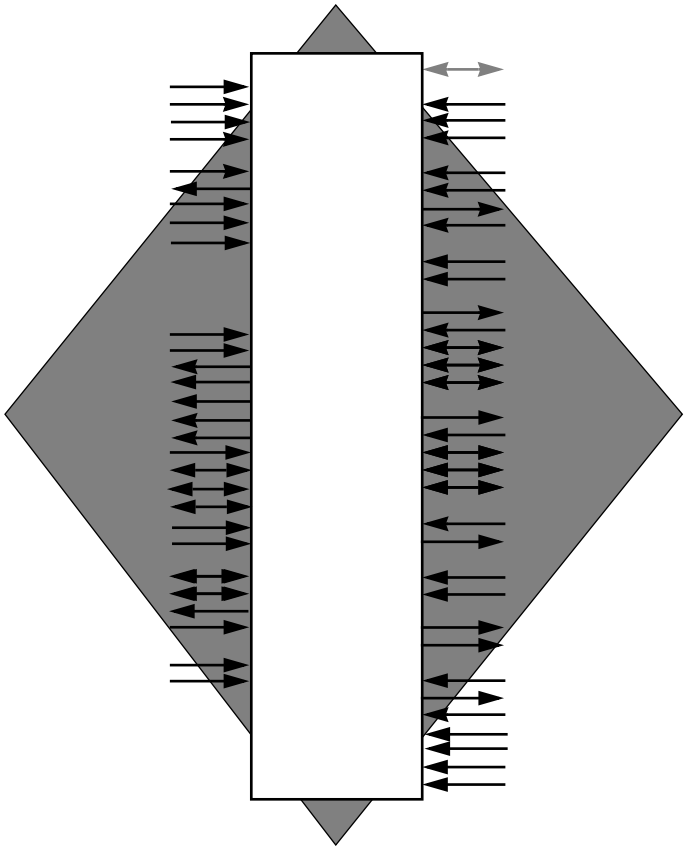
SECTION 2

DSP56166 PIN DESCRIPTIONS



SECTION CONTENTS

2.1 INTRODUCTION

The DSP56166 pinout is shown in Figure 2-1. The input and output signals on the chip are organized into the 13 functional groups shown in Table 2-1. Figure 2-2 illustrates the relative timing for the bus signals. See the timing descriptions in the technical data sheet for more information.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins
Address and Data Buses	32
Bus Control	10
Interrupt and Mode Control	4
Clock and PLL	3
Host Interface or PIO	15
Timer Interface or PIO	2
SSI Interfaces or PIO	8
On-chip CODEC	7
On-chip emulation (OnCE)	4
Power (Vdd)	10
Ground (Vss)	15
APower (Vdda)	1
AGround (Vssa)	1
Total	112

2.2 ADDRESS AND DATA BUS (32 PINS)

A0-A15 (Address Bus) — three state, active high outputs. A0-A15 change in t0, and specify the address for external program and data memory accesses. If there is no external bus activity, A0-A15 remain at their previous values. A0-A15 are three-stated during hardware reset.

D0-D15 (Data Bus) — three state, active high, bidirectional input/outputs. Read data is sampled in by the trailing edge of t2, while write data output is enabled by the leading edge of t2 and three-stated at the leading edge of t0. If there is no external bus activity, D0-D15 are three-stated. D0-D15 are also three-stated during hardware reset.

2.3 BUS CONTROL (10 PINS)

PS/$\overline{\text{DS}}$ (Program/Data Memory Select) — three state active low output. This output is asserted only when external data memory is referenced. PS/$\overline{\text{DS}}$ timing is the same as the A0-A15 address lines. PS/$\overline{\text{DS}}$ is high for program memory access and is low for data memory access. If the external bus is not used during an instruction cycle (t0, t1, t2, t3), PS/$\overline{\text{DS}}$ goes high in t0. PS/$\overline{\text{DS}}$ is in the high impedance state during hardware reset.

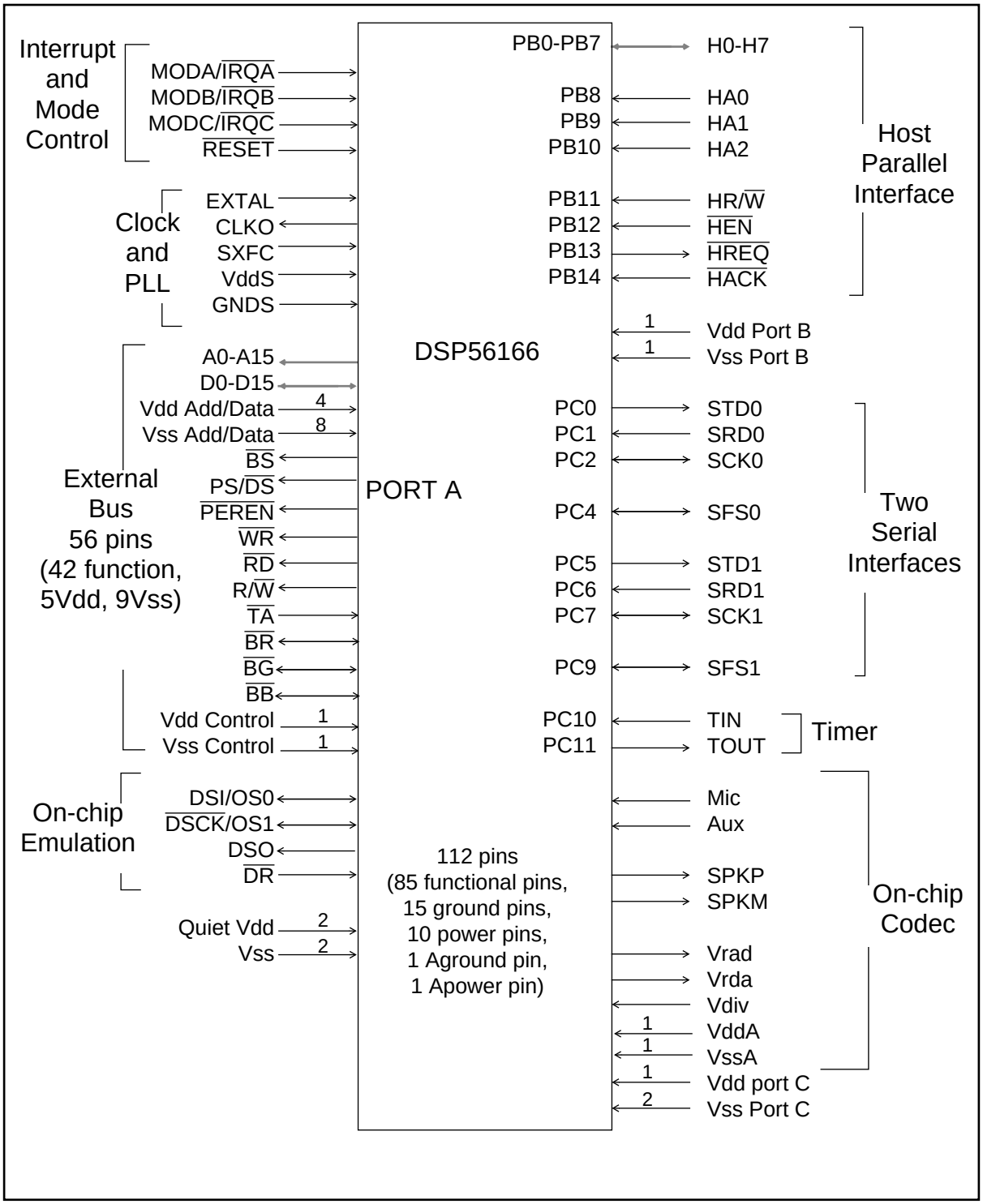


Figure 2-1. DSP56166 Pinout

$\overline{\text{PEREN}}$ **(Peripheral Enable) — three state active low output.** This output is asserted only when external peripheral space of the data memory is referenced (any address between X:$FF00 and X:$FF7F). $\overline{\text{PEREN}}$ timing is the same as the A0-A15 address lines; it is asserted and deasserted during t0. $\overline{\text{PEREN}}$ is high for any program memory access and for data memory access not in the space X:$FF00 - X:$FF7F. $\overline{\text{PEREN}}$ is in the high impedance state during hardware reset.

R/$\overline{\text{W}}$ **(Read/Write) — three state, active low output.** Timing is the same as the address lines, providing an “early write” signal. R/$\overline{\text{W}}$ (which changes to t0) is high for a read access and is low for a write access. If the external bus is not used during an instruction cycle (t0, t1, t2, and t3), R/$\overline{\text{W}}$ goes high in t0. R/$\overline{\text{W}}$ is three-stated during hardware reset.

$\overline{\text{WR}}$ **(Write Enable) — three state, active low output.** This output is asserted during external memory write cycles. When $\overline{\text{WR}}$ is asserted low in t1, the data bus pins D0-D15 become outputs and the DSP puts data on the bus during the leading edge of t2. When $\overline{\text{WR}}$ is deasserted high in t3, the external data has been latched inside the external device. When $\overline{\text{WR}}$ is asserted, it qualifies the A0-A15, PS/$\overline{\text{DS}}$ pins. $\overline{\text{WR}}$ is three-stated during hardware reset or when the DSP is not bus master. $\overline{\text{WR}}$ can be connected directly to the $\overline{\text{WE}}$ pin of a static RAM.

$\overline{\text{RD}}$ **(Read Enable) — three state, active low output.** This output is asserted during external memory read cycles. When $\overline{\text{RD}}$ is asserted low late t0/early t1, the data bus pins D0-D15 become inputs and an external device is enabled onto the data bus. When $\overline{\text{RD}}$ is deasserted high in t3, the external data has been latched inside the DSP. When $\overline{\text{RD}}$ is asserted, it qualifies the A0-A15 and PS/$\overline{\text{DS}}$ pins. $\overline{\text{RD}}$ is three-stated during hardware reset or when the DSP is not bus master. $\overline{\text{RD}}$ can be connected directly to the $\overline{\text{OE}}$ pin of a static RAM or ROM

$\overline{\text{BS}}$ **(Bus Strobe) — active low output.** This output is asserted low at the start of a bus cycle (during t0) and deasserted high at the end of the bus cycle (during t2). This pin provides an “early bus start” signal which can be used as an address latch and as an “early bus end” signal which can be used by an external bus controller. $\overline{\text{BS}}$ is three-stated during hardware reset.

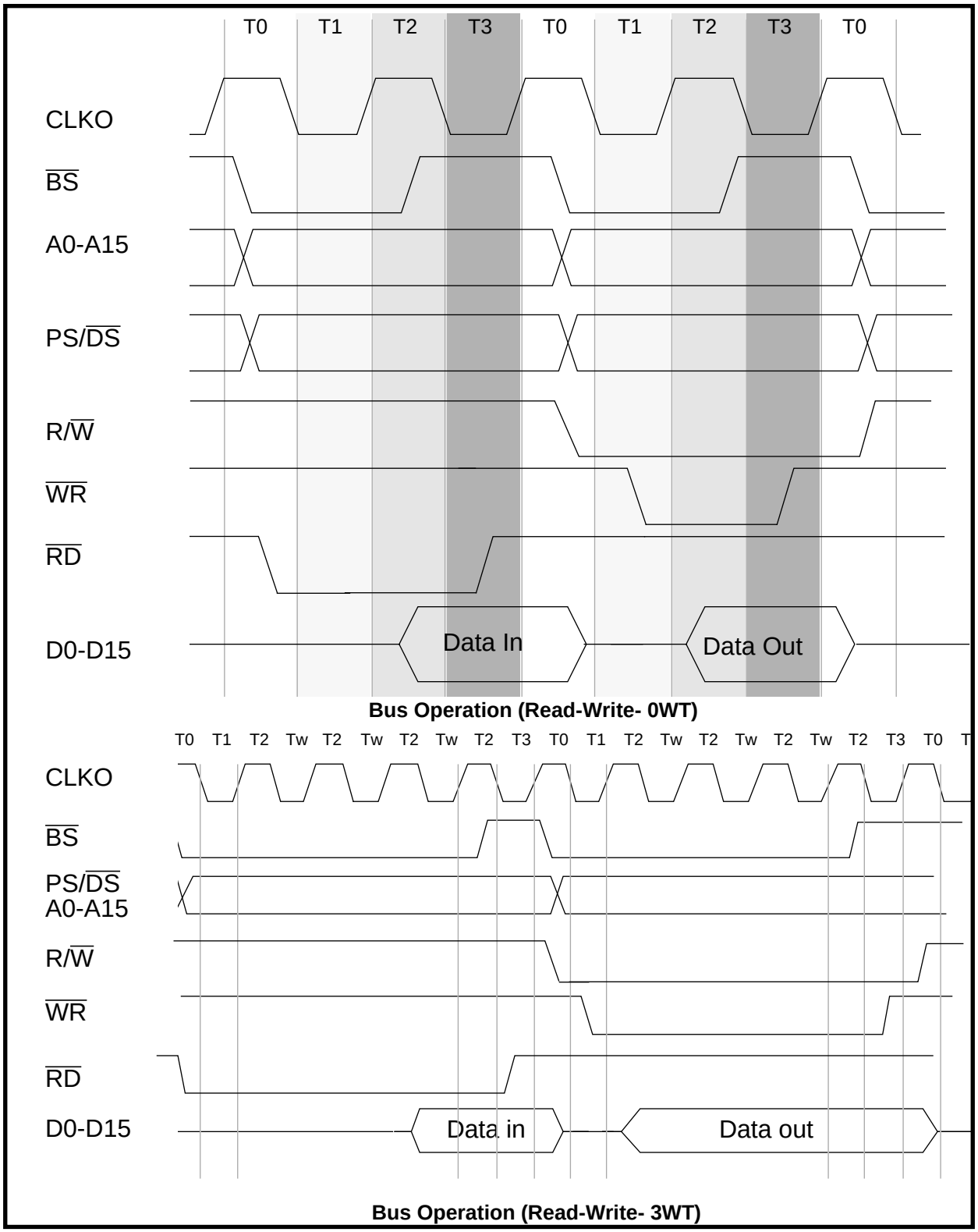


Figure 2-2 Bus Operations

$\overline{\text{TA}}$ **(Transfer Acknowledge) — active low input.** If there is no external bus activity, the $\overline{\text{TA}}$ input is ignored by the DSP. When there is external bus cycle activity, $\overline{\text{TA}}$ can be used to insert wait states in the external bus cycle. $\overline{\text{TA}}$ is sampled on the leading edge of the clock. Any number of wait states from 1 to infinity may be inserted by using $\overline{\text{TA}}$. If $\overline{\text{TA}}$ is sampled high on the leading edge of the clock beginning the bus cycle, the bus cycle will end 2T after $\overline{\text{TA}}$ has been sampled low on a leading edge of the clock; if the Bus Control Register (BCR) value does not program more wait states. The number of wait states is determined by the $\overline{\text{TA}}$ input or by the BCR, whichever is longer. $\overline{\text{TA}}$ is still sampled during the leading edge of the clock when wait states are controlled by the BCR value. In that case, $\overline{\text{TA}}$ will have to be sampled low during the leading edge of the last period of the bus cycle programmed by the BCR (2T before the end of the bus cycle programmed by the BCR) in order not to add any wait states. $\overline{\text{TA}}$ should always be deasserted high during t3 to be sampled high by the leading edge of t0. If $\overline{\text{TA}}$ is sampled low (asserted) at the leading edge of the t0 beginning the bus cycle, and if no wait states are specified in the BCR register, zero wait states will be inserted in the external bus cycle regardless the status of $\overline{\text{TA}}$ during the leading edge of t2.

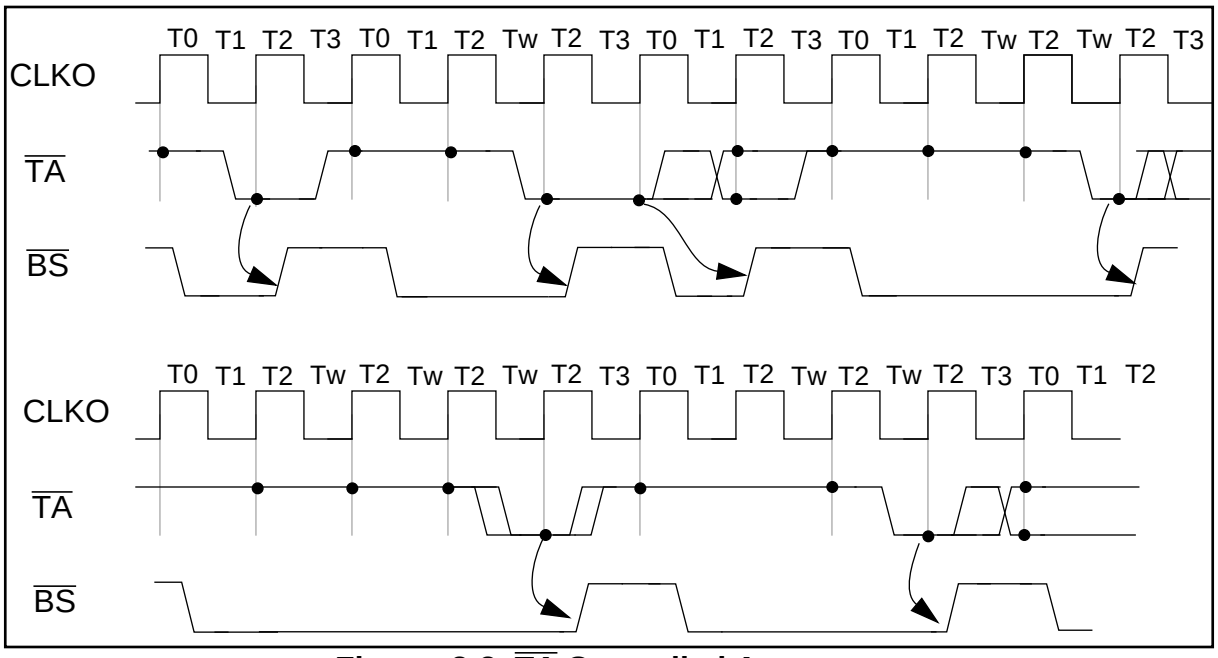


Figure 2-3 $\overline{\text{TA}}$ Controlled Accesses

$\overline{\text{BR}}$ **(Bus Request) — active low output when in the master mode, active low input when in the slave mode**. After power-on reset, this pin is an input (slave mode). In this mode, $\overline{\text{BR}}$ allows another device such as a processor or DMA

controller to become master of the DSP external data bus D0-D15 and the external address bus A0-A15. The DSP asserts $\overline{BG}$ a few T states after the $\overline{BR}$ input is asserted. The DSP bus controller will release control of the external data bus D0-D15, address bus A0-A15 and bus control pins $\overline{PEREN}$, PS/ $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, and R/$\overline{W}$ at the earliest time possible consistent with proper synchronization. These pins will then be placed in the high impedance state and the $\overline{BB}$ pin will be deasserted. The DSP will continue executing instructions only if internal program and data memory resources are being accessed. If the DSP requests the external bus while the $\overline{BR}$ input pin is asserted, the DSP bus controller inserts wait states until the external bus becomes available ($\overline{BR}$ and $\overline{BB}$ deasserted). Note that interrupts are not serviced when a DSP instruction is waiting for the bus controller. Note also that $\overline{BR}$ is prevented from interrupting the execution of a read/ modify/ write instruction.

If the master bit in the OMR register is set, this pin becomes an output (Master Mode). In this mode, the DSP is not the external bus master and has to assert $\overline{BR}$ to request the bus mastership. The DSP bus controller will insert wait states until $\overline{BG}$ input is asserted and will then begin normal bus accesses after the rising of the clock which sampled $\overline{BB}$ high. The $\overline{BR}$ output signal will remain asserted until the DSP no longer needs the bus. In this mode, the Request Hold bit (RH) of the BCR allows $\overline{BR}$ to be asserted under software control.

During external accesses caused by an instruction executed out of external program memory, $\overline{BR}$ remains asserted low for consecutive external X memory accesses and continues toggling for consecutive external P memory accesses unless the Request Hold bit (RH) is set inside the BCR.

In the master mode, $\overline{BR}$ can also be used for non arbitration purposes: if $\overline{BG}$ is always asserted, $\overline{BR}$ is asserted in t0 of every external bus access. It can then be used as a chip select to turn an external memory device off and on between internal and external bus accesses. $\overline{BR}$ timing is, in that case, similar to A0-A15, R/$\overline{W}$, and PS/$\overline{DS}$; it is asserted and deasserted during t0.

$\overline{BG}$ **(Bus Grant) — active low input when in the master mode, active low output when in the slave mode.** This pin is an output after power on reset if the slave is selected and is asserted to acknowledge an external bus request. It indicates that the DSP will release control of the external address bus A0-A15, data bus D0-D15, and bus control pins when $\overline{BB}$ is deasserted. The $\overline{BG}$ output is asserted in response to a $\overline{BR}$ input. When the $\overline{BG}$ output is asserted and $\overline{BB}$ is deasserted, the external address bus A0-A15, data bus D0-D15 and bus con-

trol pins are in the high impedance state. $\overline{BG}$ assertion may occur in the middle of an instruction which requires more than one external bus cycle for execution. Note that $\overline{BG}$ assertion will not occur during indivisible read-modify-write instructions (BFSET, BFCLR, BFCHG). When $\overline{BR}$ is deasserted and $\overline{BB}$ pin is sampled high then $\overline{BG}$ is deasserted and the DSP regains control of the external address bus, data bus, and bus control pins.

This pin becomes an input if the master bit in the OMR register is set (Master Mode). It is asserted by an external processor when the DSP may become the bus master. The DSP can start normal external memory access after the $\overline{BB}$ pin has been deasserted by the previous bus master. When $\overline{BG}$ is deasserted, the DSP will release the bus as soon as the current transfer is completed. The state of $\overline{BG}$ may be tested by testing the BS bit in the Bus Control Register.

$\overline{BG}$ is ignored during hardware reset.

$\overline{BB}$ (Bus Busy) — active low input when not a bus master, active low output when a bus master. This pin is asserted by the DSP when it becomes the bus master and it performs an external access. It is deasserted when the DSP releases bus mastership. $\overline{BB}$ becomes an input when the DSP is no longer the bus master.

2.4 INTERRUPT AND MODE CONTROL (4 PINS)

MODA/$\overline{IRQA}$ (Mode Select A/External Interrupt Request A) — This input has two functions: (1) to select the initial chip operating mode and (2), after synchronization, to allow an external device to request a DSP interrupt. MODA is read and internally latched in the DSP when the processor exits the reset state. MODA and MODB select the initial chip operating mode. Several clock cycles after leaving the reset state, the MODA pin changes to external interrupt request $\overline{IRQA}$. The chip operating mode can be changed by software after reset. The $\overline{IRQA}$ input is a synchronized external interrupt request which indicates that an external device is requesting service. It may be programmed to be level sensitive or negative edge triggered. If level sensitive triggering is selected, an external pull up resistor is required for wired-OR operation. If the processor is in the stop state and $\overline{IRQA}$ is asserted, the processor will exit the stop state.

MODB/$\overline{IRQB}$ (Mode Select B/External Interrupt Request B) — This input has two functions: (1) to select the initial chip operating mode and (2), after internal synchronization, to allow an external device to request a DSP interrupt. MODB is read and internally latched in the DSP when the processor exits the reset state.

MODA and MODB select the initial chip operating mode. Several clock cycles after leaving the reset state, the MODB pin changes to external interrupt request $\overline{\text{IRQB}}$. After reset, the chip operating mode can be changed by software. The $\overline{\text{IRQB}}$ input is an external interrupt request which indicates that an external device is requesting service. It may be programmed to be level sensitive or negative edge triggered. If level sensitive triggering is selected, an external pull up resistor is required for wired-OR operation.

MODC/$\overline{\text{IRQC}}$ (Mode Select C/External Interrupt Request C) — This input has two functions: (1) to select the initial bus operating mode and (2), after internal synchronization, to allow an external device to request a DSP interrupt. MODC is read and internally latched in the DSP when the processor exits the reset state. When tied high, the external bus is programmed in the master mode ($\overline{\text{BR}}$ output and $\overline{\text{BG}}$ input) and when tied low, the bus is programmed in the slave mode ($\overline{\text{BR}}$ input and $\overline{\text{BG}}$ output). After reset, the bus operating mode can be changed by software writing the MC bit of the OMR register. Several clock cycles after leaving the reset state, the MODC pin changes to the external interrupt request $\overline{\text{IRQC}}$. The $\overline{\text{IRQC}}$ input is an external interrupt request which indicates that an external device is requesting service. It may be programmed to be level sensitive or negative edge triggered. If level sensitive triggering is selected, an external pull up resistor is required for wired-OR operation.

$\overline{\text{RESET}}$ (Reset) — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the DSP is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the MODA and MODB pins. The internal reset signal should be deasserted synchronous with the internal clocks.

2.5 POWER, GROUND, AND CLOCK (30 PINS)

VCC (8) (Power) — power pins.

VSS (15) (Ground) — ground pins.

VDDS (Synthesizer Power) — This pin supplies a quiet power source to the VCO to provide greater frequency stability.

GNDS (Synthesizer Ground) — This pin supplies a quiet ground to the VCO to provide greater frequency stability.

EXTAL (External Clock/Crystal Input) — This input should be connected to an external clock or to an external oscillator. After being squared, the input clock can be

selected to directly provide the clock to the DSP core. In that case, it is divided by two into the core to produce a four phase instruction cycle clock, the minimum instruction time being two input clock periods.This input clock can also be selected as input clock for the on-chip codec and the on-chip PLL.

CLKO **(Clock Output)** — This pin outputs a buffered clock signal. By programming two bits (CS1-CS0) inside the PLL control register PLCR, the user can select between outputting a squared version of the signal applied to EXTAL, a squared version of the signal applied to EXTAL divided by 2, and a delayed version of the DSP core master clock. The clock frequency on this pin can be disabled by setting the Clockout Disable bit (CD; bit 7) of the Operating Mode Register (OMR).

SXFC **(External Filter Capacitor)** — This pin is used to add an external capacitor to the filter circuit of the phase locked loop. The capacitor should be connected between SXFC and VDDS.

VDDA **(Power Supply Input)** — This pin is the positive analog supply input. It should be connected to Vdd when the codec is not used.

VSSA **(Analog Ground)** — This pin is the analog ground return. It should be connected to Vss when the codec is not used.

2.6 HOST INTERFACE (15 PINS)

H0-H7 **(Host Data Bus)** — This bidirectional data bus is used to transfer data between the host processor and the DSP. This bus is an input unless enabled by a host processor read. H0-H7 may be programmed as general purpose parallel I/O pins called PB0-PB7 when the Host Interface (HI) is not being used.

HA0-2 **(Host Address 0-2)** — These inputs provide the address selection for each HI register and are stable when $\overline{\text{HEN}}$ is asserted. HA0-HA2 may be programmed as general purpose I/O pins called PB8-PB10 when the HI is not being used.

HR/$\overline{\text{W}}$ **(Host Read/Write)** — This input selects the direction of data transfer for each host processor access. If HR/$\overline{\text{W}}$ is high and $\overline{\text{HEN}}$ is asserted, H0-H7 are outputs and DSP data is transferred to the host processor. If HR/$\overline{\text{W}}$ is low and $\overline{\text{HEN}}$ is asserted, H0-H7 are inputs and host data is transferred to the DSP. HR/$\overline{\text{W}}$ is stable when $\overline{\text{HEN}}$ is asserted. HR/$\overline{\text{W}}$ may be programmed as a general purpose I/O pin called PB11 when the HI is not being used.

$\overline{\text{HEN}}$ **(Host Enable)** — This input enables a data transfer on the host data bus. When $\overline{\text{HEN}}$ is asserted and HR/$\overline{\text{W}}$ is high, H0-H7 becomes an output and DSP data

may be latched by the host processor. When $\overline{\text{HEN}}$ is asserted and HR/$\overline{\text{W}}$ is low, H0-H7 is an input and host data is latched inside the DSP when $\overline{\text{HEN}}$ is deasserted. Normally a chip select signal derived from host address decoding and an enable clock is connected to the Host Enable. $\overline{\text{HEN}}$ may be programmed as a general purpose I/O pin called PB12 when the HI is not being used.

$\overline{\text{HREQ}}$ **(Host Request)** — This open-drain output signal is used by the HI to request service from the host processor. $\overline{\text{HREQ}}$ may be connected to an interrupt request pin of a host processor, a transfer request of a DMA controller, or a control input of external circuitry. $\overline{\text{HREQ}}$ is asserted when an enabled request occurs in the HI. $\overline{\text{HREQ}}$ is deasserted when the enabled request is cleared or masked, DMA $\overline{\text{HACK}}$ is asserted, or the DSP is reset. $\overline{\text{HREQ}}$ may be programmed as a general purpose I/O pin (not open-drain) called PB13 when the HI is not being used.

$\overline{\text{HACK}}$ **(Host Acknowledge)** — This input has two functions: (1) to provide a Host Acknowledge signal for DMA transfers or (2) to control handshaking and to provide a Host Interrupt Acknowledge compatible with MC68000 family processors. If programmed as a Host Acknowledge signal, $\overline{\text{HACK}}$ may be used as a data strobe for HI DMA data transfers. If programmed as an MC68000 Host Interrupt Acknowledge, $\overline{\text{HACK}}$ is used to enable the HI Interrupt Vector Register (IVR) onto the Host Data Bus H0-H7 if the Host Request $\overline{\text{HREQ}}$ output is asserted. In this case, all other HI control pins are ignored and the HI state is not affected. $\overline{\text{HACK}}$ may be programmed as a general purpose I/O pin called PB14 when the HI is not being used.

2.7 16-BIT TIMER (2 PINS)

TIN **(Timer Input)** — This input receives external pulses to be counted by the on-chip 16-bit timer when external clocking is selected. The pulses are internally synchronized to the DSP core internal clock. TIN may be programmed as a general purpose I/O pin called PC10 when the external event function is not being used.

TOUT **(Timer Output)** — This output generates pulses, toggles on a timer overflow event, or toggles on a compare event. TOUT may be programmed as a general purpose I/O pin called PC11 when disabled by the timer out enable bits (TO2-TO0).

2.8 REDUCED SYNCHRONOUS SERIAL INTERFACES (RSSI0 AND RSSI1) AND PORT C (8 PINS)

STD0/PC0 (RSSI0 Transmit Data) — This output pin transmits serial data from the RSSI0 Transmit Shift Register. STD0 may be programmed as a general purpose I/O pin called PC0 when the RSSI0 STD0 function is not being used.

SRD0/PC1 (RSSI0 Receive Data) — This input pin receives serial data and transfers the data to the RSSI0 Receive Shift Register. SRD0 may be programmed as a general purpose I/O pin called PC1 when the RSSI0 SRD0 function is not being used.

SCK0/PC2 (RSSI0 Serial Clock) — This bidirectional pin provides the serial bit rate clock for the RSSI0 interface. The clock signal can be continuous or gated and is used by both the transmitter and receiver. SCK0 may be programmed as a general purpose I/O pin called PC2 when the RSSI0 interface is not being used.

SFS0/PC4 (Serial Frame Sync 0) — This bidirectional pin is used by the RSSI0 serial interface as frame sync I/O or flag I/O. The SFS0 is used by both the transmitter and receiver to synchronize data transfer and can be an input or an output. SFS0 may be programmed as a general purpose I/O pin called PC4 when the RSSI0 is not using this pin.

STD1/PC5 (RSSI1 Transmit Data) — This output pin transmits serial data from the RSSI1 Transmit Shift Register. STD1 may be programmed as a general purpose I/O pin called PC5 when the RSSI1 STD1 function is not being used.

SRD1/PC6 (RSSI1 Receive Data) — This input pin receives serial data and transfers the data to the RSSI1 Receive Shift Register. SRD1 may be programmed as a general purpose I/O pin called PC6 when the RSSI1 SRD function is not being used.

SCK1/PC7 (RSSI1 Serial Clock) — This bidirectional pin provides the serial bit rate clock for the RSSI1 interface. The clock signal can be continuous or gated and is used by both the transmitter and receiver. SCK1 may be programmed as a general purpose I/O pin called PC7 when the RSSI1 interface is not being used.

SFS1/PC9 (Serial Frame Sync 1) — This bidirectional pin is used by the RSSI1 serial interface as frame sync I/O or flag I/O. The SFS1 is used by both the transmitter and receiver to synchronize data transfer and can be an input or an output.

SFS1 may be programmed as a general purpose I/O pin called PC9 when the RSSI1 is not using this pin.

2.9 ON-CHIP EMULATION (4 PINS)

DSI/OS0 (Debug Serial Input/Chip Status 0) — The DSI/OS0 pin, when an input, is the pin through which serial data or commands are provided to the OnCE controller. The data received on the DSI pin will be recognized only when the DSP has entered the debug mode of operation. Data must have valid TTL logic levels before the serial clock falling edge. Data is always shifted into the OnCE serial port most significant bit (MSB) first. When the DSP is not in the debug mode, the DSI/OS0 pin provides information about the chip status if it is an output and used in conjunction with the OS1 pin.

$\overline{\text{DSCK}}$/OS1 (Debug Serial Clock/Chip Status 1) — The $\overline{\text{DSCK}}$/OS1 pin, when an input, is the pin through which the serial clock is supplied to the OnCE. The serial clock provides pulses required to shift data into and out of the OnCE serial port. Data is clocked into the OnCE on the falling edge and is clocked out of the OnCE serial port on the rising edge. When the DSP is not in the debug mode, the $\overline{\text{DSCK}}$/OS1 pin provides information about the chip status if it is an output and used in conjunction with the OS0 pin.

DSO (Debug Serial Output) — The debug serial output provides the data contained in one of the OnCE controller registers as specified by the last command received from the command controller. When idle, this pin is high. When the requested data is available, the DSO line will be asserted (negative true logic) for four T cycles (one instruction cycle) to indicate that the serial shift register is ready to receive clocks in order to deliver the data. When the chip enters the debug mode due to an external debug request ($\overline{\text{DR}}$), an internal software debug request (DEBUG), a hardware breakpoint occurrence, or a trace/step occurrence, this line will be asserted for three T cycles to indicate that the chip has entered the debug mode and is waiting for commands. Data is always shifted out the OnCE serial port most significant bit (MSB) first.

$\overline{\text{DR}}$ (Debug Request Input) — The debug request input provides a means of entering the debug mode of operation. This pin, when asserted (negative true logic), will cause the DSP to finish the instruction being executed, enter the debug mode, and wait for commands to be entered from the debug serial input line.

2.10 ON-CHIP CODEC (7 PINS)

AUX **(Auxiliary Input)** — This pin is selected as the analog input to the A/D converter when the INS bit is set in the codec control register COCR.This pin should be left floating when the codec is not used.

MIC **(Microphone Input)** — This pin is selected as the analog input to the A/D converter when the INS bit is cleared in the codec control register COCR.This pin should be left floating when the codec is not used.

SPKP **(Speaker Positive Output)** — This pin is the positive analog output from the on-chip D/A converter.This pin should be left floating when the codec is not used.

SPKM **(Speaker Negative Output)** — This pin is the negative analog output from the on-chip D/A converter.This pin should be left floating when the codec is not used.

VRAD **(Voltage Reference Output for the A/D)** — This pin is the output of the op-amp buffer in the A/D sections reference voltage generator. It has a value of (2/5) VDDA. This voltage is used as the analog ground internal to the block.This pin should always be connected to ground through two capacitors, even when the codec is not used.

VRDA **(Voltage Reference Output for the D/A)** — This pin is the output of the op-amp buffer in the D/A sections reference voltage generator. It has a value of (2/5) VDDA. This voltage is used as the analog ground internal to the block.This pin should always be connected to the ground through two capacitors, even when the codec is not used.

VDIV **(Voltage Division Output)** — This pin is the input to the op-amp buffer in the reference voltage generator. It is connected to a resistor divider network located within the codec block which provides a voltage equal to 2/5 VDDA.This pin should be left floating when the codec is not used.