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SECURE CONNECTIONS FOR A SMARTER WORLD

Agenda

- Trends in EE architectures
- Functional safety today
- Functional safety in the robot-car era







Trends in EE Architectures





Automotive Mega-Trends



Autonomous
Accident Free



Safe Transport
Optimized Routing
Driving Comfort



Electrification
Oil-Independent



Zero Emission



Service Oriented
User Defined



Entertainment
Security
Customization



Mega Trends Force Vehicle Architecture Transformation

TODAY: FLAT

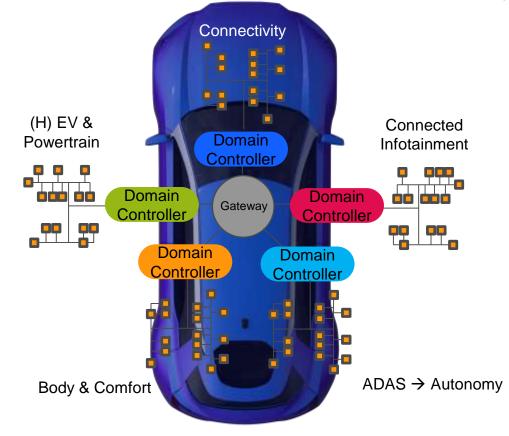


Low bandwidth, flat network One MCU per application

UNFIT FOR FUTURE MOBILITY



TOMORROW: DOMAINS

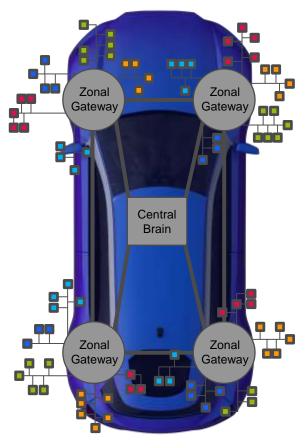


High bandwidth network
Gateway key to communication between domains

STEP TO AUTONOMOUS CAR



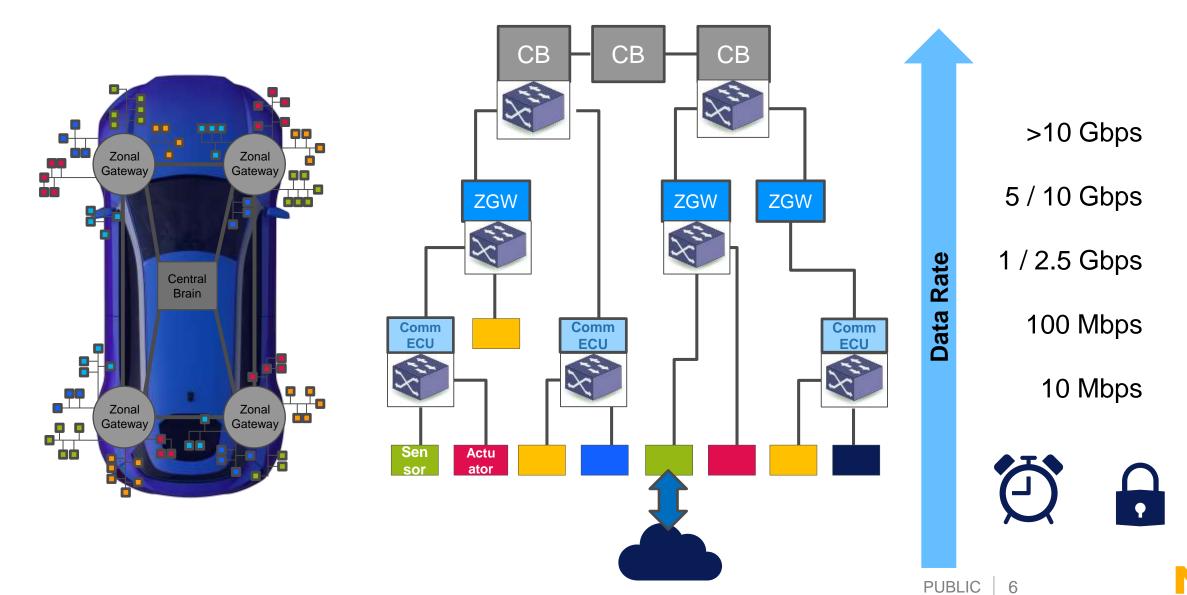
AFTER TOMORROW: ZONES



Domains virtualized by SW – enabling high flexibility Easy enable/disable or update functions



...Trend to Fully Hierarchical Ethernet Network





ISO 26262, part 1:

"absence of unreasonable risk due to hazards caused by malfunctioning behaviour of E/E systems"

ASIL A Reduce risk **ASIL B** to an ASIL C acceptable level **ASIL D**





Functional Safety Today

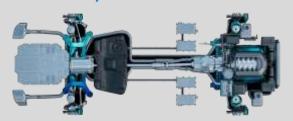




Mapping of Functional Safety Requirements to Semiconductors

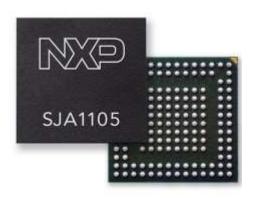
Contains functions with certain safety requirements ("context"):





Derived Functional Safety requirement: ???

In-Vehicle Networking products enable many different functions. Detailed information of the system requirements of the actual use cases are usually not available







System definition

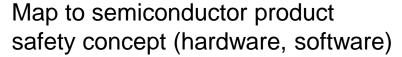


System safety concept



System safety analysis

OEM



Semiconductor Manufacturer



Defining Semiconductor Products as "Safety Element out of Context"



- Assume the use cases in the car (context)
- Assume safety goals



Assume the acceptable risk level per function



- → Assume the context, derive commonalities with relevance for In-Vehicle Networking
- → E.g. ADAS, like adaptive cruise control or parking assistant with multiple sensors, like radar and camera.

→ Define goal: ASIL A/B/C/D

e.g. Which level of self diagnosis is required during operation and which part of the product is involved in diagnostics

Transfer the assumed system requirement into product requirements and identify the related

functional blocks.



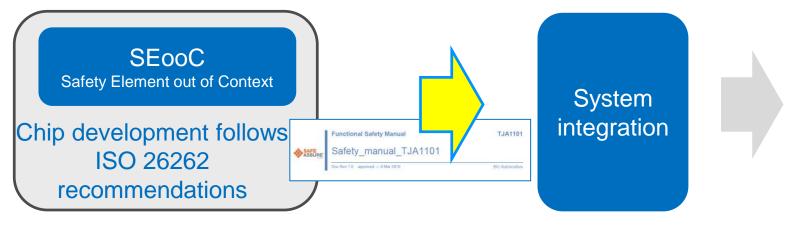


Integration Flow – From Chip To System

NXP adds safety features based on assumptions

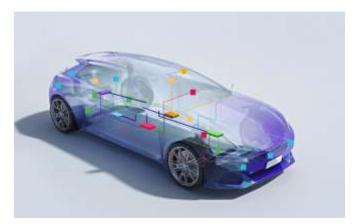
Customer to match assumptions to real use case

Matched! chip ASIL rating is valid when the assumptions are valid













Functional Safety Commitment

SafeAssure



The **SafeAssure** program →NXP's commitment to supporting functional safety through a safety-conscious culture, discipline and collaboration

Hardware

- Detect and mitigate random hardware failures using built-in safety features
- Automotive Ethernet, MCUs, analog and power management ICs and sensors

Software

Works seamlessly with hardware for system-level functional safety goals

Support

- Safety documents, Technical support
- SafeAssure product-specific safety documents, upon request

Process

- ISO 26262 certified hardware development process
- → Preventing systematic failures

Automotive
ISO 26262
Safety
Support
Safety
Hardware
Safety
Process
NXP Quality Foundation

Design for Functional Safety goes far beyond the single product...

It requires a living culture and development process to enable the system advantage.



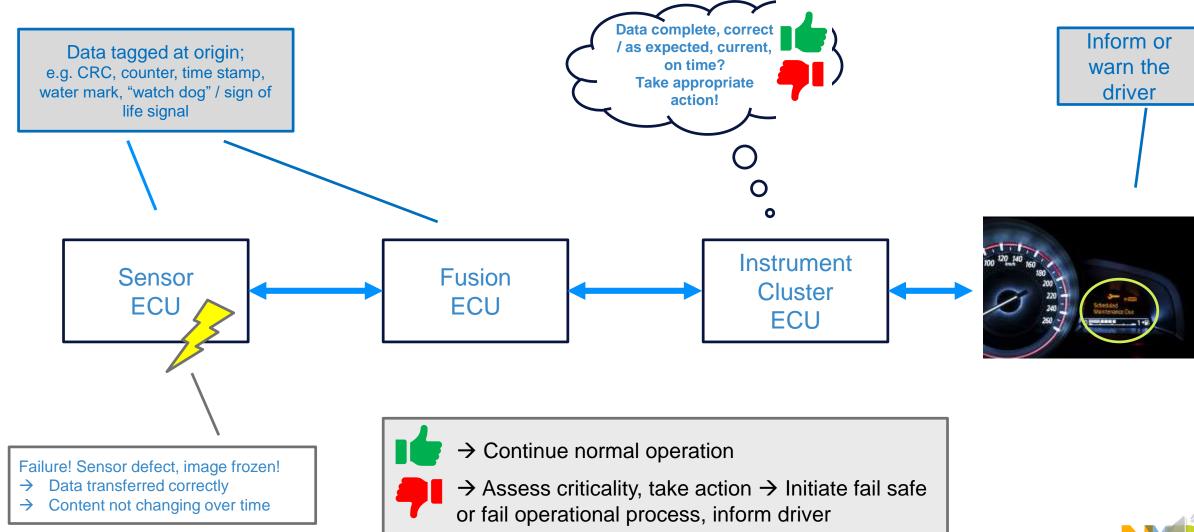


Functional Safety in The Robot-Car Era



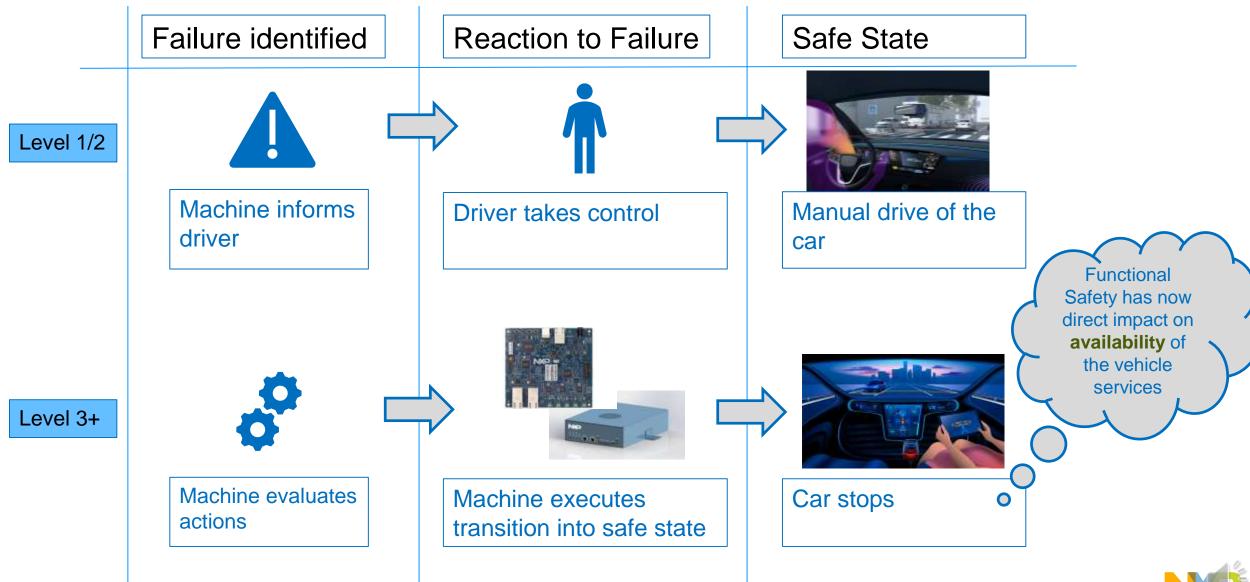


End-to-end FuSa Implementation Example up to AD Level 2





How is Autonomous Driving Changing the Game?





How the Networking IC Keeps Your Robo-Car Driving?

Vehicle service availability can be improved by ensuring the availability of communication services in the vehicle. Networking chips can:

- Prevent Failure
 - Highest reliability



- Predict Failure
 - (Self-)Diagnostic features

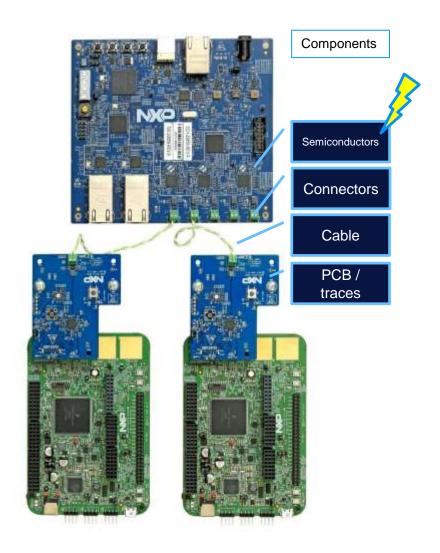


- React to Failure
 - Quickest response time to increase FTTI margin
 - Even correct some failures





Relation Between Availability and Reliability



- Availability of communication is determined by the reliability of components in the signal path
- Total FIT = SUM(Component FIT)
- FIT (Failure In Time)
 - describes the probability that a component fails, i.e. random HW failure
 - Initially estimated based on technology parameters for future products (e.g. SN92500)

Manufacturing quality directly impacts the FIT rate and probability of failure



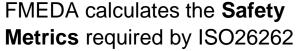
Measure of Failure Prevention

from failure rate to safety metrics

Calculate
HW failure rate (FIT)







FMEDA: Failure Mode Effects and Diagnostic Analysis

LFM: Latent Fault Metric

PMHF: Probabilistic Metric for (Random) Hardware Failures

SPFM: Single Point Fault Metric





Compare

with standard [ISO-26262, part 5]

ASIL	SPFM	LFM	PMHF
В	≥ 90 %	≥ 90 %	< 10 ⁻⁷ h ⁻¹
С	≥ 97 %	≥ 97 %	< 10 ⁻⁷ h ⁻¹
D	≥ 99 %	≥ 99 %	< 10 ⁻⁸ h ⁻¹



Failure Prevention

Example Reference FIT calculation			CL parameter details, please contact NXP
TJA1043U	Siemens Norm SN92500	HTOL Qual CAN Family	Production & Field Return Data CAN Family
Reference FIT calculation	42 FIT	3.0 FIT	0.04 FIT

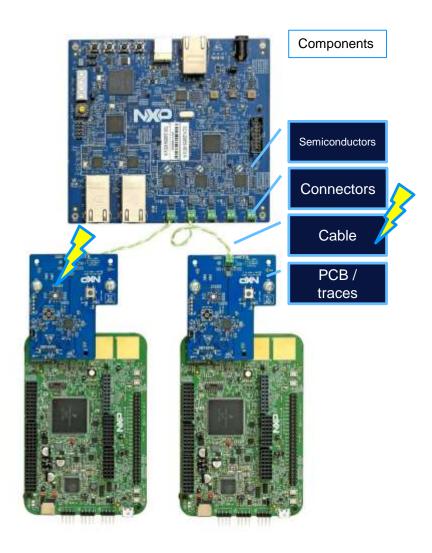
Manufacturing quality makes the difference

- NXP applies screening & continuous improvement of screening methodology based on production and field return data
- The methodology is independent of process technology



HTOL: High-Temperature Over Life

Relation Between Availability, Prediction and Reaction



- Failure may occur anywhere in the communication chain, e.g. cable degradation or weak PCB solder connections
- Availability of communication is further determined by
 - The time it takes to detect (localize / categorize) issues
 - The ability to respond depending on the criticality of issues
- Examples of FuSa features on IC level
 - Predict:
 - Temperature / Voltage Monitoring
 - Signal Quality Indicator
 - React:
 - Memory Failure Correction (ECC)
 - IEEE 802.1CB (Stream replication / elimination)

From E2E Protection To Highly Available Communication Path

Example: ECC

Failure: memory cell defect

→ Frame sent to the wrong destination

Fusion

ECU

Failure: memory cell defect

→ Frame sent to the wrong destination

Steering

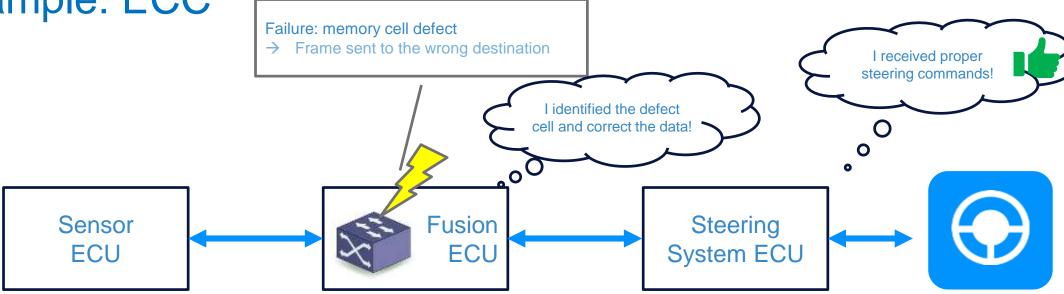
System ECU

System ECU

- Solution 1) Detected by end2end FuSa implementation!
 - → system decision: trigger safe state → stop the car!

From E2E Protection To Highly Available Communication Path

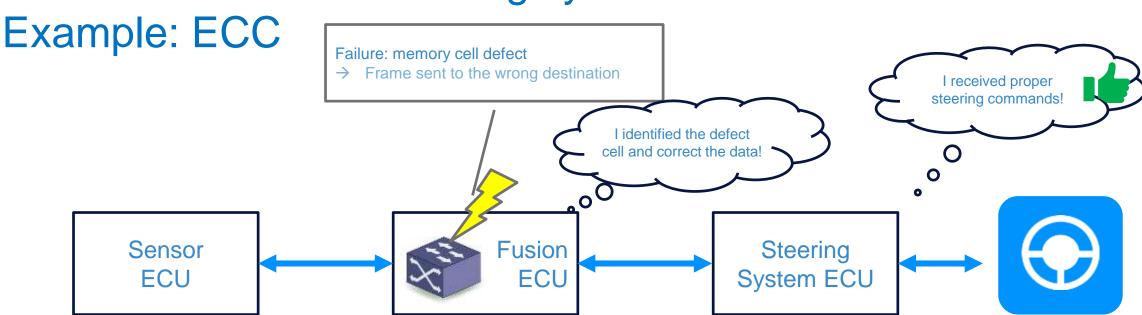
Example: ECC



- Solutions 2) Handled by highly available system:
 - Local detection and correction
 - ECC: defective memory cell detected by the switch itself
 - Action triggered by the switch: report and / or repair!
 - → System decision: → continue normal operation!
 - → Request further data for evaluation
 - Trigger service stop & ECU exchange



From E2E Protection To Highly Available Communication Path



- Solutions 2) Handled by highly available system:
 - Local detection and correction
 - ECC: defective memory cell detected by the switch itself
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 - → System decision: → continue normal operation!
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- Both system solutions achieve the same ASIL!
- Only the highly available system is enhanced by local detection / correction, plus the availability of information to the system level for more fine grain resolution of action
- In a redundant system, a part of the system may even be restarted during operation



Conclusion

- Chip ASIL ratings are valid when the assumptions match the use case!
- Cars are safe today, future cars remain safe
- Vehicle availability (customer experience) can be enhanced
- Networking IC features can increase the vehicle availability by preventing, predicting and reacting to failure scenarios
- Manufacturing quality and development process are the basis for highly available systems
- NXP is a unique partner to co-define and realize safety & availability concepts for
 - Predictive Maintenance
 - Fail operational networks



driving EthernetTM











SECURE CONNECTIONS FOR A SMARTER WORLD