June 2010

MPC5674F Hardware Requirements

FTF-AUT-F0680

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Microcontroller Automotive Applications

freescale™ semiconductor

Presentation Agenda

- Session Objectives
- MPC56xx Roadmap and MPC567xF Overview
- Power Supplies
- Clock Modes
- Analog to Digital Converter
- eTPU
- eMIOS
- BAM Controlled Startup
- Other Peripherals
- Pin Configuration
- Debug Features
- Hardware Checklist
- SmatMOS Companion Devices

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Objective

- This seminar presents the minimum hardware requirements for designing an engine controller module based on the MPC567xF Power Architecture Microcontroller with an e200z7 32-bit dual issue core, 4M flash, 256K SRAM, 96 timing channels, and 64 channel ADC, plus FlexRay, CAN, serial and SPI communication interfaces for advanced powertrain applications, including interfacing to Freescale analog SmartMOS devices. This seminar also covers basic hardware requirements for the device including using the on-chip linear and switching power supplies.

- **Application Note available:**
  - **AN3971 “MPC567xF Hardware Requirements”**

Note: not all slides in this presentation can be presented during a 1 hour training session and a reduced set will be covered that covers the objective listed above. The additional slides provide additional information that may be useful in designing a system.

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32-Bit Roadmap

rain Chassis, Safety, ADAS Body, Cluster Vehicle Communications

Application Performance / Integration

MPC5200B
300M DRAM, USB 1.1, PATA
e300, up to 400 MHz

MPC5561
1M Flash, 192K RAM
e200z6 core, up to 200 MHz

MPC5566
3M Flash, 128K SRAM
e200z6 core, up to 144 MHz

MPC5567
2M Flash, 80K SRAM, FlexRay
e200z6 core, up to 144 MHz

MPC5565
2M Flash, 80K SRAM
e200z6 core, up to 144 MHz

MPC5554
2M Flash, 64K SRAM
e200z6 core, up to 144 MHz

MPC5553
1.5M Flash, 64K SRAM
e200z6 core, up to 144 MHz

MPC5517x
1.5M Flash, 80 KB RAM,
up to 80MHz
e200z1+e200z0 (not on S version)

MPC5516x
1M Flash, 64KB RAM
Up to 80MHz
e200z1+e200z0 (not on S version)

MPC5515S
768KB Flash, 48 KB RAM
Up to 80MHz
e200z1+e200z0 (not on S version)

MPC5514E/G
512KB Flash
e200z0+e200z0

MPC5534
1M Flash, 64K SRAM
e200z3 core, 40-80 MHz

MPC5674F
4M Flash, 256K SRAM, FlexRay
e200z7 core, up to 264 MHz,

MPC5668G
2M Flash, 592K SRAM, FlexRay
E200z6+e200z0, up to 128 MHz

MPC5634M
1.5M Flash, 94K SRAM
e200z3 core, up to 80 MHz

MPC5633M
1M Flash, 64K SRAM
e200z3 core, up to 80 MHz

MPC5632M
768K Flash, 48K SRAM
e200z3 core, up to 80 MHz

MPC5604P
512K Flash, 40K SRAM, FlexRay
e200z0 core, up to 64 MHz

MPC5603P
384K Flash, 36K SRAM, FlexRay
e200z0 core, up to 64 MHz

MPC5604P
256K Flash, 20K SRAM
e200z0 core, up to 64 MHz

MPC5604B/C
512K Flash, 32K(B), 48K(C) SRAM
e200z0 core, up to 64 MHz

MPC5603B/C
384K Flash, 28K(B), 40K(C) SRAM
e200z0 core, up to 64 MHz

MPC5602B/C
256K Flash, 24K(B), 32(C) SRAM
e200z0 core, up to 64 MHz

MPC5606S
1M Flash, 48K SRAM
160K Graphics RAM, LCD
e200z0h core, up to 64 MHz

MPC5604S
512K Flash, 48K SRAM, LCD
e200z0h core, up to 64 MHz

MPC5602S
256K Flash, 24K SRAM, LCD
e200z0h core, up to 64 MHz

Offered in high temp packaging or known good die (bare die)

Qualification by 2008 | **Recently Announced** | **Future Committed Products (2009+)**

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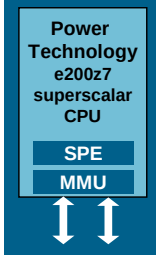
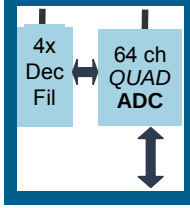
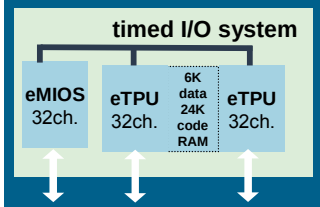
MPC5674F: 4 MB Engine Controller with FlexRay™



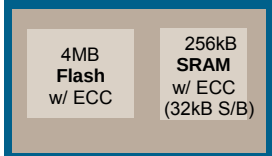
600 DMIPS from 264 MHz core, integrated DSP allowing users to create 'virtual sensors'



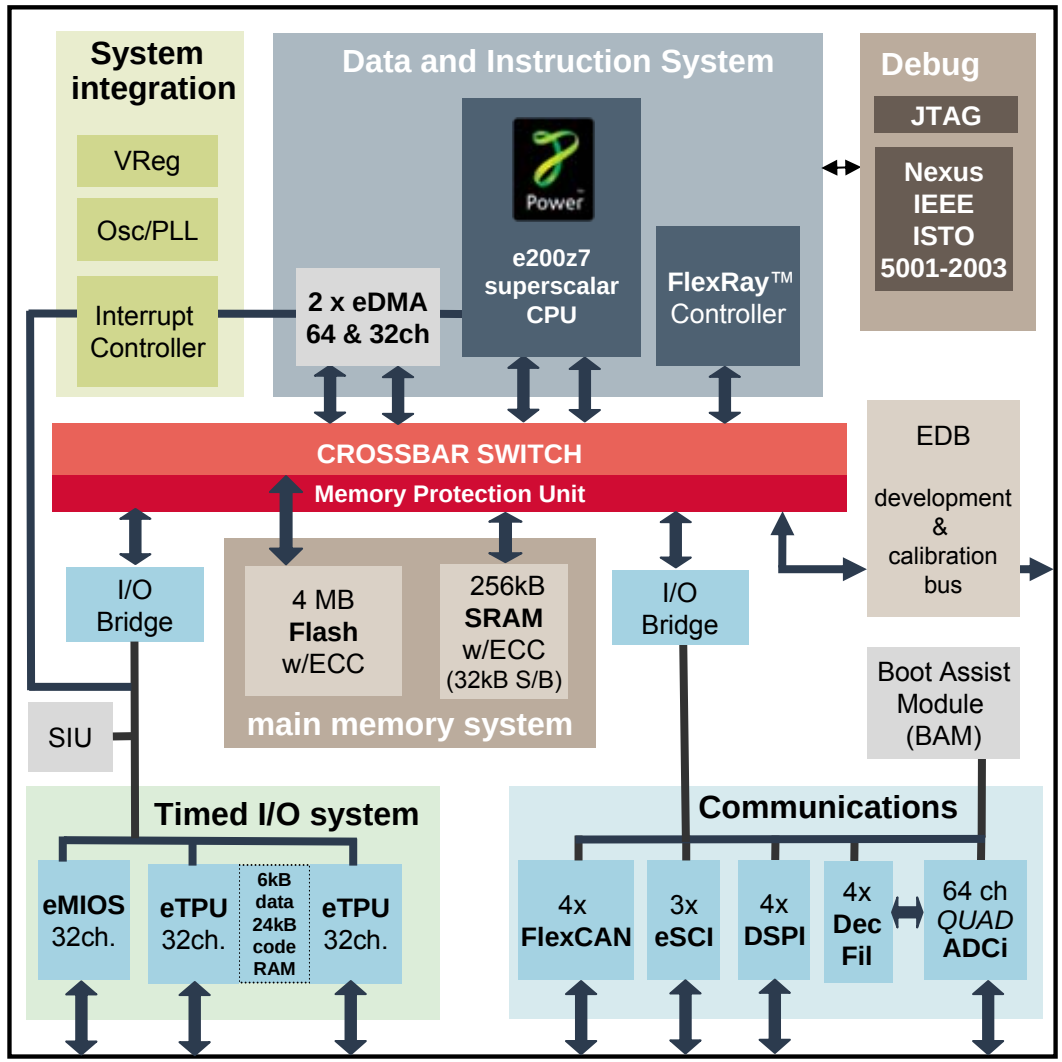
Only quadruple ADC on market, with built-in filtering system allows PCB cost reduction



Most precise engine timers available, control fuel delivery & improve gas mileage



Largest program memory for market space helps with autocoding; zero defect technology on all memories



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MPC5674F

Core

- **Single core 264 MHz e200z7**
  - Power Architecture™ ISA + VLE
  - Supports NMI and low power mode
  - Self test, context switch and debug enhancements

Memory

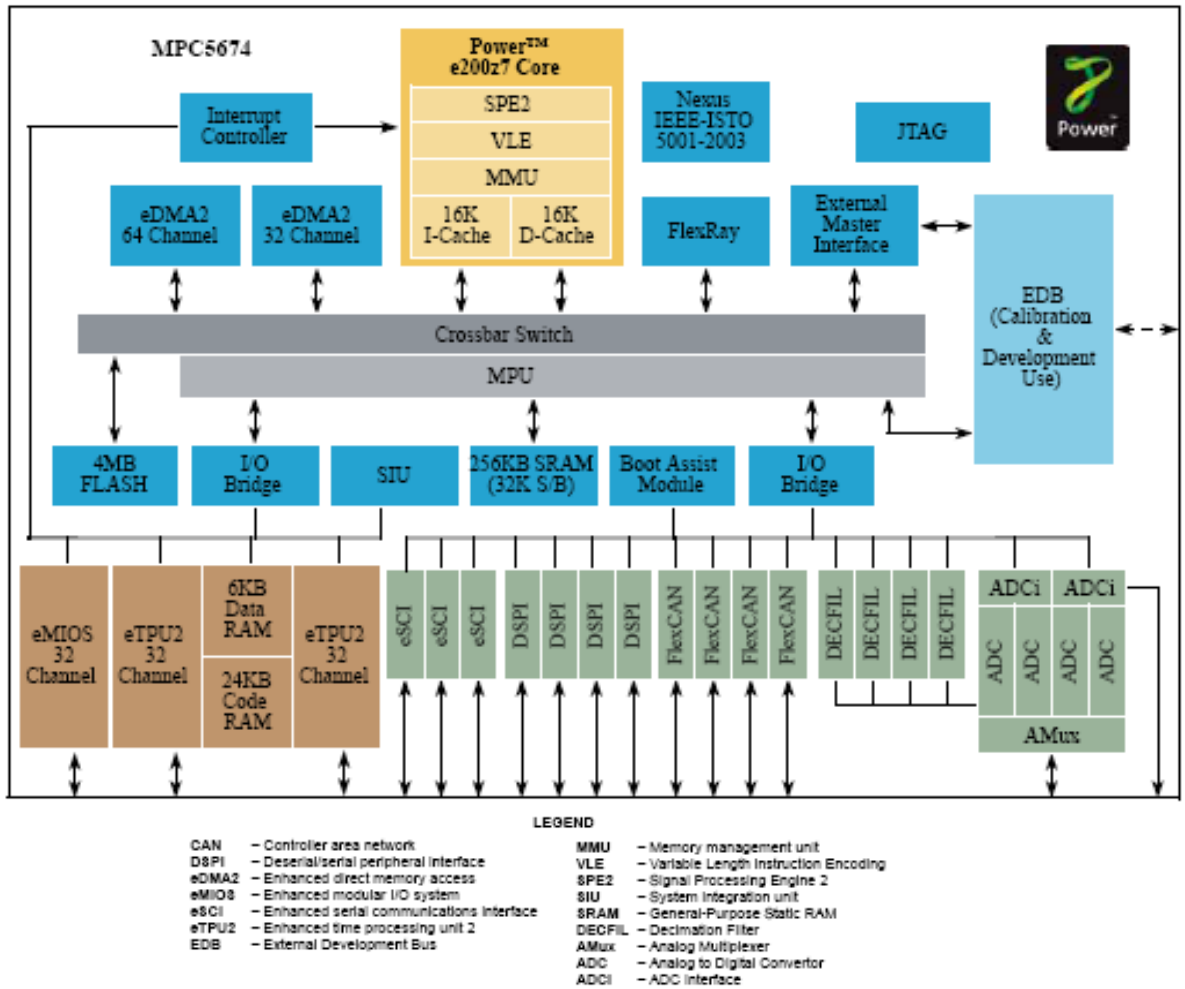
- **4M byte RWW Flash**
- **256K Data RAM**
  - 32K Standby
- **30K eTPU SRAM**
  - 32k code RAM, 6k parameter RAM
  - Parity protection
- **32K Cache (16k i-cache, 16k d-cache)**

I/O

- Selectable 2:1 or 1:1 frequency divider for I/O modules
- 64 channel Dual eTPU2
  - Reaction channels for closed loop injector control
- 32 channel EMIOS with unified channels
- Dual FlexRay - dual channel, up to 10Mbps
- 4 x FlexCAN - compatible with TouCAN, 64 buffers each
- 3 x eSCI
- 4 x DSPI 16 bits wide up to 6 chip selects each
- 64 channel quad ADC - up to 12 bit < 1□s conversions, 12 queues with triggering and DMA support.
  - Variable gain amplifier per channel
  - Temp sensor
  - 4 Decimation filter hardware with enhanced source and destination options

System

- FM-PLL
- 64 + 32 channel DMA controller
- Nexus IEEE-ISTO 5001-2003 Class 3
- 5/3.3V IO, 5V ADC, 3.3V/1.8V bus, 1.2V core (from internal regulator controller)
- System watchdog with windowing support
- System timer module
- On chip regulator for standby voltage
- Standby voltage brown-out detect
- Programmable VRC and LVI voltages
- 416 PBGA package (no EDB)
- 496 vertical CSP (Calibration package)
- 516 PBGA package (with EDB)



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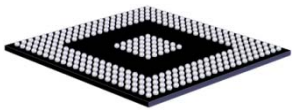
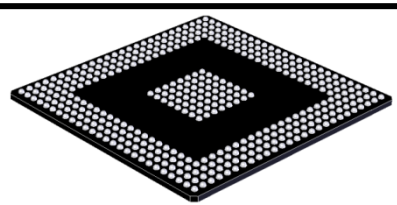
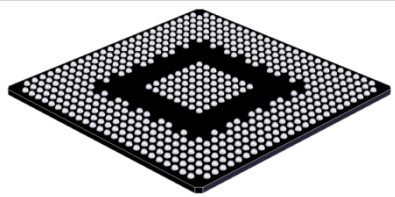
Package Options

Package	Features
416 TEPBGA (27x27mm)	Primary device with the base features of the device. No development bus (including no CLKOUT). Four outer rows of balls
516 TEPBGA (27x27mm)	All of the features of the 416 TEPBGA package with the addition of access to the development bus (External Bus Interface). Six outer rows of balls
324 TEPBGA (23x23mm)	Same basic features of the 416 TEPBGA package except: ▸Reduced number of eTPU channels as the primary pin function on both eTPUs (eighteen channels fewer) ▸No "shared" ADC channels (AN24:39, 16 channels fewer) ▸Reduced number of GPIO pins (5 dedicated GPIO fewer) ▸Reduced number of DSPI chip selects as primary pin function (13 SPI chip selects fewer) ▸Reduced number of eMIOS channels as primary pin function (1 less) ▸No BOOTCFG0 or WKPCFG pins ▸No eSCI pins as primary function are available; only eSCI A signals are available as alternate ▸functions on other pins







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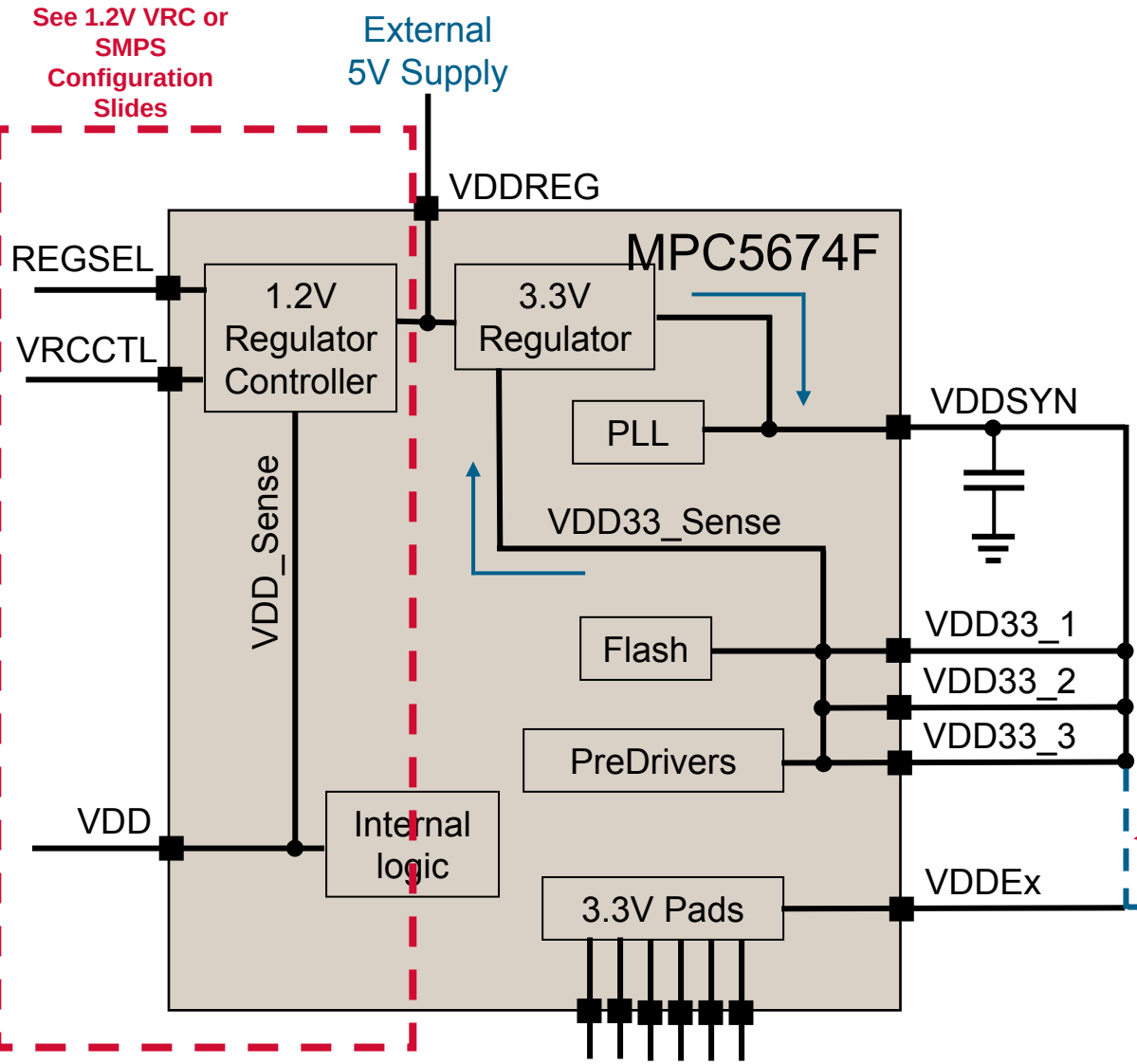
Power Supplies: Introduction

- Internally, four power supplies are required
  - 5V, 3.3V, 1.2V and VSTBY
- Externally 5V required
  - All supplies can be powered by single 5V
  - If using external development bus, external 3.3V required
- 3.3V and 1.2V can be generated from internal regulators
  - Possible to supplement these with external regulators
- SRAM standby supply can be 1.0 or 3.3 to 6.0 volts
- No sequencing requirements for power supplies

Power Supply Options

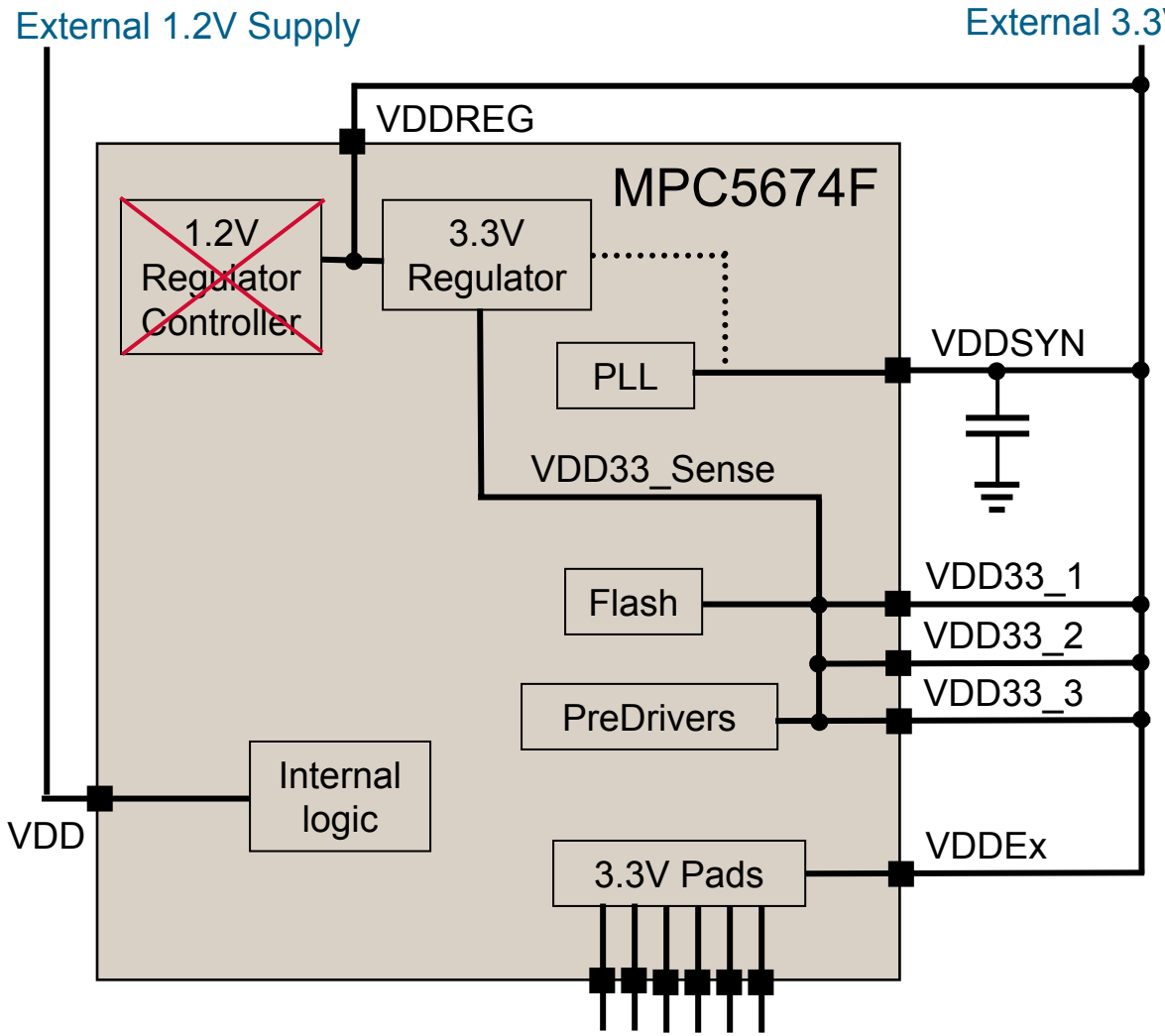
Configuration	3.3V Supply	1.2V Supply	REGSEL	VDDREG
Internal regulators with 1.2V LDO	Internal	Internal LDO	Low	5V
Internal Regulators with 1.2V SMPS	Internal	Internal SMPS	VDDREG	5V
External 5V, 3.3V, 1.2V	External 3.3V	External 1.2V	3.3V	3.3V
Mixed, internal and external	External, except VDDSYN supplies VDD33	1.2V LDO or SMPS	Low or VDDREG	5V

Internal 3.3V Regulator



- The 3.3V internal regulator is externally available on the VDDSYN pin.
- Initial documentation showed isolation between VDDSYN and VDD33. This isolation will degrade the performance of the regulator.
- Optionally, if the external bus and Nexus trace are not being used, the internal regulator can be used to power the VDDEx supplies.

Using an External 3.3V Supply (Internal Supplies Disabled)



- The internal 3.3V regulator can be disabled by connecting VDDREG to a 3.3V supply (instead of to 5V). **This also disables the 1.2V regulator.**
- Initial documentation showed isolation between VDDSYN and VDD33. This isolation will degrade the performance of the regulator.
- VDDREG also powers the internal Low Voltage Detect Circuits. If VDDREG is connected to ground, the internal LVIs are disconnected.

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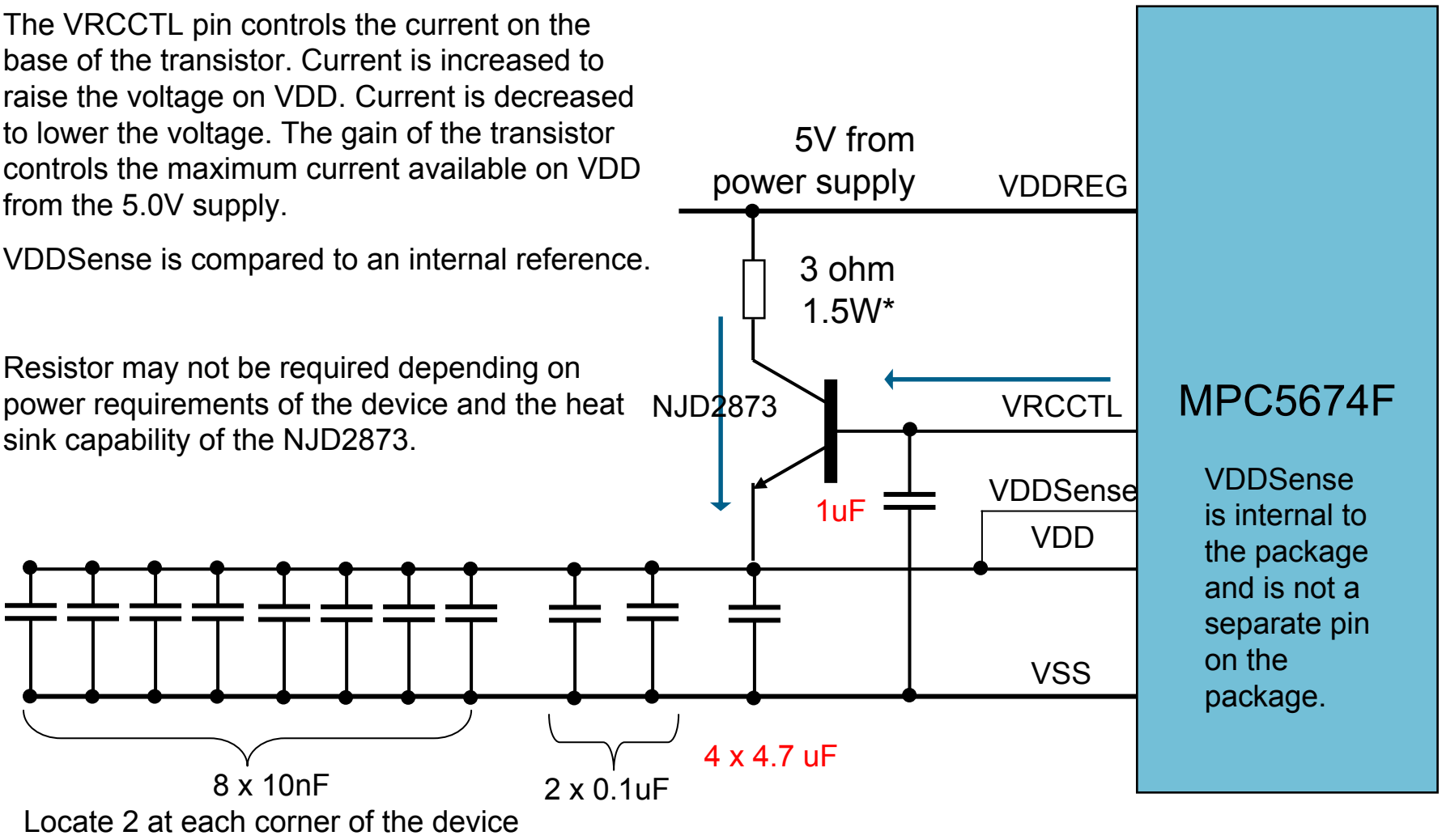
VRC: On Chip 1.2V Regulator Controller (Linear)

The VRCCTL pin controls the current on the base of the transistor. Current is increased to raise the voltage on VDD. Current is decreased to lower the voltage. The gain of the transistor controls the maximum current available on VDD from the 5.0V supply.

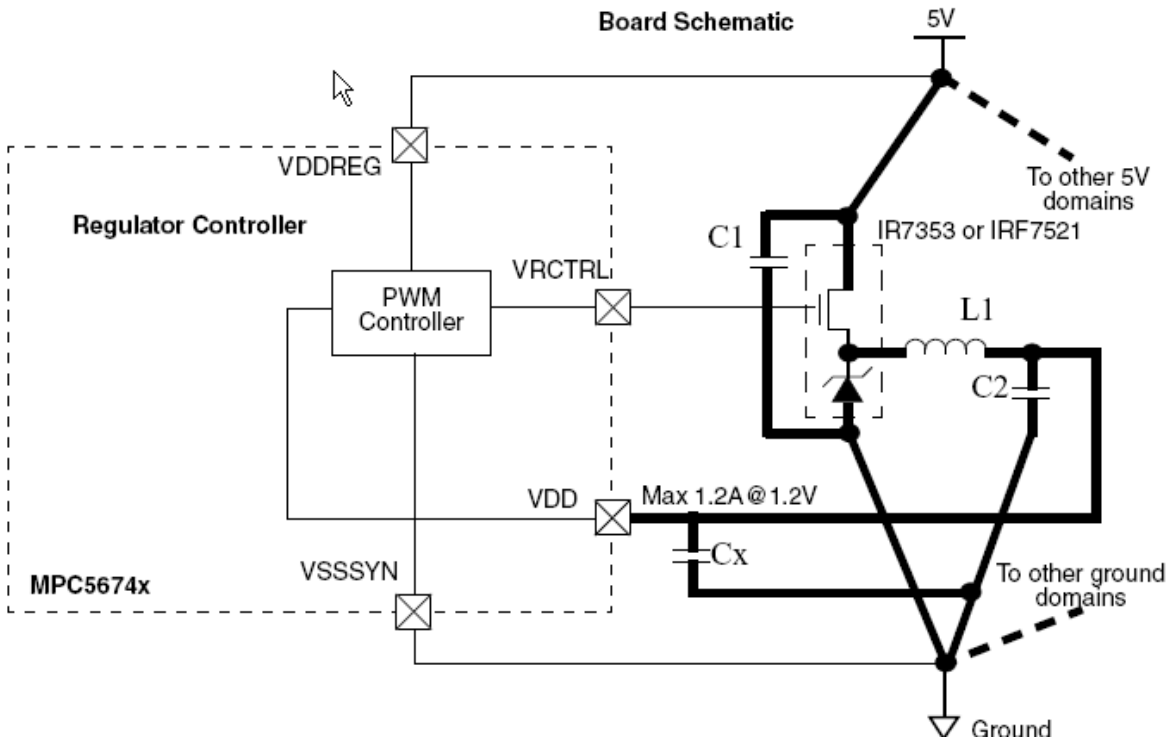
VDDSense is compared to an internal reference.

Resistor may not be required depending on power requirements of the device and the heat sink capability of the NJD2873.

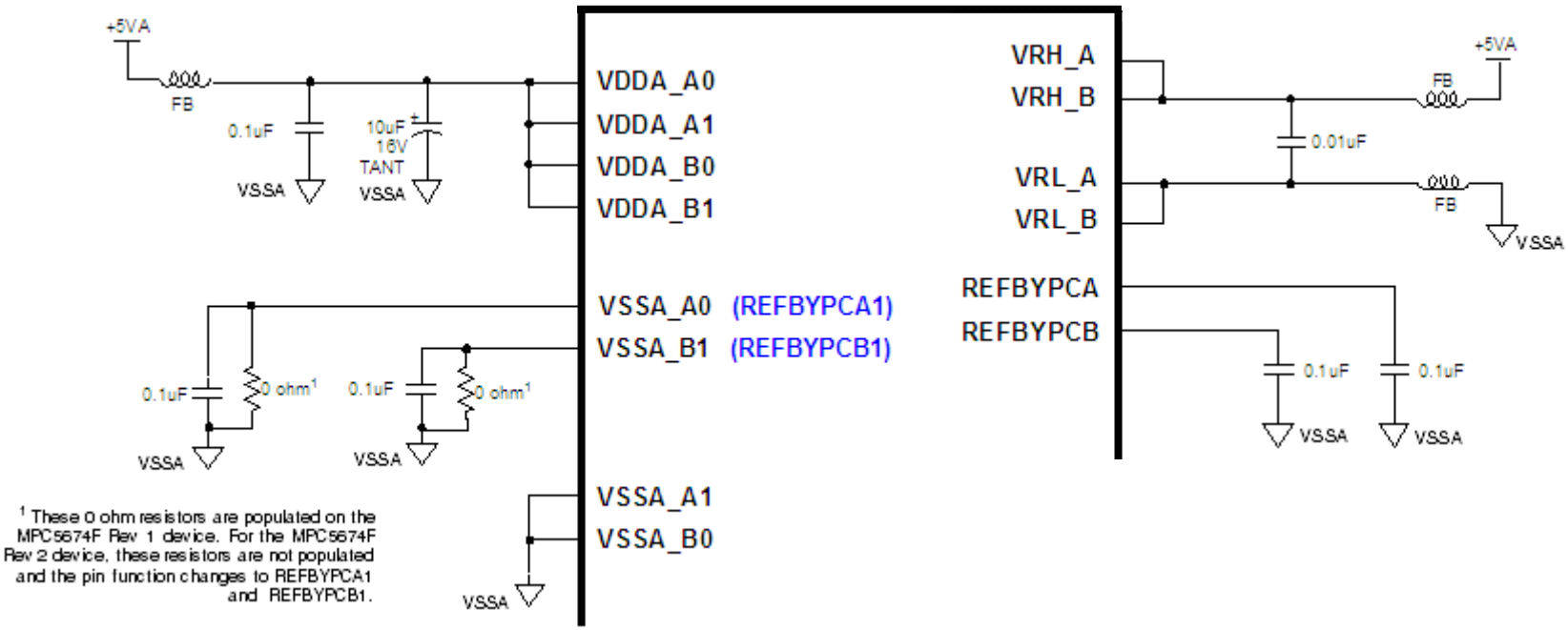


On-Chip 1.2V Regulator Controller - Switch Mode Power Supply (SMPS)

- Optional Switched Mode Power Supply (SMPS) implemented to generate 1.2V supply
  - External components required: Inductor, FET, diodes, capacitor
  - Layout considerations to be made
  - Reduced power loading for 5V power supply
  - Connect REGSEL to VDDREG externally to select SMPS
  - See application note AN3898



MPC5674F ADC Connections



- Note: Shows the revision 1 versus revision 2 changes. VSSA_A0 and VSSA_B1 pins are available on revision 1 only. These pins are replaced by REFBYPCA1 and REFBYPCB1.

Decoupling Capacitors

- In general, use the largest value capacitor, in the smallest package (lower inductance)
- When components are placed on both sides of the board, bypass capacitors can be placed directly under the MCU.
- In cases where there is no room for all of the recommended capacitors, a larger value high-frequency capacitor should be used and kept closer to the MCU.
- When deciding where to best place the bypass capacitors, use the following priority:
  1. PLL power supply (VDDSYN)
  2. ADC reference pins (VRH/VRL)
  3. ADC power pins (VDDA)
  4. Core power supply (VDD)
  5. I/O power supplies (VDDE/VDDEH)

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Digital Power Supply Bypass Capacitors

Supply	Voltage	Quantity	Capacitor Value	Notes
VDDREG	3.3V to 5V	1	4.7 uF/16V	Caps should be close to the MCU supply input
		1	0.1 uF	
VDDSYN (3.3V Output) VDD33 (3.3V Input)	3.3V	1	10 uF / 16V	VDDSYN should be shorted to VDD33 on the board with minimum impedance
		1	0.1 uF	
		1	1000 pF	
VDDE2	3.3V	5	10 nF	External bus supply
VDDEH1, VDDEH3, VDDEH4, VDDEH5, VDDEH6, VDDEH7	3.3V or 5.0V	5	10-200 nF	
VDD	1.2V (Input)	6	2.2 uF / 16 V	
		7	10-200 nF	
VSTBY	1V to 5V	2	10-200 nF	
VDDE8, VDDE9, VDDE10	3.3V	5	100 nF	516 package only

Power Supplies: Low Voltage Detection

- Low voltage detection for following supplies:
  - 5V
  - 3.3V
  - Core (1.2V)
  - RESET pin supply
  - VDDEH
  - VDDA
- Default settings
  - 3.3V, 1.2V and RESET supply generate RESET if low voltage detected
  - 5V, VDDEH and VDDA low voltage detect is disabled
- All above supplies can be configured to:
  - Raise interrupt on low voltage detection
  - Generate RESET on low voltage detection
  - These settings can be locked to avoid accidental writes

Power Supplies: ADC Monitoring

- ADC can be used to monitor power supplies
  - 1.2V bandgap for absolute conversions
- 5V and 3.3V LVD thresholds divided down to be compared to 1.2V bandgap reference
  - Keeps LVDs within ADC range
- 1.2V LVD threshold divided down to be compared to 600mV bandgap reference
- Monitoring of supplies – divided down to be compared to 1.2V bandgap reference
  - VDD33
  - VDDSYN
  - VDDEHx
  - VDD12 (absolute value taken)

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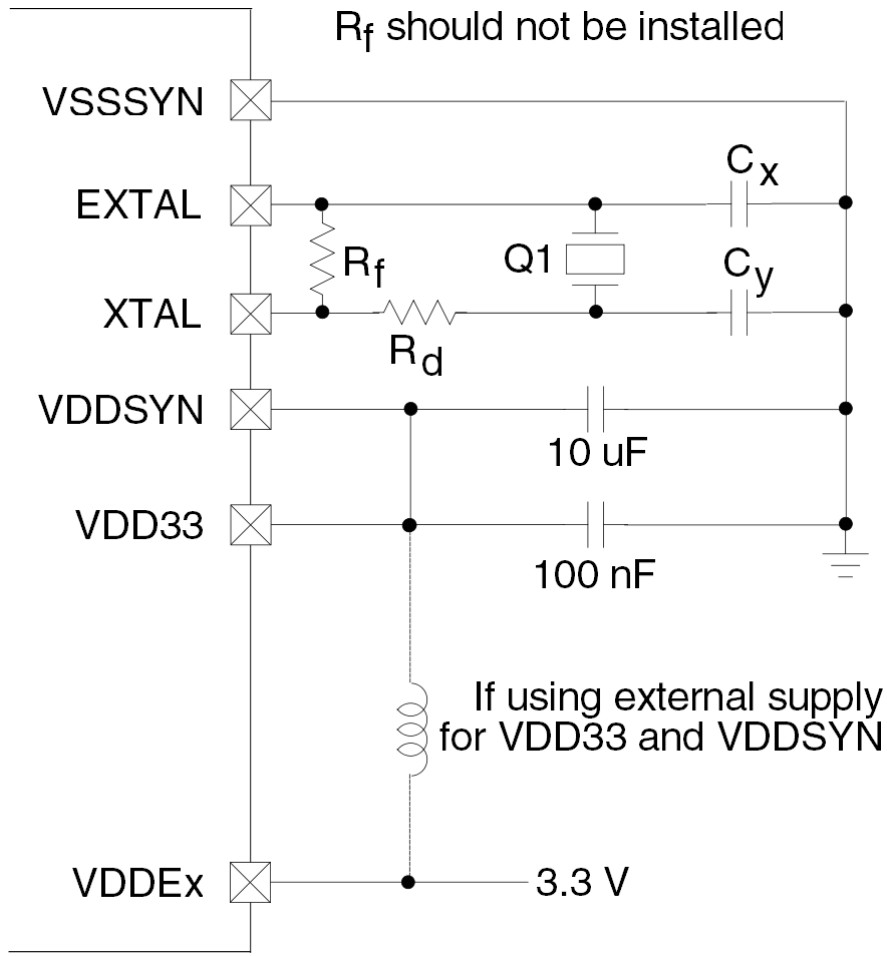
- Summary

Crystal Circuit

- MPC567xF supports either an on-chip oscillator or can use an external reference clock
  - 4 to 20 MHz crystal mode supported
  - 16 to 40 MHz crystal range supported
- On-chip PLL multiplies this frequency up to the required system frequency



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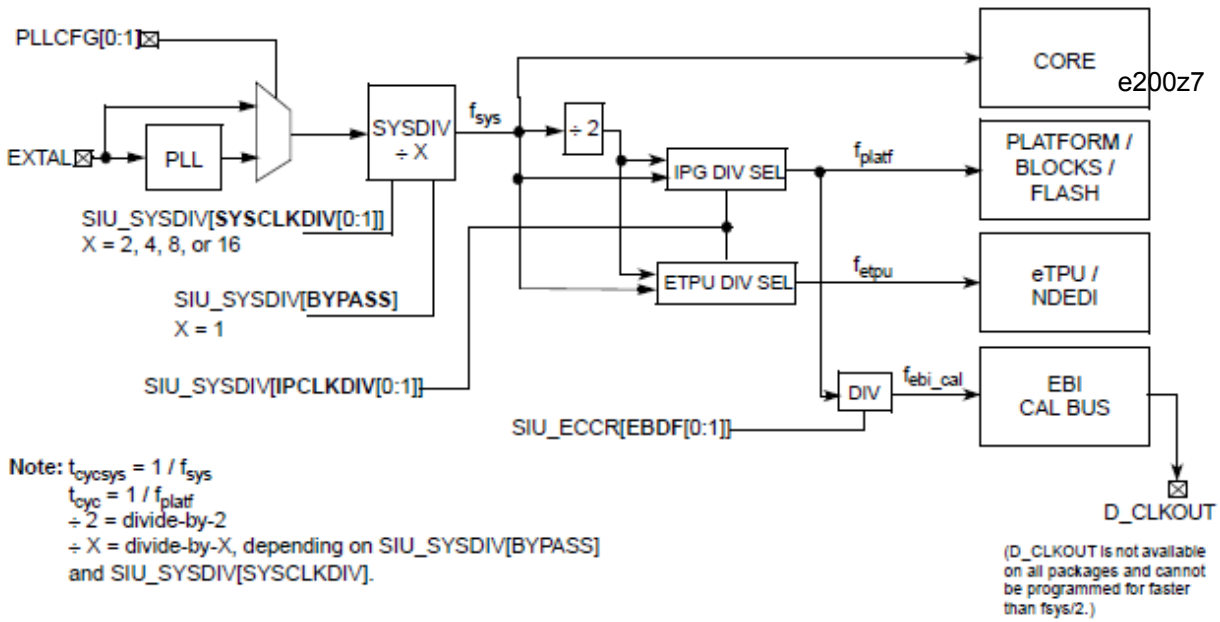
MPC567xF Clocking Modes



SIU_SYSDIV [IPCLKDIV[0:1]	Mode	Description	Maximum Frequency
0b00	Enhanced	CPU frequency is doubled. Platform, peripherals, and eTPU clocks are 1/2 of CPU frequency	264 MHz
0b01	Full	CPU and eTPU frequency is doubled. Platform and peripheral clocks are 1/2 of CPU frequency.	200 MHz
0b10	-	Reserved	-
0b11	Legacy	CPU, eTPU, platform, and peripheral clocks all run at the same speed	132 MHz

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eQADC: Features (1 of 2)

- Four independent on-chip ADCs
  - Implemented as 2 eQADC modules, each with 2 on-chip ADCs
  - 8, 10 and 12 bit resolution
  - Single-ended signal range from 0 to 5V
  - 4 pairs of differential analog input channels (+/-2.5V peak-to-peak)
    - Programmable pull ups, pull downs for each diff input for piezo sensor diagnostic
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
  - Right- justified unsigned and signed result formats
  - Provides time stamp information when requested

Resolution	Max. Rate ADC_CLK	Conversion Type	Min. # of ADC_CLKs	Conversion Rate	Conversion Time
12-bit	**16 MHz**	**Differential**	**15**	**1 M /sec**	**1.0 usec**
		Single Ended	**16**	**938 K /sec**	**1.06 usec**
10-bit	**16 MHz**	**Differential**	**13**	**1.15 M /sec**	**867 nsec**
		Single Ended	**14**	**1.07 M /sec**	**933 nsec**
8-bit	**16 MHz**	**Differential**	**11**	**1.36 M /sec**	**733 nsec**
		Single Ended	**12**	**1.25 M /sec**	**800 nsec**

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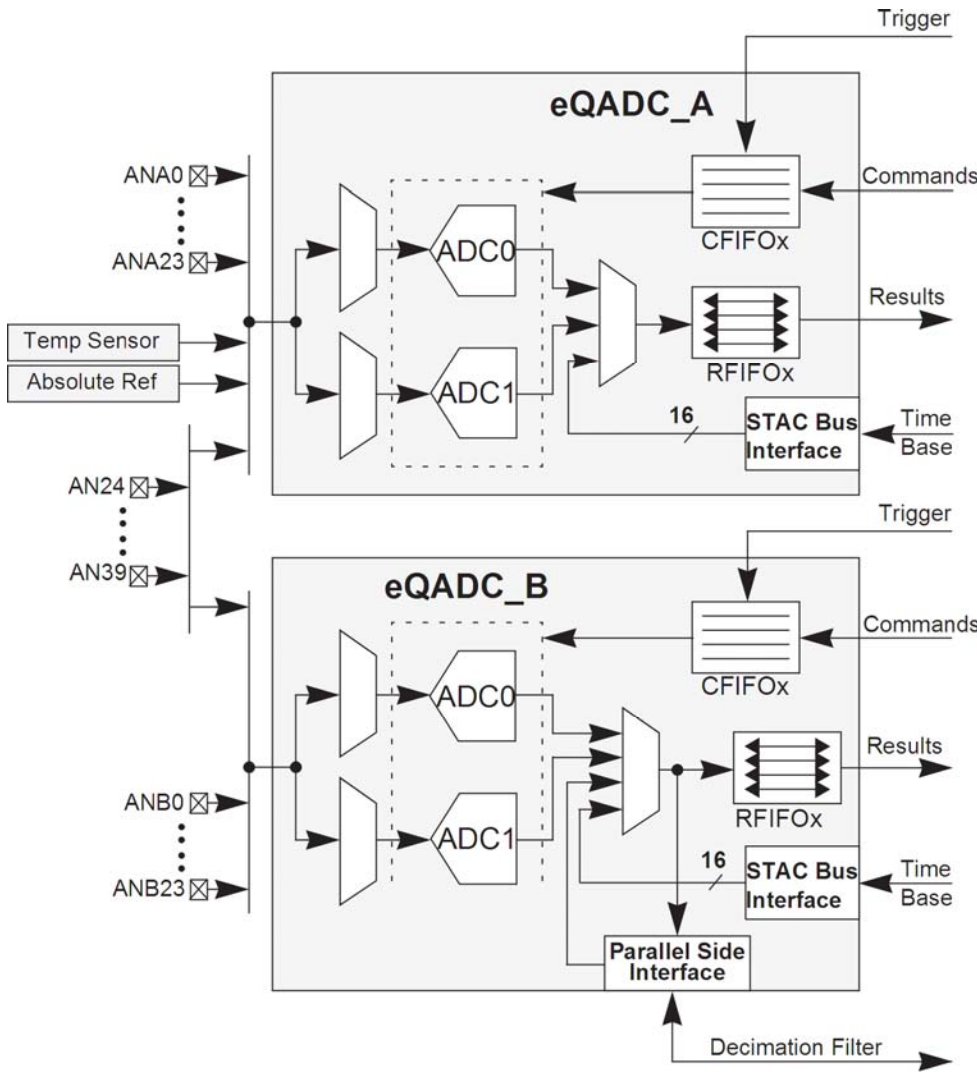
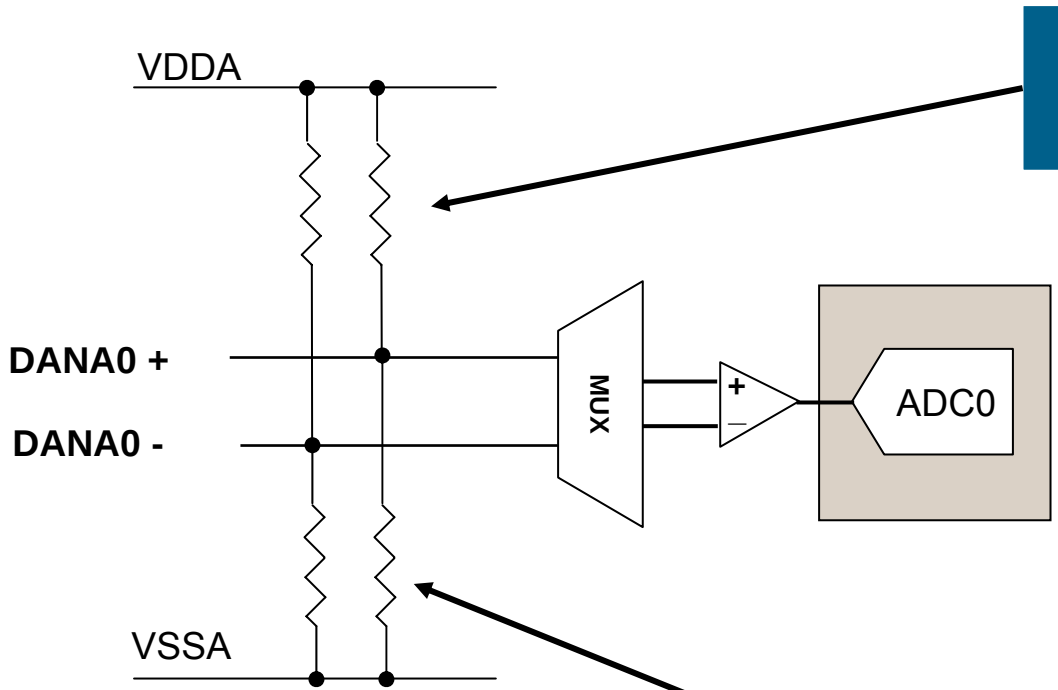
eQADC: Features (2 of 2)

- 64 input pins available in 416 BGA package
  - 24 pins exclusive to each pair of ADCs (48 total)
  - 16 pins shared among all ADCs
- Six independent trigger sources for each eQADC module
  - Implemented through 6 independent Command FIFOs (CFIFOs)
    - Each CFIFO has own trigger source
    - Each CFIFO has 4 entries to allow for DMA latency
  - External hardware triggers
- Analog channel expansion capability
  - Supports 8 external 8-to-1 muxes which can add an additional
- ADC queue 0 preempt for reduced conversion jitter
- Configurable decimation filter
- Custom calibration variables
- Queue triggers from PIT
- ADC streaming without commands



eQADC: Knock Input Bias

- All differential input pins can be supplied with bias current from internal resistors



Selectable between:

200k / 100k / 5k

Options:

Pull Up / Pull Down / Centre Bias

No Bias

1% accurate resistors

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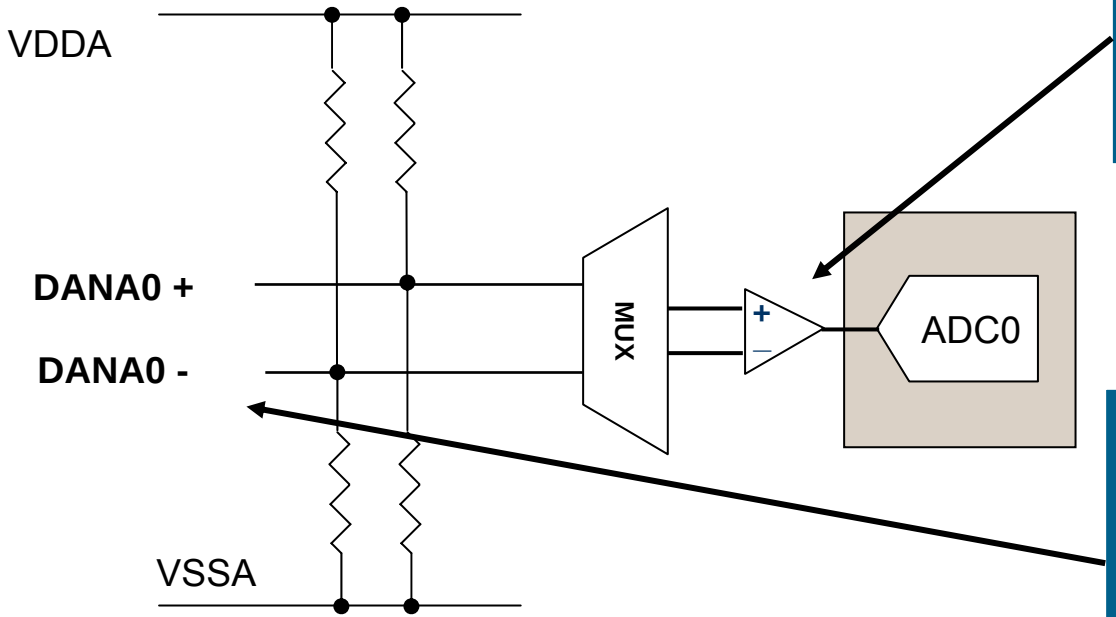
eQADC: Pre-Gain

- Differential conversions can have x2 and x4 gain applied to the signal prior to conversion
  - Reduces impact of quantization noise, targeted at knock detection



Variable gain amplifier performs x2 and x4 operations on differential inputs

Differential voltage range limitations

x2 mode: -1.15V to +1.15V

x4 mode: -0.525V to +0.525V

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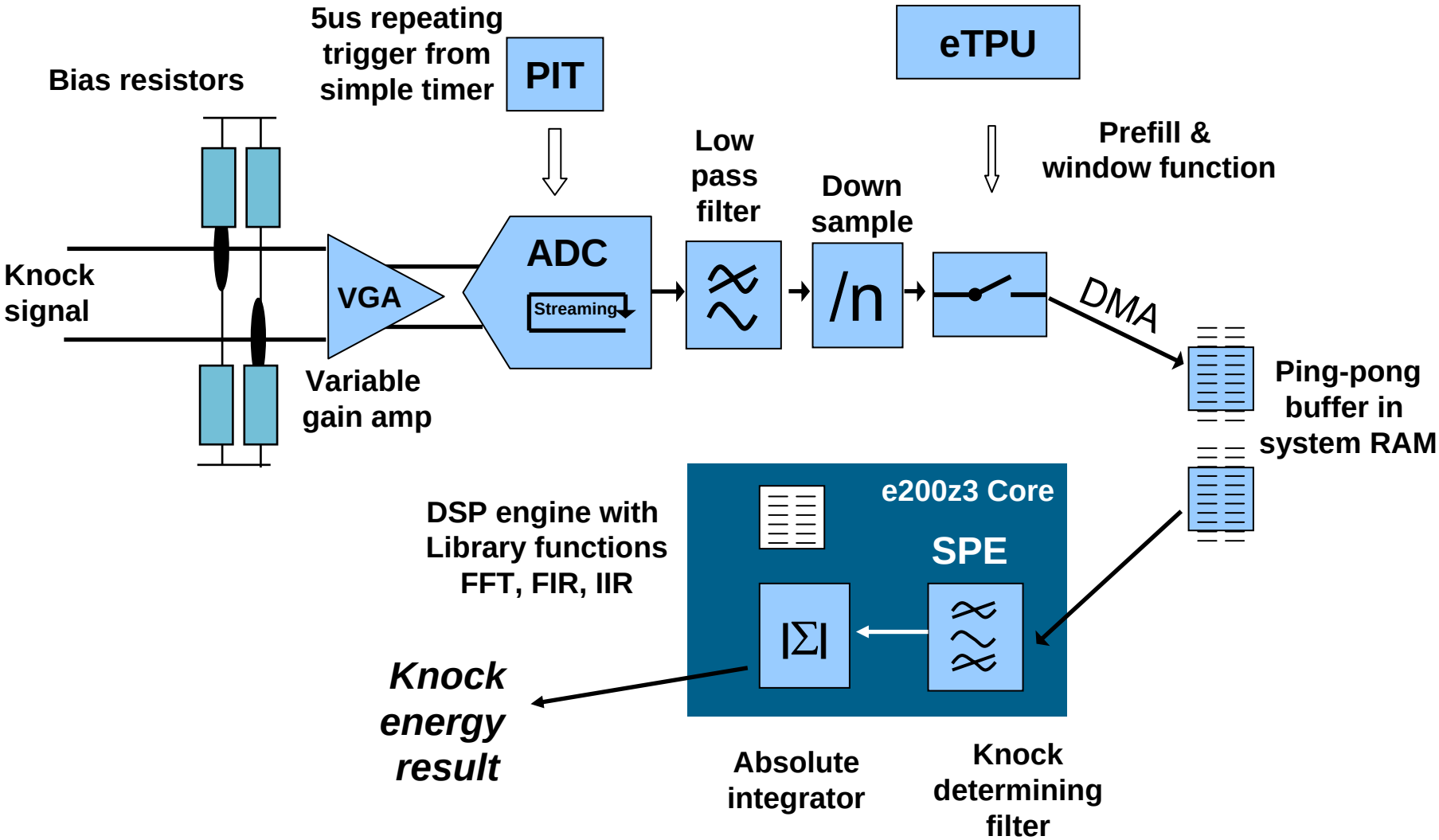
Software DSP Solution using MPC563xM



For more information, attend the following session:
FTF-AUT-F0354 Reducing System Cost with Integrated MCU Solutions for Engine and Transmission Applications

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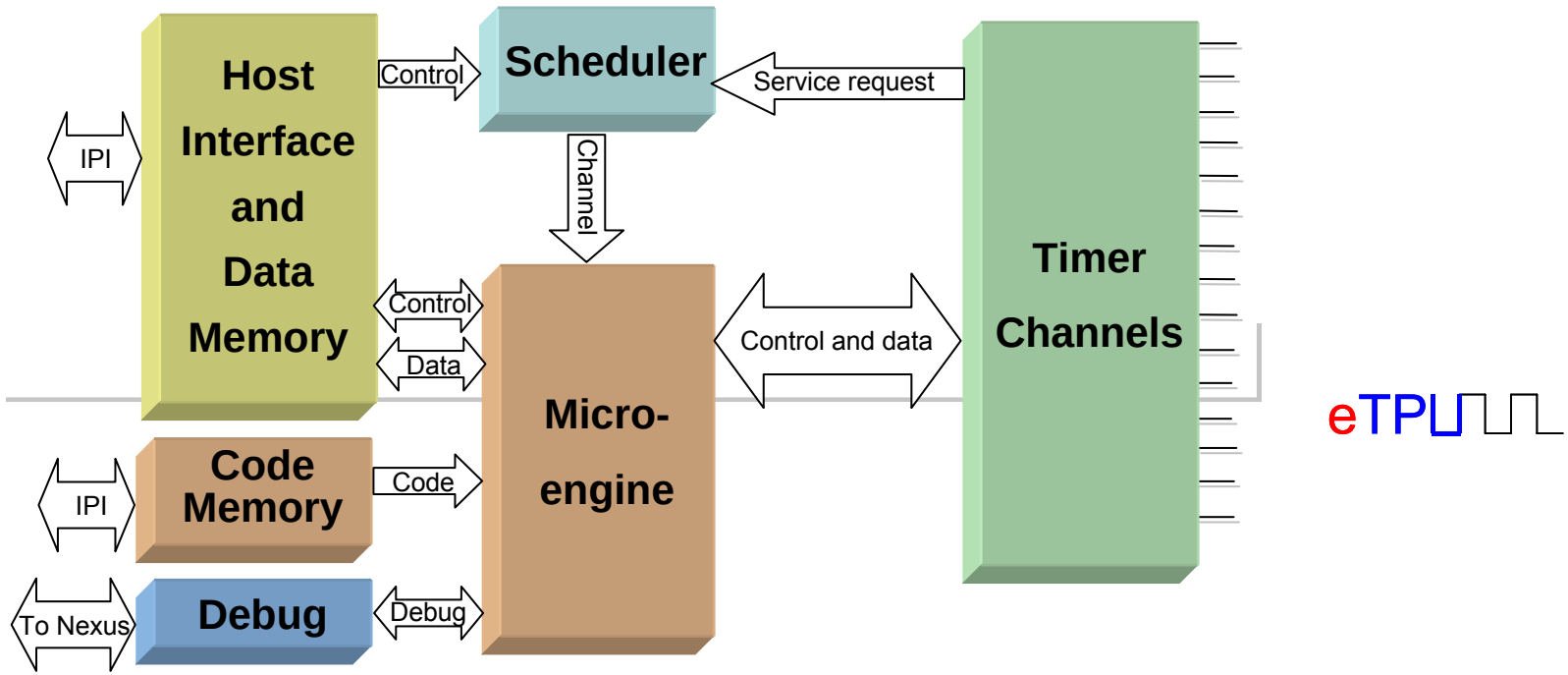
What is an eTPU?

The ***enhanced time processor unit*** is a programmable I/O controller with its own core and memory system, allowing it to perform complex timing and I/O management ***independently*** of the CPU. The eTPU is essentially a microcontroller all by itself!



For more information, attend the following session:
FTF-AUT-F0447 Using Enhanced Time Processing Unit (eTPU/eTPU2) for Combustion Engine Management and Electric Motor Control

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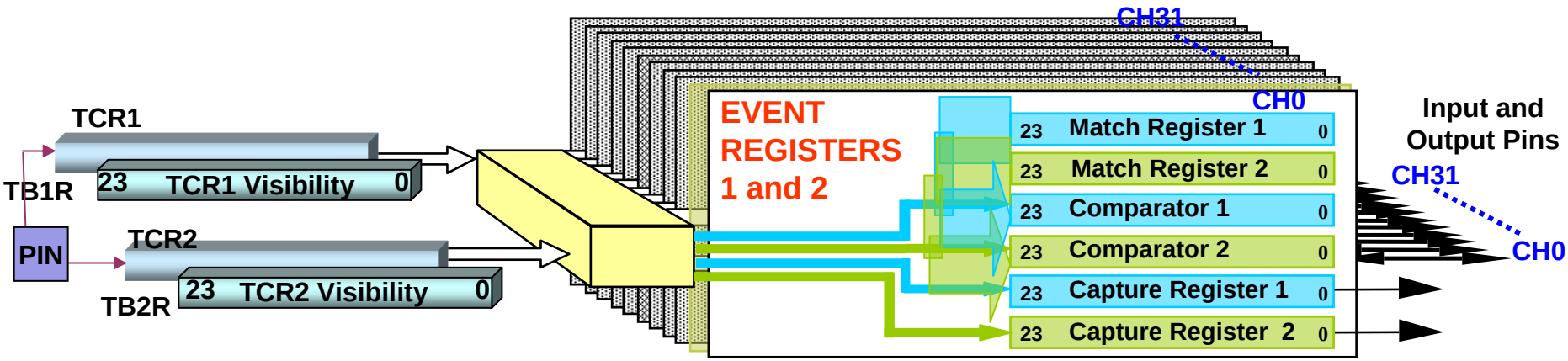
eTPU Basics: Channel Features

- Each channel has its own I/O pins and two interacting sets of event registers
- Each event register set consists (in part) of
  - a 24-bit match register
  - a 24-bit capture register
  - a 24-bit greater-than-or-equal, or equal, comparator



- Setting up for match and transition events is done in microcode
- A match is synchronized to one of the two 24-bit free-running Timer Count Registers, TCR1 or TCR2
- A capture is synchronized to one of the two 24-bit free-running Timer Count Registers, TCR1 or TCR2

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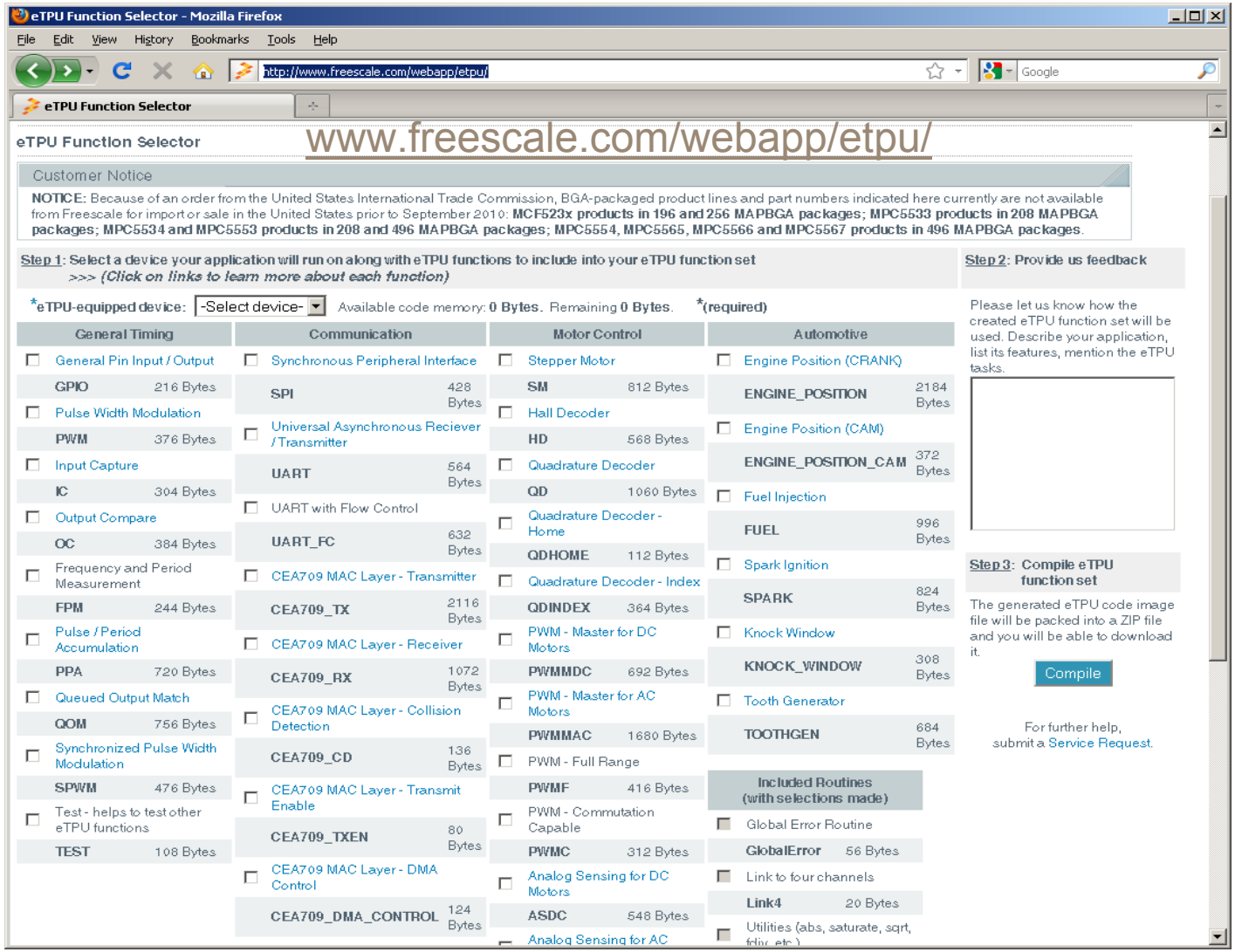
Online Tool for Compiling Libraries of Selected Functions

Select device

Select desired functions

Tool compiles the functions in real time

ZIP file provided for download



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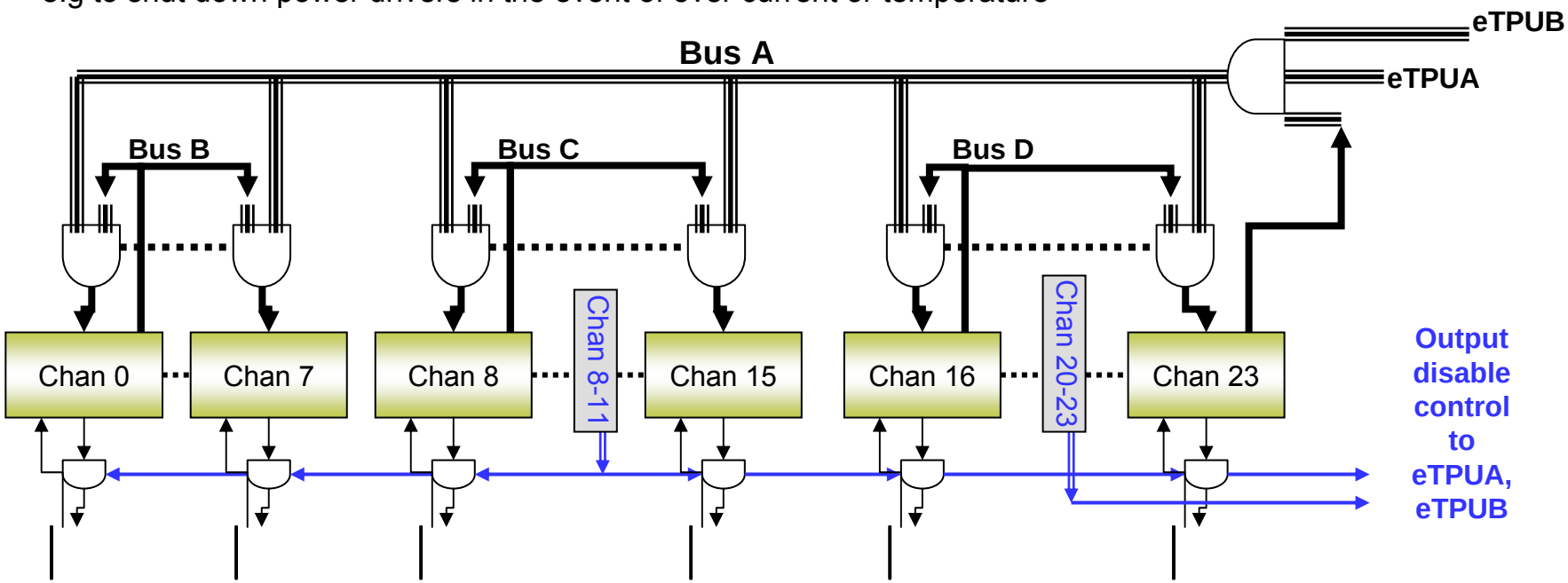
Presentation Agenda

- Session Objectives
- MPC56xx Roadmap and MPC567xF Overview
- Power Supplies
- Clock Modes
- Analog to Digital Converter
- eTPU
- **eMIOS**
- BAM Controlled Startup
- Other Peripherals
- Pin Configuration
- Debug Features
- Hardware Checklist
- SmatMOS Companion Devices

eMIOS Features

- Provides various hardware timing modes to create or measure real-time signals
- 32 channels, 24 bit resolution, 200 MHz max operation
- Programmers model is consistent with MPC5500 family eMIOS implementations
- Programmable clock prescalers (global and per channel)
- DMA request for each channel
- Programmable input filter
- Channels can be individually disabled to assist with power saving
- Four channels provide high speed hardware shut-down of other timed I/O
  - e.g to shut down power drivers in the event of over current or temperature



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eMIOS Functions

- Input Channel Modes
  - Single action input capture
  - Input pulse width measurement
  - Input period measurement
  - Pulse/edge accumulation
  - Pulse edge counting
  - Quadrature decode
  - Windowed programmable time accumulation modulus counter

- Output Channel Modes
  - Single action output compare
  - Double action output compare
  - Output pulse width modulation
  - Output pulse width and frequency modulation
  - Center aligned output pulse width modulation with dead time insertion

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Boot Assist Module Introduction

- The Boot Assist Module's (BAM) primary function is to perform essential system initialization and to locate and execute the application code.

- BAM initialisation is sub-optimal for performance
  - Cache off, max wait states, default XBAR, no BTB, etc.

- BAM tasks:
  - Initial e200z7 core MMU setup with minimum address translation for all internal MCU resources
  - Configuration of MMU to boot as either Classic PowerPC Book E code (default) or as Freescale VLE code
  - Location and detection of user boot code
  - Automatic switch to Serial Boot mode if internal flash is blank or invalid
  - User-programmable 64-bit password protection for serial boot mode
  - Boot user code from internal Flash module
  - Serial boot by loading user program via CAN bus or eSCI to the internal SRAM
  - Censorship protection for internal flash module
  - Option to use the e200z7 core watchdog timer or the system watchdog timer (SWT)

Censorship Control

BOOTCFG	Censorship Control 0x00FF_FDE0	Serial Boot Control 0x00FF_FDE2	Boot Mode Name	Internal Flash State	Nexus State	Serial Password
0	!0x55AA	Don't care	Internal - Censored	Enabled	Disabled	Flash
	0x55AA		Internal - Public	Enabled	Enabled	Public
1	Don't care	0x55AA	Serial - Flash Password	Enabled	Disabled	Flash
		!0x55AA	Serial - Public Password	Disabled	Enabled	Public

- Public password H/W fixed value: 0xFEED_FACE_CAFE_BEEF
- Flash password user defined – set to 0xFEED_FACE_CAFE_BEEF as default
- Depending on the values stored in the censorship word and serial boot control word in the shadow row of the internal flash memory:
  - The internal flash memory can be enabled or disabled
  - The Nexus port can be enabled or disabled
  - The password received in the serial boot mode is compared with the fixed public or user password

Flash: Shadow Block

- Censorship control word is programmed at manufacturing to 0x55AA_55AA
  - Device is not censored and uses a flash password for serial boot mode
- Serial password in shadow block is used when the public password
  - 0xFEED_FACE_CAFE_BEEF is not used

Address	Shadow Use	Block	Size (bytes)	Partition
0x00FF_8000- 0x00FF_FDD7	General Use	S	472	All (Shadow behaves as if it is in all partitions)
0x00FF_FFD8	Serial Password		8	
0x00FF_FDE0	Censorship Control + Serial Boot Control		4	
0x00FF_FDE4	General Use		4	
0x00FF_FDE8	FLASH_LML reset configuration		4	
0x00FF_FDEC	General Use		4	
0x00FF_FDF0	FLASH_HBL reset configuration		4	
0x00FF_FDF4	General Use		4	
0x00FF_FDF8	FLASH_SLL reset configuration		4	
0x00FF_FDFC to 0x00FF_FFFF	General Use		516	

CAUTION: Use extreme caution when erasing both censorship control word and the serial password OR ELSE the flash will become permanently disabled

Serial Boot Mode - eSCI

- Baud rate based on crystal frequency
- eSCI serial boot mode protocol
  - Download 64-bit password
  - Download start address, size of download and VLE bit
  - Download data
  - Execute code from start address

Protocol Step	Host Sent Message	BAM Response Message	Action
1	64-bit password MSB first	64-bit password	Password checked for validity and compared against stored password. e200z3 Watchdog timer is refreshed if the password check is successful.
2	32-bit store address + 31-bit number of bytes (MSB first) + VLE bit	32-bit store address + 31-bit number of bytes + VLE bit	Load address and size of download are stored for future use. Use VLE bit to determine whether the MMU entry for the SRAM is configured to run Book E or VLE code.
3	8 bits of raw binary data	8 bits of raw binary data	Each byte of data received is store in MCU memory, starting at the address specified in the previous step and incrementing until the amount of data received and stored, matched the size as specified in the previous step.
4	None	None	The BAM returns IO pins and eSCI module to their reset state, with the exception that eSCI_A_CR2[MDIS] is asserted rather than negated. Then it branches to the first address the data was stored to (as specified in step 2).

Flash: Serial Password Rules

- 64-bit serial password must have at least one ‘1’ & one ‘0’ in each half word ‘lane’

Valid Passwords

0x0001_0001_0001_0001

0xFFFE_FFFE_FFFE_FFFE

0x1xxx_x2xx_xx4x_xxx8

0xxxxE_xxDx_xBxx_7xxx

Invalid Passwords

0x**0000**_xxxx_xxxx_xxxx

0x**FFFF**_xxxx_xxxx_xxxx

0xxxxx_**0000**_xxxx_xxxx

0xxxxx_**FFFF**_xxxx_xxxx

0xxxxx_xxxx_**0000**_xxxx

0xxxxx_xxxx_**FFFF**_xxxx

0xxxxx_xxxx_xxxx_**0000**

0xxxxx_xxxx_xxxx_**FFFF**

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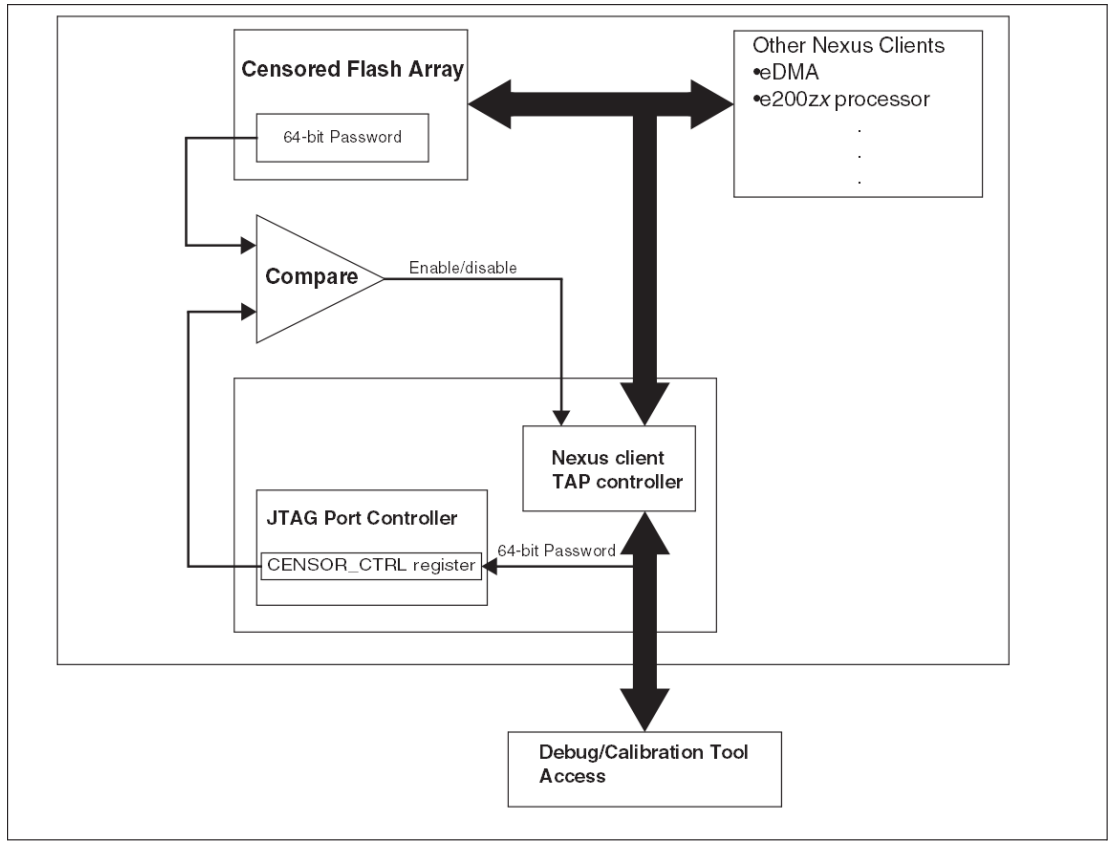
JTAG Serial Password Mechanism for Granting Temporary Access to the Secured Flash Memory Array

- When security is enabled, external accesses to the flash memory array and debug access is prohibited.
- Provides the means to temporarily access the flash array and maintains a high level of security through the use of a 64-bit password.
- Permits users with knowledge of the password stored in internal flash to use existing tools to perform debug and calibration on devices with a secured flash array.
- Flash security re-enabled on next reset.



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Communication Peripherals

- eSCI – Provides serial communications such as LIN, K-Line, and RS232
  - Three modules are available in the MPC567xF
- FlexCAN – Controller Area Network interface provides up to 1 Mbps automotive
  - Four modules available in the MPC567xF
  - CAN module supports both CAN2.0A and CAN2.0B specifications
  - 64 message buffers per module
- DSPI – Serial Peripheral Interface (SPI)
  - Four modules are available on the MPC567xF
  - Supports 32-bit MicroSecond Bus Interface with LVDS output up to 40 MHz

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Pad Configuration Register

- 16-bit register (some pads don't have a register)
- Reset values vary depending on pad type

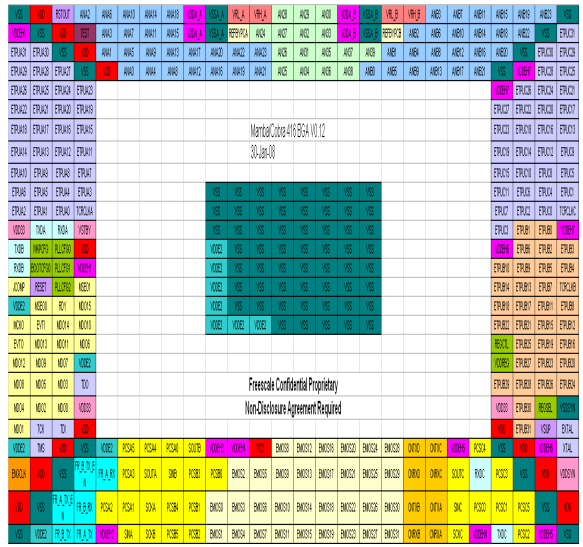
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	0	PA[1]			OBE[2]	IBE[3]	DSC		ODE[4]	HYS[5]	0	0	WPE[6]	WPS[6]
W																
RESET:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

Bit Field Name	Symbol	Description
Pad Assignment	PA	Assigns pad as GPIO (common default), alternate or primary function
Output Buffer Enable	OBE	If pad can be input or output, enables as output
Input Buffer Enable	IBE	If pad can be input or output, enables as input. If pad is configured as output, enables reading pad state
Drive Strength Control	DSC	Output drive strength of 10, 20, 30 or 50 pf
Open Drain Output Enable	ODE	Output has open drain
Input Hysteresis	HYS	Input has Hysteresis (for noise, but slower)
Slew Rate Control	SRC	Output has minimum, medium or maximum slew rate (Reset default is max. slew rate)
Weak Pull Down/Up Enable	WPE*	Enables selected pull down/up
Weak Pull Down/Up Select	WPS*	0= pull down, 1 = pull up

Pad Function Selector

- Unlike prior microcontrollers in this class, the required pin function is selected by a fixed size of PA bit field in each PCR

PA	Function Category
000	GPIO
001	Primary Function (normal default function after reset)
010	Function 2
011	Function 3
100	Function 4



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MPC567xF Typical Pin Multiplexing

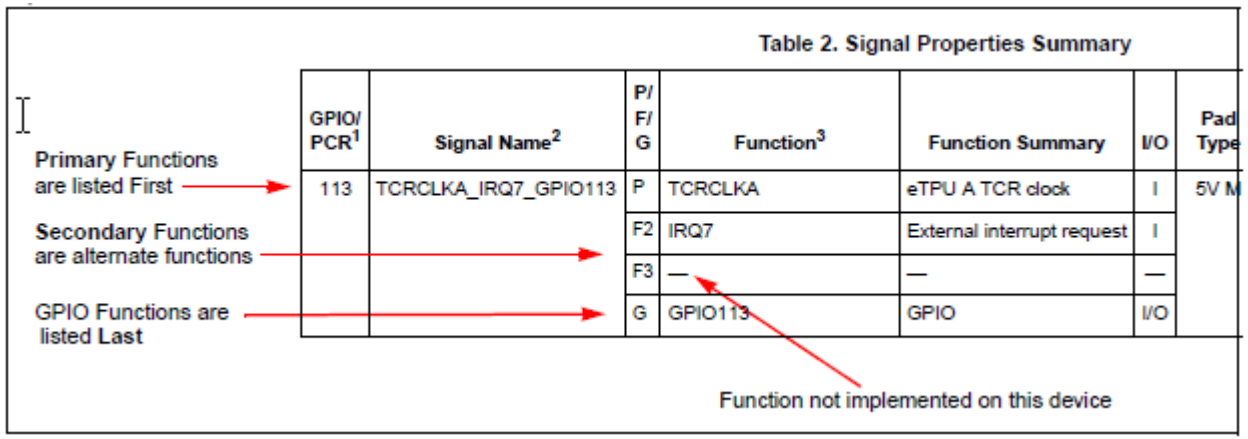

Table 2. Signal Properties Summary

GPIO/PCR[1]	Signal Name[2]	P/F/G	Function[3]	Function Summary	I/O	Pad Type
113	TCRCLKA_IRQ7_GPIO113	P	TCRCLKA	eTPU A TCR clock	I	5V M
		F2	IRQ7	External interrupt request	I	
		F3	—	—	—	
		G	GPIO113	GPIO	I/O	

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]	State after RESET[8]	Package Location 416	Package Location 516
eTPU_A											
113	TCRCLKA_IRQ7_ GPIO113	P	TCRCLKA	eTPU A TCR clock	I	MH	V_{DDEH1}	—/Up	—/Up	L1	K4
		A1	IRQ7	External interrupt request	I						
		A2	—	—	—						
		G	GPIO113	GPIO	I/O						
114	ETPUA0_ETPUA12_ GPIO114	P	ETPUA0	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG	—/WKPCFG	L2	L6
		A1	ETPUA12	eTPU A channel (output only)	O						
		A2	—	—	—						
		G	GPIO114	GPIO	I/O						

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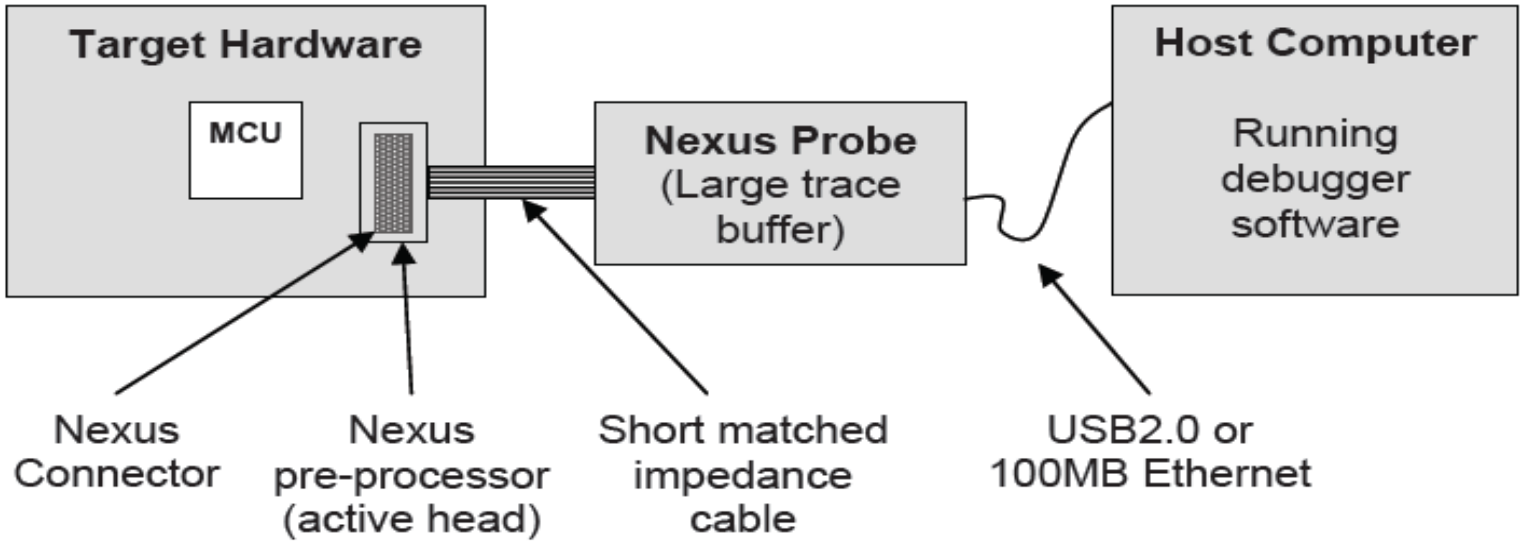
Nexus Debug Overview



- Tracing is the physical mechanism of capturing real time, non-intrusive information from the MCU via the Nexus module and transmitting this to the development tool where it is stored
- Nexus probes contain large amounts of memory dedicated to trace (256 MB to 1 GByte)
- Once captured, trace data is transmitted to the host computer for post processing

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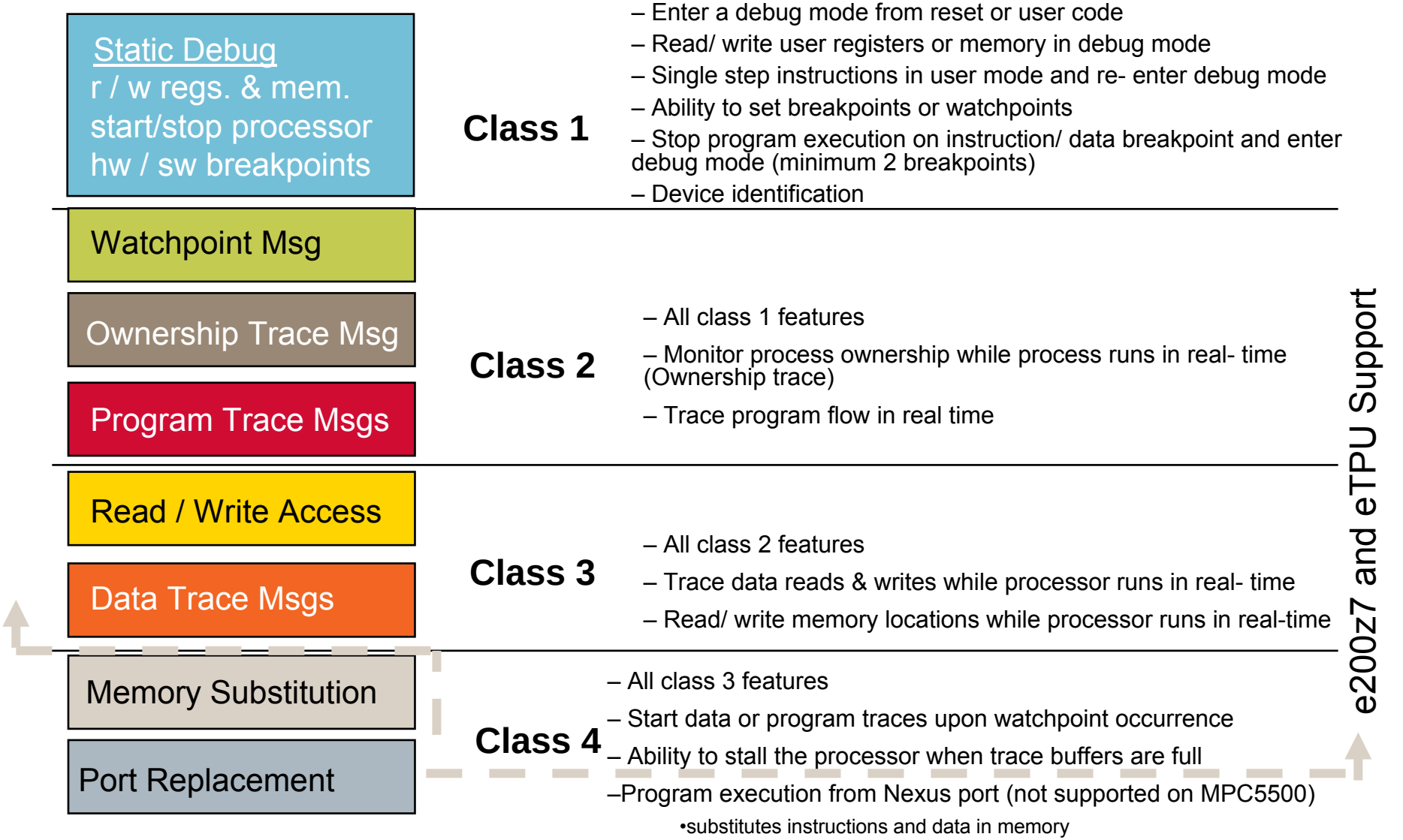
IEEE-ISTO 5001-2001 Nexus Classes of Features



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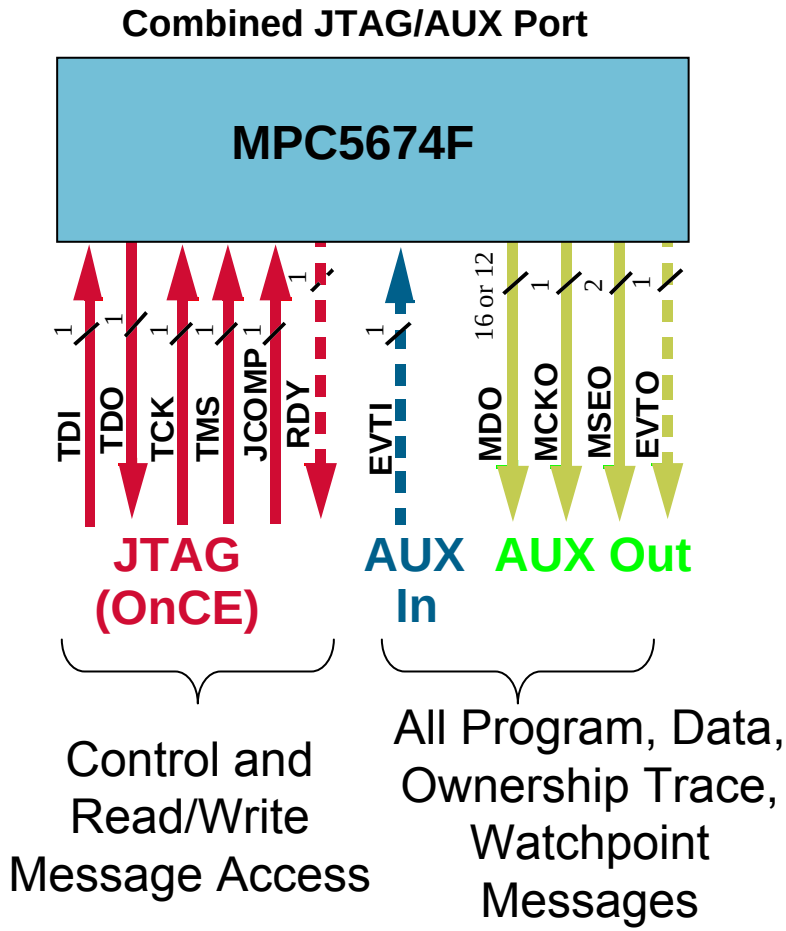
JTAG/Nexus Interface

- Reduced port mode
  - Uses a total of 23 pins
- Full port mode
  - Uses a total of 27 pins – 16 MDO pins multiplexed with GPIO[75:81]
- JTAG only mode
  - Only uses 6 pins
  - Class 1 plus R/W access from class 3 (no trace)
  - Enables low cost tools!
- Program & data trace can be performed, even on production modules with reduced or full port.
  - No bus access required.
  - No loss in performance
- JCOMP is used in place of TRST, RDY is used for R/W access



Nexus/JTAG Minimum Connector Definition

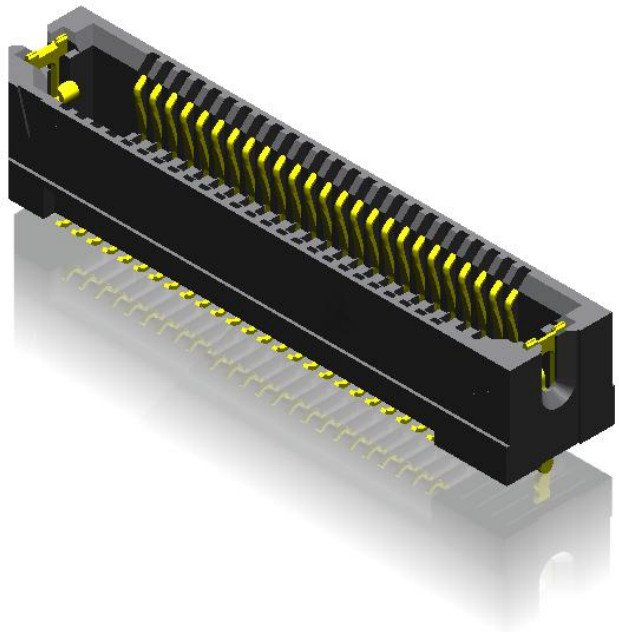
- Freescale recommends the 38-pin MICTOR connector for the Nexus port. However, for constrained board layouts, a 14-pin connector can be used.

Description	Pin	Pin	Description
TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
/EVTI	7	8	_
RESET	9	10	TMS
VDDE7	11	12	GND
/RDY	13	14	JCOMP

- /EVTI was not in the original definition, but allows additional capability to tools. Check with your tool vendor for support. Having /EVTI on the connector causes no issues for debuggers that do not use it.

Nexus Interface Port

- For 12-bit or 16-bit MDO port mode the following Nexus connector is recommended:
  - HP50 (ASP-148422-01) by Samtec (2 rows with 25 pins each; 0.8 mm pitch)
  - Supported by Lauterbach
- Freescale can provide example schematics



ob/rd

Nexus Signals

Table 4. MPC56xx High Speed Parallel Trace Connector

Position	Signal	Direction[1]	Pin Number	Pin Number	Direction[1]	Signal	IEEE-5001-2010 GEN_IO Signal Name
	GND[2]					GND[2]	
1	MSEO0	Out	1	2	Out[3]	VREF	
2	MSEO1	Out	3	4	In	TCK	
3	GND		5	6	In	TMS	
4	MDO0	Out	7	8	In	TDI	
5	MDO1	Out	9	10	Out	TDO	
6	GND		11	12	In	JCOMP	
7	MDO2	Out	13	14	Out	RDY	
8	MDO3	Out	15	16	In	EVTI	
9	GND		17	18	Out	EVTO	
10	MCKO	Out	19	20	In	RESET	
11	MDO4	Out	21	22	Out	RSTOUT	GEN_IO0
12	GND		23	24		GND	
13	MDO5	Out	25	26	Out	CLKOUT	
14	MDO6	Out	27	28	In/Out	TD/WDT	GEN_IO1
15	GND		29	30		GND	
18	GND		35	36		GND	
19	MDO9	Out	37	38		ARBREQ	GEN_IO4
20	MDO10	Out	39	40		ARBGRT	GEN_IO5
21	GND		41	42		GND	
22	MDO11	Out	43	44	Out	MDO13	
23	MDO12	Out	45	46	Out	MDO14	
24	GND		47	48		GND	
25	MDO15	Out	49	50		N/C[4]	
	GND[2]					GND[2]	

1. Viewed from the MCU.
2. The connector locking mechanism provides additional ground connections on each end of the connector.
3. This is an output from the connector standpoint. It may or may not be from the MCU.
4. No connection - should be left open. Reserved for MDO16 on devices with more than 16 MDO signals (future compatibility). In some applications, this may be used a an SRAM voltage detect to determine when voltage for a standby SRAM is taken away.

- ARBREQ and ARBGRT are for arbitration of multiple tools (when 2 tools are required to be used together). May not be needed for this device.
- TD/WDT can be used to disable any on-board external watchdog circuit when debugger is attached.
- DAI1/2 are generic signal pins that can be defined between the tool vendor and the customer for specific needs if required.

MPC56874F MICTOR Nexus Connector Definition

MPC5600 signal	Combined M38C or M38-2C	Direc-tion	Pin number		Pin number	Direc-tion	Combined M38C or M38-2C	MPC5600 signal
MDO12	Reserved	Out	1	Ground	2	Out	Reserved	MDO13
MDO14	Reserved	Out	3		4	Out	Reserved	MDO15
MDO9	VEN_IO0	Out	5		6	Out	CLOCKOUT	CLKOUT
BOOTCFG1	VEN_IO2	In	7		8	Out	VEN_IO3	MDO8
$\overline{\text{RESET}}$	/RESET	In	9		10	In	/EVTI	$\overline{\text{EVTI}}$
TDO	TDO	Out	11		12	-	VREF	VDDE7
MDO10	VEN_IO4	Out	13		14	Out	/RDY	$\overline{\text{RDY}}$
TCK	TCK	In	15		16	Out	MDO7	MDO7
TMS	TMS	In	17	Ground	18	Out	MDO6	MDO6
TDI	TDI	In	19		20	Out	MDO5	MDO5
JCOMP	/TRST	In	21		22	Out	MDO4	MDO4
MDO11	VEN_IO1	Out	23	Ground	24	Out	MDO3	MDO3
$\overline{\text{RSTOUT}}$	TOOL_IO3	Out	25		26	Out	MDO2	MDO2
TD/WDT	TOOL_IO2	-	27		28	Out	MDO1	MDO1
ARBGRT	TOOL_IO1	-	29		30	Out	MDO0	MDO0
12 volts	UBATT	-	31		32	Out	/EVTO	$\overline{\text{EVTO}}$
12 volts	UBATT	-	33		34	Out	MCKO	MCKO
ARBREQ	TOOL_IO0	-	35		36	Out	/MSEO1	$\overline{\text{MSEO1}}$
VSTBY	VALTREF	-	37		38	Out	/MSEO0	$\overline{\text{MSEO0}}$

- Note: For 16-bit wide Nexus trace, Freescale will be proposing to tool vendors that the new IEEE-5001 2009 SAMTEC connector definition be used for 16 MDO connections.
  - The SAMTEC connector is physically smaller and provides isolation between high speed trace and the low speed control signals.
- Lauterbach currently supports the 16-MDO configuration on some of their new debug probes.

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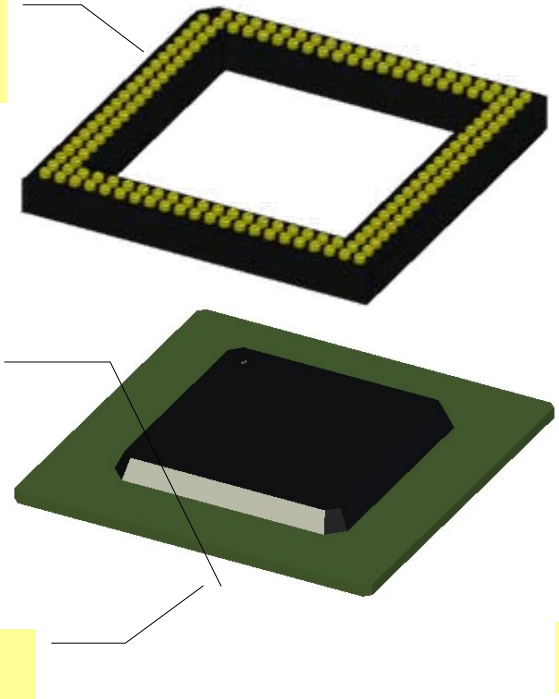
The *VertiCal* Base Solution

VertiCal Connector
159 pins

Chip Scale
Package (with
production die)

VertiCal Base Board



Replaces the production
BGA package

VertiCal Base

- The ***VertiCal*** Base replaces the production microcontroller BGA package and provides a standardized 159-pin tool connector.
- The ***VertiCal*** Base is footprint-compatible with the production BGA.

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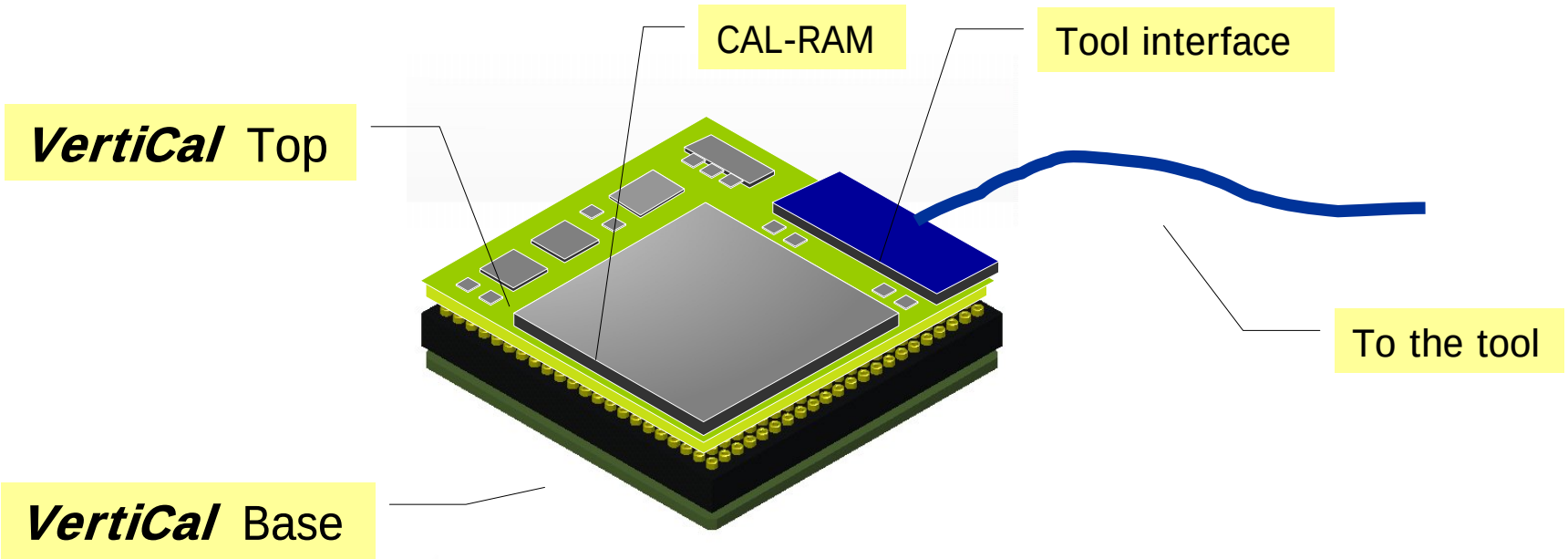
VertiCal Calibration System – Tool Top



- The ***VertiCal*** Top could be any type of tool adaptation and plugs into the 156-pin tool connector
- The ***VertiCal*** Top typically contains the CAL-RAM and the tool interface

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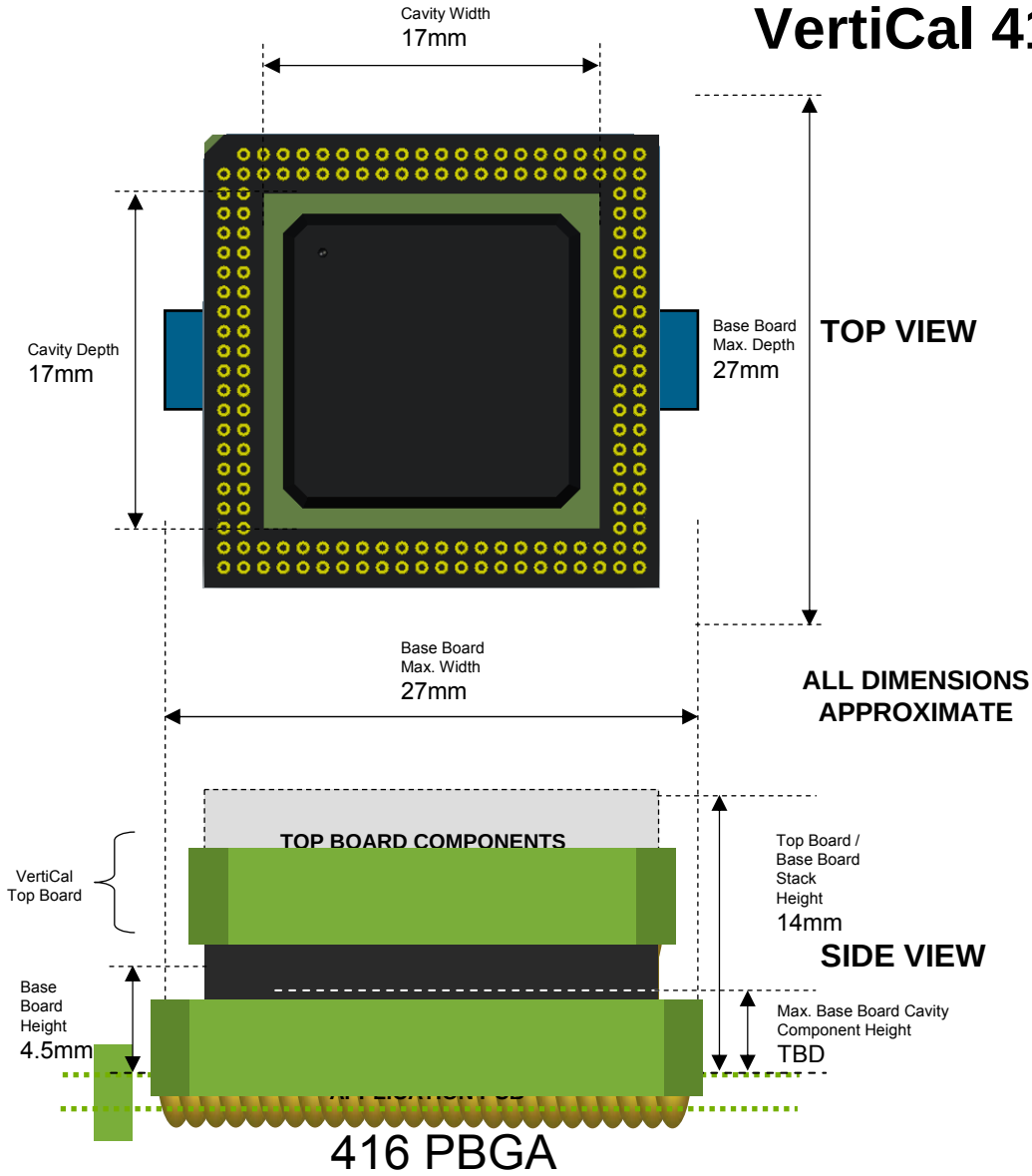
VertiCal 416 Mechanical



Debug Features Summary

- **e200z7 debug capability**
  - Fully Nexus Class 3 compliant (IEEE-ISTO 5001-2001 standard)
  - 8 instruction address break/watch points
  - 4 data address break/watch points
  - 2 data value break/watch points
  - 4 data trace window regions (within or outside the defined region)
  - Synchronize cross linked breakpoints between the e200z7 and the eTPU cores
- **eTPU2 debug capability**
  - Full Nexus Class 1 debug support (via JTAG)
  - Full Nexus Class 3 trace capability (ownership, program, and data trace)
  - 2 hardware break/watch points per engine
  - 4 data trace window regions (within or outside the defined region) – shared between 2 engines, 4 independent regions available on 3rd eTPU
- **eDMA trace (each eDMA engine)**
  - 2 data address watchpoints (read, write, or read/write)
  - 2 data trace window regions (within or outside the defined region)
- **FlexRay trace**
  - 2 data address watchpoints (read, write, or read/write)
  - 2 data trace window regions (within or outside the defined region)
- **Trace buffers will be deep enough for 128 messages per core**
- **Tool synchronization supported**

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- eMIOS
- BAM Controlled Startup
- Other Peripherals
- Pin Configuration
- Debug Features
- **Hardware Checklist**
- SmatMOS Companion Devices

MPC5674F Digital IO Pad Charateristics

- The MPC5500 family implement three primary types of pads: fast, medium, slow
- The medium pads implement slew rate control (no slow pads)
  - Slew rate should be limited for the maximum frequency of the intended use
  - Medium pad rise/fall times are settable to:
    - 5 ns maximum
    - 12 ns maximum
    - 70 ns maximum
- Fast pad types (1.2 ns rise/fall) implement drive strength, are used on the following:
  - EBI
  - Nexus
- Fast pads with slew rate control
  - FlexRay
    - 1.1 ns
    - 2.4 ns
    - 5 ns
    - 16 ns
- Refer to IBIS models and data sheet information for more detailed information on IO characteristics

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Signal Integrity Recommendations

- Software
  - Match drive strength selection to application load
  - Use the slowest drive strength that the signal can withstand

- Hardware
  - Route bus signals with controlled impedance
  - Use termination resistors on bus signals
  - Minimize board propagation delay
  - Avoid routing stubs
  - Use good decoupling techniques
  - Use a good layer stackup

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Hardware Checklist

- Review the return path of all signals. The signal return will take the path of least impendence.
- The correct number and size of decoupling capacitors have been used on the VDD power supply.
- The 10-nF or higher capacitors are in low ESL packages such as the 0306 package.
- The 10-nF capacitors are located as close as possible to the VDD balls.
- The 10-nF capacitors are distributed evenly around the device (for example, two capacitors per corner).
- The VDD balls on the device are connected to the 10-nF capacitors using a power plane or wide traces including many vias.
- There is at least one ground plane. Include isolated grounds on other layers.
- Bypass across power/ground discontinuities. Include thermal release for these transitions.
- For single-chip applications, a minimum of four layers are used. For expanded mode applications, a minimum of six layers are used.
- There is at least one power plane; mixed voltage power plane is acceptable.
- The power and ground planes have been checked for structures which obstruct the flow of current, such as via anti-pads and embedded slots or traces.
- The oscillator circuit should have a compact layout.

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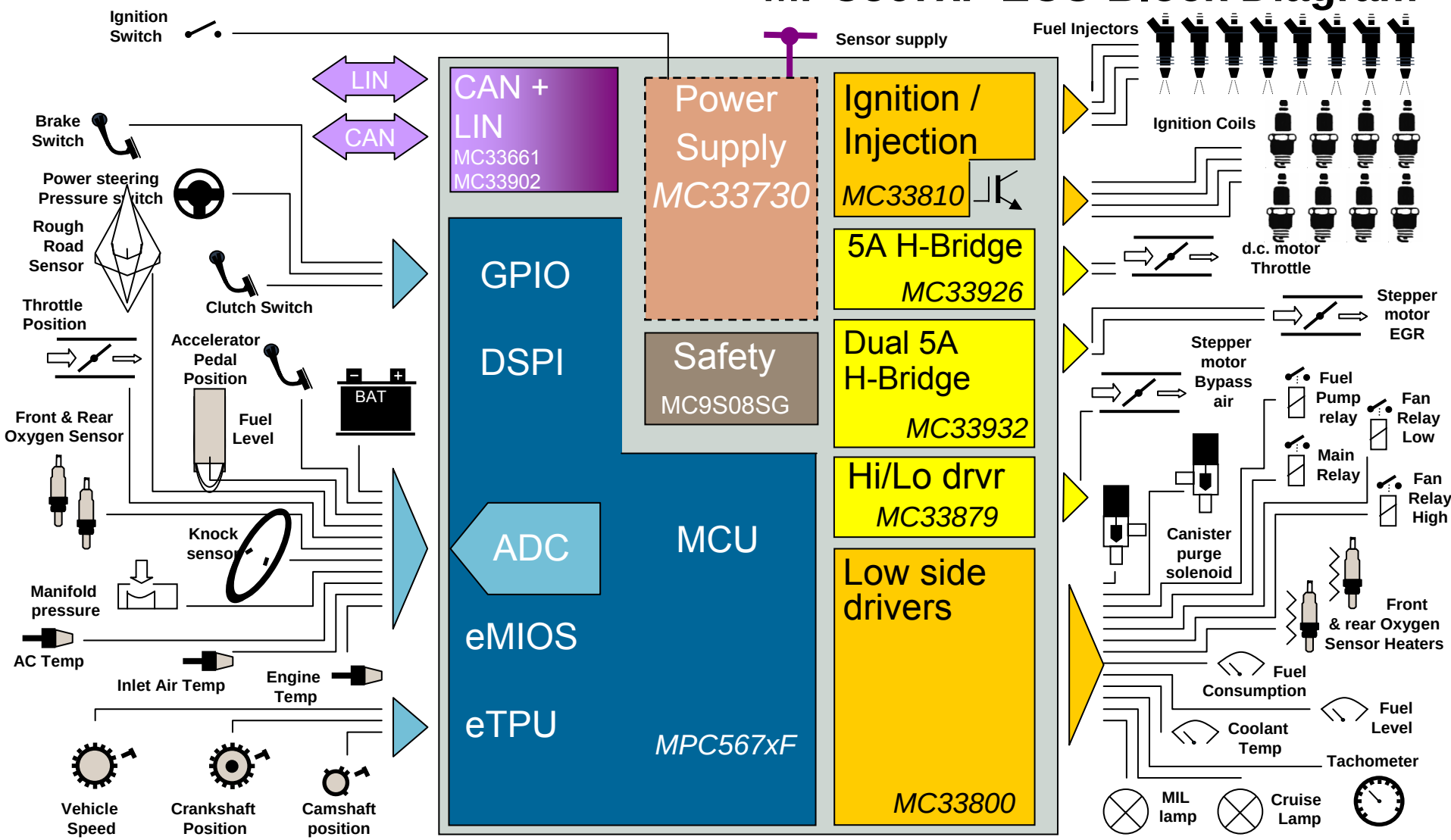
Presentation Agenda

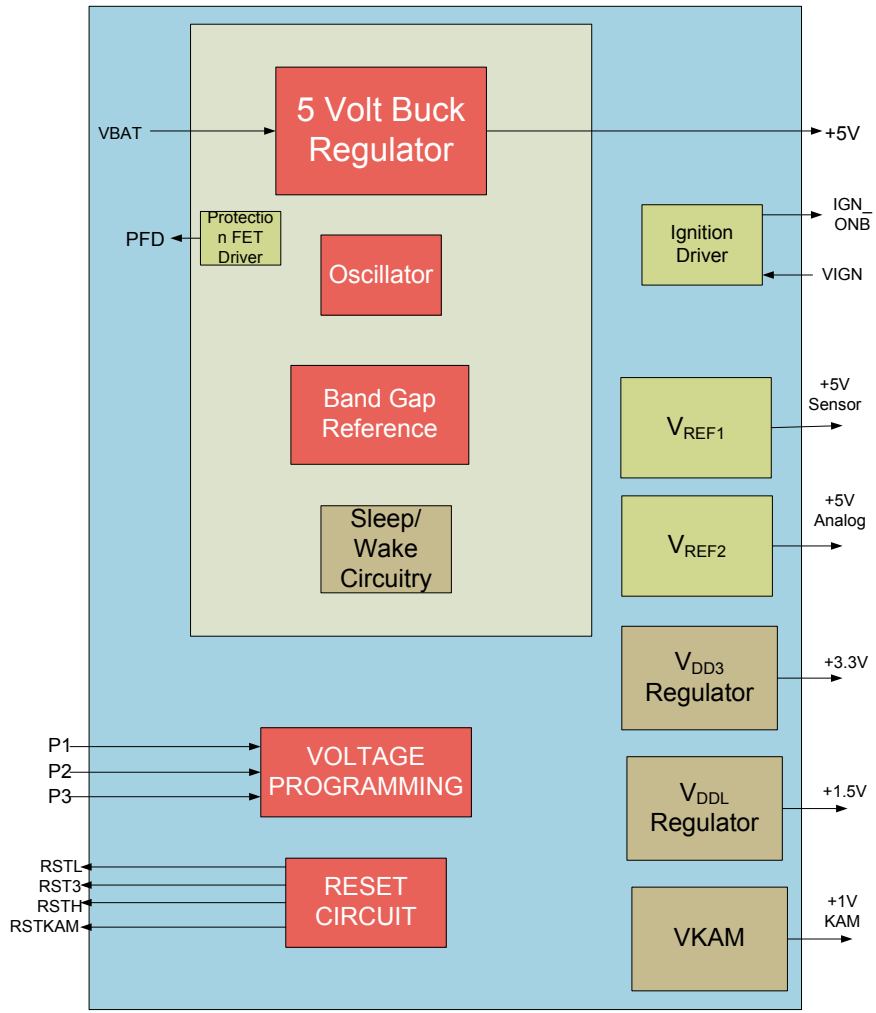
- Session Objectives
- MPC56xx Roadmap and MPC567xF Overview
- Power Supplies
- Clock Modes
- Analog to Digital Converter
- eTPU
- eMIOS
- BAM Controlled Startup
- Other Peripherals
- Pin Configuration
- Debug Features
- Hardware Checklist
- **SmatMOS Companion Devices**

MPC567xF ECU Block Diagram



MC33730 Automotive Power Supply IC: Block Diagram

- Switch mode power supply with multiple linear regulators
  - +5V switching buck regulator with adjustable frequency and slew rate
  - Two linear regulators with programmable voltage
    - VDD3
    - VDDL
  - Two isolated voltage references
    - VREF1
    - VREF2
  - Reset circuit with outputs for all four supplies and a programmable timer
  - Sleep mode with keep alive supply
  - Reverse battery protection FET drive
  - Self protection for:
    - Over current
    - Over temperature



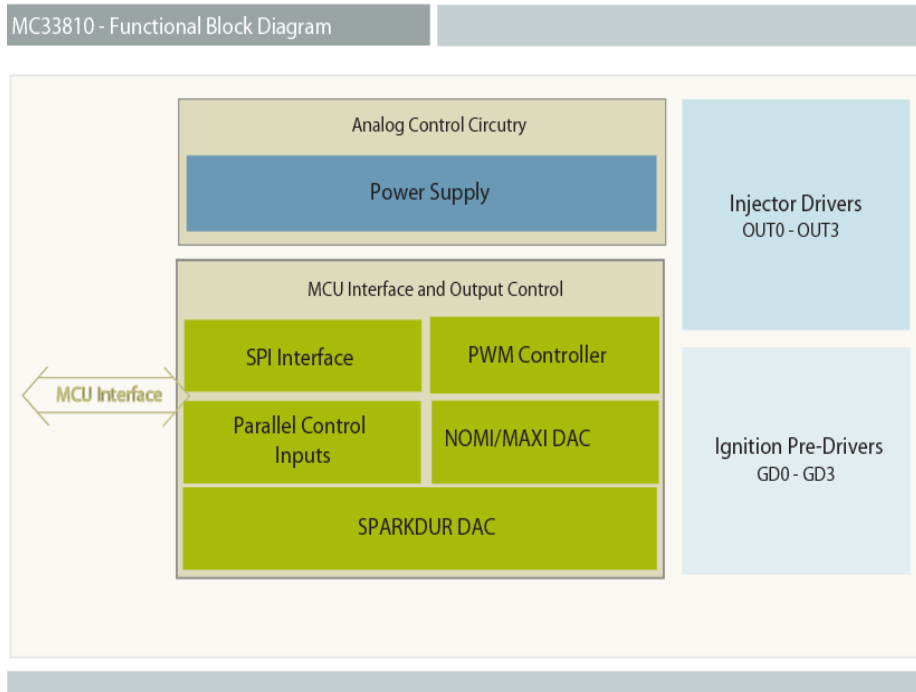
MC33810: Eight Channel Ignition and Injector Driver

Features

- Eight channels with 4 low-side drivers and 4 pre-drivers
- Pre-drivers with three different modes:
- Ignition
- General purpose gate drive
- Two devices can support up to ten cylinders
- Ignition current and spark detection with programmable thresholds
- MCU SPI and parallel interface
- Power supply/oscillator/band gap reference/POR
- Diagnostic and error detection logic
- Self protection for:
  - Shorts to battery
  - Over current and Over temperature detection
- Low power (30 µA) “sleep mode”

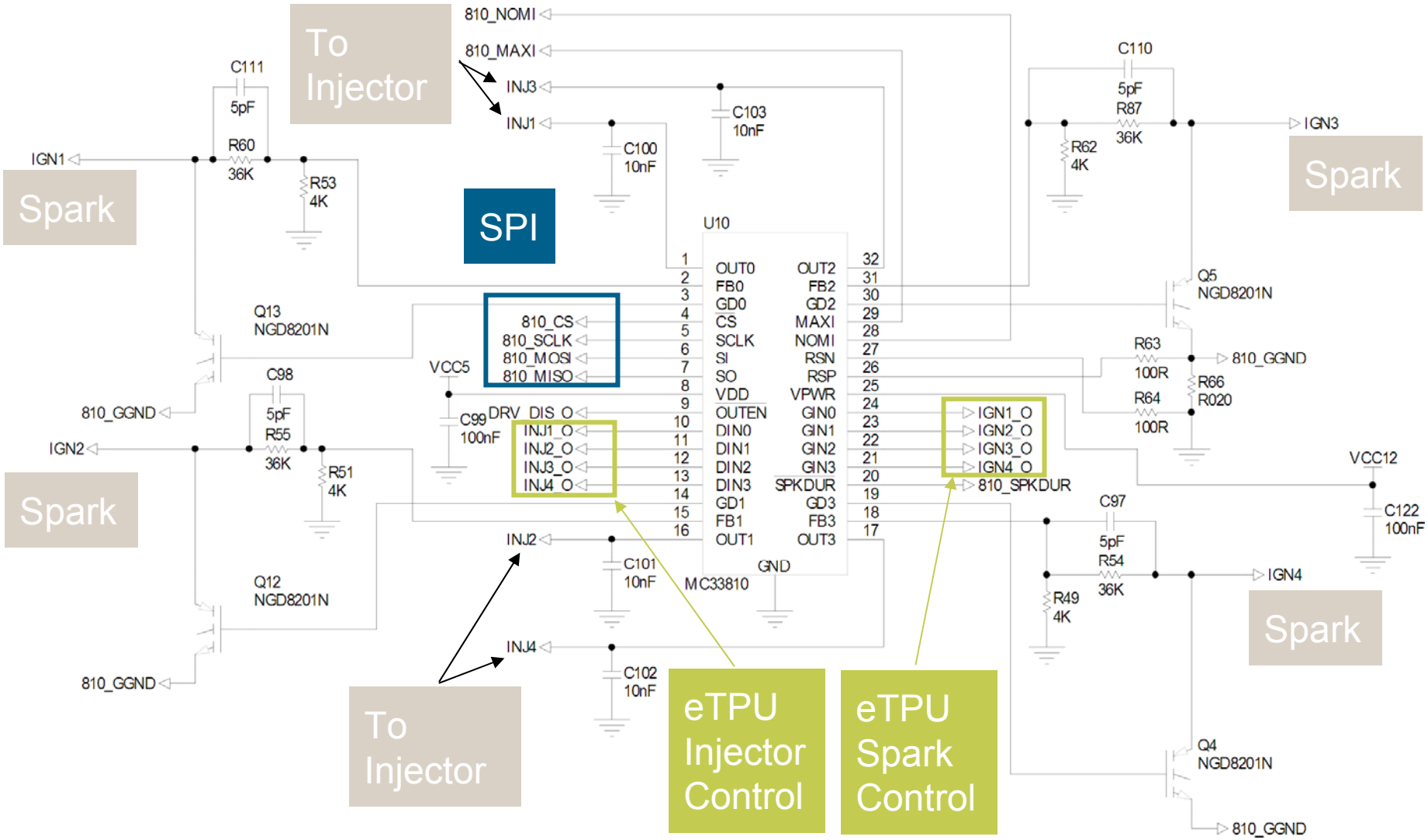
Benefits

- Highly integrated solution minimizes the need for additional external discrete components
- Reduced parts count
- Reduced manufacturing and test cost
- Improved reliability
- Reduced current consumption lowers battery drain during key off
- Small footprint, reduces printed circuit board area
- Simple MCU parallel interface
- Protected against common failure conditions



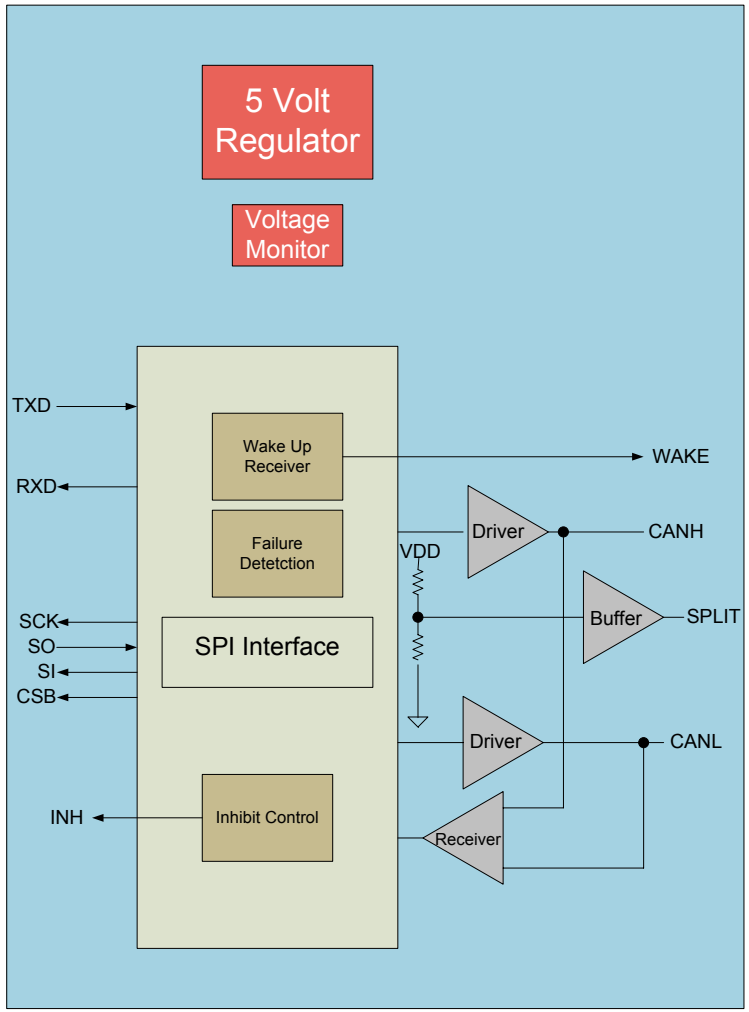
EK (Pb-FREE) SUFFIX
32-PIN SOICW EP

Example Schematic: MC33810 Ignition/Injector Driver



MC33902 High Speed CAN with Diagnostics: Block Diagram

- High-speed CAN interface with embedded 5V supply
  - High speed CAN interface for baud rates of 40 kb/s to 1 Mb/s
  - Compatible with ISO11898 standard
  - Single supply from battery; no need for 5 supply
  - I/O compatible from 2.75V to 5V via a dedicated input pin
  - Low power mode with remote CAN wake up and local wake-up recognition and reporting
  - CAN bus failure diagnostic and TXD/RXD pin monitoring, cold start detection, wake up sources reported through the NERR pin
  - Enhanced diagnostic for bus, TXD, RXD and supply pins available through a Pseudo SPI using EN, NSTB and NERR existing pins
  - Split pin for bus recessive level stabilization
  - NH output to control external



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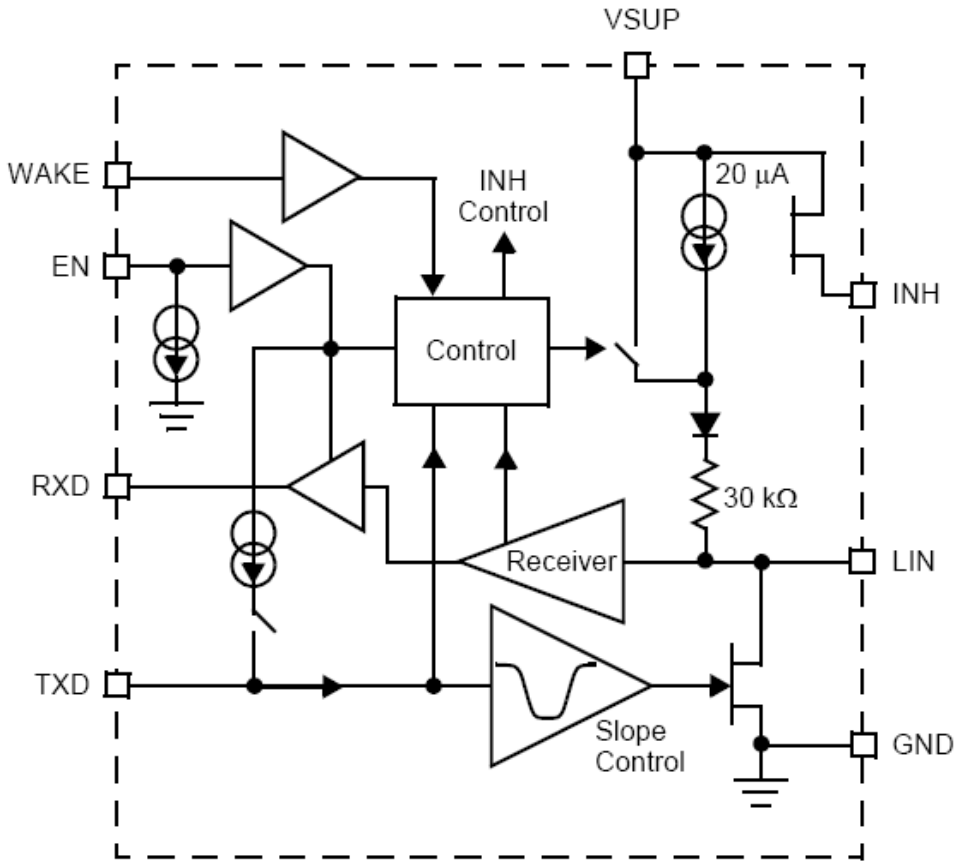
MC33661 LIN Transceiver: Block Diagram

- Local area network (LIN) enhanced physical interface with selectable slew rate
  - Operational from VSUP 6.0V to 18V DC, functional up to 27V DC, and handles 40V during load dump
  - Active bus waveshaping offering excellent radiated emission performance
  - 5.0 kV ESD on LIN bus pin
  - 30 kΩ internal pull-up resistor
  - LIN bus short-to-ground or high leakage in sleep mode
  - 18V to +40V DC voltage at LIN pin
  - 8.0 µA in Sleep mode
  - Local and remote wake-up capability reported by INH and RXD pins
  - 5.0V and 3.3V compatible digital inputs without any external components required



MC33661 Simplified Internal Block Diagram

Related Sessions

Session Code	Session Title	Class Level
FTF-AUT-F0341	Automotive MCU Architectures for the Future	Basic
FTF-AUT-F0553	Freescale Solutions for Powertrain and Hybrid	Basic
FTF-AUT-F0556	Analog Mixed Signal and Power Products for Automotive	Basic
FTF-AUT-F0732	SBCs: Power Management Solutions for 16- and 32-bit MCUs in Automotive Applications	Basic
FTF-AUT-F0819	Rapid Software Development on 32-bit Automotive MPC56xx Family of MCUs	Basic
FTF-AUT-F0354	**Reducing System Cost with Integrated MCU Solutions for Engine and Transmission Applications**	**Intermediate**
FTF-AUT-F0678	**MPC5674F Optimizing Software for Performance**	**Intermediate**
FTF-AUT-F0679	**MPC563xM Low-End Engine Control Hardware Design**	**Intermediate**
FTF-AUT-F0680	**MPC567xF Powertrain System Hardware Design**	**Intermediate**
FTF-AUT-F0684	Hands-on Workshop: An Overview of Freescale's Analog Standard Products for the Powertrain Market with Emphasis on the Newest and Most Versatile	Intermediate
FTF-AUT-F0730	Automotive Networking Protocol Overview	Intermediate
FTF-AUT-F0764	Hands-on Workshop: AUTOSAR	Intermediate
FTF-AUT-F0447	**Using Enhanced Time Processing Unit (eTPU/eTPU2) for Combustion Engine Management and Electric Motor Control**	**Advanced**
FTF-AUT-F0451	**Tips and Tricks with DMA on MPC56xx**	**Advanced**
FTF-AUT-F0737	MCU Solutions for Hybrid Drive Train	Advanced

Bolded sessions are highly recommended.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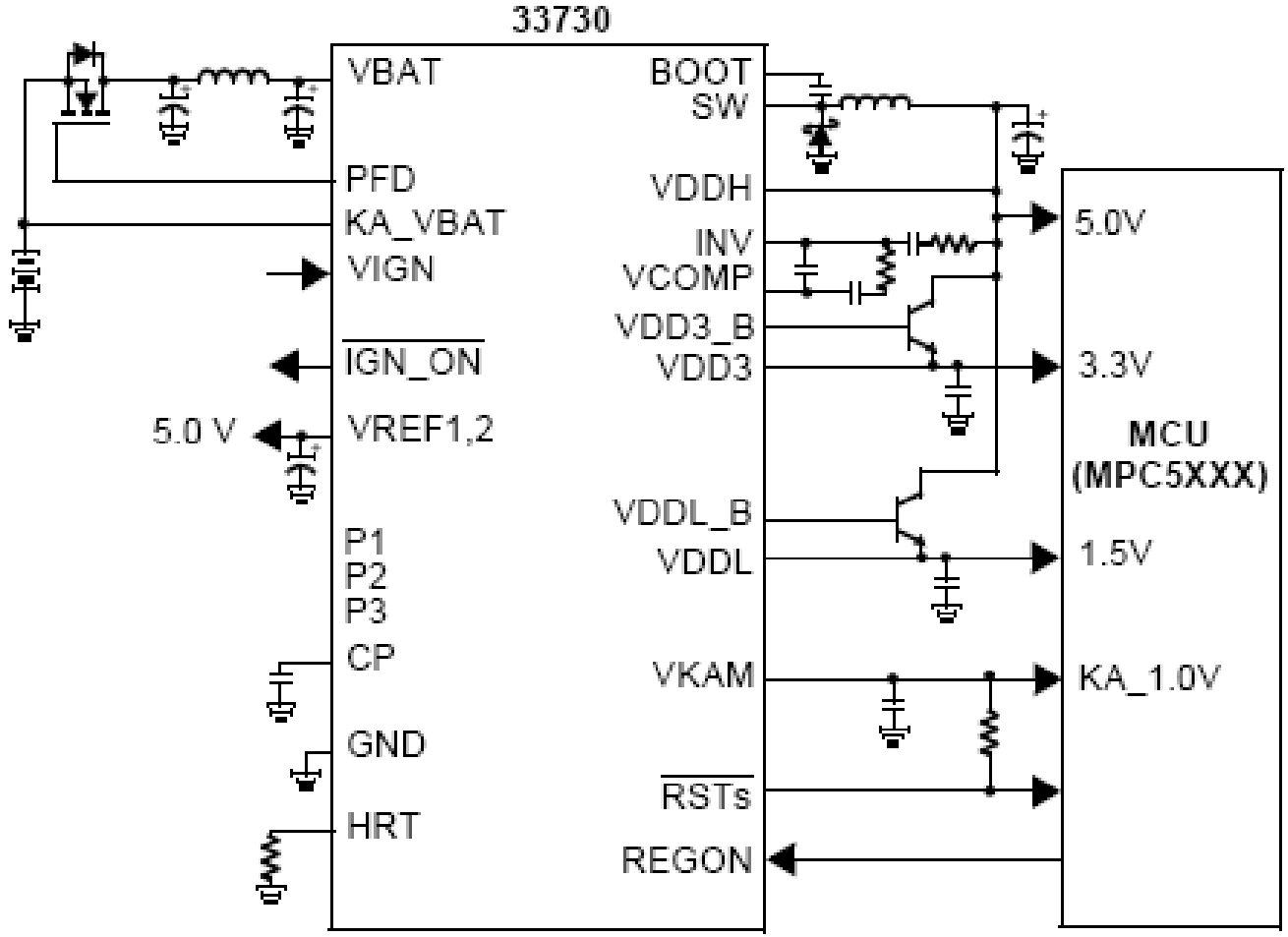
MC33730: Typical Application

Figure 1. 33730 Simplified Application Diagram



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