Introducing the Superscalar Version 5 ColdFire® Core

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Presentation Outline

- Design Goals
- Overview and Core Roadmap
- Architecture Definition and Core Microarchitecture
- Measured Performance
- Summary

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V5 ColdFire Design Goals

- Next-generation on ColdFire core performance roadmap
  - Performance Targets
    - 1.3x - 1.4x V4{e} core performance in same process technology
    - 2x V4{e} system-level performance in next-generation process
  - Maintain attributes of family heritage
    - Fully-synthesizable, highly-configurable designs for SoC
      - Compiled RAMs for cache and local memories
      - Provide SoC designers with access to key price/performance variables
    - Backward binary compatibility to preserve software investment

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ColdFire Overview

- Compatible family of cores architected for SoC and reuse
  - 100% synthesizable and technology-independent designs
  - Strong embedded debug architecture
    - Common developer tool set for std products + SoC designs
- Family of cores, software compatible with M68000 legacy
  - Generations of microarchitectures are named “versions” (Vx, CFx)
    - Executing on core performance roadmap made public in 1996
    - 4 generations have provided a 24x performance increase in 7 years
      - CF2Core 25 MIPS @ 33 MHz (0.80 *um*) in 1995
      - CF5{e}Core 610 MIPS @ 333 MHz (0.13 *um*) in 2002
- Excellent price/performance options across the family
  - 134 - 610 MIPS, 0.5 mm^2 - 5.2 mm^2 in 0.13µm
- Configurable designs: Options in cost / performance / function
- Application areas: imaging, connectivity, audio, std products

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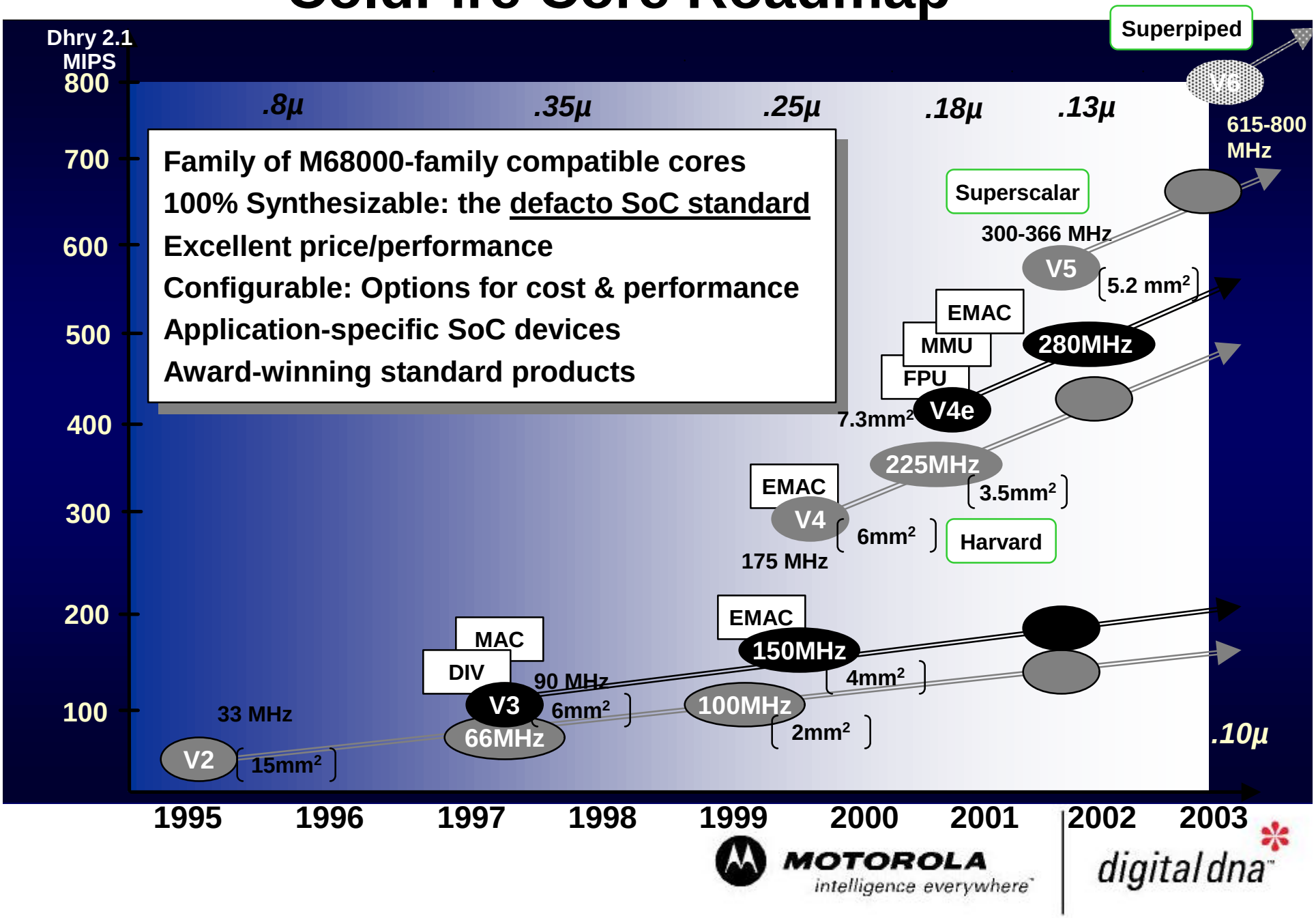
ColdFire Core Roadmap



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ColdFire Microarchitecture Definitions

- **Version 2 (V2) Core: Single-Issue**
  - Two independent, decoupled 2-stage pipelines
  - Single-cycle local bus with unified cache, RAM, ROM
- **Version 3 (V3) Core: Single-Issue + Pipelined Local Bus**
  - Two independent, decoupled (4-stage/2-stage) pipelines
  - 2-stage pipelined local bus with unified cache, RAM, ROM
- **Version 4 (V4) Core: Limited Superscalar**
  - Two independent, decoupled (4-stage/5-stage) pipelines
  - Harvard architecture with split I and D-caches: greater bandwidth
  - Instruction folding on conditional branches + moves
- **Version 5 (V5) Core: Full Superscalar**
  - Same basic pipeline organization as V4
  - Dual execution pipelines + larger branch cache with better prediction
- **Version 6 (V6) Core: Superpipelined**

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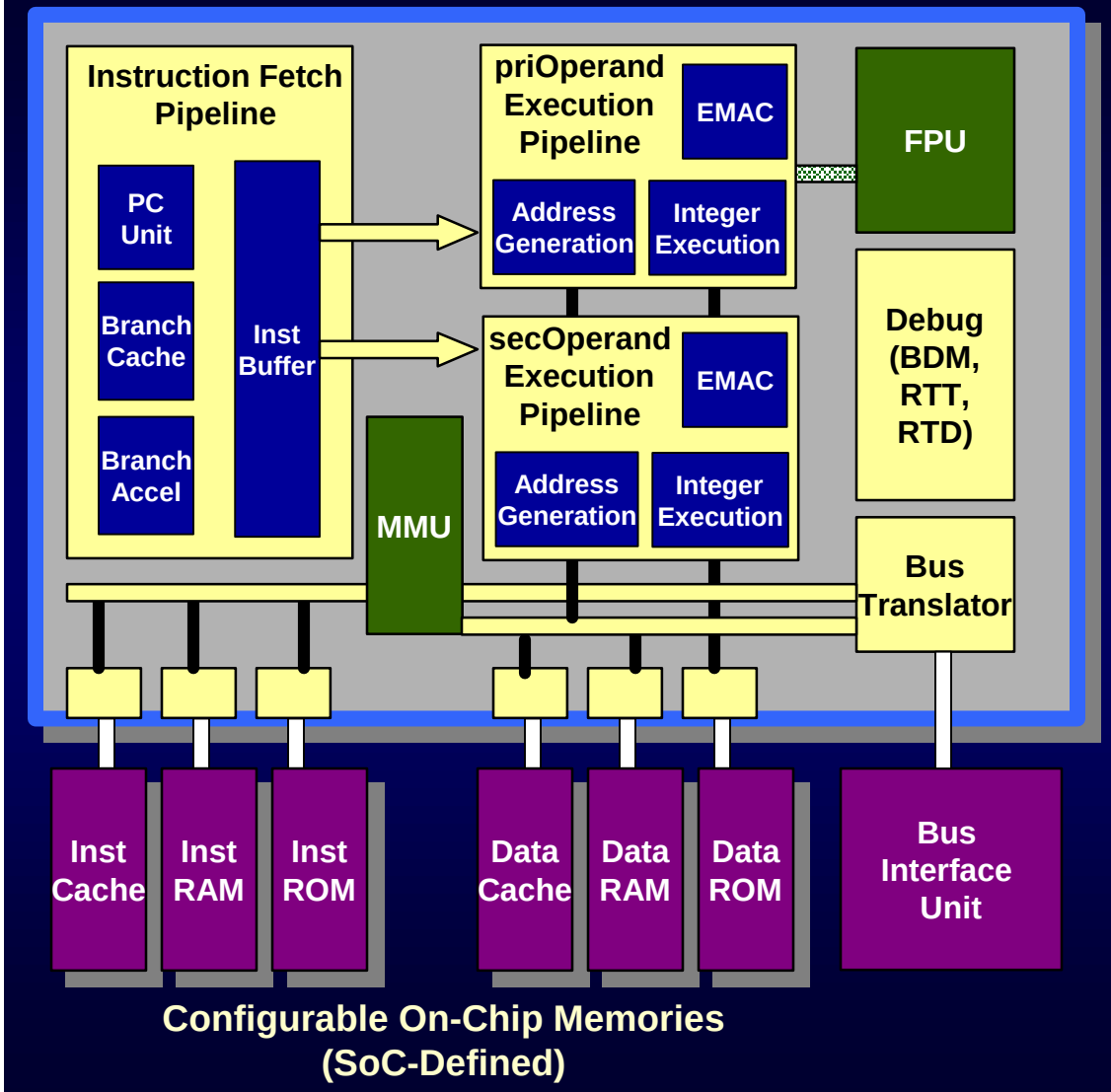
V5 ColdFire Core



Architectural Features

- Implements ISA_C, DEBUG_E
- Independent, decoupled pipelines
  - 4-stage Instruction Fetch Pipeline (IFP)
  - Dual 5-stage Operand Execution Pipelines ({pri, sec}OEP)
- Harvard memory architecture for expanded core and memory bandwidth
  - SoC-sized Cache, RAM, ROM
- Enhanced two-level branch acceleration
- Superscalar EMAC
- Optional MMU + FPU = V5e

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V5 ColdFire Architecture

- **Instruction Set Architecture, Revision C (*ISA_C*)**
  - **Small number of new instructions added to ISA_C for specific embedded application areas**
    - **Improved bit manipulation and interrupt processing**
      - `bitrev, byterev, ff1, stldsr`
    - **Multiply-accumulate: single-multiply, dual-accumulate**
      - **One instruction:** `Raccx = Raccx +/- Ry * Rx`
        `Raccw = Raccw +/- Ry * Rx`
        with optional 32-bit operand load
      - `m{a|s}{a|s}ac Ry,Rx,Raccx,Raccw,{<mem>y,Rx}`
      - **Useful in certain types of signal processing algorithms**
        - » Examples: FFT processing, Discrete Cosine Transforms (DCT)

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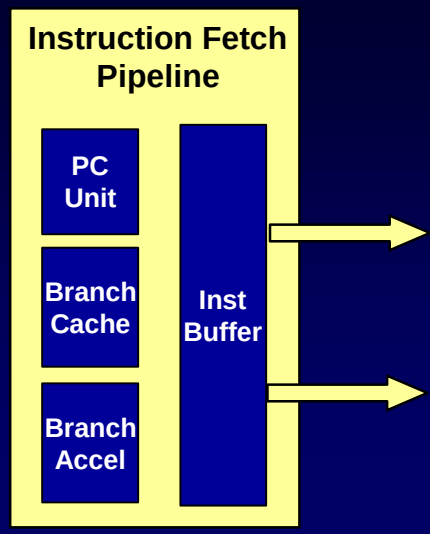
V5 ColdFire Architecture Cont'd.

- **Debug Architecture, Revision E (*DEBUG_E*)**
  - **Processor Status (PST) encoding expanded to 5 bits for RTT**
    - **PST/DebugData output speed reduced to 0.25 x Core MHz**
    - **Compression of PST values: Output 1 PST value indicating execution of *n* insts, rather than *n* PSTs each signaling 1 inst**
  - **4 more PC breakpoint registers added**
    - **Total of 8 PC breakpoints + 2 sets of address ranges with optional data values**
  - **Support for 2 *data trace* regions: automatic capture and precise display of address + data within region and no restrictions on the region (cacheable, non-cacheable, local RAM)**
  - **Optional periodic display of current PC for emulator synchronization**

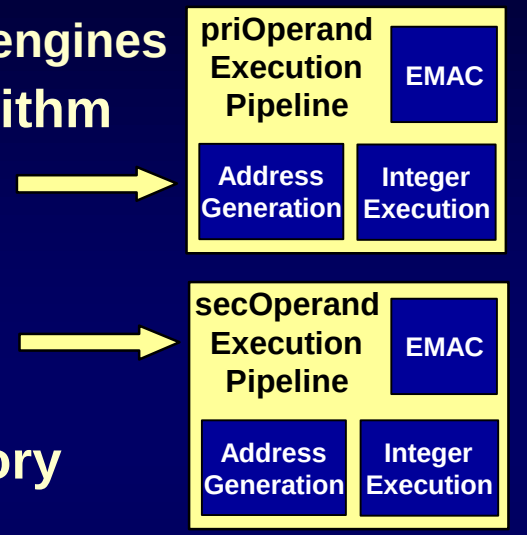
V5 Instruction Fetch Pipeline

- 4-stage, 64-bit Instruction Fetch Pipeline
  - Instruction Address Generation
  - Instruction Fetch Cycle 1
  - Instruction Fetch Cycle 2
  - Instruction Early Decode
- 16-entry FIFO Instruction Buffer: 1 inst/entry
- Branch Prediction
  - 256-entry, 2-way set-associative branch cache (BCU)
  - Local (2-bit state) and 128-entry global predictors
  - Folding on predicted-taken branches for 0-cycle execution time
  - 2nd-level Branch Acceleration Table used for BCU misses
    - 128-entries, hashed address, 2-bit prediction state
- 4-entry LIFO Hardware Return Stack



V5 Operand Execution Pipelines

- 5-stage, 64-bit Superscalar Operand Execution Pipeline
  - priOEP, secOEP: Each with two 2-stage compute engines
    - Decode/Select, evaluation of dispatch algorithm
    - Operand Address Generation
    - Operand Fetch Cycle 1
    - Operand Fetch Cycle 2
    - Execute
    - Optional Data Writeback for stores to memory



- Efficient Evaluation of Superscalar Dispatch Algorithm
  - Instruction resources determined by IFP's early decode stage
  - 6 tests evaluated: all must pass to allow secOEP inst dispatch
  - Optimizations to maximize superscalar dispatches
    - Result forwarding within instruction pairs if load + store
    - Dynamic execution selection: @ top or bottom of pipelines

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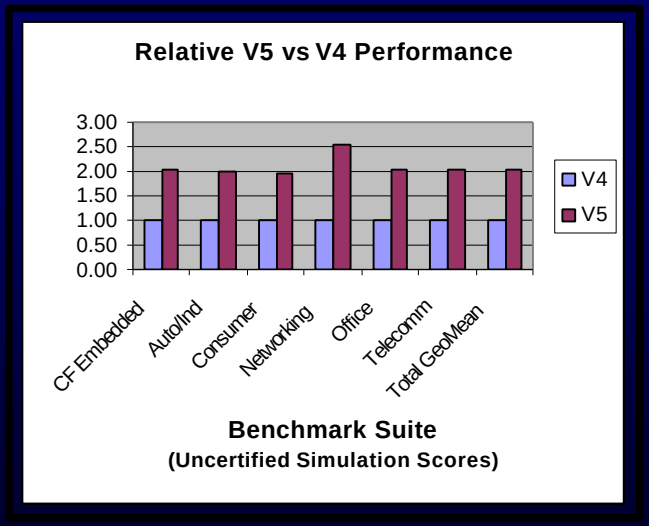
V5 Operand Execution Pipeline Cont'd

- **Superscalar EMAC (Enhanced Multiply-Accumulate)**
  - 2 instantiations (priOEP, secOEP) of 4-stage pipelined EMAC
  - Capable of dispatching two MAC instructions in single cycle with an optional 32-bit operand load on one instruction
  - Same programming model as original EMAC
    - Four 48-bit accumulators
    - Word/longword, signed/unsigned, integer/fractional data
    - Support for various product and store rounding, saturation
    - 32-bit accumulator results returned to integer register file
- **Optional Floating-Point Unit in priOEP**
  - Single-cycle, 64-bit data interface to local operand memories

V5 Measured Performance

- **Relative Performance of V5 versus V4 (MCF5407)**
  - **V5 Dhrystone 2.1 Performance = 1.83 DMIPS/MHz (vs. V4's 1.54)**
  - **Configurations**
    - **V5: 333/111 MHz, 32K I-/32K D-Cache**
    - **V4: 220/ 55 MHz, 16K I-/ 8K D-Cache**
    - **Connected to equivalent 32-bit external SDRAM memory**
  - ***Same object files* executed on both cores (70 programs total)**

ColdFire Embedded Suite	*= 2.05x*
EEMBC Auto/Industrial	*= 2.00x*
EEMBC Consumer	*= 1.97x*
EEMBC Networking	*= 2.52x*
EEMBC Office Automation	*= 2.05x*
EEMBC Telecomm	*= 2.02x*
Total Geometric Mean	***= 2.05x***



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V5 Microarchitecture Metrics

- Internal Pipeline Metrics
  - Measured on our complete benchmark suite, including EEMBC
- Comparison of V5 and V4 Pipelines

Metric	*Unit*	*V4*	*V5*
EffectiveCPI	cycles/inst	1.42	1.05
BaseCPI	cycles/inst	1.32	1.03
SS Dispatches	(pairs+triplets)/inst	0.28	0.64
Fraction of Bcc	Bcc/inst	0.14	0.14
Wrong-way Bcc	wwBcc/Bcc	0.11	0.08
Sequence Stalls	cycles/inst	0.14	0.12
Waiting for Insts	cycles/inst	0.07	0.07
Register busy	cycles/inst	0.02	0.02
Memory busy	cycles/inst	0.05	0.03

where BaseCPI is a measure of performance assuming an infinitely-large local memory, I.e., no cache misses, etc.

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Version 5 ColdFire Core Summary

- Implementations in 0.13 micron
  - 300 - 366 MHz, 549 - 670 Dhrystone 2.1 MIPS
  - 5.2 mm^2 V5e core-only, 9.6 mm^2 V5e core + 32K I-/32K D- + 4K
- Innovative architectural solutions meeting varied customer demands and achieving superior system performance through optional feature integration
- Continuing to reap the benefits of 100% synthesizability, easily moving to new, higher performance technologies
- Building on the ColdFire legacy of low-cost, high performance solutions and extending the family in both performance and integration

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