GOT NFC? LPC8N04 DOES – LEARN HOW TO LEVERAGE THIS UNIQUE FEATURE IN YOUR NEXT DESIGN?

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JUNE 21, 2018

SECURE CONNECTIONS FOR A SMARTER WORLD

Get To Market Fast with LPC800 MCUs – A Low-cost, Entry-level, 8-bit Alternative for Your Next Design

- Part I: Thursday, May 31, 10 AM Central (1 hour) | On Demand Now
  Thinking about migrating from 8-bit? Wait no longer - LPC80x MCUs are your 32-bit answer

- Part II: Thursday, June 7, 10 AM Central (1 hour) | On Demand Now
  Creative ways to leverage the LPC804 MCU's integrated programmable logic feature

- Part III: Thursday, June 14, 10 AM Central (1 hour) | On Demand Now
  Get started fast with this comprehensive enablement offering for LPC800 MCUs

- Part IV: Thursday, June 21, 10 AM Central (1 hour)
  Got NFC? LPC8N04 does – learn how to leverage this unique feature in your next design?

Agenda

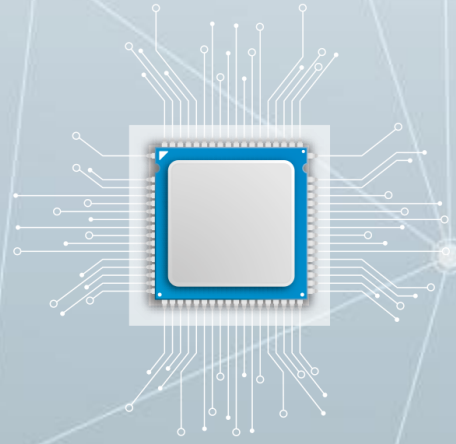
- Introduction
- LPC8N04 MCU Overview
- Target Applications / Use Cases
- Arm® Cortex®-M0+ Overview
- Memory (Flash + ROM)
- Clock System
- Power System
- GPIO
- Other Peripherals
- NFC
- Antenna Design
- Enablement
- Summary

LPC MICROCONTROLLERS
Broad Market Leader

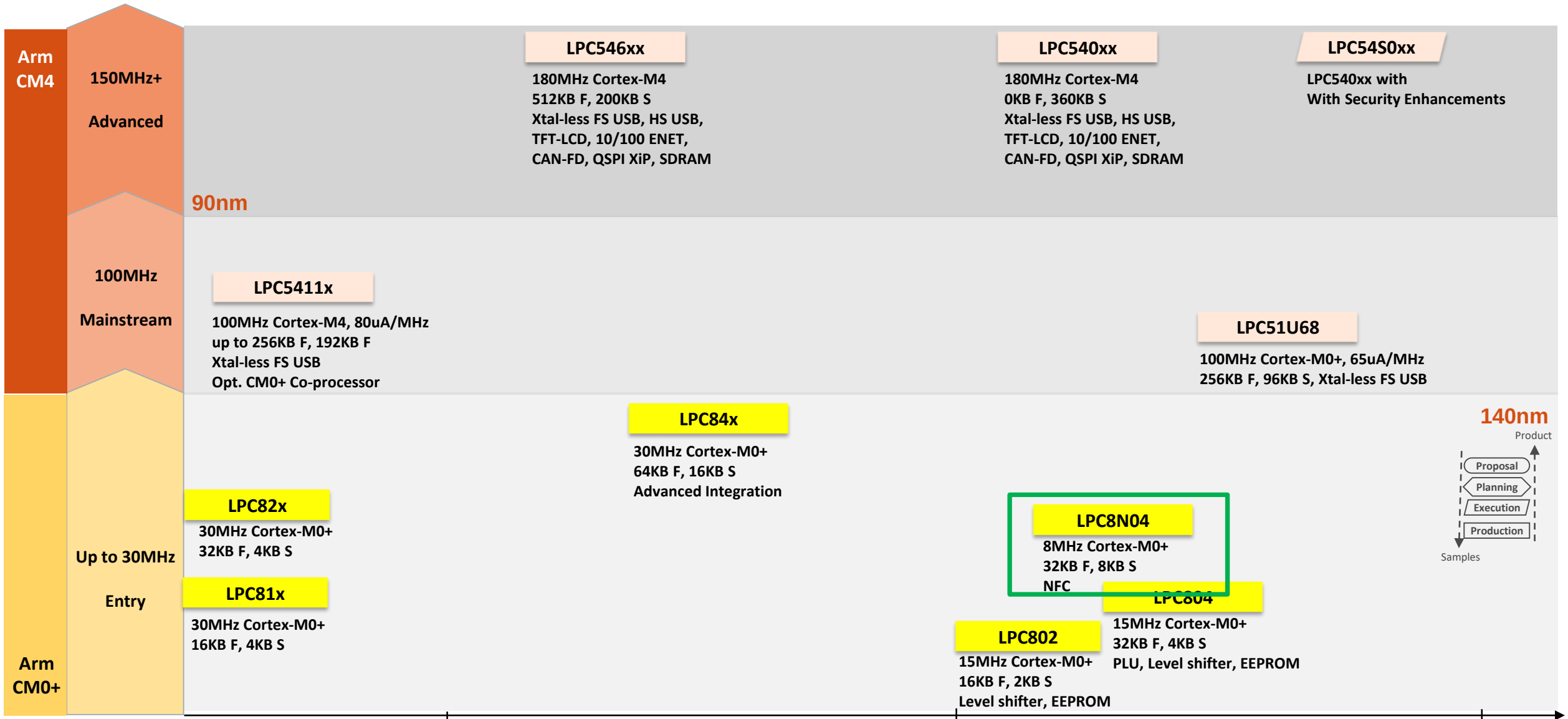
Architecting Scalable MCU Families with Flexible Integration
Enabling Fast Time To Market & Platform Re-use

1. **Innovative Arm®-based MCU Portfolio**
2. **Ecosystem & Partners**
3. **Supply, Longevity, & Quality**
4. **Local Support Network**
5. **Extensive Software & Tools**

- Accelerating the transition from 8-bit to 32-bit Arm® **Cortex-M based MCUs**
- **Low power, high performance MCUs** for energy conscious applications

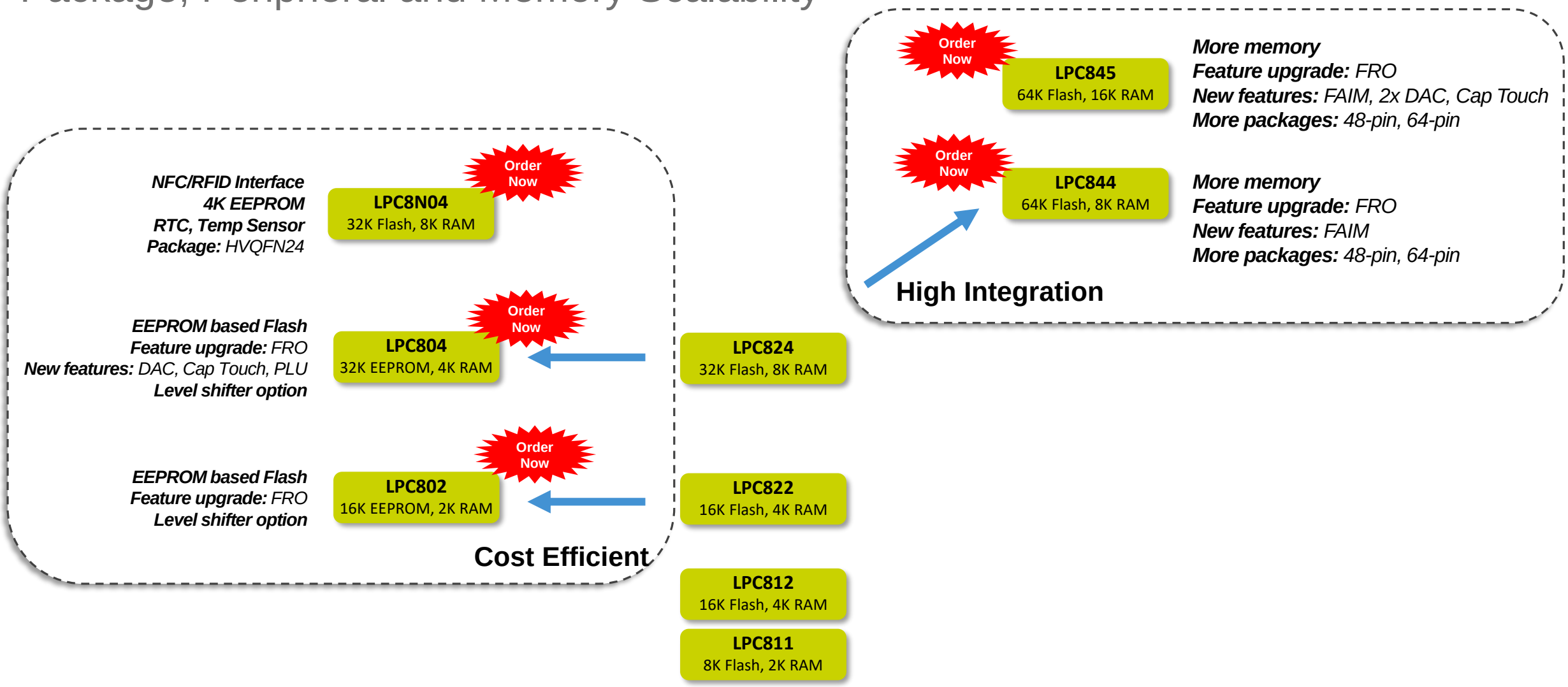


General Purpose MCU Roadmap | Power Efficient & Embedded Flash



LPC800 MCU Series | Expansion

Package, Peripheral and Memory Scalability



OVERVIEW

Introducing the LPC8N04 Microcontroller

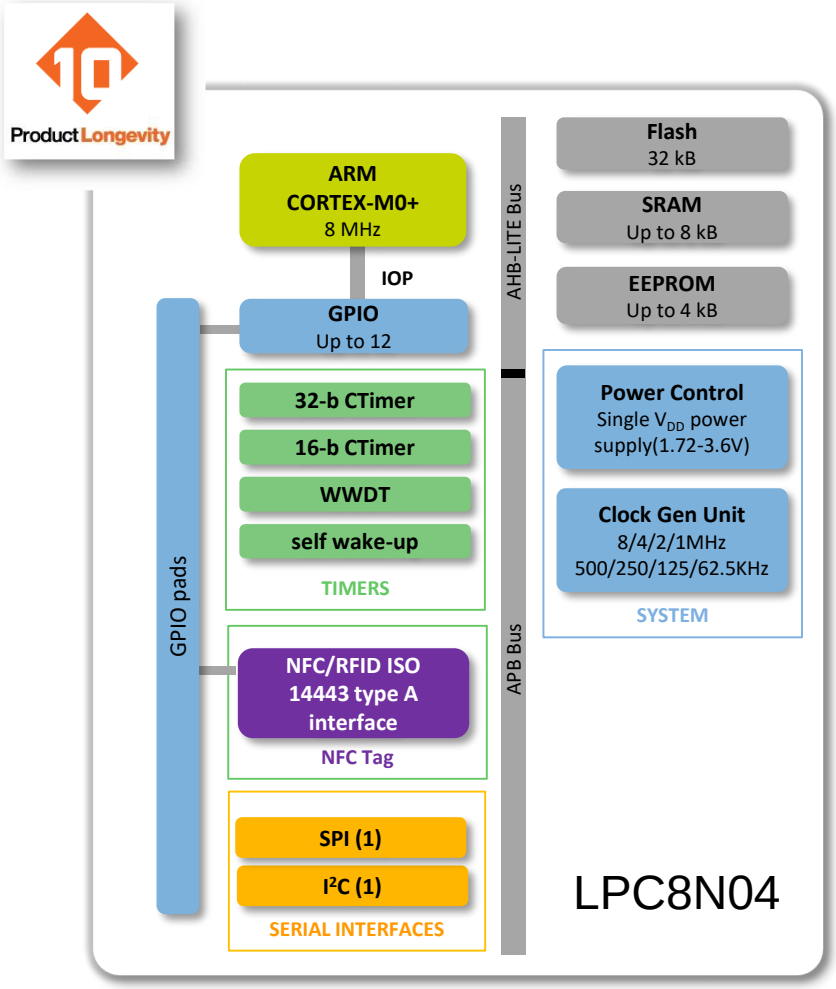
… *not just an NFC tag*

LPC8N04 combines NFC and microcontroller (MCU) technology enabling energy harvesting and wireless communication for a diverse range of tagging and provisioning applications

- An 8-Bit MCU upgrade with a 32-Bit Arm® Cortex®-M0+ core
- Integrated Flash, SRAM and EEPROM
- Featuring NFC tag connectivity in a single chip SoC
- Standard compliant for ISO14443A
- Close proximity, easy-to-use connectivity as BLE alternative
- Energy harvesting to power up MCU
- Small footprint QFN package

Key Features of the LPC8N04

An Expansion of LPC800 Series with Added NFC Tag



System

- 8 MHz Cortex-M0+ ARM core
- 32 kB Flash
- 8 kB RAM
- **4 kB EEPROM**
- **NFC/RFID ISO 14443 type A interface**

Exceptional power efficiency

- **< 900 µA/8MHz (active)**
- Four power modes
- Support to power from the NFC field
- **< 50 nA** IC current consumption in Battery-off mode at 3.0 V

Serial connectivity and GPIOs

- 1 I2C, 1 SPI
- Up to 12 GPIOs
  - High-current drivers/sinks (20 mA) on four GPIO pins
  - High-current drivers/sinks (20 mA) on two I2C-bus pins

Temperature sensor integrated

- +/- 1.5° C

Timers

- 1x 32-bit and 1 x 16-bit CTimer
- Wakeup Timer, Watchdog Timer
- RTC

Single **power supply**: **1.72 to 3.6V**

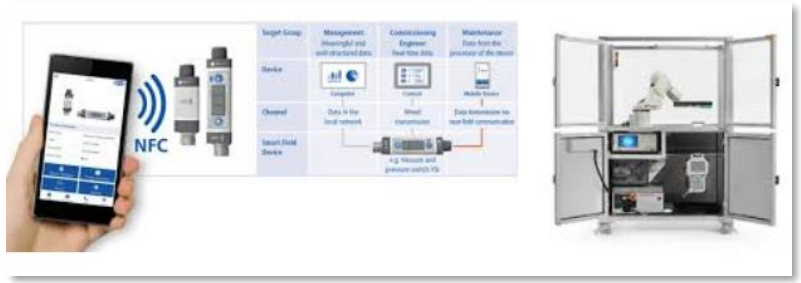
Temperature range: **-40 to +85 ° C** (ambient)

Package: HVQFN24

APPLICATIONS

LPC8N04 MCU | Target Applications

- Configurable LED strip/ Christmas tree LEDs via NFC
- Smart toy/Interactive robot
- Data logger
- Button-less/Contact-less control panel
- Contact-less Diagnostic
- NFC e-Locker
- Smart manufacturing
- NFC OTA for system FW update*

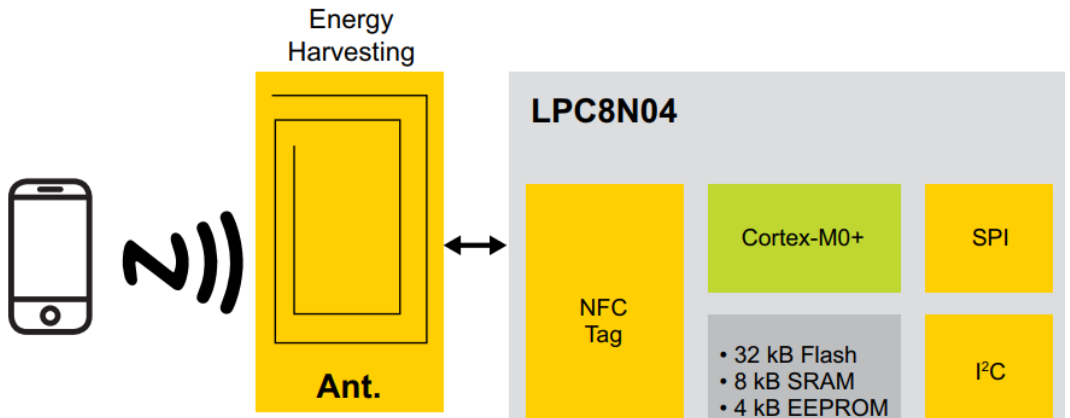


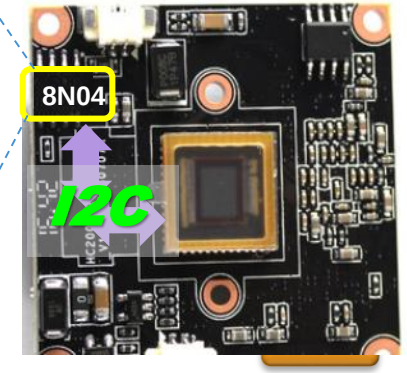
LPC8N04 MCU | Use Cases Cont'd

Why LPC8N04?

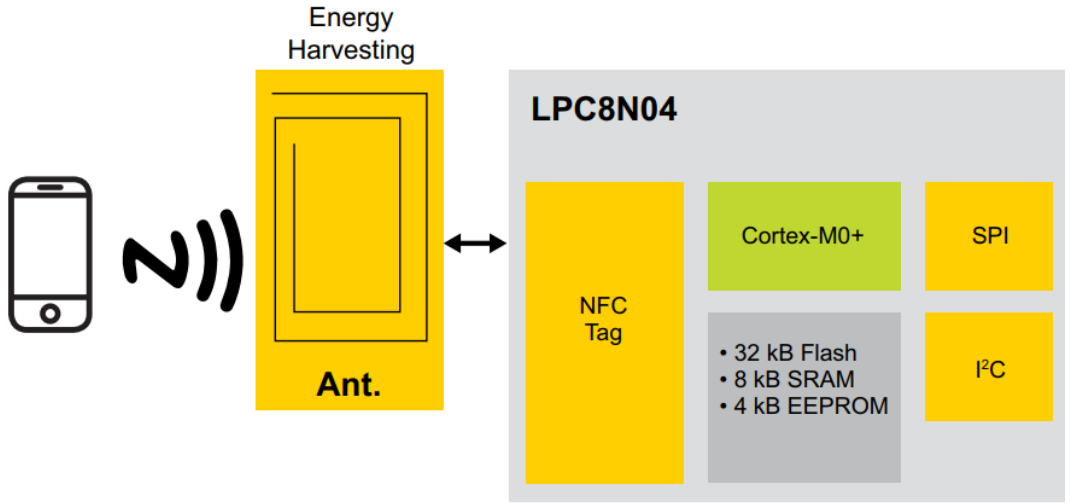
- √ 32-Bit Cortex M0+ based MCU
- √ Integrated NFC tag
- √ Integrated EEPROM
- √ Supports Keil, IAR and MCUXpresso

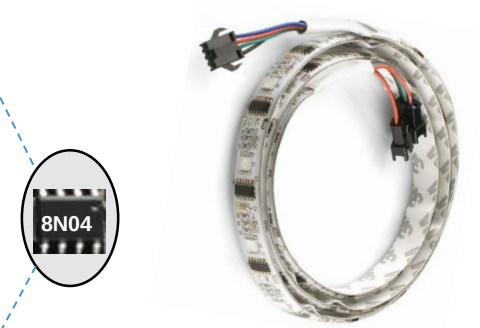
Parameter update for sensor module via NFC ***Contactless!***





Programmable LED strip via NFC ***Contactless!***

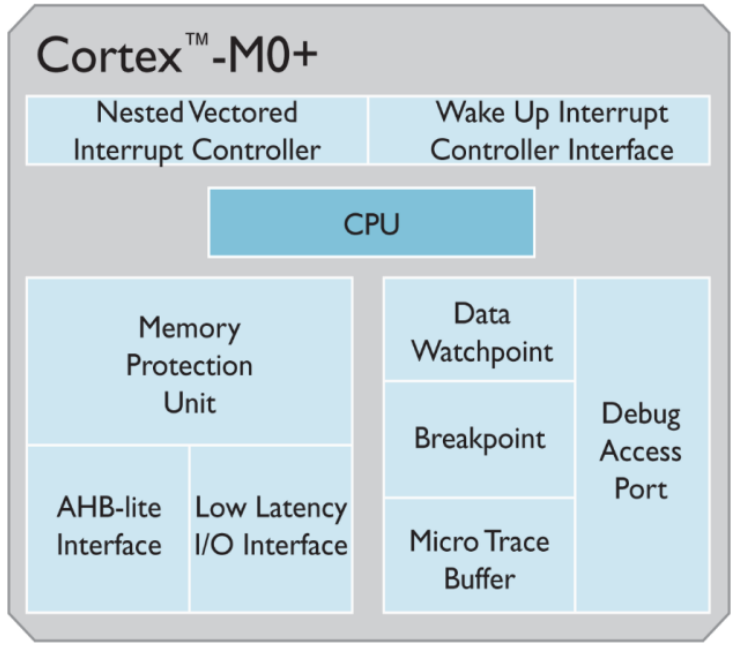




ARM® CORTEX®-M0+ CORE TECHNOLOGY OVERVIEW

Arm Cortex-M0+ Core Technology Overview

- High performance 32-bit CPU
- 2 stage pipeline
- Performance efficiency
  - 1.77 CoreMark/MHz - 0.93 DMIPS/MHz
- Deterministic operation
- Single cycle IO
- Built-in Nested Vectored Interrupt Controller (NVIC) with Wake-up Interrupt Controller (WIC)
- Debug using 2 pins with up to 4 breakpoints and 2 watchpoints
- Vector Table relocation
- Thumb2 instructions (56 instructions)



MEMORY

LPC8N04 MCU Memory Block

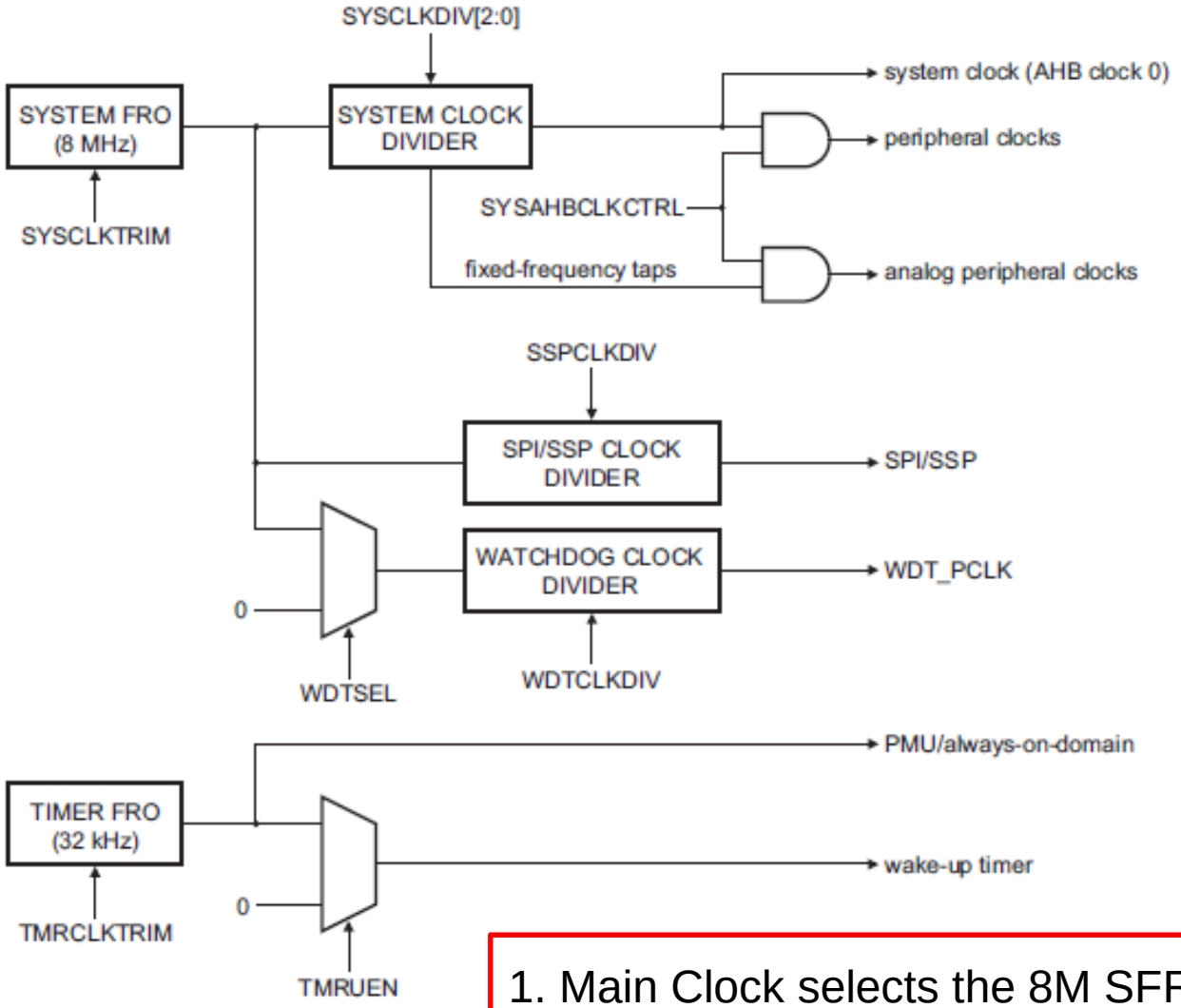
- **SRAM**
- 8KB (0x1000 0000 to 0x1000 1FFF)

- **Flash**
  - 32KB, Sector size:1 KB
  - Only 30KB can be used by user.

- **EEPROM**
  - 4KB
  - Access by ROM API

CLOCK SYSTEM

Clock System



Clock Sources	Characteristics
SFRO (System FRO)	• System clock by default • Stable. Quick power up and power down • 8MHz (±1% over 0 C to 70 C)
TFRO (Timer FRO)	• Low power operation • Always on domain power • 32.768 kHz signal to RTC

1. Main Clock selects the 8M SFRO and divided to 500Khz by default
2. TFRO cannot be disabled

POWER SYSTEM

LPC8N04 MCU | System Power Architecture

The LPC8N04 accepts power from two different sources: from the external power supply pin VDDBAT, or from the built-in NFC/RFID rectifier.

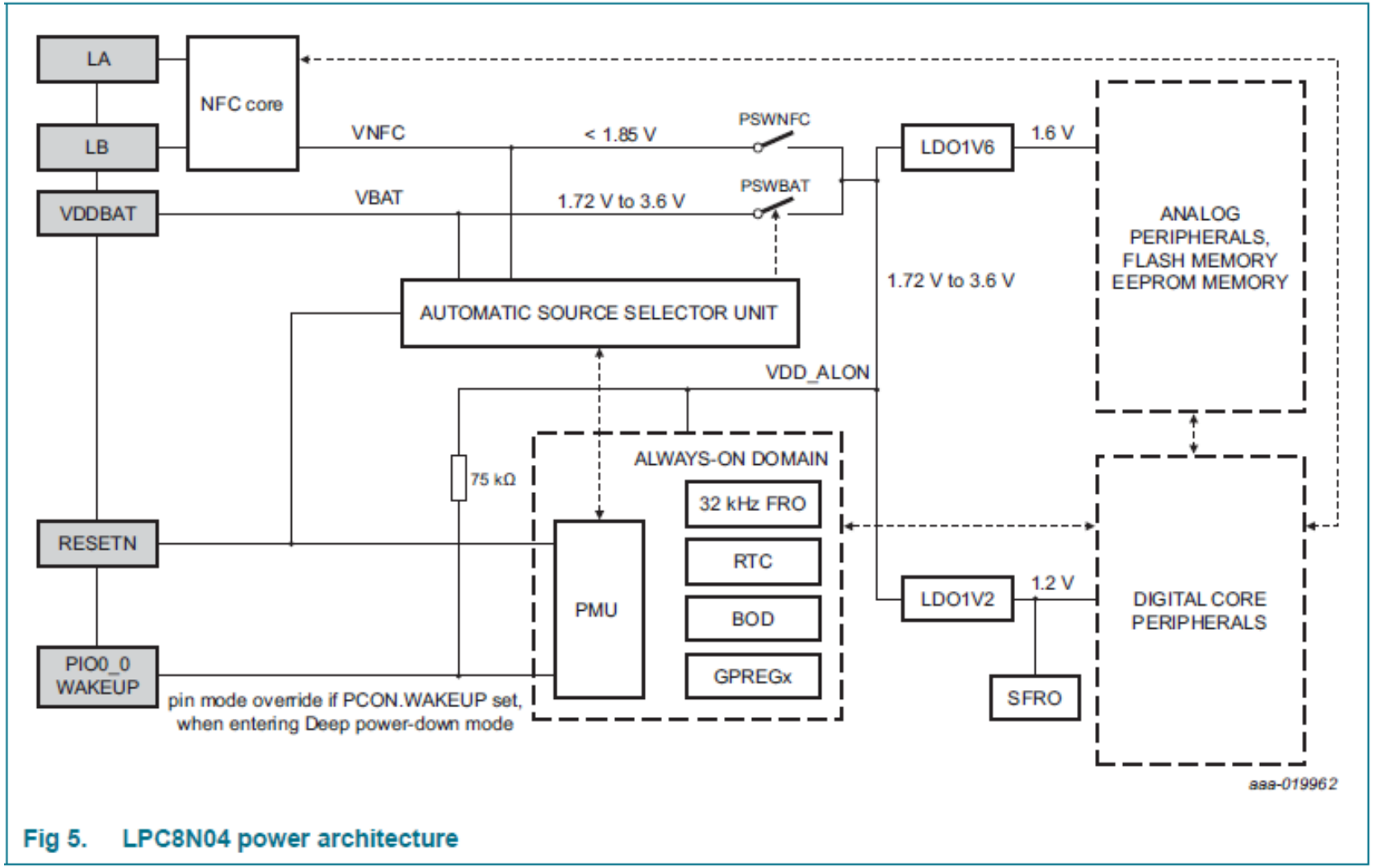
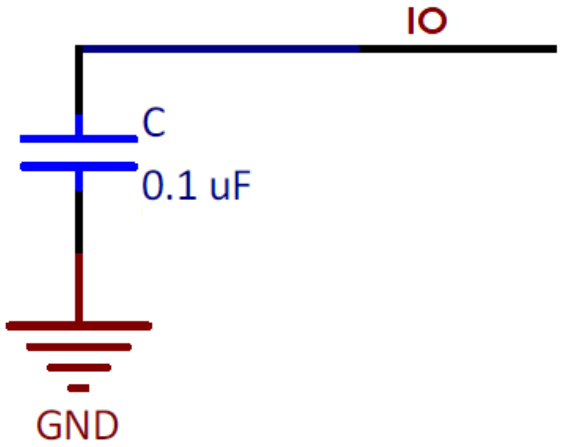


Fig 5. LPC8N04 power architecture

LPC8N04 MCU | NFC Power Harvesting

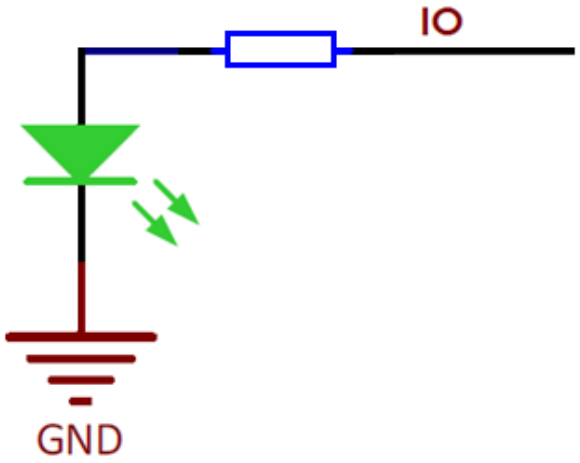


- **Battery-less solution**
  - Recommendation to add external capacitor 100-200 nF
    - Due to Miller pause at RF communication
    - If larger so serial resistor have to be used to reduce start-up current
  - Power harvesting from NFC field

- **Possibilities to power external device**
  - GPIO high drive pin (preferable)

NOTE: energy harvesting is limited to 2 MHz system clock

Important: The energy harvesting capabilities are directly related to the antenna design and NFC reader field strength.



LPC8N04 MCU | Low Power Modes

Low Power Mode	Impact	Wake-Up Sources
Sleep/deep sleep	System Clock to Cortex-M0+ is stopped. Peripherals and memories are active. Processor state and registers, peripheral registers, and internal SRAM are maintained, and the logic levels of the pins remain static	RF filed RTC event WAKEUP pin WDOG interrupt and reset External Reset
Deep Power-Down	Peripherals receive no internal clocks. The flash memory is powered down. Processor state/registers, peripheral registers, and internal SRAM contents are not retained, and the logic levels of the pins remain static. Exception for data retained is 5x32-bit general purpose register in PMU.	RF filed RTC event WAKEUP pin External Reset

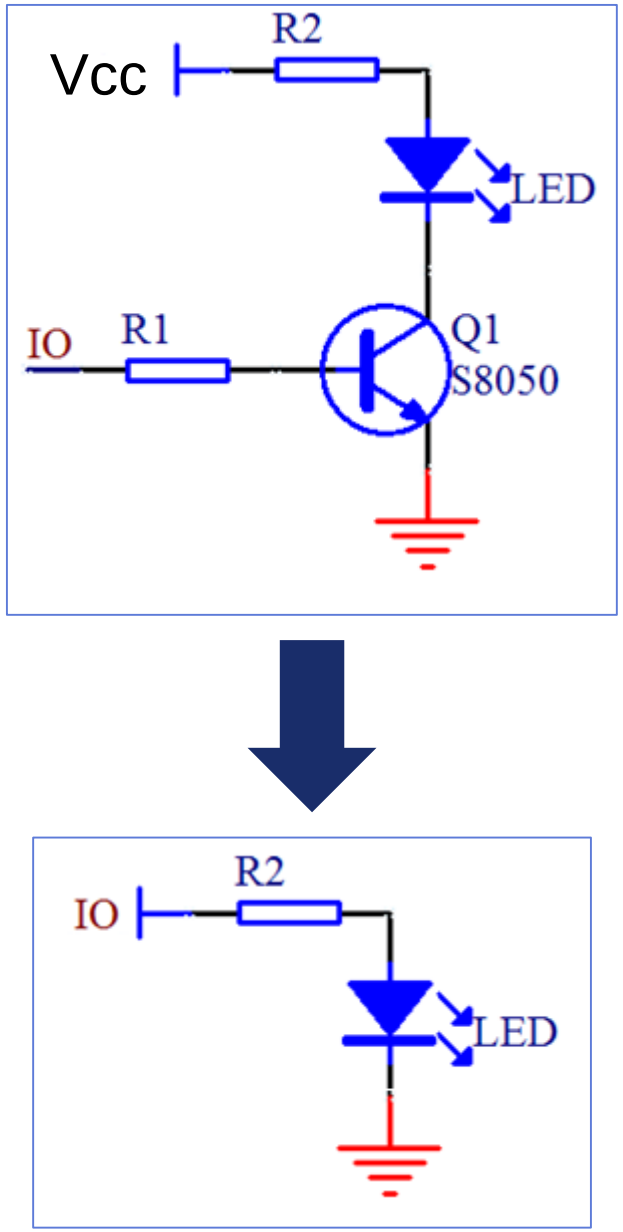
GPIO

Flexible I/O Port

- **Single cycle** access to all port pins
- **Support high frequency I/O toggling**
  - As fast as CPU_Clock/2
- **Enhanced GPIO Pin Manipulation**
  - Capable of simultaneously reading Bit/Byte/Word or toggling up to 12 I/Os per two instructions
- All GPIO pins can be configured as edge- or level-sensitive **interrupt** requests
- **Programmable** Internal pull-up/pull-down resistor, open-drain function, input inverter, and repeater mode
- High-current source output driver/**high drive** (20 mA)

High Drive Pins

- Provide high current drive capability (20mA)
- Able to directly drive LEDs
  - ***Eliminate external drive IC***
  - ***Save BOM cost and board PCB size***
- ***High drive pins***
  - 4 pins: ***PIO0_3, PIO0_7, PIO0_10, PIO0_11***



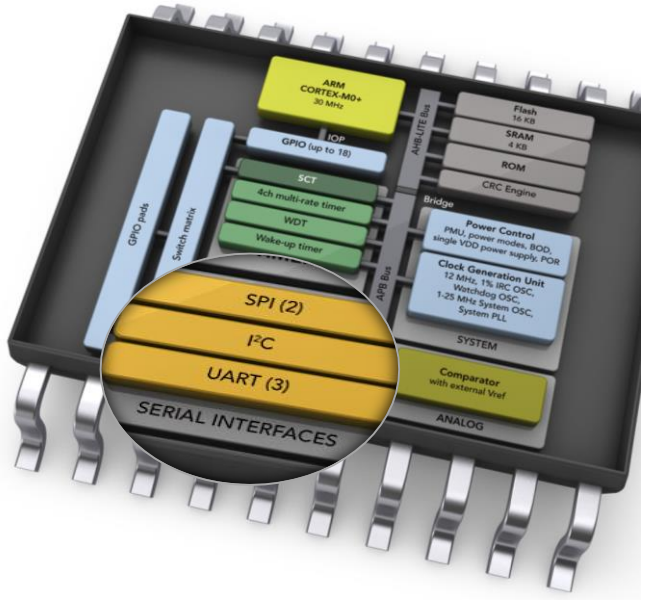
OTHER DIGITALS

Timers

- Standard 16-bit Timer (up to 2 channel PWMs)
  - Interval timer for generating internal events
  - Free-running timer
  - Pulse Width Modulator via match outputs
- Standard 32-bit Timer (up to 2 channel PWMs)
  - Interval timer for generating internal events
  - Free-running timer
  - Pulse Width Modulator via match outputs
- RTC
  - Clock source from TFRO(32.768Khz)
- Systick Timer (24-bit timer)

I²C/SPI

- I²C
  - 1 x I²C
  - Standard mode (up to 400Kbit/s) capability on the open-drain pins
- SPI
  - 1 x SPI
  - Eight-frame FIFOs for both transmit and receive
  - 4-bit to 16-bit frame
  - Maximum data rate of 8 Mbit/s in master and 2.6 Mbit/s in slave



DEBUG MODULE

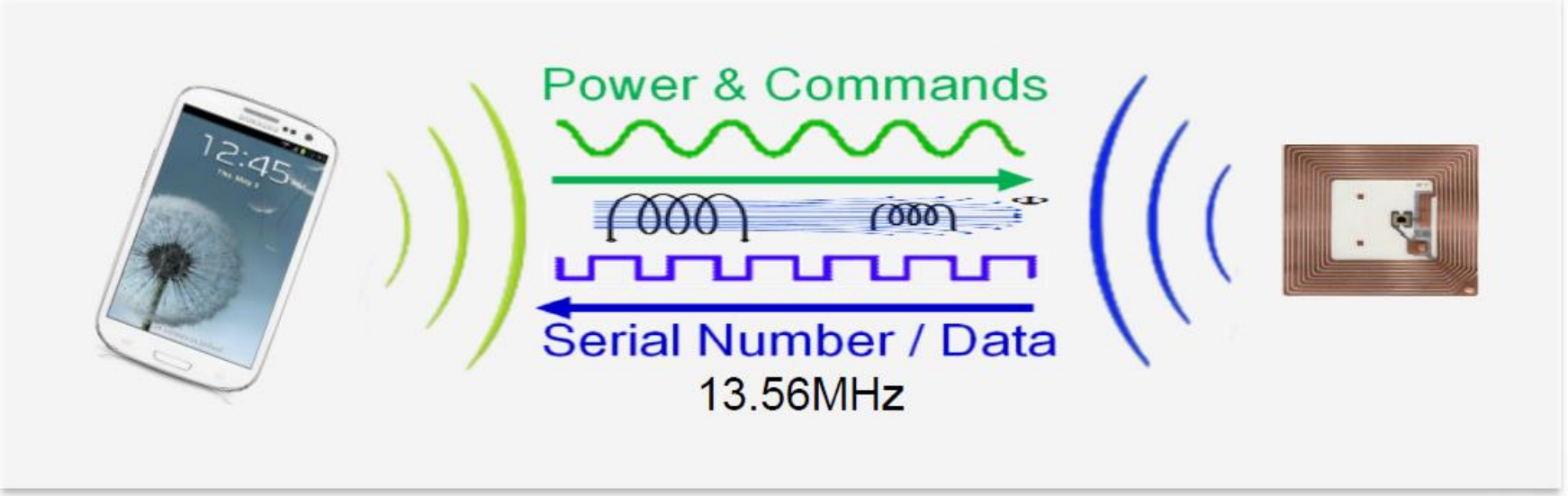
Emulation and Debugging

- Debug and trace functions are integrated into the ARM Cortex-M0+
- Serial wire debug (SWD: 2 pins)
- Supports up to four breakpoints and two watchpoints
- Standard JTAG pins (5 pins) supports ONLY boundary scan testing

NFC TAG

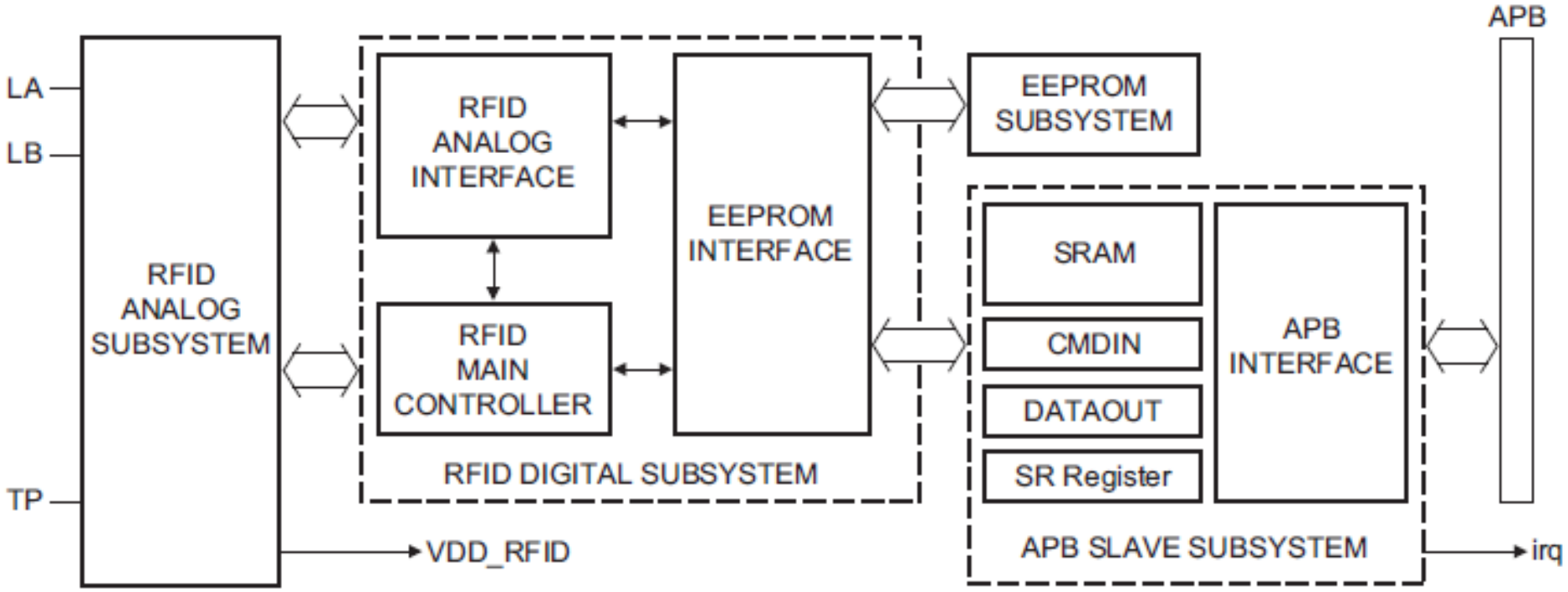
How Does a NFC Tag Work?

- Same fundamental principle as RFID, contactless smart cards or access control badges
- Reader (e.g. mobile device) provides power, initiates RF communications & captures data from the tag (or programs data into the tag)



NFC

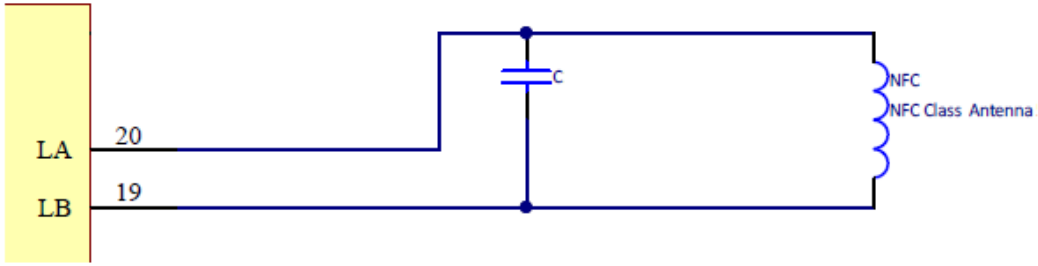
- ISO/IEC14443A part 1 to part 3 compatible
- MIFARE (Ultralight) EV1 compatible
- NFC Forum Type 2 compatible
- Easy interfacing with standard user memory space READ/WRITE commands
- Passive operation possible

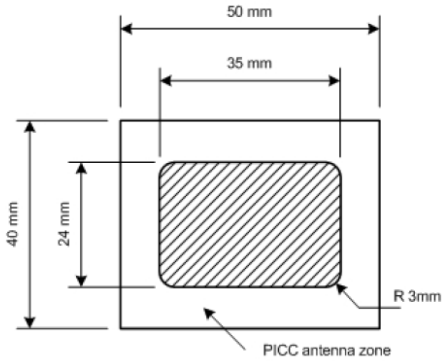


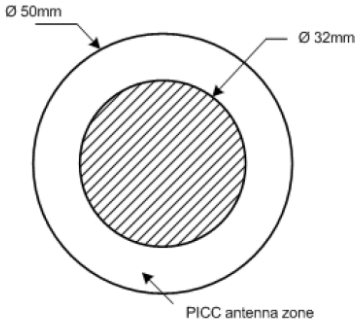
ANTENNA DESIGN

NFC Antenna

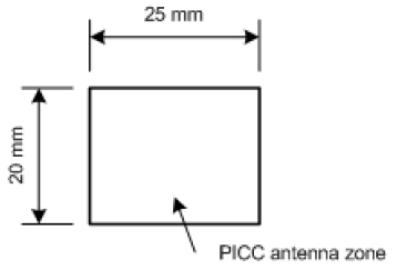
- Antenna and capacitor for tuning (optional)
  - 13.56 MHz optimized antenna does not need capacitor
  - Recomendation to use antena „Class 3“ to „Class 6“

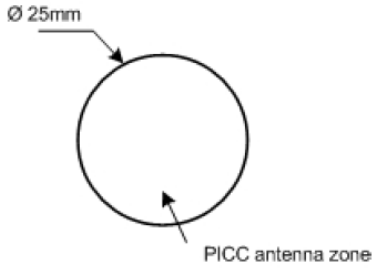






„Class 3“ antenna



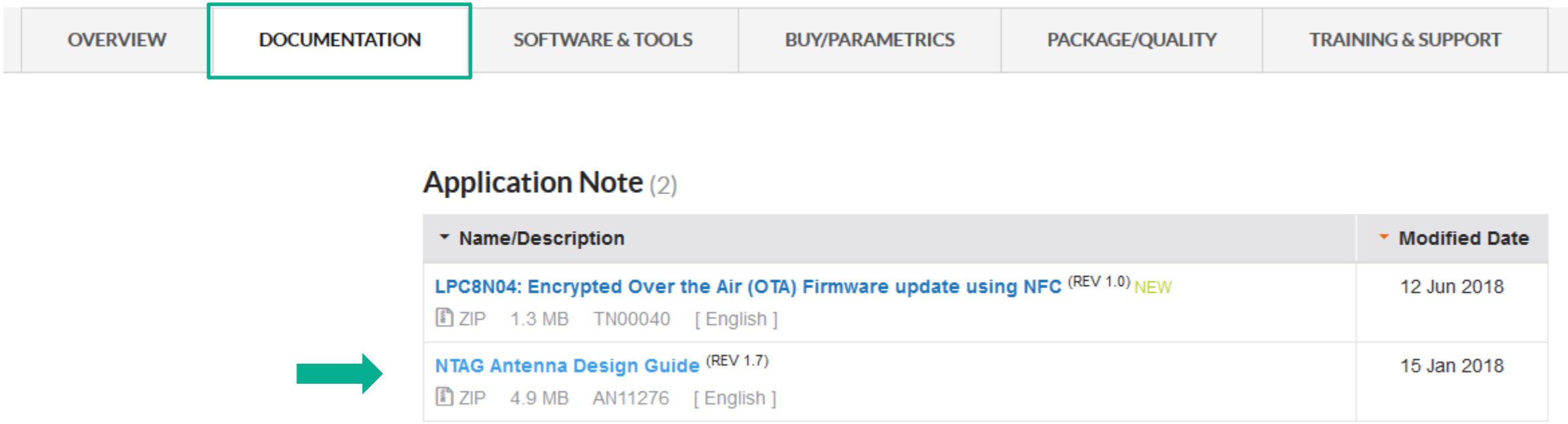


„Class 6“ antenna

- Antenna size and turncount has influence to power harvesting posibilities
  - A higher turn count improves Energy Harvesting output power on mobile phones in close coupling
  - Reducing the turn count improves the stability of energy harvesting in the distance

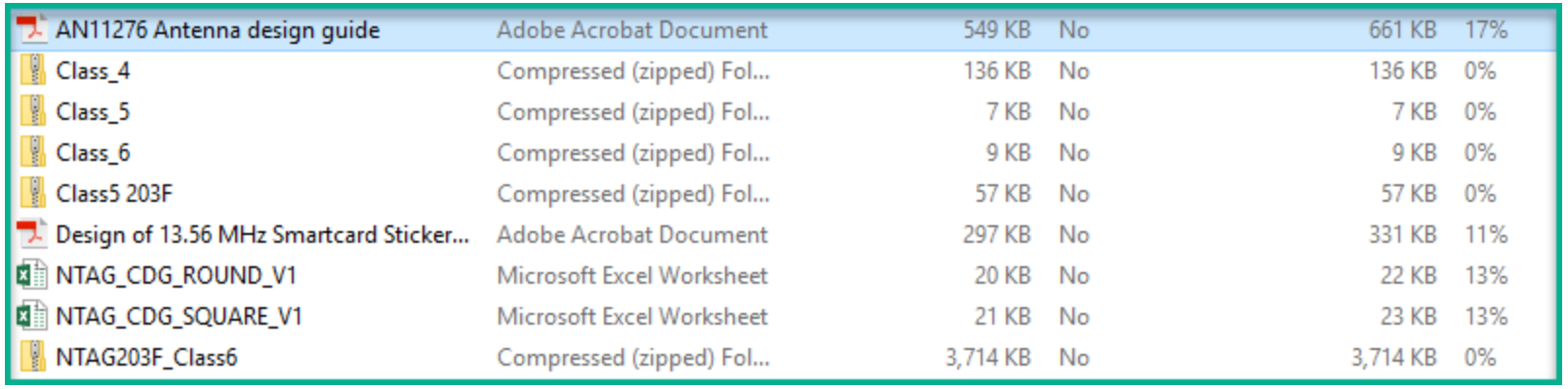
Antenna Design Documentation

Antenna Design folder available on the Application Note Section of the LPC8N04 Documentation.



Antenna Design Guide

The AN11276.zip includes documentation, gerber files and antenna calculation tools.



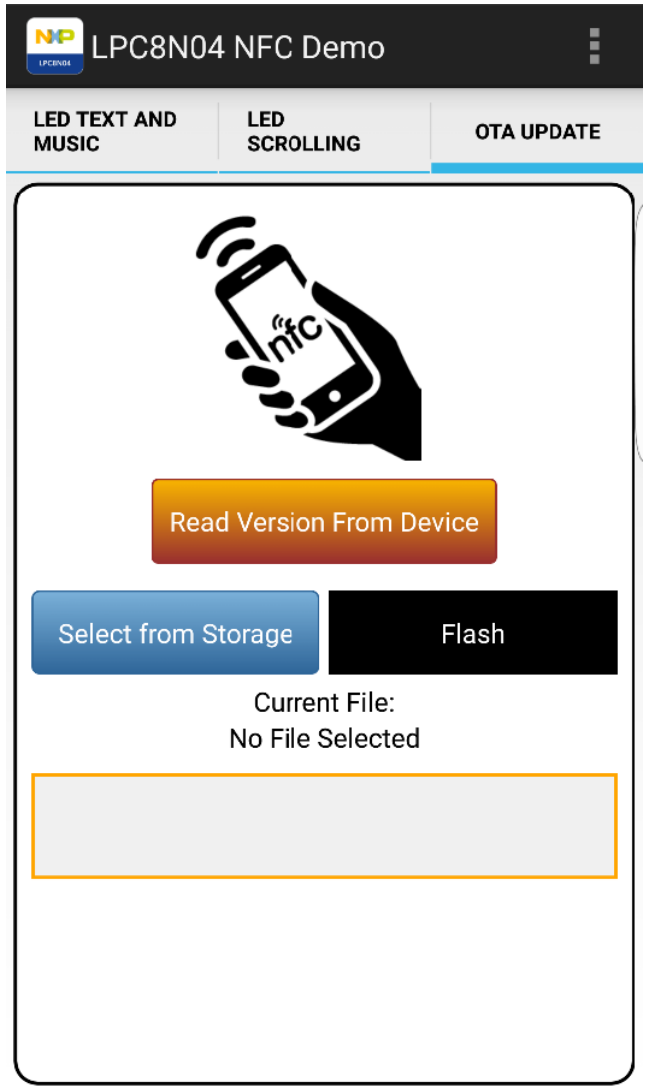
AN11276 Antenna design guide	Adobe Acrobat Document	549 KB	No	661 KB	17%
Class_4	Compressed (zipped) Fol...	136 KB	No	136 KB	0%
Class_5	Compressed (zipped) Fol...	7 KB	No	7 KB	0%
Class_6	Compressed (zipped) Fol...	9 KB	No	9 KB	0%
Class5 203F	Compressed (zipped) Fol...	57 KB	No	57 KB	0%
Design of 13.56 MHz Smartcard Sticker...	Adobe Acrobat Document	297 KB	No	331 KB	11%
NTAG_CDG_ROUND_V1	Microsoft Excel Worksheet	20 KB	No	22 KB	13%
NTAG_CDG_SQUARE_V1	Microsoft Excel Worksheet	21 KB	No	23 KB	13%
NTAG203F_Class6	Compressed (zipped) Fol...	3,714 KB	No	3,714 KB	0%

OTA

Encrypted OTA FW Update Over NFC

- LPC8N04 with Boot ROM version greater then equal to 0.14
- OTA does not work with energy harvesting
- OTA firmware update using SBL
  - SBL download the encrypted firmware over NFC
  - Decrypt
  - Update the flash memory with the new firmware

- Android app example from google store – LPC8N04 NFC demo
- Secure image creator, sample binaries and source code on websites



OTA Documentation

OVERVIEW | DOCUMENTATION | SOFTWARE & TOOLS | BUY/PARAMETRICS | PACKAGE/QUALITY | TRAINING & SUPPORT

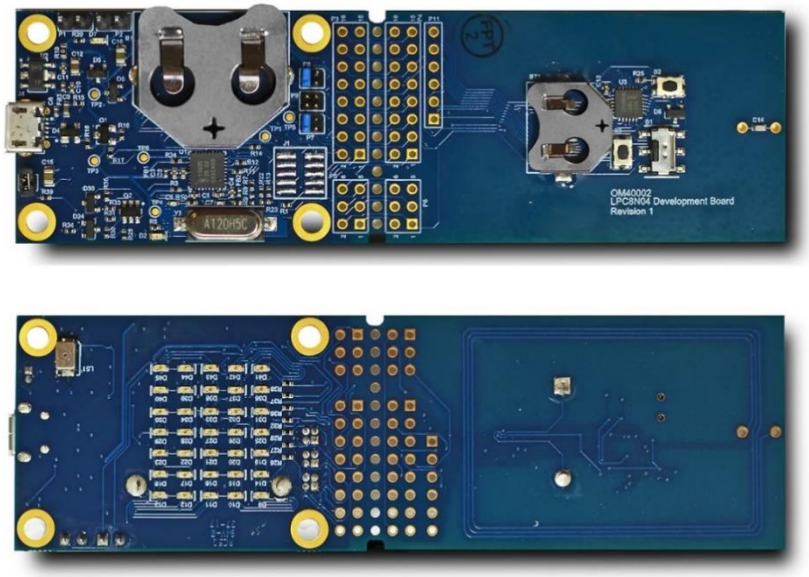
Application Note (2)

Name/Description	Modified Date
LPC8N04: Encrypted Over the Air (OTA) Firmware update using NFC (REV 1.0) NEW ZIP 1.3 MB TN00040 [English]	12 Jun 2018
NTAG Antenna Design Guide (REV 1.7) ZIP 4.9 MB AN11276 [English]	15 Jan 2018

ENABLEMENT

LPC8N04 MCU Development Board

- LPC8N04 in HVQFN24 package
- Detachable on-board CMSIS-DAP debug interface
  - Supports MCUXpresso IDE and other leading 3rd party tools
  - 10-pin SWD connector for optional external debug probe
- Expansion headers
- User button
- 5 x 7 LED matrix for debug/demo
- Integrated NFC Antenna
- Buzzer for debug/demo
- Optional coin cell battery power
- USB powered
- Supports energy harvesting operation with no battery or external power connection

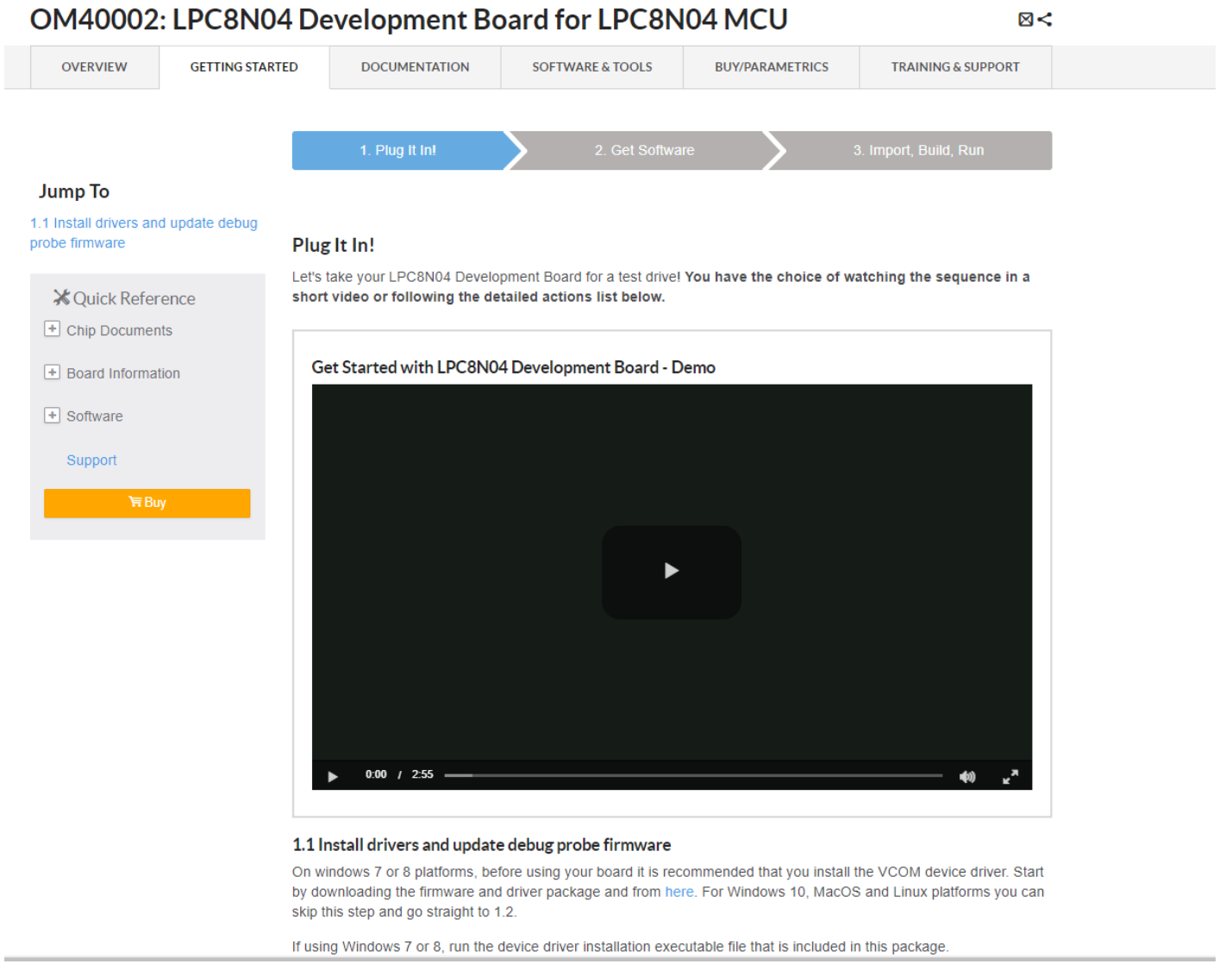


Orderable Part Number: ***OM40002UL***
http://www.nxp.com/demoboard/OM40002

✓ **LPC8N04 Board Support Package**

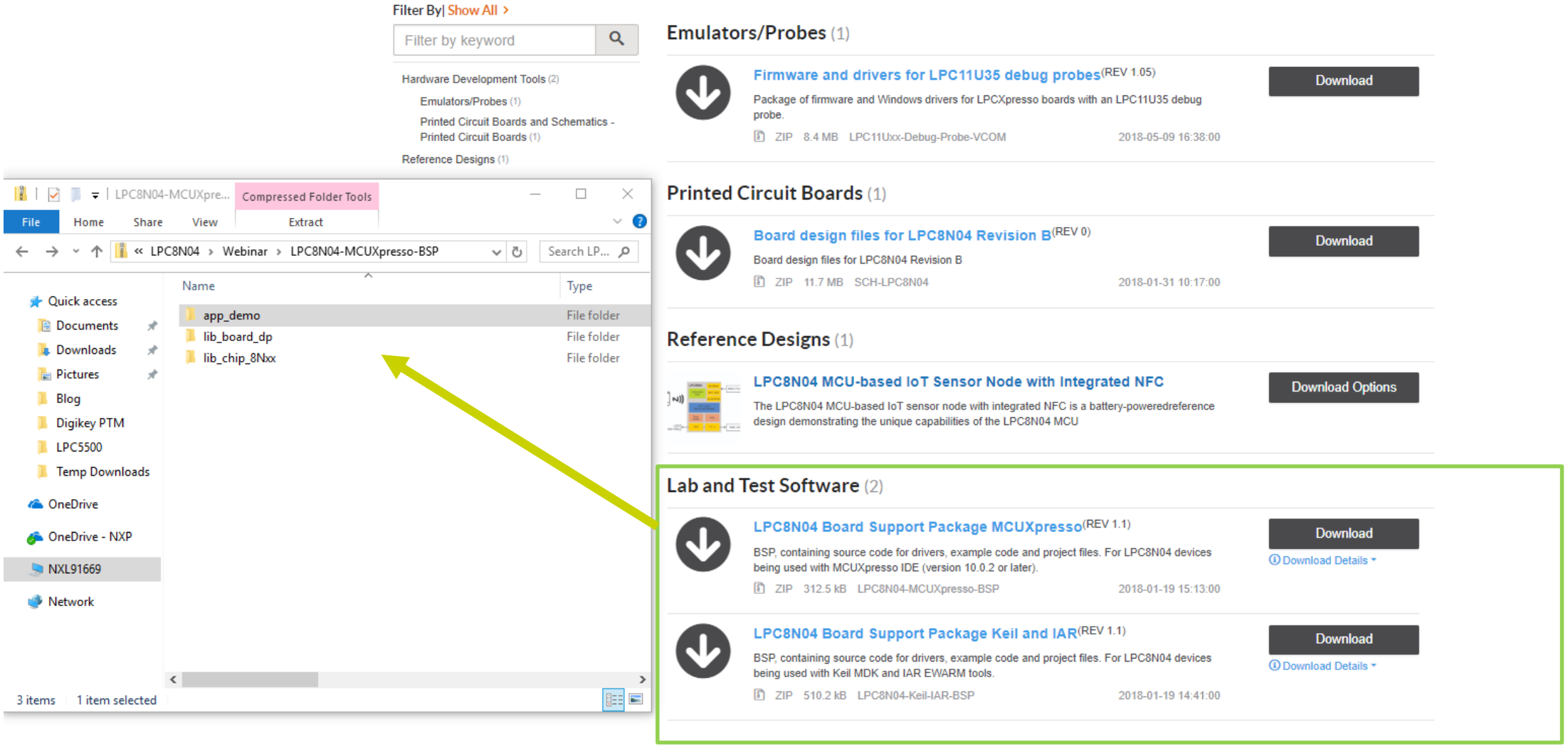
✓ **Free MCUXpresso IDE & 3rd Party Options**

Getting Started with LPC8N04 MCUs



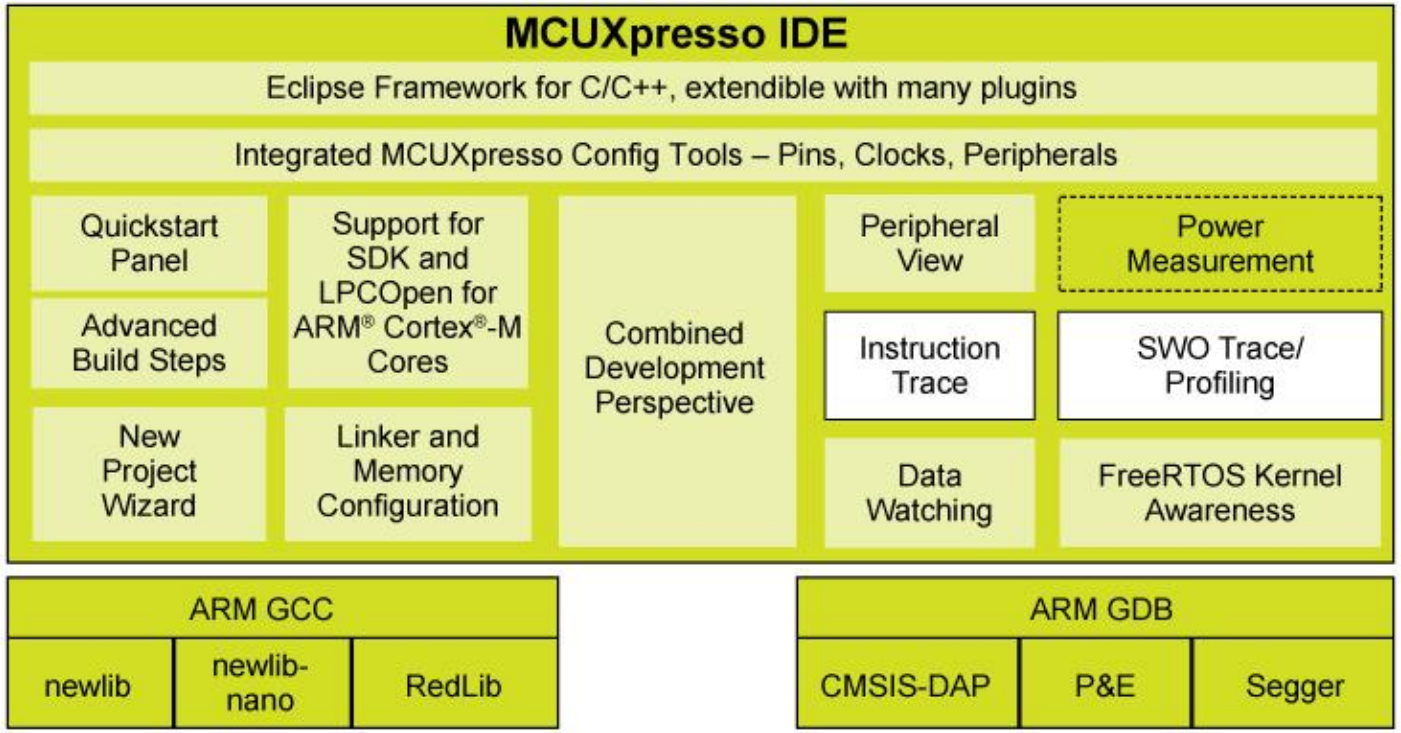
LPC8N04 MCU | Board Support Package

Learn more at: www.nxp.com/LPC8N04



MCUXpresso IDE

Free Eclipse and GCC-based IDE for C/C++ development on Kinetis and LPC MCUs and i.MX RT crossover processors



Product Features

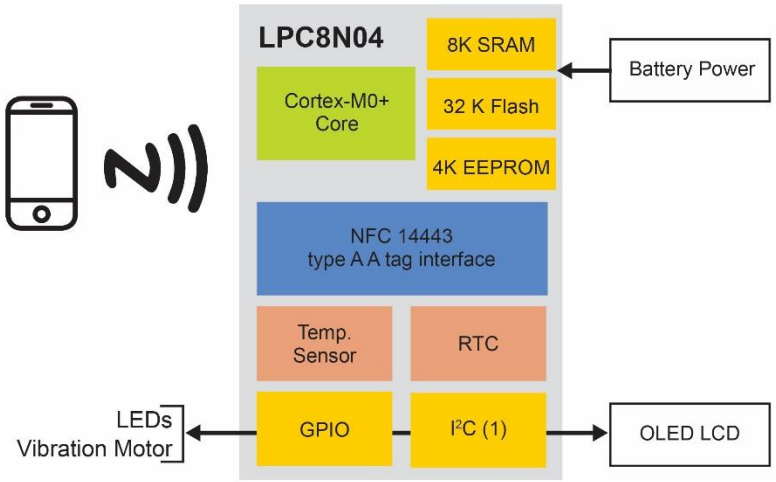
- Feature-rich, unlimited code size, optimized for ease-of-use, based on industry standard Eclipse framework for NXP's Kinetis and LPC MCUs and i.MX RT crossover processors
- Application development with Eclipse and GCC-based IDE for advanced editing, compiling and debugging
- Supports custom development boards, Freedom, Tower and LPCXpresso boards with debug probes from NXP, P&E and Segger
- Free: Full Featured, unlimited Code Size, no special activation needed, community based support, advanced trace capabilities

LPC8N04 MCU-based IoT Node with Integrated NFC

- **A button-less, IoT Node Reference Design based on LPC8N04**
  - OLED for date and time display with button-less settings
  - Cell-phone pairing via NFC interface
  - Alarm with sound notification
  - Temperature measurement and history tracking
  - LED Indicators
  - Battery power

LPC8N04 is a single chip solution to provide

- Integrated NFC 14443 type A interface
- EEPROM for temperature data log storage
- I2C for OLED LCD control
- An integrated RTC for clock
- An integrated high accurate temperature sensor
- Timers for vibration motor control
- GPIOs for LED control
- Low power mode for power saving



SUMMARY

LPC8N04 MCU | Summary

Cortex-M0+ based MCU with Integrated NFC Technology

Unique Integration
Arm® Cortex®-M0+ with integrated NFC technology, timers, real-time clock, temperature sensor, serial and digital peripherals in a single-chip solution.

Power Efficiency
Arm® Cortex®-M0+ with advanced power optimization. Four power modes integrated.

Ease of Use
Leveraging NXP's LPC8N04 Board support package and refence designs to jump-start the design

Enablement and Tools
Low-cost LPC8N04 Development Board, compatible with MCUXpresso IDE and other popular toolchains.

For more info, visit www.nxp.com/LPC

Related Resources

- LPC8N04 Webpage: http://www.nxp.com/LPC8N04
- LPC8N04 Development Board: http://www.nxp.com/demoboard/OM40002
- LPC8N04-based IoT Node: www.nxp.com/LPC8N04-IoTNode
- LPC Microcontroller Community: https://community.nxp.com/community/lpc

For More Information

- OM40002 Reference Manual
  - User Manual for LPC8N04 Development Board (REV 1.1)
- Printed Circuit Boards
  - Board design files for LPC8N04 Revision B(REV 0)
- Encrypted OTA FW update using NFC
  - TN00040
- Antenna Design
  - AN11276
- Testing code
  - KEIL&IAR
  - MCUXpresso

SECURE CONNECTIONS
FOR A SMARTER WORLD

BACK UP

PINNING
PACKAGE

LPC8N04 Product Overview

LPC8N04FHI24

MEMORY (Kbyte)	
Flash	32
SRAM	8
EEPROM	4
NFC tag	
	NFC/RFID ISO 14443 type A interface
Serial Communication	
I^2C	1
SPI	1
TIMERS	
Ctimer	2
GPIO	
	12
Package	 HVQFN24 (4x4x0.85mm)

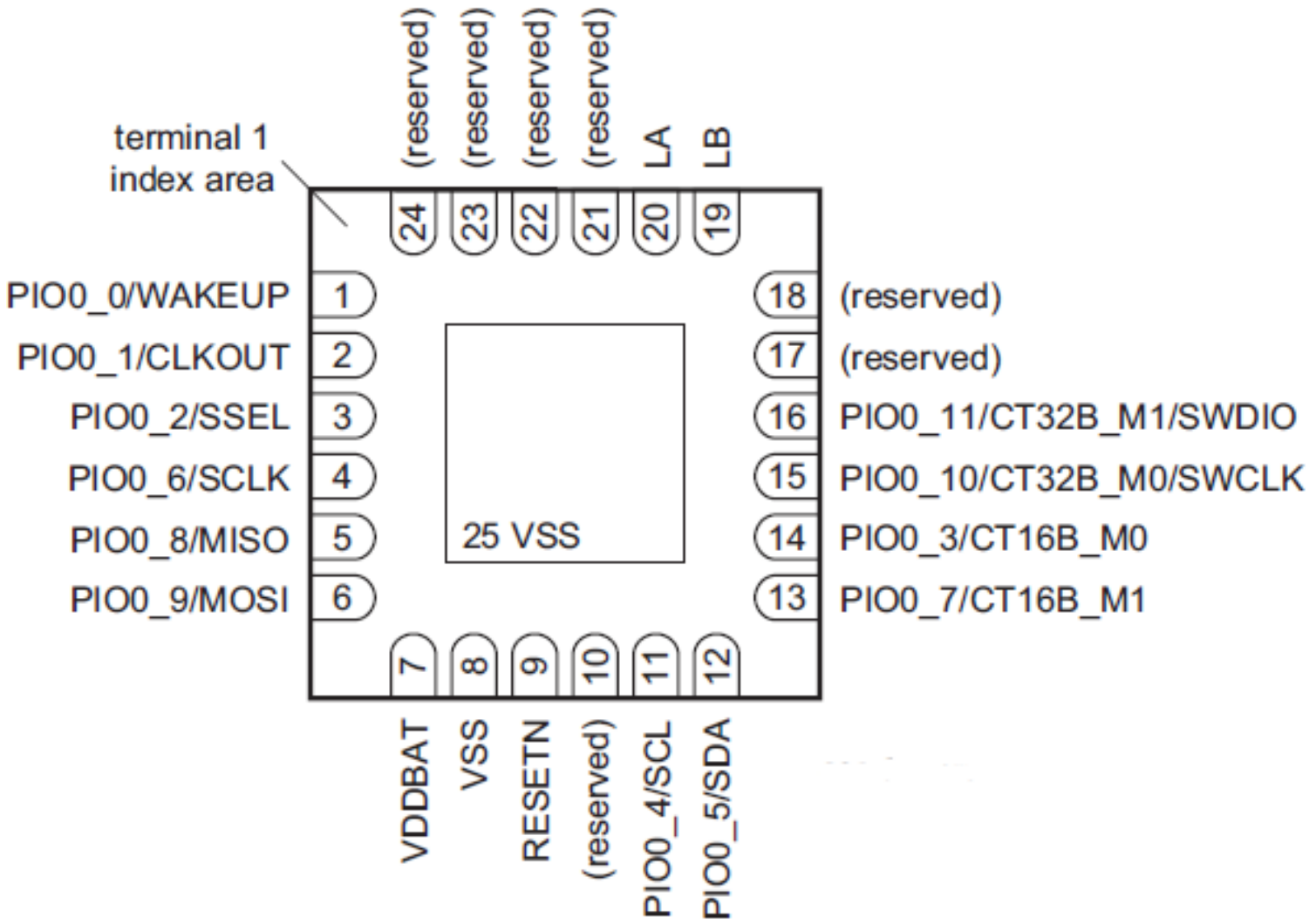
LPC8N04FHI24E
(935359392551)

Tray, Bakeable, Single in Drypack
Min. Packing Quantity:490

LPC8N04FHI24Z
(935359392515)

Reel 7" Q1/T1 in Drypack
Min. Packing Quantity:1500

LPC8N04 PINNING HVQFN24



LPC8N04 PINNING

- PIO0_3, PIO0_7, PIO0_10, and PIO0_11 are high-drive pads that can deliver up to 20 mA to the load

Pad	Symbol	Pad	Symbol
1	PIO0_0/WAKEUP	13[1]	PIO0_7/CT16B_M1
2	PIO0_1/CLKOUT	14[1]	PIO0_3/CT16B_M0
3	PIO0_2/SSEL	15[1]	PIO0_10/CT32B_M0/SWCLK
4	PIO0_6/SCLK	16[1]	PIO0_11/CT32B_M1/SWDIO
5	PIO0_8/MISO	17[2]	AN0_5
6	PIO0_9/MOSI	18[2]	AN0_4
7	VDDBAT	19	LB
8	VSS	20	LA
9	RESETN	21[2]	AN0_3
10	(reserved)	22[2]	AN0_2
11	PIO0_4/SCL	23[2]	AN0_1
12	PIO0_5/IDA	24[2]	AN0_0

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