

MCUXPRESSO IDE, SDK AND CONFIG TOOLS TRAINING

HAND ON BASED ON LPC54608



7th Jul 2017



SECURE CONNECTIONS
FOR A SMARTER WORLD

AGENDA

- **MCUXpresso Software And Tools Overview**
- **MCUXpresso SDK**
 - Web Builder
 - File Structure
- **MCUXpresso IDE**
 - Importing/Building
 - Debugging
- **MCUXpresso Config Tool**
 - Project Cloner
 - Pins Tool
 - Clocks Tool
- **LPC54608 LCD Lab, Key API and EmWin Demo**

MCUXPRESSO SOFTWARE AND TOOLS OVERVIEW





MCUXpresso Software and Tools

COMMON TOOLKIT
FOR THOUSANDS
OF KINETIS® & LPC
MICROCONTROLLERS



www.nxp.com/mcuxpresso



MCUXpresso Software and Tools for Kinetis and LPC microcontrollers



MCUXpresso IDE

Edit, compile, debug and optimize in an intuitive and powerful IDE



MCUXpresso SDK

Runtime software including peripheral drivers, middleware, RTOS, demos and more



MCUXpresso Config Tools

Online and desktop tool suite for system configuration and optimization



MCUXpresso Software and Tools

- Common toolkit across Kinetis and LPC microcontrollers
- Easy to use
- High quality
- Shared software experience and broader portfolio support
- Offers easy migration and scalability
- Supports large ARM® Cortex®-M ecosystem
- Built on the 'best of' Kinetis SDK, LPCXpresso and Kinetis Design Studio IDEs



MCUXpresso Software and Tools

- IDE
- SDK
- Config Tools

For NXP's ARM® Cortex®-M controllers

- Kinetis MCUs
- LPC Microcontrollers
- i.MX Application Processors



MCUXpresso Software & Tools — Products

Integrated Development Environment (IDE)



- Offers edit, compile, debug, and many more tools with an intuitive and powerful interface
- Brings “best of” legacy IDEs (LPCXpresso and Kinetis® Design Studio) together, including GNU tool integration and library, multicore capable debugger, as well as trace functionality
- Debug connections that support all Freedom, Tower®, and LPCXpresso development boards plus industry leading commercial debug probes

Software Development Kit (SDK)



- The software framework and reference for application development with NXP’s MCUs based on ARM® Cortex®-M cores
- Includes production-grade software with integrated RTOS, integrated stacks and middleware, reference software, and more
- Highest quality with MISRA compliance on all drivers; checked with Coverity® static analysis tools
- Available in custom downloads based on user selections of MCU, evaluation board, and optional software components

System Configuration Tools



- Integrated configuration and development tools for Kinetis, LPC and i.MX products
- A suite of evaluation and configuration tools that helps guide users from first evaluation to production software development
- Includes SDK builder, power estimator, pins and clocks tools
- Available in online and desktop versions



Origins of MCUXpresso Software & Tools

Kinetis and LPC SW

Independent software and tools

MCUXpresso Software and Tools

Supporting Kinetis & LPC Cortex-M MCUs

LPCXpresso IDE
& Kinetis Design Studio



MCUXpresso IDE

Kinetis SDKv2



MCUXpresso SDK

Kinetis Expert



MCUXpresso Config Tools



MCUXpresso IDE



Free Eclipse and GCC-based IDE for C/C++ development on Kinetis and LPC MCUs

Learn more at: www.nxp.com/mcuxpresso/ide



Product Features

- **Feature-rich, unlimited code size**, optimized for **ease-of-use**, based on **industry standard Eclipse** framework for **NXP's Kinetis and LPC MCUs**
- **Application development** with Eclipse and GCC-based IDE for advanced **editing, compiling and debugging**
- Supports **custom** development boards, **Freedom, Tower** and **LPCXpresso** boards with debug probes from **NXP, P&E** and **Segger**
- **Free Edition:** Full Featured, **unlimited Code Size**, no special activation needed, community based support
- **Pro Edition:** Email IDE support, **Advanced Trace Features**

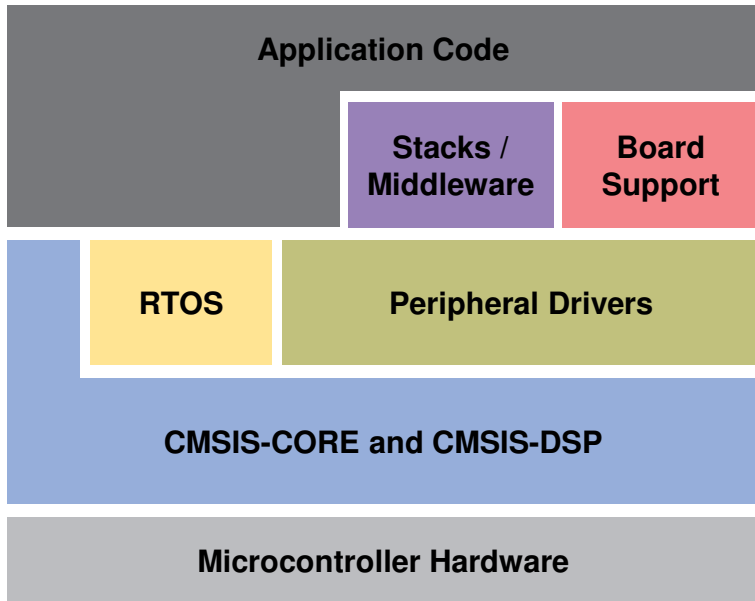
MCUXpresso IDE					
Eclipse Framework for C/C++, extensible with many plugins					
Quickstart Panel	Support for SDK and LPCOpen for ARM@ Cortex@-M Cores		Peripheral View	Power Measurement	
Advanced Build Scripts	Combined Development Perspective		Instruction Trace	SWO Trace / Profiling	
New Project Wizard			Linker and Memory Configuration	Data Watching	FreeRTOS Kernel Awareness
ARM GCC			ARM GDBC		
newlib	newlib-nano	RebLib	CMSIS-DAP	P&E	Segger



MCUXpresso SDK



The software framework and reference for Kinetis & LPC MCU application development



Learn more at: www.nxp.com/mcuxpresso/sdk



Product Features

Architecture:

- CMSIS-CORE compatible
- Single driver for each peripheral
- Transactional APIs w/ optional DMA support for communication peripherals

Integrated RTOS:

- FreeRTOS v9
- RTOS-native driver wrappers

Integrated Stacks and Middleware

- USB Host, Device and OTG
- lwIP, FatFS
- Crypto acceleration plus wolfSSL & mbedTLS
- SD and eMMC card support

Reference Software:

- Peripheral driver usage examples
- Application demos
- FreeRTOS usage demos

License:

- BSD 3-clause for startup, drivers, USB stack

Toolchains:

- MCUXpresso IDE
- IAR®, ARM® Keil®, GCC w/ Cmake

Quality

- Production-grade software
- MISRA 2004 compliance
- Checked with Coverity® static analysis tools

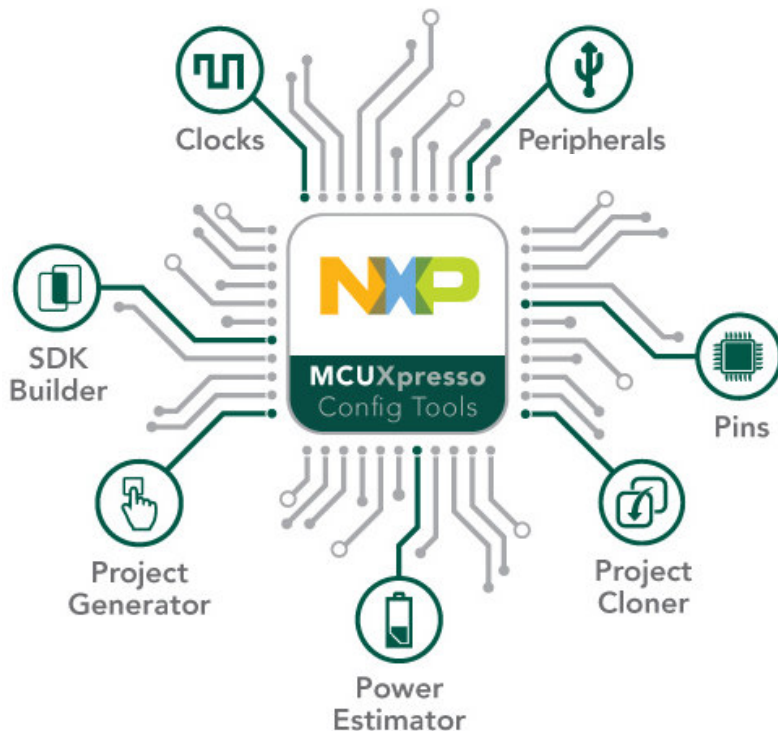


MCUXpresso Config Tools

Learn more at: www.nxp.com/mcuxpresso/config



Integrated configuration and development tools for LPC and Kinetis MCUs



MCUXpresso Config Tools is a suite of evaluation and configuration tools that helps guide users from first evaluation to production software development.



SDK Builder packages custom SDKs based on user selections of MCU, evaluation board, and optional software components.



Pins, **Clocks**, and **Peripheral** tools generate initialization C code for custom board support. Features validation of inputs and cross-tool conflict resolution.



Project Generator creates new SDK projects with generated Pins and Clocks source files.



Project Cloning creates a standalone SDK project based on an example application available within SDK release.



Power Estimation tool provides energy and battery-life estimates based on a user's application model.

Available as a standalone tool for select devices.





MCUXpresso
Software and Tools

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MICROCONTROLLERS



www.nxp.com/mcuxpresso

MCUXpresso Software and Tools Additional Resources

Web pages

- MCUXpresso Software and Tools – www.nxp.com/mcuxpresso
 - MCUXpresso SDK – www.nxp.com/mcuxpresso/sdk
 - MCUXpresso IDE – www.nxp.com/mcuxpresso/ide
 - MCUXpresso Config Tools – www.nxp.com/mcuxpresso/config

Supported Devices

- [Supported Devices Table \(Community Doc\)](#)

Communities

- MCUXpresso Software and Tools –
<https://community.nxp.com/community/mcuxpresso>
 - MCUXpresso SDK:
<https://community.nxp.com/community/mcuxpresso/mcuxpresso-sdk>
 - MCUXpresso IDE:
<https://community.nxp.com/community/mcuxpresso/mcuxpresso-ide>
 - MCUXpresso Config Tools:
<https://community.nxp.com/community/mcuxpresso/mcuxpresso-config>



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MCUXPRESSO SDK



MCUXPRESSO SDK WEB BUILDER



MCUXpresso Homepage

NXP MCUXpresso OVERVIEW TOOLS MANAGE English Guest

MCUXpresso Config Tools

MCUXpresso Config Tools provides a set of system configuration tools that help users of all levels with a Kinetis or LPC-based MCU solution. Let it be your guide from first evaluation to production development.

Select or create a configuration
Login to view configurations

- Config Settings**
Specify optional middleware and environment settings for your configuration
- SDK Builder**
Generate a downloadable SDK archive for use with desktop MCUXpresso Tools
- Pins Tool**
Assign signals to pins, set electrical properties, and generate initialization code
- Clocks Tool**
Setup the system clocks and generate initialization code

Feedback

What's new Additional Links

<https://mcuxpresso.nxp.com/en/welcome>

Configuration

- What is a configuration?
 - A group of configured settings used across the MCUXpresso configuration tools (SDK builder, Pins, and Clocks)
- What is included in a configuration?
 - SDK builder configuration settings (e.g. Board/Processor, Toolchain, Host OS, etc.)
 - Pin assignments in the Pins Tool
 - Clock initializations in the Clocks Tool
- Configurations can be saved and shared as a .mex file

Get Started

1. Login

MCUXpresso Config Tools

MCUXpresso Config Tools provides a set of system configuration tools that help users of all levels with a Kinetis or LPC-based MCU solution. Let it be your guide from first evaluation to production development.

Select or create a configuration

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Config Settings
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SDK Builder
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Pins Tool
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Clocks Tool
Setup the system clocks and generate initialization code

What's new Additional Links

Routed to
nxp.com

2. Enter account info

Sign in

Email Address

Password

Remember me

Sign in

Forgot your password?

Not yet registered?
Start here to become a new member

Register

Why register?

- Get easy access to all your embedded design needs when you register on nxp.com
- Download software and tools
- Order product samples
- Get technical help
- Access on-demand training and register for the courses
- Receive weekly Design News to stay up-to-date—particularly with errata and new documentation
- Track your browsing history for easy access to previously viewed items
- System Update: NXP support tickets area now uses your new nxp.com email and password. Login to [www.nxp.com](#) to see existing tickets. If you don't have an account, register here.

Still having trouble logging in?
If this is your first sign, you will be required to review and agree to the Access Agreement. Once access is granted. By clicking "Register" you signify your ACCEPTANCE OF THE TERMS contained in the Access Agreement.

Return to
mcuxpresso.nxp.com

3. Start New Configuration

MCUXpresso Config Tools

MCUXpresso Config Tools provides a set of system configuration tools that help users of all levels with a Kinetis or LPC-based MCU solution. Let it be your guide from first evaluation to production development.

Select or create a configuration

- No configuration created yet

Config Settings
Specify optional middleware and environment settings for your configuration

SDK Builder
Generate a downloadable SDK archive for use with desktop MCUXpresso Tools

Pins Tool
Assign signals to pins, set electrical properties, and generate initialization code

Clocks Tool
Setup the system clocks and generate initialization code

What's new Additional Links

Create a New Configuration (1/3)

1. Type in search

Search by Name

LPC54608J512

Select a Device, Board, or Kit

- Boards
- Processors
 - LPC54608J512
- Kits

Name your configuration

Select Configuration Specify Additional Configuration Settings Jump start your configuration

(No configuration selected)

Create a New Configuration (2/3)

2. Make selection

Configuration name automatically assigned. Name can be modified



Create a New Configuration (3/3)

Select Configuration | M x

Secure | <https://mcuxpresso.nxp.com/en/select>

MCUXpresso OVERVIEW TOOLS - MANAGE -

English - Audrey -

Create a New Configuration

Search by device, board, kit name and filter by supported middleware.

Search by Name

lpc54608j512

Select a Device, Board, or Kit

- Boards
- Processors
 - LPC54608J512
- Kits

Name your configuration

LPC54608J512

Select Configuration Specify Additional Configuration Settings Jump start your configuration

Hardware Details

Included Part Numbers	LPC54608J512BD208, LPC54608J512ET180
Board(s)	LPCXpresso54608
Device	LPC54608
Core Type / Max Freq	Cortex-M4F / 180MHz
Memory Size	512 KB Flash 200 KB RAM

- Select Configuration
 - Proceed to builder with default options selected for toolchain, OS, and middleware
- Specify Additional Configuration Settings
 - Select toolchain, OS, and middleware other than default.

Additional Configuration Settings

- User selects:
 - Host OS
 - Toolchain/IDE
 - Middleware
- Defaults (first session):
 - Host OS -> **Windows**
 - IDE -> **MCUXpresso**
 - Middleware -> **FatFS, USB Stack*, lwIP***

Configuration Settings | x

Secure | https://mcuxpresso.nxp.com/en/configuration-settings

MCUXpresso OVERVIEW TOOLS MANAGE

English Audrey

Configuration Settings

Specify included middleware, RTOS selections, and development preferences.

Current Configuration

LPC54608J512

Developer Environment Settings

Selections here will impact files and examples projects included in the SDK Download and Generated Projects

Host OS: Windows

Toolchain / IDE: MCUXpresso IDE

Set as default

Select Optional Middleware

Selections here will be included in your SDK download, generated projects, and will impact Peripheral Tool settings

3 items selected

Selected Middleware: FatFS, USB stack, lwIP

Hardware Details

Included Part Numbers	LPC54608J512BD208, LPC54608J512ET160
Board(s)	LPCXpresso54608
Device	LPC54608
Core Type / Max Freq	Cortex-M4F / 180MHz
Memory Size	512 KB Flash 200 KB RAM

Return to Overview Go to SDK Builder Jump start your configuration

Additional Configuration Settings: Choose an OS

NXP MCUXpresso OVERVIEW TOOLS ▾ MANAGE ▾ English ▾ Bryan ▾

Configuration Settings

Specify included middleware, RTOS selections, and development preferences.

Current Configuration

LPC54608J512

Select a host operating system for which the package will be generated. Examples projects included in the SDK Download and Generated Projects

Host OS: Windows (selected), macOS, Linux

Toolchain / IDE: MCUXpresso IDE

Set as default

3 items selected

Selected Middleware: FatFS, USB stack, lwIP

Return to Overview | Go to SDK Builder

Hardware Details

Board	FRDM-K64F
Device	MK64F12
Core Type / Max Freq	Cortex-M4F / 120MHz
Memory Size	1024 KB Flash 256 KB RAM

Feedback

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Additional Configuration Settings: Choose an IDE

Configuration Settings
Specify included middleware, RTOS selections, and development preferences.

Current Configuration
LPC54608J512

Developer Environment Settings
Select a toolchain for which the package will be generated.

Host OS: Windows

Toolchain IDE: MCUXpresso IDE

Select Optional Middleware: 3 items selected

Hardware Details:

Included Part Numbers	LPC54605J512ET180
Board(s)	LPCXpresso54608
Device	LPC54605
Core Type / Max Freq	Cortex-M4F / 180MHz
Memory Size	512 KB Flash 200 KB RAM

Buttons: Return to Overview, Go to SDK Builder

Feedback

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Additional Configuration Settings: Choose Middleware/RTOS

Configuration Settings

RTOS selections, and development preferences.

Middleware

- CMSIS DSP Library
- FatFS ✓
- ISSDK
- NTAG I2C
- USB stack ✓
- emWin
- lwIP ✓
- mbedtls

Operating systems

FreeRTOS

3 items selected

Selected Middleware

FatFS, USB stack, lwIP

Hardware Details

Board	FRDM-K64F
Device	MK64F12
Core Type / Max Freq	Cortex-M4F / 120MHz
Memory Size	1024 KB Flash 256 KB RAM

Return to Overview | Go to SDK Builder

Feedback

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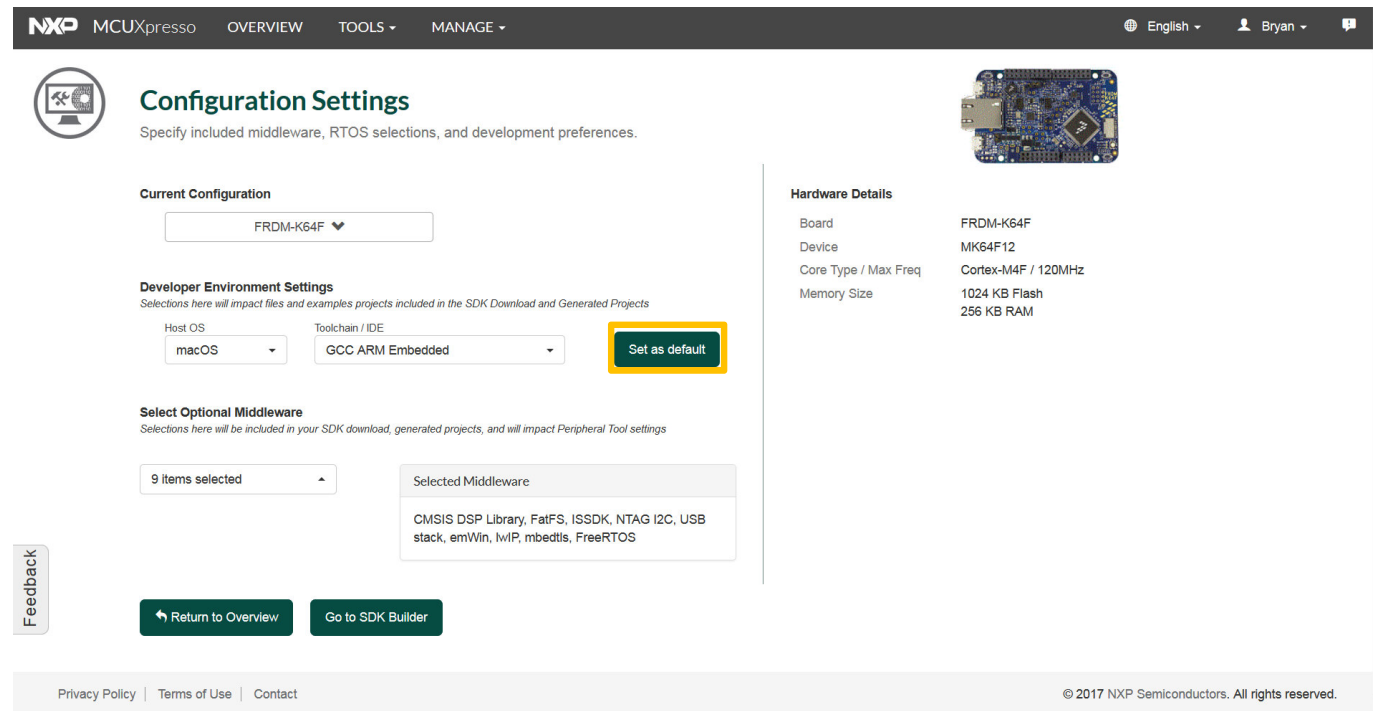
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Select
Middleware



Change Default Build Settings

- Select “Set as Default” to save Host OS and Toolchain to preferences
- Future configurations will use these build settings as defaults



NXP MCUXpresso OVERVIEW TOOLS MANAGE English Bryan

Configuration Settings

Specify included middleware, RTOS selections, and development preferences.

Current Configuration
FRDM-K64F

Developer Environment Settings
Selections here will impact files and examples projects included in the SDK Download and Generated Projects

Host OS: macOS | Toolchain / IDE: GCC ARM Embedded | **Set as default**

Select Optional Middleware
Selections here will be included in your SDK download, generated projects, and will impact Peripheral Tool settings

9 items selected

Selected Middleware
CMSIS DSP Library, FatFS, ISSDK, NTAG I2C, USB stack, emWin, lwIP, mbedtis, FreeRTOS

Hardware Details

Board	FRDM-K64F
Device	MK64F12
Core Type / Max Freq	Cortex-M4F / 120MHz
Memory Size	1024 KB Flash 256 KB RAM

Feedback

[Return to Overview](#) [Go to SDK Builder](#)

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Finish Settings

The screenshot shows the 'Configuration Settings' page for the NXP MCUXpresso IDE. The browser address bar shows the URL <https://mcuxpresso.nxp.com/en/configuration-settings>. The page title is 'Configuration Settings' with a subtitle 'Specify included middleware, RTOS selections, and development preferences.' The 'Current Configuration' section shows 'LPC54608J512' selected. The 'Developer Environment Settings' section includes 'Host OS' set to 'Windows' and 'Toolchain / IDE' set to 'MCUXpresso IDE', with a 'Set as default' button. The 'Select Optional Middleware' section shows '3 items selected' and a list of 'Selected Middleware' including 'FatFS, USB stack, IwIP'. The 'Hardware Details' section lists: 'Included Part Numbers: LPC54608J512B0208, LPC54608J512ET160', 'Board(s): LPCXpresso54608', 'Device: LPC54608', 'Core Type / Max Freq: Cortex-M4F / 180MHz', and 'Memory Size: 512 KB Flash, 200 KB RAM'. At the bottom, there are three buttons: 'Return to Overview', 'Go to SDK Builder' (highlighted with a red box), and 'Jump start your configuration'.

Build SDK

Summary | MCUxpresso x Audrey

Secure | https://mcuxpresso.nxp.com/en/builder

MCUXpresso OVERVIEW TOOLS MANAGE English Audrey

SDK Builder

Generate a downloadable SDK archive for use with desktop MCUxpresso Tools.

Current Configuration
LPC54608.J512

Review SDK Details
Items listed on the side panel will be included in your SDK download.
These selections can be edited using the Tools -> Configurations Settings page

This MCUxpresso SDK configuration is available for direct download

Download Now

Package Name
SDK 2.2.LPC54608.J512

SDK Configuration

Hardware Details

Included Part Numbers	LPC54608.J512BD208, LPC54608.J512ET180
Board(s)	LPCxpresso54608
Device	LPC54608
Core Type / Max Freq	Cortex-M4F / 180MHz
Memory Size	512 KB Flash 200 KB RAM

SDK Details [Edit](#)

SDK Version:	KSDK 2.2.0
Host OS:	Windows
Toolchain:	MCUXpresso IDE
Middleware:	FatFS, USB stack, lwIP

Documentation

Base SDK: [MCUXpresso SDK API Reference Manual](#)

After reviewing configuration, click to download SDK

Download SDK

Software Terms and Conditions

Please read the following agreement and click "I AGREE" at the bottom before downloading your software.

EULA Software Content Registry

LA_OPT_BASE_LICENSE v17 December 2016

IMPORTANT. Read the following NXP Software License Agreement ("Agreement") completely. By selecting the "I Accept" button at the end of this page, you indicate that you accept the terms of the Agreement and you acknowledge that you have the authority, for yourself or on behalf of your company, to bind your company to these terms. You may then download or install the file.

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1. DEFINITIONS

1.1. For NXP the term "Affiliate" includes entities Controlled by NXP where "Control" means direct or indirect beneficial ownership of more than fifty percent (50%) of the voting stock, or decision-making authority in the event that there is no voting stock, in another entity.

[SDK_2.2_LPC54608J512.zip](#)

Download SDK Build Archive Item

If your download does not start after 10 seconds, please click the following link to initiate package download:

[SDK_2.2_LPC54608J512.xip](#)

[Return to SDK Builder](#)

Opening SDK_2.2_FRDM-K54F.zip

You have chosen to open:

- Sdk_2.2.LPC54608J512 which is: WinZip File (92.3 MB) from: http://nx-stage.freescale.net

What should Firefox do with this file?

Open with WinZip (default)

Save File

Do this automatically for files like this from now on.

Feedback

Click to Agree to terms and conditions

SDK download will begin

Feedback

Save SDK once build completes



Request Build

- In some occasions, if the SDK configuration has not previously been built, “Request Build” will be displayed in place of “Download Now”
- An email notification with direct link will be sent once the build is finished

The screenshot shows the NXP MCUXpresso SDK Builder web interface. The top navigation bar includes the NXP logo, 'MCUXpresso', 'OVERVIEW', 'TOOLS', and 'MANAGE'. The user is logged in as 'Bryan'. The main content area is titled 'SDK Builder' and includes a sub-header 'Generate a downloadable SDK archive for use with desktop MCUXpresso Tools.' Below this, the 'Current Configuration' is set to 'LPC54608J512'. A 'Request Build' button is visible. The 'Review SDK Details' section provides instructions on how to edit configurations. A 'Building!' notification indicates that the build has started. The 'Hardware Details' section lists the board (FRDM-KL43Z), device (MKL43Z4), core type (Cortex-MQP / 48MHz), and memory (256 KB Flash, 32 KB RAM). The 'SDK Details' section shows the SDK version (KSDK 2.2.0), host OS (Windows), toolchain (MCUXpresso IDE), and middleware (CMSIS DSP Library, FatFS, NTAG I2C, FreeRTOS). The footer contains links for 'Privacy Policy', 'Terms of Use', and 'Contact', along with the copyright notice '© 2017 NXP Semiconductors. All rights reserved.'

Build Archive

Access SDK Archive from Manage menu





Build Archive

Remove all

SDK Packages

Show 10 entries

Search:

Name	Configuration	Date	Actions
SDK_2.2_LPC54608J512 Device: LPC54608J512, SDK version: KSDK 2.2.0, OS: Windows, Toolchain: MCUXPRESSO. Selected optional items: FatFS, IWP, USB stack Package hash: 65a3cde62d9301aa15e2eede76429eb8 (57MB)	LPC54608J512	2017-06-16 09:09 AM GMT	 

Shows all SDK builds

Download/ Delete SDK build



Download SDK

Click to Agree to terms and conditions

➔
SDK download will begin

Save SDK once build completes

Configurations Archive

Access Configuration Archive from Manage menu

Switch Configurations
LPC54608J512



Create a New Configuration
Start a new configuration for a specific NXP device, development board, or development kit.

Manage Existing Configurations
Create, Delete, Edit, and Share an existing configuration.

SDK Archive
Download a previously requested SDK build or download package via hash

SDK Packages

Show 10 entries

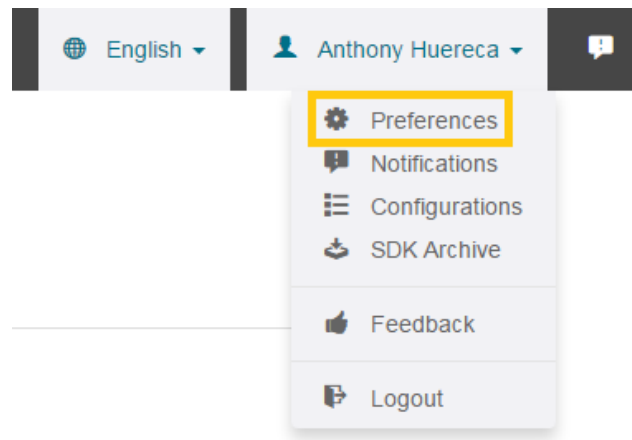
Name	Configuration	Date	Actions
SDK_2.2_LPC54608J512 Device: LPC54608J512, SDK version: KSDK 2.2.0, OS: Windows, Toolchain: MCUXPRESSO, Selected optional items: FatFS, lwIP, USB stack Package hash: 65a3cde62d9301aa15e2eede76429eb8 (57MB)	LPC54608J512	2017-06-19 01:52 AM GMT	 

Current configuration

Upload a configuration

Preferences

- First time users may see an error if they have not filled out profile in “Preferences” as required for export control compliance
 - Name
 - Company
 - Country
 - Project Description



MCUXPRESSO SDK STRUCTURE

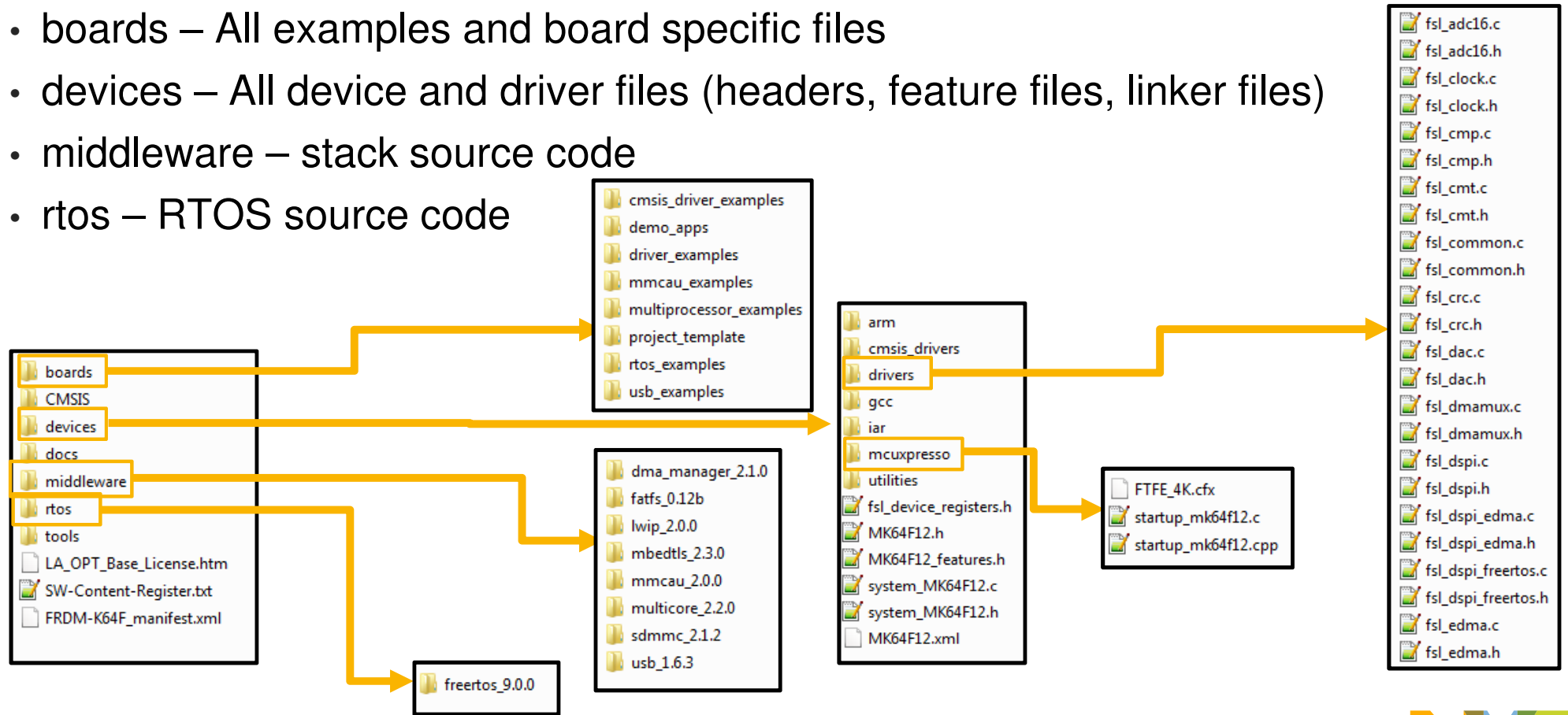


Zip or Unzip an SDK package

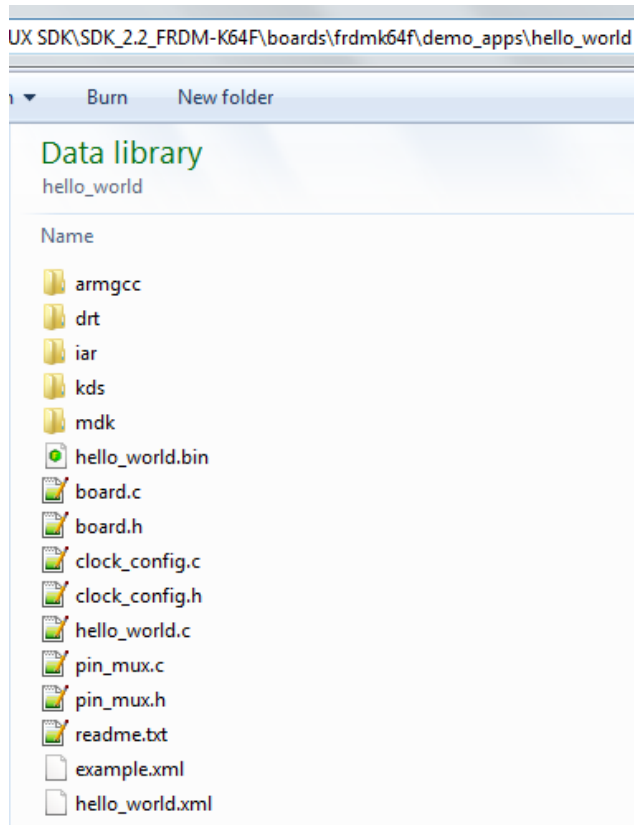
- SDK packages are downloaded as .zip files
- When using 3rd party IDEs, the SDK package must be unzipped
- For SDK support in the MCUXpresso Config Tools, the SDK package must also be unzipped
- MCUXpresso IDE can import SDK packages in either zipped or unzipped format.
 - Zipped SDKs:
 - When creating new projects or importing example projects, SDK source files are copied into the workspace (no linked references).
 - Unzipped SDKs:
 - When creating new projects or importing example projects, SDK source files can be copied into the workspace or referenced directly (linked references).
 - Requires additional time to unzip (one-time).
 - Provides speed improvement when many examples are imported to the workspace.

MCUXpresso SDK File Structure

- boards – All examples and board specific files
- devices – All device and driver files (headers, feature files, linker files)
- middleware – stack source code
- rtos – RTOS source code



MCUX Expresso SDK File Structure - Examples



- Each example application has its own unique copy of the board, pin_mux, and clock_config files.
- Also each example also contains a pre-compiled .bin file for easy drag-and-drop programming
- Readme.txt contains instructions on how to run the demo and pins used

MCUXpresso File Structure - Examples

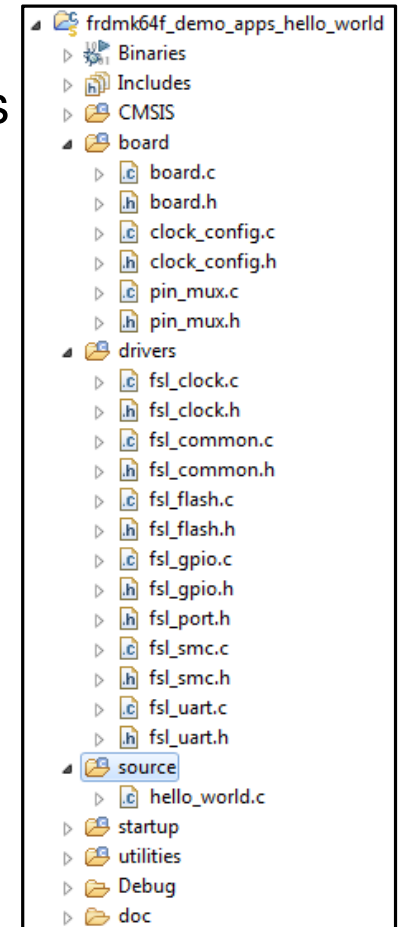
- Most configuration settings are in **board.h** file
 - UART module
 - UART baud
 - GPIO pins defined

```
44 /* The UART to use for debug messages. */
45 #define BOARD_DEBUG_UART_TYPE DEBUG_CONSOLE_DEVICE_TYPE_UART
46 #define BOARD_DEBUG_UART_BASEADDR (uint32_t) UART0
47 #define BOARD_DEBUG_UART_CLKSRC SYS_CLK
48 #define BOARD_DEBUG_UART_CLK_FREQ CLOCK_GetCoreSysClkFreq()
49 #define BOARD_UART_IRQ UART0_RX_TX_IRQn
50 #define BOARD_UART_IRQ_HANDLER UART0_RX_TX_IRQHandler
51
52 #ifndef BOARD_DEBUG_UART_BAUDRATE
53 #define BOARD_DEBUG_UART_BAUDRATE 115200
54 #endif /* BOARD_DEBUG_UART_BAUDRATE */
55
56 /* Define the port interrupt number for the board switches */
57 #define BOARD_SW2_GPIO GPIOC
58 #define BOARD_SW2_PORT PORTC
59 #define BOARD_SW2_GPIO_PIN 6U
60 #define BOARD_SW2_IRQ PORTC_IRQn
61 #define BOARD_SW2_IRQ_HANDLER PORTC_IRQHandler
62 #define BOARD_SW2_NAME "SW2"
63
```

- Default UART pins defined in pin_mux.c in BOARD_InitPins().

MCUXpresso SDK Projects

- All source files are included in the example application projects
- Drivers are found under the **drivers** folder
- Board specific files under the **board** folder
- Application specific files under **source** folder



MCUXpresso SDK Startup

- Reset_Handler found in \devices\\<compiler>\startup_<device>.s
 - Called ResetISR for MCUXpresso IDE
- SystemInit() found at \devices\\system_<device>.c is used to enable cache (if available) and disable the watchdog timer.
- Then jumps to main(), and three configuration functions run:
 - **BOARD_InitPins();**
 - **BOARD_BootClockRUN();**
 - **BOARD_InitDebugConsole();**

LAB 1



Lab 1 : To create a new SDK configuration online

- **Pre-requisites**

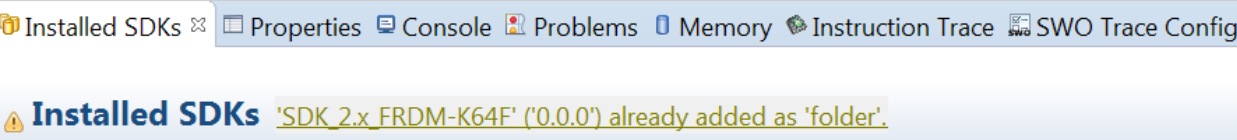
- PC running Windows/Linux/macOS
- Internet connection
- Follow the Lab1 Hand out
- Download SDK_2.2_LPC54608J512

WALKTHROUGH INSTALLED SDK



Copy of SDK made in default path

- What happens when an SDK is dragged/dropped into the IDE?
- The Drag/Drop feature creates a copy of the SDK located at **default path**:
C:\Users\“user_name”\mcuxpresso\SDKPackages

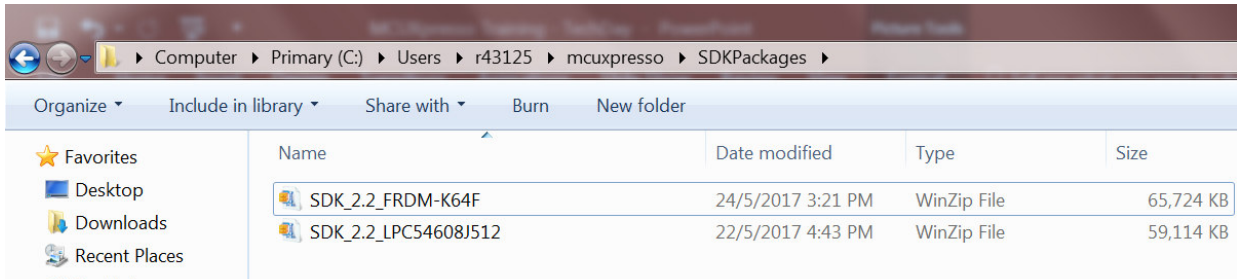


Installed SDKs Properties Console Problems Memory Instruction Trace SWO Trace Config

⚠ **Installed SDKs** 'SDK_2.x_FRDM-K64F' ('0.0.0') already added as 'folder'.

To install an SDK, simply drag and drop an SDK (zip file/folder) into the 'Installed SDKs' view.

Name	Version	Location
✓ # SDK_2.x_FRDM-K64F	2.2.0	<Default Location>/SDK_2.x_FRDM-K64F
✓ # SDK_2.x_LPC54608J512	2.2.0	<Default Location>/SDK_2.x_LPC54608J512

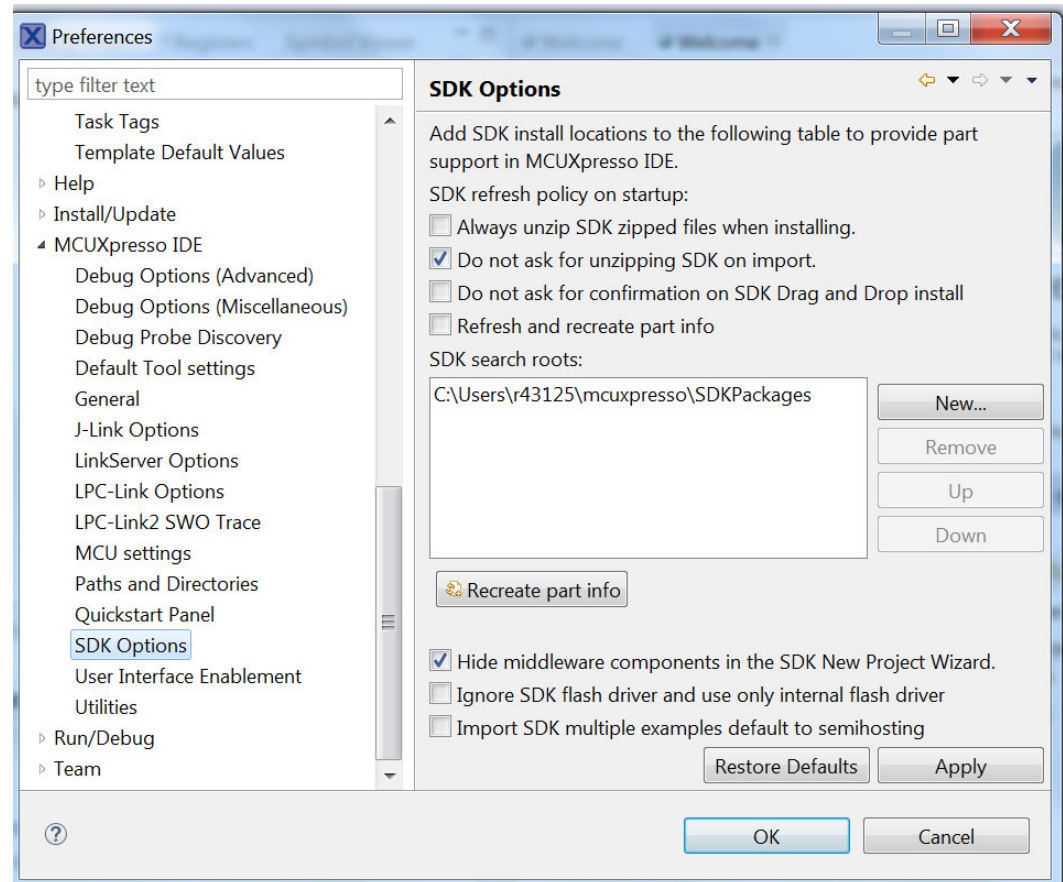


Computer > Primary (C:) > Users > r43125 > mcuxpresso > SDKPackages

Name	Date modified	Type	Size
SDK_2.2_FRDM-K64F	24/5/2017 3:21 PM	WinZip File	65,724 KB
SDK_2.2_LPC54608J512	22/5/2017 4:43 PM	WinZip File	59,114 KB

Install an SDK: Advanced

- Add paths to “SDK search roots:” for IDE to find current or future stored SDK packages
 - Window -> Preferences -> MCUXpresso IDE -> SDK Options
- SDKs can be zipped or unzipped
- For SDKs stored outside the default location:
 - “Delete SDK” function is disabled
 - Knowledge of SDKs is per workspace
- If multiple SDKs are found for the same device in various locations, you can choose which is loaded by reordering list (top has priority)
- Note: default location for drag/drop:
C:\Users\”user_name”\mcuxpresso\SDKPackages



AGENDA

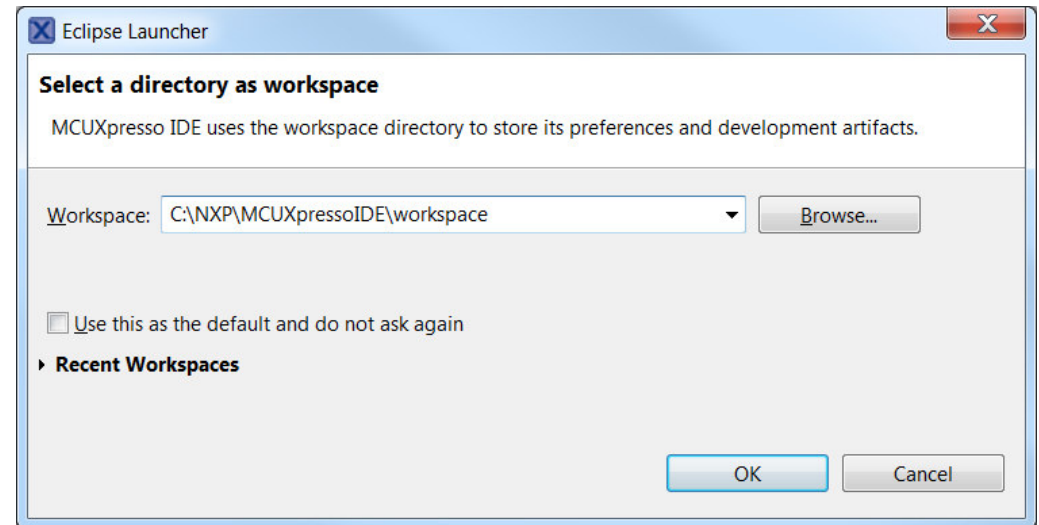
- **MCUXpresso Software And Tools Overview**
- **MCUXpresso SDK**
 - Web Builder
 - File Structure
- **MCUXpresso IDE**
 - Importing/Building
 - Debugging
- **MCUXpresso Config Tool**
 - Project Cloner
 - Pins Tool
 - Clocks Tool
- **LPC54608 LCD Lab, Key API and EmWin Demo**

MCUXPRESSO IDE



Open MCUXpresso IDE

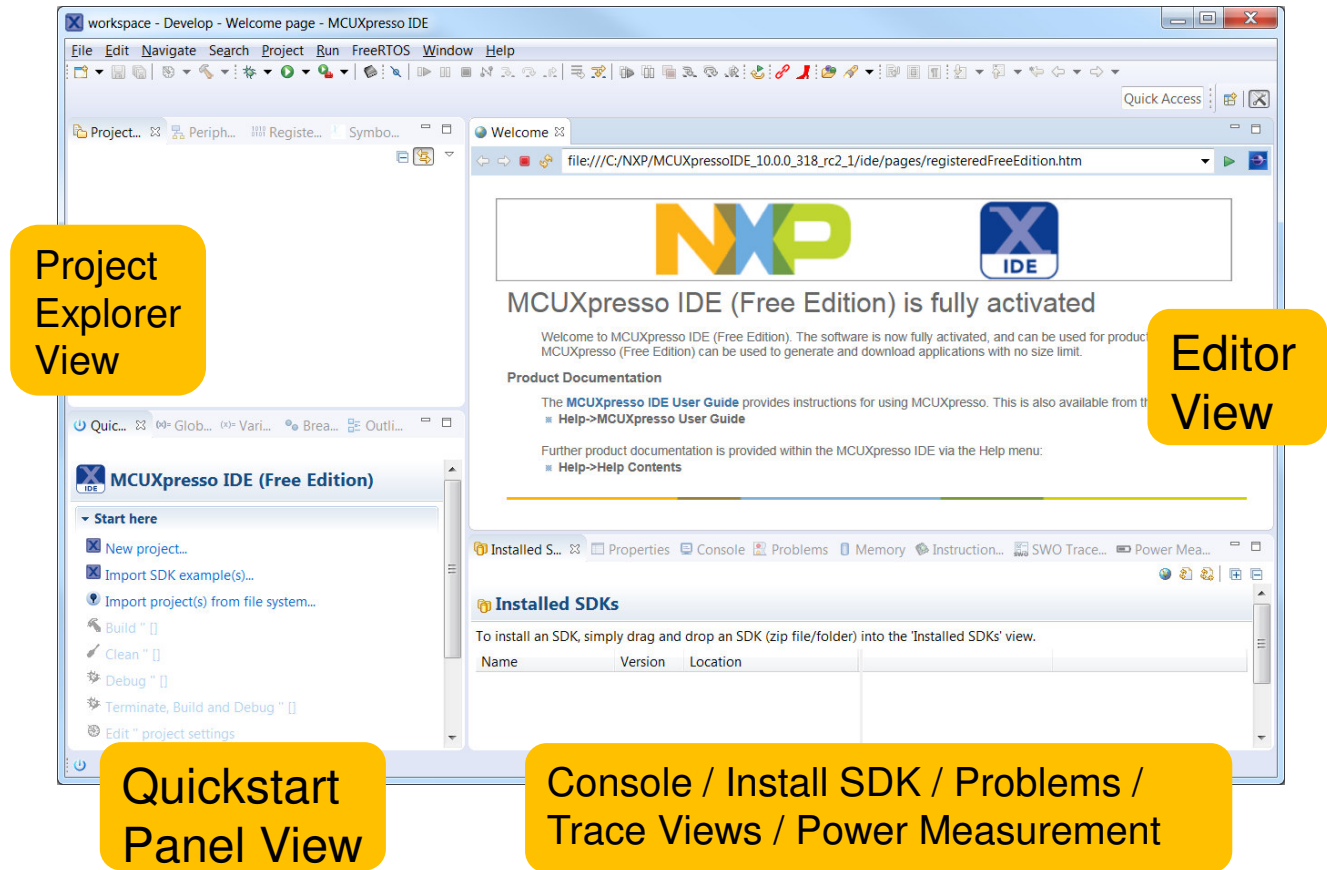
- Open MCUXpresso IDE on your system
- At the dialog box, enter a location for your workspace then click OK
 - Example)
C:\NXP\MCUXpressoIDE\workspace
- Note: A workspace is a directory used to store projects that you want to actively work on during the IDE session



www.nxp.com/mcuxpresso/ide

Develop Perspective

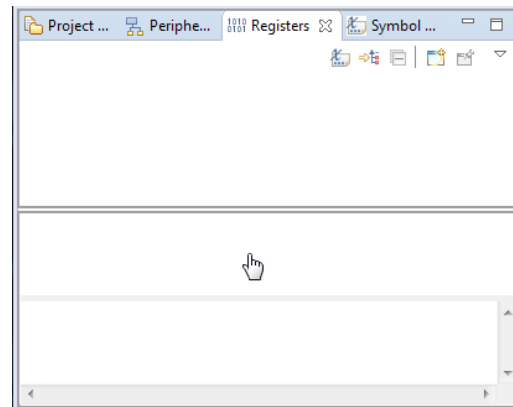
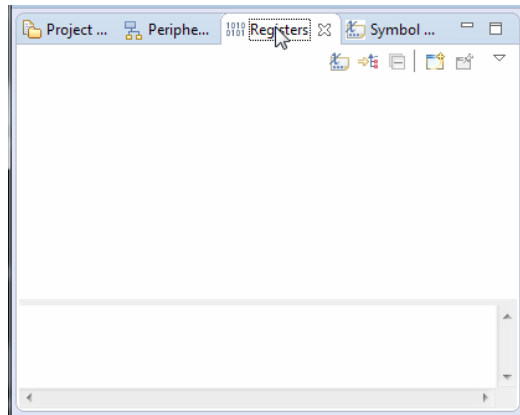
- MCUXpresso IDE will startup in a new workspace with no projects in the Develop Perspective
- A “perspective” is a collection of different “views”
- The Develop perspective provides a single combined project management and debugging view
- In addition to the default Develop perspective, the MCUXpresso IDE also supports traditional Eclipse C/C++ and Debug perspectives



Changing the Layout of the Develop Perspective

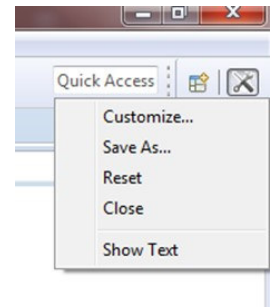
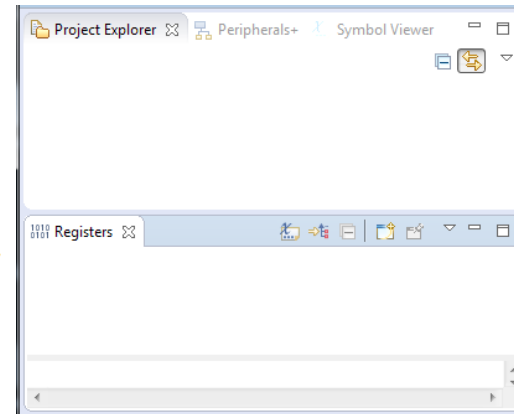
- Layout of views within a perspective can be tailored to meet your personal needs
- For example, if we wanted to have the Registers view always visible...

Click and hold down on the View you want to move



Continue to hold down and drag the cursor to the location you want to view to be displayed

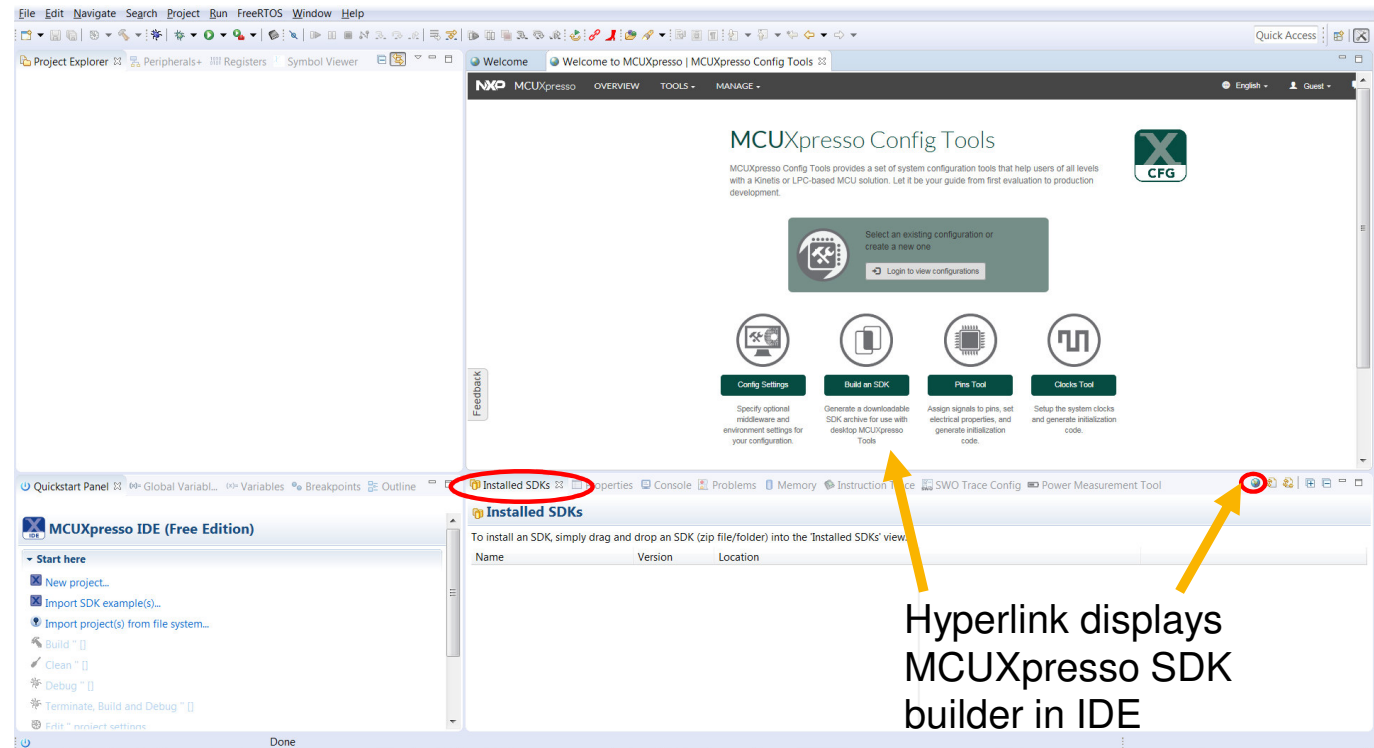
Then release the mouse click, and the view will be placed at the required position



Right click on the Perspective button (top right of IDE window) to reset the layout back to the default

Installing an SDK in the IDE

- Part support is added by installing MCUXpresso SDKs into the IDE
- Allows example projects and driver examples from SDK to be easily imported
- New project generation based on board or processor in SDK
- The IDE is only compatible with SDKs built for MCUXpresso

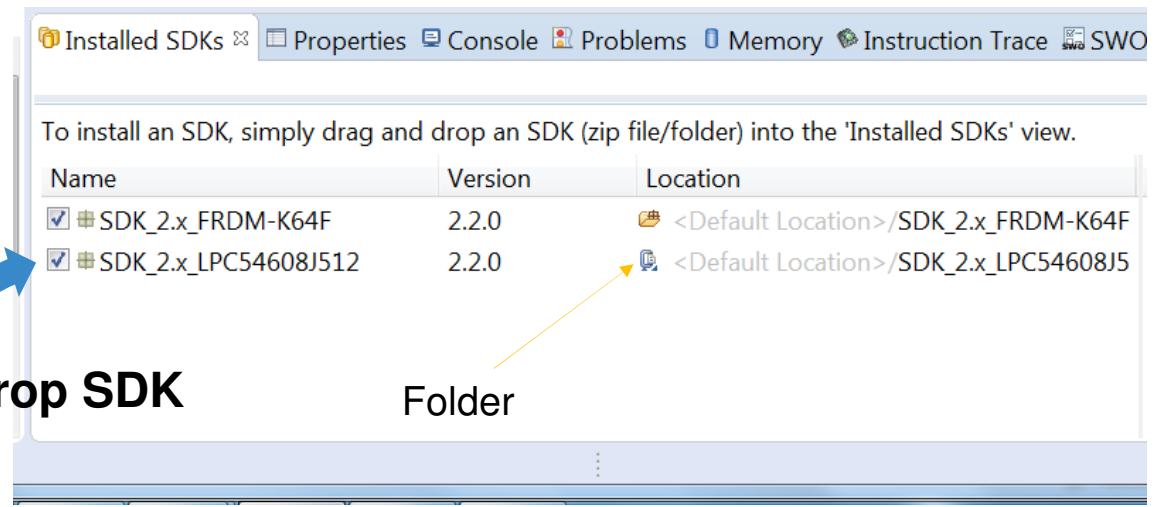


Install an SDK: Drag and Drop

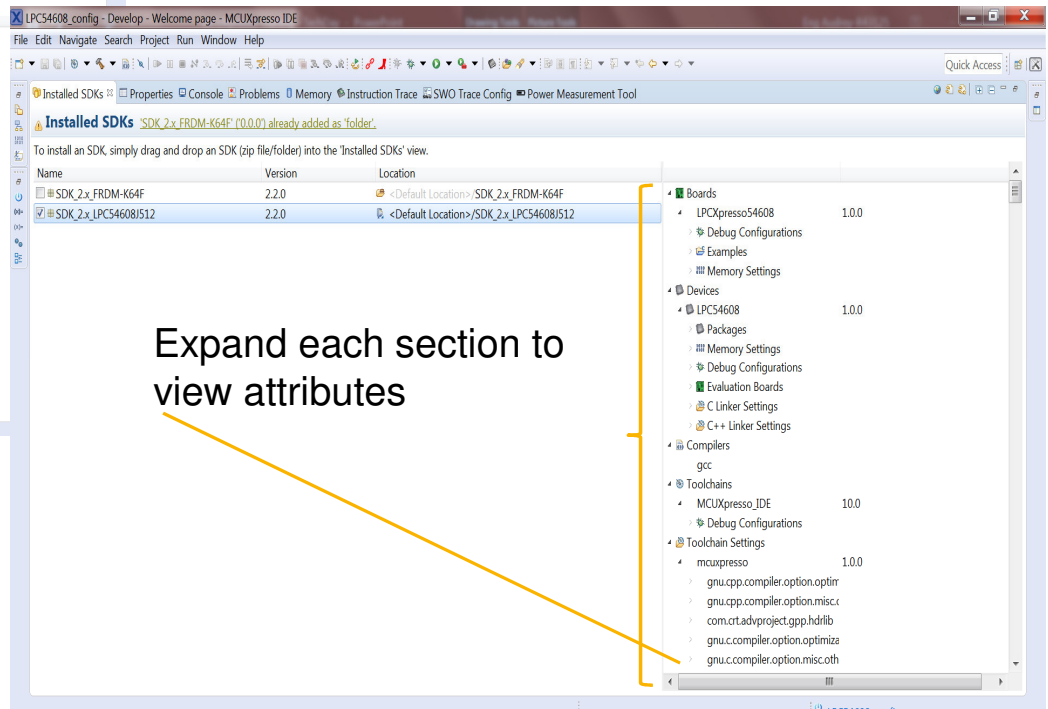
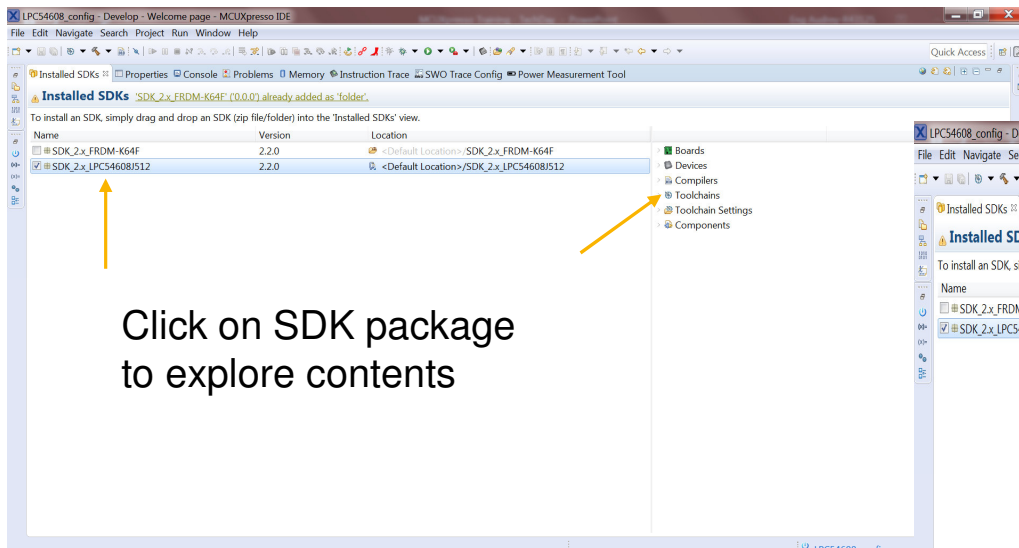
- Drag/Drop SDK packages directly into the IDE in the **Installed SDKs** view
- Can drag SDK as folder or zip (archive). IDE uses separate icon for each type
- SDKs installed in the default location are shared across workspaces

Drag and Drop SDK

Folder



Inspect SDK

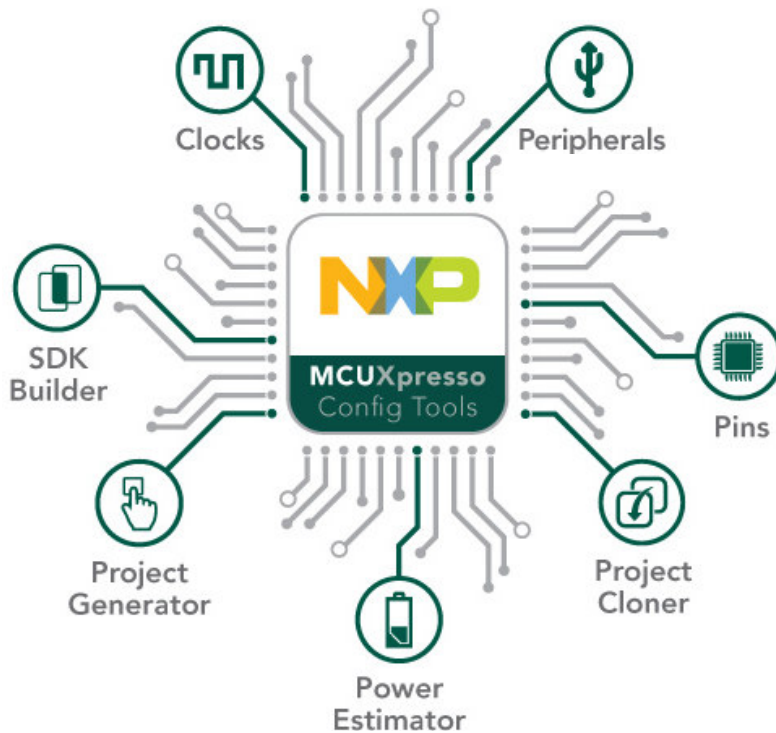


MCUXpresso Config Tools

Learn more at: www.nxp.com/mcuxpresso/config



Integrated configuration and development tools for LPC and Kinetis MCUs



MCUXpresso Config Tools is a suite of evaluation and configuration tools that helps guide users from first evaluation to production software development.



SDK Builder packages custom SDKs based on user selections of MCU, evaluation board, and optional software components.



Pins, **Clocks**, and **Peripheral** tools generate initialization C code for custom board support. Features validation of inputs and cross-tool conflict resolution.



Project Generator creates new SDK projects with generated Pins and Clocks source files.



Project Cloning creates a standalone SDK project based on an example application available within SDK release.



Power Estimation tool provides energy and battery-life estimates based on a user's application model.

Available as a standalone tool for select devices.



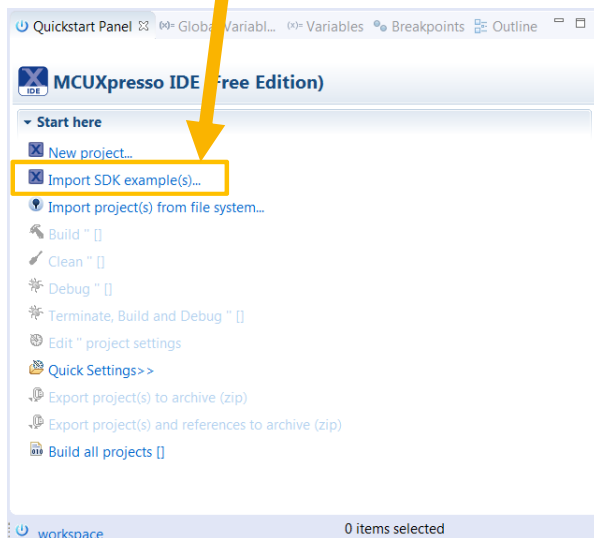
MCUXPRESSO IDE IMPORTING/BUILDING



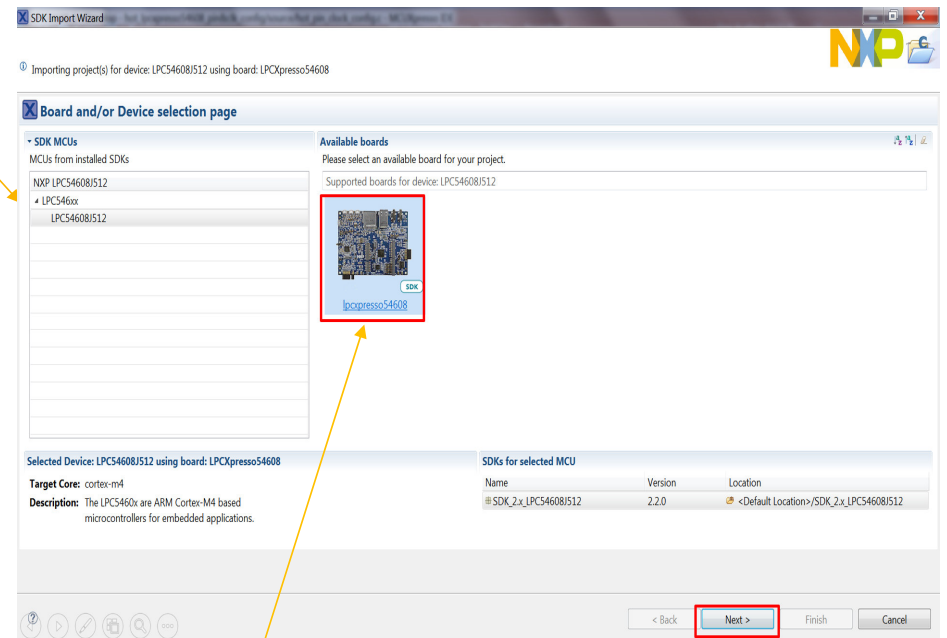
Import an SDK Example into the workspace

1. Click “Import SDK examples...” from Quickstart panel

Processors from installed SDKs



Opens selection wizard

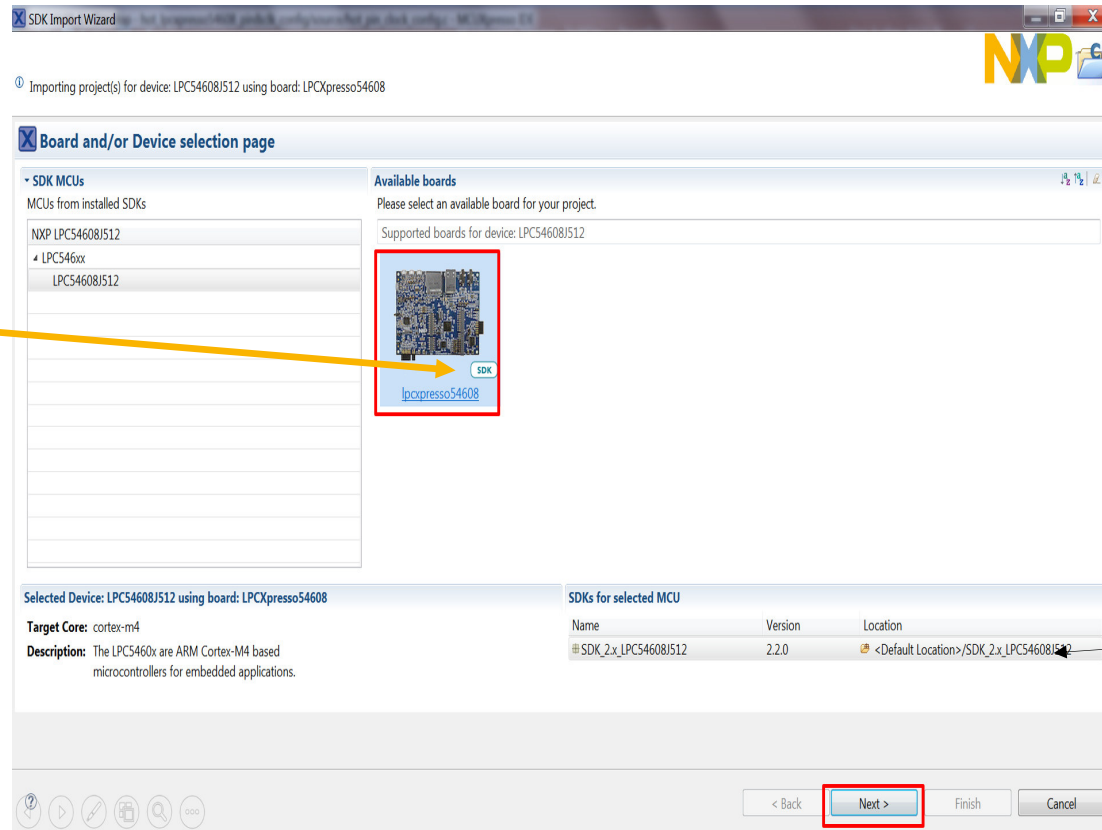


Boards from installed SDKs and preinstalled LPC boards

- SDK examples are board specific

Import an SDK Example into the workspace

2. Click on board image to import an SDK example



Installed SDK for selected board

3. Select Next to continue

SDK Example Import Wizard

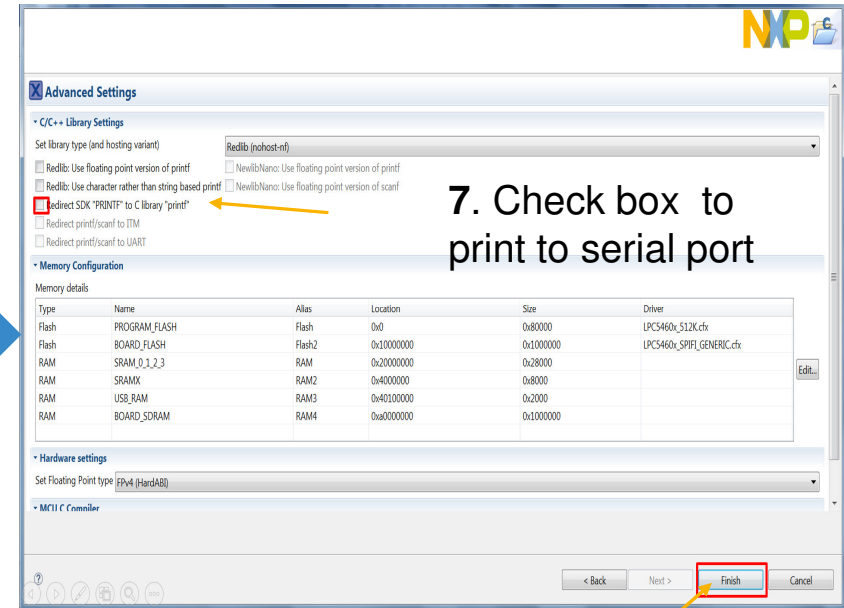
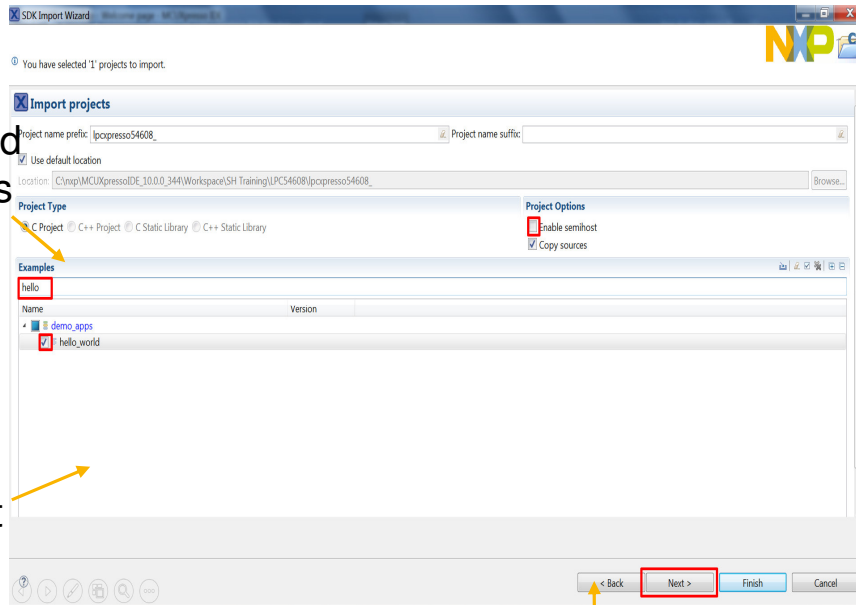
4. Expand examples

5. Select project

6. Click Next

7. Check box to print to serial port

8. Click Finish



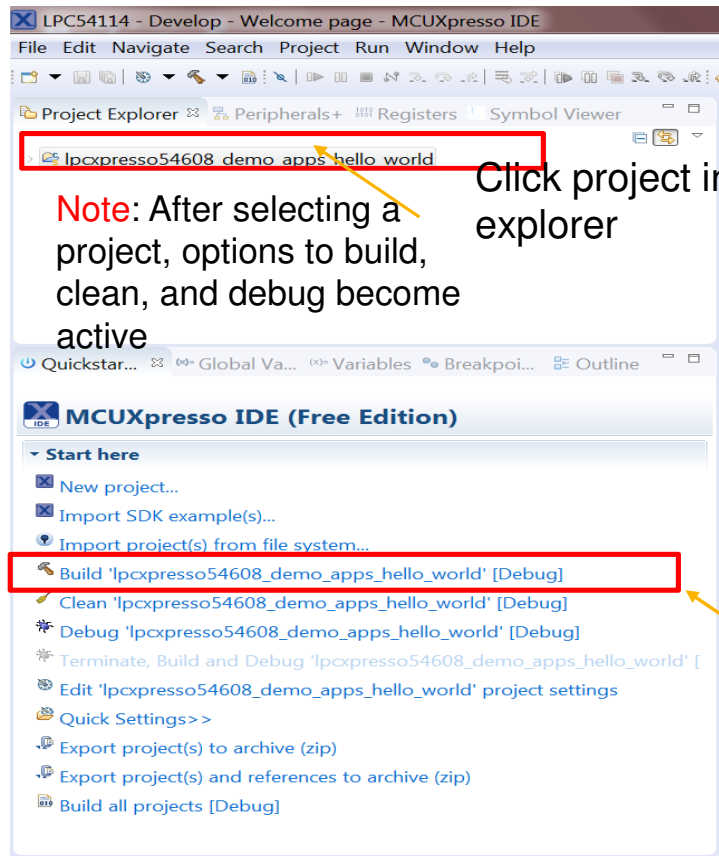
Copy Sources

- If copy sources is selected, files needed for example project are copied from the installed SDK into the project folder located in your workspace
- If the SDK was zipped this option would be selected automatically and greyed out
- If Copy Sources is not selected, SDK source files used in the project are linked directly from the installed SDK
- **NOTE:** Linking sources will modify the installed SDK

Sharing Projects

- If a project is built using part support from an SDK and is then exported – for example to share the project with a colleague who also uses MCUXpresso IDE, then the colleague must also install an SDK providing part support for the project's MCU.
- **Note:** Because device support is included in the SDK, it is recommended that any required SDKs are installed before a project requiring SDK part support is imported. However, if this is not done beforehand, simply select the imported project in the project explorer and right click and select: *C/C++ Build -> MCU settings* ensure the correct MCU is selected and click **Refresh MCU Cache**.

Building an Example



Click project in explorer

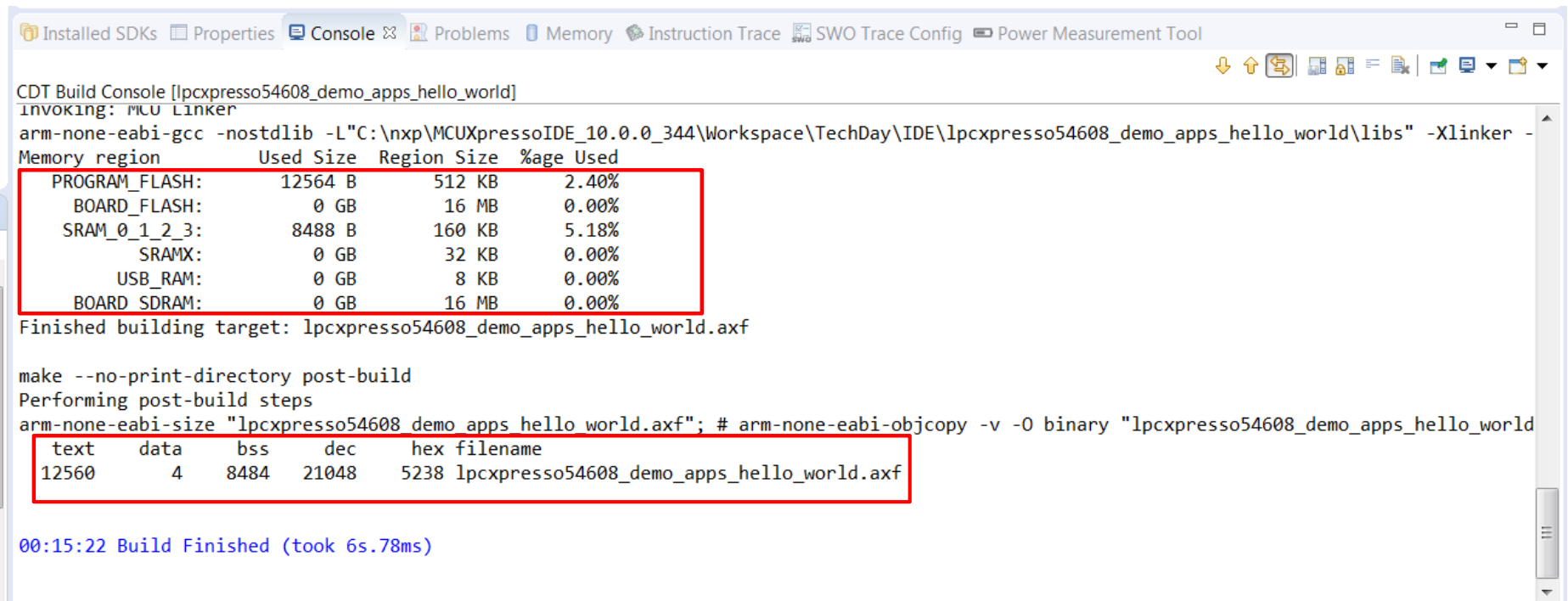
View Build Status in Console



Click Build



Memory Usage in Build Console



```
CDT Build Console [lpcpresso54608_demo_apps_hello_world]
invoking: MCU Linker
arm-none-eabi-gcc -nostdlib -L"C:\nxp\MCUXpressoIDE_10.0.0_344\Workspace\TechDay\IDE\lpcpresso54608_demo_apps_hello_world\libs" -Xlinker -
Memory region      Used Size  Region Size  %age Used
PROGRAM_FLASH:    12564 B    512 KB      2.40%
BOARD_FLASH:      0 GB      16 MB       0.00%
SRAM_0_1_2_3:     8488 B    160 KB      5.18%
SRAMX:            0 GB      32 KB       0.00%
USB_RAM:          0 GB      8 KB        0.00%
BOARD_SDRAM:      0 GB      16 MB       0.00%
Finished building target: lpcpresso54608_demo_apps_hello_world.axf

make --no-print-directory post-build
Performing post-build steps
arm-none-eabi-size "lpcpresso54608_demo_apps_hello_world.axf"; # arm-none-eabi-objcopy -v -O binary "lpcpresso54608_demo_apps_hello_world
text  data  bss  dec  hex filename
12560  4  8484  21048  5238 lpcpresso54608_demo_apps_hello_world.axf

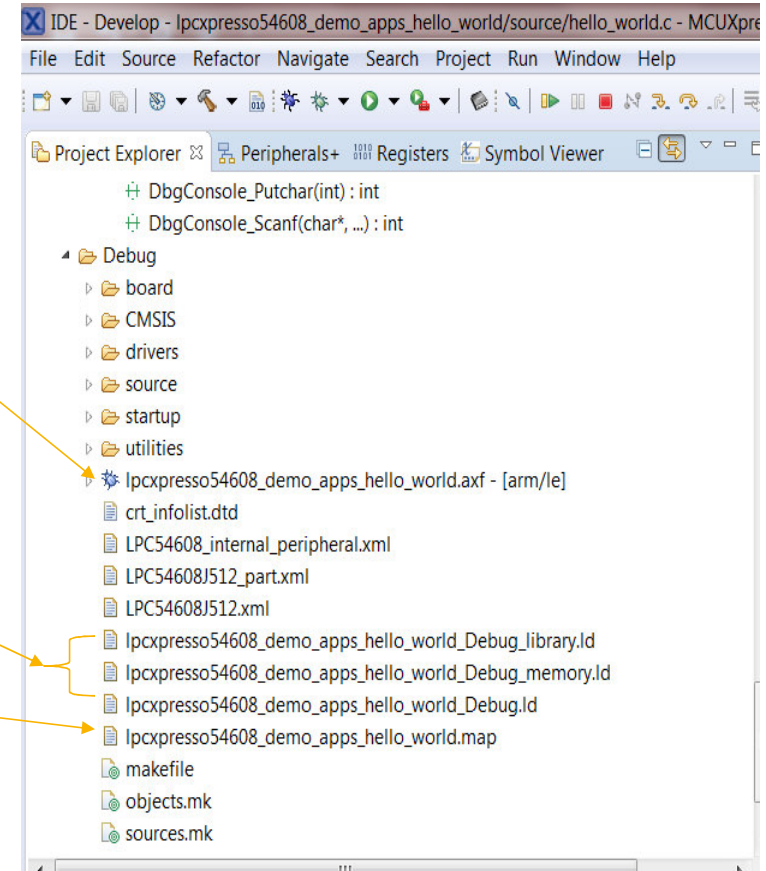
00:15:22 Build Finished (took 6s.78ms)
```

- **text** - shows the code and read-only data in your application (in decimal)
- **data** - shows the read-write data in your application (in decimal)
- **bss** - show the zero initialized ('bss' and 'common') data in your application (in decimal)
- **dec** - total of 'text' + 'data' + 'bss' (in decimal)
- **hex** - hexadecimal equivalent of 'dec'



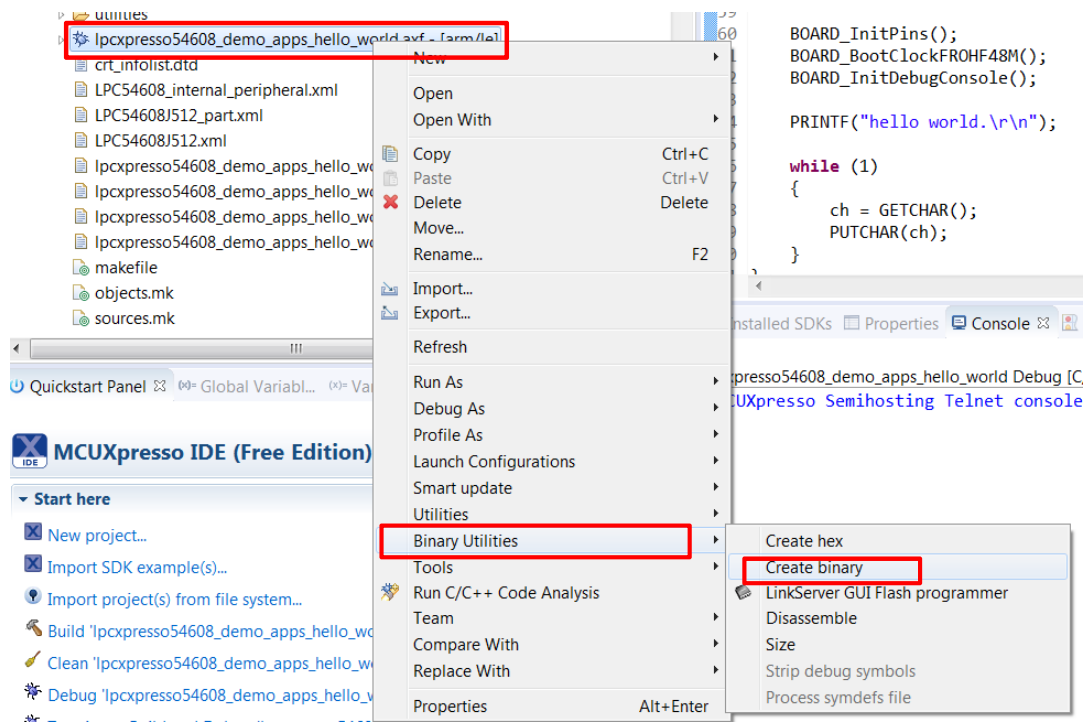
Build Results

- Link step will generate an AXF file
 - Standard ARM Executable Format – ELF/DWARF
 - MCUXpresso IDE can directly download to target
 - Post build step can be used to convert to other formats, such as binary or hex (using arm-none-eabi-objcopy)
- Linker scripts, controlling placement of code and data in memory, generated automatically by IDE
- MAP file generated by linker can be very useful too
 - Shows where code and data has been placed, and sizes of individual sections

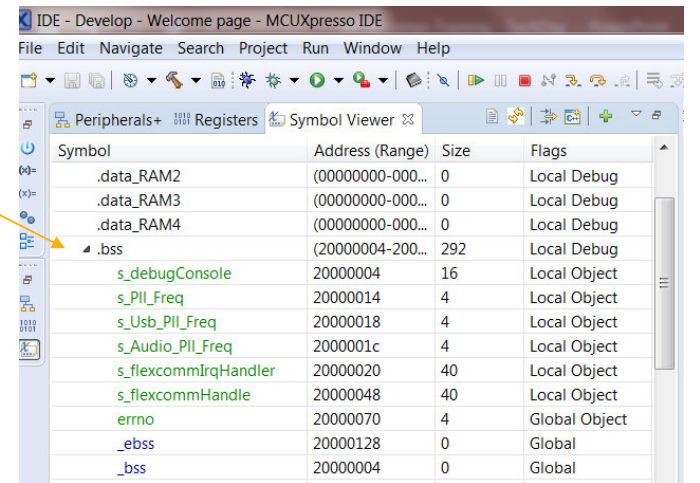
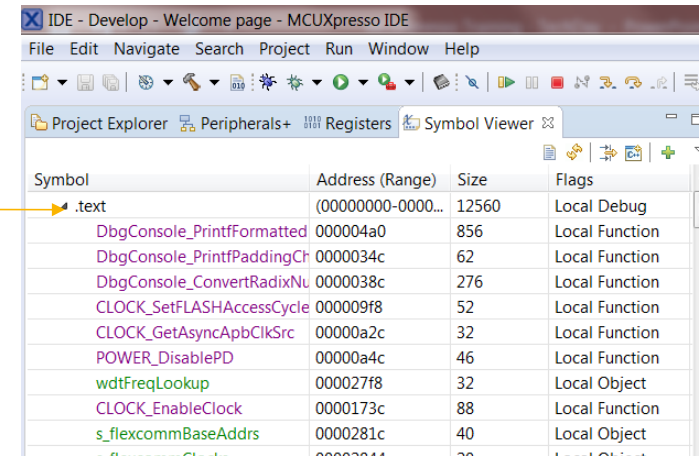
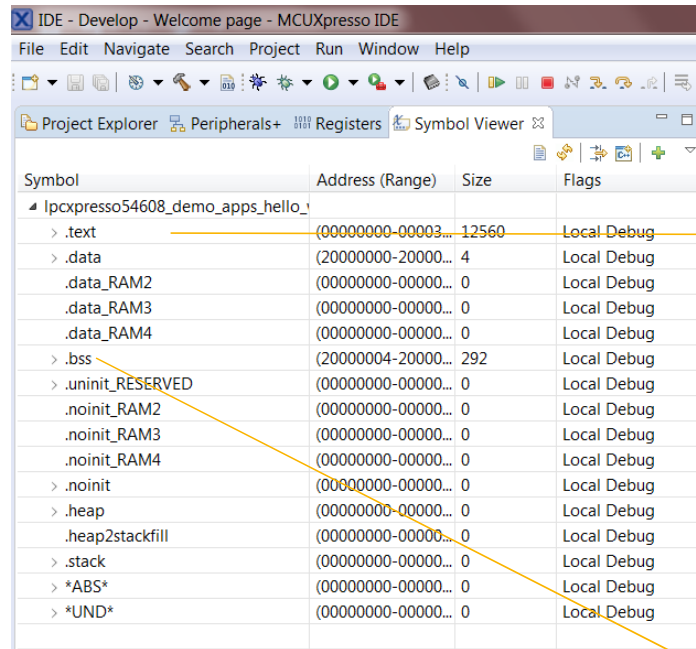
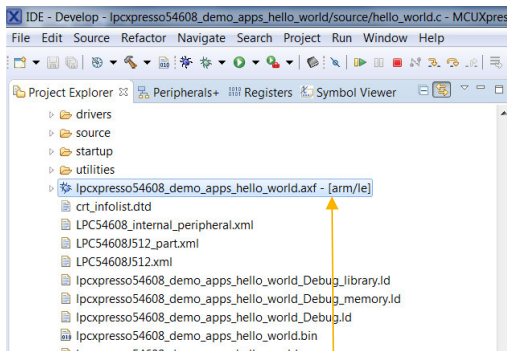


Create Binary

- Useful for drag-and-drop programming via OpenSDA
- Right Click on .axf file: Binary Utilities -> Create Binary



Symbol Viewer



- Right-click .axf file in explorer, then select Tools > View Symbols

- Symbol viewer will move to front of view
- Expand each section to examine its symbols

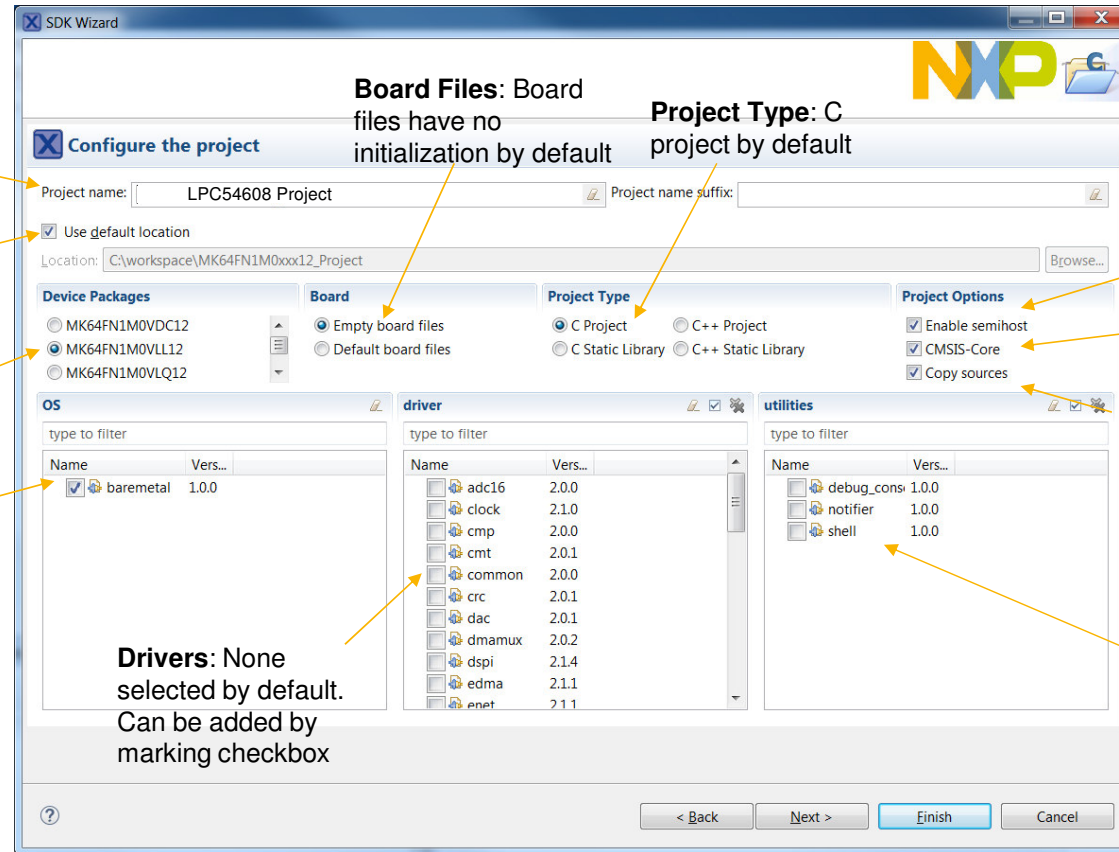
New Project for Board (Defaults)

Project Name:
Automatically named but can be modified.

Project Location:
Defaults to current workspace

Packages: Package of processor on board selected

OS: Baremetal selected by default



Semihosting enabled by default

CMSIS-Core files are added by default

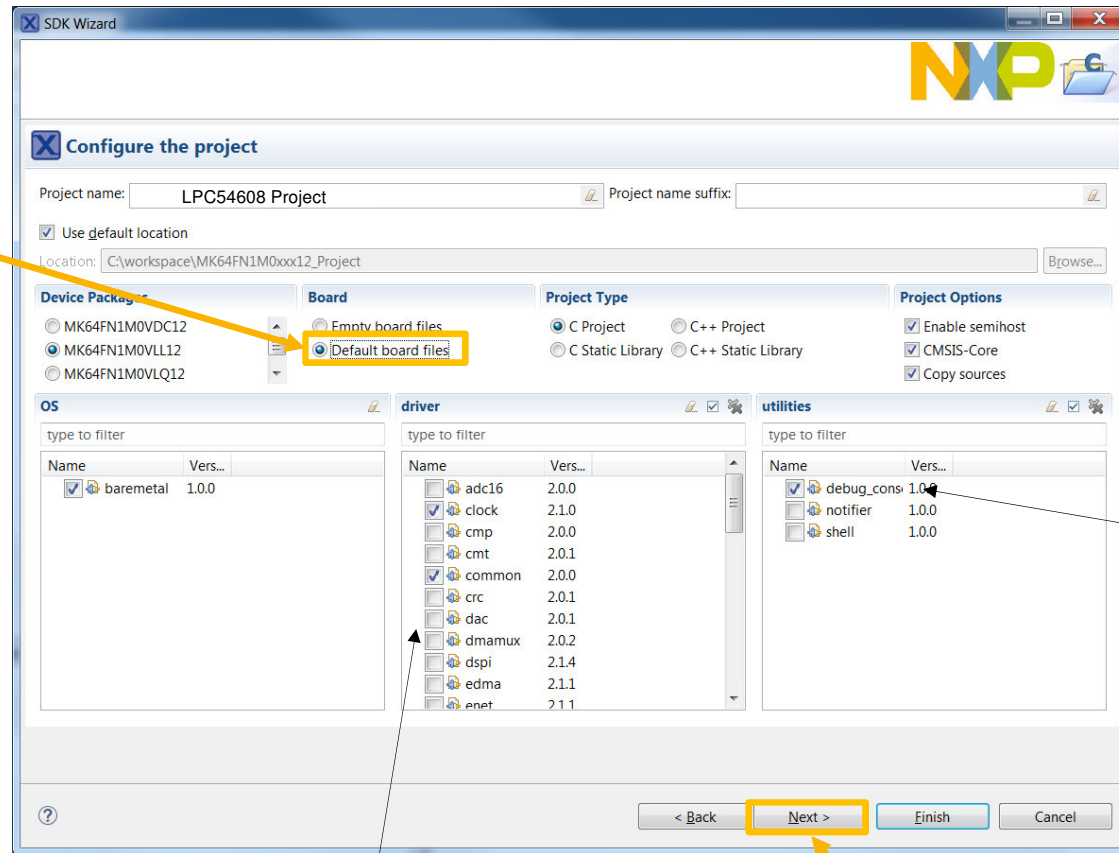
Source files are copied by default. Deselect for linked references (only available if SDK is unzipped)

Utilities: None selected by default. Can be added by marking checkbox

New Project for Board

4. Select Default Board files

Adds initialization code in board files for pins, clocks, and debug console



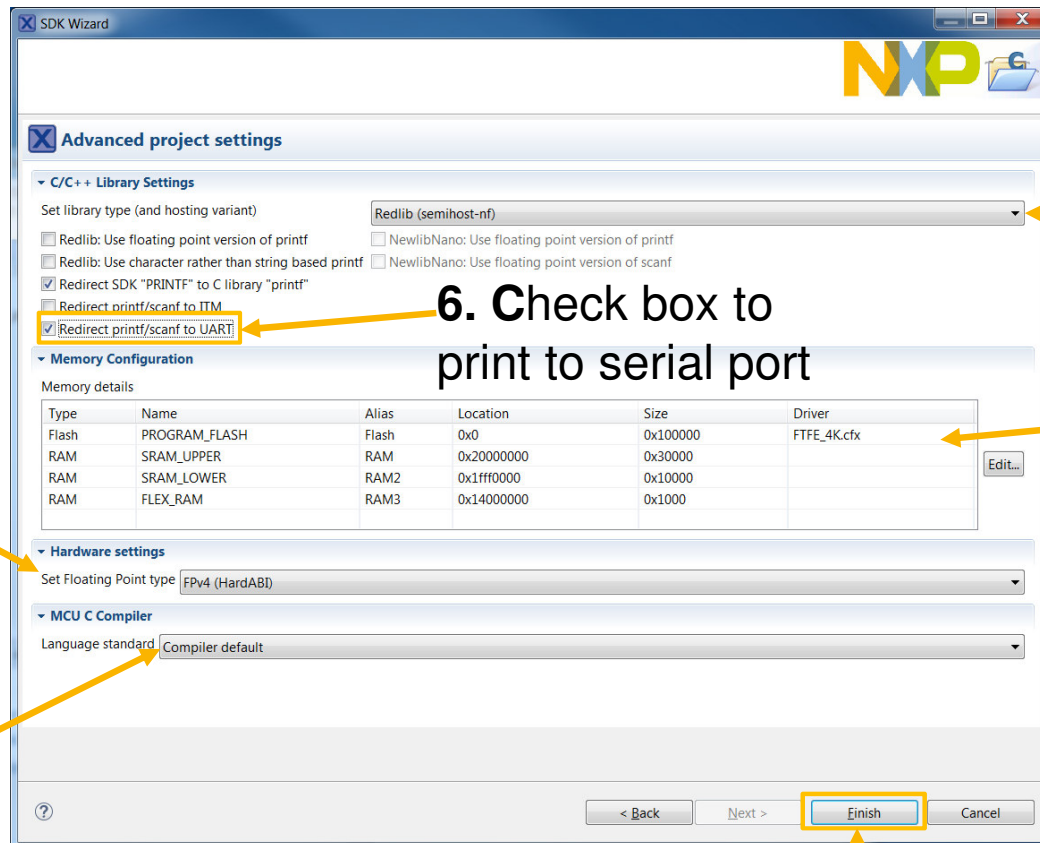
Adds debug_console support for board

Adds drivers to support initialization

5. Select Next to continue



New Project Advanced Settings



Library Selection

6. Check box to print to serial port

Memory Configuration

Floating Point Setup

Compiler selection

7. Click Finish



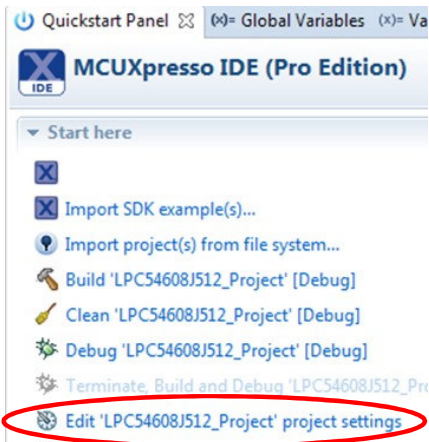
Changing Project Settings

Open the Properties for the "myproj" project via the Quickstart Panel

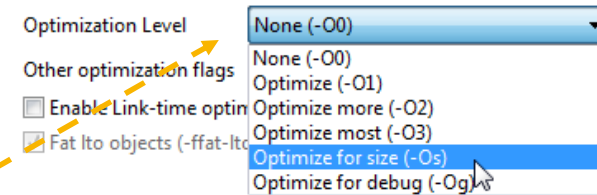
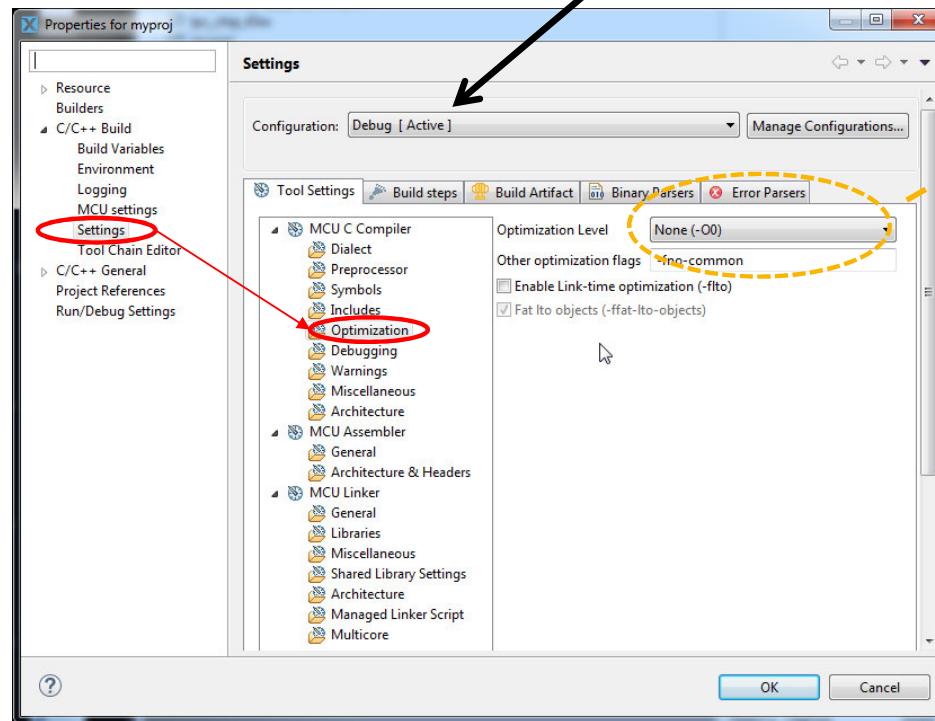
Switch to Compiler Optimization settings

Settings are for specified Build Configuration

Change optimization level, click OK, then trigger a build



Or use "Properties" entry on Project Explorer right-click menu or press Alt-Menu (Windows)



Default Build at -O0

```
Building target: LPC54608J512_Project.axf
Invoking: MCU Linker
arm-none-eabi-gcc -nostdlib -L"C:\Users\nxp73360\Documents"
Memory region      Used Size  Region Size  %age Used
PROGRAM_FLASH:    15512 B    512 KB      2.96%
BOARD_FLASH:       0 GB      16 MB       0.00%
SRAM_0_1_2_3:     8496 B    160 KB      5.19%
SRAMX:             0 GB      32 KB       0.00%
USB_RAM:          0 GB      8 KB        0.00%
BOARD_SDRAM:      0 GB     16 MB       0.00%
Finished building target: LPC54608J512_Project.axf
```

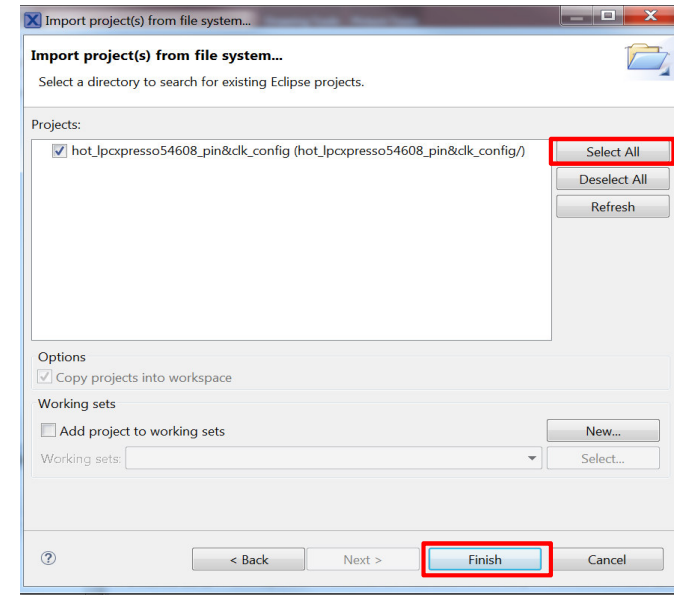
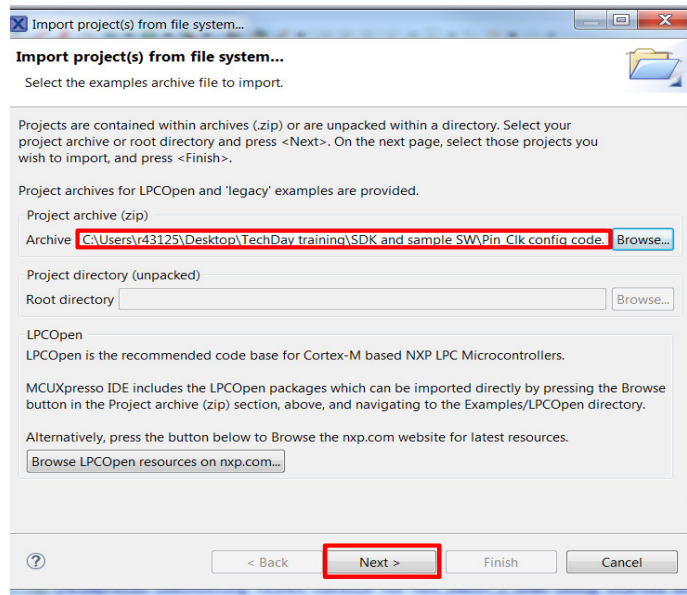
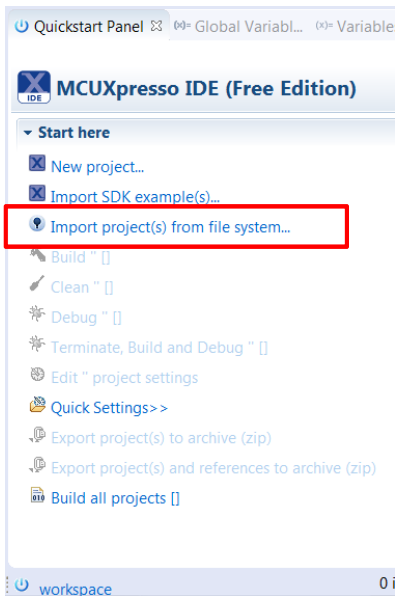
Project changed to -Os

```
arm-none-eabi-gcc -nostdlib -L"C:\Users\nxp73360\Documents"
Memory region      Used Size  Region Size  %age Used
PROGRAM_FLASH:    12756 B    512 KB      2.43%
BOARD_FLASH:       0 GB      16 MB       0.00%
SRAM_0_1_2_3:     8496 B    160 KB      5.19%
SRAMX:             0 GB      32 KB       0.00%
USB_RAM:          0 GB      8 KB        0.00%
BOARD_SDRAM:      0 GB     16 MB       0.00%
Finished building target: LPC54608J512_Project.axf
```

Note : We have only changed the application, not library projects

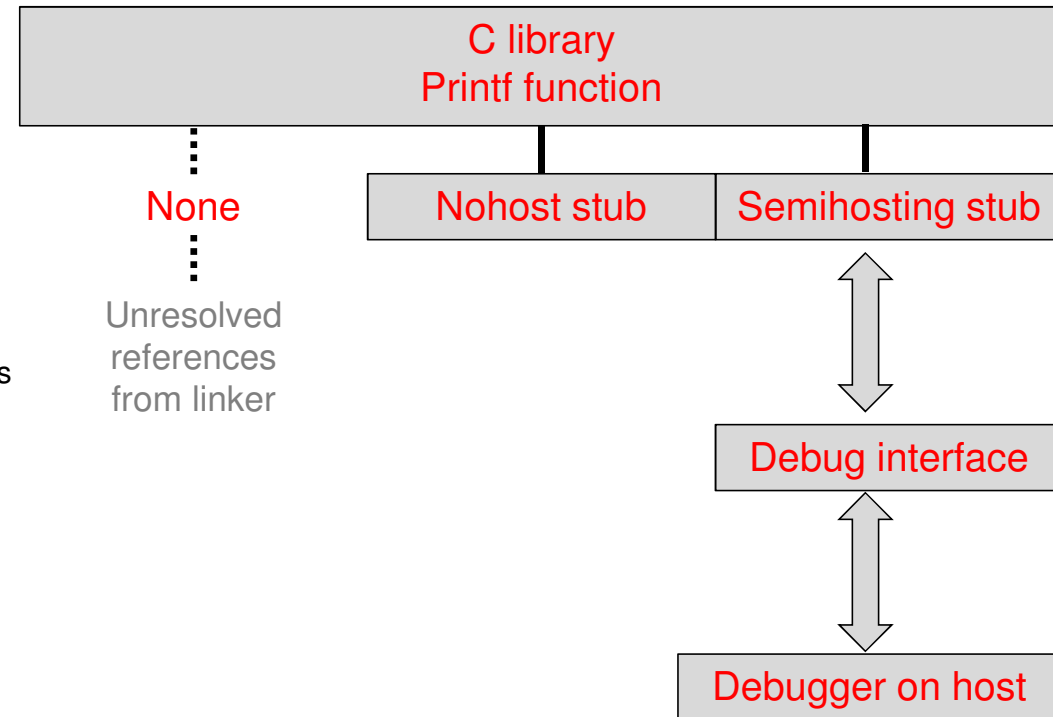


Import Project from File System



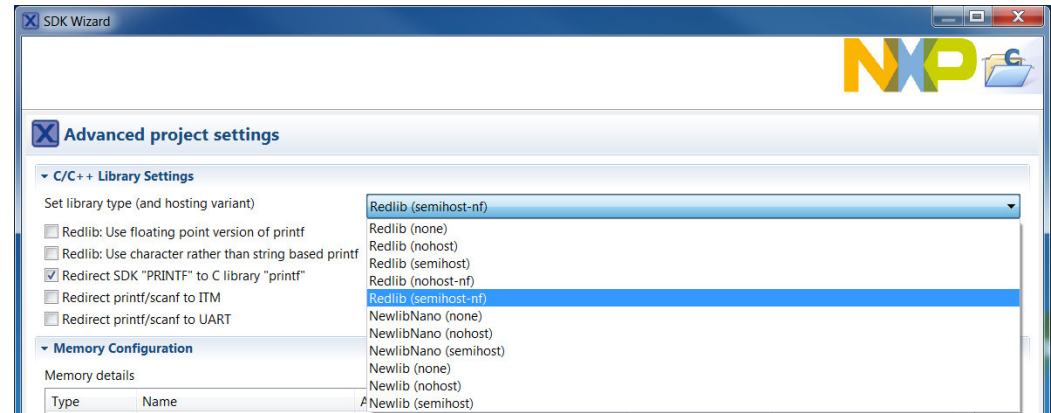
Library Variants

- Libraries are provided in number of variants, with different underlying “stub” providing support functions:
 - None
 - Smallest footprint. Excludes low-level file I/O
 - For Newlib, excludes memory handling functions
 - Nohost and Nohost-nf
 - Provides memory handling functions and some file I/O.
 - However, it assumes no host, and so file I/O will do nothing
 - Semihost-nf (no files)
 - Replib only
 - Similar to Semihost but only supports 3 standard built in streams (stdin, stdout, stderr)
 - Reduces memory overhead, but application cannot open files
 - Semihost
 - Full functionality
 - I/O resources are on the host side
- More C library information at:
 - <http://community.nxp.com> (MCUXpresso IDE FAQs)



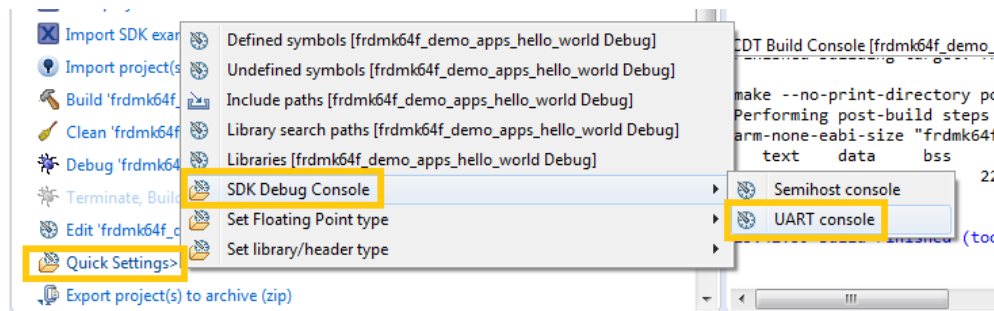
C/C++ Library Selection

- C projects
 - Default to Redlib
 - C90 library, with some C99 extensions
 - Optimized for code size
 - Select use of integer printf in wizard
- C++
 - Default to Newlib
 - Provides C++ support, plus full C99
 - Can switch C projects to use Newlib if required
- MCUXpresso also supports “Newlib-Nano”
 - Code size optimized version of Newlib
 - Can switch C or C++ projects to use this
 - Integer only printf by default – enable floating point in Linker options

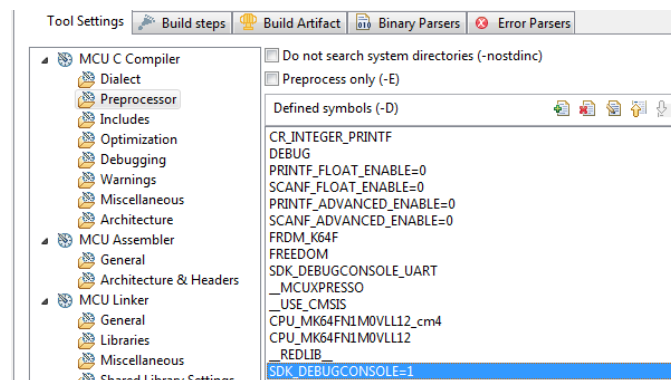


Change to UART Console

- If user forgets to check the box to redirect printf/scanf to UART, can change in project via the Quick Settings:



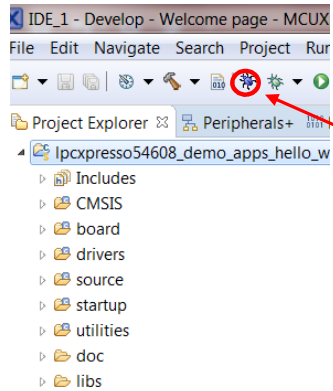
- Verify setting in Project Settings->Preprocessor that `SDK_DEBUGCONSOLE=1`



MCUXPRESSO IDE DEBUG



Start a Debug Session

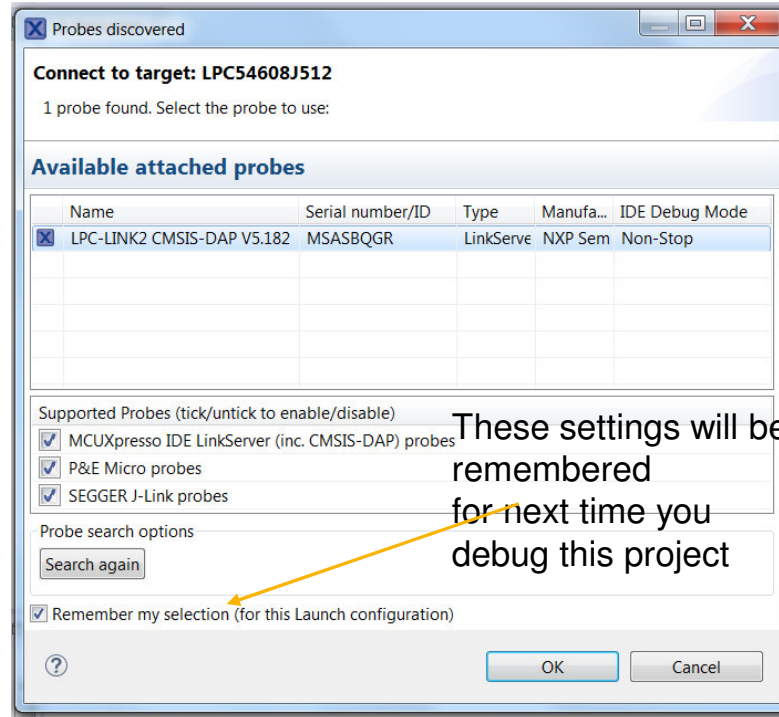


Note: Do not use this icon, Use the Quickstart Panel instead



Open Quickstart Panel

Click Debug



These settings will be remembered for next time you debug this project

Note: By default, selecting "Debug" will trigger a build before the debug session is launched, so it is not required to run a "build" first

Debug Perspective

Registers and Peripherals View

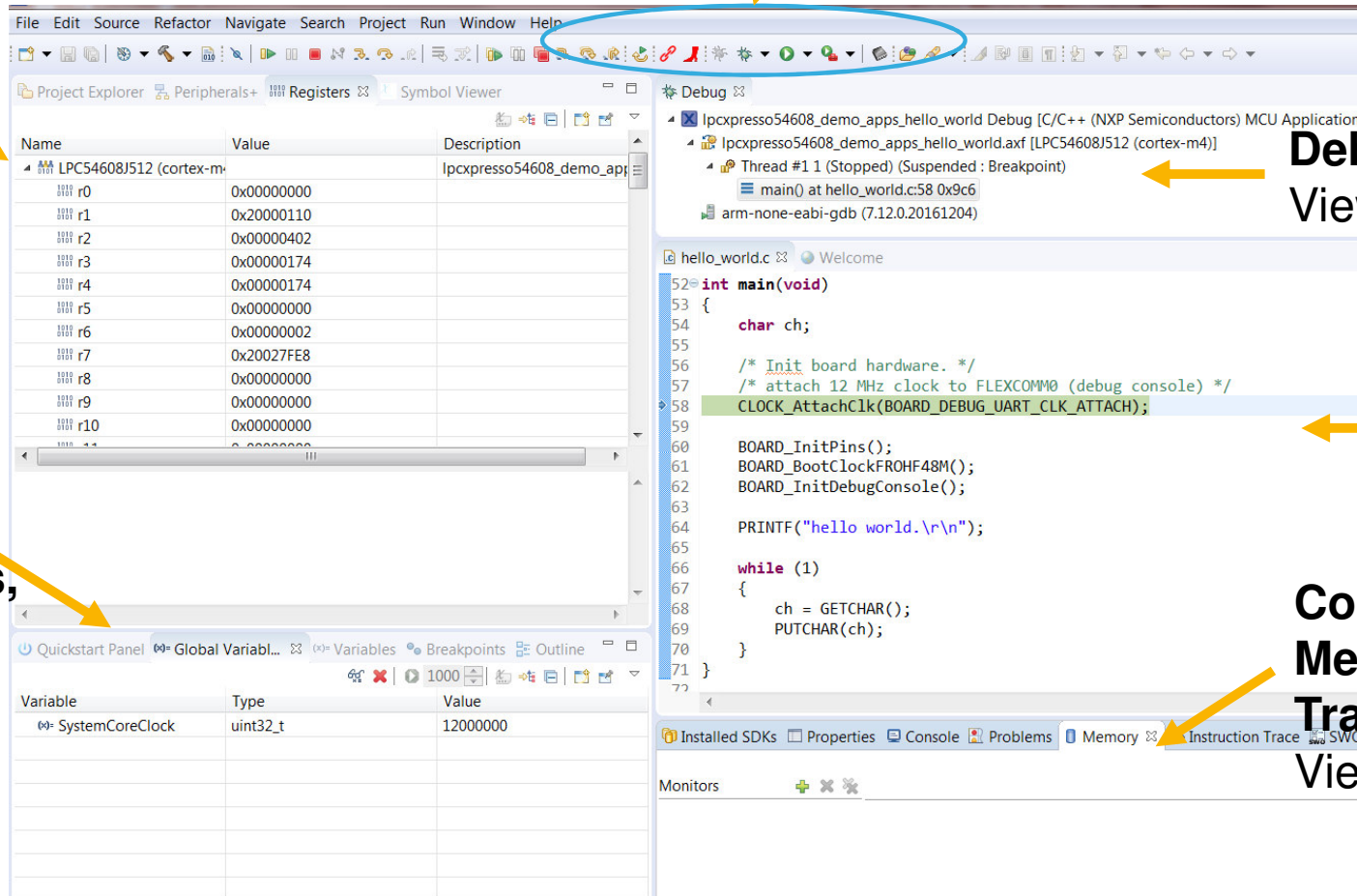
Variables, Expressions, and Breakpoints View

Run Controls

Debug View

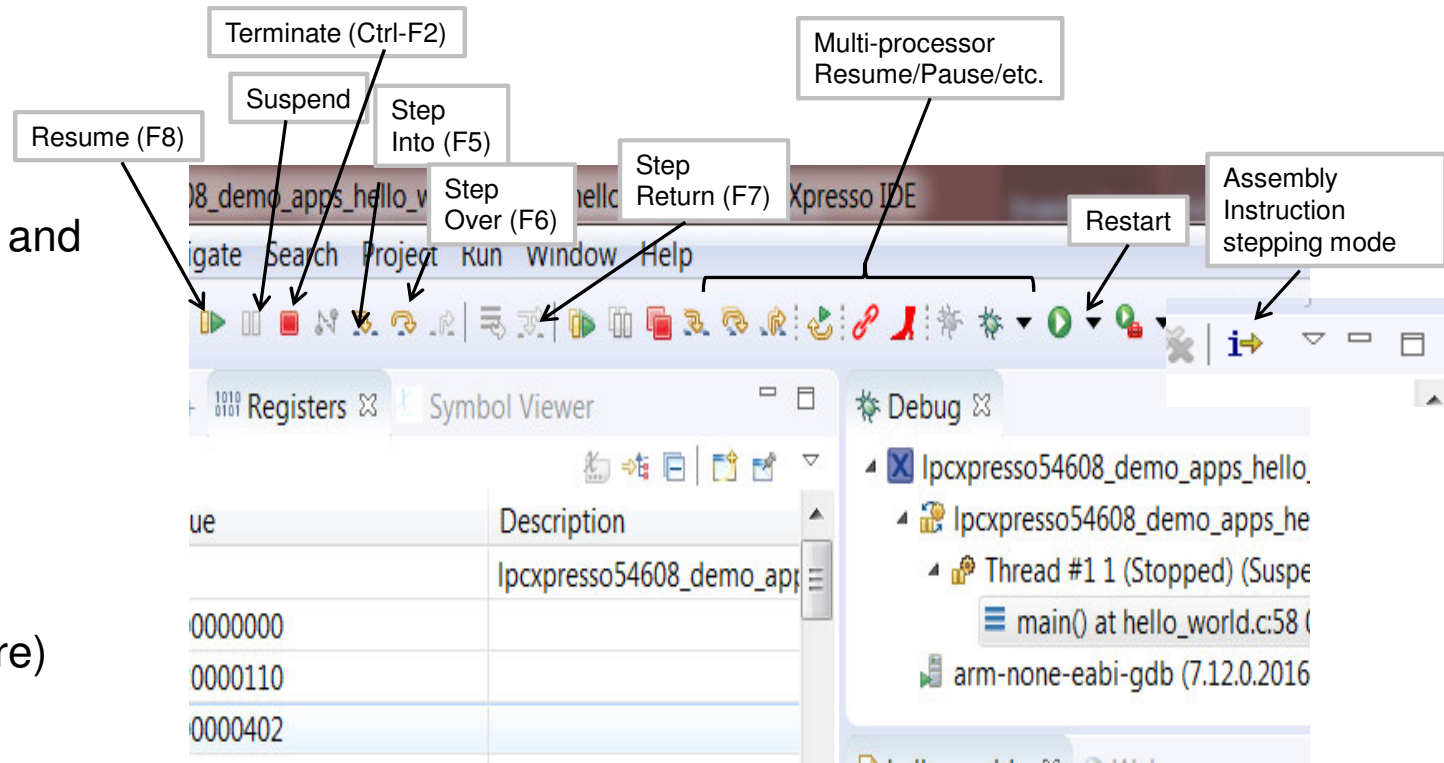
Editor View

Console, Memory, and Trace Views



Stopped At Main()

- Image downloaded to flash and execution started
 - Default breakpoint set on function main()
- Debug View displayed automatically
 - Shows / controls current scope and target (multicore)
 - Run controls are on main toolbar
- **But before you begin to run the code ...**



Debug: Step Over

```
Welcome | hello_world.c | pin_mux.c
48 *****
49 /*!
50 * @brief Main function
51 */
52 int main(void)
53 {
54     char ch;
55
56     /* Init board hardware. */
57     BOARD_InitPins();
58     BOARD_BootClockRUN();
59     BOARD_InitDebugConsole();
60
61     PRINTF("hello world.\r\n");
62
63     while (1)
64     {
65         ch = GETCHAR();
66         PUTCHAR(ch);
67     }
68 }
```

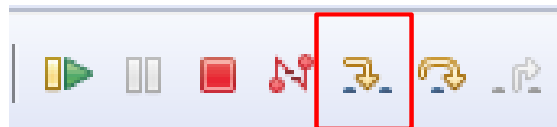
```
Welcome | hello_world.c | pin_mux.c
49 /*!
50 * @brief Main function
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52 int main(void)
53 {
54     char ch;
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56     /* Init board hardware. */
57     BOARD_InitPins();
58     BOARD_BootClockRUN();
59     BOARD_InitDebugConsole();
60
61     PRINTF("hello world.\r\n");
62
63     while (1)
64     {
65         ch = GETCHAR();
66         PUTCHAR(ch);
67     }
68 }
```



Debug: Step Into Function

```
Welcome | hello_world.c | pin_mux.c
48
49 /*!
50 * @brief Main function
51 */
52 int main(void)
53 {
54     char ch;
55
56     /* Init board hardware. */
57     BOARD_InitPins();
58     BOARD_BootClockRUN();
59     BOARD_InitDebugConsole();
60
61     PRINTF("hello world.\r\n");
62
63     while (1)
64     {
65         ch = GETCHAR();
66         PUTCHAR(ch);
67     }
68 }
```

```
187 /******
188 * Code for BOARD_BootClockRUN configuration
189 *****/
190 void BOARD_BootClockRUN(void)
191 {
192     /* Set the system clock dividers in SIM to safe value. */
193     CLOCK_SetSimSafeDivs();
194     /* Initializes OSC0 according to board configuration. */
195     CLOCK_InitOsc0(&oscConfig_BOARD_BootClockRUN);
196     CLOCK_SetXtal0Freq(oscConfig_BOARD_BootClockRUN.freq);
197     /* Configure the Internal Reference clock (MCGIRCLK). */
198     CLOCK_SetInternalRefClkConfig(mcgConfig_BOARD_BootClockRUN.irclockEnableMode,
199                                   mcgConfig_BOARD_BootClockRUN.ircs,
200                                   mcgConfig_BOARD_BootClockRUN.fcrdiv);
201     /* Configure FLL external reference divider (FRDIV). */
202     CLOCK_CONFIG_SetFllExtRefDiv(mcgConfig_BOARD_BootClockRUN.frddiv);
203     /* Set MCG to PEE mode. */
204     CLOCK_BootToPeeMode(mcgConfig_BOARD_BootClockRUN.oscsele,
205                        kMCG_PllClkSelPLL0,
206                        &mcgConfig_BOARD_BootClockRUN.pll0Config);
207     /* Set the clock configuration in SIM module. */
208     CLOCK_SetSimConfig(&simConfig_BOARD_BootClockRUN);
209     /* Set SystemCoreClock variable. */
210     SystemCoreClock = BOARD_BOOTCLOCKRUN_CORE_CLOCK;
211 }
```



Debug: Step Return

```
187= /*****
188 * Code for BOARD_BootClockRUN configuration
189 *****/
190= void BOARD_BootClockRUN(void)
191 {
192     /* Set the system clock dividers in SIM to safe value. */
193     CLOCK_SetSimSafeDivs();
194     /* Initializes OSC0 according to board configuration. */
195     CLOCK_InitOsc0(&oscConfig_BOARD_BootClockRUN);
196     CLOCK_SetXtal0Freq(oscConfig_BOARD_BootClockRUN.freq);
197     /* Configure the Internal Reference clock (MCGIRCLK). */
198     CLOCK_SetInternalRefClkConfig(mcgConfig_BOARD_BootClockRUN.irclkEnableMode,
199                                  mcgConfig_BOARD_BootClockRUN.ircs,
200                                  mcgConfig_BOARD_BootClockRUN.fcrdiv);
201     /* Configure FLL external reference divider (FRDIV). */
202     CLOCK_CONFIG_SetFllExtRefDiv(mcgConfig_BOARD_BootClockRUN.frddiv);
203     /* Set MCG to PEE mode. */
204     CLOCK_BootToPeeMode(mcgConfig_BOARD_BootClockRUN.oscsele,
205                        kMCG_PllClkSelPLL0,
206                        &mcgConfig_BOARD_BootClockRUN.pll0Config);
207     /* Set the clock configuration in SIM module. */
208     CLOCK_SetSimConfig(&simConfig_BOARD_BootClockRUN);
209     /* Set SystemCoreClock variable. */
210     SystemCoreClock = BOARD_BOOTCLOCKRUN_CORE_CLOCK;
211 }
```

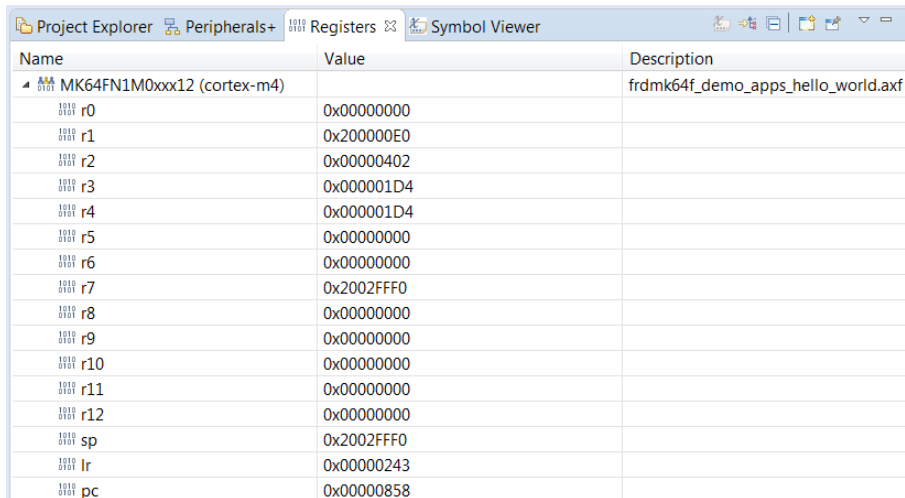


```
Welcome | hello_world.c | pin_mux.c
47 * Code
48 *****/
49 /*!
50 * @brief Main function
51 */
52= int main(void)
53 {
54     char ch;
55
56     /* Init board hardware. */
57     BOARD_InitPins();
58     BOARD_BootClockRUN();
59     BOARD_InitDebugConsole();
60
61     PRINTF("hello world.\r\n");
62
63     while (1)
64     {
65         ch = GETCHAR();
66         PUTCHAR(ch);
67     }
68 }
```

Registers, Local Variables, and Memory Views

Registers View:

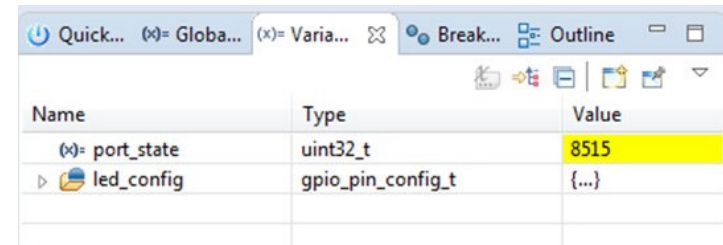
- CPU registers are displayed. Will highlight in yellow when contents update



Name	Value	Description
MK64FN1M0xxx12 (cortex-m4)		frdmk64f_demo_apps_hello_world.axf
r0	0x00000000	
r1	0x200000E0	
r2	0x00000402	
r3	0x000001D4	
r4	0x000001D4	
r5	0x00000000	
r6	0x00000000	
r7	0x2002FFFO	
r8	0x00000000	
r9	0x00000000	
r10	0x00000000	
r11	0x00000000	
r12	0x00000000	
sp	0x2002FFFO	
lr	0x00000243	
pc	0x00000858	

Variables View:

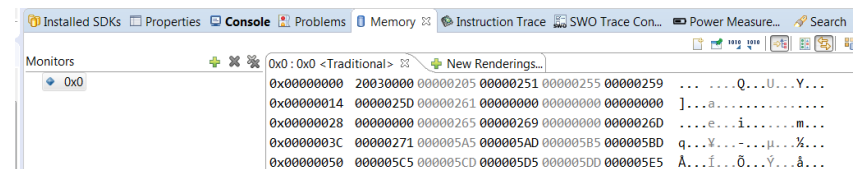
- In-scope local variables displayed
- Locals displayed will change as move up and down the call stack



Name	Type	Value
(*)= port_state	uint32_t	8515
led_config	gpio_pin_config_t	{...}

Memory View:

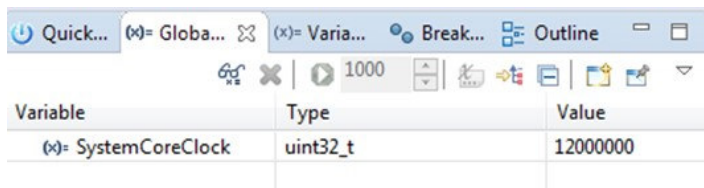
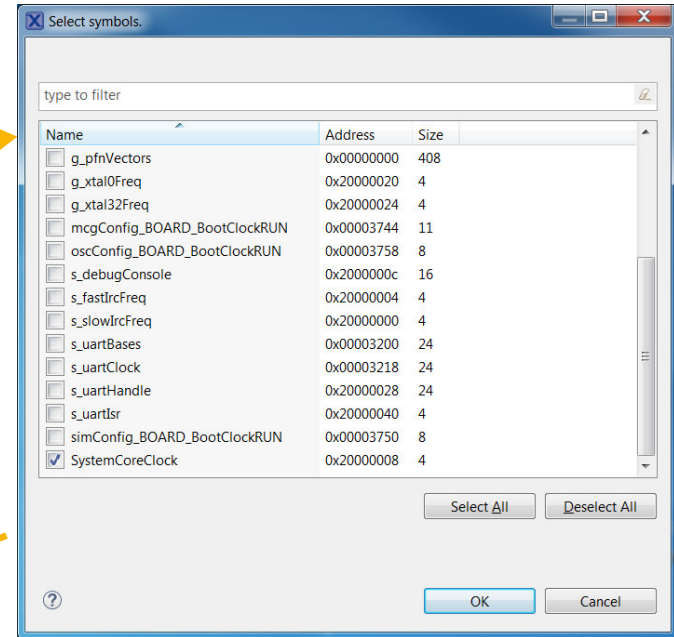
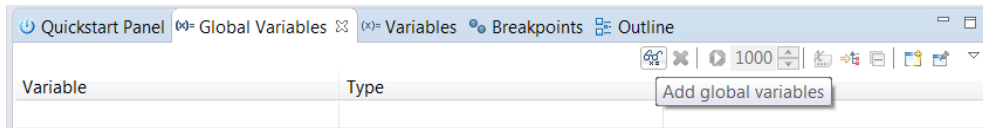
- Add address to display view of memory contents starting at that location



Address	Value
0x00000000	20030000 00000205 00000251 00000255 00000259Q...U...Y...
0x00000014	0000025D 00000261 00000000 00000000 00000000]...a.....
0x00000028	00000000 00000265 00000269 00000000 0000026D ...e...i.....m...
0x0000003C	00000271 000005A5 000005AD 000005B5 000005BD q...V...μ...%
0x00000050	000005C5 000005CD 000005D5 000005DD 000005E5 A...f...ö...ÿ...â...

Add a Global Variable

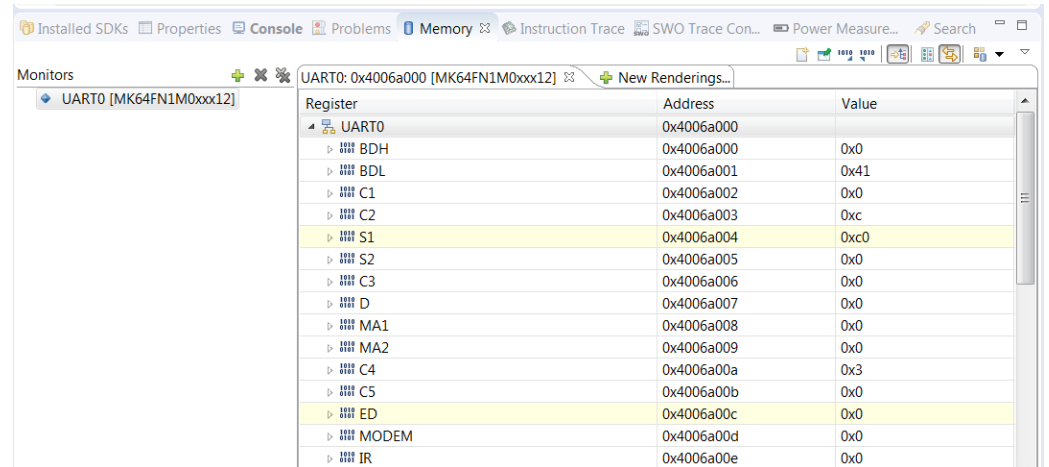
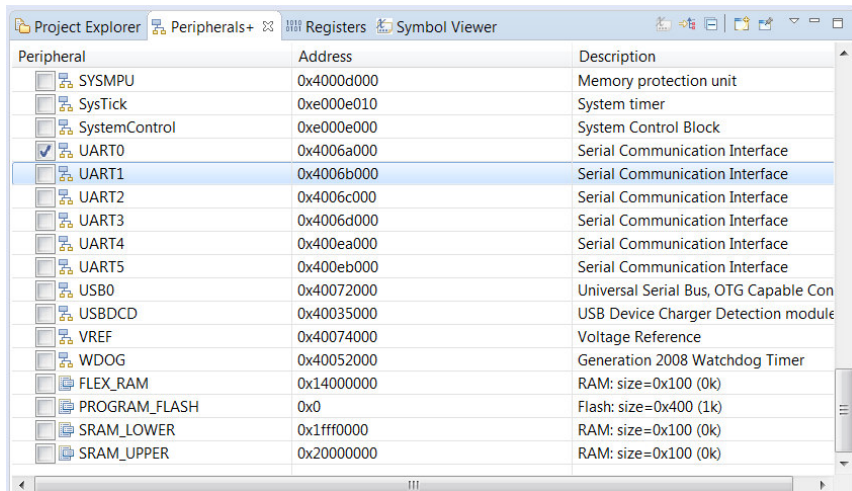
1) Switch to the Global Variables View and click on the “Add global variables” button



3) SystemCoreClock global is now visible in the Expressions View

2) Scroll down and select “SystemCoreClock”, which will hold the main CPU clock speed

Peripherals View



- In Peripherals View, click checkbox next to peripheral to select it

- This will open the peripheral in the Memory View
- Expand the peripheral to see details of registers

Sharing Projects

- If a project is built using part support from an SDK and is then exported – for example to share the project with a colleague who also uses MCUXpresso IDE, then the colleague must also install an SDK providing part support for the project's MCU.
- **Note:** it is recommended that any required SDKs are installed before a project requiring SDK part support is imported. However, if this is not done, simply select the imported project in the project explorer and right click and select: *C/C++ Build - > MCU settings* ensure the correct MCU is selected and click **Refresh MCU Cache**.

LAB 2



Lab 2 : To import SDK example and run in MCUXpresso

- **Pre-requisites**

- Boards
 - OM13092(LPCXpresso54608)
- Software
 - SDK_2.2_LPC54608J512 : <https://mcuxpresso.nxp.com/en/welcome>
 - MCUXpresso IDE: <http://nxp.com/mcuxpresso/ide>
 - Terminal Software (like TeraTerm or PuTTY)
 - mbed Serial Driver: <https://developer.mbed.org/handbook/Windows-serial-configuration>
 - Need to install with the board plugged in. Only need to do once per computer.
- Follow Lab 2 instruction

AGENDA

- **MCUXpresso Software And Tools Overview**
- **MCUXpresso SDK**
 - Web Builder
 - File Structure
- **MCUXpresso IDE**
 - Importing/Building
 - Debugging
- **MCUXpresso Config Tool**
 - Project Cloner
 - Pins Tool
 - Clocks Tool
- **LPC54608 LCD Lab, Key API and EmWin Demo**

MCUXPRESSO CONFIG TOOLS



Configurations

- What is a configuration?
 - A group of settings used across the MCUXpresso configuration tools (Pins, Clocks, and Project Generator)
- SDK provides configurations to start development with specific to the board or processor.
- Users can import a configuration, modify clocks and pin settings, and export the configuration.
- If no SDK is selected, default configurations for boards and processors are available.
- Configurations can be saved and shared as a .mex file

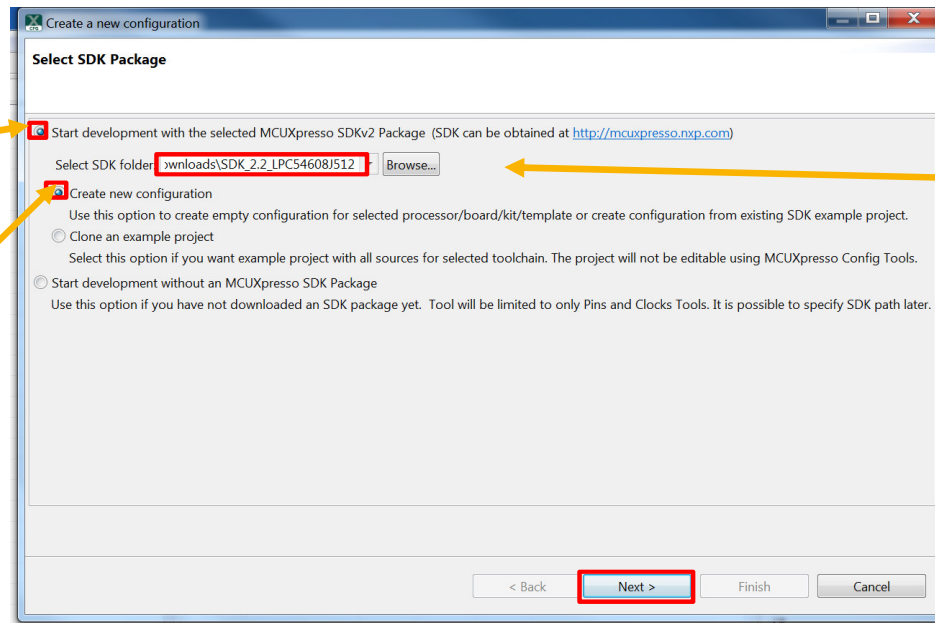
MCUXPRESSO CONFIG TOOLS PROJECT CLONE



Configuration Tool Wizard

Select an SDK to build configurations

Start a configuration



Point to SDK installation folder (unzipped)

Once finished, select Continue

Creating a New Configuration using SDK

- New Board Configuration
 - Board-specific pin initialization (e.g. UART, LEDs, etc.)
 - Board-specific clock initialization (e.g. External OSC)
- Example Based Board Configuration
 - Pin initialization specific to board and example (e.g. I2C, SPI, etc.)
 - Clock initialization specific to board and examples
- Processor Based Board Configuration
 - Empty pin initialization
 - Supports reset clock configuration

Create a New Configuration

The image shows three sequential screenshots of the 'Create a new configuration' wizard. The first screenshot shows the 'Select Processor/Board' step with 'LPC' entered in the search field. The second screenshot shows the 'LPCXpresso54608' board selected, with the 'Examples' folder expanded to show 'demo_apps' and 'driver_examples'. The third screenshot shows the 'hello_world' example selected, with the 'Name your configuration' field containing 'hello_world' and the 'Finish' button highlighted.

Kit-based (points to the 'Boards' section)

Board-based (points to the 'Examples' section)

Processor-based (points to the 'Processors' section)

New configuration based on example (points to the 'demo_apps' and 'driver_examples' folders)

Search for example (points to the search field in the third screenshot)

Name configuration (points to the 'Name your configuration' field in the third screenshot)

Finish (points to the 'Finish' button in the third screenshot)

MCUXPRESSO CONFIG TOOLS PINS TOOL



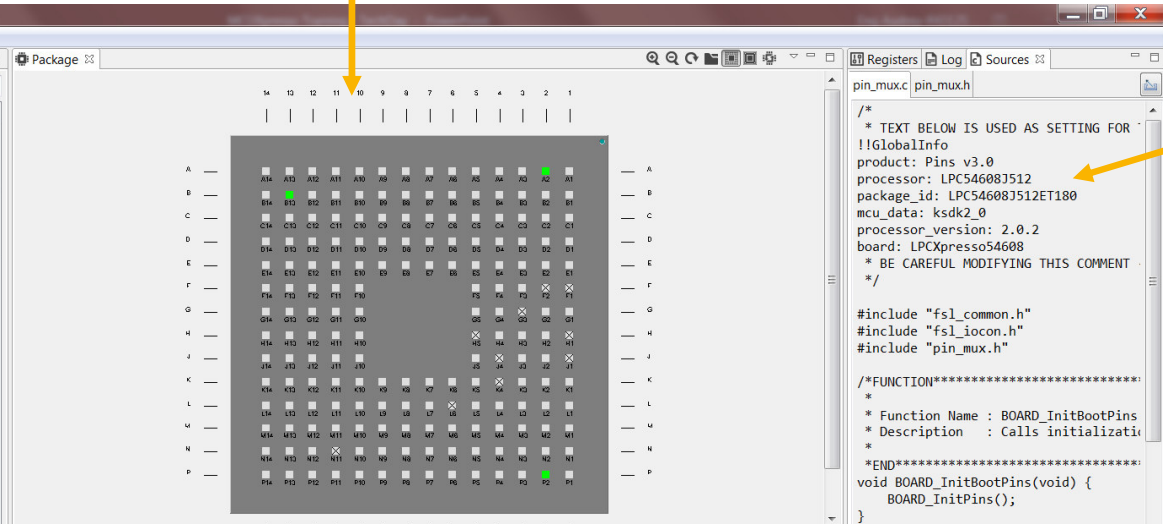
Pins Tool Views

Pins/
Peripherals
View

Pin

Pin	Pin name	Label	Identifier	GPIO	F
A1	PIO0_1/CAN...	U26[14]/J14[...	ISP_FC3_SSELO	PIO0_1	F
B1	PIO2_3/ENET...	U9[3]/P2_3-S...	SD_CLK	PIO2_3	F
C1	PIO2_5/ENET...	Q3[1]/P2_5-S...	SD_POW_EN	PIO2_5	F
D1	PIO1_18/FC8...			PIO1_18	F
E1	PIO3_16/FC8...			PIO3_16	F
F1	USB1_REXT				
G1	USB1_ID	J2[4]/USB1_I...	USB1_ID		
H1	USB1_AVDD1				
J1	USB1_AVSS1...				
K1	PIO3_17/FC8...			PIO3_17	F
L1	PIO1_19/FC8...	U28[E1]/RP4...	EMC_D8	PIO1_19	F
M1	PIO1_20/FC7...	U28[D2]/RP4...	EMC_D9	PIO1_20	F
N1	PIO1_7/FC0...	U28[H3]/P1...	EMC_A6	PIO1_7	F
P1	PIO2_10/ENE...	RP1[2]/U9[7]...	SD_CDn	PIO2_10	F
A2	FC0_TXD_SC...	U24[12]/P0...	ISP_FC0_TXD	PIO0_30	F
B2	PIO3_11/MC...	J11[8]/J12[7]...	MCLK	PIO3_11	F
C2	PIO3_23/FC2...	J11[10]/J9[3]...	FC2_SDAX	PIO3_23	F
D2	PIO3_15/FC8...	RP1[1]/U9[8]...	SD_WPh	PIO3_15	F
E2	PIO3_24/FC2...	J11[9]/J9[1]...	FC2_SCLX	PIO3_24	F
F2	USB1_AVSSC				
G2	USB1_VBUS	J2[1]/U2[4]/...	USB1_VBUS		
H2	USB1_DM	J2[2]/U2[3]/...	USB1_DM		
J2	PIO2_7/ENET...	RP1[4]/U9[5]...	SD_D1	PIO2_7	F
K2	PIO2_9/ENET...	RP1[7]/U9[1]...	SD_D3	PIO2_9	F
L2	PIO3_12/SCT...			PIO3_12	F
M2	PIO2_12/LCD...	U26[A13]/P2...	SPIF_RSTn	PIO2_12	F
N2	PIO3_20/FC9...			PIO3_20	F
P2	SWO	U16[12]/SW...	SWO_TRGT	PIO0_10	F
A3	PIO3_10/SCT...			PIO3_10	F
B3	VSSO				
C3	PIO2_2/ENET...	J9[6]/LED3/P...	LED3	PIO2_2	F
D3	PIO2_4/ENET...	RP1[6]/U9[2]...	SD_CMD	PIO2_4	F
E3	PIO3_14/SCT...	J13[5]/LED1...	LED1	PIO3_14	F
F3	PIO2_6/ENET...	RP1[5]/U9[4]...	SD_D0	PIO2_6	F
G3	USB1_AVDD0				
H3	USB1_DP	J2[3]/U2[2]...	USB1_DP		

Package view



Sources/
Registers/
Log
View

```
pin_mux.c pin_mux.h
/*
 * TEXT BELOW IS USED AS SETTING FOR
 * !!GlobalInfo
 * product: Pins v3.0
 * processor: LPC54608J512
 * package_id: LPC54608J512ET180
 * mcu_data: kSDK2_0
 * processor_version: 2.0.2
 * board: LPCXpresso54608
 * * BE CAREFUL MODIFYING THIS COMMENT
 * */

#include "fs1_common.h"
#include "fs1_iocon.h"
#include "pin_mux.h"

/*FUNCTION*****
 *
 * Function Name : BOARD_InitBootPins
 * Description : Calls initializati
 *
 *END*****
void BOARD_InitBootPins(void) {
    BOARD_InitPins();
}

#define IOCON_PIO_DIGITAL_EN 0:
#define IOCON_PIO_FUNC1
#define IOCON_PIO_FUNC6
#define IOCON_PIO_INPFILT_OFF 0:
#define IOCON_PIO_INV_DI
#define IOCON_PIO_MODE_INACT
#define IOCON_PIO_OPENDRAIN_DI
#define IOCON_PIO_SLEW_STANDARD
#define PIN10_IDX
#define PIN29_IDX
#define PIN30_IDX
#define PORT0_IDX

/*
 * TEXT BELOW IS USED AS SETTING FOR
 * BOARD_InitPins:
 * - options: {callFromInitBoot: 'true',
 * - pin_list:
```

Problems
View

Routed Pins

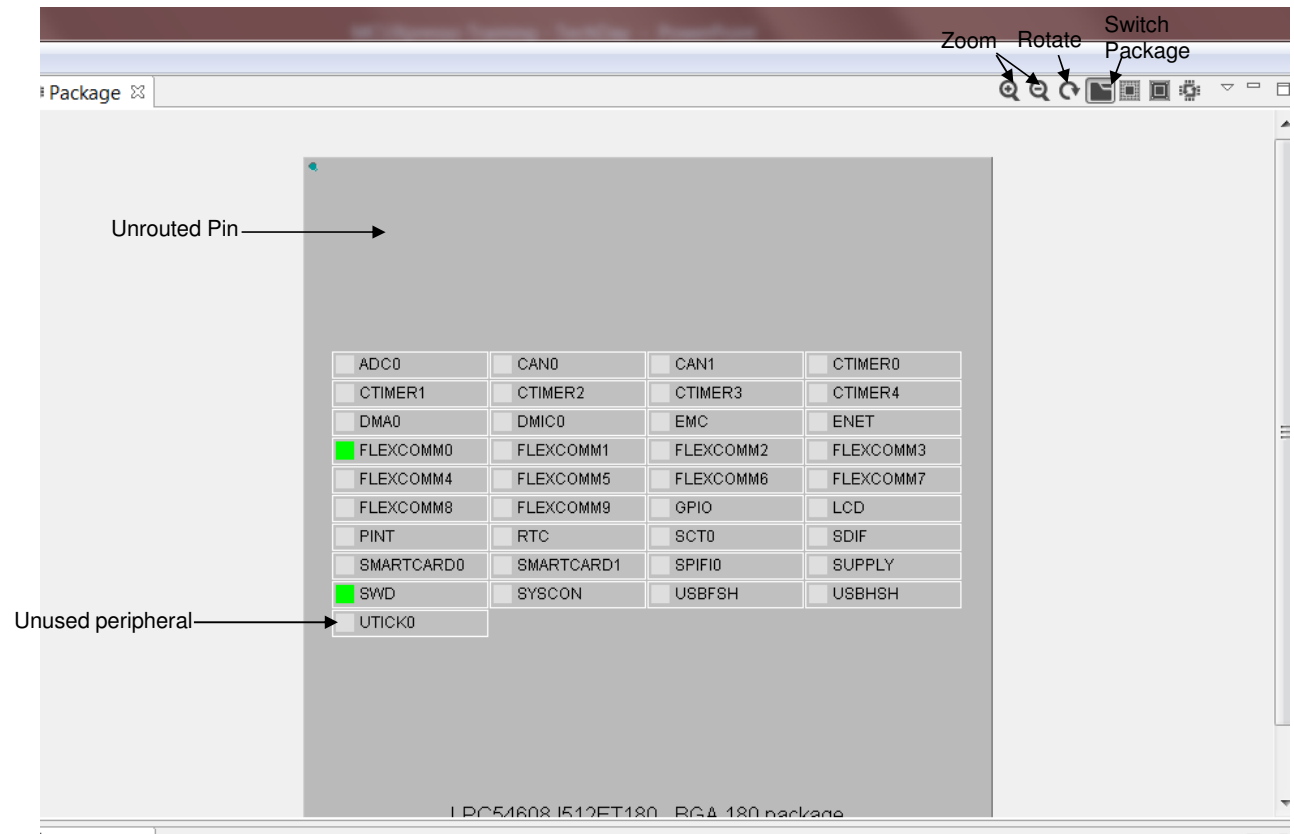
#	Peripheral	Signal	Route to	Label	Identifier	Direction	Mode	Invert
B13	FLEXCOMM0	RXD_SDA_MOSI	FC0_RXD_SDA_MOSI	U24[13]/P0_29-ISP_FC0_RXD	ISP_FC0_RXD	Not Specified	Inactive	Disablec
A2	FLEXCOMM0	TXD_SCL_MISO	FC0_TXD_SCL_MISO	U24[12]/P0_30-ISP_FC0_TXD	ISP_FC0_TXD	Not Specified	Inactive	Disablec
P2	SWD	SWO	SWO	U16[12]/SWO_TRGT	SWO_TRGT	Output	Inactive	Disablec

Routed Pins
view



Package View

- Provides overview of package
- Available peripherals are indicated inside the package
- Pin names are listed next to each pin
- Color Coding:
 - Green indicates pin/peripheral is routed
 - Yellow indicates pin/peripheral is currently selected
 - Red indicates an error
 - Light grey indicates pin/peripheral is available but is not currently routed



Pins View

- Provides a table of all the pins for the device / package
- Pins are listed by number and name
- Signals available for each pin are listed in columns across the pin's row
- The checkbox next to the pin name indicates whether the pin is routed

Signal routed to pin

Pin	Pin name	Label	Identifier	GPIO	UART	FTM	ADC	
<input type="checkbox"/>	60	VSS109	GND					
<input type="checkbox"/>	61	VDD110	P3V3_K64F					
<input checked="" type="checkbox"/>	62	UART0_RX	U7[4]/UART0...	DEBUG_UAR...	PTB16	UART0_RX	FTM_CLKIN0[...]	
<input checked="" type="checkbox"/>	63	UART0_TX	U10[1]/UART...	DEBUG_UAR...	PTB17	UART0_TX	FTM_CLKIN1[...]	
<input type="checkbox"/>	64	PTB18/CAN0...	J1[1]		PTB18		FTM2_CH0[...]	
<input type="checkbox"/>	65	PTB19/CAN0...	J1[3]		PTB19		FTM2_CH1[...]	
<input type="checkbox"/>	66	PTB20/SPI2_...	J6[3]/J4[9]/R...	RF_WIFI_CE	PTB20			
<input checked="" type="checkbox"/>	67	PTB21/SPI2_...	D12[3]/LEDR...	LED_BLUE	PTB21			
<input checked="" type="checkbox"/>	68	PTB22/SPI2_...	D12[1]/LEDR...	LED_RED	PTB22			
<input type="checkbox"/>	69	PTB23/SPI2_...	J1[10]		PTB23			
<input type="checkbox"/>	70	ADC0_SE14[...]	J1[11]		PTC0		ADC0_SE14[...]	
<input checked="" type="checkbox"/>	71	ADC0_SE15[...]	J1[5]		PTC1	UART1_RTS_b	FTM0_CH0	ADC0_SE15
<input checked="" type="checkbox"/>	72	ADC0_SE4b[...]	J1[14]		PTC2	UART1_CTS_b	FTM0_CH1	ADC0_SE4b
<input checked="" type="checkbox"/>	73	CMP1_IN1/P...	J1[16]		PTC3	UART1_RX	FTM0_CH2	
<input type="checkbox"/>	74	VSS123	GND					
<input type="checkbox"/>	75	VDD124	P3V3_K64F					
<input type="checkbox"/>	76	PTC4/LLWU_...	J2[4]		PTC4	UART1_TX	FTM0_CH3	
<input type="checkbox"/>	77	PTC5/LLWU_...	J1[15]		PTC5		FTM0_CH2	
<input checked="" type="checkbox"/>	78	CMP0_IN0/P...	U8[11]/SW2	SW2:ACCEL_I...	PTC6			PDB0_EXTRG...
<input type="checkbox"/>	79	CMP0_IN1/P...	J1[13]	CMP0_IN1	PTC7			
<input checked="" type="checkbox"/>	80	PTC8/FTM3_...	J1[7]		PTC8		FTM3_CH4	ADC1_SE4b
<input checked="" type="checkbox"/>	81	PTC9	J1[9]		PTC9		FTM3_CH5[...]	ADC1_SE5b
<input checked="" type="checkbox"/>	82	PTC10	J4[12]		PTC10		FTM3_CH6	ADC1_SE6b
<input checked="" type="checkbox"/>	83	PTC11	J4[10]		PTC11		FTM3_CH7	ADC1_SE7b
<input checked="" type="checkbox"/>	84	PTC12	J2[2]		PTC12	UART4_RTS_b	FTM3_FLT0	
<input checked="" type="checkbox"/>	85	PTC13/UART...	U8[9]	ACCEL_INT2	PTC13	UART4_CTS_b		
<input type="checkbox"/>	86	PTC14/UART...	J199[3]/BT_TX		PTC14	UART4_RX		
<input type="checkbox"/>	87	PTC15/UART...	J199[4]/BT_RX		PTC15	UART4_TX		
<input type="checkbox"/>	88	VSS139	GND					

Routed Pins → [pins 62, 63, 71, 72, 73, 78, 81, 82, 83, 84, 85]

Unrouted Pins → [pins 60, 61, 64, 65, 66, 67, 68, 69, 70, 74, 75, 76, 77, 79, 80, 86, 87, 88]

Pin Error → [pin 80]



Routed Pins View

Remove row

Add row

#	Peripheral	Signal	Route to	Label	Identifier	Direction	Mode	Invert
B13	FLEXCOMMO	RXD_SDA_MOSI	FC0_RXD_SDA_MOSI	U24[13]/P0_29-ISP_FC0_RXD	ISP_FC0_RXD	Not Specified	Inactive	Disablc
A2	FLEXCOMMO	TXD_SCL_MISO	FC0_TXD_SCL_MISO	U24[12]/P0_30-ISP_FC0_TXD	ISP_FC0_TXD	Not Specified	Inactive	Disablc
P2	SWD	SWO	SWO	U16[12]/SWO_TRGT	SWO_TRGT	Output	Inactive	Disablc

Click on fields to modify

Add function

Functions

- View shows table of every routed pin
- 'Functions' are used to group a set of routed pins
- Functions create code which can be called by the application.

Functions

- Functions in Routed Pins View are used to generate functions in source code
- Pins that are routed in the Routed pins view will be initialized in the corresponding function in the source code

The screenshot shows the TI Pin Manager interface. At the top, there is a grid of peripheral selection buttons. Below it, the 'Routed Pins' view is displayed as a table. A red box highlights the 'BOARD_InitPins' function name in the bottom-left corner of the interface. A red arrow points from this box to the source code on the right, where the function definition is shown. The source code includes headers, a function comment, and the function definition: `void BOARD_InitBootPins(void) { BOARD_InitPins(); }`. A tooltip 'Show only routed pins containing specified text.' is visible over the code area.

#	Peripheral	Signal	Route to	Label	Identifier	Direction	Mode	Invert
B13	FLEXCOMM0	RXD_SDA_MOSI	FC0_RXD_SDA_MOSI	U24[13]/P0_29-ISP_FC0_RXD	ISP_FC0_RXD	Not Specified	Inactive	Disablec
A2	FLEXCOMM0	TXD_SCL_MISO	FC0_TXD_SCL_MISO	U24[12]/P0_30-ISP_FC0_TXD	ISP_FC0_TXD	Not Specified	Inactive	Disablec
P2	SWD	SWO	SWO	U16[12]/SWO_TRGT	SWO_TRGT	Output	Inactive	Disablec

```
pin_mux.c pin_mux.h
/*
 * TEXT BELOW IS USED AS SETTING FOR
 !!GlobalInfo
product: Pins v3.0
processor: LPC54608J512
package_id: LPC54608J512ET180
mcu_data: ksdk2_0
processor_version: 2.0.2
board: LPCXpresso54608
 * BE CAREFUL MODIFYING THIS COMMENT
 */

#include "fsl_common.h"
#include "fsl_iocon.h"
#include "pin_mux.h"

/*FUNCTION*****
 * Function Name : BOARD_InitBootPins
 * Description : Calls initializati
 *
 *END*****
void BOARD_InitBootPins(void) {
    BOARD_InitPins();
}

#define IOCON_PIO_DIGITAL_EN 0:
#define IOCON_PIO_FUNC1
Show only routed pins containing specified text.
#define IOCON_PIO_INPFILT_OFF 0:
#define IOCON_PIO_INV_DI
#define IOCON_PIO_MODE_INACT
#define IOCON_PIO_OPENDRAIN_DI
#define IOCON_PIO_SLEW_STANDARD
#define PIN10_IDX
#define PIN29_IDX
#define PIN30_IDX
#define PORT0_IDX

/*
 * TEXT BELOW IS USED AS SETTING FOR
 BOARD_InitPins:
 - options: {callFromInitBoot: 'true',
 - pin_list:
```

Labels and Identifiers

- Board and kit configurations have predefined pin labels and identifiers
- Label
 - Can be defined for any pin for easy identification
- Identifier
 - Used to generate the #define in the pin_mux.h file
 - Can be modified in Pins View

The screenshot displays a software development environment with three main components:

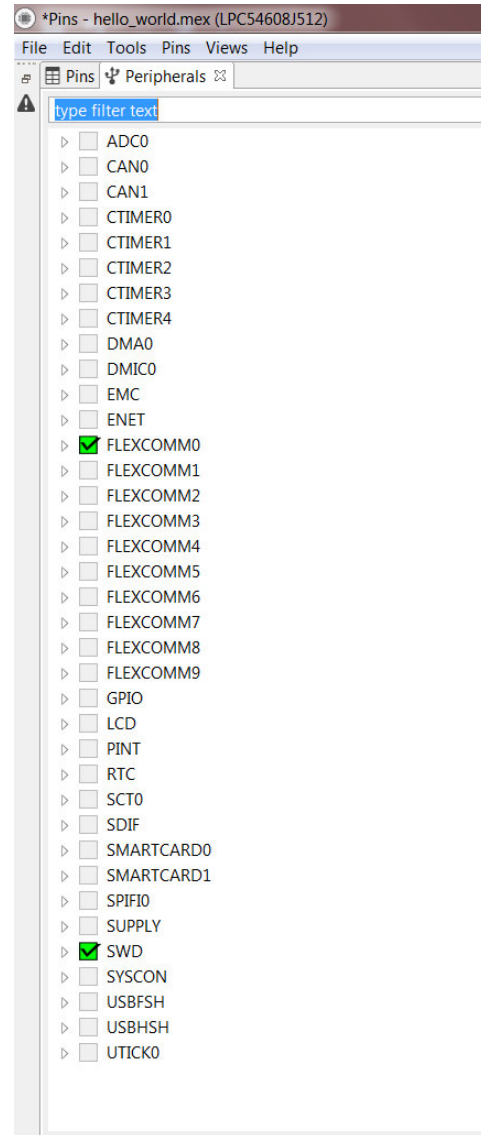
- Package View:** A grid of peripheral labels for the LPC54608J512ET180 - BGA 180 package. The SWD peripheral is highlighted in green.
- Routed Pins Table:** A table showing the mapping of signals to pins. The 'Identifier' column for the SWD signal is highlighted in red.
- Code Editor:** The pin_mux.h file, showing the BOARD_InitPins function. A red bracket highlights the configuration for the SWD pin (pin 12), which corresponds to the identifier SWO_TRGT in the table above.

#	Peripheral	Signal	Route to	Label	Identifier	Direction	Mode	Invert
B13	FLEXCOMM0	RXD_SDA_MOSI	FC0_RXD_SDA_MOSI	U24[13]/P0_29-ISP_FC0_RXD	ISP_FC0_RXD	Not Specified	Inactive	Disablec
A2	FLEXCOMM0	TXD_SCL_MISO	FC0_TXD_SCL_MISO	U24[12]/P0_30-ISP_FC0_TXD	ISP_FC0_TXD	Not Specified	Inactive	Disablec
P2	SWD	SWO	SWO	U16[12]/SWO_TRGT	SWO_TRGT	Output	Inactive	Disablec



Peripherals View

- Displays list of all peripherals of device
- Expand peripheral to see available signals
- Peripherals with marks in checkbox have signals routed



Sources View

- The pins tool modifies and creates code in pin_mux.c and pin_mux.h files
- The pin configuration info is stored in YAML format
- YAML code is not intended for user modification

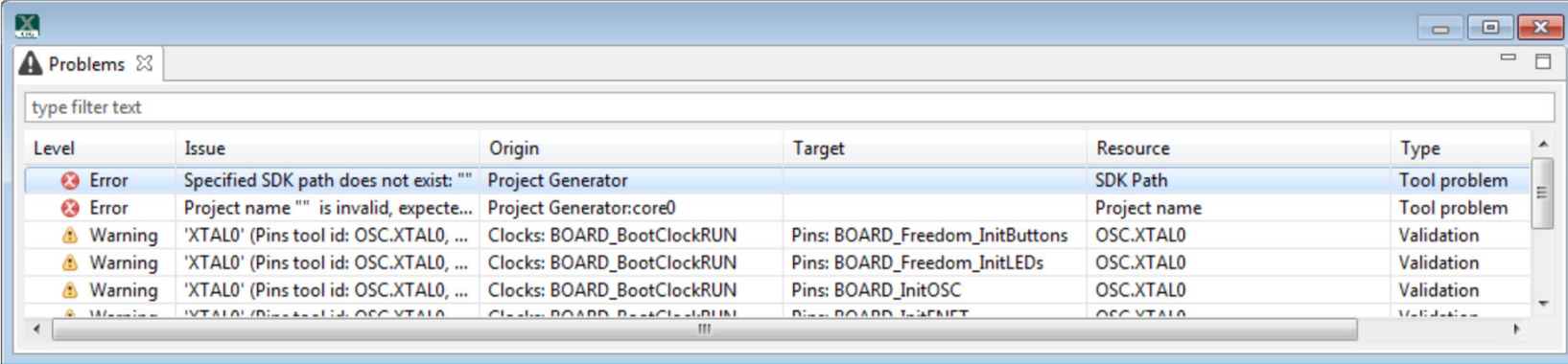
```
*Pins - hello_world.mex (LPC54608J512)
File Edit Tools Pins Views Help
Registers Log Sources
pin_mux.c pin_mux.h
/*FUNCTION*****
*
* Function Name : BOARD_InitPins
* Description   : Configures pin routing and optionally pin electrical features.
*
*END*****/
void BOARD_InitPins(void) { /* Function assigned for the Core #0 (ARM Cortex-M4) */
    CLOCK_EnableClock(kCLOCK_Iocon); /* Enables the clock for the IOCON block. 0 = Disable; 1 = Enable.: 0x01u */

    const uint32_t port0_pin10_config = (
        IOCON_PIO_FUNC6 | /* Pin is configured as SW0 */
        IOCON_PIO_MODE_INACT | /* No addition pin function */
        IOCON_PIO_INV_DI | /* Input function is not inverted */
        IOCON_PIO_DIGITAL_EN | /* Enables digital function */
        IOCON_PIO_INPFILT_OFF | /* Input filter disabled */
        IOCON_PIO_OPENDRAIN_DI | /* Open drain is disabled */
    );
    IOCON_PinMuxSet(IOCON, PORT0_IDX, PIN10_IDX, port0_pin10_config); /* PORT0 PIN10 (coords: P2) is configured as SW0 */
    const uint32_t port0_pin29_config = (
        IOCON_PIO_FUNC1 | /* Pin is configured as FC0_RXD_SDA_MOSI */
        IOCON_PIO_MODE_INACT | /* No addition pin function */
        IOCON_PIO_INV_DI | /* Input function is not inverted */
        IOCON_PIO_DIGITAL_EN | /* Enables digital function */
        IOCON_PIO_INPFILT_OFF | /* Input filter disabled */
        IOCON_PIO_SLEW_STANDARD | /* Standard mode, output slew rate control is enabled */
        IOCON_PIO_OPENDRAIN_DI | /* Open drain is disabled */
    );
    IOCON_PinMuxSet(IOCON, PORT0_IDX, PIN29_IDX, port0_pin29_config); /* PORT0 PIN29 (coords: B13) is configured as FC0_RXD_SDA_MOSI */
    const uint32_t port0_pin30_config = (
        IOCON_PIO_FUNC1 | /* Pin is configured as FC0_TXD_SCL_MISO */
        IOCON_PIO_MODE_INACT | /* No addition pin function */
        IOCON_PIO_INV_DI | /* Input function is not inverted */
        IOCON_PIO_DIGITAL_EN | /* Enables digital function */
        IOCON_PIO_INPFILT_OFF | /* Input filter disabled */
        IOCON_PIO_SLEW_STANDARD | /* Standard mode, output slew rate control is enabled */
        IOCON_PIO_OPENDRAIN_DI | /* Open drain is disabled */
    );
    IOCON_PinMuxSet(IOCON, PORT0_IDX, PIN30_IDX, port0_pin30_config); /* PORT0 PIN30 (coords: A2) is configured as FC0_TXD_SCL_MISO */
}

/*****
* EOF
*****/
```



Problems View

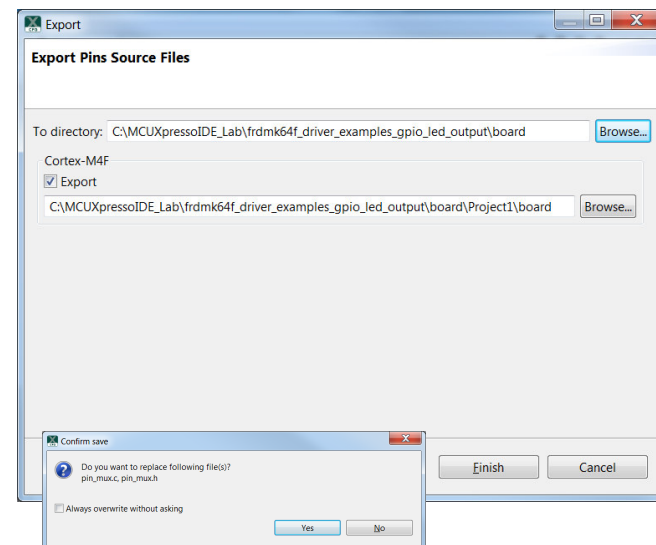
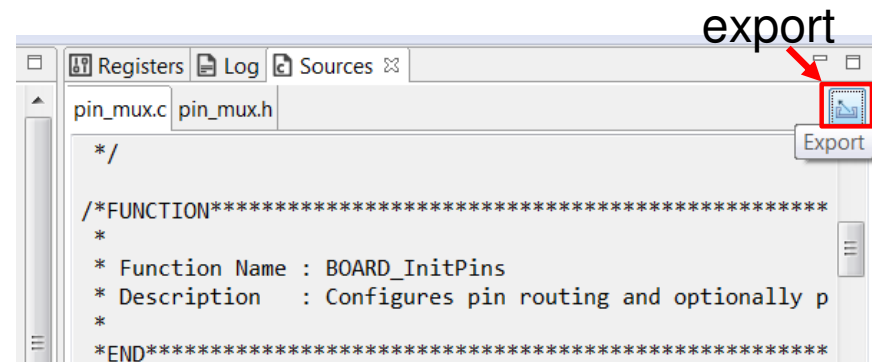


Level	Issue	Origin	Target	Resource	Type
Error	Specified SDK path does not exist: ""	Project Generator		SDK Path	Tool problem
Error	Project name "" is invalid, expecte...	Project Generator:core0		Project name	Tool problem
Warning	'XTAL0' (Pins tool id: OSC.XTAL0, ...	Clocks: BOARD_BootClockRUN	Pins: BOARD_Freedom_InitButtons	OSC.XTAL0	Validation
Warning	'XTAL0' (Pins tool id: OSC.XTAL0, ...	Clocks: BOARD_BootClockRUN	Pins: BOARD_Freedom_InitLEDs	OSC.XTAL0	Validation
Warning	'XTAL0' (Pins tool id: OSC.XTAL0, ...	Clocks: BOARD_BootClockRUN	Pins: BOARD_InitOSC	OSC.XTAL0	Validation
Warning	'XTAL0' (Pins tool id: OSC.XTAL0, ...	Clocks: BOARD_BootClockRUN	Pins: BOARD_InitNET	OSC.XTAL0	Validation

- **Level** – Lists the severity of the problem: Information, Warning, or Error.
- **Issue** – Description of the problem.
- **Origin** – Information on the dependency source.
- **Target** – Lists the tool that handled the dependency and where it should be fulfilled.
- **Resource** – Lists the resource which is related to the problem,. For example, the signal name, the clock signal, and so on.
- **Type** – The type of the problem. It is either the validation that is

Export Source Files

- Export a configuration to a pin_mux.c and pin_mux.h file
- Includes functions with initialization for routed pins in configurations
- Accessed from menu:
 - File->Export
 - Can also access by selecting the export icon in the Sources view
- Select directory to export pin_mux.c and pin_mux.h



MCUXPRESSO CONFIG TOOLS CLOCK TOOL



Clocks Tool Views

Clocks Table

Clocks Diagram

Global Settings

Clock Configuration tabs

Status bar

Details View Selected

Problems View

The screenshot displays the NXP Clocks Tool interface for a project named "FRDM-K64F.mex (MK64FN1M0xxx12)". The main window is divided into several sections:

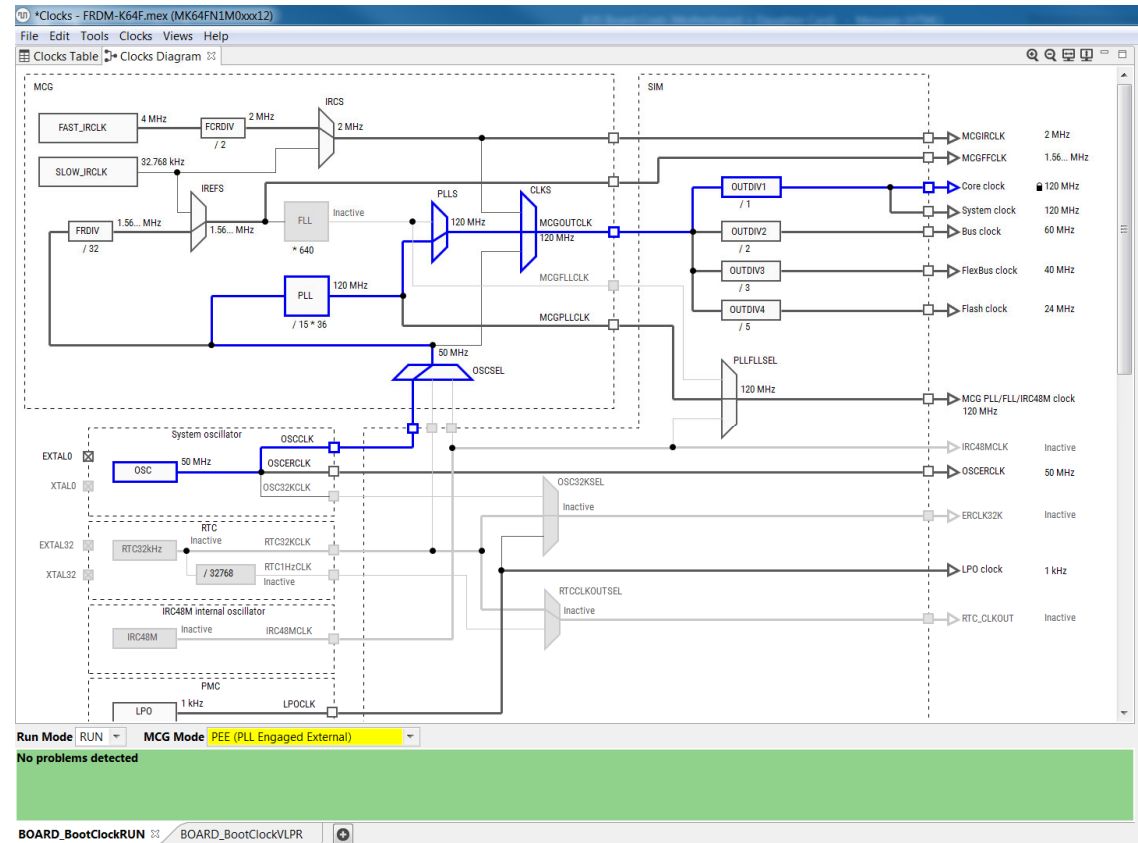
- Clocks Diagram:** A central schematic showing the clock tree. It includes components like FAST_IRCLK (4 MHz), SLOW_IRCLK (32.768 kHz), FRODIV (1.56 MHz), IREFS (1.56 MHz), FLL (Inactive), PLL (120 MHz), MCGOUTCLK (120 MHz), MCGFLLCLK, MCGPFLCLK, OUTDIV1-4 (7/1, 7/2, 7/3, 7/5), OSCSEL (50 MHz), and various peripheral clocks like IRC48MCLK, OSOERCLK, ERCLK32K, RTCCLK, LPOCLK, and LPOCLK.
- Processor Details:** A table on the right showing the configuration for various clocks. The "Value" column is highlighted in yellow.
- Global Settings:** At the bottom left, "Run Mode" is set to "RUN" and "MCG Mode" is set to "PEE (PLL Engaged External)".
- Status bar:** At the bottom, it shows "No problems detected" and "BOARD_BootClockRUN".
- Problems View:** A table at the bottom right for reporting issues, currently empty.

Name	Available	Lock	Value
Core clock		<input checked="" type="checkbox"/>	120 MHz
System clock		<input checked="" type="checkbox"/>	120 MHz
Bus clock		<input checked="" type="checkbox"/>	60 MHz
FlexBus clock		<input checked="" type="checkbox"/>	40 MHz
Flash clock		<input checked="" type="checkbox"/>	24 MHz
MCGIRCLK		<input checked="" type="checkbox"/>	2 MHz
MCGFCLK		<input checked="" type="checkbox"/>	1.56... MHz
OSCCERCLK		<input checked="" type="checkbox"/>	50 MHz
ERCLK32K		<input checked="" type="checkbox"/>	Inactive
RTCCLKOUT		<input checked="" type="checkbox"/>	Inactive
Initialize RTCCLKOUT		<input checked="" type="checkbox"/>	yes
MCG PLL/FLL/IRC48M clock		<input checked="" type="checkbox"/>	120 MHz
LPO clock		<input checked="" type="checkbox"/>	1 kHz
IRC48MCLK		<input checked="" type="checkbox"/>	Inactive
USB FS clock		<input checked="" type="checkbox"/>	48 MHz
Initialize USB clock		<input checked="" type="checkbox"/>	yes
Trace clock input		<input checked="" type="checkbox"/>	120 MHz
Initialize Itrace clock		<input checked="" type="checkbox"/>	yes
ENET IEEE 15_888 clock		<input checked="" type="checkbox"/>	50 MHz
Initialize E...1588 clock		<input checked="" type="checkbox"/>	yes
ENET RMII clock		<input checked="" type="checkbox"/>	50 MHz
Initialize RMII clock		<input checked="" type="checkbox"/>	yes
SDHC clock		<input checked="" type="checkbox"/>	50 MHz
Initialize SDHC clock		<input checked="" type="checkbox"/>	yes



Clocks Diagram View

- Provides a block diagram of the clock generation for the device
- Solid lines indicate connections between elements
 - Dark lines indicate currently active clock paths
 - Gray lines indicate inactive clock paths
- Clock settings can be edited within the diagram
- When an active clock output is selected (e.g. Core clock), the clock path highlights in blue



Elements of Clock Diagram

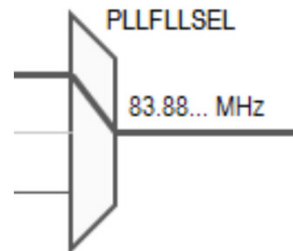
- **Clock Source**

- Provides a clock frequency



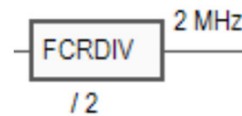
- **Multiplexer**

- Selects between clock options



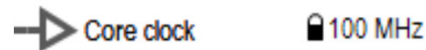
- **Prescaler**

- Divides clock frequency



- **Clock Output**

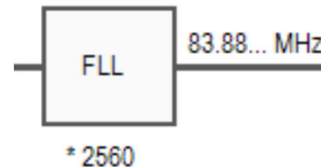
- Marks the clock signal output



Elements of Clock Diagram (cont)

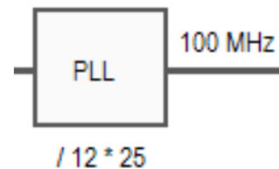
- **FLL (Frequency Locked Loop)**

- Multiplies an incoming frequency by a given factor



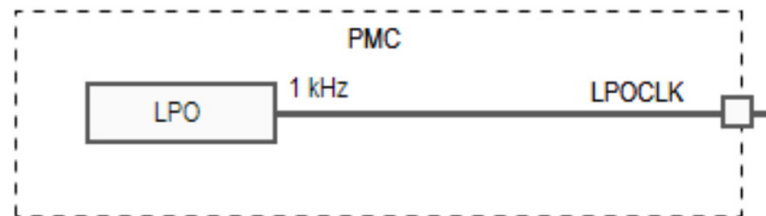
- **PLL (Phase Locked Loop)**

- Contains pre-divider and thus is able to divide/multiply with a given value.



- **Clock Component**

- Group of clock elements surrounded with a border. The clock component usually corresponds to the processor modules or peripherals.



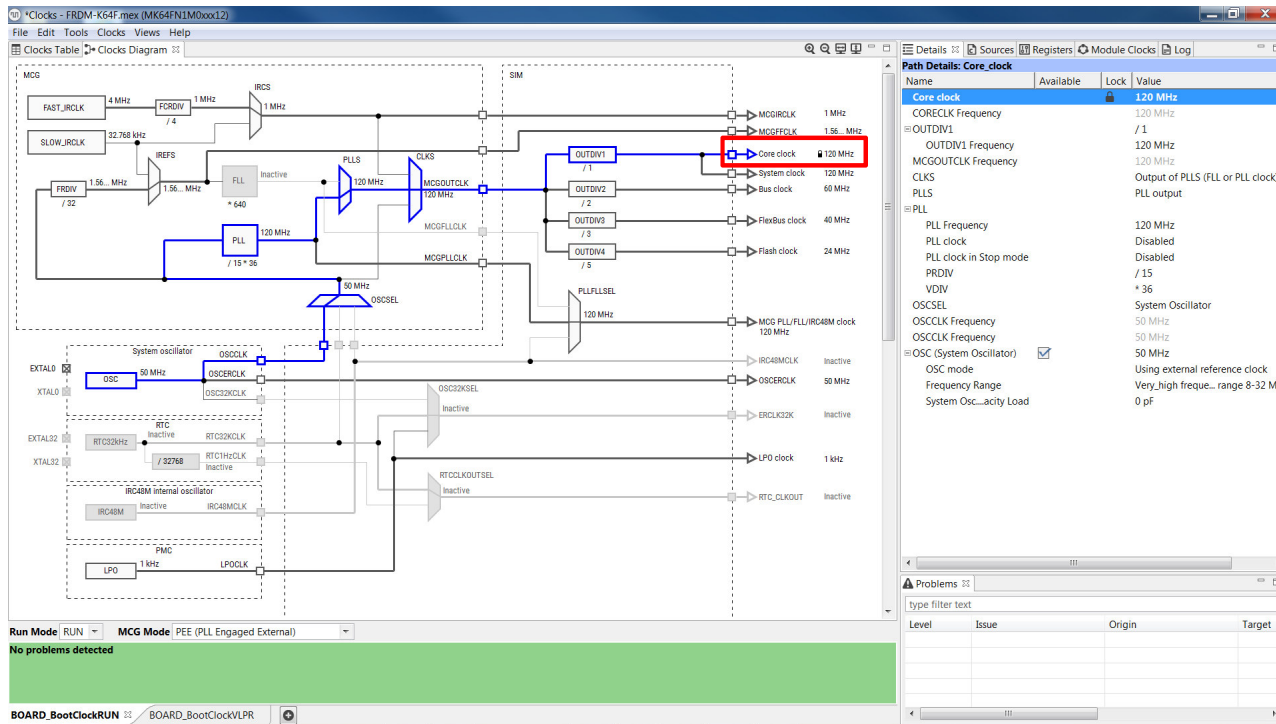
Details View: Overview

- The details for any element in the block diagram are displayed in the Details view when selected in the diagram
- The MCG component is selected in the figure to the right. The details for clocks, mux settings, and dividers in the MCG are shown in the details view

The screenshot shows the 'Clocks - FRDM-K64F.mex (MK64FN1M0xx12)' configuration tool. The main window displays a block diagram of the MCG (Microcontroller Clock Generator) component. The 'Details' pane on the right shows the configuration for the selected MCG component.

Name	Available	Lock	Value
FAST_JRCLK			4 MHz
SLOW_JRCLK			32.768 kHz
FCRDIV			/ 4
FCRDIV Frequency			1 MHz
JRCS			Fast internal reference clock
OSCESEL			System Oscillator
FRDIV			/ 32
FRDIV Frequency			1.56... MHz
Frequency Range			Very high frequen...V range 32-155
IREFS			External reference clock
FLL			Inactive
FLL Frequency			* 640
FLL Factor			* 640
PLL			120 MHz
PLL Frequency			120 MHz
PLL clock			Disabled
PLL clock in Stop mode			Disabled
PRDIV			/ 13
VDIV			* 36
PLL output			Output of PLLS (FLL or PLL clock)
CLKS			120 MHz
MCGOUTCLK Frequency			1 MHz
MCGIRCLK output			Enabled
MCGIRCLK...top mode			Disabled
Allow MCGFFCLK clock			yes
MCGFFCLK Frequency			1.56... MHz
MCGFLLCLK Frequency			Inactive
MCGPLLCLK Frequency			120 MHz

Details View: Clock Path Details



- Clock path details are shown in the Details View when a clock output is selected (in Clock Diagram or Clock Table)
- The Details view shows information for each element in the clock path (e.g. OSC, PLL, mux selections, divider settings)

Clocks Table View

- Provides overview of the clocking system and its current state
- Available clock sources are shown in the left panel
- Clock outputs and their current frequencies are shown in the right panel

The screenshot displays the 'Clocks Table View' for an FRDM-K64F board. The interface is divided into several panels:

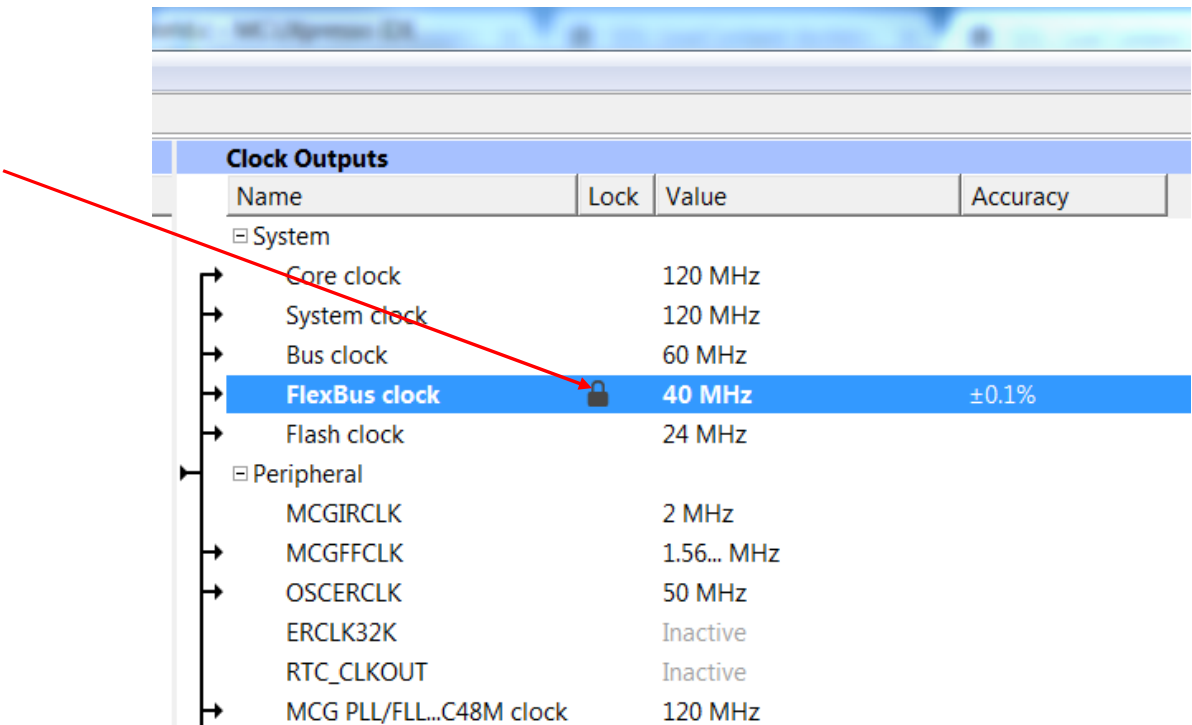
- Clock Sources Table:**


Name	Available	Value
Internal		
FAST_IRCLK		4 MHz
SLOW_IRCLK		32.768 kHz
IRC48M		Inactive
LPO		1 kHz
External		
OSC (System Oscillator)	<input checked="" type="checkbox"/>	50 MHz
RTC32kHz	<input type="checkbox"/>	Inactive
USB clock input	<input type="checkbox"/>	Inactive
ENET 1588 clock input	<input type="checkbox"/>	Inactive
- Clock Outputs Table:**

Name	Lock	Value	Accuracy
System			
Core clock	<input checked="" type="checkbox"/>	120 MHz	±0.1%
System clock		120 MHz	
Bus clock		60 MHz	
FlexBus clock		40 MHz	
Flash clock		24 MHz	
Peripheral			
MCGIRCLK		2 MHz	
MCGFFCLK		1.56... MHz	
OSCCERCLK		50 MHz	
ERCLK32K		Inactive	
RTC_CLKOUT		Inactive	
MCG PLL/FLL_C48M clock		120 MHz	
LPO clock		1 kHz	
IRC48MCLK		Inactive	
USB FS clock		48 MHz	
Trace clock input		120 MHz	
ENET IEEE 1588 clock		50 MHz	
ENET RMII clock		50 MHz	
SDHC clock		50 MHz	
CLKOUT(FB_CLK)		40 MHz	
- Code Generation Panel:** Shows a list of instructions for setting up the clocking system, including:
 - 1. CLOCK_SetSimSafeDivs, to make sure core clock, bus and flash clock are in allowed range during clock r...
 - 2. Call CLOCK_Osc0Init to setup OSC clock, if it is u...
 - 3. Set MCG configuration, MCG includes three parts: FI...
 - 4. Call CLOCK_SetSimConfig to set the clock configurat...
- Status Bar:** Indicates 'Run Mode: RUN', 'MCG Mode: PEE (PLL Engaged External)', and 'No problems detected'. A message at the bottom states 'Code successfully generated.'

Locked Settings

- Lock Icon indicates that a setting (that may be automatically adjusted by the tool) is locked to prevent any automatic adjustment.
- If the setting can be locked, they are automatically locked when you change the value.
- To add/remove the lock manually, use the pop-up menu command **Lock/Unlock**.



Clock Outputs			
Name	Lock	Value	Accuracy
System			
Core clock		120 MHz	
System clock		120 MHz	
Bus clock		60 MHz	
FlexBus clock		40 MHz	±0.1%
Flash clock		24 MHz	
Peripheral			
MCGIRCLK		2 MHz	
MCGFFCLK		1.56... MHz	
OSCERCLK		50 MHz	
ERCLK32K		Inactive	
RTC_CLKOUT		Inactive	
MCG PLL/FLL...C48M clock		120 MHz	

Dependency Arrows

- Arrows between the Clock Sources and Clock Outputs indicate dependency
- Arrows lead from the clock source used for the selected output
- Arrows lead to clock outputs that are using the signal from the same clock source (as selected output)

The screenshot displays the 'Clocks' configuration window for the FRDM-K64F. It is divided into two main sections: 'Clock Sources' and 'Clock Outputs'. The 'Clock Sources' section lists various sources, with 'OSC (System oscillator)' selected. The 'Clock Outputs' section lists various outputs, with 'System clock' selected. Arrows indicate dependencies between sources and outputs. The 'Details' pane on the right shows the generated code for the clock configuration, including comments and function calls like `CLOCK_SetSimSafeDivs` and `CLOCK_Osc0Init`. The status bar at the bottom indicates 'No problems detected'.

Clock Sources		Clock Outputs			
Name	Available	Name	Lock	Value	Accuracy
Internal					
FAST_IRCLK		Core clock	✓	120 MHz	±0.1%
SLOW_IRCLK		System clock		120 MHz	
IRC48M		Bus clock		60 MHz	
LPO		FlexBus clock		40 MHz	
External					
OSC (System oscillator)	✓	Flash clock		24 MHz	
RTC32kHz		Peripheral			
USB clock input		MCGIRCLK		2 MHz	
ENET 1588 clock input		MCGFFCLK		156. MHz	
		OSCCERCLK		50 MHz	
		ERCLK32K		Inactive	
		RTC_CLKOUT		Inactive	
		MCG PLL/FLL_C48M clock		120 MHz	
		LPO clock		1 kHz	
		IRC48MCLK		Inactive	
		USB FS clock		48 MHz	
		Trace clock input		120 MHz	
		ENET IEEE 1588 clock		50 MHz	
		ENET RMII clock		50 MHz	
		SDHC clock		50 MHz	
		CLKOUT(FB_CLK)		40 MHz	

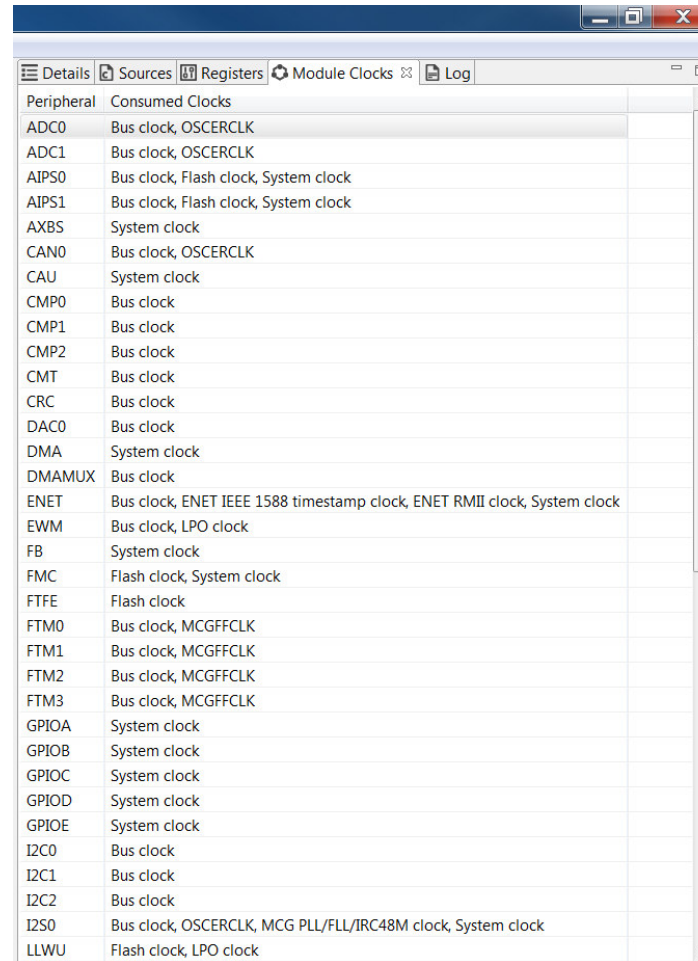
Enabling External Clock Sources in Clocks Table View

- External clock sources can be enabled in the Clock Sources panel
- External clock settings can also be changed in this view

Name	Available	Value
Internal		
FAST_IRCLK		4 MHz
SLOW_IRCLK		32.768 kHz
IRC48M		Inactive
LPO		1 kHz
External		
OSC (System Oscillator)	<input checked="" type="checkbox"/>	50 MHz
OSC mode		Using external reference clock
Frequency Range		Very_high freque... range 8-32 MHz
System Os...ity Load		0 pF
RTC32kHz	<input type="checkbox"/>	Inactive
RTC 32kHz oscillator		Enabled
RTC32KCLK output		Enabled
RTC Oscill...city Load		10 pF
RTC initialization		yes
USB clock input	<input type="checkbox"/>	Inactive
ENET 1588 clock input	<input type="checkbox"/>	Inactive

Module Clocks View

- Provides list of peripherals and currently selected clock sources



The screenshot shows a software window titled "Module Clocks" with a menu bar containing "Details", "Sources", "Registers", "Module Clocks", and "Log". The main area is a table with two columns: "Peripheral" and "Consumed Clocks".

Peripheral	Consumed Clocks
ADC0	Bus clock, OSCERCLK
ADC1	Bus clock, OSCERCLK
AIPS0	Bus clock, Flash clock, System clock
AIPS1	Bus clock, Flash clock, System clock
AXBS	System clock
CAN0	Bus clock, OSCERCLK
CAU	System clock
CMP0	Bus clock
CMP1	Bus clock
CMP2	Bus clock
CMT	Bus clock
CRC	Bus clock
DAC0	Bus clock
DMA	System clock
DMAMUX	Bus clock
ENET	Bus clock, ENET IEEE 1588 timestamp clock, ENET RMII clock, System clock
EWM	Bus clock, LPO clock
FB	System clock
FMC	Flash clock, System clock
FTFE	Flash clock
FTM0	Bus clock, MCGFFCLK
FTM1	Bus clock, MCGFFCLK
FTM2	Bus clock, MCGFFCLK
FTM3	Bus clock, MCGFFCLK
GPIOA	System clock
GPIOB	System clock
GPIOC	System clock
GPIOD	System clock
GPIOE	System clock
I2C0	Bus clock
I2C1	Bus clock
I2C2	Bus clock
I2S0	Bus clock, OSCERCLK, MCG PLL/FLL/IRC48M clock, System clock
LLWU	Flash clock, LPO clock

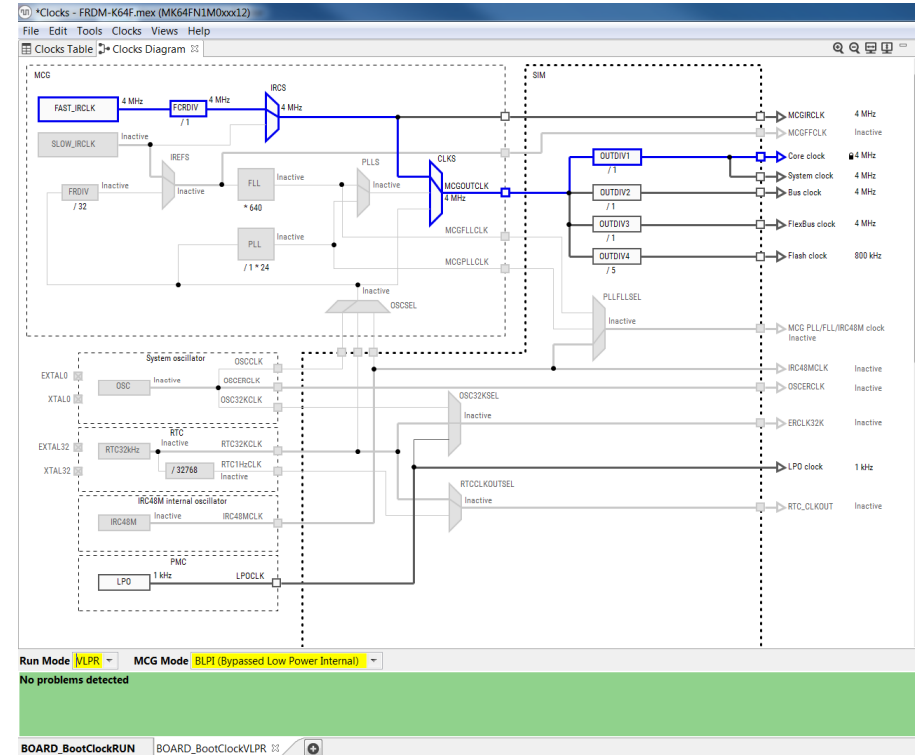
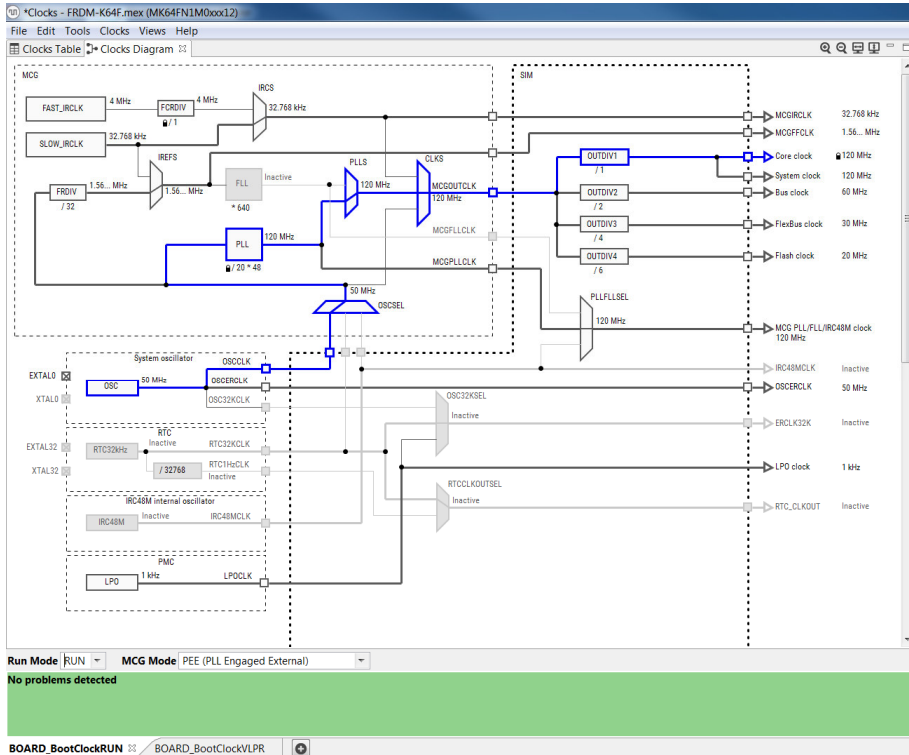
Registers View

The screenshot shows the Registers View of a software tool. The left pane displays a clock tree diagram with various clock sources and dividers. The right pane shows a table of registers with their current and reset values. The table is highlighted in yellow for several registers.

Reg. Name	Set Value	Reset Value
MCG_C1	0x02	0x04
MCG_C2	0xa1	0x80
MCG_C4	0x??	0x??
MCG_C5	0x0e	0x00
MCG_C6	0x4c	0x00
MCG_C7	0x00	0x00
MCG_SC	0x02	0x02
OSG_CR	0x80	0x00
RTC_CR	0x00002900	0x00000000
SIM_CLKDIV1	0x01240000	0x00110000
OUTDIV1 (bits 31-28)	0b0000	0b0000
OUTDIV2 (bits 27-24)	0b0001	0b0000
OUTDIV3 (bits 23-20)	0b0010	0b0001
OUTDIV4 (bits 19-16)	0b0100	0b0001
Reserved (bits 15-0)	0b000000000000...	0b000000000000...
SIM_CLKDIV2	0x00000009	0x00000000
SIM_SOPT1	0x800870??	0x800070??
SIM_SOPT2	0x20251010	0x00001000

- Displays register values for current clock configuration
- Current register value and default value after reset are shown
- Recently changed registers are highlighted in yellow.

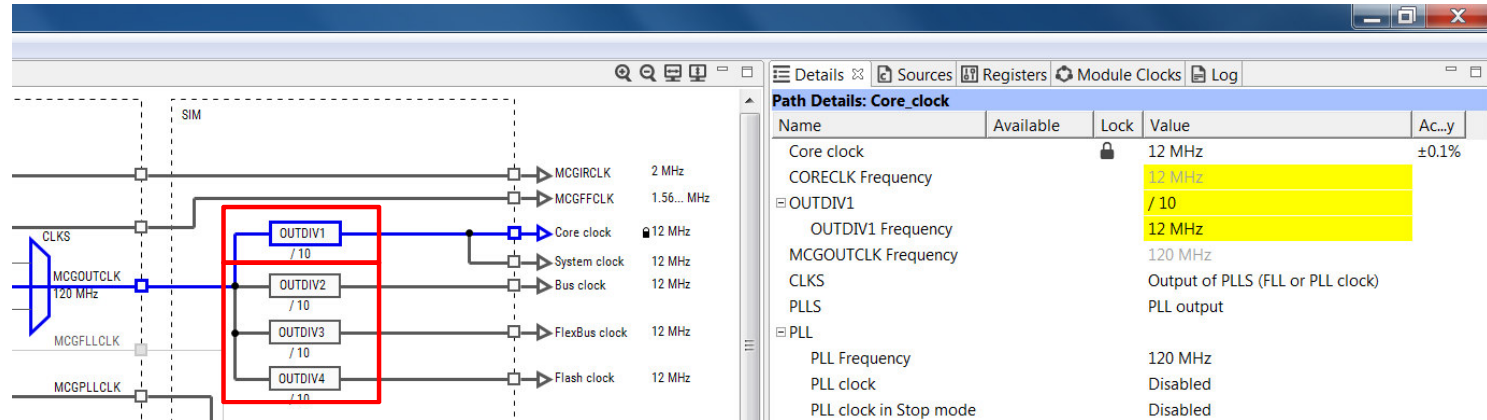
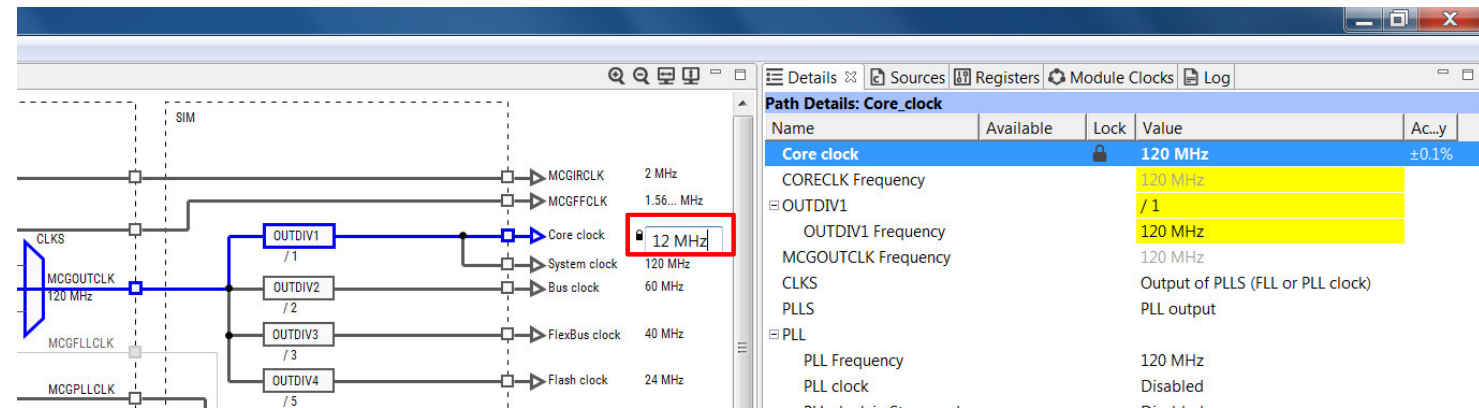
Configuration Tabs



- Switch between clock configurations using the tabs

Clocks Diagram: Change Clock Output Frequency

- Clock output frequency can be typed directly into the field (e.g. core clock)
- Tool will attempt to achieve target frequency by increasing divider (e.g. OUTDIV1)
- Bus/Flexbus/Flash divide values also update to meet requirement (must be less than or equal to core clock)



Clocks Diagram: Component Settings

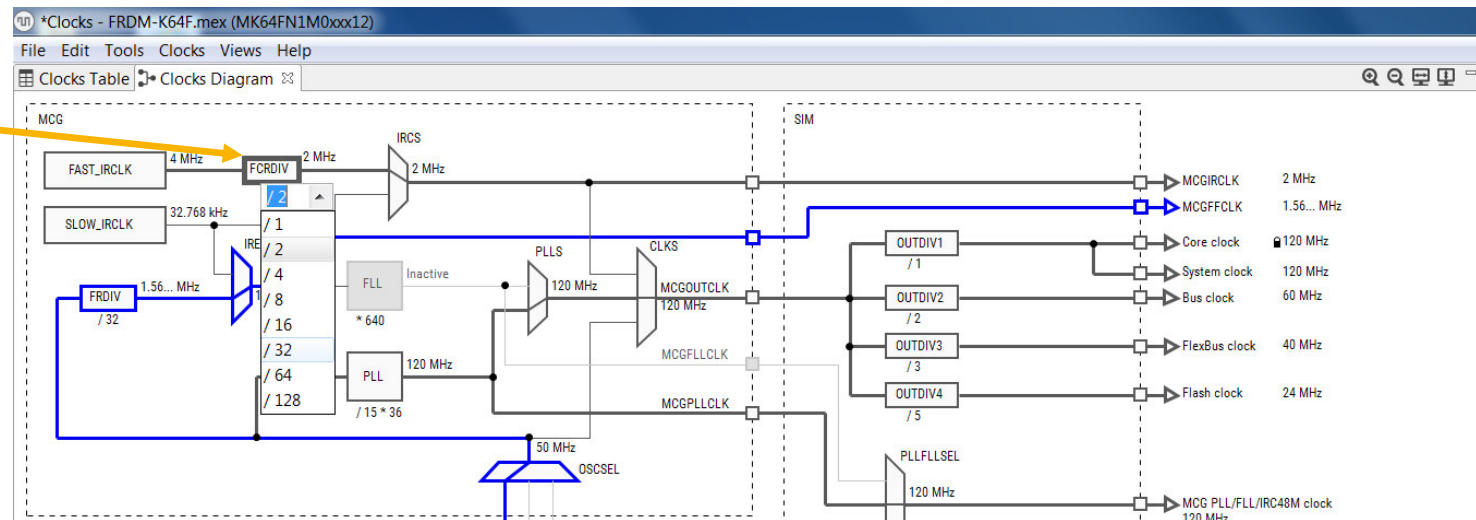
- Double click on a component in the block diagram to view/modify its configuration
- Pop-up box shows current configuration of component
- Element settings (e.g. frequency, etc.) can be modified in pop-up box

The screenshot displays the Clocks Diagram tool interface. The main window shows a clock tree diagram with various components like FAST_IRCLK, SLOW_IRCLK, PFDIV, PFDIV2, PFDIV3, PFDIV4, PFDIV5, PFDIV6, PFDIV7, PFDIV8, PFDIV9, PFDIV10, PFDIV11, PFDIV12, PFDIV13, PFDIV14, PFDIV15, PFDIV16, PFDIV17, PFDIV18, PFDIV19, PFDIV20, PFDIV21, PFDIV22, PFDIV23, PFDIV24, PFDIV25, PFDIV26, PFDIV27, PFDIV28, PFDIV29, PFDIV30, PFDIV31, PFDIV32, PFDIV33, PFDIV34, PFDIV35, PFDIV36, PFDIV37, PFDIV38, PFDIV39, PFDIV40, PFDIV41, PFDIV42, PFDIV43, PFDIV44, PFDIV45, PFDIV46, PFDIV47, PFDIV48, PFDIV49, PFDIV50, PFDIV51, PFDIV52, PFDIV53, PFDIV54, PFDIV55, PFDIV56, PFDIV57, PFDIV58, PFDIV59, PFDIV60, PFDIV61, PFDIV62, PFDIV63, PFDIV64, PFDIV65, PFDIV66, PFDIV67, PFDIV68, PFDIV69, PFDIV70, PFDIV71, PFDIV72, PFDIV73, PFDIV74, PFDIV75, PFDIV76, PFDIV77, PFDIV78, PFDIV79, PFDIV80, PFDIV81, PFDIV82, PFDIV83, PFDIV84, PFDIV85, PFDIV86, PFDIV87, PFDIV88, PFDIV89, PFDIV90, PFDIV91, PFDIV92, PFDIV93, PFDIV94, PFDIV95, PFDIV96, PFDIV97, PFDIV98, PFDIV99, PFDIV100. A pop-up window titled 'System Oscillator: [OSC]' is open, showing the configuration for the System Oscillator. The configuration includes the following settings:

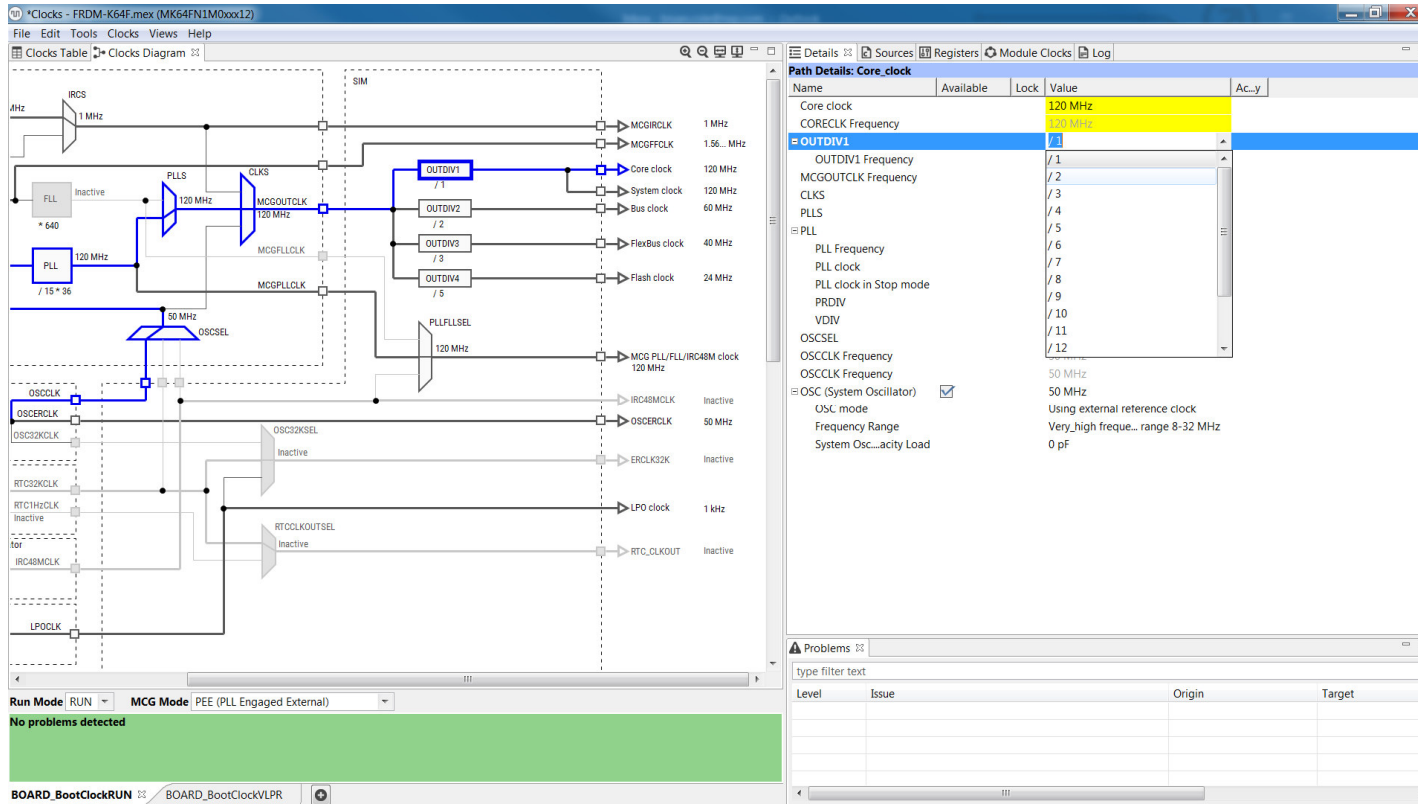
Name	Available	Value	Ac_y
OSC (System Oscillator)	<input checked="" type="checkbox"/>	50 MHz	
OSC mode	<input checked="" type="checkbox"/>	Using external reference clock	
Frequency Range		Very_high frequ... range 8-32 MHz	
System Osc. Capacity Load		0 pF	
OSCERCLK Frequency		50 MHz	
OSCERCLK output		Enabled	
OSCERCLK out_n Stop mode		Disabled	
OSCCLK Frequency		50 MHz	
OSC32CLK Frequency		Inactive	

Clocks Diagram: Set a Clock Divider

- Click once on a divider for a drop-down of available divide values
- Select divide value from the list and the clock output frequency automatically updates



Details View



- Elements can be modified in the Details View

Enable/Disable A Clock Source

- Clock sources such as the Slow/Fast IRCLK and OSCERCLK have clock gates that can be enabled/disabled
- Select the component containing the clock (e.g. MCG for MCGIRCLK)
- Disable the MCGIRLCK in the Details View

Select component

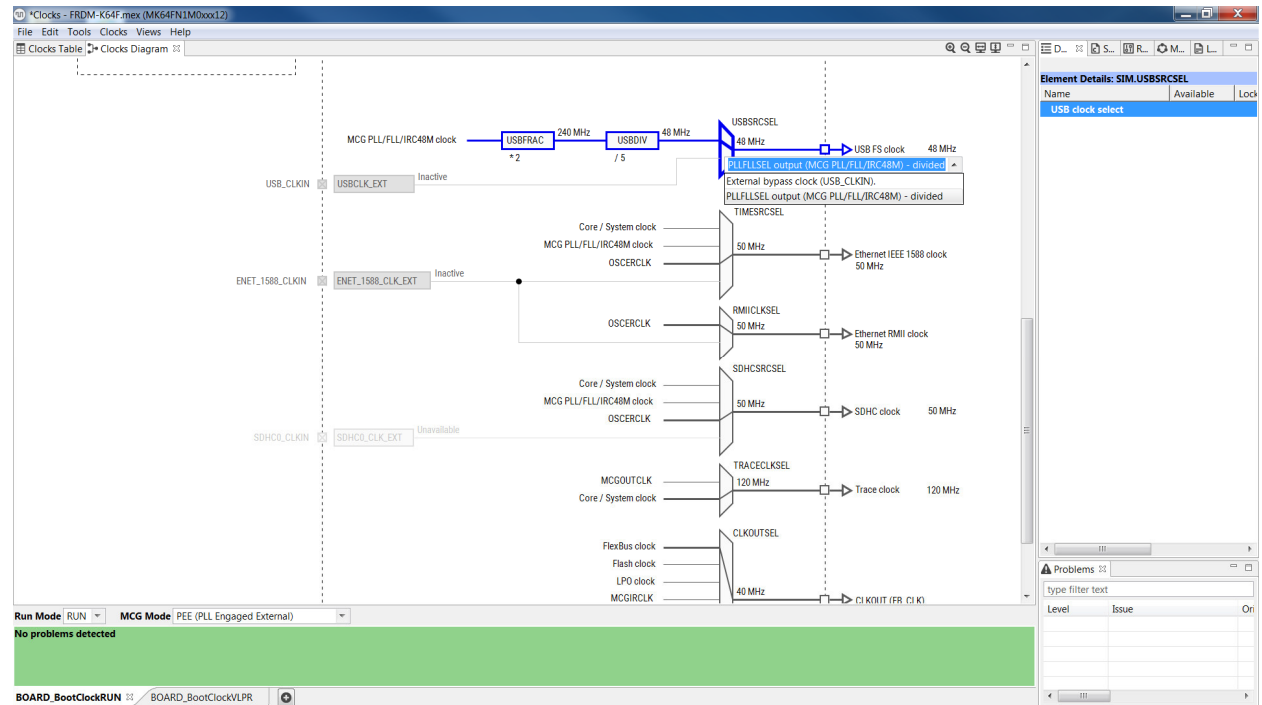
Component Details: MCG

Name	Available	Lock	Value	Ac..y
IRCS			Fast internal reference clock	
OSCSEL			System Oscillator	
FRDIV			/ 32	
FRDIV Frequency			1.56... MHz	
Frequency Range			Very high frequen..V range 32-1536	
IREFS			External reference clock	
FLL			Inactive	
FLL Frequency				
FLL Factor			* 640	
PLL			120 MHz	
PLL Frequency				
PLL clock			Disabled	
PLL clock in Stop mode			Disabled	
PRDIV			/ 15	
VDIV			* 36	
PLLS			PLL output	
CLKS			Output of PLLS (FLL or PLL clock)	
MCGUICLK Frequency			100 MHz	
MCGIRCLK Frequency			2 MHz	
MCGIRCLK output			Enabled	
MCGIRCLK_top mode			Enabled	
MCGFFCLK Frequency			Disabled	
Allow MCGFFCLK clock			yes	
MCGFLLCLK Frequency			100 MHz	
MCGPLLCLK Frequency			100 MHz	

Enable/Disable Clock

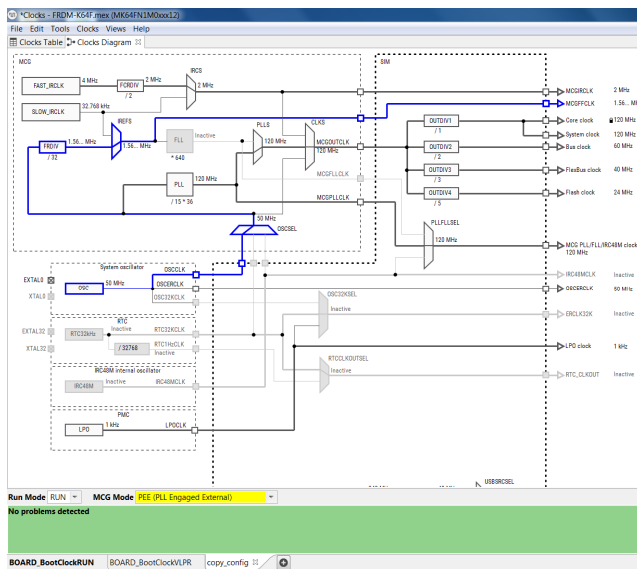
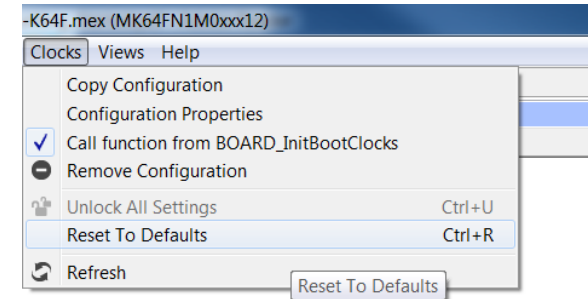
Peripheral Clocks in SIM

- Peripheral clock selections are often controlled through the SIM
- The multiplexers in the SIM component can be used to change the clock source for a peripheral
- The clock source must be enabled to change the mux

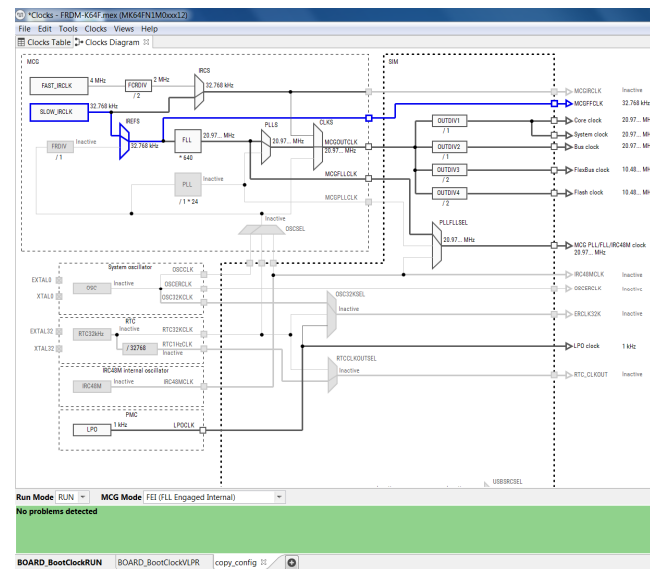


Reset To Defaults

- Reset to Defaults
 - Resets clock configuration to the default reset clock configuration for the processor
 - Not the same as Board_BootClock configuration



- PEE at 120 MHz

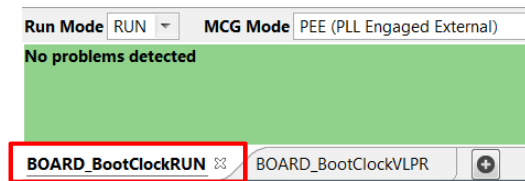


- FEI at 21 MHz (reset)

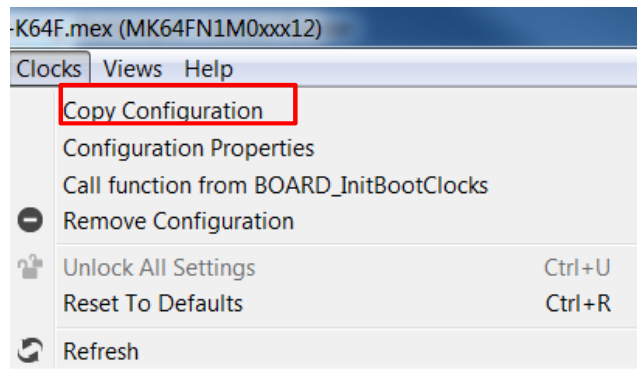
Copy Clock Configuration

- To Copy an existing clock configuration:

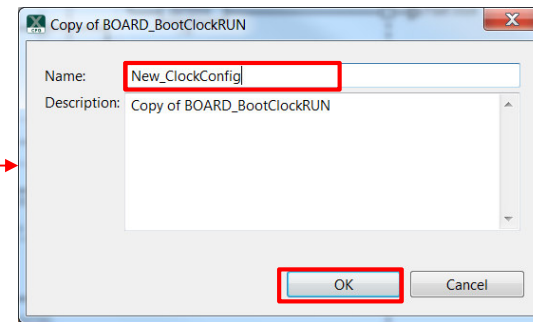
1. Select an existing configuration tab



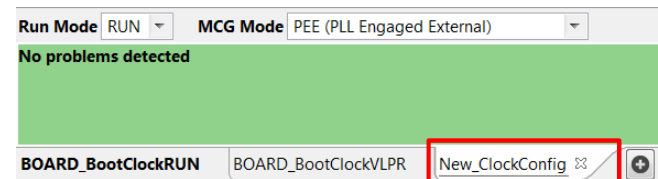
2. Select Clocks > Copy Configuration



3. Name the configuration. Select ok



4. Copied Configuration will be created



Configuration Errors

- Errors may occur when changing the clock configurations
- Error conditions will cause the status bar to become RED
- Potential Problems:
 - **Requirement(s) not satisfiable:** Indicates that there are one or more locked frequency or frequency constraints for which the tool is not able to find a valid settings and satisfy those requirements.
 - **Invalid settings or requirements:** [*element list*] – Indicates that the value of some settings is not valid. For example: The current state of settings is beyond the acceptable range.

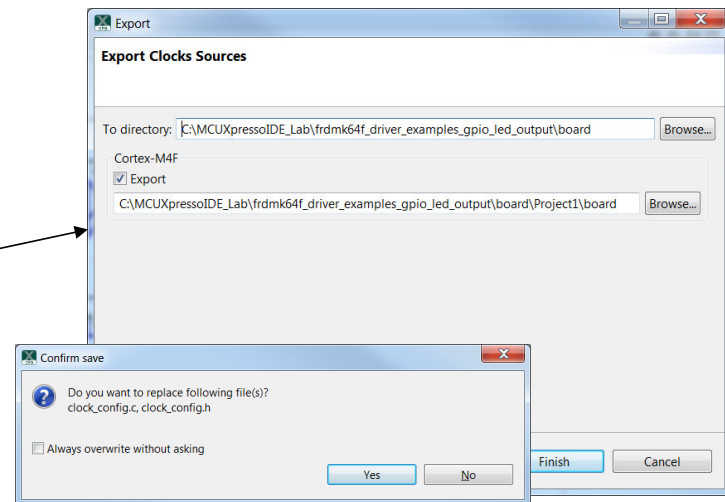
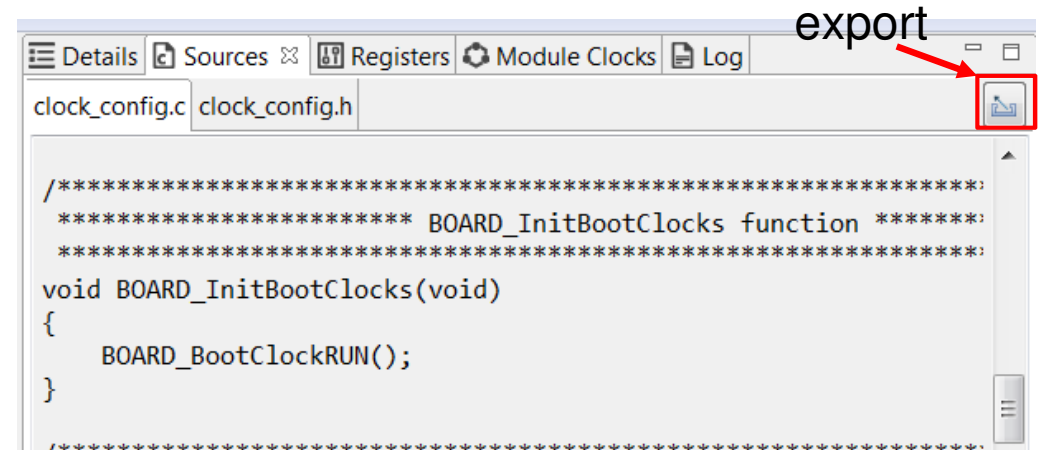
The screenshot shows the TI Clocks configuration tool interface. The main window displays a clock tree diagram with various clock sources and dividers. The 'Problems' window is open, showing several error messages related to the configuration of OUTDIV1.

Level	Issue
Error	Divider must be integer divide of master divider: OUTDIV1
Error	Divider must be integer divide of master divider: OUTDIV1
Error	Divider must be integer divide of master divider: OUTDIV1
Error	Scale value must be in integer divide relation with slave dividers: OUTDIV2, OUTDIV3, OUTDIV4
Warning	There are some erroneous elements on path to the clock output: SIM.OUTDIV1
Warning	There are some erroneous elements on path to the clock output: SIM.OUTDIV3
Warning	There are some erroneous elements on path to the clock output: SIM.OUTDIV2
Warning	There are some erroneous elements on path to the clock output: SIM.OUTDIV3
Warning	There are some erroneous elements on path to the clock output: SIM.OUTDIV1
Warning	There are some erroneous elements on path to the clock output: SIM.OUTDIV4

The status bar at the bottom of the tool displays a red bar with the message: "Requirements are not satisfiable. Consider removing requirements on: OUTDIV1".

Export Clock Configuration

- Export a configuration to clock_config.c and clock_config.h files
- Exports source files, and generates code to initialize current clock configurations
- Access from menu:
 - File->Export
 - Can also be accessed from Export icon in Sources view
- Select the directory to export clock_config.c and clock_config.h.



LAB 3



Lab 2 : To use Config Tools to generate code for pins and clock configuration

- **Pre-requisites**

- Boards
 - OM13092(LPCXpresso54608)
- Software
 - MCUXpresso IDE: <http://nxp.com/mcuxpresso/ide>
 - MCUXpresso Config Tools v3.0 : <http://nxp.com/mcuxpresso/config>
 - SDK_2.2_LPCXpresso54608 (Thumbdrive)
 - Terminal Software (like TeraTerm or PuTTY)
 - mbed Serial Driver: <https://developer.mbed.org/handbook/Windows-serial-configuration>
 - Pin_clk config code file (Thumbdrive)
- Follow Lab 3 instruction

Outline

- Create a new configuration based on hello_world example to be use in hot_pin&clock config project.
- Modify pins and generate the code to pin_mux.c and pin_mux.h files
- Generate the clock code to clock_config.c and clock_config.h
- Export pin and clock sources to workspace by dragging the files to Board directory in the pin&clock config project
- Initiate pins and clocks in hot_pin&clock_config.c by adding “BOARD_InitPins(); and BOARD_BootClockFROHF48M()”;
- Build,debug and run the project.
- Result in Tera Term : Success in Pin Config and Success in Clock Config!

AGENDA

- **MCUXpresso Software And Tools Overview**
- **MCUXpresso SDK**
 - Web Builder
 - File Structure
- **MCUXpresso IDE**
 - Importing/Building
 - Debugging
- **MCUXpresso Config Tool**
 - Project Cloner
 - Pins Tool
 - Clocks Tool
- **LPC54608 LCD Lab, Key API and EmWin Demo**

LPC54608



LPC546XX MCU FAMILY

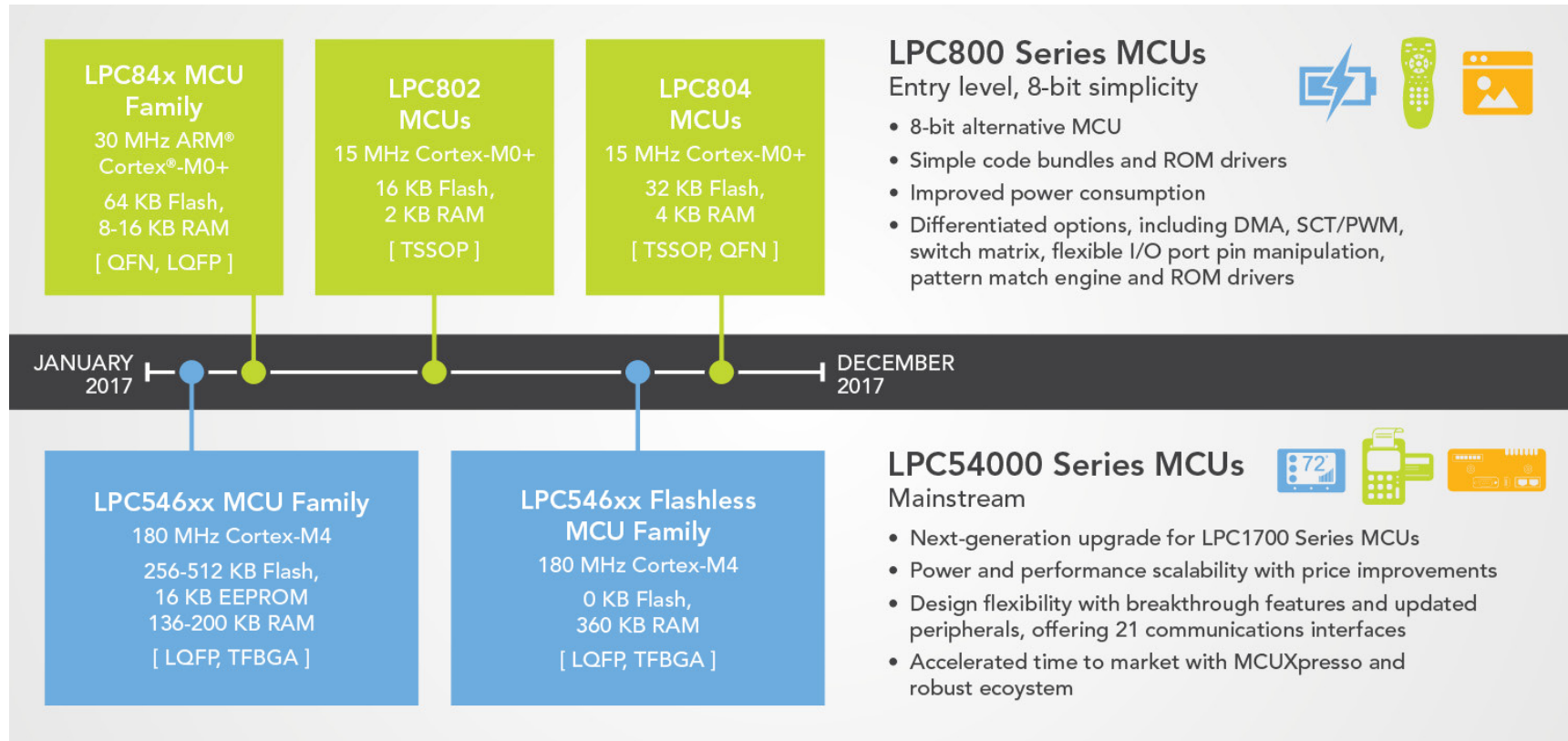
SCALABLE AND POWER-EFFICIENT MULTI-MARKET MCUS

HMI & FLEXIBLE COMMUNICATION INTERFACES FOR IOT APPLICATIONS



SECURE CONNECTIONS
FOR A SMARTER WORLD

2017 LPC Roadmap



Introducing LPC54000 Series of MCU

Mainstream, Power Efficient Microcontrollers

LPC5410x

Baseline Cortex-M4

Cortex-M4F at 100 MHz
1.62 V to 3.6 V
256-512 KB Flash
104 KB RAM

Differentiating Features:

- Optional Dual Core (Cortex-M0+)
- <100uA / MHz (Cortex-M4)
- Digital Mic Subsystem

Available Now

LQFP64
CSP49

LPC5411x

FS USB Large Internal SRAM

Cortex-M4F at 100 MHz
1.62 V to 3.6 V
128-256 KB Flash
96-192 KB RAM
FRO, FS USB

Differentiating Features:

- Optional Dual Core (Cortex-M0+)
- <80uA / MHz (Cortex-M4)
- Flexible Comm Interface
- Digital Mic Subsystem

Available Now

LQFP64
CSP49

LPC546xx

Performance & Integration

Cortex-M4F at 180 MHz
1.71 V to 3.6 V
256-512 KB Flash
136-200 KB RAM
FRO, FS/HS USB

Differentiating Features:

- 120uA / MHz (Cortex-M4)
- Flexible Comm Interfaces
- TFT-LCD Controller
- External Memory Interface
- Ethernet PTP IEE1588 v2
- Dual CAN2.0 / CAN-FD
- Digital Mic Subsystem

Available Now

LQFP208, TFBGA180 (NOW)
LQFP100, TFBGA100 (MAY)



LPC546xx Family Introduction

Power-efficiency, Advanced HMI & Flexible Comms for next-generation IoT



✓ Extremely Low Active Current with 180MHz Performance

- ARM Cortex-M4 core running up to 180MHz at 120 μ A / MHz

✓ Advanced HMI & Flexible Communication Peripherals

- Up to 21 flexible communication peripherals to interface with memory, connectivity modules, and a variety of sensors
- Numerous wake-up sources, ample timers
- Integrated TFT control allows to keep the overall cost and complexity to a minimum

✓ Comprehensive Enablement

- Complimentary MCUXpresso IDE and Software Development Kit (SDK)
- Integration of Segger's emWIN Graphics Library into SDK
- Faster time to market with comprehensive development hardware and reference designs

LPC546xx Target Applications

Industrial, Building, Energy, General Embedded

- Diagnostic equipment
- Industrial control devices
- PLC
- Data Aggregator & Comms Hub
- Building control & automation
- HVAC control
- Multi-protocol bridge
- Data acquisition
- Medical/industrial grade scale
- Scanners / Mini printers



Consumer, Smart Home & Automation

- Small Appliance
- White Goods HMI
- Thermostat
- In Home Display (IHD)
- IOT gateway
- Security monitoring
- High end gaming accessories
- Fitness equipment
- Audio accessories

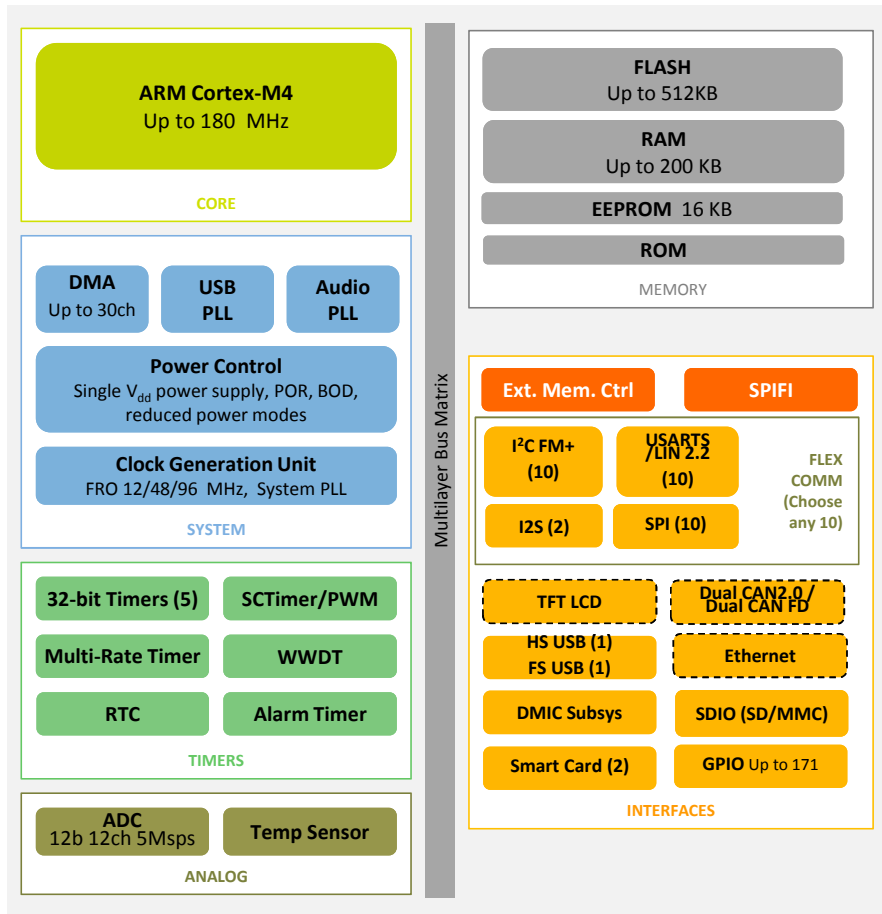


Automotive Aftermarket

- Satellite Radio
- Portable GPS Tracker
- Data aggregator for Infotainment/Navigation
- Fleet Management/Telematics
- Vehicle Diagnostic
- Tachograph
- OBD-II



LPC546xx Series Block Diagram



CPU

- 180MHz Cortex-M4 with floating point unit

Memory

- Up to 512 KB Flash, Up to 200 KB RAM
- 16 KB EEPROM

Interfaces for connectivity & sensors

- Dual CAN2.0 or CAN FD Controller Options
- XTAL-less FS USB (H/D)
- 10 SPI, 10 I2C, 10 USART, 2 I²S channels. Max 10 channels
- Graphic LCD with resolutions up to 1024x768
- 10/100 Ethernet Controller with PTP
- Stereo DMIC subsystem
 - (PDM, decimator, HW VAD)
- 1x HS USB (H/D) w/ on-chip HS PHY
- XIP from QSPI via SPIFI
- External Memory Ctrl (up to 32 bits)

Other

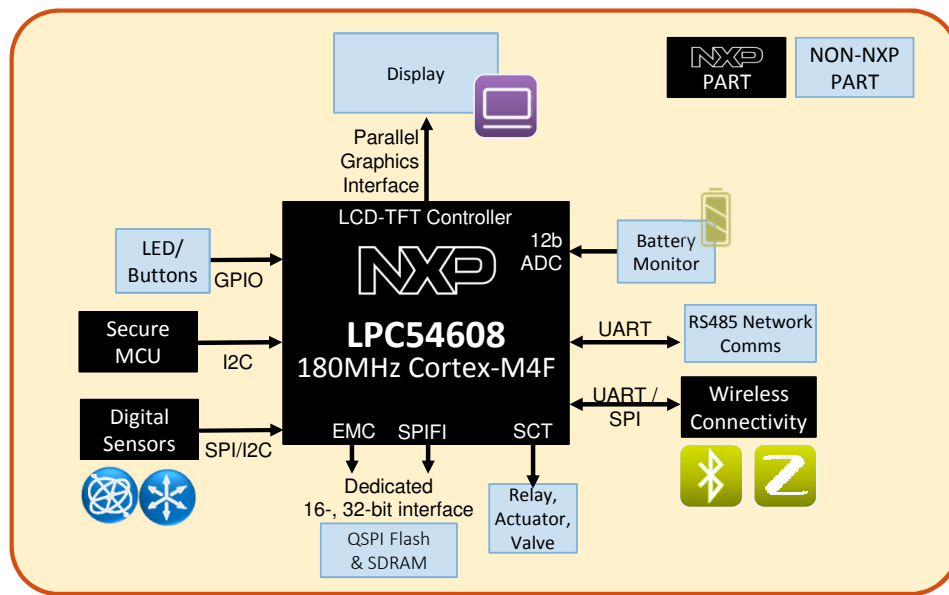
- Operating voltage: 1.71 to 3.6V
- Temperature range: -40 to 105 °C
- LQFP208, LQFP100
- TFBGA180, TFBGA100



Typical Application

Connected, HMI Control Panel/Edge Node in Industrial Applications

LPC546xx Family of MCUs Combine a 180MHz Cortex-M4, for real-time performance, with its unique architecture for outstanding power-efficiency.



Key Features:

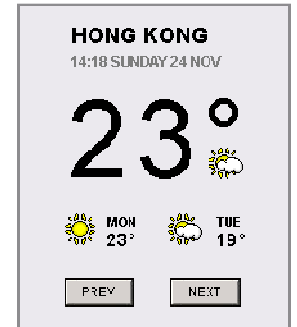
- 30 channel Direct Memory Access (DMA)
- Fast wake-up & mode transitions with 12 MHz Free Running Oscillator (FRO) trimmed to +/- 1% accuracy over voltage & temperature (selectable 48/96 MHz outputs)
- Code Security with Enhanced Code Read Protection (eCRP) and a 128 bit unique device serial number for identification
- Powerful, feature rich 32-bit timers, including State Configurable Timer (SCT/PWM)
- Flexible communication interface with up to 10x USARTS, I2C (supporting FM+) and SPI, along with up to two I2S
- Large availability of GPIOs (up to 171) with fast access (on AHB), DMA support of GPIO ports
- Ethernet with IEEE1588 PTP, Dual CAN supporting CAN-FD and CAN2.0
- FS & HS USB with integrated PHY
- Flexible wake-up & clock sources



LPC's Complete Offering of Graphics Solutions

Segger emWIN Provided Complementary with NXP's MCUXpresso SDK

- Offered as Library + API in C language, compatible with any RTOS (although not required)
- GUI tool builder available
- Source Code from Segger available with a per product license fee
- Free/no royalty required



Provider / Product	Type	Language	GUI Tool Builder	Business model	RTOS Required
TARA / Embedded Wizard	Source code generator	C Javascript	Yes	Developer seats Volume based product line license	Optional (any)
Drapner / TouchGFX	Library + API	C++	Yes	Free developer tools Volume based product line license	Recommended (any)
MicroEJ	Library + API	C/C++ Java	Yes	Part of MicroEJ platform Developer seat licenses Volume based licenses	Yes (MicroEJ)
expresslogic / GUIX	Library + API	C	Yes	Source code per product license	Yes (ThreadX)



Enablement Overview

Runtime Software

NXP Solutions:



MCUXpresso Software and Tools

- IDE
- SDK
- Config Tools

For NXP Cortex-M controllers

- Kinetis MCUs
- LPC Microcontrollers
- i.MX Application Processors





RTOS, Middleware Partners:










Comprehensive frameworks and solutions for low-power, connected, and secure embedded systems

Software Development Tools

IDE / Toolchains:









Industry leading IDE support and intuitive software configuration tools to accelerate application development

Hardware Development Tools

Evaluation Kits:






Partner Solutions





Low cost hardware platforms for evaluation and application development. Partner solutions for hardware debugging solutions

Application Specific

- Graphics
- Cloud Connectivity
- Voice activation
- USB Audio
- Touch HMI
- Camera interface

Connectivity Solutions











Software frameworks and development tools for targeted applications and certified connectivity solutions


Support

Broad Market:

- OOB Walkthroughs
- NXP Community
- Solution Designs
- Application Notes
- Schematics

High Touch:



- Professional Support
- Professional Services

Get started quickly and get the support you need, when you need it



Enablement: LPC546xx Development Board

OM13092

Base Development Board

On-board Display

Available Now

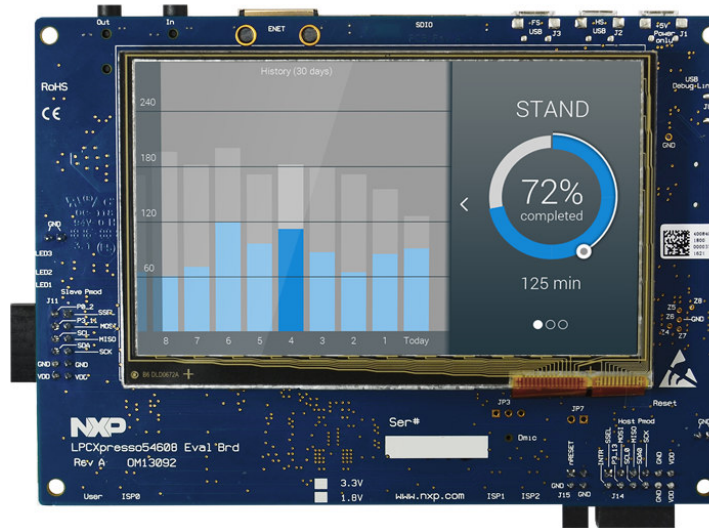
OM13094

CAN-FD Enabled Kit

CAN Physical Transceiver Shield

(no display)

Orderable March-2017

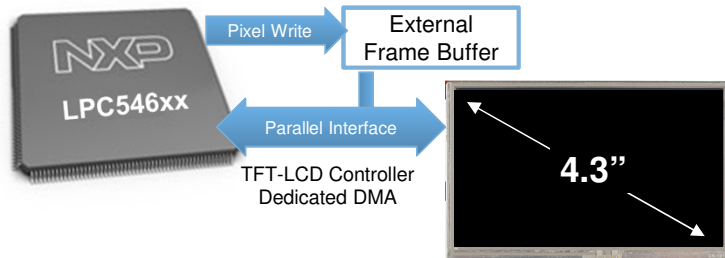


- **LPC54608 in BGA180 package**
 - Cortex-M4F@180MHz
- **Standard LPCXpresso features:**
 - Link2 OBD / external debug
 - Wake, ISP, Reset buttons
 - HS micro USB AB connector
 - FS micro USB AB connector
- **4.3” cap touch display (parallel interface)**
- **2 x PMod expansion connectors**
- **Expansion connectors**
 - Can support Arduino shields such as WiFi modules

Additional (new) on-board features:

- 16MB Micron SDRAM (required for graphics)
- Ethernet (PHY, magnetics & connector)
- DMIC (Knowles Morello)
- I²S connected CODEC with Line In/Out
- SD/MMC card (SDIO)
- Accelerometer on I²C
- 16MB Micron QSPIFI with XIP

Graphics – 24-bit LCD Interface Supports up to XGA



Features and Advantages

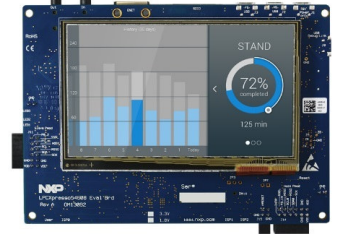
- Up to 1024x768 resolution
- 24-bit LCD interface supports 24bpp (16M colors)
- Palette table allows display of up to 256 of 64K colors
- Dedicated LCD DMA controller
- Hardware cursor support

Target Applications

- Thermostat
- Appliance/White Goods HMI
- Fitness equipment
- Industrial Panel

Enablement and Third Parties

- Free MCUXpresso IDE with SDK, configuration tools
- LPCXpresso54608 Development Board
- LCD App notes and Design recommendation
- Complementary Segger emWIN to develop GUI applications
- Additional GUI solutions from industry leading partners



LAB 4



Lab 4.1 LCD Basic

- **Pre-requisite:** Install the SDK(SDK2.2_LPCXpresso54608) from Thumb drive and import project from file system hot_LCD_1_tft16bpp.
- **Build, Debug and run** hot_LCD_1_tft16bpp.
- **Objective :** Understanding how to
 - Defines LCD parameters and use SDK APIs to initialize LCD controller, start LCD operation
 - Allocate framebuffer in SDRAM w/o having to initialize SDRAM before main()
 - Draw on framebuffer
- **Description :** Initializes LCD controller, SDRAM, and draw on framebuffer
- **Result:** 8 color stripes moving on LCD screen

Key API and codeHOT_LCD_1_tft16bpp

- Initialize SDRAM for framebuffer availability

```
BOARD_InitSDRAM();
```

- Enabled clock to LCD controller

```
CLOCK_SetClkDiv(kCLOCK_DivLcdClk, 1, true);
```

- Initialize LCD controller with specified parameters, including panel clock, resolution, color format, timings, framebuffer address.

```
LCDC_GetDefaultConfig(&lcdConfig);
```

```
lcdInFreq = CLOCK_GetFreq(kCLOCK_LCD);
```

```
LCDC_Init(LCD, &lcdConfig, lcdInFreq);
```

- Start LCD controller and power up LCD

```
LCDC_Start(LCD);
```

```
LCDC_PowerUp(LCD);
```

Observation and changes

- Change the color of stripes by modifying “colTab” array.
- Change panel clock frequency macro “LCD_PANEL_CLK”, suggested range no less than 4MHz.
- Learn the members of “lcdc_config_t”, how they map to LCD controller to registers.
- Check the “Flash.sct” and the definition of “**s_FB**” to see how to make framebuffer placed into SDRAM w/o involving compiler to generate “zero-init” code to framebuffer before main().
- Otherwise, Compiler will generate “zero-init” code to framebuffer before jumping to “main()”; however, w/o having SDRAM initialized, accessing SDRAM will cause hard fault.

Lab 4.2 DUAL FRAMEBUFFER

- **Pre-requisite:** Import project from file system hot_LCD_2_tft16bpp_2fb
- **Build, Debug and run** hot_LCD_2_tft16bpp_2fb.
- **Objective :** Understanding how to
 - Defines 2 framebuffers
 - Using LCD's "base address update" interrupt to safely draw to background FB.
 - Draw on framebuffer
- **Description :** Repeating drawings in main loop: first clear the screen to black, then draw color stripes. Use SysTick timer to limit draw rate.
 - If "SW5" is not pressed, then use one FB to draw,
 - if "SW5" is pressed, then waits for "base address update" IRQ, then draws on backup FB (the previous active FB), after drawing, set the next active FB to this FB.
- **Result:** If "SW5" is not pressed, then black screen and color stripes shows on screen interleaved, get flicker feeling; if "SW5" is pressed, only the rotating color stripes are shown (like HOT1).

Key API and code HOT_LCD_2_tft16bpp_fb

- Enable LCD “base address update” interrupt

```
LCDC_EnableInterrupts(LCD, kLCDC_BaseAddrUpdateInterrupt);
```

- IRQ handler: Get LCD interrupt flag and clear in LCD IRQ handler, set the s/w level notify ---- “s_frameAddrUpdated = true;”

```
void LCD_IRQHandler(void) {...}
```

- intStatus = **LCDC_GetEnabledInterruptsPendingStatus**(LCD);

```
LCDC_ClearInterruptsStatus(LCD, intStatus);
```

```
if (intStatus & kLCDC_BaseAddrUpdateInterrupt) {...}
```

- Update FB address after background FB drawing is done, and switch the active/background FB.

```
LCDC_SetPanelAddr(LCD, kLCDC_UpperPanel, (uint32_t)(pFB32)); s_actFBIdx = !s_actFBIdx;
```

- Background code: Wait for “s_frameAddrUpdated” to become true before drawing next frame.

```
while (!s_frameAddrUpdated){}
```

Observation with changes

- See different drawing effects when “SW5” is pressed and not pressed.
- Enter debug mode , press ”F10” to step over or “F11” to step into to analyze and check how the FBs are switched with “s_actFBIdx” variable.
- Experiments :
 - Change SysTick rate, check if it can resolve the flicker effect w/o dual-FB, and/or affects dual-FB effect.
 - Comment out the “while (!s_frameAddrUpdated){}”, see if it affects dual-FB effect.
 - Switch “stage1” and “stage2” in code, check the differences of LCD display for single FB and dual-FB respectively.

Lab 4.3 PALETTE

- **Pre-requisite:** Import project from file system hot_LCD_3_palette
- **Build, Debug and run** hot_LCD_3_palette

- **Objective :** Understanding how to
 - use palette to put framebuffer in SRAM, instead of SDRAM
 - Palette color settings

- **Description :** Draw moving rectangle periodically. Every period is synchronized to a new LCD base address update IRQ. The examples implements a rectangle draw & fill routine with 2bpp mode.

- **Result:** There is a rectangle moving smoothly and when reach a edge (either left, top, right ,bottom), it changes color and bounces.

Key API and code HOT_LCD_3_palette

- Setup palette colors

```
static const uint32_t palette[] = {0x001F0000U, 0x7C0003E0U};
```

- Set palette buffer

```
LCDC_SetPalette(APP_LCD, palette, ARRAY_SIZE(palette));
```

- Update FB address after background FB drawing is done, and switch the active/background FB.

```
LCDC_SetPanelAddr(LCD, kLCDC_UpperPanel, (uint32_t)(pFB32));
```

```
s_actFBIdx = !s_actFBIdx;
```

Observation with changes

- Locate palette color settings and change color to see the result. Color is RGB565 format.
- Change the moving speed of rectangle, either X or Y.

Lab 4.4 H/W CURSOR

- **Pre-requisite:** Import project from file system hot_LCD_4_cursor
- **Build, Debug and run** hot_LCD_4_cursor
- **Objective** : Understanding how to
 - Understands how to setup cursor bitmap, including transparent and XOR colors
 - Set new position of cursor synchronized with LCD vertical back porch.
- **Description** : Draw and moves cursor periodically. Every period is synchronized to a new LCD vertical back porch IRQ.
- **Result:** There is a cursor moving smoothly and when reach a edge (either left, top, right ,bottom), it bounces.

Key API and code HOT_LCD_4_cursor

- Defines the bitmap (w/ transparency and XOR “colors”) of cursor

```
static const uint8_t cursor32Img0[]
```

- Configure cursor

```
lcdc_config_t lcdConfig;  
LCDC_CursorGetDefaultConfig(&cursorConfig);  
cursorConfig.size = kLCDC_CursorSize32;  
cursorConfig.syncMode = kLCDC_CursorSync;  
cursorConfig.image[0] = (uint32_t *)cursor32Img0;
```

- Select cursor image number (0 to 3). LCDC supports 64x64, divided into 4 32x32 images like a “田”. As we just setup one left-top 32x32, the number is 0.

```
LCDC_ChooseCursor(APP_LCD, 0);
```

- Cursor update is synchronized to vertical back porch, so enabled the “vertical compare” IRQ and select vertical back porch as IRQ trigger source.

```
LCDC_SetVerticalInterruptMode(APP_LCD, kLCDC_StartOfBackPorch);  
LCDC_EnableInterrupts(APP_LCD, kLCDC_VericalCompareInterrupt);  
NVIC_EnableIRQ(APP_LCD_IRQn);
```

- Enable H/W cursor layer

```
LCDC_EnableCursor(APP_LCD, true);
```

- Update cursor location after a new vertical back porch IRQ fired.

```
LCDC_SetCursorPosition(APP_LCD, cursorPosX, cursorPosY);
```

Observation with changes

- cursor position update synchronized to vertical back porch, to verify if this is required,
- comment out the “while (!s_frameEndFlag){}” and uncomment “while (!s_isNewTick){}” to see the change of cursor movement (Which one is more smoother?).

EMWIN DEMO



Emwin

- **Pre-requisite:** Import project from file system Emwin_code
- **Build, Debug and run** Emwin_2_demo
- **Objective :** Segger's EmWin provides a complimentary way to develop your next GUI application



<http://www.nxp.com/pages/emwin-graphics-library:EMWIN-Graphics-LIBRARY>



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