PF9455

Highly optimized PMIC for functionally safe and quality managed i.MX9 MPU-based applications

Rev. 1.0 — 19 November 2024 Product brief

1 Introduction

This product brief is intended to provide overview/summary information for the purpose of evaluating a product for design suitability. It is intended for quick reference only and should not be relied upon to contain detailed and full information.

Some of the content in this product brief is extracted from the product's full data sheet. In case of any inconsistency or conflict, the full data sheet shall prevail.

For detailed and full information, see the relevant PF9455 full data sheet, available via the NXP Secure Files content interface.

2 General description

The PF9455 is a power management integrated circuit (PMIC) optimized for high-performance i.MX9x based applications. It Integrates multiple high-efficiency switch mode and linear voltage regulators to support base system power from a pre-regulated system rail (3.3 V to 5.0 V). It provides low quiescent current in Standby and Low-power Off modes.

A built-in multiple time programmable configuration stores key startup configurations, drastically reducing the number of external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I^2C communication after startup, offering flexibility for various system states.

The PF9455 complies with the IEC61508 industrial safety specification targeting high safety integrity levels up to SIL 2.

3 Features and benefits

- Up To five buck regulators with internal power stage and programmable current limit
- Three low-dropout linear regulators with load switch operation
- Ultra-low power always-on LDO supply
- Two external voltage monitoring inputs
- Programmable I/O interfacing pins
- Advanced frequency management with frequency spread spectrum
- Multi-channel analog multiplexer for system voltage monitoring
- High-speed I^2C interface with up to 3.4 MHz operation
- Advanced thermal monitoring and thermal shutdown protection
- Functional safety architecture to target industrial applications up to SIL 2
- Multiple time programmable configuration (MTP)
- 56-pin QFN package with exposed pad
- Operating ambient temperature from -40 °C to 105 °C, junction temperate from -40 °C to 150 °C

4 Applications

- High-end consumer and industrial
- Human machine interfaces
- Connectivity domain controller
- Telematics

5 Ordering information

Table 1. Ordering information

Type number[1]	Package		
	Name	Description	Version
PF9455	HVQFN56	HVQFN56, plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, 56 terminals, 0.5 mm pitch, 8 mm x 8 mm x 0.53 mm body	SOT684-32(DD)

[1] To order parts in tape and reel, add the R2 suffix to the part number.

Table 2. Ordering options

Part number[1][2]	Target market	NXP processor	System comments	Safety grade	OTP ID
PPF9455AVMA7ES	Industrial	i.MX 943	LPDDR5 memory	QM	MA7
PPF9455AVMA8ES	Industrial	i.MX 943	LPDDR4 memory	QM	MA8
PPF9455AVSA3ES	Industrial	i.MX 943	LPDDR5 memory	SIL 2	SA3
PPF9455AVSA4ES	Industrial	i.MX 943	LPDDR4 memory	SIL 2	SA4

[1] P = engineering sample part number
[2] M = production part number

6 Functional block diagram

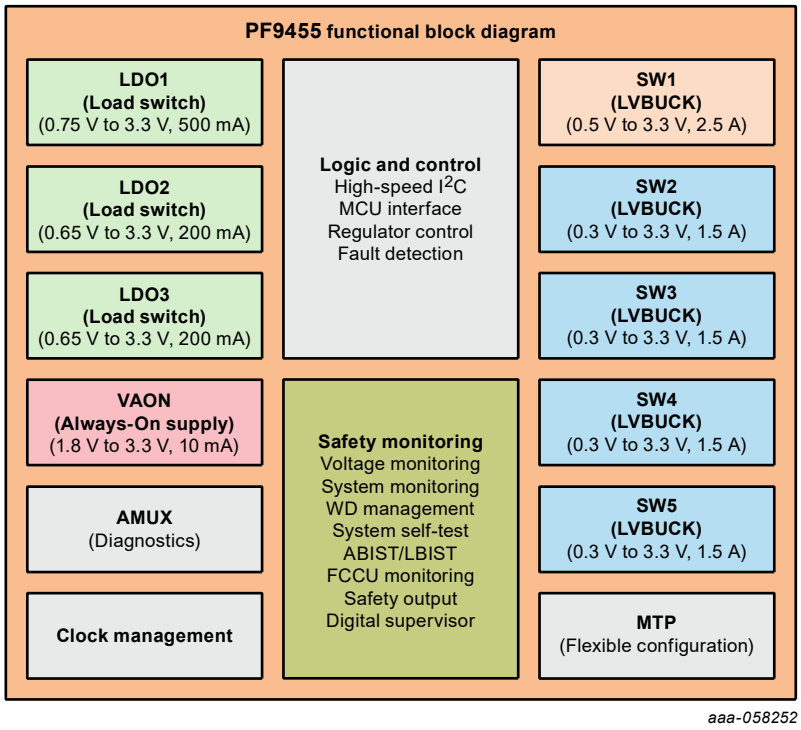

Figure 1. Functional block diagram

7 Package pinout

The PF9455 is offered in a 56-pin, 8x8 mm^2 body size QFN with exposed pad and wettable flanks.

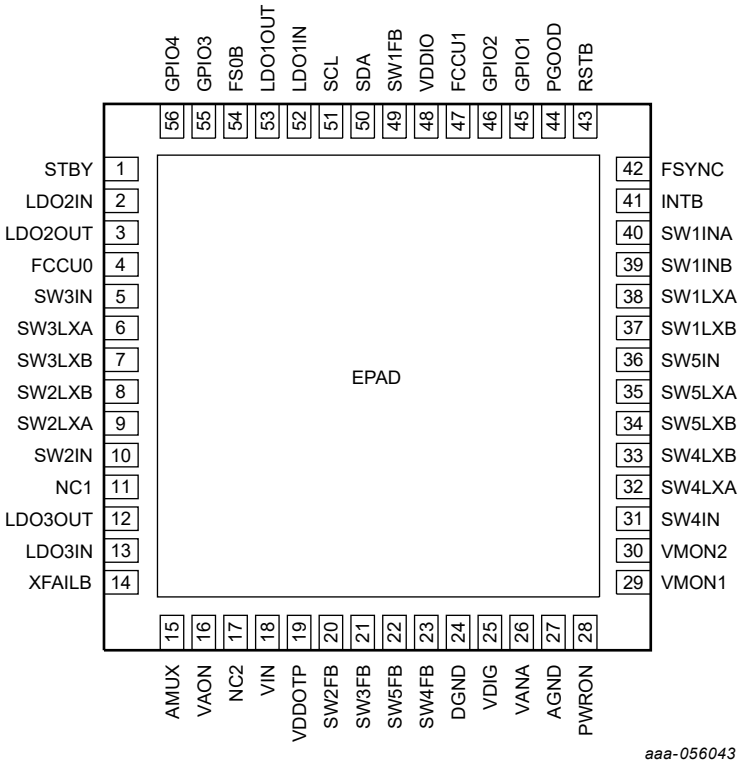

Figure 2. PF9455 package pinout (top view)

7.1 Pin description

Table 3. QFN56 pin description

Pin	Pin Name	Description	Min	Max	Units
1	STBY	Standby request	-0.3	6.0	V
2	LDO2IN	LDO2 input	-0.3	6.0	V
3	LDO2OUT	LDO2 Output	-0.3	6.0	V
4	FCCU0	FCCU fault monitoring input 0	-0.3	6.0	V
5	SW3IN	SW3 Input	-0.3	6.0	V
6	SW3LXA	SW3 switching node A	-0.3	6.0	V
7	SW3LXB	SW3 switching node B	-0.3	6.0	V
8	SW2LXB	SW2 switching node B	-0.3	6.0	V
9	SW2LXA	SW2 switching node A	-0.3	6.0	V
10	SW2IN	SW2 input	-0.3	6.0	V
11	NC1	Not connected	-0.3	6.0	V
12	LDO3OUT	LDO3 output	-0.3	6.0	V

Table 3. QFN56 pin description*...continued*

Pin	Pin Name	Description	Min	Max	Units
13	LDO3IN	LDO3 input	-0.3	6.0	V
14	XFAILB	External fail	-0.3	6.0	V
15	AMUX	Analog multiplexer output	-0.3	6.0	V
16	VAON	Always-on output	-0.3	6.0	V
17	NC2	Not connected	-0.3	6.0	V
18	VIN	PMIC input supply	-0.3	6.0	V
19	VDDOTP	OTP supply	-0.3	10.0	V
20	SW2FB	SW2 feedback	-0.3	6.0	V
21	SW3FB	SW3 feedback	-0.3	6.0	V
22	SW5FB	SW5 feedback	-0.3	6.0	V
23	SW4FB	SW4 feedback	-0.3	6.0	V
24	DGND	Digital ground	-0.3	0.3	V
25	VDIG	Internal digital supply	-0.3	2.0	V
26	VANA	Internal analog supply	-0.3	2.0	V
27	AGND	Analog ground	-0.3	0.3	V
28	PWRON	Power-on request	-0.3	6.0	V
29	VMON1	External VMON1	-0.3	6.0	V
30	VMON2	External VMON2	-0.3	6.0	V
31	SW4IN	SW4 input	-0.3	6.0	V
32	SW4LXA	SW4 switching node A	-0.3	6.0	V
33	SW4LXB	SW4 switching node B	-0.3	6.0	V
34	SW5LXB	SW5 switching node B	-0.3	6.0	V
35	SW5LXA	SW5 switching node A	-0.3	6.0	V
36	SW5IN	SW5 input	-0.3	6.0	V
37	SW1LXB	SW1 switching node B	-0.3	6.0	V
38	SW1LXA	SW1 switching node A	-0.3	6.0	V
39	SW1INB	SW1 input B	-0.3	6.0	V
40	SW1INA	SW1 input A	-0.3	6.0	V
41	INTB	Interrupt request	-0.3	6.0	V
42	FSYNC	Clock sync input	-0.3	6.0	V
43	RSTB	MCU reset pin	-0.3	6.0	V
44	PGOOD	Power good	-0.3	6.0	V
45	GPIO1	Programmable IO1	-0.3	6.0	V
46	GPIO2	Programmable IO2	-0.3	6.0	V
47	FCCU1	XRESET / FCCU fault monitoring input 1	-0.3	6.0	V
48	VDDIO	I/O supply input	-0.3	6.0	V

Table 3. QFN56 pin description*...continued*

Pin	Pin Name	Description	Min	Max	Units
49	SW1FB	SW1 feedback	-0.3	6.0	V
50	SDA	I^2C data	-0.3	6.0	V
51	SCL	I^2C clock	-0.3	6.0	V
52	LDO1IN	LDO1 input	-0.3	6.0	V
53	LDO1OUT	LDO1 output	-0.3	6.0	V
54	FS0B	Fail-safe output	-0.3	6.0	V
55	GPIO3	Programmable IO3	-0.3	6.0	V
56	GPIO4	Programmable IO4	-0.3	6.0	V
57	EPAD	Exposed-pad ground	-0.3	0.3	V

8 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Description	Min	Typ	Max	Unit
VIN	Main input supply voltage	-0.3		6	V
SWxIN	Switching regulator input supply voltage	-0.3		6	V
LDOxIN	LDO regulator input supply voltage	-0.3		6	V
VDDIO	IO input supply voltage	-0.3		6	V
VDDOTP	OTP programming input supply voltage	-0.3		10	V

9 Revision history

Table 5.

Revision	Date	Description of changes
1.0	19 November 2024	Initial preliminary release

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