BMI7018_PB

Product brief for 18-cell battery-cell controller IC

Rev. 1 — 12 August 2024 Product brief

1 General description

The BMI7018 is a lithium-ion battery-cell controller IC designed for industrial applications, such as energy storage systems (ESS) and uninterruptible power supply (UPS) systems.

The BMI7018 offers transport protocol link (TPL3 - proprietary isolated daisy chain protocol of NXP) and serial peripheral interface (SPI) for communication with the host MCU.

These devices support high-precision cell voltage and temperature measurements, along with various cell-voltage balancing strategies. Aside from a SPI interface to enable direct communication with the host MCU, they alternatively provide a daisy-chain communication interface (TPL), which supports capacitive and inductive isolation between nodes.

2 Features and benefits

- Ambient temperature range: –20 °C to 60 °C
- Support for cell voltage and cell temperature measurements from the host microcontroller unit (MCU)
- Cell voltage measurement
  - 4 to 18 cells per device
  - Operating voltage range from 9 V to 90 V
  - Supports bus bars voltage measurement with –3 V to +5 V input voltage
  - 16-bit resolution and up to ±0.8 mV typical measurement accuracy with ultra low long-term drift
  - Integrated configurable digital filter
- External temperature and auxiliary voltage measurements
  - One analog input for absolute measurement, 5 V input range
  - Eight analog inputs configurable as absolute or ratiometric, 5 V input range
  - 16-bit resolution and ±5 mV typical measurement accuracy
  - Integrated configurable digital filter
- Internal measurement
  - Two redundant internal temperature sensors
  - Supply voltages
  - External transistor current
- Cell voltage balancing
  - 18 internal balancing field effect transistors (FET), up to 360 mA peak with 0.5 Ω R_{DSon} per channel (typ.)
  - Support for simultaneous passive balancing of all channels with automatic odd/even sequence
  - Global balancing timeout timer
  - Timer controlled balancing with individual timers with 10 s resolution and up to 45 h duration
  - Voltage controlled balancing with global and individual undervoltage thresholds
  - Temperature controlled balancing; if balancing resistors or the IC are in overtemperature, balancing is interrupted
  - Configurable pulse width modulation (PWM) duty cycle balancing
  - Automatic pause of balancing during measurement with configurable filter settling time
  - Configurable delay of the start of balancing after transition to sleep
  - Automatic discharge of the battery pack (emergency discharge)
  - Constant current cell balancing to compensate the balancing current variation because of cell voltage variation
- I^2C-bus master interface to control external devices, for example, EEPROMs and security ICs
- Configurable alarm output
- Cyclic wake-up to monitor the pack and the balancing function during sleep
- Capability to wake up the host MCU via daisy chain in case of a fault event
- Host interface supporting SPI or isolated daisy chain communication (TPL3)
  - 2 Mbit/s data rate for TPL interface
  - 4 Mbit/s data rate for SPI interface
- TPL3 daisy chain communication supports
  - Two-wire daisy chain with capacitive or inductive isolation
  - Protocol supporting up to six daisy chains and 62 nodes per chain
- Unique device ID with dynamic addressing
- Operation modes
  - Active mode FP (12 mA typ.)
  - Sleep mode LP (60 µA typ.)
  - Deep sleep mode ULP (15 µA typ.)

3 Applications

3.1 Industrial

- Energy storage systems (ESS)
- Uninterruptible power supply (UPS)

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
MBMI7018	LQFP64	Plastic, thermal enhanced low profile quad flat package; 64 terminals; 0.50 mm pitch; 10 x 10 x 1.4 mm body	SOT1510-2

4.1 Ordering options

Table 2. Part numbers

Type number	Description
MBMI7018TA1AE	Premium version - TPL interface
MBMI7018SA1AE	Premium version - SPI interface

5 Block diagram

Figure 1 shows the general architecture of the BMI7018.

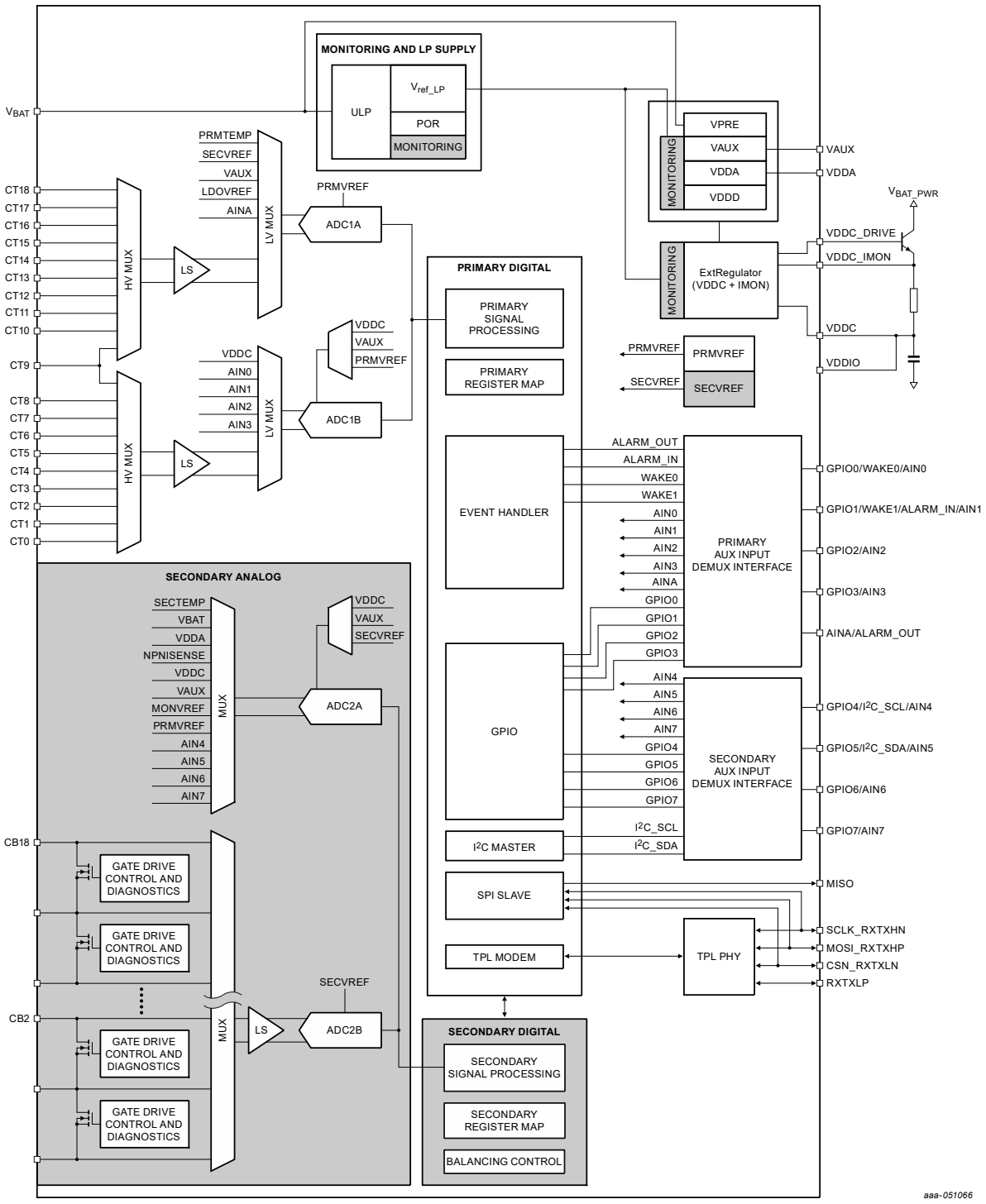

Figure 1. Simplified internal block diagram

6 Pinning information

6.1 Pinout diagram

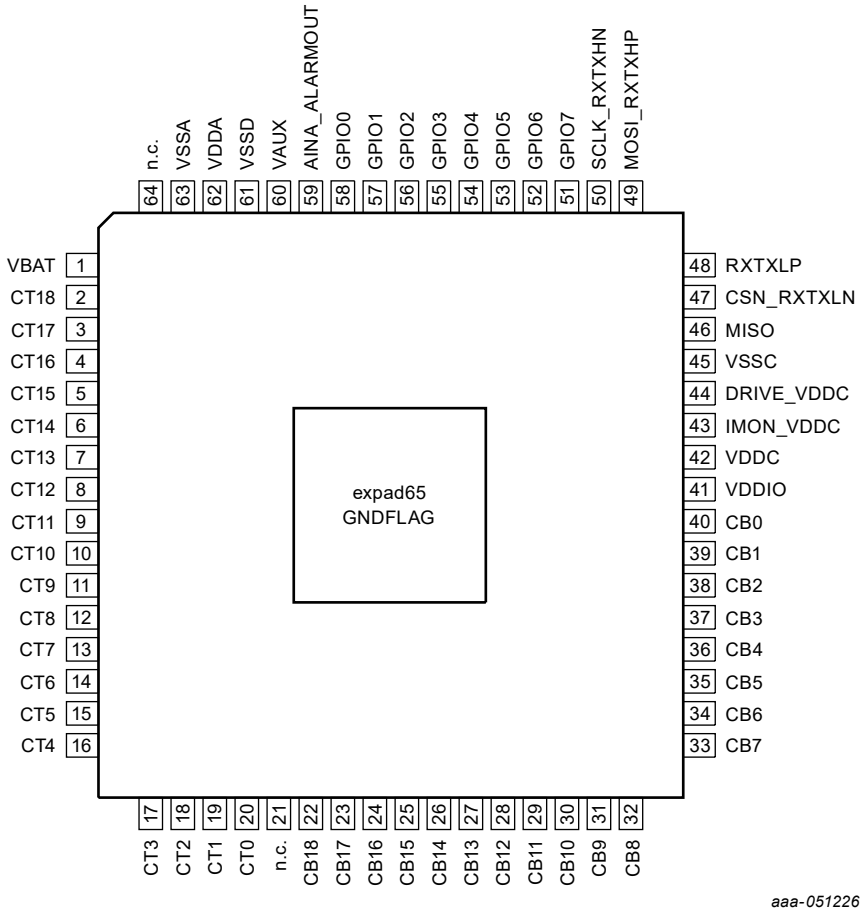

Figure 2. Pinout

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VBAT	1	Supply input of the product
CT18	2	Cell terminal 18 input
CT17	3	Cell terminal 17 input
CT16	4	Cell terminal 16 input
CT15	5	Cell terminal 15 input
CT14	6	Cell terminal 14 input
CT13	7	Cell terminal 13 input
CT12	8	Cell terminal 12 input
CT11	9	Cell terminal 11 input
CT10	10	Cell terminal 10 input

Table 3. Pin description...*continued*

Symbol	Pin	Description
CT9	11	Cell terminal 9 input
CT8	12	Cell terminal 8 input
CT7	13	Cell terminal 7 input
CT6	14	Cell terminal 6 input
CT5	15	Cell terminal 5 input
CT4	16	Cell terminal 4 input
CT3	17	Cell terminal 3 input
CT2	18	Cell terminal 2 input
CT1	19	Cell terminal 1 input
CT0	20	Cell terminal 0 input
n.c.	21	Not connected
CB18	22	1. Secondary cell terminal 18 input 2. High input for cell 17 balancing
CB17	23	1. Secondary cell terminal 17 input 2. Low input for cell 17 balancing 3. High input for cell 16 balancing
CB16	24	1. Secondary cell terminal 16 input 2. Low input for cell 16 balancing 3. High input for cell 15 balancing
CB15	25	1. Secondary cell terminal 15 input 2. Low input for cell 15 balancing 3. High input for cell 14 balancing
CB14	26	1. Secondary cell terminal 14 input 2. Low input for cell 14 balancing 3. High input for cell 13 balancing
CB13	27	1. Secondary cell terminal 13 input 2. Low input for cell 13 balancing 3. High input for cell 12 balancing
CB12	28	1. Secondary cell terminal 12 input 2. Low input for cell 12 balancing 3. High input for cell 11 balancing
CB11	29	1. Secondary cell terminal 11 input 2. Low input for cell 11 balancing 3. High input for cell 10 balancing
CB10	30	1. Secondary cell terminal 10 input 2. Low input for cell 10 balancing 3. High input for cell 9 balancing
CB9	31	1. Secondary cell terminal 9 input 2. Low input for cell 9 balancing 3. High input for cell 8 balancing
CB8	32	1. Secondary cell terminal 8 input 2. Low input for cell 8 balancing 3. High input for cell 7 balancing
CB7	33	1. Secondary cell terminal 7 input 2. Low input for cell 7 balancing 3. High input for cell 6 balancing

Table 3. Pin description...*continued*

Symbol	Pin	Description
CB6	34	1. Secondary cell terminal 6 input 2. Low input for cell 6 balancing 3. High input for cell 5 balancing
CB5	35	1. Secondary cell terminal 5 input 2. Low input for cell 5 balancing 3. High input for cell 4 balancing
CB4	36	1. Secondary cell terminal 4 input 2. Low input for cell 4 balancing 3. High input for cell 3 balancing
CB3	37	1. Secondary cell terminal 3 input 2. Low input for cell 3 balancing 3. High input for cell 2 balancing
CB2	38	1. Secondary cell terminal 2 input 2. Low input for cell 2 balancing 3. High input for cell 1 balancing
CB1	39	1. Secondary cell terminal 1 input 2. Low input for cell 1 balancing 3. High input for cell 0 balancing
CB0	40	1. Secondary cell terminal 0 input 2. Low input for cell 0 balancing
VDDIO	41	External VDDIO supply input.
VDDC	42	External VDDC supply input.
IMON_VDDC	43	External NPN monitoring input.
DRIVE_VDDC	44	External NPN base output.
VSSC	45	VDDIO and VDDC ground reference.
MISO	46	SPI slave data output to master.
CSN_RXTXLN	47	1. SPI chip select input from master 2. TPLRX negative input from lower node 3. TPLTX negative output to lower node
RXTXLP	48	1. TPLRX positive input from lower node 2. TPLTX positive output to lower node
MOSI_RXTXHP	49	1. SPI slave data input from master 2. TPLRX positive input from upper node 3. TPLTX positive output to upper node
SCLK_RXTXHN	50	1. SPI clock input from master 2. TPLRX negative input from upper node 3. TPLTX negative output to upper node
GPIO7	51	1. Analog input AIN7 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN7 for absolute measurement 3. General-purpose input 7 4. General-purpose output 7
GPIO6	52	1. Analog input AIN6 for ratiometric measurement to VAUX / VDDC 2. Analog input AIN6 for absolute measurement 3. General-purpose input 6 4. General-purpose output 6

Table 3. Pin description...*continued*

Symbol	Pin	Description
GPIO5	53	1. Analog input AIN5 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN5 for absolute measurement 3. General-purpose input 5 4. General-purpose output 5 5. I2CSDA
GPIO4	54	1. Analog input AIN4 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN4 for absolute measurement 3. General-purpose input 4 4. General-purpose output 4 5. I2CSCL
GPIO3	55	1. Analog input AIN3 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN3 for absolute measurement 3. General-purpose input 3 4. General-purpose output 3
GPIO2	56	1. Analog input AIN2 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN2 for absolute measurement 3. General-purpose input 2 4. General-purpose output 2
GPIO1	57	1. Analog input AIN1 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN1 for absolute measurement 3. General-purpose input 1 4. General-purpose output 1 5. Wake-up input 1 6. Alarm input
GPIO0	58	1. Analog input AIN0 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN0 for absolute measurement 3. General-purpose input 0 4. General-purpose output 0 5. Wake-up input 0
AINA_ALARMOUT	59	1. Analog input AINA for absolute measurement 2. Alarm output
VAUX	60	Supply output for external sensors.
VSSD	61	Digital ground.
VDDA	62	Internal analog supply. Should be connected to a 100 nF capacitor. Should not be used for application.
VSSA	63	Analog ground.
n.c.	64	Not connected.
GNDFLAG	Expad 65	Grounded exposed pad.

7 Revision history

Revision history

Revision	Date	Description
BMI7018_PB v.1	12 August 2024	Initial version

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