SOT619-25(D)

plastic thermal enhanced very thin quad flat package; no leads; 0.1 dimple wettable flank, 48 terminals; 7 mm x 7 mm x 0.9 mm body

30 March 2018 **Package information**

1. Package summary

Terminal position code	Q (quad)
Package type descriptive code	HVQFN48
Package style descriptive code	HVQFN (thermal enhanced very thin quad flatpack; no leads)
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Issue date	28-2-2018
Manufacturer package code	98ASA01192D

Table 1. Package summary

Symbol	Parameter		Min	Typ	Nom	Max	Unit
D	package length		-	-	7	-	mm
E	package width		-	-	7	-	mm
A_2	package height		-	-	0.9	-	mm
e	nominal pitch		-	-	0.5	-	mm
n_2	actual quantity of termination		-	-	48	-	A/A

2. Package outline

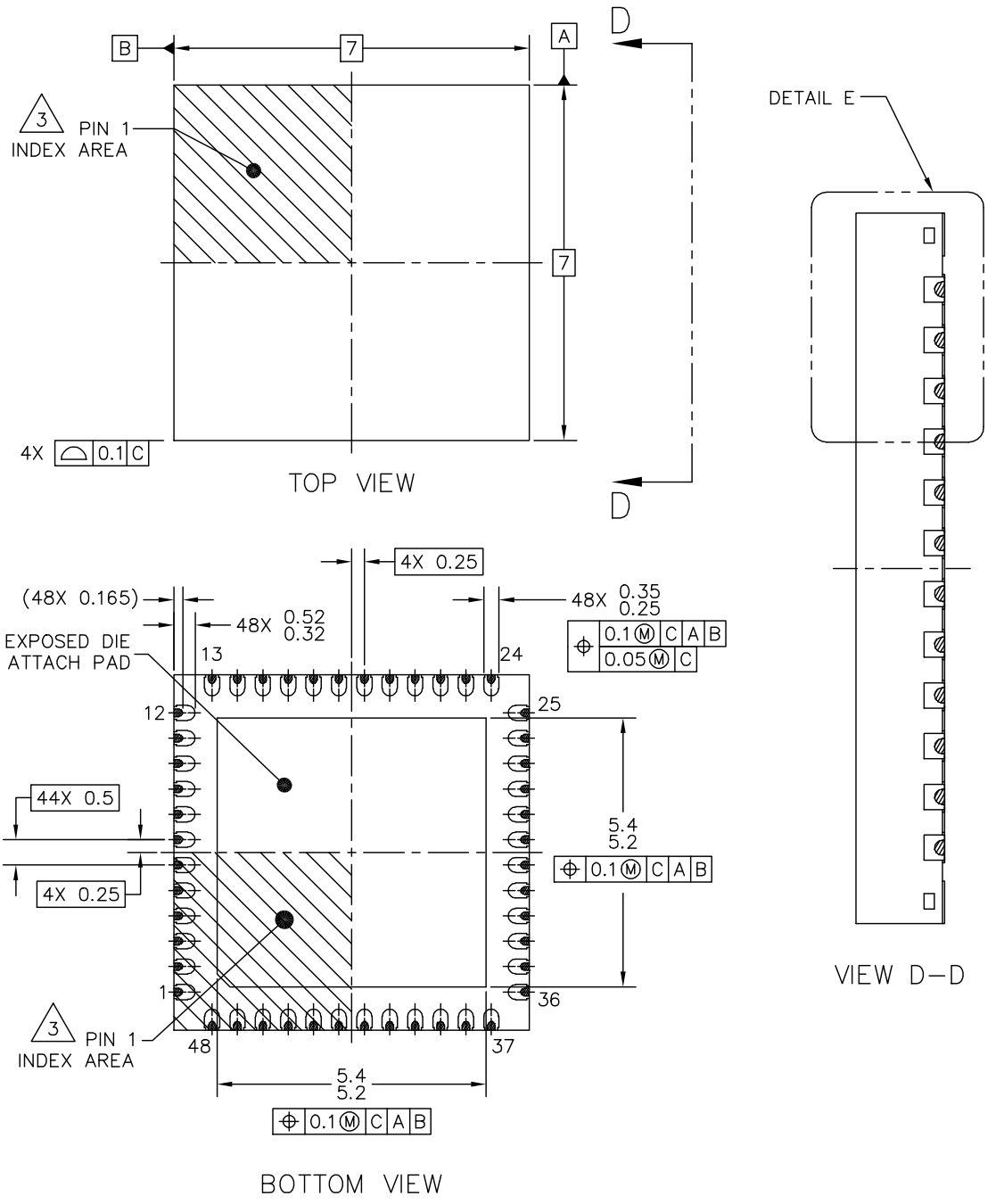
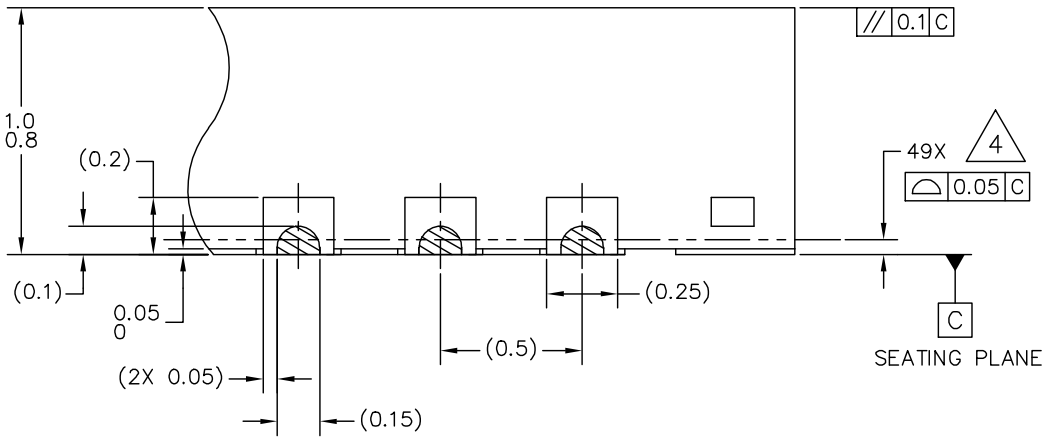


Fig. 1. Package outline SOT619-25(D)

plastic thermal enhanced very thin quad flat package; no leads; 0.1 dimple wettable flank, 48 terminals; 7 mm x 7 mm x 0.9 mm body



DETAIL E
VIEW ROTATED 90° CW

DATE: 28 FEB 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT619−25(D)	REVISION: O	

Fig. 2. Package outline dt1 HVQFN48 (SOT619-25(D))

plastic thermal enhanced very thin quad flat package; no leads; 0.1 dimple wettable flank, 48 terminals; 7 mm x 7 mm x 0.9 mm body

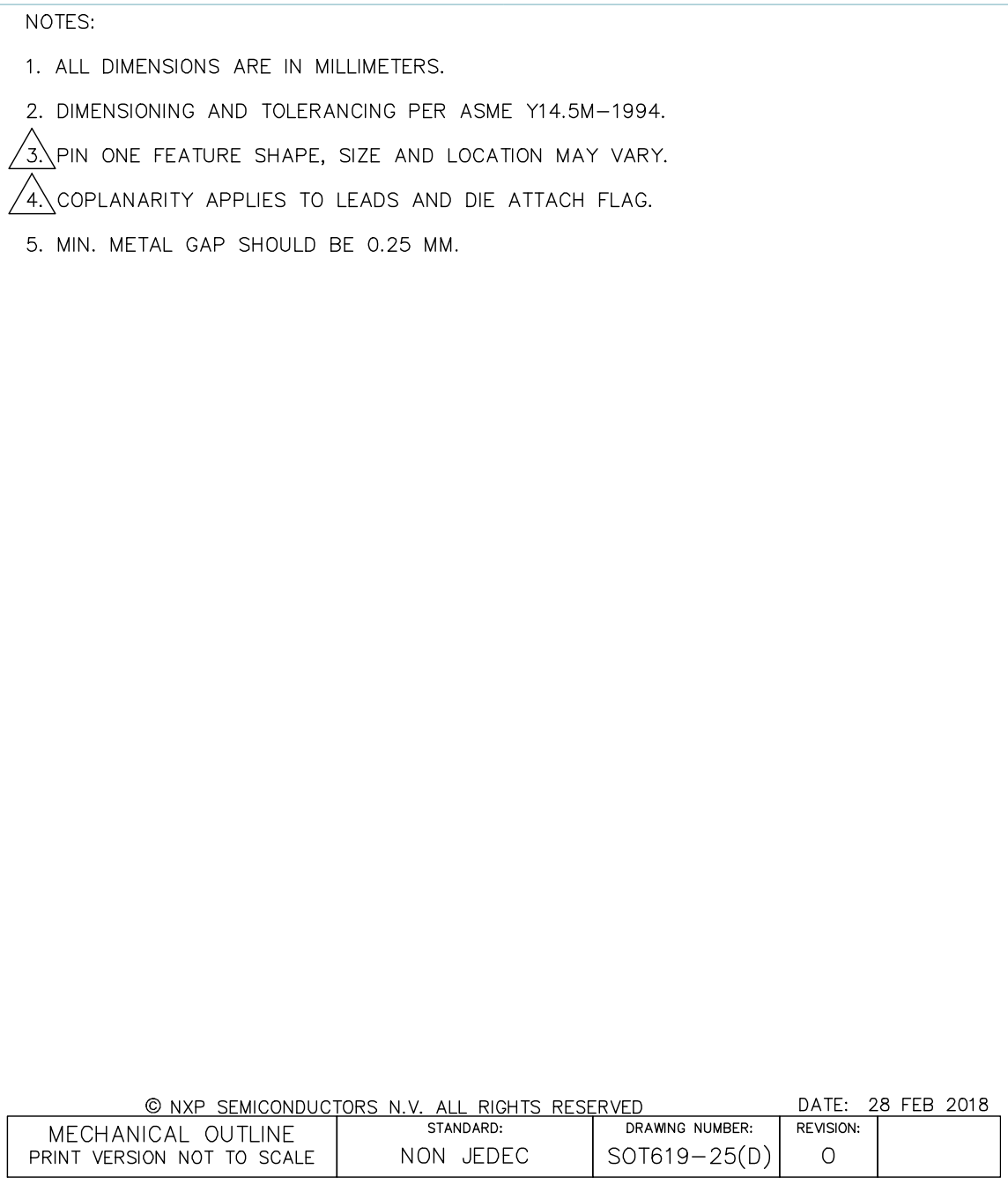


Fig. 3. Package outline note HVQFN48 (SOT619-25(D))

3. Soldering

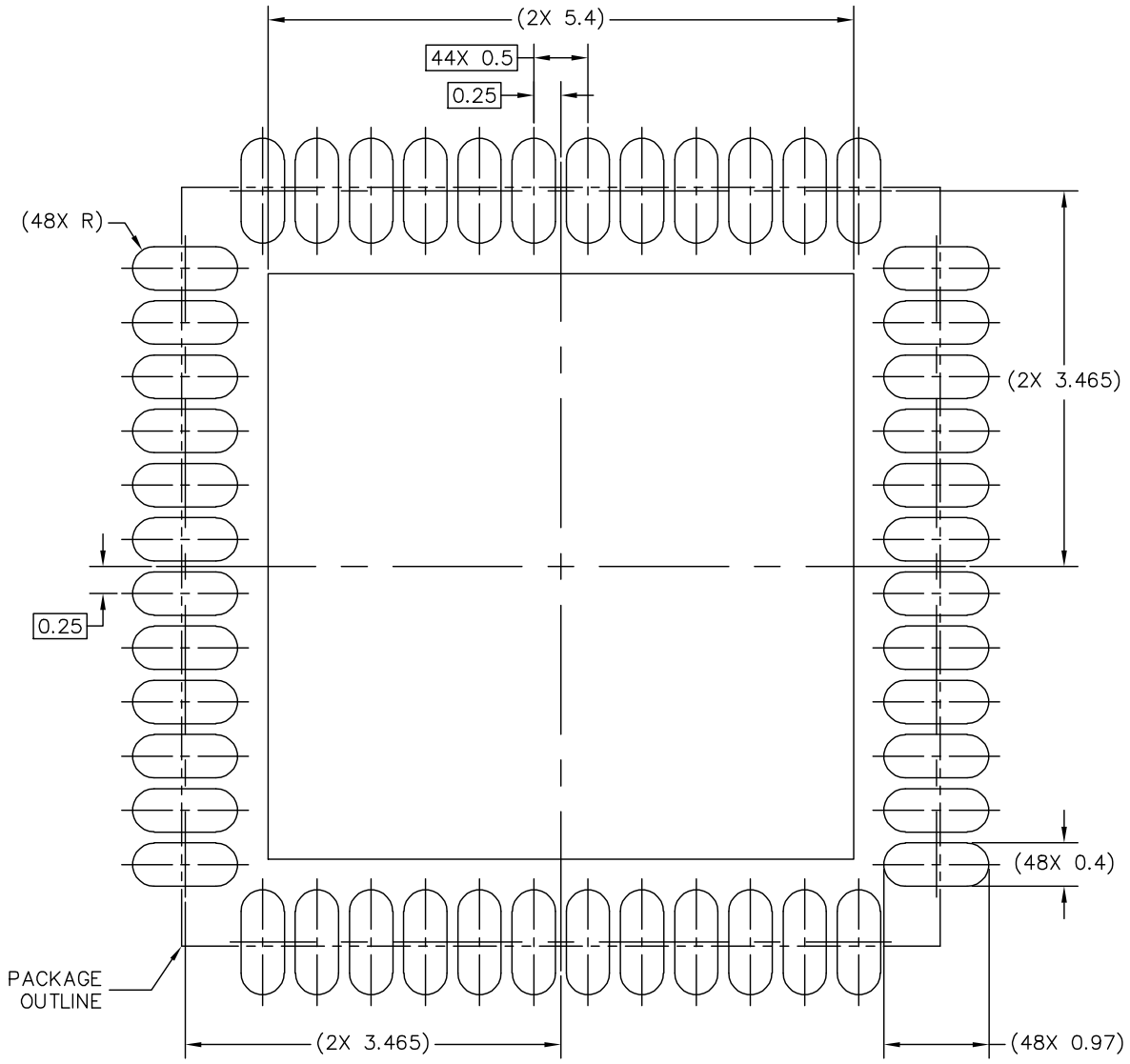
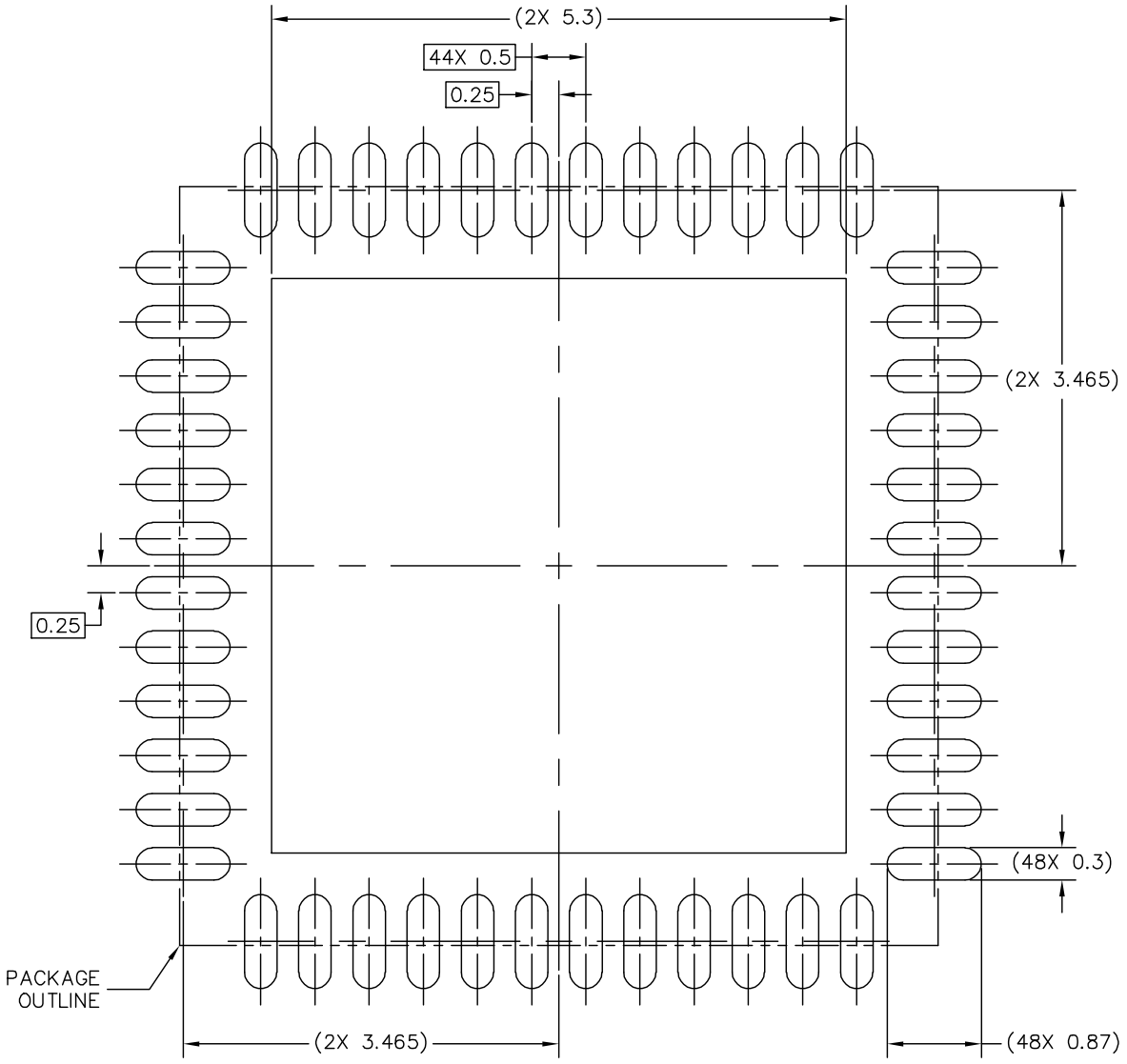


Fig. 4. Reflow soldering footprint for SOT619-25(D)

plastic thermal enhanced very thin quad flat package; no leads; 0.1 dimple wettable flank, 48 terminals; 7 mm x 7 mm x 0.9 mm body



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 28 FEB 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT619–25(D)	REVISION: O	

Fig. 5. Reflow soldering footprint part2 for HVQFN48 (SOT619-25(D))

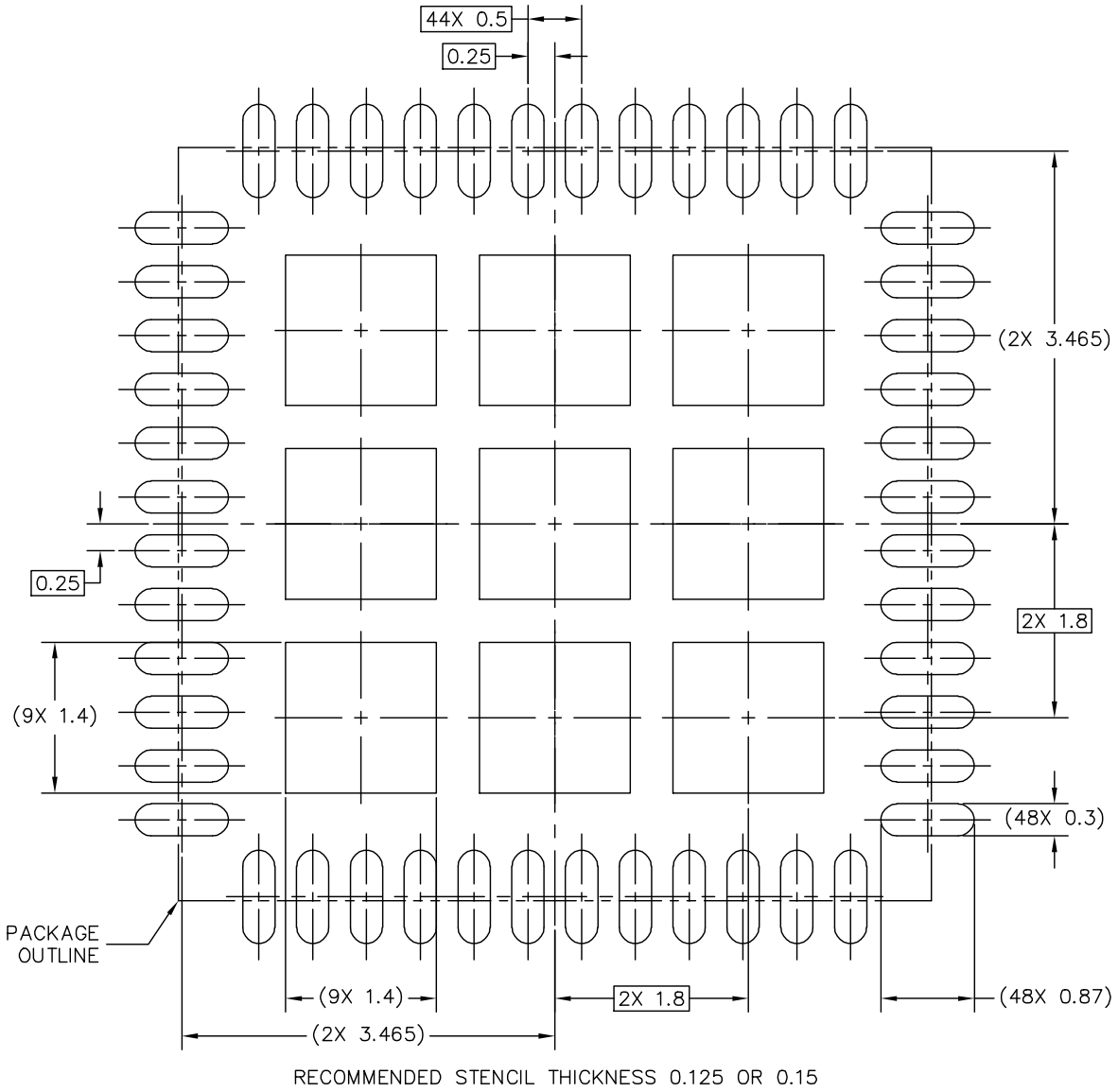


Fig. 6. Reflow soldering footprint part3 for HVQFN48 (SOT619-25(D))

4. Legal information

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

5. Contents

1. Package summary..... 1
2. Package outline..... 2
3. Soldering..... 5
4. Legal information..... 8

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com
Date of release: 30 March 2018