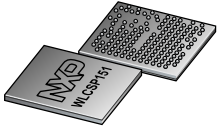# SOT2152-1

WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

27 October 2023   **Package information**

1   Package summary

Terminal position code	P (perpendicular)
Package type descriptive code	WLCSP151
Package style descriptive code	WLCSP (wafer level chip-size package)
Package body material type	S (silicon)
Mounting method type	S (surface mount)
Issue date	04-05-2023
Manufacturer package code	98ASA01782D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	5.135	5.165	5.195	mm
package width	4.38	4.68	4.98	mm
package height	0.425	0.455	5.195	mm
nominal pitch	-	0.3	-	mm

WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

2 Package outline

WLCSP-151 I/O
5.165 X 4.68 X 0.455 PKG, 0.3 PITCH (BACKSIDE COATING INCLUDED)

SOT2152-1

TOP VIEW

BOTTOM VIEW

VIEW D-D

RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01782D	REVISION: O	DATE: 04 MAY 2023

Figure 1. Package outline WLCSP151 (SOT2152-1)

SOT2152-1

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Package information

27 October 2023

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WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

WLCSP-151 I/O
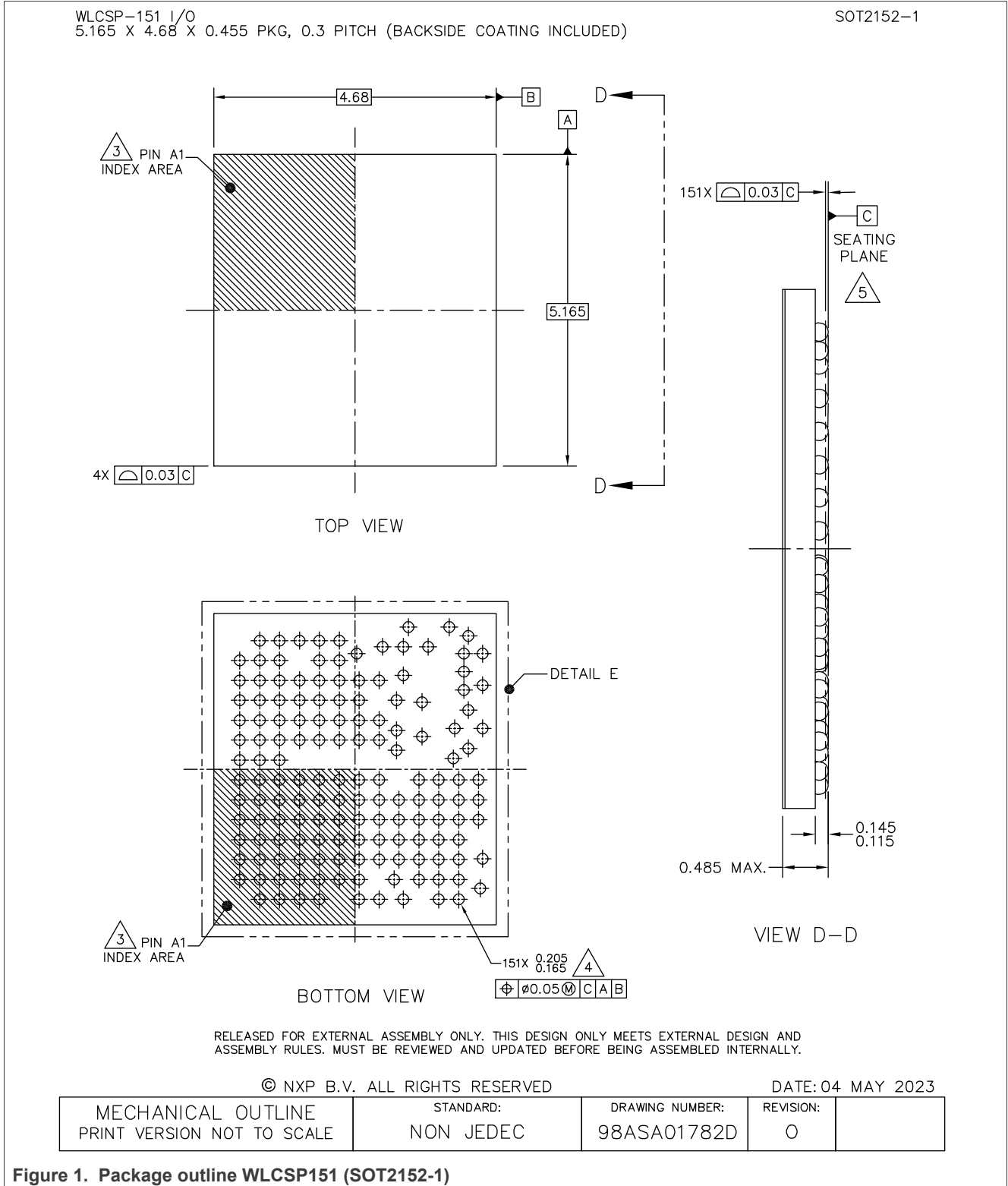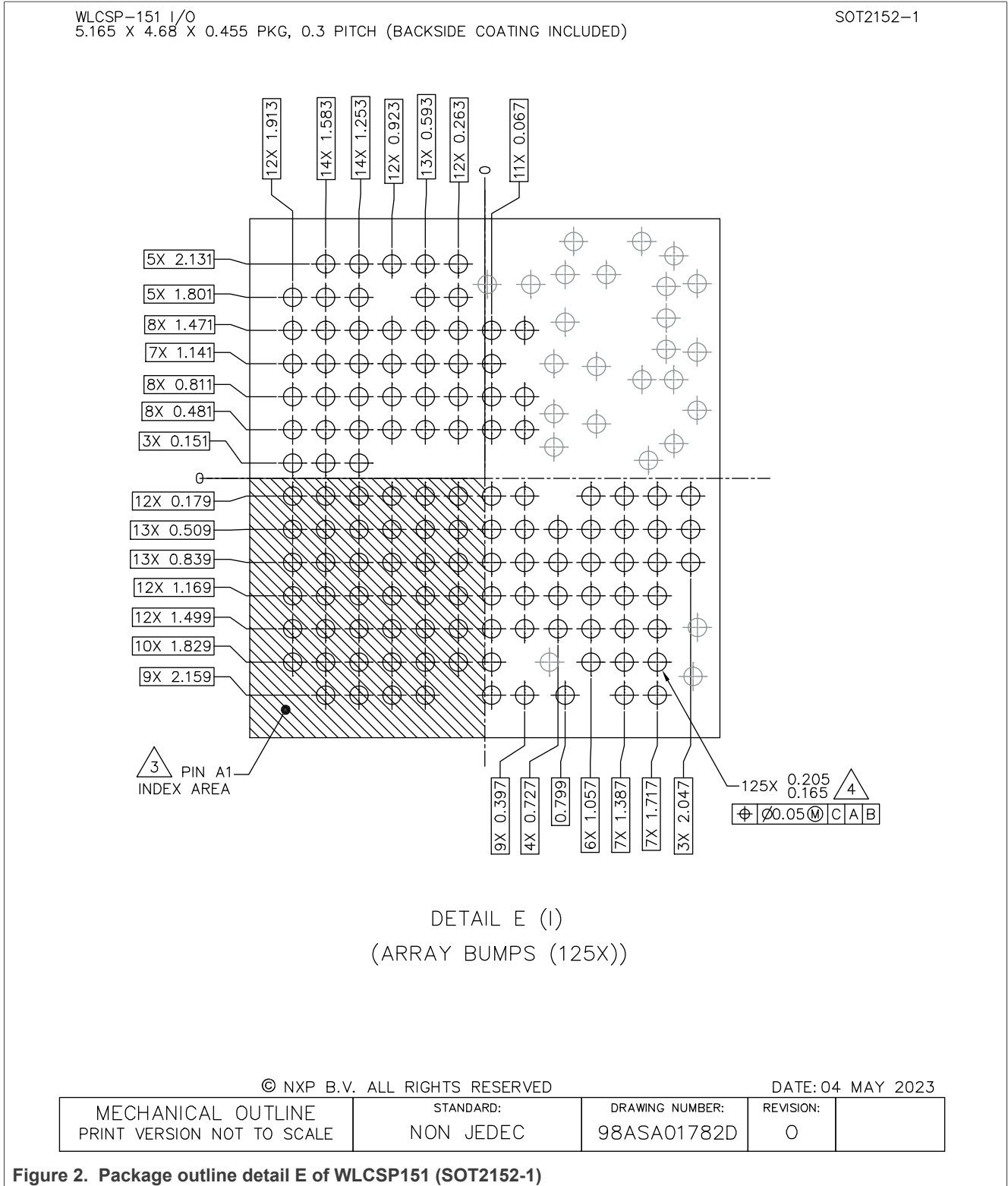5.165 X 4.68 X 0.455 PKG, 0.3 PITCH (BACKSIDE COATING INCLUDED)

SOT2152-1

12X 1.913
14X 1.583
14X 1.253
12X 0.923
13X 0.593
12X 0.263
0
11X 0.067

5X 2.131
5X 1.801
8X 1.471
7X 1.141
8X 0.811
8X 0.481
3X 0.151
0
12X 0.179
13X 0.509
13X 0.839
12X 1.169
12X 1.499
10X 1.829
9X 2.159

△3 PIN A1
INDEX AREA

9X 0.397
4X 0.727
0.799
6X 1.057
7X 1.387
7X 1.717
3X 2.047

125X $\frac{0.205}{0.165}$ △4

⊕ ⌀0.05 Ⓜ C A B

DETAIL E (I)
(ARRAY BUMPS (125X))

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DATE: 04 MAY 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01782D	REVISION: O

Figure 2. Package outline detail E of WLCSP151 (SOT2152-1)

SOT2152-1

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Package information **27 October 2023**

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WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)
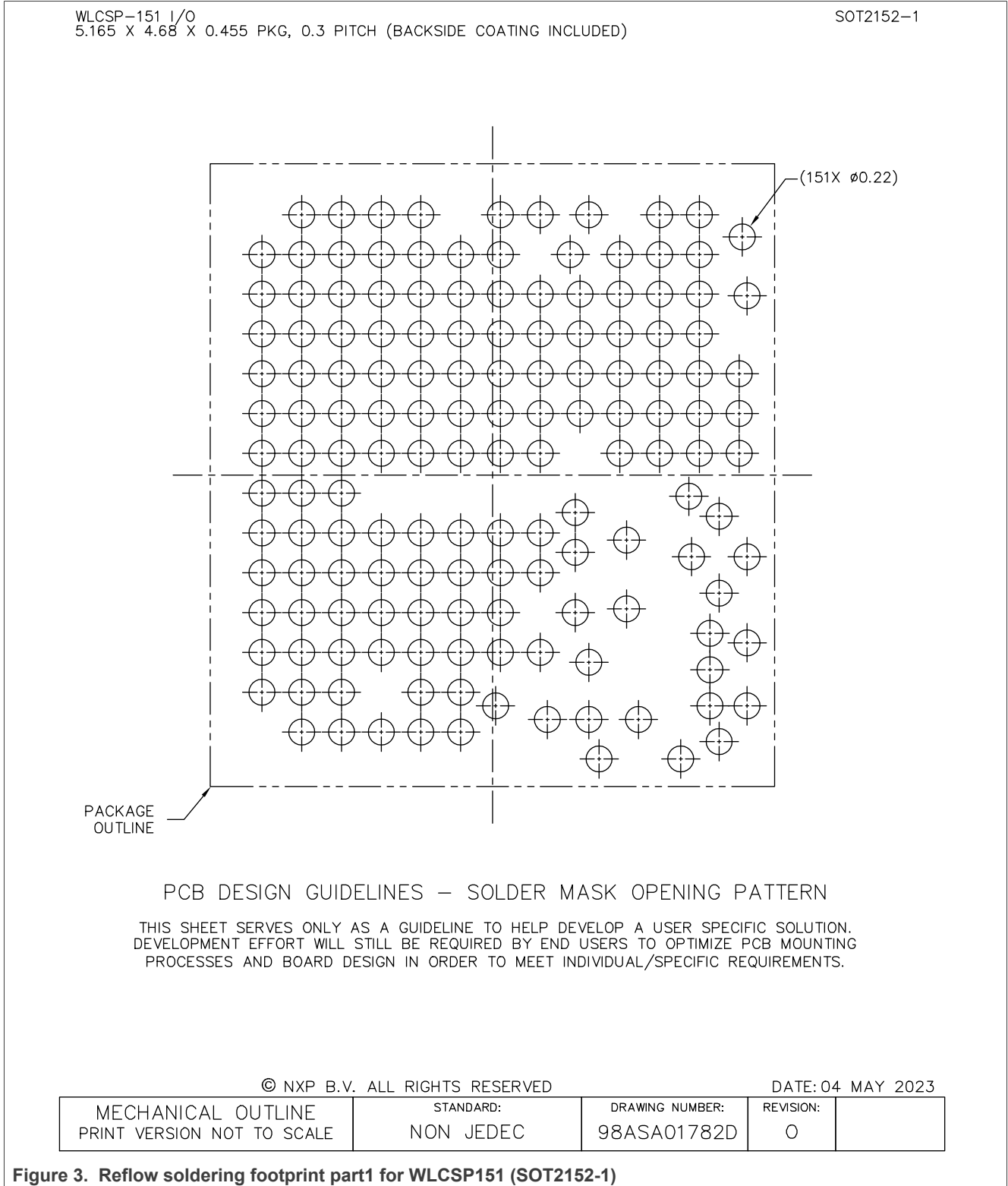
3 Soldering

WLCSP-151 I/O
5.165 X 4.68 X 0.455 PKG, 0.3 PITCH (BACKSIDE COATING INCLUDED)

SOT2152-1

(151X ∅0.22)

PACKAGE
OUTLINE

PCB DESIGN GUIDELINES — SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING
PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 04 MAY 2023

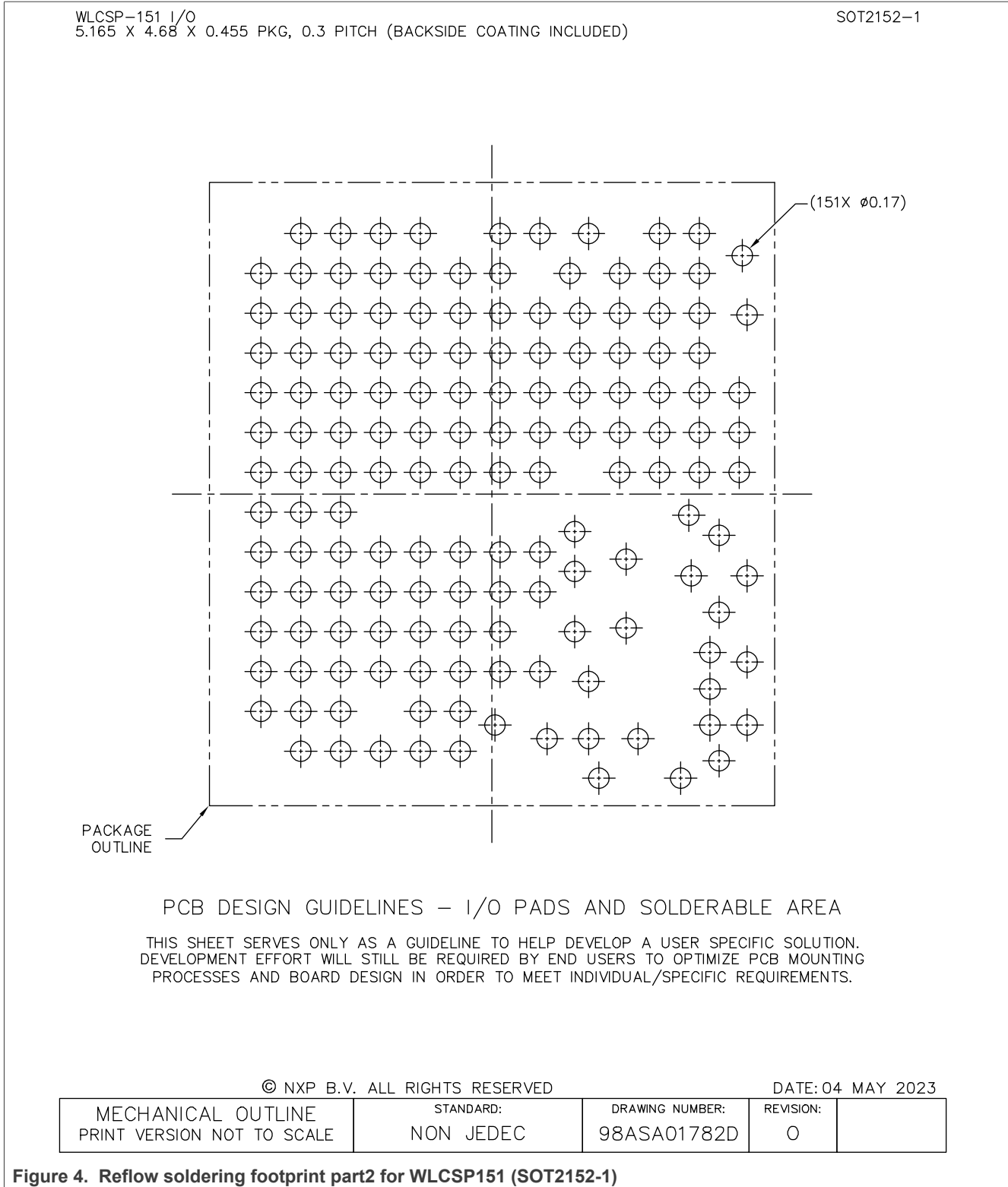| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01782D	REVISION: O	

Figure 3. Reflow soldering footprint part1 for WLCSP151 (SOT2152-1)

WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)
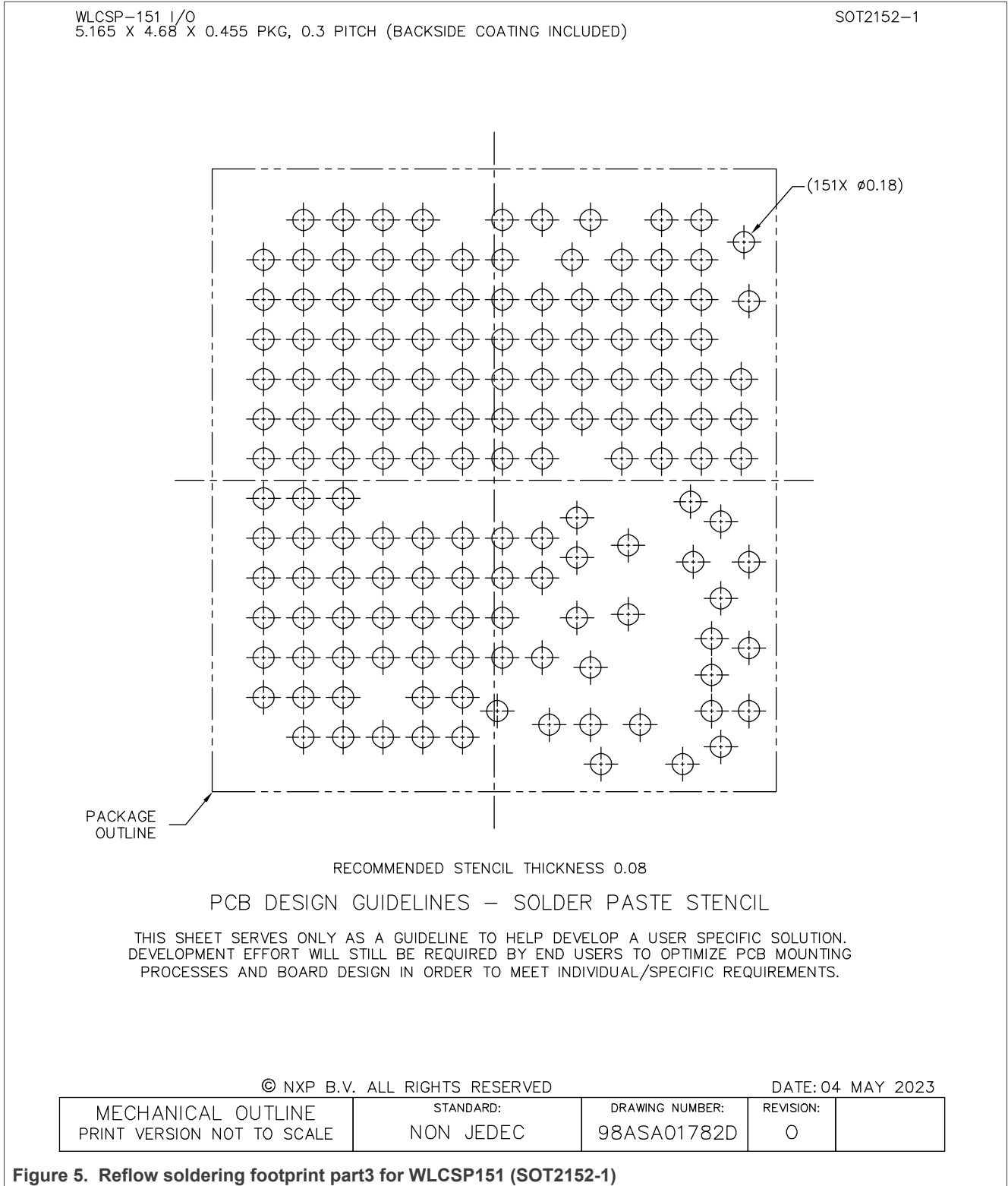
WLCSP-151 I/O
5.165 X 4.68 X 0.455 PKG, 0.3 PITCH (BACKSIDE COATING INCLUDED)

SOT2152-1

(151X ⌀0.17)

PACKAGE
OUTLINE

PCB DESIGN GUIDELINES — I/O PADS AND SOLDERABLE AREA

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PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 04 MAY 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01782D	REVISION: O	

Figure 4. Reflow soldering footprint part2 for WLCSP151 (SOT2152-1)

WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

WLCSP-151 I/O
5.165 X 4.68 X 0.455 PKG, 0.3 PITCH (BACKSIDE COATING INCLUDED)

SOT2152-1

(151X ∅0.18)

PACKAGE
OUTLINE

RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES — SOLDER PASTE STENCIL

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DATE: 04 MAY 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01782D	REVISION: O

Figure 5. Reflow soldering footprint part3 for WLCSP151 (SOT2152-1)

SOT2152-1

Package information

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27 October 2023

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NXP Semiconductors **SOT2152-1**

WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

WLCSP-151 I/O   SOT2152-1
5.165 X 4.68 X 0.455 PKG, 0.3 PITCH (BACKSIDE COATING INCLUDED)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01782D	REVISION: O

Figure 6. Package outline note WLCSP151 (SOT2152-1)

NXP Semiconductors **SOT2152-1**

WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

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WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

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