



# SOT2146-1

WLCSP70, wafer level chip scale package, 70 terminals, 0.35 mm pitch, 3.64 mm x 3.16 mm x 0.49 mm body (backside coating included)

1 December 2021

Package information

## 1 Package summary

<b>Terminal position code</b>	B (bottom)
<b>Package type descriptive code</b>	WLCSP70
<b>Package style descriptive code</b>	WLCSP (wafer level chip-size package)
<b>Mounting method type</b>	S (surface mount)
<b>Issue date</b>	01-06-2021
<b>Manufacturer package code</b>	98ASA01767D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	3.61	3.64	3.67	mm
package width	3.13	3.16	3.19	mm
package height	-	0.49	0.525	mm
nominal pitch	-	0.35	-	mm
actual quantity of termination	-	70	-	



WLCSP70, wafer level chip scale package, 70 terminals, 0.35 mm pitch, 3.64 mm x 3.16 mm x 0.49 mm body (backside coating included)

2 Package outline

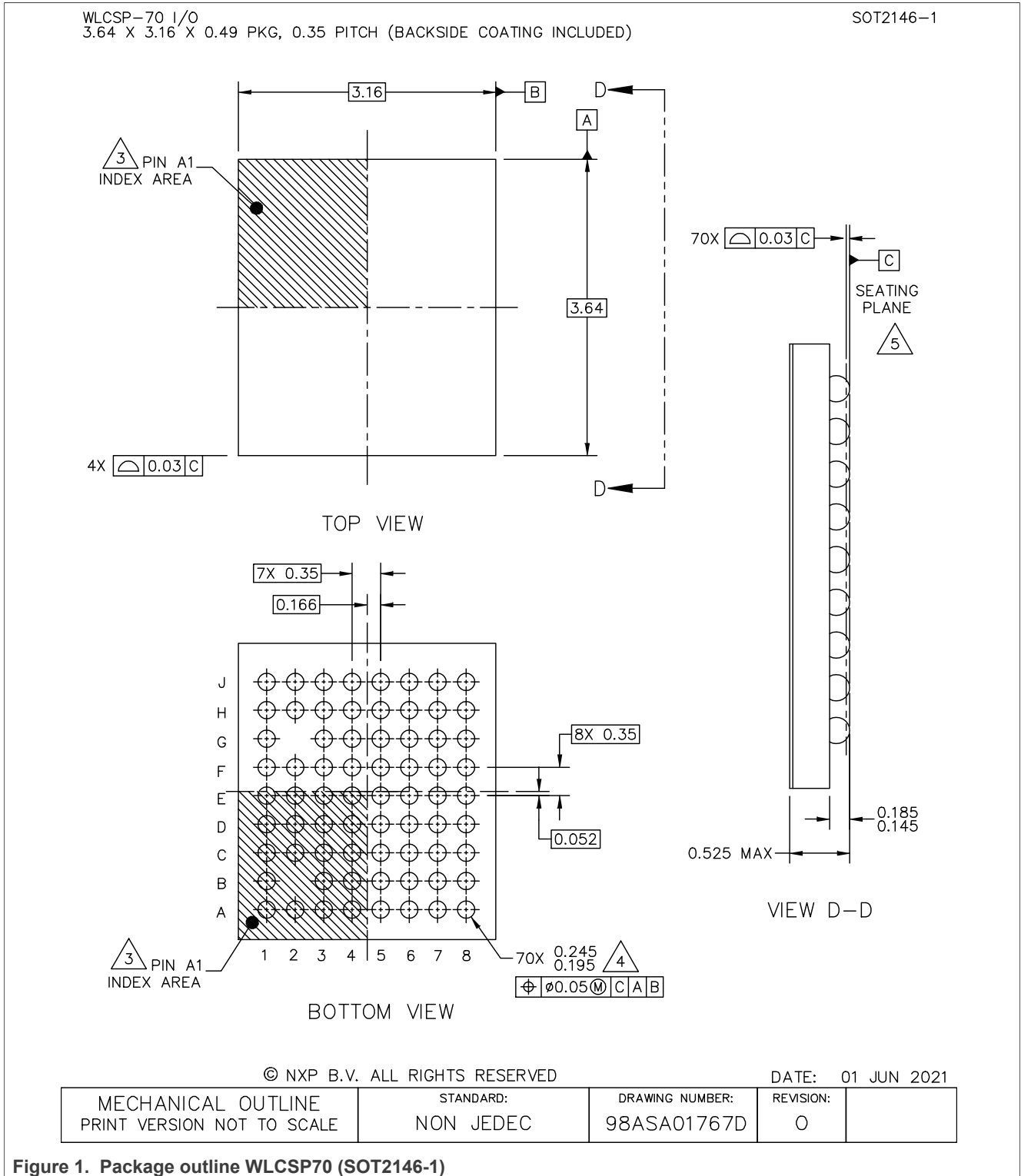


Figure 1. Package outline WLCSP70 (SOT2146-1)

WLCSP70, wafer level chip scale package, 70 terminals, 0.35 mm pitch, 3.64 mm x 3.16 mm x 0.49 mm body (backside coating included)

3 Soldering

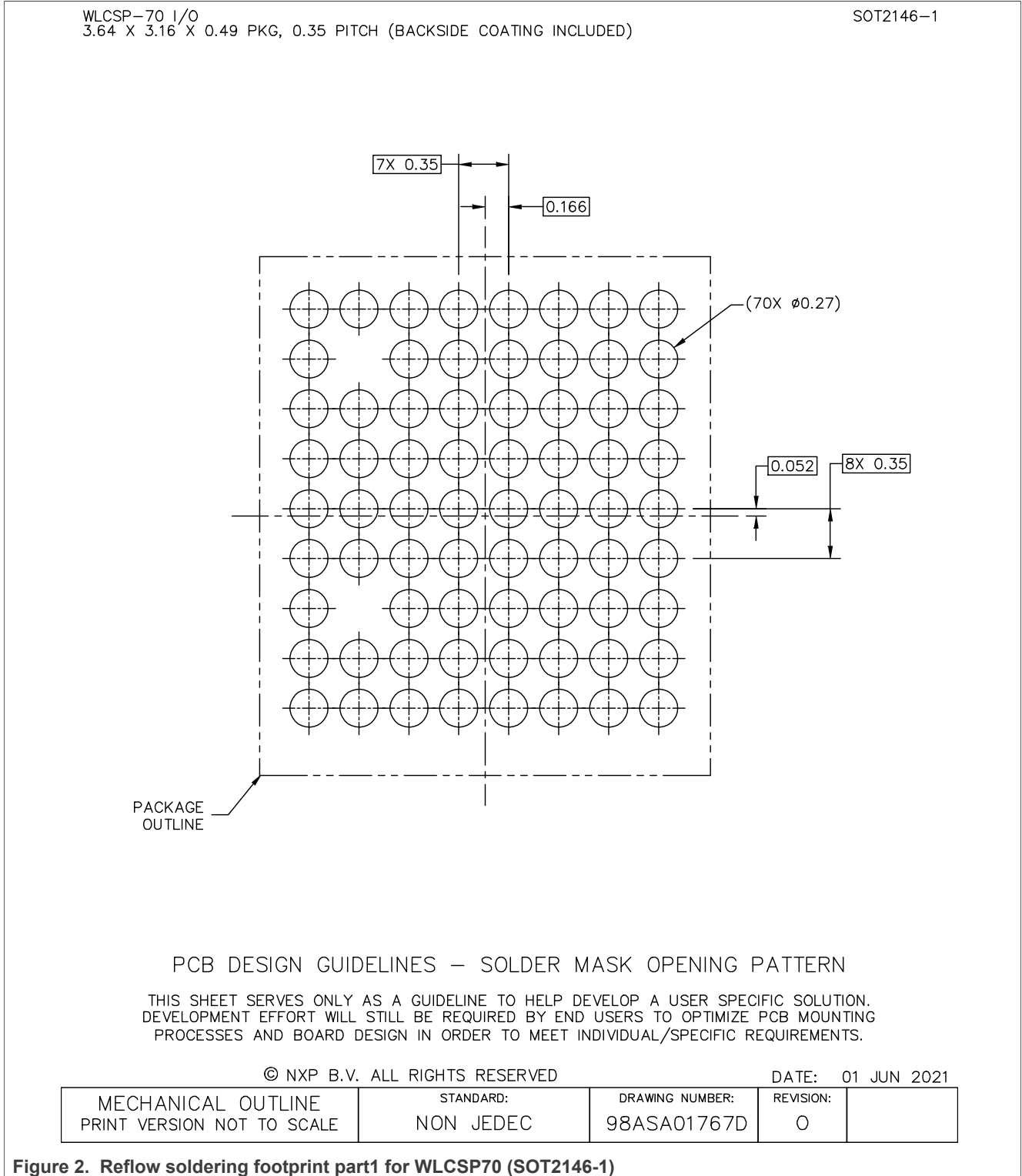
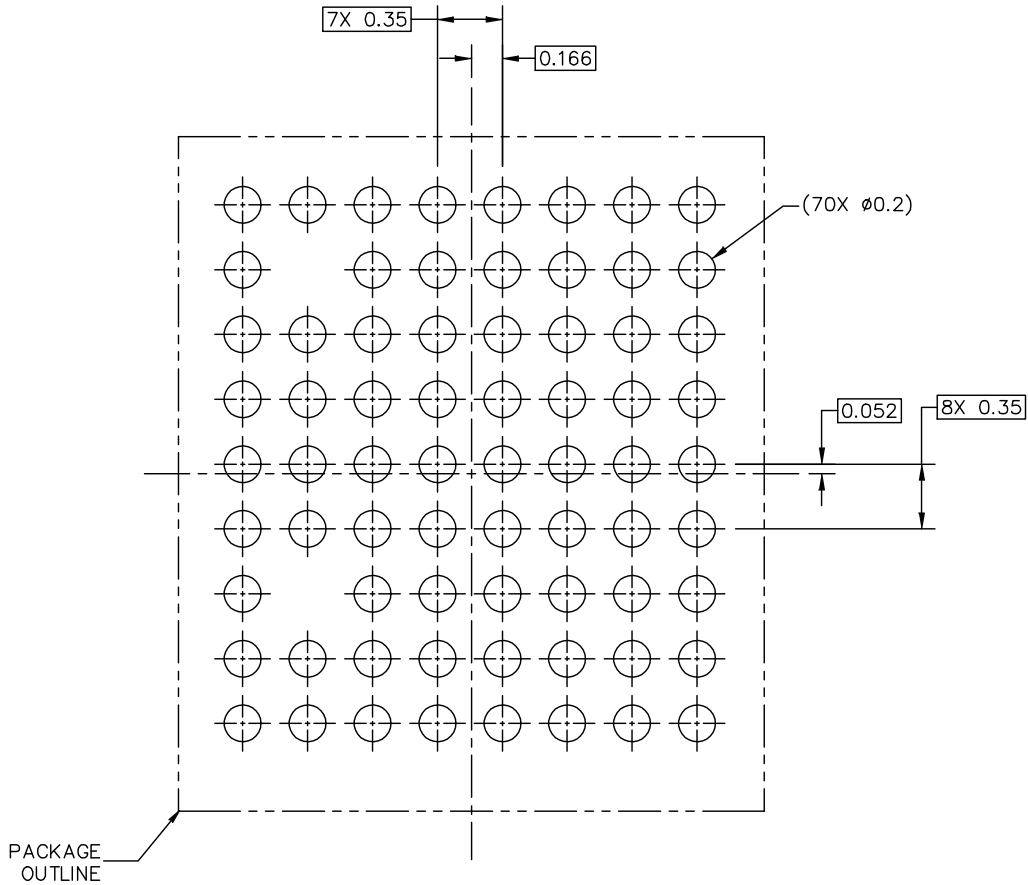


Figure 2. Reflow soldering footprint part1 for WLCSP70 (SOT2146-1)

WLCSP70, wafer level chip scale package, 70 terminals, 0.35 mm pitch, 3.64 mm x 3.16 mm x 0.49 mm body (backside coating included)

WLCSP-70 I/O  
3.64 X 3.16 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2146-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

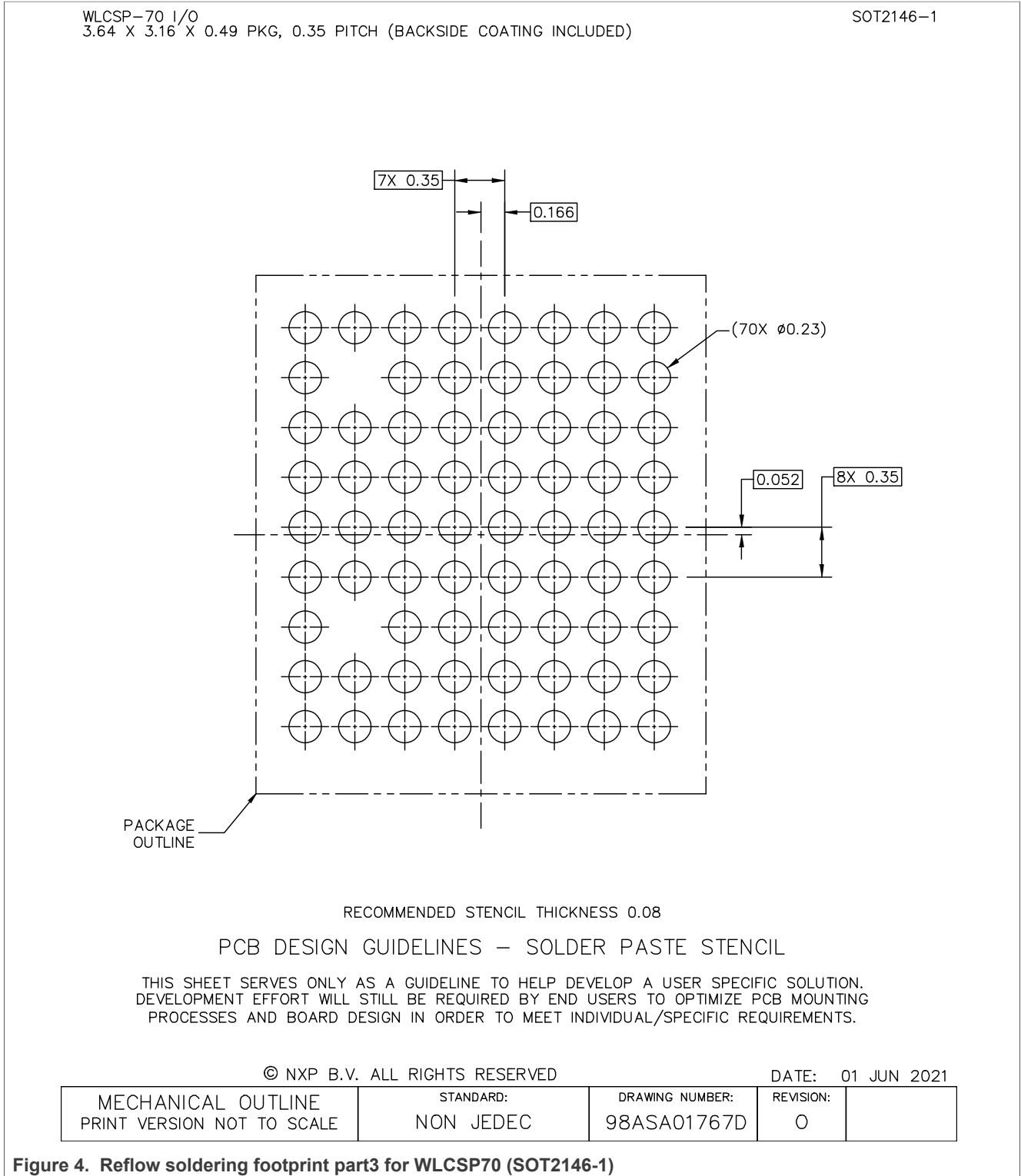
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DATE: 01 JUN 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01767D	REVISION: 0
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Figure 3. Reflow soldering footprint part2 for WLCSP70 (SOT2146-1)

WLCSP70, wafer level chip scale package, 70 terminals, 0.35 mm pitch, 3.64 mm x 3.16 mm x 0.49 mm body (backside coating included)



**WLCSP70, wafer level chip scale package, 70 terminals, 0.35 mm pitch, 3.64 mm x 3.16 mm x 0.49 mm body (backside coating included)**

WLCSP-70 I/O  
3.64 X 3.16 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2146-1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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Figure 5. Package outline note WLCSP70 (SOT2146-1)

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WLCSP70, wafer level chip scale package, 70 terminals, 0.35 mm pitch, 3.64 mm x 3.16 mm x 0.49 mm  
body (backside coating included)

## 4 Legal information

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