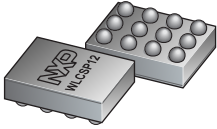


SOT2063-4

WLCSP12, wafer level chip-size package, 12 terminals, 0.35 mm pitch, 1.405 mm x 1.055 mm x 0.49 mm body (backside coating included)

27 September 2024

Package information



1 Package summary

Package type descriptive code	WLCSP12
Package style descriptive code	WLCSP (wafer level chip-size package)
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Issue date	03-07-2024
Manufacturer package code	98ASA02192D

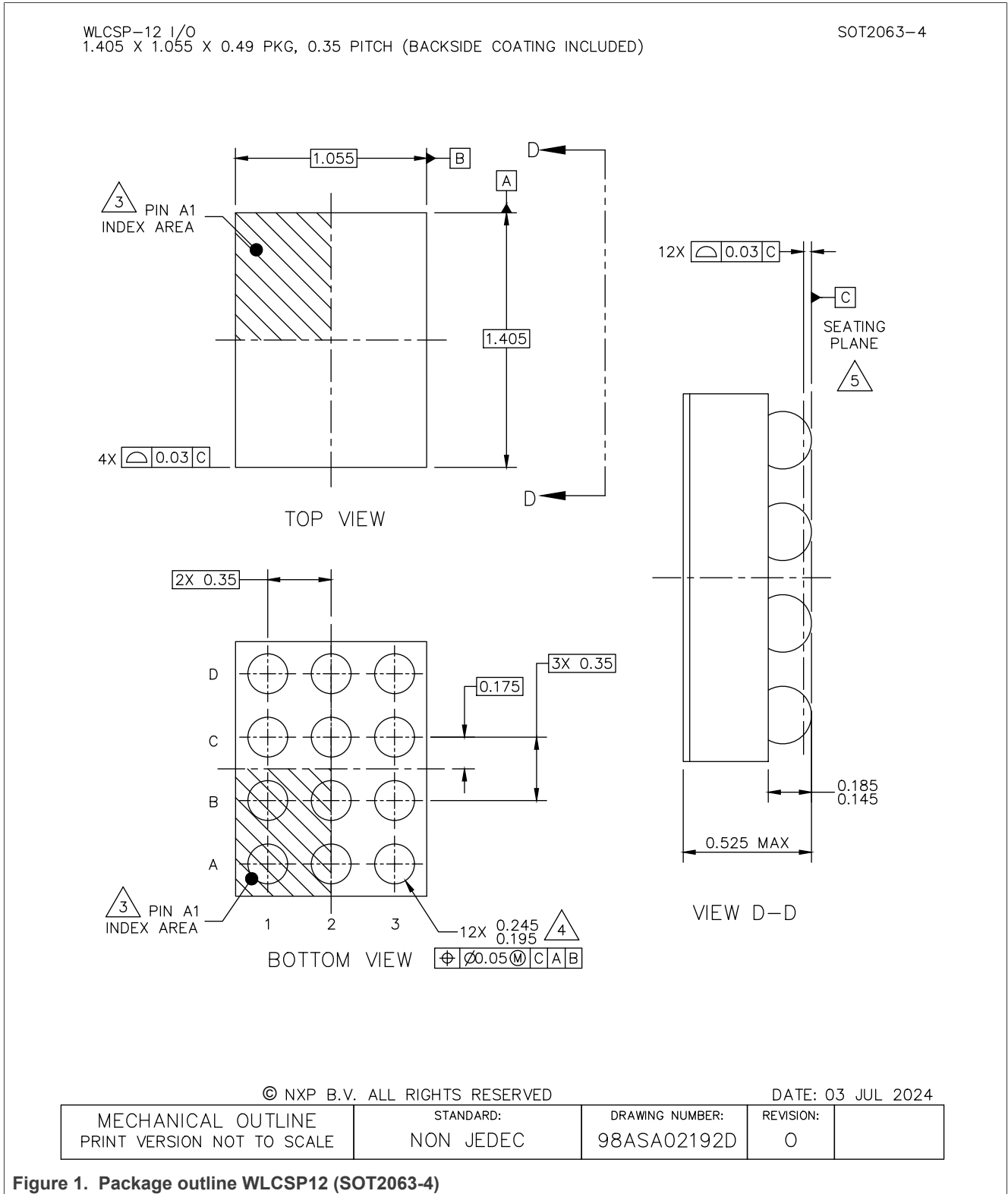
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	1.375	1.405	1.435	mm
package width	1.025	1.055	1.085	mm
seated height	0.455	0.49	0.525	mm
package height	0.3	0.325	0.35	mm
nominal pitch	-	0.35	-	mm
actual quantity of termination	-	12	-	



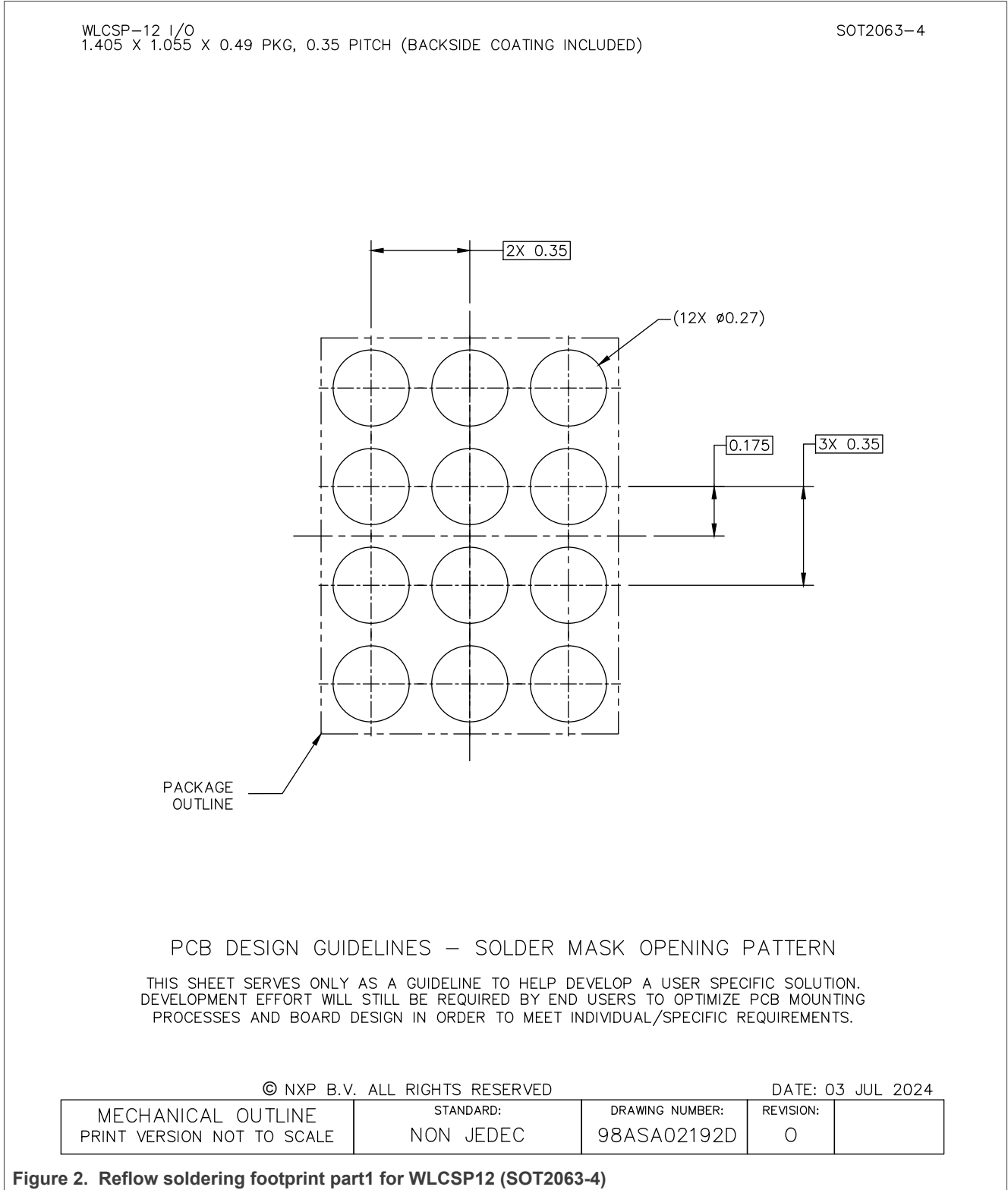
WLCSP12, wafer level chip-size package, 12 terminals, 0.35 mm pitch, 1.405 mm x 1.055 mm x 0.49 mm body (backside coating included)

2 Package outline



WLCSP12, wafer level chip-size package, 12 terminals, 0.35 mm pitch, 1.405 mm x 1.055 mm x 0.49 mm body (backside coating included)

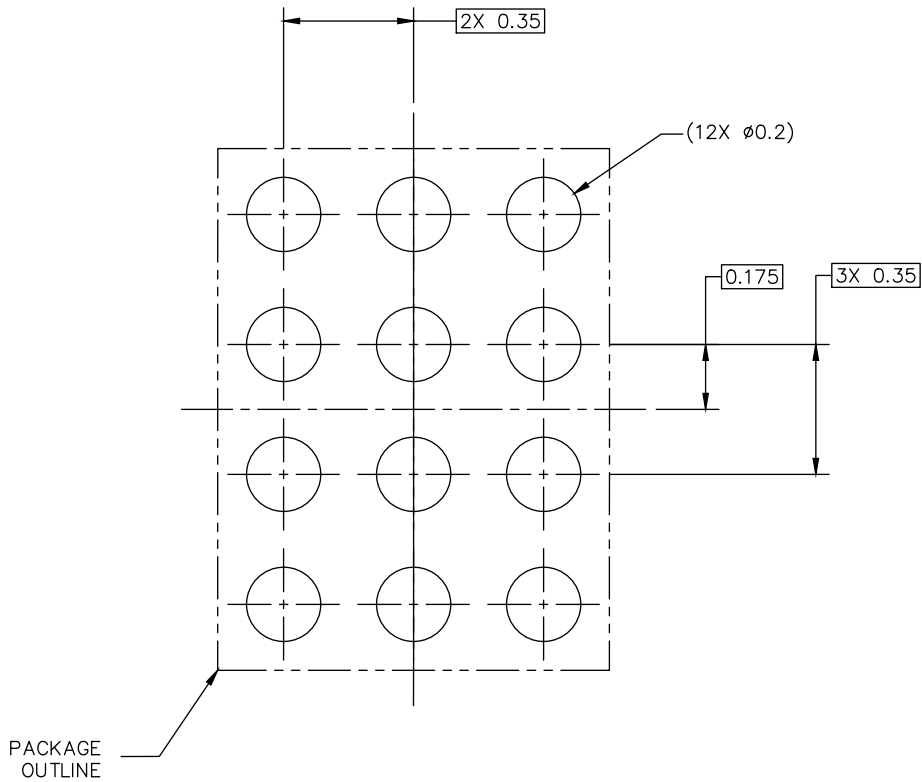
3 Soldering



WLCSP12, wafer level chip-size package, 12 terminals, 0.35 mm pitch, 1.405 mm x 1.055 mm x 0.49 mm body (backside coating included)

WLCSP-12 I/O
1.405 X 1.055 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2063-4



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 03 JUL 2024

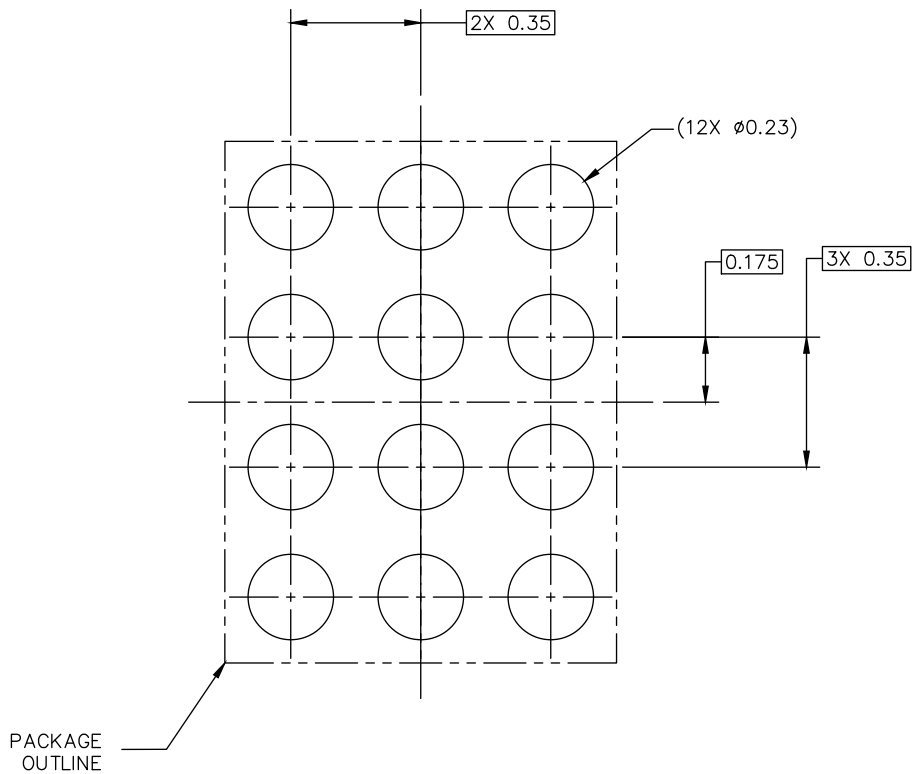
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02192D	REVISION: 0	
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Figure 3. Reflow soldering footprint part2 for WLCSP12 (SOT2063-4)

WLCSP12, wafer level chip-size package, 12 terminals, 0.35 mm pitch, 1.405 mm x 1.055 mm x 0.49 mm body (backside coating included)

WLCSP-12 I/O
 .405 X 1.055 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2063-4



RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 03 JUL 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02192D	REVISION: 0	
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Figure 4. Reflow soldering footprint part3 for WLCSP12 (SOT2063-4)

WLCSP12, wafer level chip-size package, 12 terminals, 0.35 mm pitch, 1.405 mm x 1.055 mm x 0.49 mm body (backside coating included)

WLCSP-12 I/O
 .405 X 1.055 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2063-4

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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DATE: 03 JUL 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02192D	REVISION: 0	
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Figure 5. Package outline note WLCSP12 (SOT2063-4)

WLCSP12, wafer level chip-size package, 12 terminals, 0.35 mm pitch, 1.405 mm x 1.055 mm x 0.49 mm body (backside coating included)

4 Legal information

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WLCSP12, wafer level chip-size package, 12 terminals, 0.35 mm pitch, 1.405 mm x 1.055 mm x 0.49 mm body (backside coating included)

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