

SOT2063-2

WLCSP12, wafer level chip scale package, 12 terminals, 0.35 mm pitch, 1.545 mm x 1.26 mm x 0.495 mm body

28 December 2020

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP12
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	07-09-2020
Manufacturer package code	98ASA01703D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	1.445	1.545	1.645	mm
package width	1.16	1.26	1.36	mm
package height	-	0.495	0.525	mm
nominal pitch	-	0.35	-	mm
actual quantity of termination	-	12	-	



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2 Package outline

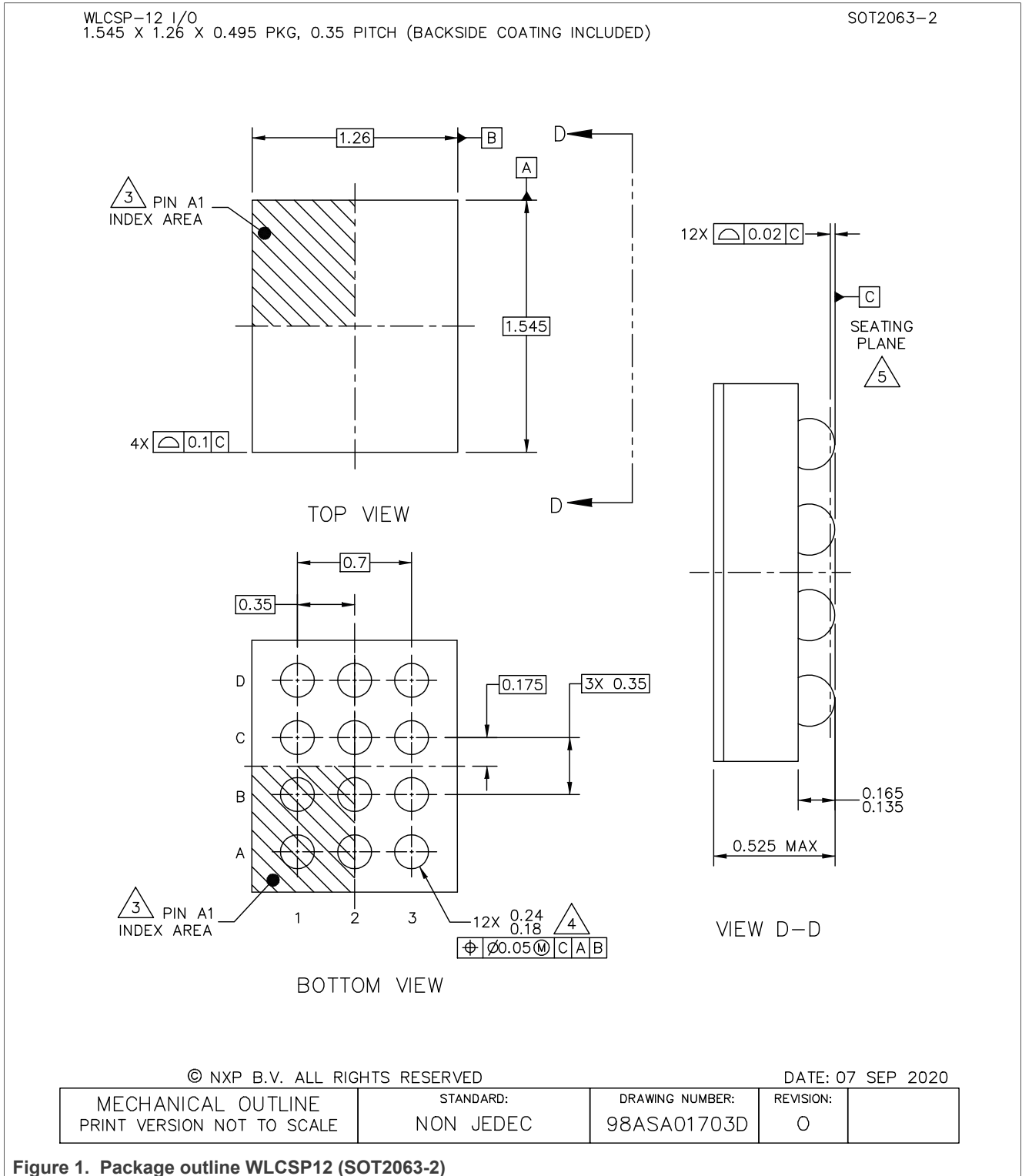
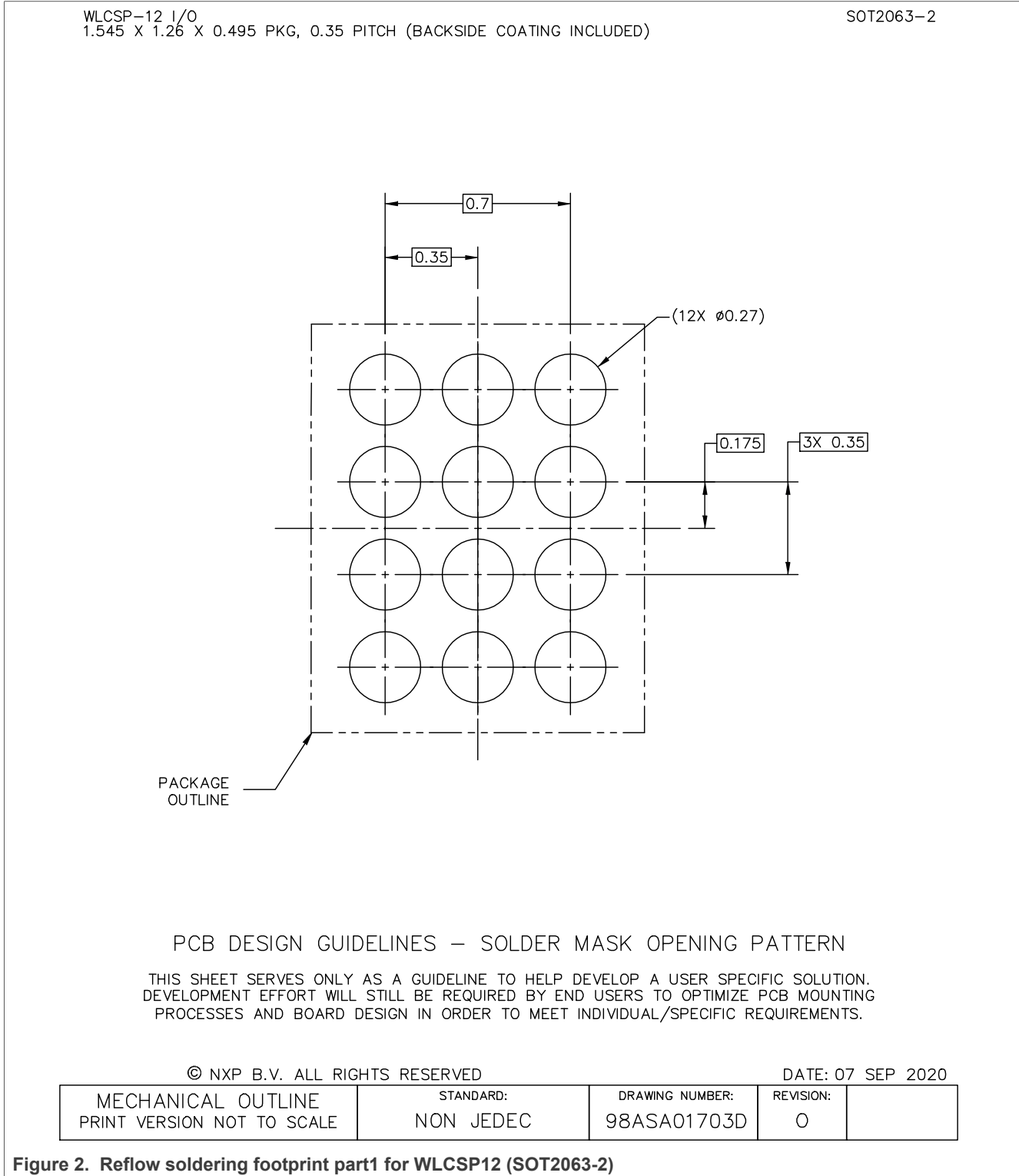


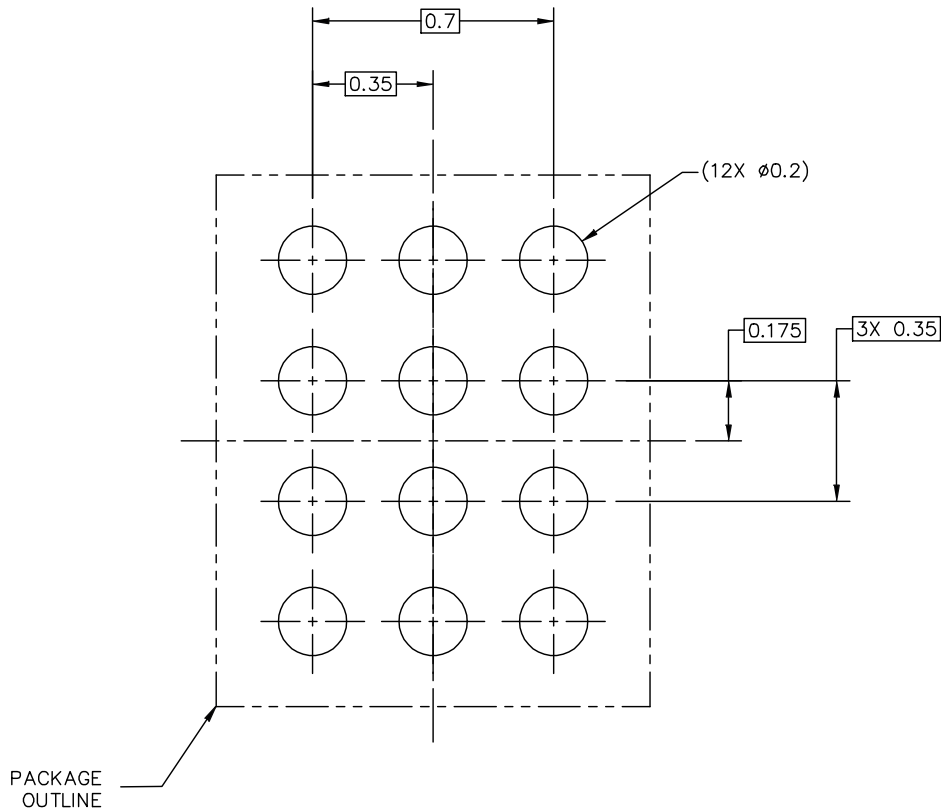
Figure 1. Package outline WLCSP12 (SOT2063-2)

3 Soldering



WLCSP-12 I/O
1.545 X 1.26 X 0.495 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2063-2



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

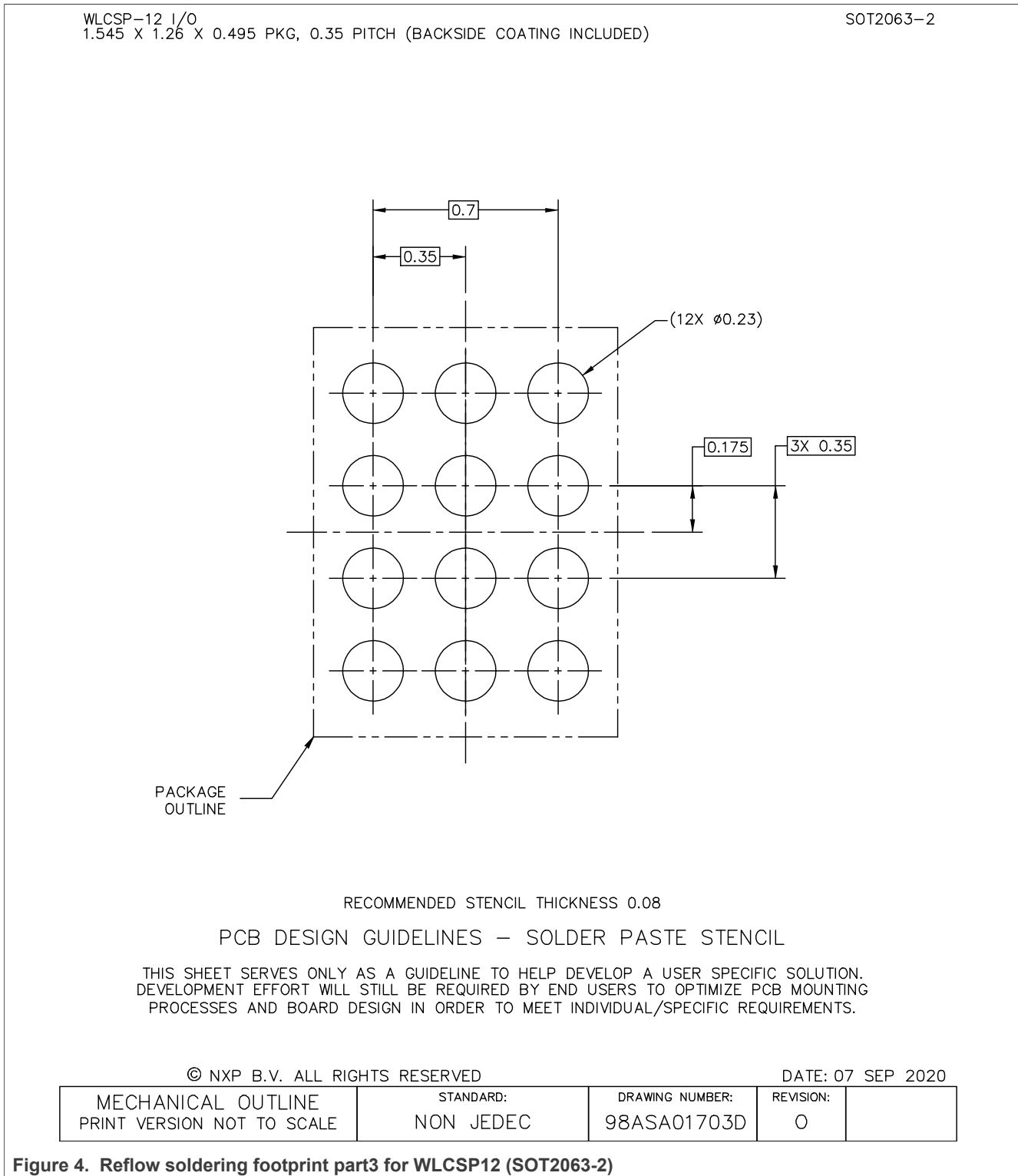
THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01703D	REVISION: 0	
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Figure 3. Reflow soldering footprint part2 for WLCSP12 (SOT2063-2)



WLCSP12, wafer level chip scale package, 12 terminals, 0.35 mm pitch, 1.545 mm x 1.26 mm x 0.495 mm body

WLCSP-12 I/O
1.545 X 1.26 X 0.495 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2063-2

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.04.

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Figure 5. Package outline note WLCSP12 (SOT2063-2)

4 Legal information

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body

Contents

- 1 Package summary1
- 2 Package outline2
- 3 Soldering3
- 4 Legal information7