

# SOT1966-1

WLCSP81, wafer level chip-scale package; 81 bumps; 0.35 mm pitch, 3.55 mm x 3.36 mm x 0.365 mm body

15 February 2018

Package information

## 1. Package summary

<b>Terminal position code</b>	B (bottom)
<b>Package type descriptive code</b>	WLCSP81
<b>Package style descriptive code</b>	WLCSP (wafer level chip-size package)
<b>Mounting method type</b>	S (surface mount)
<b>Issue date</b>	12-2-2018
<b>Manufacturer package code</b>	98ASA01195D

Table 1. Package summary

Symbol	Parameter	Min	Typ	Nom	Max	Unit
D	package length	3.52	-	3.55	3.58	mm
E	package width	3.33	-	3.36	3.39	mm
A	seated height	0.335	-	0.365	0.395	mm
e	nominal pitch	-	-	0.35	-	mm
n <sub>2</sub>	actual quantity of termination	-	-	81	-	A/A



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## 2. Package outline

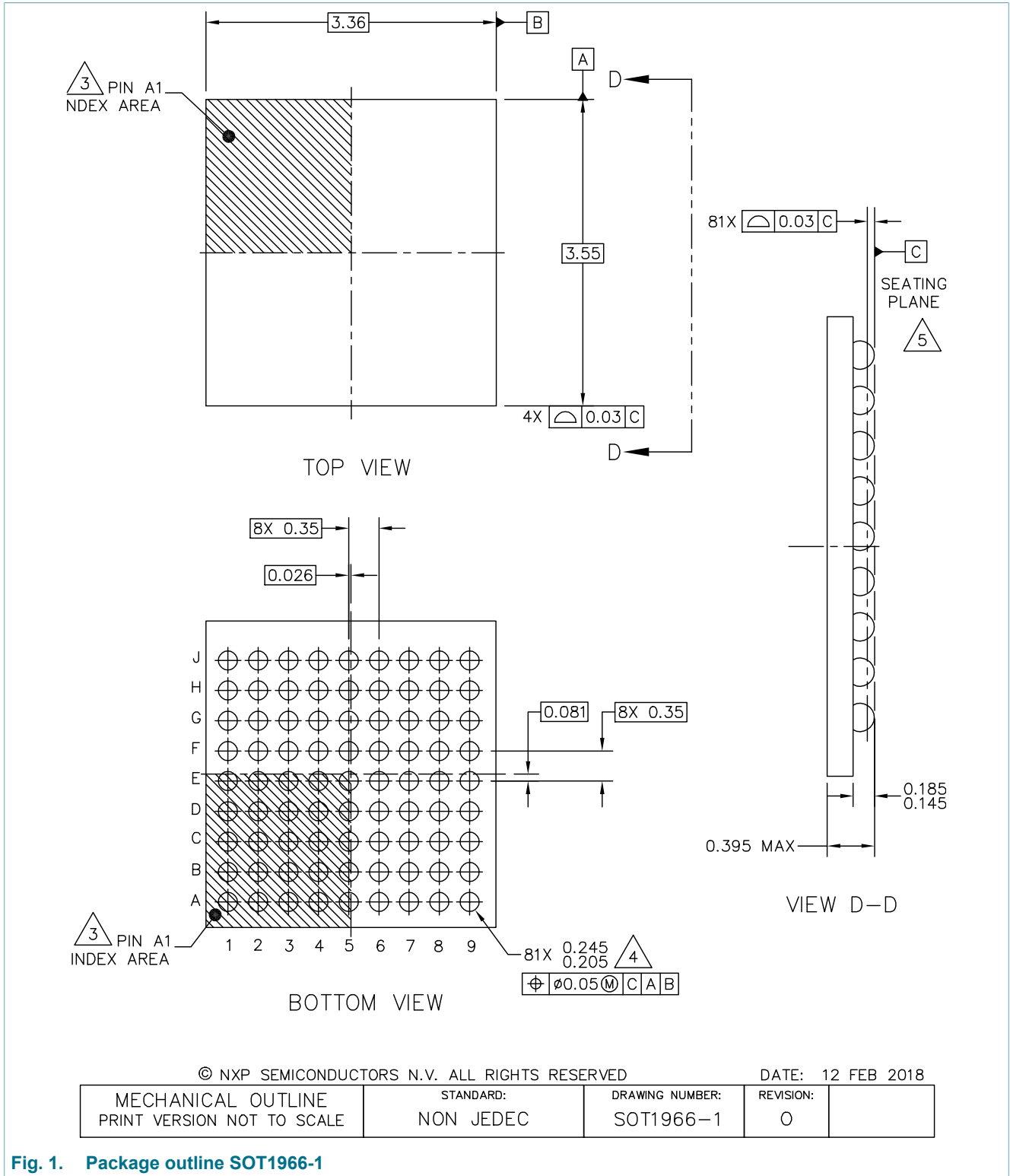


Fig. 1. Package outline SOT1966-1

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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

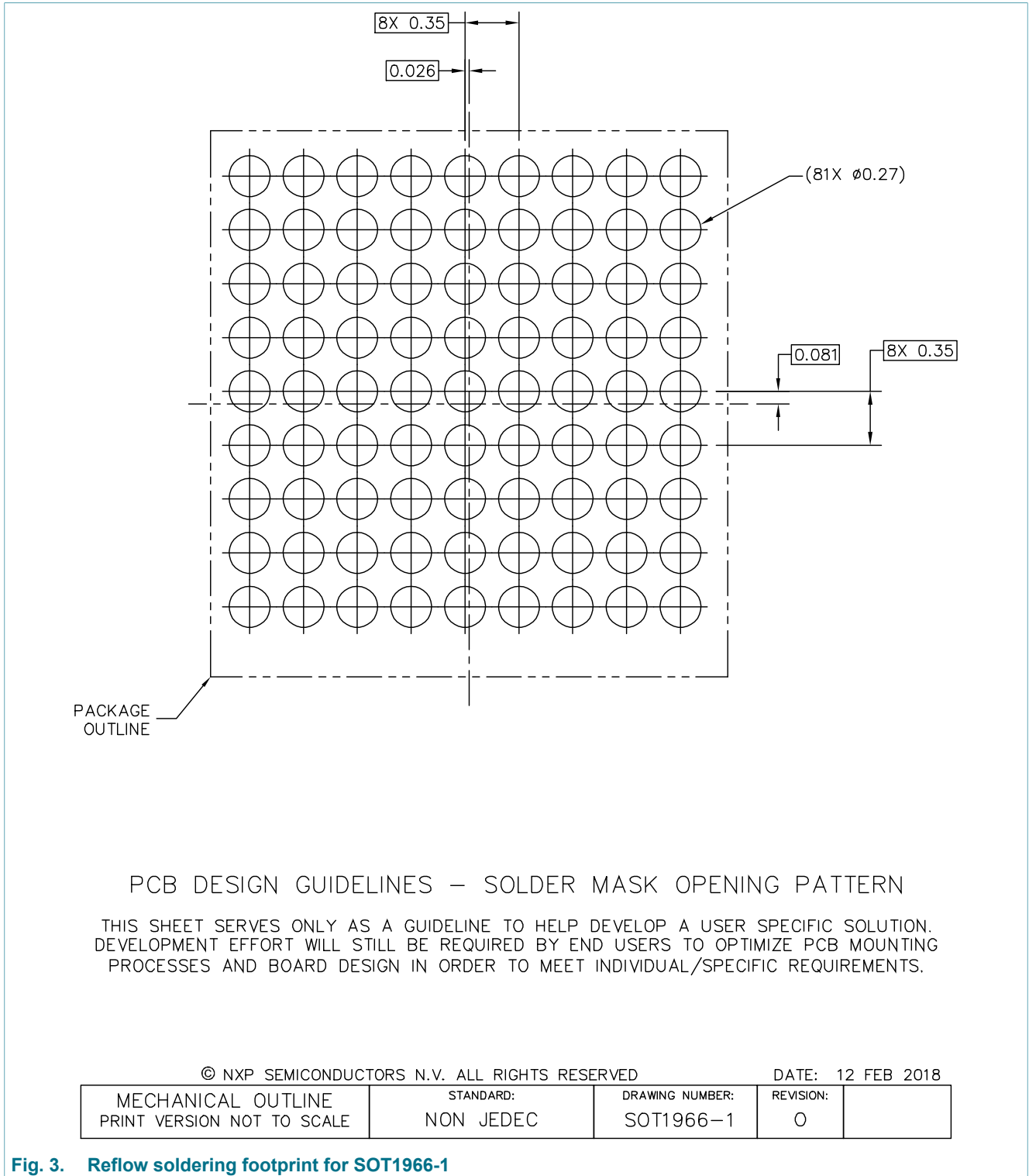
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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1966-1	REVISION: 0	
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Fig. 2. Package outline note WLCSP81 (SOT1966-1)

### 3. Soldering



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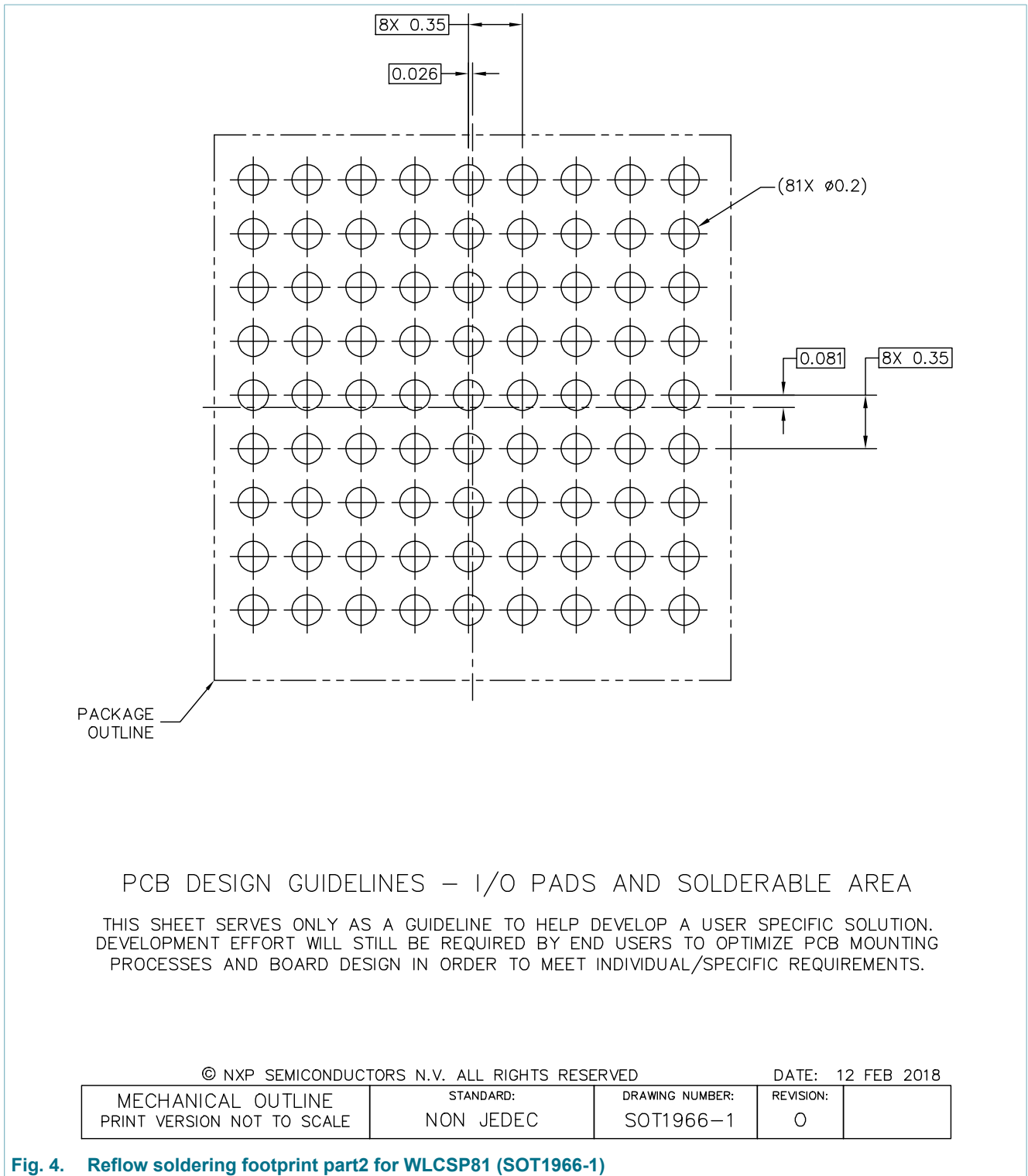
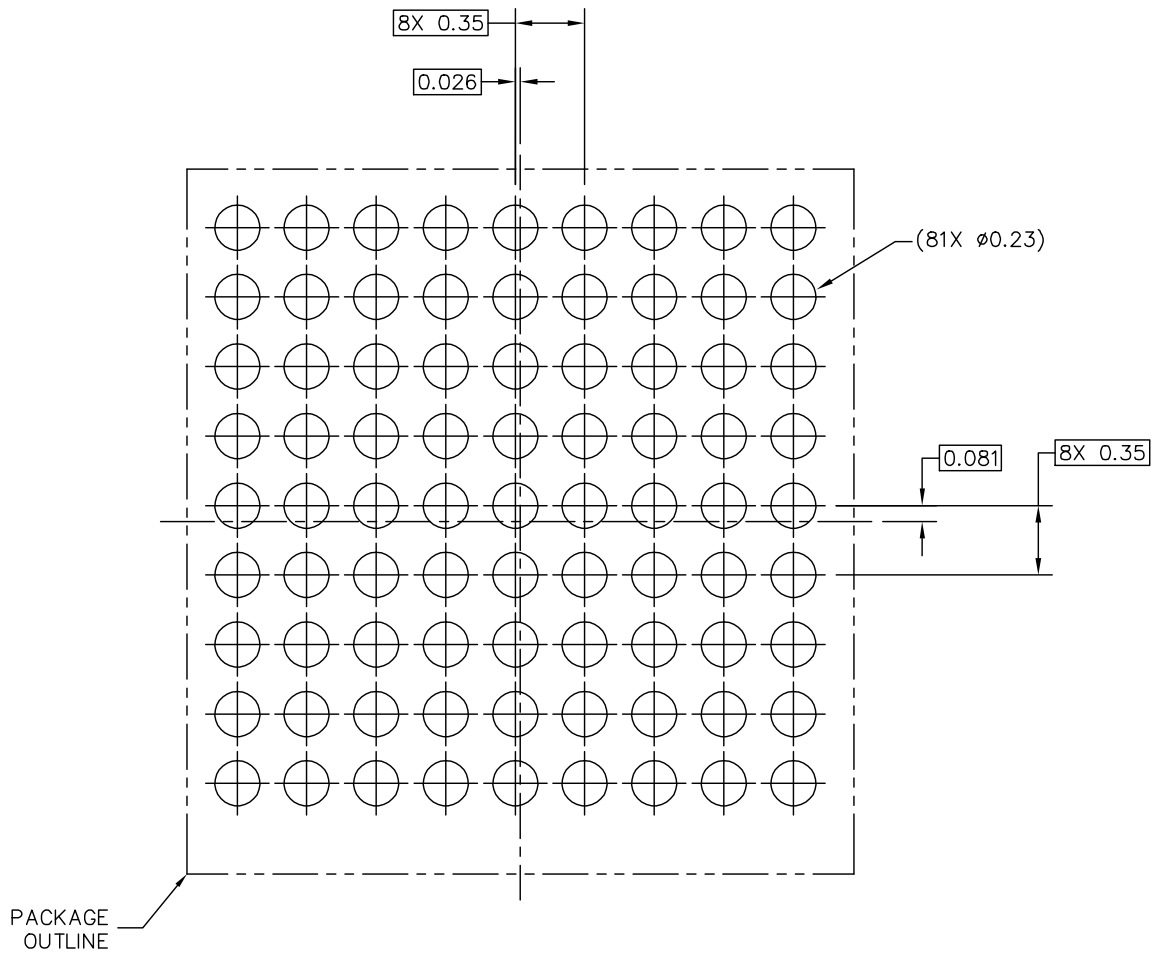


Fig. 4. Reflow soldering footprint part2 for WLCSP81 (SOT1966-1)

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RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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Fig. 5. Reflow soldering footprint part3 for WLCSP81 (SOT1966-1)

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body

## 4. Legal information

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