

SOT1914-2

WLCSP56, wafer level chip-scale package; 56 bumps, 0.4 mm pitch, 3.455 mm x 3.06 mm x 0.495 mm body (backside coating included)

6 May 2020

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP56
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	06-04-2020
Manufacturer package code	98ASA01508D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	3.425	3.455	3.485	mm
package width	3.03	3.06	3.09	mm
seated height	-	0.495	0.53	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	56	-	



WLCSP56, wafer level chip-scale package; 56 bumps, 0.4 mm pitch, 3.455 mm x 3.06 mm x 0.495 mm body (backside coating included)

2 Package outline

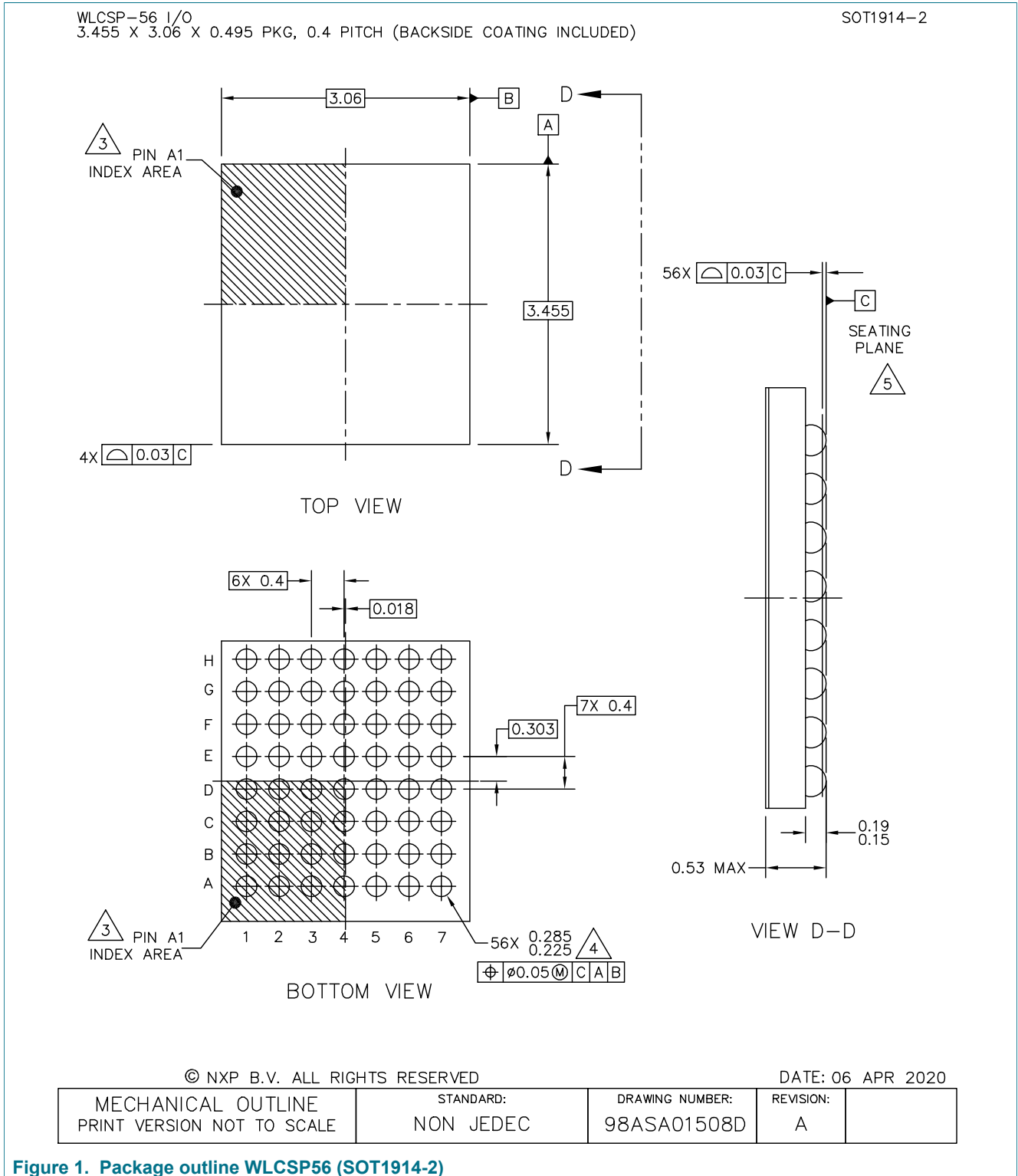
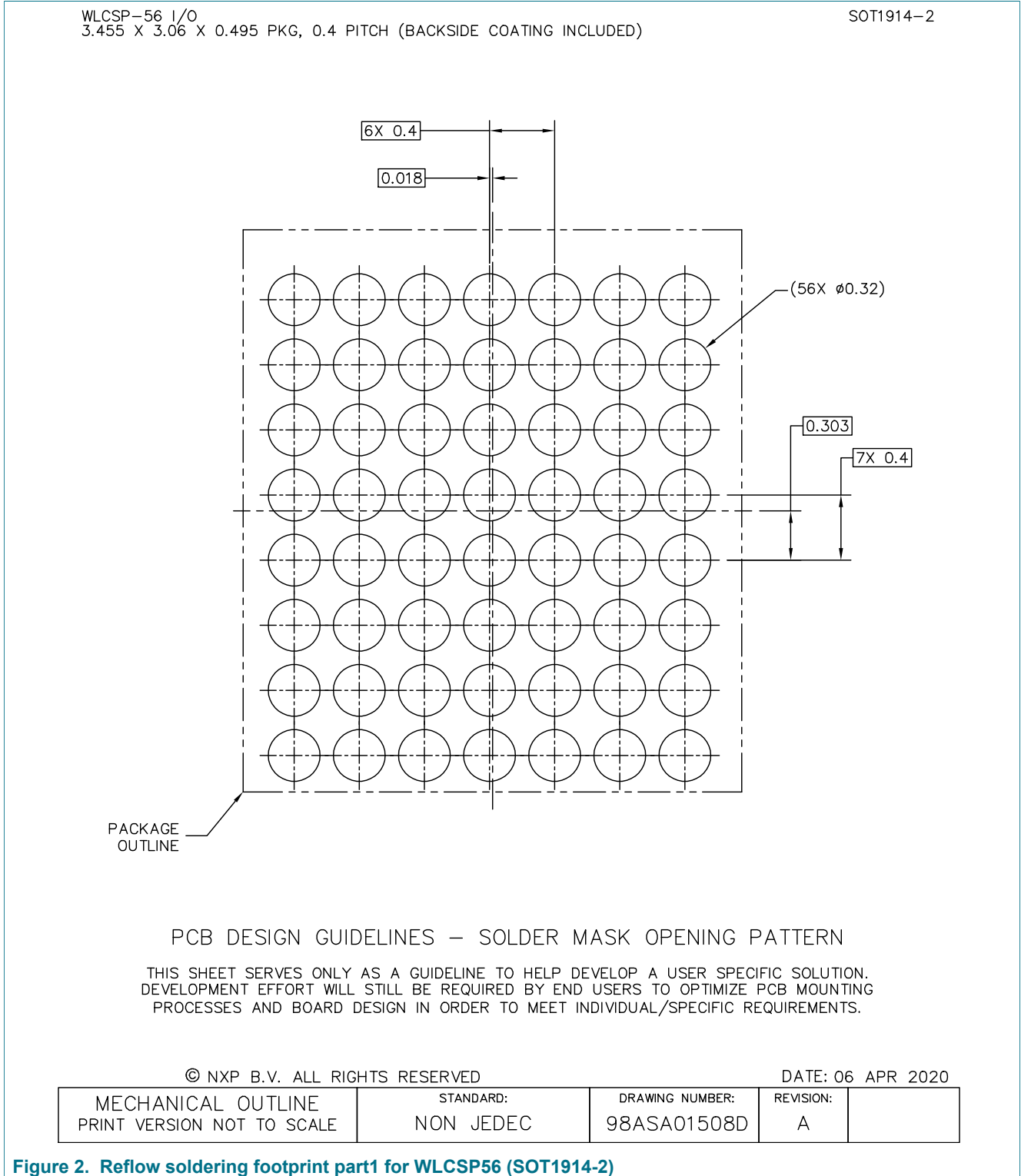


Figure 1. Package outline WLCSP56 (SOT1914-2)

WLCSP56, wafer level chip-scale package; 56 bumps, 0.4 mm pitch, 3.455 mm x 3.06 mm x 0.495 mm body (backside coating included)

3 Soldering



WLCSP56, wafer level chip-scale package; 56 bumps, 0.4 mm pitch, 3.455 mm x 3.06 mm x 0.495 mm body (backside coating included)

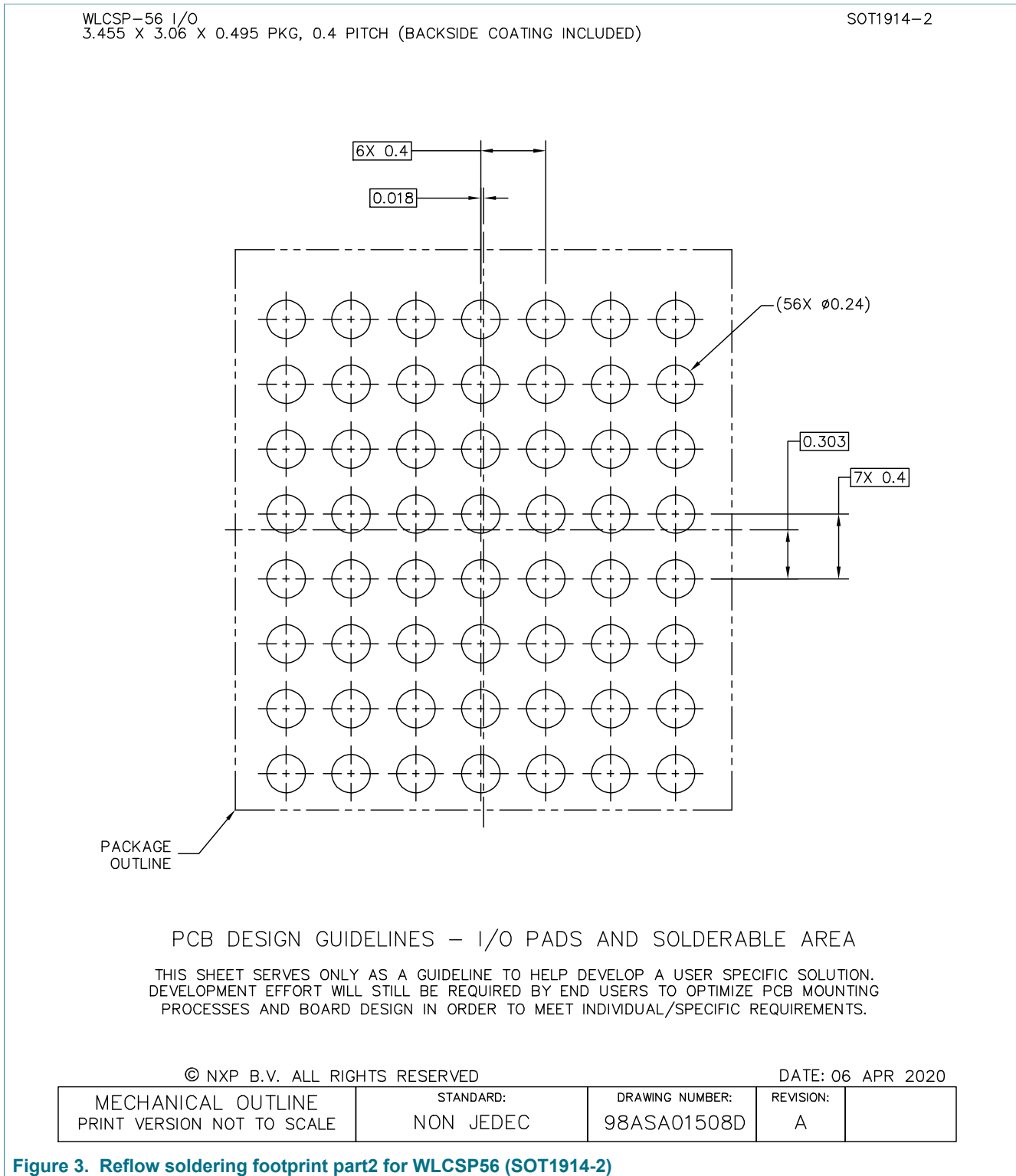
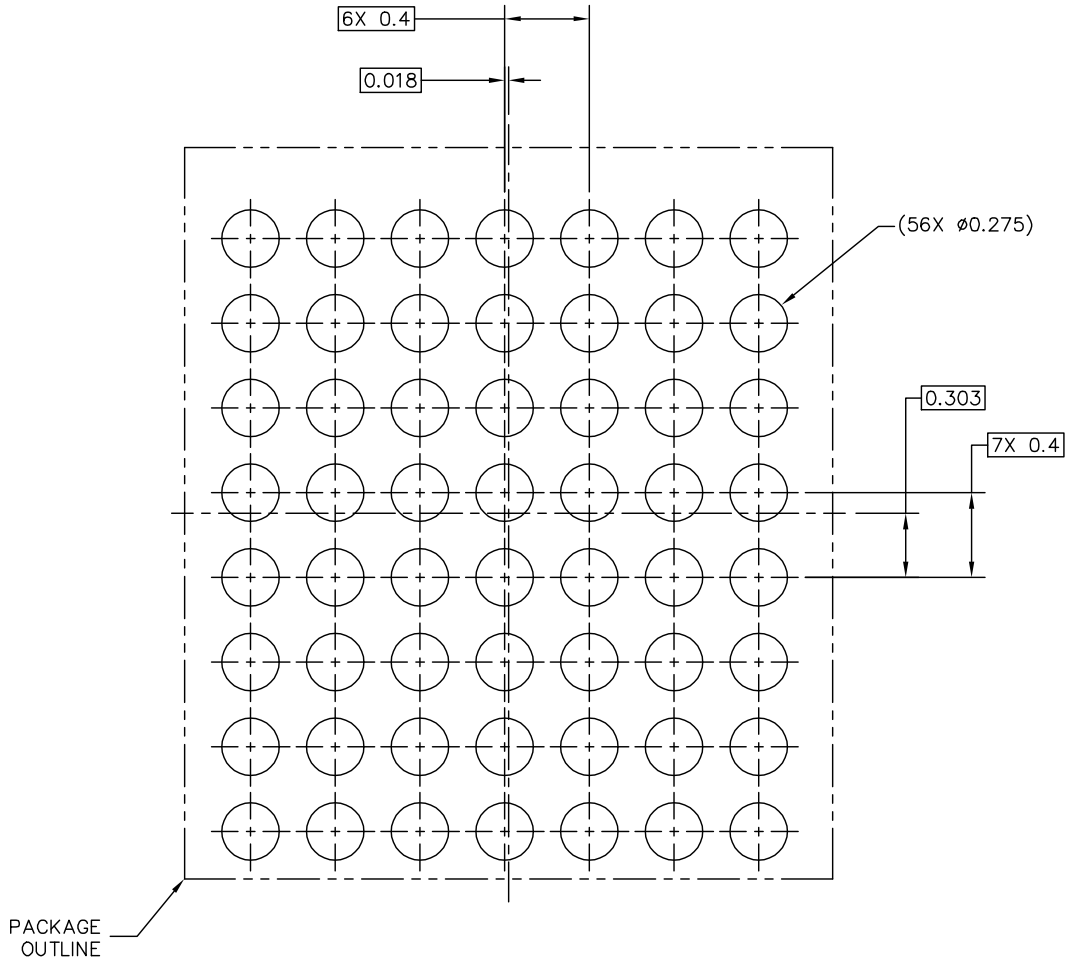


Figure 3. Reflow soldering footprint part2 for WLCSP56 (SOT1914-2)

WLCSP56, wafer level chip-scale package; 56 bumps, 0.4 mm pitch, 3.455 mm x 3.06 mm x 0.495 mm body (backside coating included)

WLCSP-56 I/O
3.455 X 3.06 X 0.495 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1914-2



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 06 APR 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01508D	REVISION: A	
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Figure 4. Reflow soldering footprint part3 for WLCSP56 (SOT1914-2)

WLCSP56, wafer level chip-scale package; 56 bumps, 0.4 mm pitch, 3.455 mm x 3.06 mm x 0.495 mm body (backside coating included)

WLCSP-56 I/O
3.455 X 3.06 X 0.495 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1914-2

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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Figure 5. Package outline note WLCSP56 (SOT1914-2)

WLCSP56, wafer level chip-scale package; 56 bumps, 0.4 mm pitch, 3.455 mm x 3.06 mm x 0.495 mm body (backside coating included)

4 Legal information

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