

SOT1397-10

WLCSP20, wafer level chip-size package, 20 terminals, 0.4 mm pitch, 2.1 mm x 1.7 mm x 0.49 mm body (backside coating included)

25 October 2022

Package information

1 Package summary

Terminal position code B (bottom)

Package type descriptive code WLCSP20

Package style descriptive code WLCSP (wafer level chip-size package)

Package body material type S (silicon)

Mounting method type S (surface mount)

Issue date 07-07-2022

Manufacturer package code 98ASA01955D

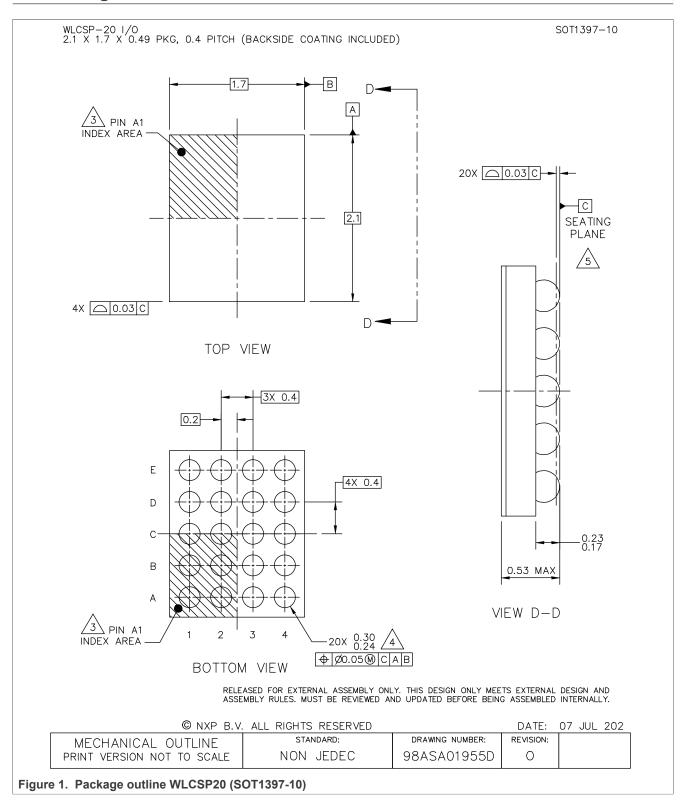
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	2.07	2.1	2.13	mm
package width	1.67	1.7	1.73	mm
seated height	-	0.49	0.53	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	20	-	



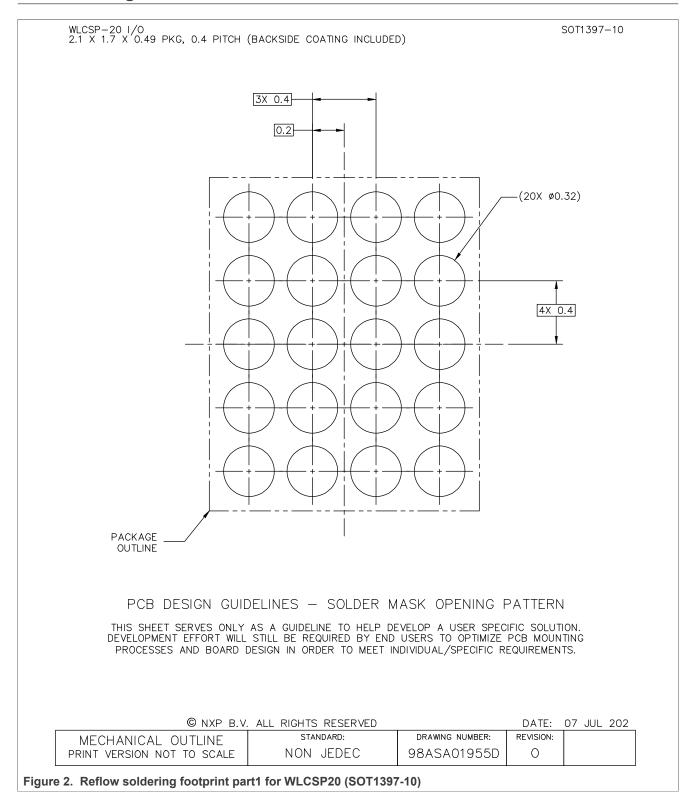
WLCSP20, wafer level chip-size package, 20 terminals, 0.4 mm pitch, 2.1 mm x 1.7 mm x 0.49 mm body (backside coating included)

2 Package outline



WLCSP20, wafer level chip-size package, 20 terminals, 0.4 mm pitch, 2.1 mm x 1.7 mm x 0.49 mm body (backside coating included)

3 Soldering



WLCSP20, wafer level chip-size package, 20 terminals, 0.4 mm pitch, 2.1 mm x 1.7 mm x 0.49 mm body (backside coating included)

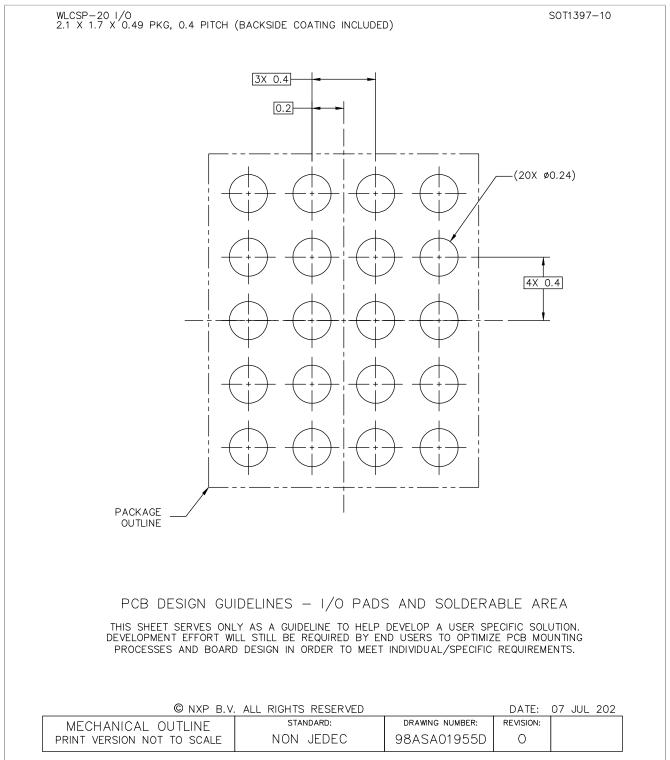


Figure 3. Reflow soldering footprint part2 for WLCSP20 (SOT1397-10)

WLCSP20, wafer level chip-size package, 20 terminals, 0.4 mm pitch, 2.1 mm x 1.7 mm x 0.49 mm body (backside coating included)

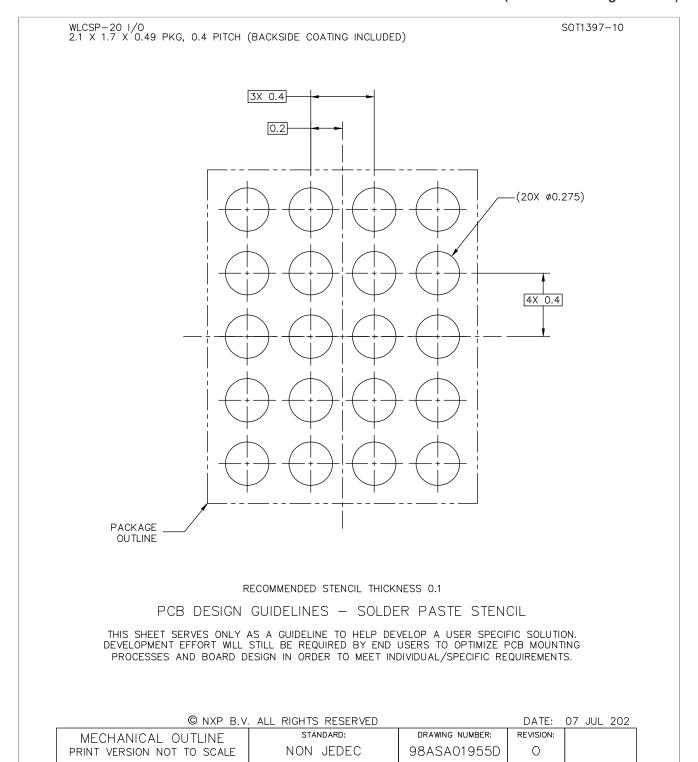


Figure 4. Reflow soldering footprint part3 for WLCSP20 (SOT1397-10)

WLCSP20, wafer level chip-size package, 20 terminals, 0.4 mm pitch, 2.1 mm x 1.7 mm x 0.49 mm body (backside coating included)

WLCSP-20 I/O 2.1 X 1.7 X 0.49 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED) SOT1397-10

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.04.

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MECHANICAL OUTLINE STANDARD: DRAWING NUMBER: REVISION: PRINT VERSION NOT TO SCALE NON JEDEC 98ASA01955D O

Figure 5. Package outline note WLCSP20 (SOT1397-10)

WLCSP20, wafer level chip-size package, 20 terminals, 0.4 mm pitch, 2.1 mm x 1.7 mm x 0.49 mm body (backside coating included)

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