

WLCSP12, wafer level chip scale package; 12 bumps; 0.4 mm pitch; 1.65 mm x 1.25 mm x 0.525 mm body (backside coating included)

24 October 2017

Package information

## 1. Package summary

Terminal position code	B (bottom)		
Package type descriptive code	WLCSP12		
Package type industry code	WLCSP12		
Package style descriptive code	WLCSP (wafer level chip-size package)		
Mounting method type	S (surface mount)		
Issue date	23-10-2017		
Manufacturer package code	SOT1390-8		

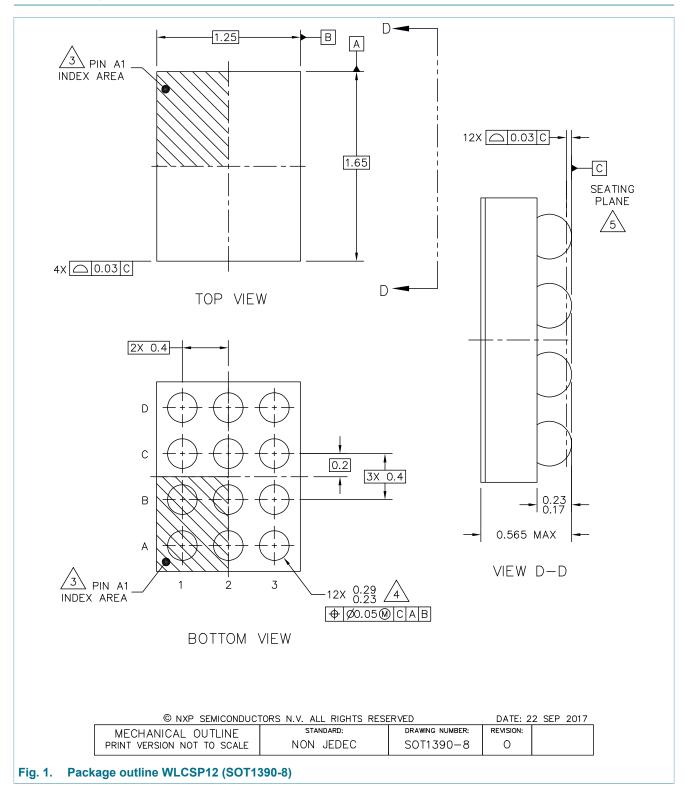
#### Table 1. Package summary

Symbol	Parameter	Min	Тур	Nom	Max	Unit
D	package length	-	-	1.65	-	mm
E	package width	-	-	1.25	-	mm
A	seated height	-	-	0.525	-	mm
e	nominal pitch	-	-	0.4	-	mm
n <sub>2</sub>	actual quantity of termination	-	-	12	-	A/A



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### 2. Package outline



SOT1390-8

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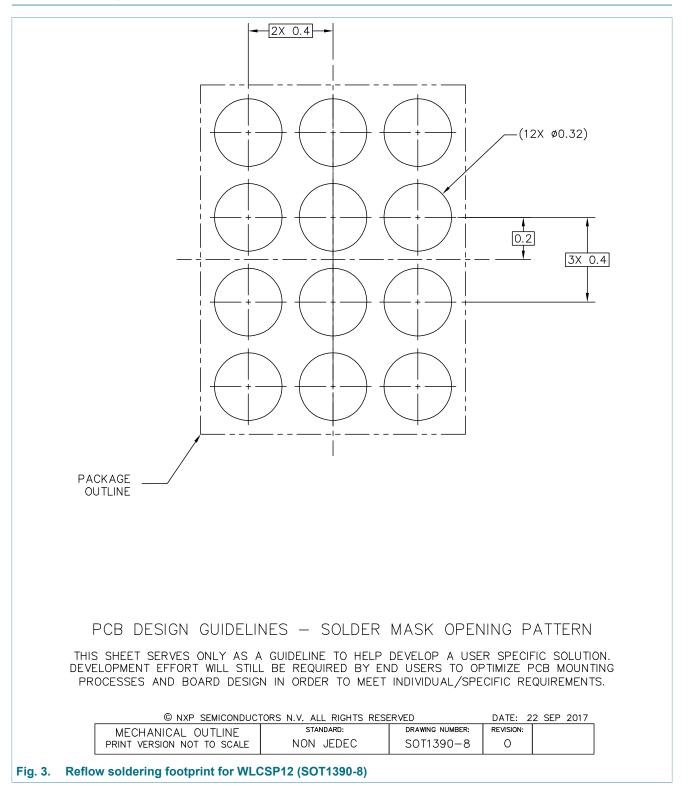
NOTES:							
1. ALL DIMENSIONS IN MILLIMETERS.							
DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.							
$_{\rm A}$ PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.							
$\overline{/4.}$ maximum solder ball diameter measured parallel to datum c.							
$\Delta$ datum c, the seating plane, is determined by the spherical crowns of the solder balls.							
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.							
© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED DATE: 22 SEP 2017 MECHANICAL OUTLINE STANDARD: DRAWING NUMBER: REVISION:							
PRINT VERSION NOT TO SCALE NON JEDEC SOT1390-8 0							
Fig. 2. Package outline note WLCSP12 (SOT1390-8)							

**Package information** 

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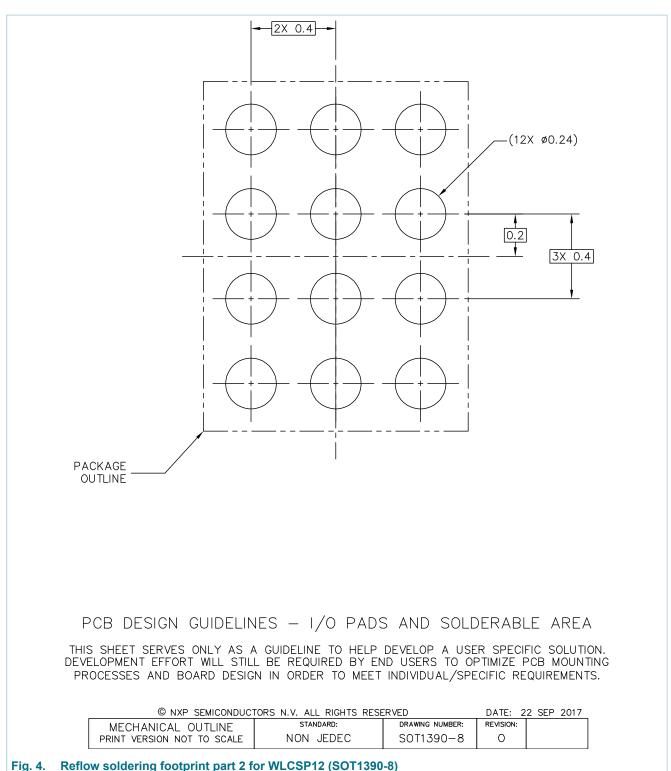
WLCSP12, wafer level chip scale package; 12 bumps; 0.4 mm pitch; 1.65 mm x 1.25 mm x 0.525 mm body (backside coating included)

### 3. Soldering

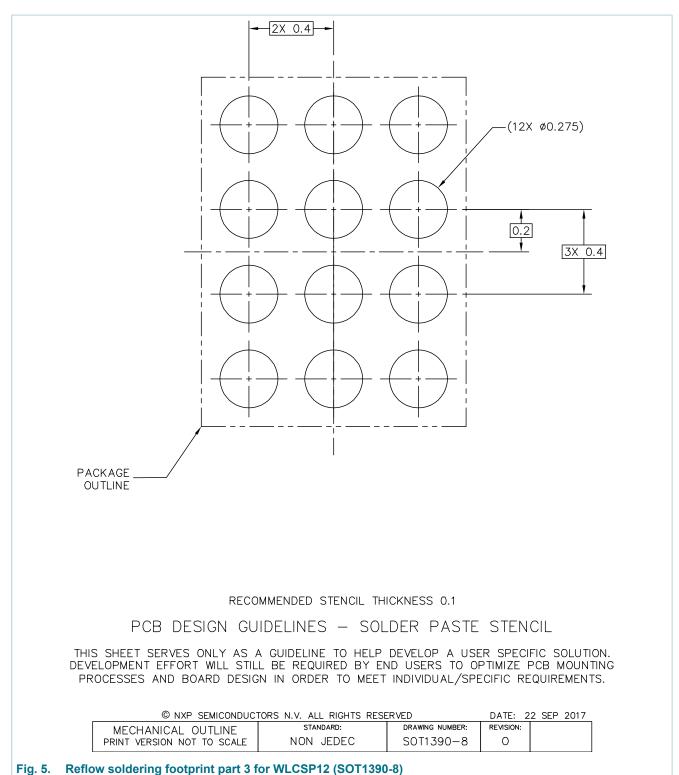


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