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MCXA153VLH_0P07H

Mask Set Errata

Mask Set Errata for Mask 0P07H

Revision History

This report applies to mask 0P07H for these products:

- MCXA152VFT
- MCXA153VLH
- MCXA152VFM
- MCXA143VLH
- MCXA143VFT
- MCXA143VFM
- MCXA142VLH
- MCXA142VFT
- MCXA142VFM
- MCXA153VFT
- MCXA153VFM
- MCXA152VLH

Table 1. Revision History

Revision	Date	Significant Changes
1.0	3/2024	Initial Revision

Errata and Information Summary

Table 2. Errata and Information Summary

Erratum ID	Erratum Title
ERR050501	Core: DFSR.EXTERNAL is not set correctly when waking up from sleep
ERR050502	Core: Execution priority might be wrong for one cycle after AIRCR is changed
ERR051588	LPSPI:Reset transmit FIFO after FIFO underrun by LPSPI Slave.
ERR051629	LPUART:Transmit Complete bit (STAT[TC]) is not set.
ERR051874	I2C clock stretching mode is not supported
ERR052138	Cannot connect to device with JTAG to enter debug if main flash and CMPA are empty (which is the status when device is out of manufacturing)

Known Errata

ERR050501: Core: DFSR.EXTERNAL is not set correctly when waking up from sleep

Description

Cortex-M33 1367266-C:

An external debug event which causes the processor to enter Debug state or the debug monitor should set DFSR.EXTERNAL. It has been found that this field is not set if the event occurs while the processor is asleep.

Workaround

There is no workaround.

ERR050502: Core: Execution priority might be wrong for one cycle after AIRCR is changed

Description

Cortex-M33 1435973-C:

AIRCR is used in the NVIC active tree to calculate the execution priority, which in turn is used to determine fault escalation, exception preemption, and other NVIC-related behaviors. When the active tree is pipelined and there are high latency IRQs active, there might be a glitch in the active tree output for one cycle after AIRCR is changed. The glitch results in NVIC producing wrong execution priority that is neither based on the old AIRCR value nor the new one.

Workaround

There is no workaround for this erratum.

ERR051588: LPSPI:Reset transmit FIFO after FIFO underrun by LPSPI Slave.

Description

Transmit FIFO pointers are corrupted when a transmit FIFO underrun occurs (SR[TEF]) in slave mode.

Workaround

When clearing the transmit error flag (SR[TEF] = 0b1) following a transmit FIFO underrun, reset the transmit FIFO (CR[RTF] = 0b1) before writing any new data to the transmit FIFO.

ERR051629: LPUART:Transmit Complete bit (STAT[TC]) is not set.

Description

When the CTS pin is negated and the CTS feature is enabled (MODIR[TXCTSE] = 0b1) and the TX FIFO is flushed by software then, the Transmit Complete (STAT[TC]) flag is not set.

Workaround

Clear (MODIR[TXCTSE]) bit and reset the transmit FIFO (FIFO[TXFLUSH] = 0b1) when flushing the FIFO with CTS enabled(MODIR[TXCTSE] = 0b1).

ERR051874: I2C clock stretching mode is not supported

Description

I3C IP when working as I2C master mode it doesn't support Clock stretching feature.

Workaround

Application must not use I2C clock stretching feature. It will create clock contention on bus.

I2C Targets on the bus must keep Clock stretching feature disabled.

ERR052138: Cannot connect to device with JTAG to enter debug if main flash and CMPA are empty (which is the status when device is out of manufacturing)

Description

Cannot connect to device with JTAG to enter debug if main flash and CMPA are empty (which is the status when device is out of manufacturing).

Workaround

Use SWD to connect MCU first, after SWD connection establishing, use JTAG connection successfully.

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