SL3S1005

UCODE 9xm

Rev. 3.1 — 12 February 2025 **Product data sheet**

1 General description

The UCODE 9xm is the latest NXP product of the UCODE family supporting user memory. UCODE 9xm offers high performance and features for use in the most demanding RAIN RFID tagging applications.

Due to its exceptional RF performance, UCODE 9xm is particularly well suited for inventory management applications within various industries such as manufacturing, airline baggage tracking and smart logistics. UCODE 9xm enables long read ranges and fast inventory speed of dense RFID tag populations. With its broadband design, UCODE 9xm offers both the foundation for truly global RAIN RFID labels whilst providing the additional memory required for today's demanding RFID applications.

2 Features and benefits

2.1 Key features

- Read sensitivity -24 dBm
- Write sensitivity -22 dBm
- Innovative functionality
  - Customer configurable EPC/User Memory size
  - Self-Adjust
  - Memory Safeguard
  - Brand Identifier
  - Standardized Untraceable
  - Pre-serialization of 96-bit EPC
- Compatible with single-slit antenna
- EPC Gen2v2.1

2.2 Memory

- Up to 496-bit of EPC memory
- Up to 752-bit of user memory
- Pre-serialized 96-bit EPC
- 96-bit Factory locked Tag Identifier (TID)
- 48-bit unique serial number factory-encoded into TID
- 32-bit kill password to permanently disable the tag
- 32-bit access password
- Wide operating temperature range: -40 °C up to +85 °C
- Minimum 100k write cycle endurance

2.3 Supported features

- All mandatory commands of the EPC Gen2v2.1 specification are implemented including:
  - Kill command
- The following optional commands are implemented in conformance with the EPC Gen2v2.1:
  - BlockWrite (2 words, 32-bit)
  - Blockpermalock (128-bit)
  - Untraceable including read range reduction
  - Access command
- Self-Adjust for automated tag performance optimization
- Brand Identifier: enables product authentication verification

All supported features of the UCODE 9xm can be activated using standard EPCglobal READ / WRITE / ACCESS / SELECT commands. No custom commands are needed to take advantage of any of the features.

3 Applications

3.1 Target markets

- Industrial applications
- Logistics
- Automotive
- Aviation
- Healthcare

3.2 Applications

- Supply chain management
- Inventory management
- Asset tracking
- Production tracking
- Product life-cycle management
- Aerospace
- Tire tagging
- Waste management
- Pharmaceutical
- Healthcare
- Brand protection

The above non-exhaustive lists show some of the target markets for UCODE 9xm, however, this product is applicable for many other industries and use cases where exceptional performance coupled with user memory is required. Please contact NXP Semiconductors for further support.

4 Ordering information

Table 1. Ordering information

Type number	Package			
	Name	IC type	Description	Version
SL3S1005FUD2/HAP	Wafer	UCODE 9xm	Die on sawn 12" 120 µm wafer 10 µm polyimide spacer with large pads, plasma diced	not applicable

5 Block diagram

The UCODE 9xm IC consists of three major blocks:

- Analog interface
- Digital control
- EEPROM

The analog part provides stable supply voltage and demodulates data received from the reader which is then processed by the digital part. Further, the modulation transistor of the analog part transmits data back to the reader.

The digital section includes the state machines, processes the protocol, and handles communication with the EEPROM, which contains the EPC and the user data.

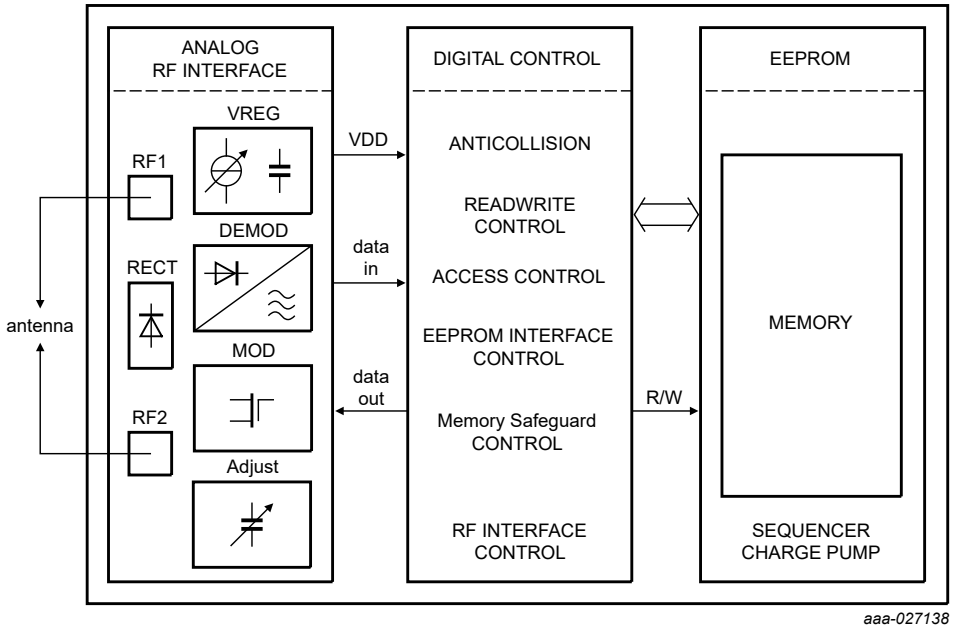


Figure 1. Block diagram of UCODE 9xm IC

6 Pinning information

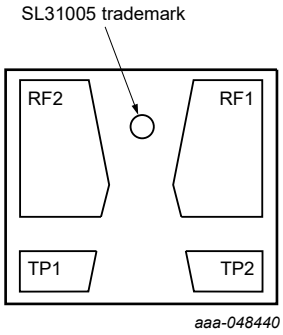


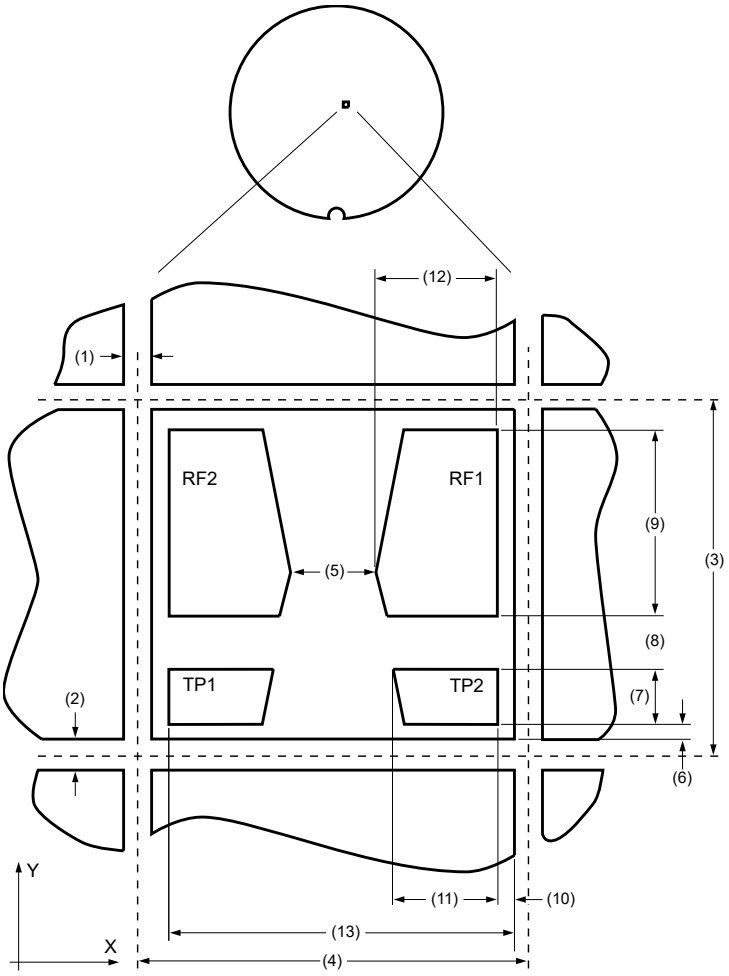
Figure 2. Pinning bare die

6.1 Pin description

Table 2. Pin description bare die

Symbol	Description
TP1	test pad 1
RF1	antenna connector 1
TP2	test pad 2
RF2	antenna connector 2

7 Wafer layout



1. Die to die distance (metal sealring - metal sealring) 16.6 µm, (X-scribe line width: 8.6 µm)
2. Die to die distance (metal sealring - metal sealring) 16.6 µm, (Y-scribe line width: 8.6 µm)
3. Chip step, Y-length: 533.6 µm
4. Chip step, X-length: 518.6 µm
5. Bump to bump distance X (RF1 - RF2): 115 µm
6. Distance bump to metal sealring Y: 17.5 µm
7. Bump size (TP1, TP2) Y: 70.5 µm
8. Bump to bump distance Y (RF1 - TP2, RF2 - TP1): 50 µm
9. Bump size (RF1, RF2) Y: 361.5 µm
10. Distance bump to metal sealring X: 17.5 µm
11. Bump size (TP1, TP2) X: 160.1 µm
12. Bump size (RF1, RF2) X: 176 µm
13. Distance bump to metal sealring Y: 484.5µm

Figure 3. UCODE 9xm plasma diced, 12" wafer layout

8 Mechanical specification

UCODE 9xm wafers are available in 120 µm thickness. The 120 µm thick wafer includes a 10 µm Polyimide spacer resulting in less coupling between the antenna and the active circuit, leaving more room for process control (for example, pressure).

8.1 Wafer specification

8.1.1 12-inch wafer

See [3].

Table 3. 12-inch specification, plasma diced

Wafer	
Designation	each wafer is scribed with batch number and wafer number
Diameter	300 mm (12") unsawn
Thickness	120 µm ± 15 µm
Number of pads	4
Pad location	nondiagonal / placed in chip corners
Process	CMOS 0.14 µm
Batch size	25 wafers
Net printed dies per wafer	242104
Wafer backside	
Material	Si
Treatment	ground and stress release
Roughness	R_a max. 0.5 µm, R_t max. 5 µm
Chip dimensions	
Die size excluding scribe	0.525 mm × 0.51 mm = 0.268 mm^2
Scribe line width:	X-dimension = 8.6 µm
	Y-dimension = 8.6 µm
Passivation on front	
Type	Sandwich structure
Material	PE-Oxide (on top)
Thickness	2.25 µm total thickness of passivation
Polyimide spacer	10 µm ± 2 µm
Au pads	
Pad material	> 99.9 % pure Au
Pad hardness	35 – 80 HV 0.005
Pad shear strength	> 70 MPa
Pad height	3 µm

Table 3. 12-inch specification, plasma diced*...continued*

Pad height uniformity	
– within a die	max. 2 µm
– within a wafer	max. 4 µm
Pad flatness	max. 3 µm
Pad size	
– RF1, RF2 (max. details see wafer layout)	176 µm × 361.5 µm
– TP1, TP2 (max. details see wafer layout)	160 µm × 70.5 µm
Pad size variation	± 5 µm

8.1.2 Fail die identification

No ink dots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See [3].

8.1.3 Map file distribution

See [3].

9 Functional description

9.1 Air interface standards

The UCODE 9xm fully supports all parts of the "EPC™ Radio-Frequency Identity Protocols Generation-2 UHF RFID, Specification for RFID Air Interface, Protocol for Communications at 860 MHz to 960 MHz, Version 2.1" [1].

9.2 Power transfer

The interrogator provides an RF field that powers the tag, equipped with a UCODE 9xm. The antenna transforms the impedance of free space to the chip input impedance in order to get the maximum power for the UCODE 9xm on the tag.

The RF field, which is oscillating on the operating frequency provided by the interrogator, is rectified to provide a smoothed DC voltage to the analog and digital modules of the IC.

The antenna that is attached to the chip may use a DC connection between the two antenna pads. Therefore the UCODE 9xm also enables loop antenna design.

9.3 Data transfer

9.3.1 Interrogator to tag link

An interrogator transmits information to the UCODE 9xm by modulating an UHF RF signal. The UCODE 9xm receives both information and operating energy from this RF signal. Tags are passive, meaning that they receive all of their operating energy from the interrogator's RF waveform.

An interrogator is using a fixed modulation and data rate for the duration of at least one inventory round. It communicates to the UCODE 9xm by modulating an RF carrier.

For further details, refer to [1].

9.3.2 Tag to interrogator link

Upon transmitting a valid command, an interrogator receives information from a UCODE 9xm tag by transmitting an unmodulated RF carrier and listening for a backscattered reply. The UCODE 9xm backscatters by switching the reflection coefficient of its antenna between two states in accordance with the data being sent. For further details, refer to [1].

The UCODE 9xm communicates information by backscatter-modulating the amplitude and/or phase of the RF carrier. Interrogators shall be capable of demodulating either demodulation type.

The encoding format, selected in response to interrogator commands, is either FM0 baseband or Miller-modulated subcarrier.

9.4 Supported commands

UCODE 9xm supports all **mandatory** EPC Gen2v2.1 commands.

In addition, the UCODE 9xm supports the following **optional** commands:

- Access
- Block Write (32 bit on even addresses)
- Blockpermalock (128 bit)
- Untraceable including read range reduction

9.5 UCODE 9xm memory

The UCODE 9xm memory is implemented according to EPC Gen2v2.1:

Table 4. UCODE 9xm memory sections

Name	Size	Bank
Reserved memory (32-bit Kill password and 32-bit access password)	64 bit	00b
EPC (excluding 16-bit CRC-16 and 16-bit PC)	128 / 256 / 496 bit	01b
TID (including permalocked unique 48-bit serial number)	96 bit	10b
UCODE 9xm configuration word	16 bit	10b
USER	752 / 624 / 384 bit	11b

The logical address of all memory banks begins at zero (00h).

In addition to the four memory banks, one configuration word to handle the UCODE 9xm specific features is available at TID bank 10 address bit-70h.

The configuration word is described in detail in Section 9.6.1.

The EPC/UM configuration is described in detail in Section 9.6.2.

The TID complies with the GS1 EPC Tag Data Standard. See [2].

The initial value of the Kill- and Access-password is 0000h. It is recommended to use diversified passwords for tag populations.

9.5.1 UCODE 9xm overall memory map

Table 5. UCODE 9xm memory map 128-bit EPC / 752-bit UM

Bank	Address	Type	Content	Initial	Remark
Bank 00	00h to 1Fh	reserved	Kill password	all 00h	unlocked memory
	20h to 3Fh	reserved	Access password	all 00h	unlocked memory
Bank 01 EPC	00h to 0Fh	EPC	CRC-16: refer to [1]		memory mapped calculated CRC
	10h to 14h	EPC	EPC length	00110b	unlocked memory
	15h	EPC	UMI	1b	hardwired to 1
	16h	EPC	XPC indicator	0b	hardwired to 0
	17h to 1Fh	EPC	numbering system indicator	00h	unlocked memory
	20h to 9Fh	EPC	EPC	[1]	unlocked memory
Bank 10 TID	00h to 07h	TID	allocation class identifier	1110 0010b	locked memory
	08h to 13h	TID	tag mask designer identifier	1000 0000 0110b	locked memory
	14h	TID	config word indicator	1b[2]	locked memory
	15h to 1Fh	TID	tag model number	TMNR[3]	locked memory
	20h to 2Fh	TID	XTID header	2000h	locked memory
	30h to 5Fh	TID	serial number	SNR	locked memory
Bank 10 Config Word	70h	TID	RFU	0b	locked memory
	71h	TID	Read NOK	0b	indicator bit
	72h	TID	EPC NOK	0b	indicator bit
	73h	TID	RFU	0b	locked memory
	74h	TID	Brand Identifier	0b	action bit
	75h	TID	RFU	0b	locked memory
	76h	TID	RFU	0b	locked memory
	77h	TID	Self-Adjust disable	0b	permanent bit[4]
	78h	TID	Dynamic backscatter	0b	permanent bit[4]
	79h	TID	min. backscatter strength	0b	permanent bit[4]
	7Ah	TID	RFU	0b	locked memory
	7Bh	TID	RFU	0b	locked memory
	7Ch	TID	RFU	0b	locked memory
	7Dh	TID	RFU	0b	locked memory
	7Eh	TID	Mem Config1	0b	permanent bit[4]
	7Fh	TID	Mem Config0	0b	permanent bit[4]
Bank 11 USER	000h - 2EFh	USER	User memory	undefined	unlocked memory

[1] `HEX E280 6897 0000 nnnn nnnn nnnn 0000 0000` where `n` are the nibbles of the SNR from the TID
[2] Indicates the existence of a Configuration Word at the end of the TID number
[3] See Figure 4
[4] Permanent bit: permanently stored bits in the memory, see Section 9.6.1

Table 6. UCODE 9xm memory map 256-bit EPC / 624-bit UM

Bank	Address	Type	Content	Initial	Remark
Bank 00	00h to 1Fh	reserved	Kill password	all 00h	unlocked memory
	20h to 3Fh	reserved	Access password	all 00h	unlocked memory
Bank 01 EPC	00h to 0Fh	EPC	CRC-16: refer to [1]		memory mapped calculated CRC
	10h to 14h	EPC	EPC length	00110b	unlocked memory
	15h	EPC	UMI	1b	hardwired to 1
	16h	EPC	XPC indicator	0b	hardwired to 0
	17h to 1Fh	EPC	numbering system indicator	00h	unlocked memory
	20h to 11Fh	EPC	EPC	[1]	unlocked memory
Bank 10 TID	00h to 07h	TID	allocation class identifier	1110 0010b	locked memory
	08h to 13h	TID	tag mask designer identifier	1000 0000 0110b	locked memory
	14h	TID	config word indicator	1b[2]	locked memory
	15h to 1Fh	TID	tag model number	TMNR[3]	locked memory
	20h to 2Fh	TID	XTID header	2000h	locked memory
	30h to 5Fh	TID	serial number	SNR	locked memory
Bank 10 Config Word	70h	TID	RFU	0b	locked memory
	71h	TID	Read NOK	0b	indicator bit
	72h	TID	EPC NOK	0b	indicator bit
	73h	TID	RFU	0b	locked memory
	74h	TID	Brand Identifier	0b	action bit
	75h	TID	RFU	0b	locked memory
	76h	TID	RFU	0b	locked memory
	77h	TID	Self-Adjust disable	0b	permanent bit[4]
	78h	TID	Dynamic backscatter	0b	permanent bit[4]
	79h	TID	min. backscatter strength	0b	permanent bit[4]
	7Ah	TID	RFU	0b	locked memory
	7Bh	TID	RFU	0b	locked memory
	7Ch	TID	RFU	0b	locked memory
	7Dh	TID	RFU	0b	locked memory
	7Eh	TID	Mem Config1	0b	permanent bit[4]
	7Fh	TID	Mem Config0	1b	permanent bit[4]
Bank 11 USER	000h - 26Fh	USER	User memory	undefined	unlocked memory

[1] `HEX E280 6897 0000 nnnn nnnn nnnn 0000 0000` where `n` are the nibbles of the SNR from the TID
[2] Indicates the existence of a Configuration Word at the end of the TID number
[3] See Figure 4
[4] Permanent bit: permanently stored bits in the memory, see Section 9.6.1

Table 7. UCODE 9xm memory map 496-bit EPC / 384-bit UM

Bank	Address	Type	Content	Initial	Remark
Bank 00	00h to 1Fh	reserved	Kill password	all 00h	unlocked memory
	20h to 3Fh	reserved	Access password	all 00h	unlocked memory
Bank 01 EPC	00h to 0Fh	EPC	CRC-16: refer to [1]		memory mapped calculated CRC
	10h to 14h	EPC	EPC length	00110b	unlocked memory
	15h	EPC	UMI	1b	hardwired to 1
	16h	EPC	XPC indicator	0b	hardwired to 0
	17h to 1Fh	EPC	numbering system indicator	00h	unlocked memory
	20h to 20Fh	EPC	EPC	[1]	unlocked memory
Bank 10 TID	00h to 07h	TID	allocation class identifier	1110 0010b	locked memory
	08h to 13h	TID	tag mask designer identifier	1000 0000 0110b	locked memory
	14h	TID	config word indicator	1b[2]	locked memory
	15h to 1Fh	TID	tag model number	TMNR[3]	locked memory
	20h to 2Fh	TID	XTID header	2000h	locked memory
	30h to 5Fh	TID	serial number	SNR	locked memory
Bank 10 Config Word	70h	TID	RFU	0b	locked memory
	71h	TID	Read NOK	0b	indicator bit
	72h	TID	EPC NOK	0b	indicator bit
	73h	TID	RFU	0b	locked memory
	74h	TID	Brand Identifier	0b	action bit
	75h	TID	RFU	0b	locked memory
	76h	TID	RFU	0b	locked memory
	77h	TID	Self-Adjust disable	0b	permanent bit[4]
	78h	TID	Dynamic backscatter	0b	permanent bit[4]
	79h	TID	min. backscatter strength	0b	permanent bit[4]
	7Ah	TID	RFU	0b	locked memory
	7Bh	TID	RFU	0b	locked memory
	7Ch	TID	RFU	0b	locked memory
	7Dh	TID	RFU	0b	locked memory
	7Eh	TID	Mem Config1	1b	permanent bit[4]
	7Fh	TID	Mem Config0	0b	permanent bit[4]
Bank 11 USER	000h - 17Fh	USER	User memory	undefined	unlocked memory

[1] `HEX E280 6897 0000 nnnn nnnn nnnn 0000 0000` where `n` are the nibbles of the SNR from the TID
[2] Indicates the existence of a Configuration Word at the end of the TID number
[3] See Figure 4
[4] Permanent bit: permanently stored bits in the memory, see Section 9.6.1

9.5.2 UCODE 9xm TID memory details

	First 48 bit of TID memory	Class ID	Mask Designer ID	Model Number			XTID Header
				Config Word Indicator	Sub Version Nr.	Version (Silicon) Nr.	
UCODE 9xm	E28068972000	E2h	806h	1b	0001b	0010111b	2000h

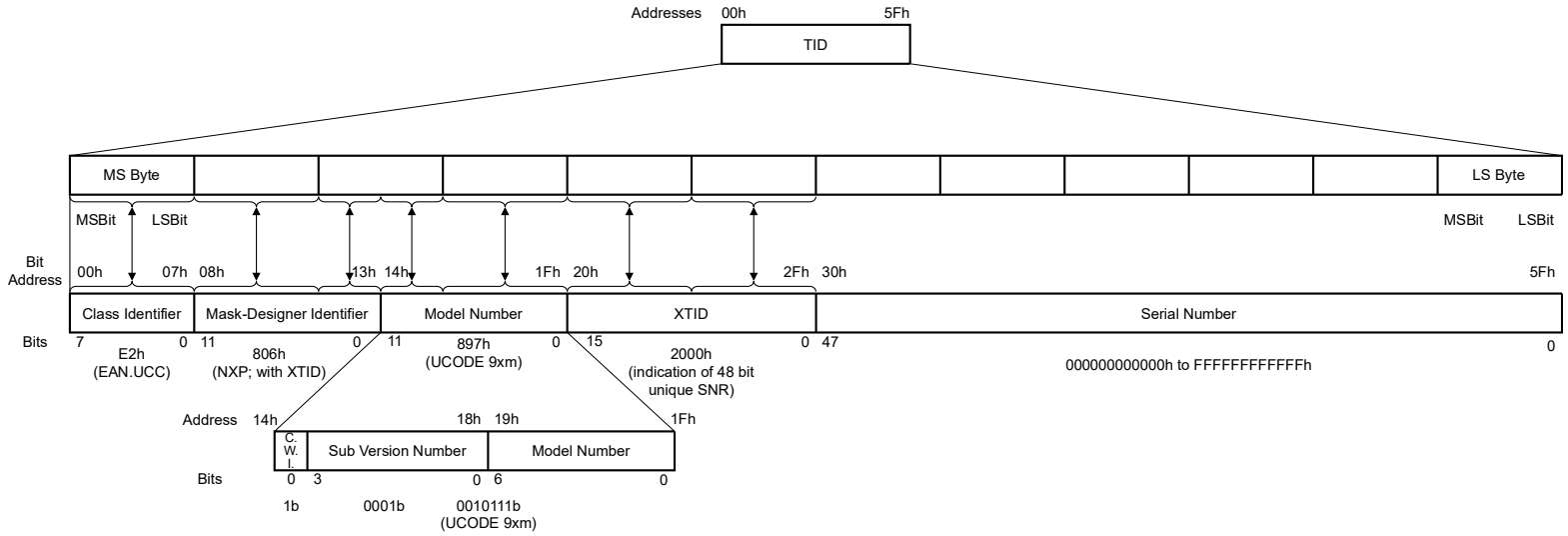


Figure 4. UCODE 9xm TID memory structure

9.6 Supported features

The UCODE 9xm is equipped with a number of additional features. They are implemented in such a way that standard EPCglobal READ / WRITE / ACCESS / SELECT commands can be used to operate these features.

The Configuration Word, as mentioned in the memory map, controls the additional features at address 70h of the TID memory bank.

9.6.1 UCODE 9xm features control mechanism

The different features of the UCODE 9xm can be activated / de-activated by addressing or changing the content of the corresponding bit in the configuration word at address 70h in the TID memory bank (Table 8). The de-activation of the action bit feature will only happen after chip reset.

Table 8. Configuration word UCODE 9xm

Locked memory	Indicator bit		Locked memory	Action bit	Locked memory		Permanent bit
RFU	Read NOK	EPC NOK	RFU	Brand Identifier	RFU	RFU	Self-Adjust disable
0	1	2	3	4	5	6	7

Table 9. Configuration word UCODE 9xm ... continued

Permanent bit	Permanent bit	Locked memory				Permanent bit	
Dynamic backscatter	min.backscatter strength	RFU	RFU	RFU	RFU	MemConfig1	MemConfig0
8	9	10	11	12	13	14	15

The configuration word contains 3 different type of bits:

- **Indicator bit**: cannot be changed by command
  Read NOK
  EPC NOK
- **Action bit**: meant to trigger a feature upon a SELECT command on the related bit:
  Brand Identifier
- **Permanent bits**: permanently stored bits in the memory
  Self-Adjust disable
  Dynamic backscatter
  Min. Backscatter Strength
  MemConfig1/MemConfig0

A change of the permanent bits Configuration word is **not** possible under the following conditions:

- EPC or user memory is either locked, permalocked or permaunlocked
- Permalock of a block in the user memory
- EPC or user memory hidden by the Untraceable command

9.6.2 UCODE 9xm memory configuration

UCODE 9xm supports three memory configurations for EPC and USER memory selectable by customer:

1. 128-bit EPC / 752-bit USER
2. 256-bit EPC / 624-bit USER (default configuration at delivery)
3. 496-bit EPC / 384-bit USER

The Configuration word of UCODE 9xm is located in the Memory Bank ‘10’ (TID), starting at address 70h.

The EPC/USER memory configuration is done by the Configuration word bits 7Eh (MemConfig1) and 7Fh (MemConfig0).

The configuration can be changed until a lock is performed. For details see Section 9.6.1.

Table 10. UCODE 9xm memory configuration

MemConfig1	MemConfig0	EPC Bank size	UM Bank size
0	0	128 bit	752 bit
0	1	256 bit	624 bit
1	0	496 bit	384 bit
1	1	do not use	do not use

9.6.3 Untraceable

The EPC Gen2v2.1 Untraceable command allows the UCODE 9xm to hide the complete or parts of the EPC, TID and/or user memory. In addition, the read range can be completely or temporarily reduced.

This command can only be executed from the secured state.

Memory parts which are set untraceable are acting as non-existing.

EPC-field:

Specifies the number of words of the EPC memory which the UCODE 9xm back scatters. A change of this field therefore also changes the L bit in the Protocol Control (PC) word.

TID-field:

Hide some ("01") hides the TID memory from address 20h (included) onwards.

Range-field:

In case of activated range toggling, the read range reduction toggles from the actual value to the second. (e.g. when actual state is normal it toggles to reduced). In case of power loss, the chip reverts to its prior state. At activation of this feature the chip checks if sufficient power would be available, in case range reduction would be active, to communicate with the tag. Only in case this condition is ensured the feature will be activated.

UCODE 9xm does not support the U bit and therefore ignores this value.

Table 11. Untraceable command

	Command	RFU	U	EPC	TID	User	Range	RN	CRC
No. of bits	16	2	1	6	2	1	2	16	16
Description	1110 0010 0000 0000	00	do not care	MSB: "0": show memory above EPC "1": hide memory above EPC 5 LSBs: New EPC length	"00": hide none "01": hide some "10": hide all "11": RFU	"0": view "1": hide	"00": normal "01": toggle "10": reduced "11": RFU	handle	CRC-16

9.6.4 Self-Adjust

9.6.4.1 Description

The UCODE 9xm has an automatic mechanism implemented which adjusts the chip sensitivity to a maximum in the operated environment. This adjustment will be performed at startup and selects between three different input capacitance values (center capacitance -60 fF / +100 fF). The feature is enabled by default, but can also be deactivated by the config word bit 77h (Self-Adjust disable). In case of deactivation, the center capacitance is used.

9.6.5 Dynamic backscatter

9.6.5.1 Description

UCODE 9xm provides the Dynamic backscatter feature in addition to the standard UCODE backscatter control. The three modes can be controlled by modifying bit 78h and bit 79h within the configuration word. Per default, minimum backscatter is disabled in order to achieve maximum read rates. In case backscatter strength reduction is necessary, nominal backscatter strength can be selected.

The Dynamic backscatter mode enables maximum backscatter at low chip power levels and gradually reduces the backscatter strength at high-power levels enabling the best performance and also meet regulatory limits.

Table 12. Backscatter Control

Dynamic Backscatter Bit	Min. Backscatter Bit	Description
0	0	Maximum backscatter
0	1	Minimum backscatter
1	0	Maximum backscatter
1	1	Dynamic backscatter

9.6.6 Memory safeguard

9.6.6.1 Description

The Memory safeguard of UCODE 9xm implements two separate countermeasures which ensure integrity of the stored data:

ECC (Error correction code):

The implemented ECC is applied on the complete UCODE 9xm memory and requires no user action. With this feature, a single bit failure in the memory is detected and corrected automatically. In case of 2-bit fail, an indication as described below is given.

EPC Memory:

Config word bit 02h (EPC NOK) provides an indication that a 2-bit failure occurred in the EPC memory by changing its value to "1". In such a case, UCODE 9xm responds with an EPC value of F's indicating a corrupted EPC. A read of the EPC memory content provides the actual content.

All Memories:

Config word bit 01h (Read NOK) provides an indication on the last EPC READ command, that a 2-bit failure occurred in Reserved, User, EPC, or TID Memory by changing its value to "1".

Parity check:

A parity check on the TID is implemented to offer the possibility to identify a change in the TID. The parity bit (Even parity) will be calculated and locked in the manufacturing process. For a check, the TID content needs to be read out and parity checked.

9.6.7 Brand Identifier

9.6.7.1 Description

The feature allows brand owners to implement a product originality check option for their products. The customer dedicated unique 16-bit brand identifier is programmed during manufacturing process by NXP and therefore unalterable stored in the memory.

A SELECT command on bit 74h (Brand Identifier) in the configuration word triggers the UCODE 9xm to respond in the inventory round with PC + EPC + Brand Identifier + CRC.

In order to prevent manipulation, the Brand Identifier is scrambled with the RN16 and not sent in plain. The implemented scrambling is performed by bitwise XOR operation of the 16-bit Brand Identifier and the RN16. At the reader, the Brand identifier can be descrambled and the originality check completed.

The PC value is adjusted accordingly for UCODE 9xm. A SELECT on the Brand Identifier bit always gives a Tag matching. The usage of this feature requires an update on the reader firmware with the Brand Identifier check routine.

Default value of the UCODE 9xm Brand Identifier is "AAAAh".

Customer-specific Brand Identifiers can be requested by a dedicated product ordering code. For details, contact your NXP sales representative.

9.6.8 Pre-serialization of the 96-bit EPC

9.6.8.1 Description

UCODE 9xm is delivered with a pre-serialized content of the 96-bit EPC, which is the initial programmed length of the EPC.

The EPC content is identical to the TID content except for the 16-bit XTID content which is set to 16-bit 0's.

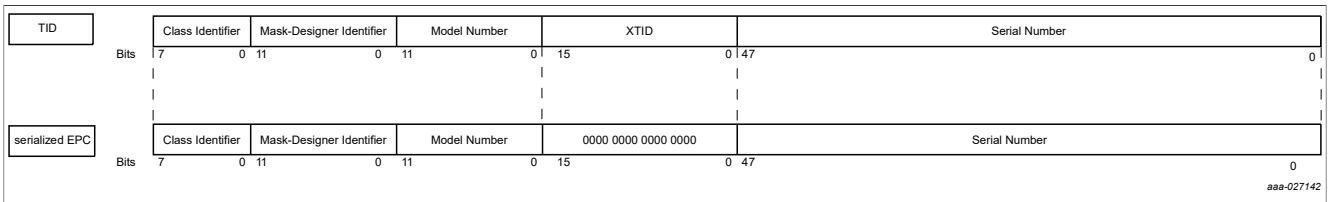


Figure 5. Pre-serialization of 96-bit EPC

9.6.9 Single-slit antenna solution

9.6.9.1 Description

In UCODE 9xm, the test pads TP1 and TP2 can be safely short-circuited to the RF pads (RF1, RF2). See Figure 6 and Figure 7.

Single-slit antenna enables easier assembly and antenna design. In addition to the standard antenna assembly, the related increased input capacitance (Table 14) can be used for optimization for different antenna design.

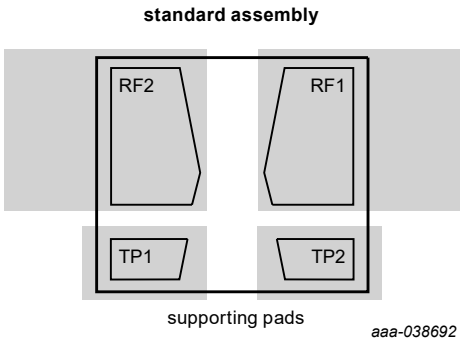


Figure 6. Standard antenna design versus single-slit antenna

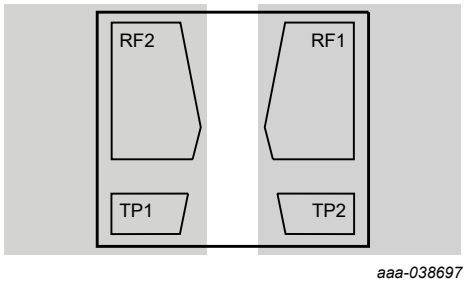


Figure 7. Single-slit assembly

9.6.10 Large pads

9.6.10.1 Description

The large gold pads of UCODE 9xm enable more robust and reliable assembly. This pad design allows for more freedom in the placement accuracy (see Figure 8).

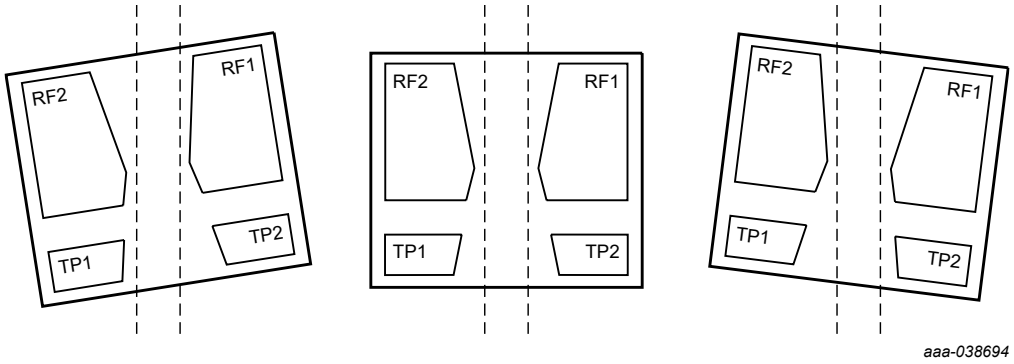


Figure 8. Rotation tolerant pad design

10 Limiting values

Table 13. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to RFN. [1] [2]

Symbol	Parameter	Conditions		Min	Max	Unit
Bare die limitations						
T_{stg}	storage temperature			-55	+125	°C
T_{amb}	ambient temperature			-40	+85	°C
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[3]	[4]	-	± 2	kV
Pad limitations						
P_i	input power	maximum power dissipation, RF1/RF2 pad		-	100	mW

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

[3] According to ANSI/ESDA/JEDEC JS-001

[4] For ESD measurement, the die chip has been mounted into a CDIP8 package.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

11 Characteristics

11.1 UCODE 9xm bare die characteristics

Table 14. UCODE 9xm RF interface characteristics (RF1, RF2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency			840	-	960	MHz
$P_{i(min)}$	minimum input power	READ sensitivity	[1]	-	- 23.6	-	dBm
$P_{i(min)}$	minimum input power	WRITE sensitivity	[1]	-	-21.6	-	dBm
t 16bit	encoding speed	16-bit	[2]	-	0.6	-	ms
		32-bit (block write)	[2]	-	1.05	-	ms
C_i	chip input capacitance	parallel	[3] [4] [5]	-	0.72	-	pF
Z	chip impedance	915 MHz	[3] [4] [5]	-	10.6-j242	-	Ω
R_P	chip resistance	parallel	[4]	-	3.3	-	kΩ
Z	typical assembled impedance in case of single-slit antenna assembly[6]	915 MHz	[7] [8] [5]	-	10.7-j187	-	Ω
Z	typical assembled impedance[9]	915 MHz	[7] [10] [5]	-	15.7-j226	-	Ω

[1] Tag sensitivity on a 2.15 dBi gain antenna
[2] When the memory content is "0000...".
[3] Measured with a 50 Ω source impedance directly on the chip
[4] At minimum operating power
[5] At center capacitor of Self-Adjust
[6] see Figure 7
[7] The antenna shall be matched to this impedance
[8] Assuming 205 fF additional assembly+test pad capacitance
[9] see Figure 6
[10] Assuming 45 fF additional assembly capacitance

Table 15. Table 13.UCODE 9xm memory characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
EEPROM characteristics							
t_{ret}	retention time	T_{amb} ≤ 55 °C		20	-	-	year
$N_{endu(W)}$	write endurance			100k	-	-	cycle

12 Packing information

12.1 Wafer

See [3].

13 Abbreviations

Table 16. Abbreviations

Acronym	Description
CRC	cyclic redundancy check
CW	continuous wave
DSB-ASK	double side band-amplitude shift keying
DC	direct current
EAS	electronic article surveillance
EEPROM	electrically erasable programmable read-only memory
EPC	electronic product code (containing header, domain manager, object class and serial number)
FM0	bi-phase space modulation
G2	Generation 2
IC	Integrated Circuit
PIE	pulse interval encoding
PSF	product status flag
RF	radio frequency
UHF	ultra high frequency
SECS	Semi Equipment Communication Standard
TID	tag identifier

14 References

[1] EPCglobal: EPC Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz, Version 2.1 (July 2018)

[2] EPCglobal: EPC Tag Data Standard, Release 1.13 (November 2019)

[3] Data sheet - Delivery type description – General specification for 12" wafer on UV-tape with electronic fail die marking, document number: 1862** [1]

1 ** ... document version number

15 Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Supersedes
SL3S1005 v.3.1	12 February 2025	Product data sheet	SL3S1005 v.3.0
Modifications:	Editorial changes. • Document security status changed to "Public". • Section 9.6.10 "Large pads": updated.		
SL3S1005 v.3.0	16 March 2023	Product data sheet	SL3S1005 v.1.0
Modifications:	• Section 9.5 "UCODE 9xm memory": updated • Section 9.6.1 "UCODE 9xm features control mechanism": updated • Section 9.6.7 "Brand Identifier": added • Section 11.1 "UCODE 9xm bare die characteristics": updated		
SL3S1005 v.1.0	22 September 2022	Objective data sheet	-

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

UCODE — is a trademark of NXP B.V.

Tables

Figures

Contents