# PN7220

**NFC controller with NCI interface supporting EMV and NFC Forum applications**

**Rev. 3.4 — 12 November 2024**                                              **Product data sheet**

## 1  General description

This document describes the functionality and electrical specification of the PN7220 high-power NFC controller family with NCI interface.

As an NCI 2.2 compliant NFC controller with high RF output (2 W) and high receiver sensitivity, the NXP PN7220 is a robust solution for payment terminals and all readers that must generate a strong RF field in a difficult environment. Offering full compliance with EMVCo 3.1 L1 analog and digital, the PN7220 simplifies designs while ensuring interoperability with a broad range of smartcards and mobile phones.

In addition to the reader/writer functionality, the device supports the host card emulation of ISO14443-A cards up to 848 kbit/s and allows to connect up to 3 TDA8035 which offer the possibility for an ISO7816 contact interface connection.

The PN7221 is based on the PN7220 and supports all features of PN7220 plus "Enhanced Contactless Polling" (ECP) by Apple - this description is not part of this document. Note, that the ECP feature is available after formal authorization only.

Two host connection options are available for this product:

1. Connection to one single host - this is typically one host running an Android operating system
2. Connection to two hosts - in this case one host is typically a security CPU connected by the SPI interface to meet PCI compliance requirements for an EMVCo payment subsystem, and the second host connected by an I2C interface which is typicallly used to run an Android operating system for all non-EMVCo payment related applications.

The PN7220 communicates with a connected host through a physical interface using the NCI 2.2 protocol.

The PN7220 supports two types of configurable polling loops: one NFC Forum polling loop, and one EMVCo compliant polling loop. Switching between the polling loops is done based on a hardware input (GPIO) triggered by a connected host - in case of a switching of the polling loop all data from an ongoing transaction is cleared from the internal buffers, the NCI software stack is beeing reset and an RF reset is beeing executed. This helps to ensure data integrity for the performed transaction and allows to connect the right logical software endpoints to each of the polling loops.

To speed-up the switching between NFC Forum polling and EMVCo polling and ease the RF configuration of each polling loop, two independent sets of RF configuration data can be stored in EEPROM. This allows to optimize each polling loop to meet individual RF requirements.

The PN7220 product family supports highly innovative and unique features which do not require any host controller interaction. These features include dynamic power control (DPC), adaptive waveform control (AWC), and fully automatic EMD error handling.

Additional documents supporting a design-in of the are available from NXP, this additional design-in information is not part of this document.

In this document, the term "MIFARE card" refers to a contactless card with an embedded MIFARE IC.

# 2 Features and benefits

## 2.1 RF functionality

### 2.1.1 ISO/IEC14443-A

• Reader/writer mode supporting ISO/IEC 14443-A R/W up to 848 kbit/s

### 2.1.2 ISO/IEC 14443-B

• Reader/writer mode supporting ISO/IEC 14443-B up to 848 kbit/s

### 2.1.3 FeliCa

• Reader/writer mode supporting FeliCa 212 kbit/s and 424 kbit/s (without crypto)

### 2.1.4 Tag type reading

• Supports reading of all NFC tag types ( type 2, type 3, type 4A and type 4B, type 5 )

### 2.1.5 MIFARE card reading

• Reader/writer communication mode for the MIFARE card family including MIFARE Classic Crypto supporting MIFARE Classic en-/decryption is integrated in hardware

### 2.1.6 ISO/IEC 15693

• Reader/writer mode supporting ISO/IEC 15693 (ICODE)
  – RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 6.6 kBd
  – RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 26 kBd
  – RX: "Manchester" encoding with 424 kHz single-subcarrier (SSC) and 53 kBd
  – TX: "1 of 4" encoding with 10 % modulation (53 kBd)
  – TX: "1 of 4" encoding with 100 % modulation (53 kBd).

### 2.1.7 NFC Forum compliancy

• NFC Forum version 13 compliance for R/W – analog and digital

### 2.1.8 EMVCo contactless compliancy

• Contactless EMVCo 3.1 compliance for R/W – digital
• Contactless EMVCo 3.1 compliance for R/W analog can be achieved, but depends on connected antenna geometry and size, matching network and RF settings.

### 2.1.9 Host interface

The devices PN7220 and PN7221 support one host interface using a single interface connection based on a I$^2$C interface host interface (host interface 1) with data rates up to 3.4 Mbit/s.

In addition, the device support two host interfaces using one interface connection based on a I$^2$C interface (host interface 2) up to 3.4Mbit/s and one SPI interface (host interface 1) up to 15Mbit/s.

The logical interface layer of the host interfaces is based on the NCI 2.2 interface specification, enhanced by NXP proprietary commands.

## 2.2 Transmitter

• Transmitter with high RF output power of 2.0 W
• Dynamic power control 2.0 (DPC) (dynamic power control without processing load on host MCU)
• Adaptive waveshaping control (AWC)

## 2.3 Receiver

• Robust receiver: Automatic configuration, advanced insensitivity against TFT display noise for higher RF performance

## 2.4 Integrated polling loop

• RF polling loop according to NFC Forum
• RF Polling loop according to EMVCo 3.1, integrated EMVCo L1 software stack

## 2.5 Integrated DC-DC

The PN7220 implements an integrated DC-DC which can be used to supply the transmitter. Since the supply voltage of the transmitter LDO can be up to 6.0 Volts, this simplifies the design of the power supply.

A single supply concept for the RF system, for example, with single 3.3 V supply, is possible and allows making use of the maximum RF output power by providing a maximum transmitter supply voltage.

The integrated DC-DC is used by the dynamic power control (DPC) to reduce the maximum power dissipation of the chip.

The usage of the DC-DC is optional.

For applications making use of the low-power card detection, the DC-DC is available.

## 2.6 RF debugging support

• RF debugging without external probing of test signals possible by sampling debug data into chip-internal memory based on pre-define trigger conditions – ideal debugging solution for PCI-compliant POS terminals
• One digital and one analog debug signal is provided by the chip for connection of an oscilloscope

## 2.7 ISO7816 contact interface

The product supports the connection of up to three TDA8035 ICs which is the default EEPROM configuration of the device.

The device features an integrated EMVCo L1 contact card activation, and is compliant with contactless EMVCO specification 3.x.

The contact interface can be used for a single or dual host configuration.

## 3  Applications

- Payment terminals following the COTS security requirements with full EMVCo3.1 analog and digital compliancy
- Multi-Application terminals
- Ticket validators for the controlling staff in public transport
- E-Vehicle charging stations
- Vending machines

# 4 Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $VDD_{(VBAT)}$ | supply voltage on pin VBAT (analog and digital supply) | VBAT ≥ VDDIO | 2.4 | - | 5.5 | V |
| $VDD_{(VDDIO)}$ | supply voltage on pin VDDIO (supply for host interface and GPIOs) | 1.8 V supply | 1.62 | - | 1.98 | V |
| | | 3.3 V supply | 2.4 | - | 3.6 | V |
| $VDD_{(VDDPA)}$ | supply voltage on pin VDDPA (input of the transmitter power amplifier) | PN7220 - supply with VDDPA from internal VDDPALDO with DC-DC | 1.5 | - | 5.7 | V |
| $I_{pd}$ | power down current | $VDD_{(VDDPA)} = VDD_{(VDDIO)} = VDD_{(VDD)}$ 3.0 V; hard power down state; pin VEN set LOW, $T_{amb}$ = 25 °C, External supply by VDDIO | - | 40 | 105 | µA |
| $I_{stb}$ | standby current | $T_{amb}$ = 25 °C | - | 45 | 110 | µA |
| $IDD_{(VDDPA)}$ | supply current on pin VDDPA | supplied via VUP_TX (TX_LDO active) | - | - | 350 | mA |
| | | supplied without DC-DC and TXLDO active | - | - | 400 | mA |
| $P_{(PA)}$ | transmitter output power | supplied via VUP_TX (TX_LDO active) | - | - | 2.0 | W |
| | | supplied without DC-DC and TXLDO active | - | - | 2.3 | W |
| $T_{amb}$ | ambient operating temperature | in still air with exposed pins soldered on a 4 layer JEDEC PCB, | -40 | - | +85 | °C |
| $T_{amb}$ | ambient operating temperature | in still air with exposed pins soldered on a 4 layer JEDEC PCB, | -40 | - | +85 | °C |
| | | in still air with exposed pins soldered on a 4 layer JEDEC PCB, TX current = 120 mA @ VDDPA = 3.6 V | -40 | - | +105 | °C |
| $T_{stg}$ | storage temperature | no supply voltage applied | -55 | - | +150 | °C |
| $T_{j\_max}$ | maximum junction temperature | - | - | - | +125 | °C |

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# 5 Firmware versions

## Firmware version 1.00

- Android reads out this firmware version as 03.01.00
- Available on chip for PN7220 and PN7221

*Functionality of Firmware 1.00*

- HOST interface:
  – Single CPU configuration (HIF_SEL0 pulled to '0')
  – HIF1-I2C interface
- Mode switch GPIO handling to either start in NFC Forum mode or EMVCo mode.
- EMVCo polling for Type A, Type B, Type F, and VAS (PN7221 only).
- NFC Forum polling for Type A, Type B, Type F, Type V, and VAS (PN7221 only) in Reader Mode.
- Proprietary commands:
  – NCI_PROPRIETARY_ACT_CMD/RSP
  – WTX_NTF
  – EMVCo Collision Error NTF
  – TEST_PRBS_CMD/RSP
  – REG_TEST_API_CMD/RSP
  – CTS Support
  – SWITCH_RF_FIELD_CMD/RSP
  – EEPROM_ACCESS_CMD/RSP
  – LOAD_PROTOCOL_CMD/RSP

## Firmware version 2.01

- Android reads out this firmware version as 03.02.01
- Available on chip for PN7220 and PN7221
- This version cannot be replaced by lower firmware versions. For example replacing FW2.01 by FW1.00 is not possible.

*New functionality of firmware version 2.01 compared to firmware version 1.00:*

- HOST interface
  – Dual CPU configuration (HIF_SEL0 pulled to '1')
  – HIF2-I2C interface in NFC Forum mode (Mode Select pulled to '0')
  – HIF1-SPI Interface in EMVCo Mode (Mode Select pulled to '1')
- Mode switch GPIO handling to either start in NFC Forum mode or EMVCo mode in Dual CPU mode.
- NFC Forum polling for Type A (T4AT) in Listen mode.
- Contact support for maximum of three slots. One slot can be configured as Dynamic EMVCo slot.
- Proprietary commands
  – RAW_EXCHANGE_CMD/RSP

# 6 Ordering information

**Table 2. Ordering information**

| Type number | Package | | Version |
|---|---|---|---|
| | **Name** | **Description** | |
| PN7220EV/C100K | VFBGA64 | Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs<br><br>The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557<br><br>Version for connection to 1 host microcontroller<br><br>Initialized with firmware version 1.00 | SOT1307-2 |
| PN7220EV/C100Y | VFBGA64 | Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs<br><br>The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518<br><br>Version for connection to 1 host microcontroller<br><br>Initialized with firmware version 1.00 | SOT1307-2 |
| PN7221EV/C100K | VFBGA64 | Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs<br><br>The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557<br><br>Version for connection to 1 host microcontroller and ECP - Initialized with firmware version 1.00 | SOT1307-2 |
| PN7221EV/C100Y | VFBGA64 | Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs<br><br>The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518<br><br>Version for connection to 1 host microcontroller and ECP - Initialized with firmware version 1.00 | SOT1307-2 |
| PN7220EV/C101K | VFBGA64 | Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs<br><br>The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557<br><br>Version for connection to 1 or 2 host microcontroller<br><br>Initialized with firmware version 2.01 | SOT1307-2 |
| PN7220EV/C101Y | VFBGA64 | Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs<br><br>The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518<br><br>Version for connection to 1 or 2 host microcontroller<br><br>Initialized with firmware version 2.01 | SOT1307-2 |

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**Table 2. Ordering information**...*continued*

| Type number | Package | | Version |
|---|---|---|---|
| | **Name** | **Description** | |
| PN7221EV/C101K | VFBGA64 | Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered in 5 trays, MSL = 3. Minimum order quantity = 5 x 490 pcs<br><br>The ending "K" in the product name is indicating the packing "multiple tray"; 12NC (order number) ending - 557<br><br>Version for connection to 1 or 2 host microcontroller and ECP - Initialized with firmware version 2.01 | SOT1307-2 |
| PN7221EV/C101Y | VFBGA64 | Plastic thin fine-pitch ball grid array package; 64 balls, body 4.5 x 4.5 x 0.9 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs<br><br>The ending Y in the product name is indicating the packing "reel"; 12NC (order number) ending - 518<br><br>Version for connection to 1 or 2 host microcontroller and ECP - Initialized with firmware version 2.01 | SOT1307-2 |

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## 7  Block diagram



**Figure 1.  System connections** [1]

[1]    The replacement of "MOSI/MISO" to "COTI/CITO" in this document follows the recommendation of the NXP - I$^2$C standards organization.

The PN7220 is connected to an application processor / host CPU based on an NCI interface.

The device offers high compatibility to existing solutions which offer an NCI interface (Host IF_1). The physical interface used for the connection is a I2C interface.

Host IF_1 allows $I^2C$ data rates up to 3.4 Mbit/s.

*$I^2C$ address:*

The PN7220 host interface 1 supports the 7-bit addressing mode, first 5-bits are fixed and is decimal 40, last two bits are configurable using ADDR0 and ADDR1 pins . This provides maximum flexibility even in cases where the $I^2C$ bus is shared with other devices on top of the PN7220.

*Default mode after boot:*

The system is always booting in mode (EMVCo polling or NFC Forum polling) defined by the level on the pin MODE/GPIO2.

*Switching between NFC Forum and EMVCo polling:*

Switching to a EMVCo polling loop is done based on a physical signal "MODE/GPIO2" controlled by the application processor / host CPU. All previous data from earlier communications are erased, and the NCI software stack is being reset. The system enters then the new EMVCo polling mode. Switching back to NFC Forum mode again clears all previous data from earlier communication and resets the NCI software stack.

# 8   Pinning information

## 8.1   Pin description VFBGA64



ball A1
index area

Transparent top view

*aaa-035352*
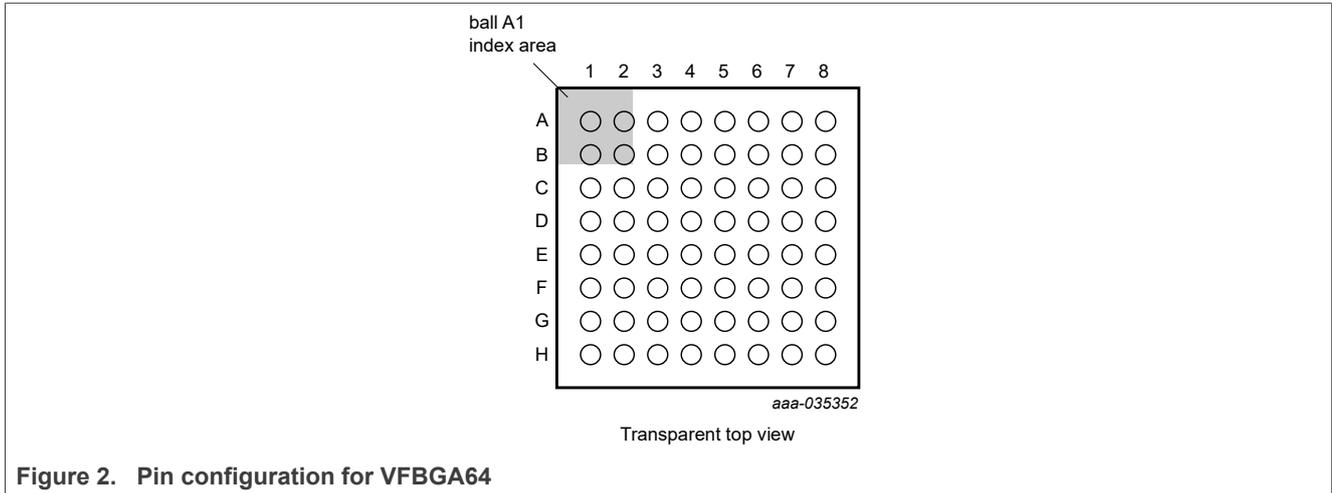
**Figure 2.   Pin configuration for VFBGA64**

**Table 3.  Pin description VFBGA64**

| Pin Number | Symbol[1] | Type | Description [1] |
|---|---|---|---|
| **Host Interface 1 (I$^2$C / SPI)** | | | |
| E6 | SPI CITO / I2C1_ SDA | Output | One CPU system: I$^2$C1_ SDA |
| | | | Two CPU system: SPI CITO |
| E5 | SPI SCK / I2C1_ SCL | Input | One CPU system: I$^2$C1_SCL |
| | | | Two CPU system: SPI SCK |
| D6 | SPI NSS / I2C1 Adr Bit 0 | Input | One CPU System: I$^2$C Adr Bit 0 (Address is configured using 5 fixed bits (40d - 028h) and 2 Bits from D5/D6) I$^2$C interface address can be configured to 0x28 (00), 0x29 (01), 0x2A (10), 0x2B (11) based on D6 and D5 Pins |
| | | | Two CPU system: SPI NSS |
| D5 | SPI COTI / I2C1 Adr Bit 1 | Input | One CPU system: I$^2$C Adr Bit 1 ((Address is configured using 5 fixed bits (40d - 028h) and 2 Bits from D5/D6) I$^2$C interface address can be configured to 0x28 (00), 0x29 (01), 0x2A (10), 0x2B (11) based on D6 and D5 Pins |
| | | | Two CPU system: SPI COTI |
| B7 | IRQ1 | Output | Host communication IF1 / event interrupt signal |

**Table 3.  Pin description VFBGA64**...*continued*

| Pin Number | Symbol[1] | Type | Description [1] |
|---|---|---|---|
| **Host Interface 2 (I2C)** | | | |
| A6 | I2C2_SDA | Input/Output | One CPU system: n.c. |
| | | | Two CPU system: I$^2$C 2 SDA |
| B6 | I2C2_SCL | Input | One CPU system: n.c. |
| | | | Two CPU system: I$^2$C 2 SCL |
| D7 | I2C2_WAKEUP | Input | one CPU system: GND |
| | | | Two CPU system: Standby wakeup signal |
| H8 | I2C2_IRQ | Output | One CPU system: n.c. |
| | | | Two CPU system: Host communication interface 2 event interrupt signal |
| **Hardware reset** | | | |
| B3 | VEN | Input | Hardware reset, low active (independent from $V_{VDDIO}$) |
| **Host interface and Mode selection** | | | |
| E7 | MODE | Input | Mode selection (EMVCo or NFC Forum polling loop) Input H: EMVCo polling mode Input L: NFC Forum polling mode Input defines always EMVCo or NFC Forum polling loop, but the used host interface is different dependent on the configuration of C7: C7= Level L at boot (1 CPU system): NFC Forum and EMVCo polling loop data transfer is done always using host interface 1 C7 = Level H at boot (2 CPU system): NFC Forum polling loop is doing data transfer using host interface 2 and EMVCo polling loop is doing data transfer using host interface 1 |
| C6 | HOST_IF_SEL1 | Input | Shall always be on GND on PN7220 |
| C7 | HOST_IF_SEL0 | Input | Host interface select 0 - selection of 1 or 2 CPU system Level L: Host Interface 1 active after boot (I2C Host Interface 2 has no function) Level H: Host Interface 2 is always active after boot, SPI Interface 1 is active only after selecting EMVCo mode on E7 - MODE/GPIO2 HIF_SEL0 pin is read by FW after POR or reset via VEN or boot from low-power mode (OFF, standby, LPCD etc.). |
| **Xtal connection** | | | |
| F8 | XTAL1 | Input | Crystal / system clock input |
| G8 | XTAL2 | Output | Clock output (amplifier-inverted signal output) for crystal |
| **Supply pins** | | | |
| H2 | VSS_PA | Supply GND | Transmitter ground |
| G3 | VSS_PLL | Supply GND | PLL ground (low noise) |
| A2 | VSS_PWR | Supply GND | DC-DC boost ground |
| D3 | VSS_REF | Supply GND | PMU ground |
| B2, E3 | VSS_SUB | Supply GND | Substrate ground |

**Table 3. Pin description VFBGA64**...*continued*

| Pin Number | Symbol[1] | Type | Description [1] |
|---|---|---|---|
| C3 | VSS_PMU | Supply GND | PMU ground |
| F4 | VSS_DIG | Supply GND | Digital ground |
| F3 | VSS_NFC | Supply GND | NFC ground |
| E1 | VBAT | Supply | System supply, used to supply the analog and digital blocks, memory and internal voltage references |
| A8 | VDDIO | Supply | I/O pads power supply |
| G1 | VDDPA | Supply | Transmitter supply |
| F1 | VUP_TX | Supply | Input supply voltage for transmitter LDO |
| B1 | VDDBOOST | Supply | DC-DC boost supply |
| A1 | BOOST_LX | Output | Boost inductance loopback, to be connected to boost inductor |
| A3 | VBATPWR | Supply | To be connected to boost inductor and transmitter power supply |
| **Outputs for stabilizing cap** | | | |
| A4 | VDDNV | Output | Nonvolatile memory power supply, to be connected to ground via 220 nF blocking cap |
| D2 | VREF | Output | High quiescent reference voltage, to be connected to ground via 100 nF blocking cap |
| C1 | VDDC | Output | Power supply for Digital Core, to be connected to ground via 220 nF blocking cap |
| G2 | TXVCM | Output | Transmitter voltage common mode, to be connected to ground via 220 nF blocking cap |
| F2 | TXVCASC | Output | TX decoupling cap, to be connected to VDDPA |
| H6 | VMID | Output | Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground) by 100 nF blocking cap |
| **RF Debug signals** | | | |
| G7 | AUX_1 | Output | Test bus 1 |
| F7 | AUX_2 | Output | Test bus 2 |
| **Antenna connections** | | | |
| H5 | RXP | Input | Receiver input "Positive" |
| H4 | RXN | Input | Receiver input "Negative" |
| H1 | TX1 | Output | Antenna driver output 1 |
| H3 | TX2 | Output | Antenna driver output 2 |
| **Analog/Digital inputs and outputs** | | | |
| E8 | TDA_CS0 / GPIO0 | Output | Digital test bus0 / TDA chip select 0 |
| D8 | TDA_CS1 / GPIO1 | Output | Digital test bus1 / TDA chip select 1 |

**Table 3. Pin description VFBGA64**...*continued*

| Pin Number | Symbol[1] | Type | Description [1] |
|---|---|---|---|
| **Security feature** | | | |
| B4 | PRD1 | Input/ Output | Package removal detection, internally connected to PRD2 |
| G4 | PRD2 | Input/ Output | Package removal detection, internally connected to PRD1 |
| **TDA8035 interface** | | | |
| A7 | TDA_CS2 | Output | TDA chip select 2 (TDA_CS2) <br> ***Note:*** *Pulldown resistor required. EEPRM configuration to configure as TDA_CS. Default is TDA_CS = disabled.* |
| B5 | TDA_ CMDVCCN / GPIO5 | Input/Output | TDA_CMDVCCN |
| C4 | ISO_INT_AUX | Input/Output | Auxiliary Card Interrupt: **In case no TDA is connected, connection to GND is mandatory** |
| C5 | TDA_RSTIN / GPIO4 | Input/Output | TDA_RSTIN |
| D4 | ISO_IO_AUX | Input/Output | Auxiliary Card I/O |
| E4 | ISO_CLK_AUX | Input | Auxiliary Card Clock |
| F5 | TDA_CLKDIV2 / SPIM_COTI | Input | TDA_CLKDIV2 |
| F6 | TDA_CLKDIV1 / SPIM_CITO | Input / Output | TDA_CLKDIV1 |
| G5 | SPIM_SCLK / TDA_EN_5V_3V | Input / Output | TDA_EN5V_3V |
| G6 | SPIM_SSN / TDA_EN_1.8V | Input / Output | TDA_EN_1.8V |
| **Pins not to be connected** | | | |
| A5 | PVDD_OUT | Output | Do not connect |
| B8 | SWDIO | Input/Output | Do not connect |
| C2 | TEST | Input/Output | Do not connect. |
| C8 | SWD_CLK | Input | Do not connect |
| D1 | USB_VBUS | Supply | Do not connect |
| E2 | AD1 | Input | Do not connect |
| H7 | VTUNE1 | Output | Do not connect |

[1]    The replacement of "MOSI/MISO" to "COTI/CITO" in this document follows the recommendation of the NXP - I2C standards organization.

For good RF performance, all blocking capacitors shall be placed on the same side of the PCB. Traces from pin to capacitor shall be as short as possible.

All supply GND connections shall be connected by low-ohmic connections on the PCB.

**"Do not connect" means: No connection to power supply or GND.**

# 9  Functional description

PN7220 can be connected to a host controller through the physical host interface - a pulldown resistor is required.

The logical interface toward the host controller is NCI 2.2-compliant Ref. [2] with additional commands for NXP-specific product features.

The device implements a contactless EMVCo3.1 compliant polling loop and allows to be compliant to contalctless EMVCo L1 digital.

The EEPROM configuration allows to configure the device to support up to three contact interfaces using a TDA8035 for interfacing to ISO7816 compliant cards.

ISO7816 contact card activation is supported by the device.

Enhanced RF debugging and easy configuration are supported by usage of the SPI interface, analog and digital debug outputs (AUX) and the CLIF test station.

## 9.1  Functional overview

The PN7220 is an NFC controller with high transmitter output power. It implements the RF functionality like an antenna driving and receiver circuitry and the functionality to realize an NFC Forum and EMVCo compliant reader.

**Connection to host controller**

Two host connection options do exist for this product:

1. Connection to one single host - this is typically one host running an Android operating system
2. Connection to two hosts - in this case one host is typically a security CPU connected by the SPI interface to meet PCI compliance requirements for an EMVCo payment subsystem, and the second host connected by an I2C interface which is typicallly used to run an Android operating system for all non-EMVCo payment related applications.

For NFC data exchange a high-level NCI 2.2 protocol implementation extended by proprietary commands is available.

For the two host system which makes use of two host interfaces, the switching of the polling loops is switching the physical interfaces. The system is always booting up in the non-EMVco mode using the I2C interface. The SPI interface connecting the security CPU is disabled at this time. Switching to EMVCo mode disables the I2C interface completely, and activtates the SPI interface which is connected e.g. to a security microcontroller. Effectively, the NFC Forum polling loop data transfer is linked to the I2C interface, and the EMVCo polling loop data transfer is linked to the SPI interface.

The processing of the NCI commands had been improved on the PN7220 compared to previous NFC reader generations with NCI interface which eases the meeting of EMVCo timing requirements.

**Integrated NFC Forum polling loop**

All supported RF technologies can be independently enabled within this PCD polling loop. The sequence of RF technologies within the PCD polling loop cannot be modified.

**Integrated EMVCo3.1 L1 polling loop**

The PN7220 implements an integrated EMVCo3.1 PCD-compliant polling loop. The polling loop can be configured to poll as well for FeliCa compliant cards following the EMVCo specification for "other technologies". Alternatively, the device can be configured to poll for FeliCa cards exclusively. In addition, the PN7221 allows to configure the ECP. The firmware of the device had been optimized for low latency which helps to achieve the EMVCo timing requirements even with Android-based host systems.

**Selection of a dedicated polling loop: NFC Forum or EMVCo**

The selection of a dedicated polling loop is done based on a hardware input MODE.

After reset, the polling loop which can be activated depends on the MODE selection. It can be either EMVCo or NFC Forum compliant pollinig.

Switching the polling loop from one mode to the other is done by changing the level of the MODE input pin. Switching from NFC Forum polling mode to the EMVCo polling mode resets the NCI stack, clears all data in the buffers, performs an RF reset and allows then to activate the polling according to EMVCo 3.1. Switching back to the NFC Forum polling mode, again reset resets the NCI stack, performs an RF reset, clears all data in the buffers and is ready to receive NCI Interface commands to activate NFC Forum polling.

In addition to the selection of the polling loop, the MODE input activates a dedicated user defined set of RF configuration parameters. With this, a different RF behaviour for EMVco and NFC Forum can be realized.

This switching of modes based on an external mode pin is working faster than alternative solutions based on loading configuration files, and allows a more secure implementation of the software on the host MCU.

**Contact interface**

The product allows to connect up to 3 TDA8035 which offer the possibility for an ISO7816 contact interface connection.

**Clock supply**

The PN7220 uses an external 27.12 MHz crystal as clock source for generating the RF field and its internal digital logic. Alternatively, an internal PLL allows using an accurate external clock source of either 24 MHz, 32 MHz, and 48 MHz (configured in EEPROM register CLK_INPUT_FREQ, 0012h)). This allows saving the 27.12 MHz crystal in systems which implement one of the mentioned clock frequencies. For EMVCo compliant applications and best RF performance, the usage of a 27.12MHz crystal is recommended.

**Integrated DC-DC**

The DC-DC is a step-up converter and is able to deliver an output voltage from approx. 2.8 V up to 6.0 V. The targeted output voltage can be configured by software. It allows a single supply voltage (for example, 3.3 V) while delivering maximum RF output power. Dependent on the application target either a direct transmitter supply or a transmitter supply by the integrated DC-DC can be chosen. The DC-DC is controlled by the Dynamic Power Control 2.0 to keep the power dissipation of the chip minimized in antenna loading cases which require a reduction of the RF output power.

**Transmitter LDO (TX_LDO)**

The Transmitter output drivers are supplied by a transmitter LDO which reduces external noise and is used for the DPC functionality to lower the supply voltage of the transmitters. The high granularity of 100 mV for setting the TX_LDO output voltage together with a sophisticated control loop and true current measurement ensures that a DPC regulation is not accidentally treated as received data.

### Low-power card detection

The low-power card detection (LPCD) allows saving battery charge during polling for NFC counterparts like cards and mobile phones. In general, the low-power card detection provides a functionality, which allows to power down the reader for a certain amount of time to safe energy. After some time, the reader becomes active again to poll for cards. If no card is detected, the reader can go back to the power down state. During the polling time, a host controller can be set to a power-saving mode. An interrupt request from the PN7220 allows waking up the host controller in case an antenna detuning by a card or cell phone had been detected.

### Dynamic power control 2.0

The next generation Dynamic Power Control (DPC2.0) with true transmitter current measurement works autonomous without host interaction. Avoiding additional host controller processing load is important for time critical applications like payment. A fast control response time of less than 1 ms allows using optimized antenna matchings.

### Adaptive wave shape control

The Adaptive Wave Shape Control (AWC) helps to keep the waveshapes within specification limits, even in case of antenna detuning. This simplifies the time-consuming antenna matching procedure and does not require any matching compromises to be taken.

### Receiver signal level control

The receiver signal chain consists of an automatic controller RF input attenuator and a true Baseband Amplifier (BBA). This feature delivers an outstanding communication range with tags, labels, cards, and mobile phones.

### RF Debugging

Comprehensive and innovative debug features are implemented to support the NFC reader development even for difficult and non-standard compliant cards and mobile phones. An integrated contactless test station allows performing a non-intrusive debugging of receiver signals without the need of connecting additional wires to the chip. Capturing of chip-internal signals is done by configuring flexible trigger conditions, sampled internal data is stored in RAM memory, transferred by SPI to a host microcontroller and visualized on a PC by the NFC Cockpit development tool. A virtual comfort interface (VCOM) is supported by the NFC cockpit tool, which allows to use the NFC cockpit together with any host microcontroller. Analog and digital debug signals (AUX1, AUX2) are available as well and allow the connection of an Oscilloscope for analog and digital signal debugging.

The receiver signal processing is optimized to cope with noisy environments. This is beneficial, especially in case a TFT display or DC-DCs are part of the NFC system design.

### Automatic EMD error handling

An automatic EMD handling performed without host interaction relaxes the timing requirements on the host controller. Automatic EMD error handling according to ISO/IEC14443 and EMVCo 3.0 is supported. In addition, the EMD error handling is widely configurable, which allows adaptions in case of future possible specification changes.

**Firmware update**

The PN7220 supports a secure update of the implemented firmware. In Secure Firmware update mode, the PN7220 requires no dedicated physical handling of the SPI interface lines. The firmware download does not require any additional hardware pin to be handled, instead the download mode is activated by a command, followed by a hardware reset. After booting from reset, the PN7220 will be in download mode.

**EEPROM configuration**

Non-Volatile EEPROM memory of the PN7220 is used to store configuration data that must be preserved in case the PN7220 is not connected to any supply voltage. The configuration for dedicated RF protocols and antenna-dependent configuration is defined in this non-volatile memory as well as other configuration data which must be preserved during power supply disconnect is stored in this EEPROM memory. Examples for these are settings for receiver sensitivity, DPC, waveshaping, LPCD, and power supply configurations.

**RF configuration**

The PN7220 allows an automatic RF protocol selection based on the actual polling loop state. Pre-defined user configuration data is stored in non-volatile memory (EEPROM) and is automatically loaded for the modulation scheme currently activated by the polling loop.

Two dedicated configuration sets do exist for the RF configuration: One defining the settings in case the EMVCo polling loop is active, and another one on case the NFC Forum polling loop is active. Activating a dedicated polling loop automatically causes the related RF configuration to be loaded from the non-volatile memory. There is no need to load configuration files like it is required by other products supporting the NCI interface.

The loading of the RF configuration to the non-volatile memory is typically done only once during production.

**Note:** *Frequent automatic reloading of the RF configuration in the application is not recommended, since the number of possible configuration updates (EEPROM programming cycles) is technically limited. The device allows to store data which requires a frequent update in the application in registers / RAM.*

## 9.2 NCI interface

The functionality of the NCI interface is described in the user manual and the NCI 2.2 Interface standard.

## 9.3 Byte and bit order

The byte and bit order describes the order of bytes or bits within a binary representation of a value in the memory, which can be a register or EEPROM.

"Array size" defines the number of elements of "type size". Type size can be uint8 (8 bit), uint16 (16 bit) or uint32 (32 bit).

The location of byte-sized data (8 bit) with an array size of 2 is as follows:

- Value hex: 0x1234
- address x: 12
- address x+1: 34

The location of word-sized data (16 bit) is as follows:

- Value hex: 0x1234
- address x: 34
- address x+1: 12

The location of word-sized data (16 bit) in an array size of 2 is as follows:

- The placement of the array is large endian, the placement of nibbles of the variable is small endian.
- Value hex: 0xAABBCCDD
- address x: BB
- address x+1: AA
- address x+2: DD
- address x+3: CC

The location of double word-sized data (32 bit) is as follows:

- Value hex: 0xAABBCCDD
- address x: DD
- address x+1: CC
- address x+2: BB
- address x+3: AA
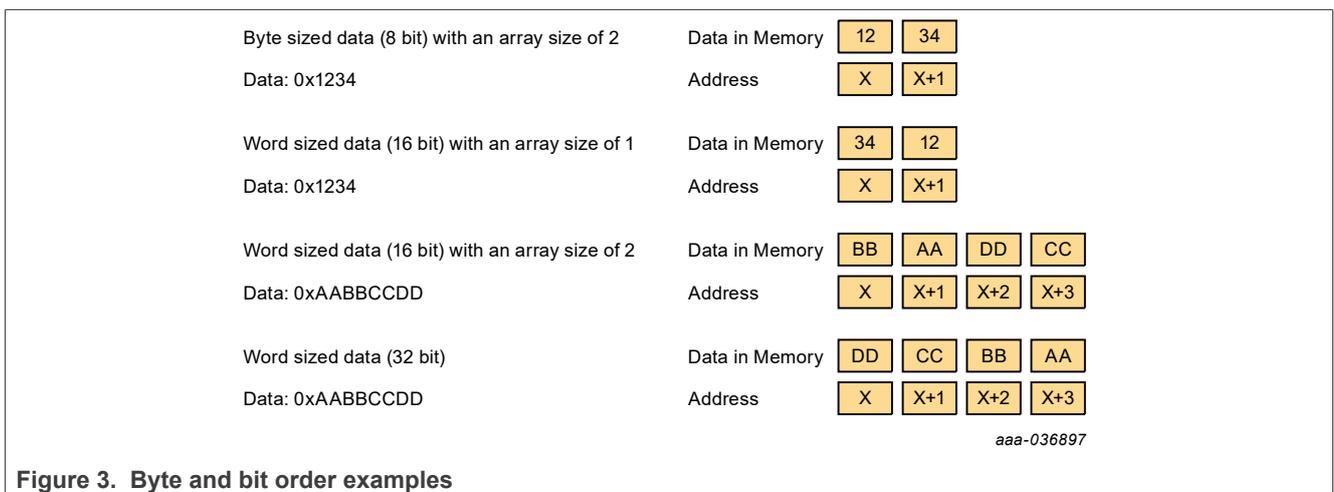


**Figure 3. Byte and bit order examples**

Data from the EEPROM is read in little-endian format - LSB first. This means that the byte at the lower address is read first.

The PN7220 is a little-endian system. This means that the byte at the lower address is read first.

## 9.4  Initial calibration

The PN7220 requires a calibration before the RF field is switched on for the first time with unloaded condition.

"Unloaded" means: Without any additional metal in proximity of the antenna, except for the NFC reader components itself.

During development of new readers, this calibration shall be done each time the antenna design, antenna matching, or EMC filter is modified.

The calibration sequence is the following:

Write EEPROM CfgNovCal – 0x00

Write REGISTER TX_NOV_CALIBRATE_AND_STORE_VAL - 0x01

Write EEPROM CfgNovCal – 0x02

## 9.5  System power states

The PN7220 can operate in different power states. The functionality and current consumption is dependent on the actual system power state.

Power states can be changed by the level on the pin VEN and by connecting/disconnecting the power supply of VBAT. Power state change will also be triggered by certain events - VDDIO Loss, overcurrent detection, overtemperature.

In addition, state changes are triggered possible by host commands.

Disconnecting and connecting the power supply on VBAT restarts the PN7220 always in Active State after releasing the pin VEN (transition low to high).

A transition of low to high on pin VEN restarts the PN7220 always in Active State.

Table 4 lists the supported power states.

**Table 4.  PN7220 power states**

| Power state | Description | Typical current consumption |
|---|---|---|
| Power off | The NFC system (supply pin VBAT, RF transmitter) is not supplied by a battery/system PMU. Other domains might be supplied (for example, I/O pad interface on pin VDDIO). Device is not functional | - |
| PMU off | The NFC system is disabled by the host via a low signal on pin VEN. No internal clocks of the PN7220 are active. Entry to PMU OFF can also be triggered by power loss on VDDIO. Wake-up events to change PMU OFF state: Power reset on pin VBAT, VEN rising edge, VDDIO restore. | 5 µA |
| ULP standby | Not supported | - |

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**Table 4. PN7220 power states**...*continued*

| Power state | Description | Typical current consumption |
|---|---|---|
| Standby | The NFC system can switch after a specific time of inactivity automatically into a low-power mode to minimize power dissipation. The state of external interfaces is maintained properly. PMU operates in low-power state. Wake-up counter clock is available. PCRM is supplied and running in low-power mode. I/Os are supplied by VDDC_LP. PMU FSM in PCRM manages the transition in power state. Wake-up sources: Activity on host IF, SWPM communication, LPDET, wake-up counter, power loss on VDDIO, GPIO, RxPROT, No High Temp on TX and so on. | 45 µA |
| Active | The PN7220 is able to process internal or external events or data. All external power supply sources and the external clock must be available, and all internal clocks are active. | 20 mA (system without RF current) |

## 9.6 Power supply

The device allows to configure different power supply options for the transmitter power amplifier. To make use of them, a combination of external connections and chip internal configurations must be done. The following supply options are available:

- Internal VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO). In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.
- Direct VDDPA configuration: This configuration is recommended for applications which require highest efficiency, like battery supplied devices. In this configuration, a battery can be connected directly to the transmitter supply avoiding the voltage drop of approximately 0.3 V caused by the TX_LDO. A clean supply voltage without noise is required to achieve a good RF performance.
  In this configuration the DPC, current measurement and overcurrent protection is not available.

### 9.6.1 System power supply overview

The PN7220 is using three different supplies each for the following functional blocks:

1. Supply for the host interface and GPIOs (VDDIO)

2. Supply for the analog and digital blocks (VBAT/VBAT_PWR)

3. Supply of the RF drivers (VDDPA), DC-DC (VBAT_PWR), and TX_LDO (VUP)

The functionality of the GPIOs, host interface and internal analog and digital blocks is independent from the supply of the RF driver. This allows to configure a dedicated transmitter supply configuration at any time. Care shall be taken to switch on the RF field only after the transmitter-related power supply had been configured according to the external physical supply connections (VDDPA, VBAT_PWR, VUP).

The power supply configuration is configured in EEPROM and therefore will not get lost in case of power supply loss or reset of the chip. Typically, this configuration is only performed once during the production of a reader.

RF field shall not be turned on without setting the correct power supply configuration in the EEPROM.

**Note:** The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT.

### 9.6.2 Connecting blocking capacitors

Some pins are connected to blocking supply capacitors. PCB traces to these capacitors must be as short as possible, and a low-ohmic grounding of the GND-side of the capacitors is required for optimized RF performance.
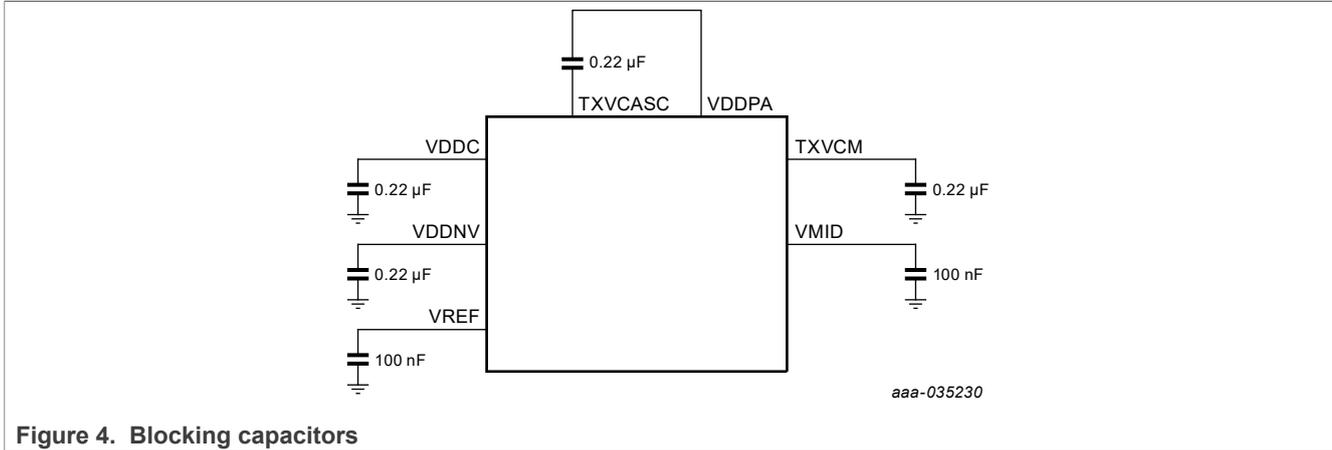


**Figure 4. Blocking capacitors**

### 9.6.3 Transmitter power supply

The PN7220 is configured by EEPROM for the different power supply options.

The following EEPROM Addresses are used to configure the power supply of the transmitter:

DCDC_PWR_CONFIG (0000h) - Enables/disables and configures the DC-DC according to the external supply connections.

TX_LDO_CONFIG (address 0002h) - Enables/disables and configures the TX_LDO.

TX_LDO_VDDPA_HIGH (address 0006h) - initial out voltage when DPC is used.

TX_LDO_VDDPA_LOW (address 0007h) - lowest VDDPA when DPC is used.

TX_LDO_VDDPA_MAX_RDR (address 0008h) - maximum voltage to be set in reader mode used by DPC.

TX_LDO_VDDPA_MAX_CARD (address 0009h) - VDDPA maximum voltage to be set in card mode used by DPC.

No specific registers are required to configure the pad supply (VDDIO) or the supply for the analog and digital blocks (VUP).

### 9.6.3.1 TX_LDO transmitter supply

TX_LDO supplied VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX_LDO).

In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX_LDO is adding an improved rejection of noise on the supply lines.

A decoupling cap is required on VDDPA pin.



(a) Internal VDDPA configuration

*aaa-035233*
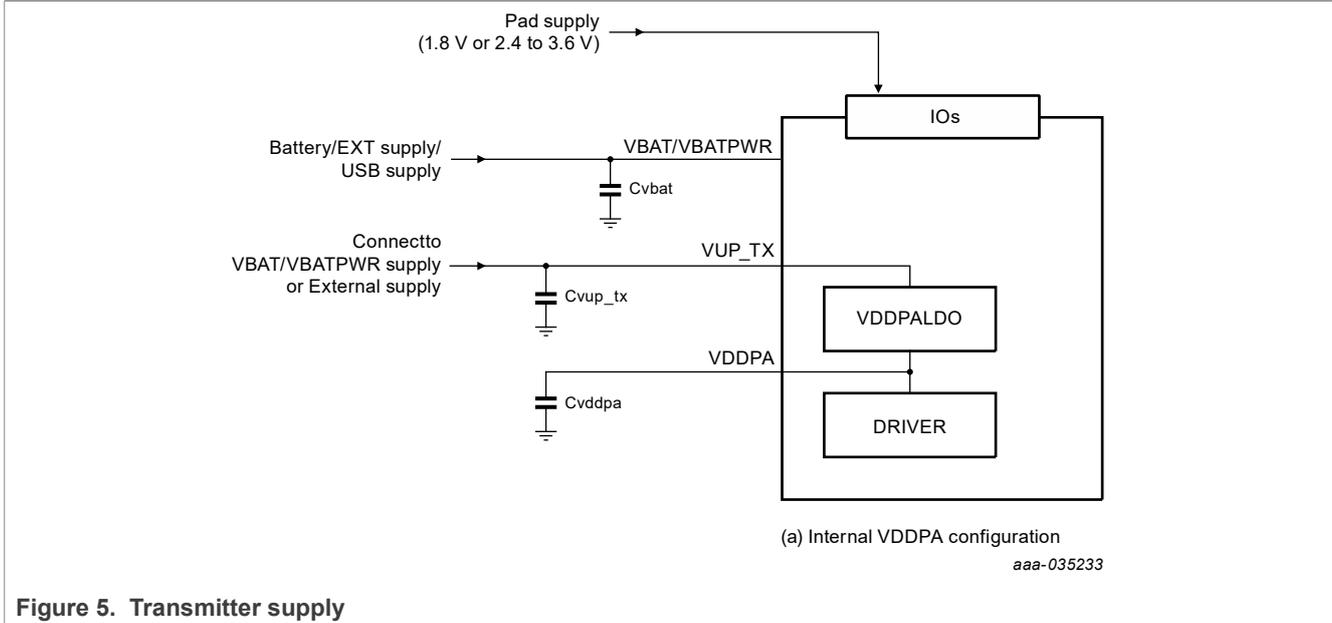
**Figure 5.  Transmitter supply**

### 9.6.3.2 Direct transmitter supply

Direct VDDPA configuration:

TX_LDO must be configured OFF by SW configuration. VUP_TX and VDDPA connected to VBAT/VBATPWR.



(a) Direct VDDPA configuration

*aaa-035232*
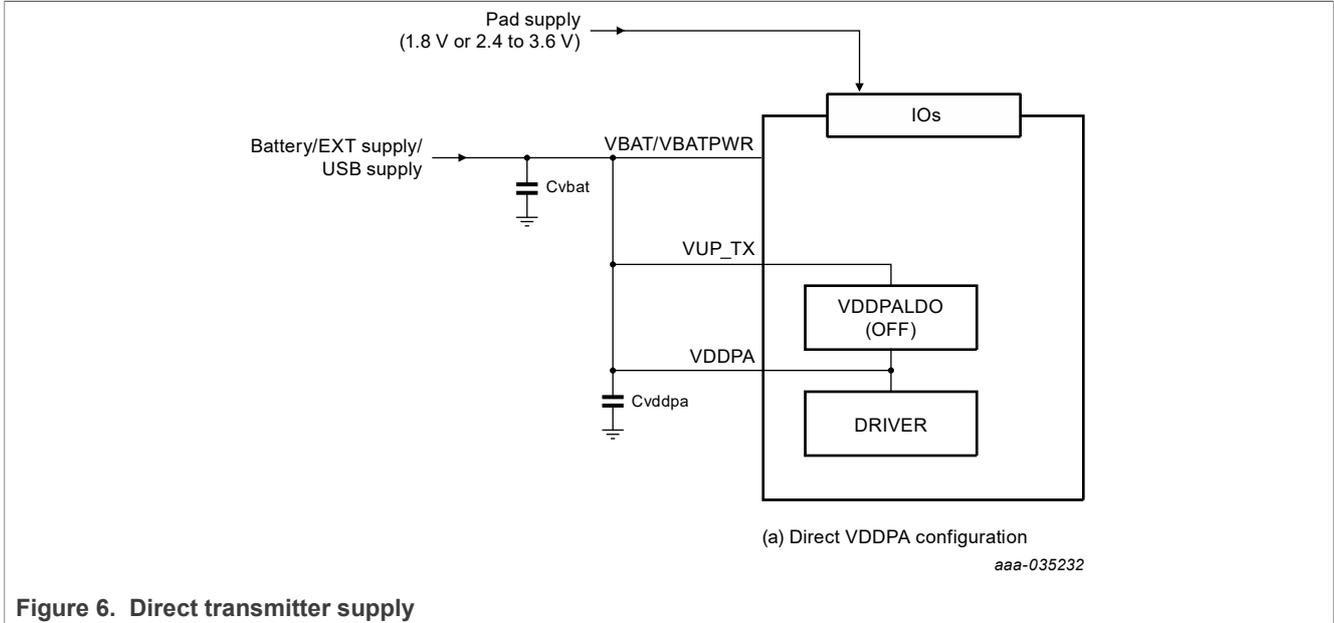
**Figure 6. Direct transmitter supply**

### 9.6.3.3 DC-DC (boost) supply



*aaa-035231*
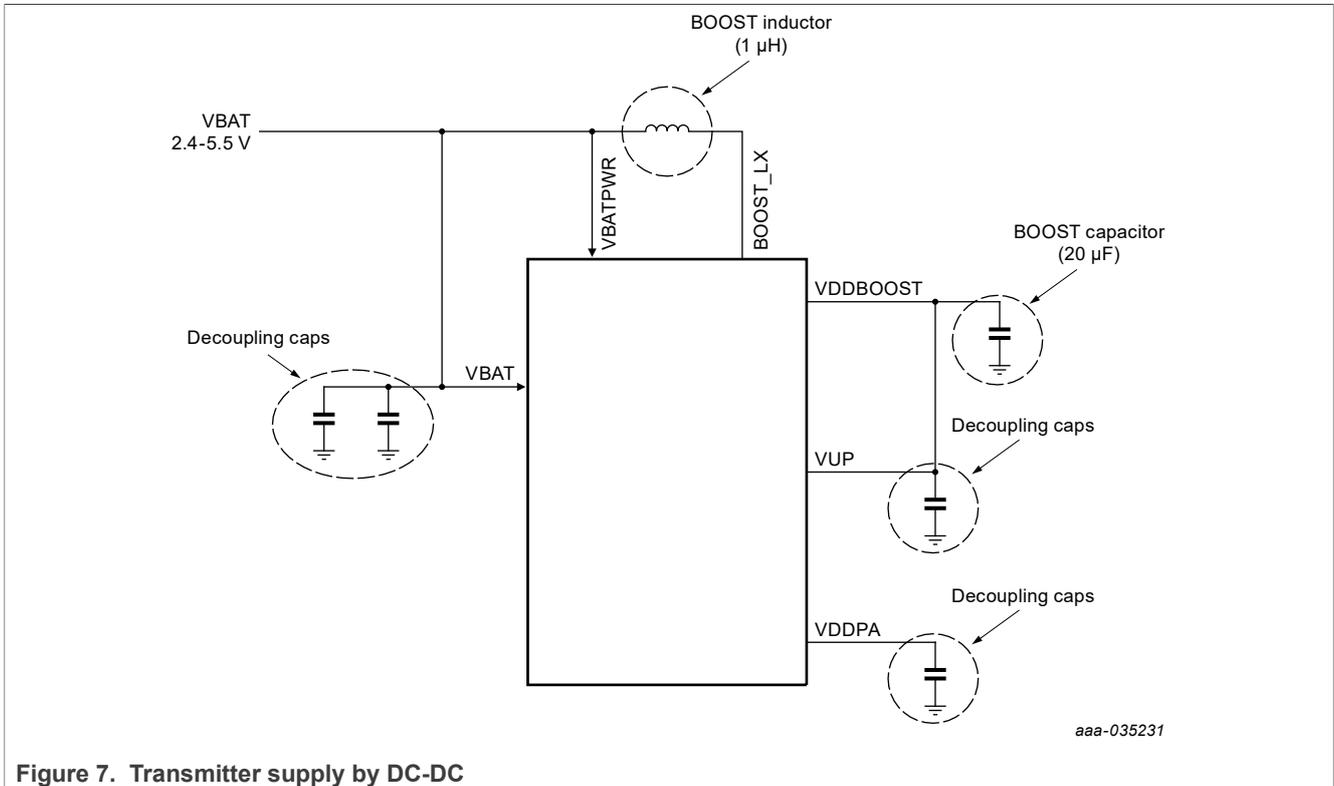
**Figure 7. Transmitter supply by DC-DC**

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### 9.6.3.4 Configuration example 1: TX_LDO transmitter supply - DC-DC active

VBAT is connected to VBATPWR.
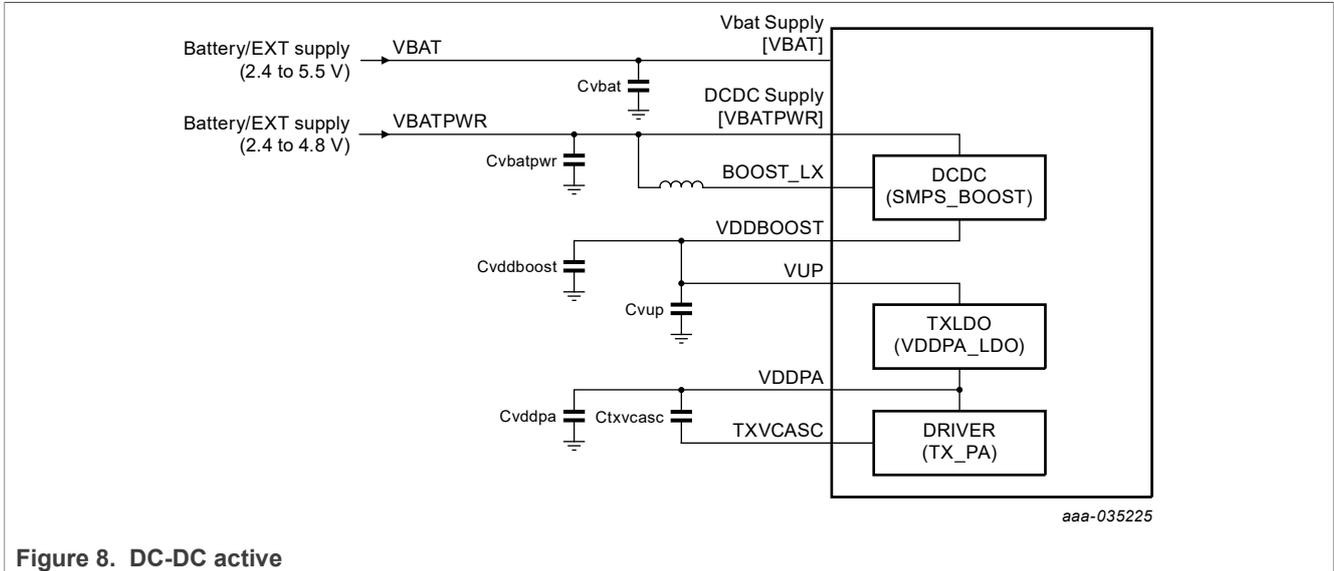


**Figure 8. DC-DC active**

### 9.6.3.5 Configuration example 2: TX_LDO transmitter supply - DC-DC bypassed

VBAT is connected to VBATPWR.
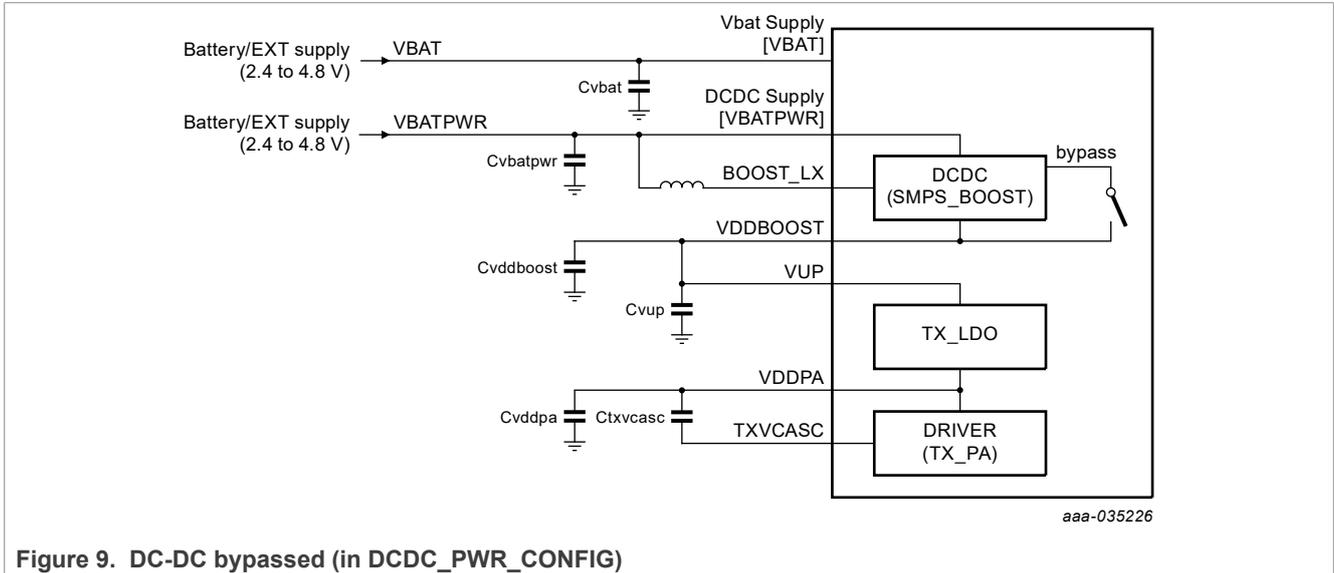


**Figure 9. DC-DC bypassed (in DCDC_PWR_CONFIG)**

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### 9.6.3.6 Configuration example 3: TX_LDO transmitter supply connected to VBAT - no DC-DC

VBAT is connected to VBATPWR.



**Figure 10. No DC-DC used**
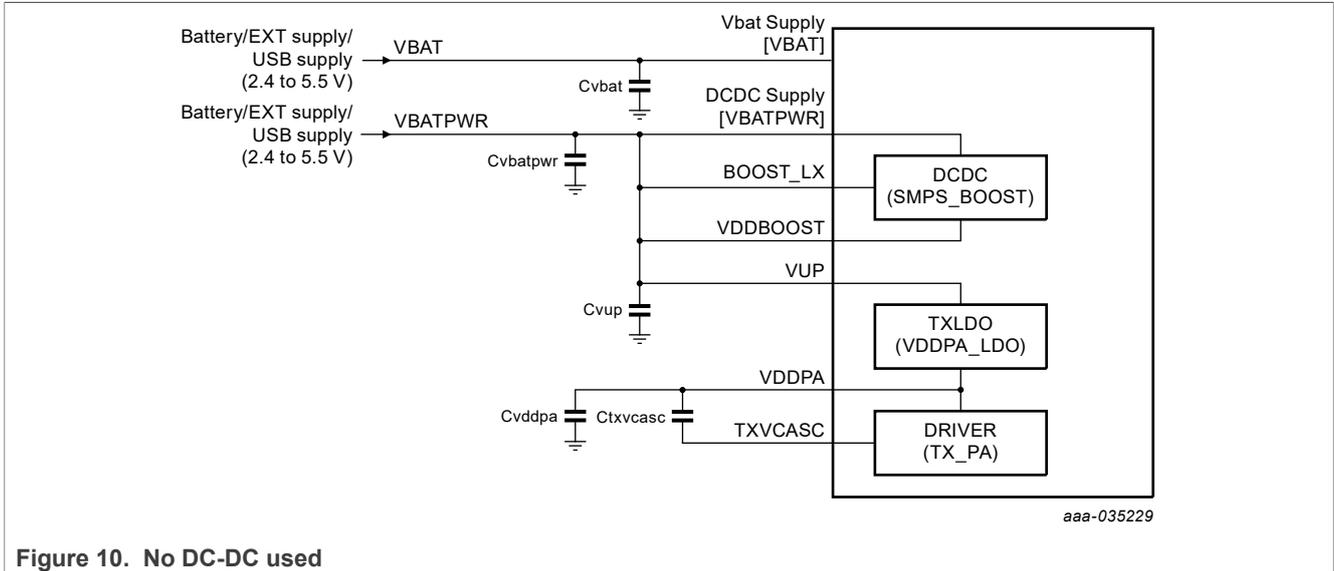
### 9.6.3.7 Configuration example 4: TX_LDO supplied independent from VBAT - no DC-DC

VBAT is connected to VBATPWR.



**Figure 11. No DC-DC used**
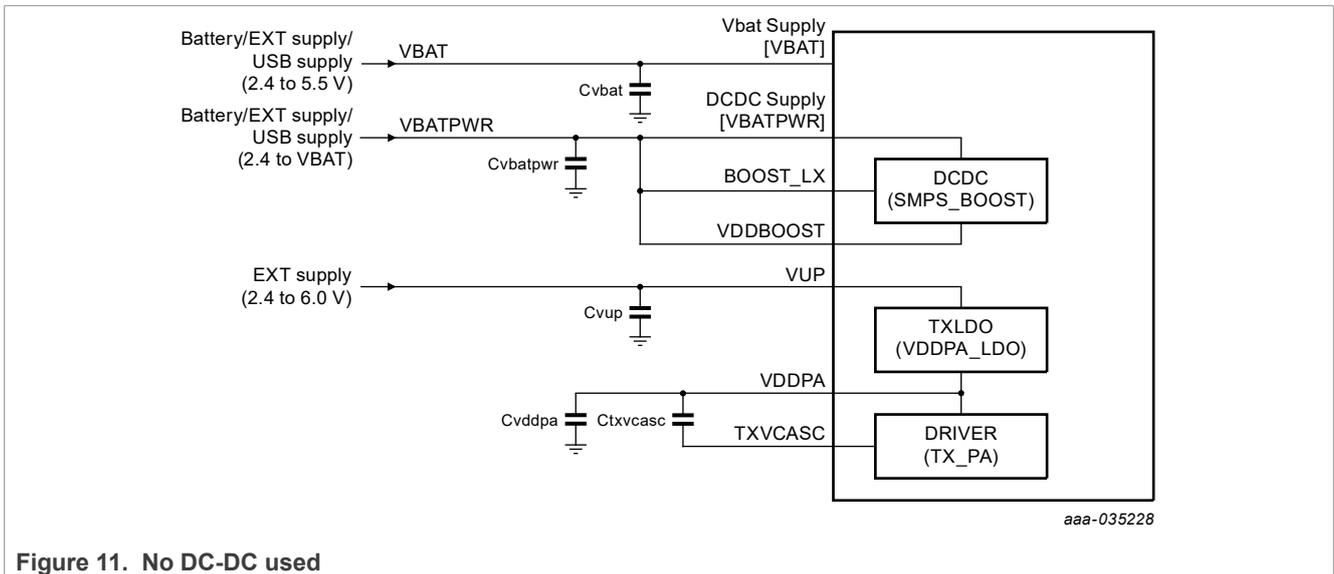
### 9.6.3.8 Configuration example 5: TX_LDO not used - no DC-DC

VBAT is connected to VBATPWR.



**Figure 12. No DC-DC used - no TX_LDO**
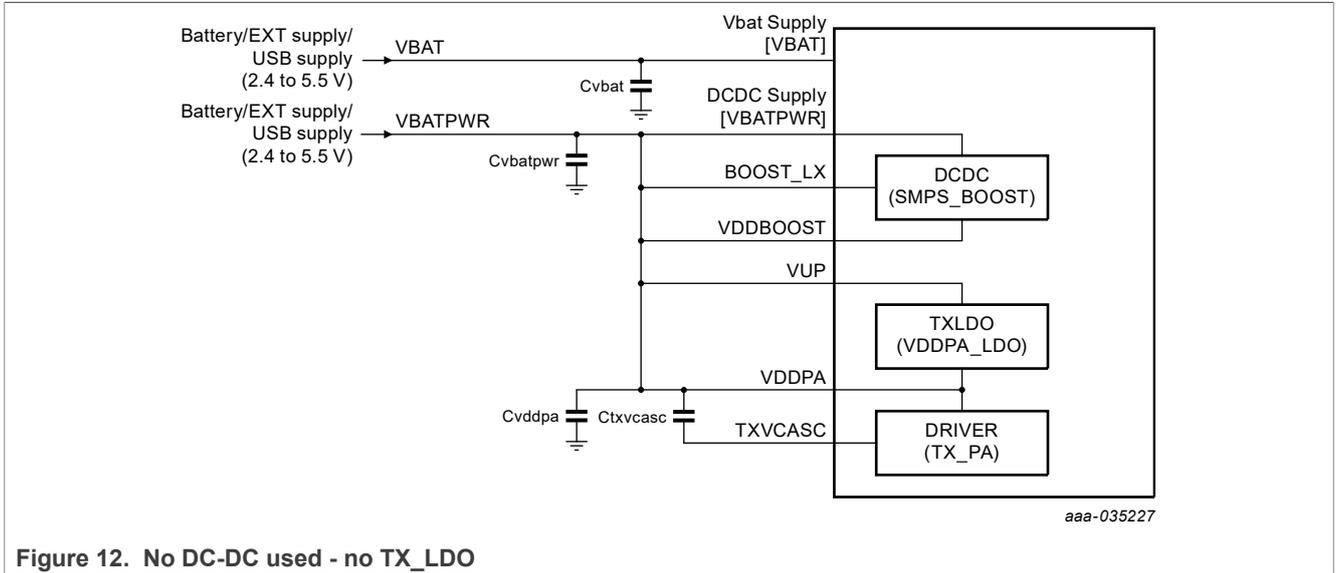
### 9.6.3.9 Supply voltage range for transmitter supply configuration examples

**Table 5. Supply voltage range configuration**

| Supply | Config1:<br>TX_LDO transmitter supply<br>DC-DC active | Config2:<br>TX_LDO transmitter supply<br>DC-DC bypassed | Config3:<br>TX_LDO transmitter supply connected to VBAT<br>no DC-DC | Config4:<br>TX_LDO supplied independent from VBAT<br>no DC-DC | Config5:<br>TX_LDO not used<br>no DC-DC |
|---|---|---|---|---|---|
| EEPROM configuration for DPC ENABLED - configured in DPC_CONFIG (address 0076h) | | | | | |
| DCDC_PWR_CONFIG (address 0000h) | - 0xE4(Variable BOOST with Auto Bypass).<br>- 0xE2(Fixed BOOST) | 0xE4 (Variable BOOST with Auto Bypass) | 0x01 | 0x01 | NA |
| TXLDO_VDDPA_HIGH (0x06) | 0x0 (1.5 V) | 0x0(1.5 V) | 0x0(1.5 V) | 0x0(1.5 V) | NA |
| TXLDO_VDDPA_MAX_RDR (0008h) | 0x2A(5.7 V) | 0x2A(5.7 V) | 0x2A(5.7 V) | 0x2A(5.7 V) | NA |
| BOOST_DEFAULT_VOLTAGE (000Ah) | 0x1D (6 V). | NA | NA | NA | NA |
| EEPROM configuration - DPC DISABLED - configured in DPC_CONFIG (address 0076h) | | | | | |
| DCDC_PWR_CONFIG (address 0000h) | - 0xE4(Variable BOOST with Auto Bypass).<br>- 0xE2(Fixed BOOST) | 0xE4 (Variable BOOST with Auto Bypass) | 0x21 | 0x21 | 0x00 |
| TXLDO_VDDPA_HIGH (0x06) | 0x0 (1.5 V) | 0x0(1.5 V) | 0x0(1.5 V) | 0x0(1.5 V) | 0x0(1.5 V) |
| TXLDO_VDDPA_MAX_RDR (0008h) | NA | NA | NA | NA | NA |
| BOOST_DEFAULT_VOLTAGE (000Ah) | 0x1D (6 V). | NA | NA | NA | NA |

**Table 6. Supply voltage range**

| Supply | Config1:<br>TX_LDO transmitter supply<br>DC-DC active | Config2:<br>TX_LDO transmitter supply<br>DC-DC bypassed | Config3:<br>TX_LDO transmitter supply connected to VBAT<br>no DC-DC | Config4:<br>TX_LDO supplied independent from VBAT<br>no DC-DC | Config5:<br>TX_LDO not used<br>no DC-DC |
|---|---|---|---|---|---|
| VBAT | 2.8 V … 4.8 V | 2.8 V … 4.8 V | 2.4 V … 5.5 V | 2.4 V … 5.5 V | 2.4 V … 5.5 V |
| VBATPWR | 2.8 V ... 4.8 V | 2.8 V … 4.8 V | 2.4 V … 5.5 V | 2.4 V ... 5.5 V | 2.4 V … 5.5 V |
| VUP | 3.1 V … 6.0 V | 2.8 V … 6.0 V | 2.4 V ... 6.0 V | 2.4 V … 6.0 V | 2.4 V … 5.5 V |
| VDDPA | VUP-0.3V drop of TX_LDO. max 5.7 V | VBATPWR - 0.5 V voltage drop | internally connected to TX_LDO | internally connected to TX_LDO | 2.4 V … 5.5 V |

## 9.7 Clock generation

The device supports the operation with two clock options, which is configured in EEPROM address CLK_INPUT_FREQ (0012h).

One option is clocking by a crystal (default), the other a clocking by an external clock input frequency.

It is important to consider additional phase noise introduced, for example by clock drivers in the design. Phase noise of the external clock has an impact on the RF performance which can be achieved.



READER IC

XTAL1    XTAL2

27.12 MHz

*001aam308*
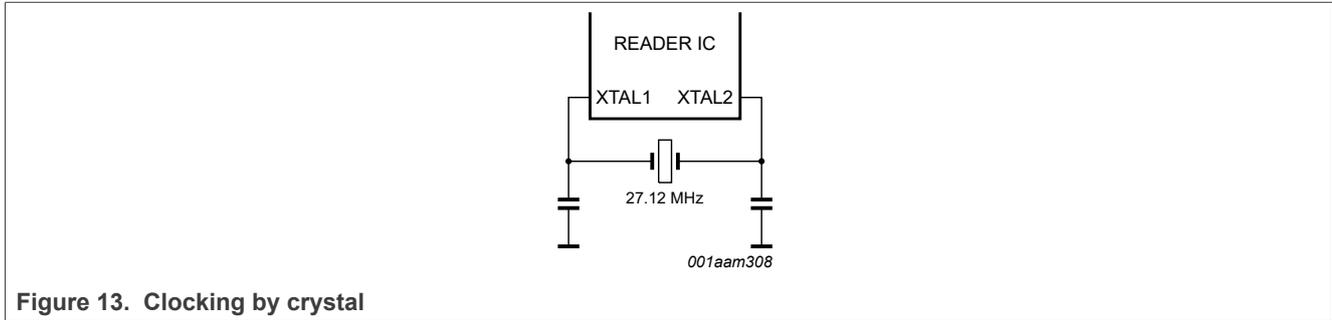
**Figure 13. Clocking by crystal**

## 9.8 External interfaces

The PN7220 requires the connection of a power supply, and a clock source like crystal or external clock and a host microcontroller connected to at least one NCI host interface for operation.

Additional connections of the package require the connection of stabilizing capacitors and ground.

The RF interface connects transmitter and receiver to the EMC filter of a connected antenna matching network. Additional connections are available for the GPIOs (on PN7220 only outputs are implemented).

The device supports the connection of up to 3x TDA8035 contact reader ICs which allow to realize an ISO/IEC7816 compliant interfaces.

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## 9.9 Transmitter overcurrent and temperature protection

The PN7220 implements different mechanisms to protect the chip against damage.

On the one hand, an overcurrent protection exists which shuts down the transmitter driver if there is a out of spec current. This can be enabled in EEPROM TXLDO_CONFIG (0002h), bit 11: overcurrent enable (0: disable, 1: enable)

An NCI notification is used to indicate the shut-down of the transmitter driver to a connected host.

On the other hand, an internal temperature sensor allows to monitor the temperature of the chip. This is configured in the EEPROM TEMP_WARNING (0648h). Three temperatures can be configured: 114 °C, 2:125 °C, 3:130 °C.

An NCI notification is used to indicate this temperature warning to a connected host.

The actual measured temperature is available in the register TEMP_SENSOR (005Bh). The chip will go into standby immediately.

This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

## 9.10 Dynamic power control (DPC)

The DPC is used for a special antenna tuning, called "symmetric antenna tuning". For an "asymmetric antenna tuning", the DPC is not required.

However, even for "asymmetric antenna tuning" with high output power needs, it might turn out that the RF field is too strong near of the antenna to be compliant with ISO/IEC14443 requirements. In this case, the DPC can be used as well to reduce the RF output power dependent on the distance of the card from the reader antenna.

The DPC works very well with a tuning called "symmetric tuning". With symmetric tuning, a detuning of the antenna is causing a reduction of the antenna impedance. This low antenna impedance might lead to a current which is too high for the targeted application. The DPC allows to limit the transmitter current even under antenna detuning conditions.

DPC is useful:

- To achieve NFC Forum and ISO/IEC 14443 compliancy (e.g. NFC Forum Power Transfer Maximum, ISO/IEC 14443 Field Emission Maximum)
- To improve interoperability

The Dynamic Power Control (DPC 2.0) allows controlling the transmitter driver voltage in 100 mV steps dependent on the actual transmitter current.

A lookup table is used to configure the transmitter output voltage and by this control the RF output power.

**The DPC allows to define two different targets current and maximum VDDPA settings for the two available modes to address EMVCo and NFC-related requirements with the same antenna.**

Features of the Dynamic power control (DPC 2.0):

• True current measurement provides maximum information for the regulation loop
• The transmitter current can be limited and additionally reduced according to detected transmitter current condition / antenna detuning condition
• DPC works autonomously without host interaction causing no additional processing load on the host
• Fastest response time of 1 ms for regulation

• Used for adaptive waveshape control (AWC)
• Used for adaptive RX sensitivity control (ARC)

The DPC is able to operate in two modes:

1. Current limiting mode
2. Current limiting + Current reduction mode

The DPC is configured in the EEPROM, this configuration is used after startup. This avoids that the host must configure the chip after each reset or power off.

The following EEPROM registers are most relevant for the DPC configuration:

**DPC_Config:** Enables/Disables the DPC (enable: 0x39, disable: 0x00)

**DPC_TargetCurrent:** Unloaded VDDPA target current in mA, the target current +/- Hysteresis is limiting the current for the DPC.

• The DPC_TargetCurrent is the current which can be measured for the selected antenna impedance and transmitter supply voltage in unloaded condition. This is the current the system is designed to operate at. For each of the modes - NFC Forum and EMVCo, one dedicated configuration does exist:
DPC_TargetCurrent_EMVCO
DPC_TargetCurrent_NFC
VDDPA_max_EMVCo
VDDPA_max_NFC
All other DPC-related settings are used for both modes.

**DPC_Hysteresis:** Absolute difference to current target current in mA that triggers a DPC update event.

• The configuration of the hysteresis ensures, that the DPC is not regulating if small changes of the transmitter current occur due to external disturbances. A typical value for the DPC_Hysteresis is e.g. 20 mA.

**DPC_Lookup_Table:** configures the current reduction

The DPC_LOOKUP_TABLE allows, in addition to the limitation of the current, to configure:

• an additional current reduction on top of the current limitation, achieved by further lowering the transmitter supply voltage
• a relative change of modulated amplitude level
• and a relative change of falling and raising edge time constant for ASK10 % and ASK100 % modulations

This lookup table is initialized with 0x00 for devices delivered from the factory. (The customer development board is already initialized with useful data in EEPROM which work well with the antenna of the board).

The 0x00 entry in the DPC_LOOKUP_TABLE means that no additional function then the current limitation takes place for the DPC.

In order to achieve a limitation of the current even in the case of an antenna impedance that is lowered, the Transmitter supply voltage is reduced accordingly.

This transmitter supply voltage reduction is now used as index for the DPC_LOOKUP_TABLE.

For a specific transmitter supply voltage, it is possible to further reduce the current below the value of DPC_TargetCurrent or to configure parameters for waveshaping and modulation. All these entries are relative values, granularity of the entries dependent on the transmitter supply voltage is 0.1 V, resulting in 42 table entries.

The DPC updates the content of the following register dependent on the antenna load / lookup table configuration:

0x30 - DGRM_RSSI
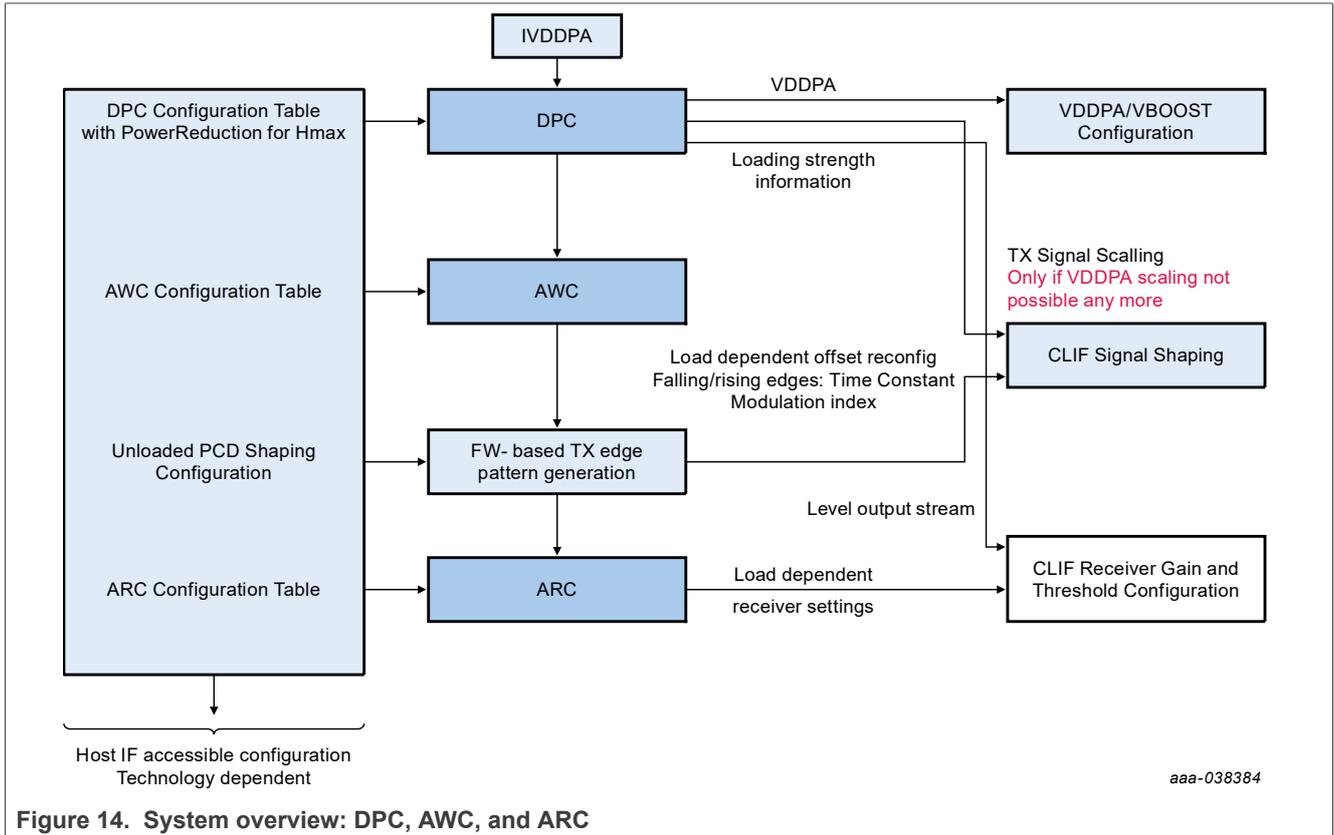
Figure 14.  System overview: DPC, AWC, and ARC
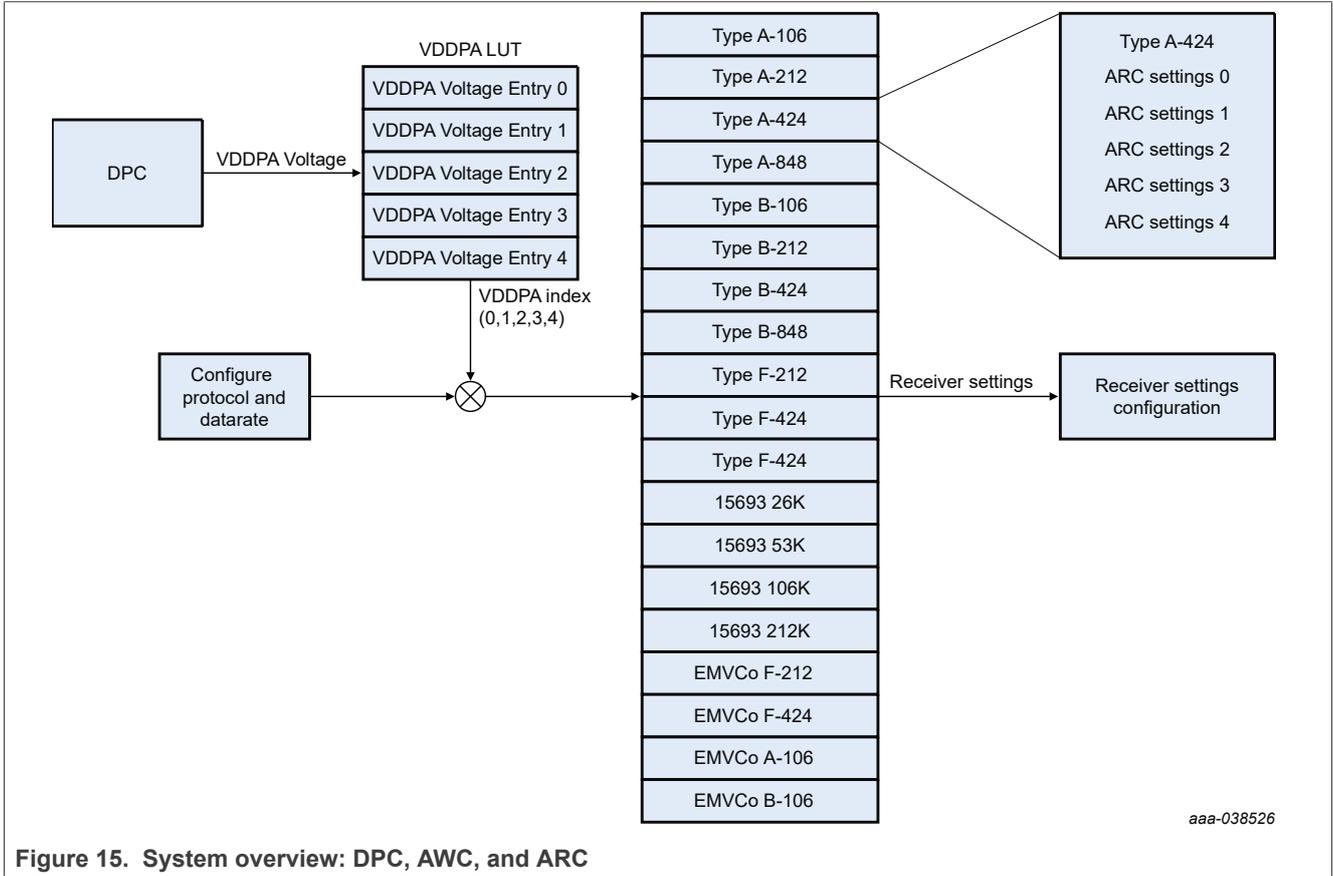
**Figure 15.  System overview: DPC, AWC, and ARC**
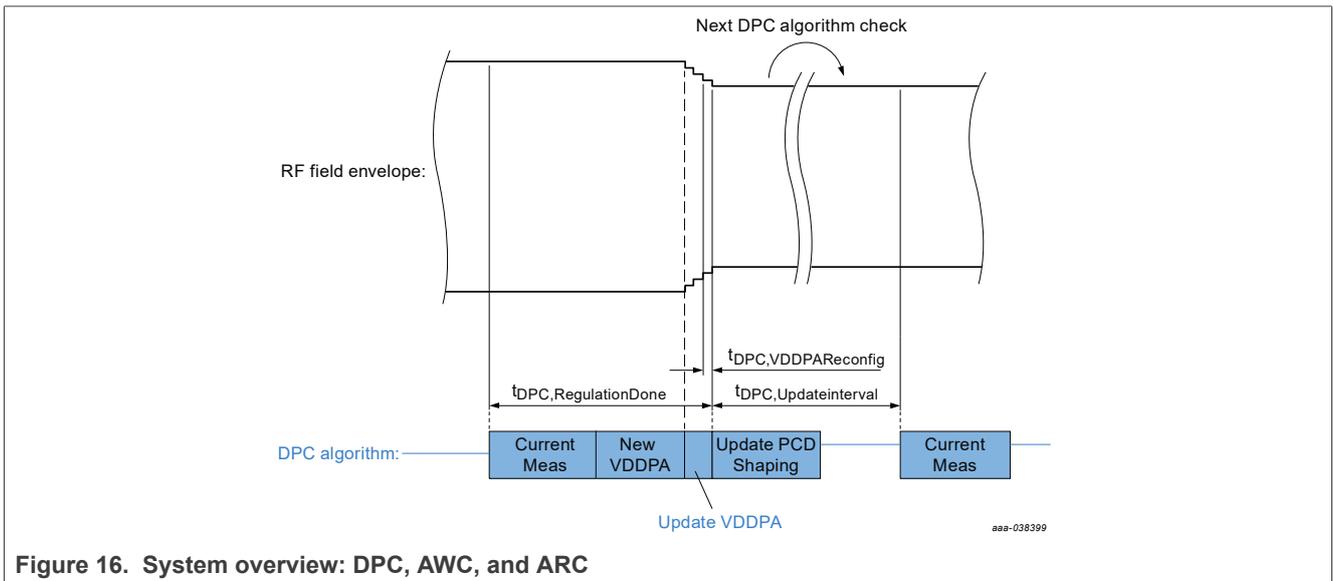


**Figure 16.  System overview: DPC, AWC, and ARC**
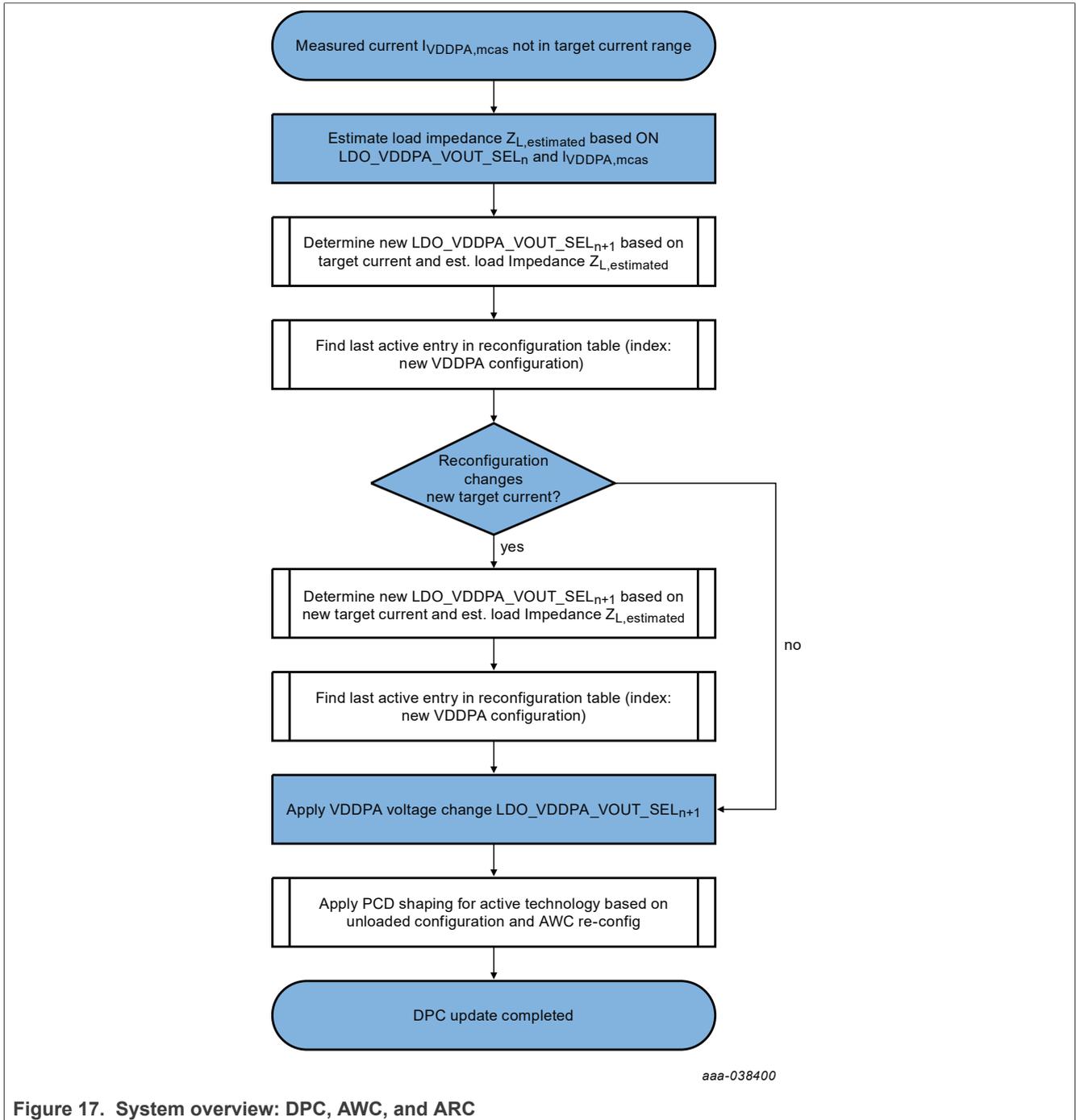
**Figure 17.  System overview: DPC, AWC, and ARC**

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### 9.10.1 DPC algorithm

The DPC algorithm is controlling the transmitter current. It is using the following states:

1. Current measurement: Performs VDDPA current measurement
2. New VDDPA: Determine new VDDPA configuration based on measured current
   VDDPA New (for target current of Itarget) = VDDPA Voltage / VDDPA current * Itarget
3. Update VDDPA: Perform output power update
4. Update PCD Shaping: Apply AWC configuration updates for active technology
5. Update RX sensitivity parameter only for short duration

Reconfiguration table includes Relative changes of target current and of waveform parameters adaption for all VDDPA voltage configurations. The VDDPA configuration is implicitly defined by the row index. The first row refers to LDO_VDDPA_VOUT_SEL=0 (represents 1V5).

EXAMPLE:

Unloaded configuration After Field ON:

VDDPA max set to 42 (5.7 V) ·target current set to 280 mA

Technology B106: amp_mod=200

Falling edge time constant=rising edge time constant=3

**Table 7. DPC_LOOKUP_TABLE element, defining the configuration for one dedicated VDDPA voltage**

| Function | Bit | Description |
|---|---|---|
| ENTRY 0 | 31:0 | This is the entry for 1.5 V. |
| Target current reduction | 31:23 | ENTRY 0 -LSB - byte 0<br>Voltage step between DPC entries = 100 mV. Voltage offset start = 1.5 V bEntry_00 = 1V5 ... bEntry_42 = 5V7<br>Bits[7:0] = Target current reduction in mA (unsigned) |
| AWC amp mod change | 23:16 | ENTRY 0 - byte 1<br>Bits[7:0] = Relative change of modulated amplitude level (signed) |
| AWC edge time constant for ASK100 | 15:8 | ENTRY 0 - byte 2<br>Bits[3:0] = ASK100, Relative change of falling edge time constant (signed)<br>Bits[7:4] = ASK100, Relative change of rising edge time constant (signed) |
| AWC falling edge time constant for ASK10 | 7:0 | ENTRY 0 -MSB - byte 4<br>Bits[3:0] = ASK10, Relative change of falling edge time constant (signed)<br>Bits[7:4] = ASK10, Relative change of rising edge time constant (signed) |

Loaded configuration After Field ON:

DPC regulates from unloaded VDDPA configuration 42 to 31. Consequently, new configuration to be applied based on index entry 31.

Target current stays at 280 mA.

Technology B106: amp_mod=205, falling edge time constant=2, rising edge time constant=0

## 9.11  Adaptive waveshaping control (AWC)

Depending on the level of detected detuning of the antenna, waveshaping related register settings can be automatically updated.

Two different waveshaping mechanisms can be used:

1. Firmware based shaping (1,2,3)

2. Lookup table based shaping (4,5,6)

The firmware based shaping allows to correct rise times and overshoot with linear transition shapes.

The lookup table based shaping allows maximum flexibility and enables to configure almost any possible correction.
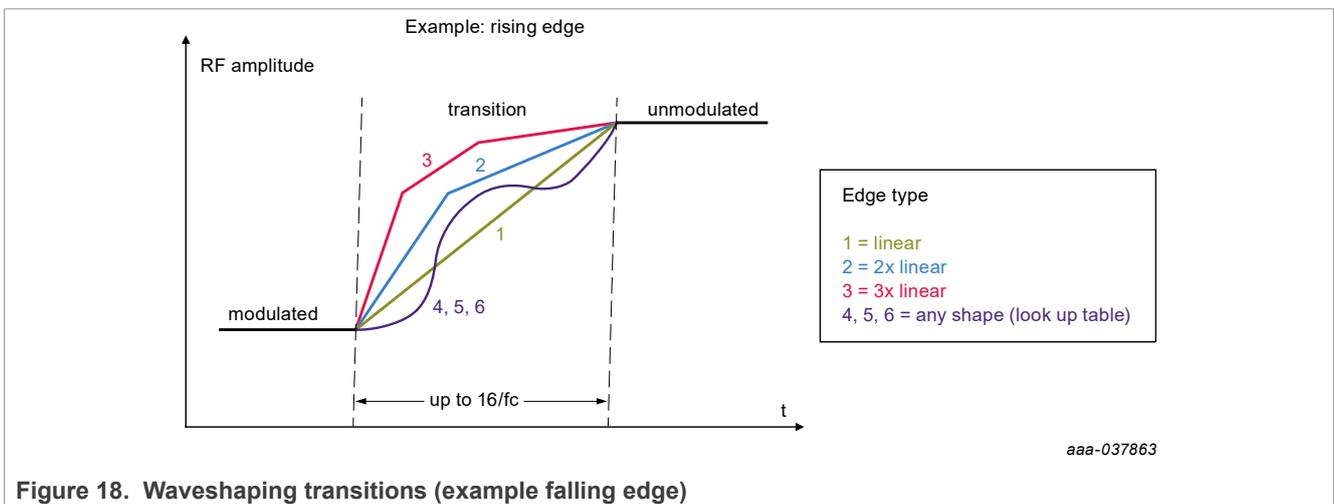


**Figure 18.  Waveshaping transitions (example falling edge)**

The shaping related register settings are stored in a lookup table located in EEPROM, and selected dependent on the actual detected detuning condition.

Each lookup table entry allows the configuration not only of a dedicated waveshaping configuration for the corresponding detuning condition. But allows in addition to configure the waveshaping individually dependent on the actual protocol which is active.

Features of the Adaptive Waveshape Control:

• No external components required

• No need to compromise antenna matching to meet waveshape requirements

• Waveshapes automatically adapted according to detected detuning condition

• RF standards define envelope timing and residual carrier parameters required for compliance and interoperability.

The device supports the design of compliant antennas by allowing to actively shaping the style of edge transition for falling and rising edges. The shaping of modulation edges is achieved by selecting one from three edge transition styles:

1. Linear transition between two amplitude levels

2. Two linear transitions between amplitude levels and

3. Three linear transitions between amplitude levels.

The type of the transition is selected in the EEPROM registers EDGE_TYPE_(protocol). It can be defined independent for each RF protocol and data rate - for both falling and rising edge.

The EEPROM registers EDGE_STYLE_(protocol) define the time constant "s" of falling/rising edge (depends on edge style).

The EEPROM registers EDGE_LENGTH_(protocol) define the total length of the edge pattern.

Figure 19 to Figure 21 illustrate the edge type for the falling edge.



**Figure 19. One linear transition (example falling edge)**



**Figure 20. Two linear transitions (example falling edge)**
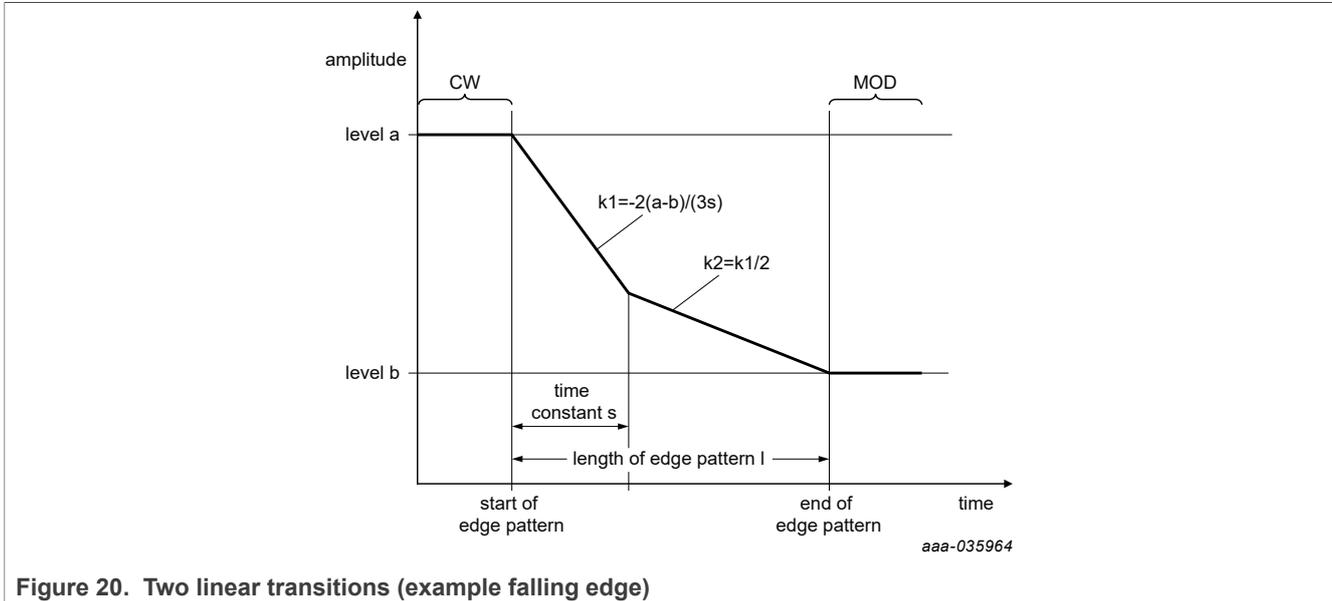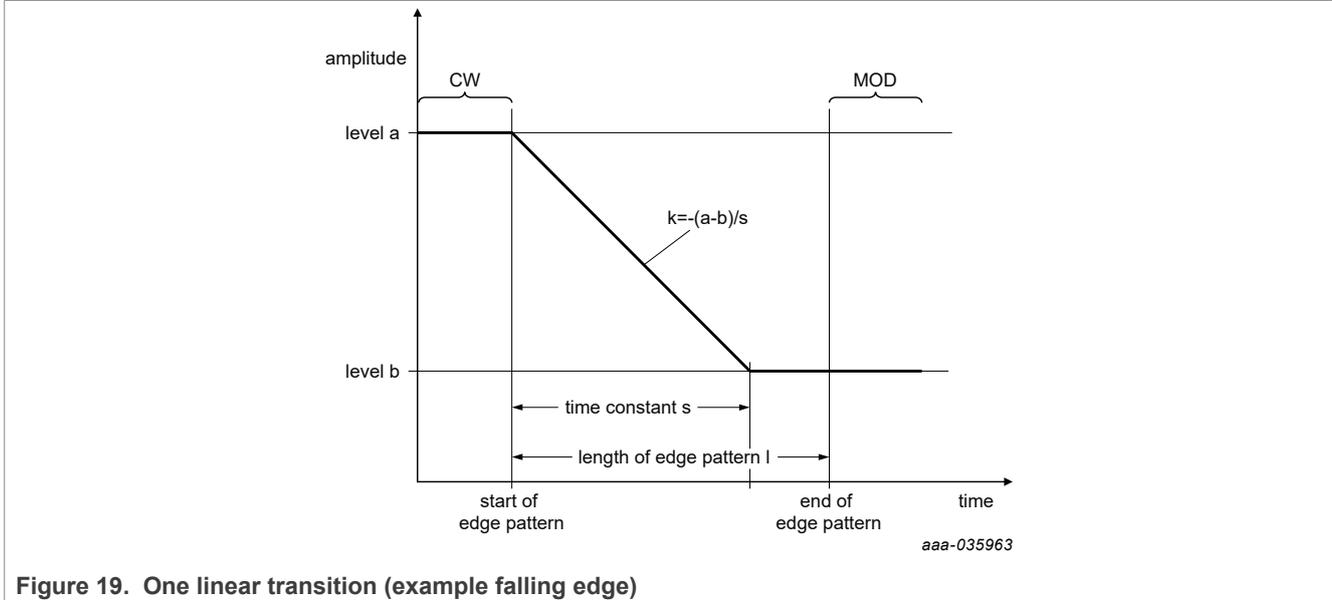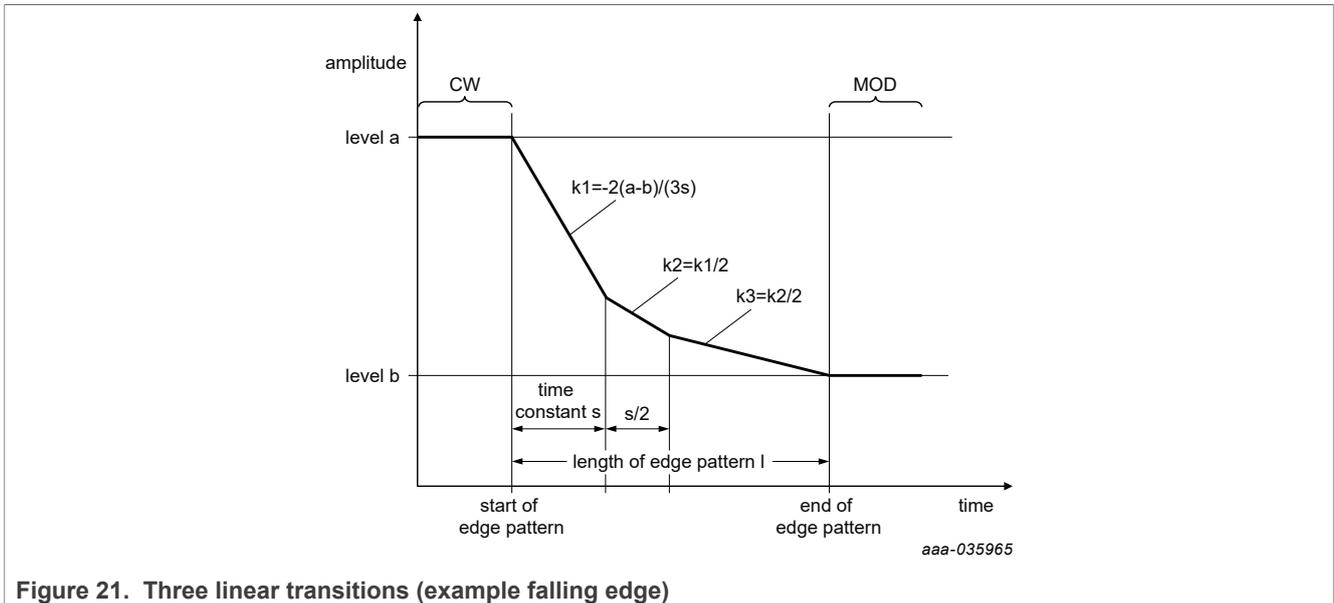
**Figure 21. Three linear transitions (example falling edge)**

The transition patterns are used as implicit pre-distortion to compensate effects of TX loading circuitry (for example, resonant circuitry parameters) to the emitted RF envelope.

## 9.12 Adaptive receiver control (ARC)

Depending on the level of detected antenna detuning, receiver-related register settings can be automatically updated. The receiver-related registers which are allowed to be dynamically controlled are:

DGRM_RSSI_REG (30h) ->DGRM_SIGNAL_DETECT_TH_OVR_VAL

SIGPRO_RM_TECH_REG (22h) ->RM_MF_GAIN,

The adaptive receiver control settings override the default RM_MF_GAIN and DGRM_SIGNAL_DETECT_TH_OVR_VAL settings configured by the command LOAD_RF_CONFIGURATION (0Dh).

The ARC algorithm is called when VDDPA voltage changes after DPC. There are two lookup tables used in ARC algorithm i.e VDDPA lookup and ARC lookup. In case of a VDDPA change, an EEPROM lookup (at current protocol and baud rate) is performed. The receiver-related settings i.e RM_MF_GAIN, DGRM_SIGNAL_DETECT_TH_OVR_VAL and IIR_ENABLE are read from EEPROM lookup table and configured in registers.

**VDDPA lookup table:**

VDDPA lookup table defines a maximum of five voltage ranges. Number of VDDPA voltage ranges used in ARC algorithm is configured in bArcConfig[2:0]. VDDPA voltage output from DPC algorithm is input to VDDPA lookup. VDDPA lookup returns VDDPA_range_index (i.e 0,1,2,3,4).

**Table 8. ARC_VDDPA EEPROM configuration bit description**

| Function | Bit | Description |
|---|---|---|
| ARC VDDPA Setting | 7:0 | Byte[4] = ARC_VDDPA_0: ARC_VDDPA_3 > VDDPA < ARC_VDDPA_4 |
| | 7:0 | Byte[3] = ARC_VDDPA_0: ARC_VDDPA_2 > VDDPA < ARC_VDDPA_3 |
| | 7:0 | Byte[2] = ARC_VDDPA_0: ARC_VDDPA_1 > VDDPA < ARC_VDDPA_2 |
| | 7:0 | Byte[1] = ARC_VDDPA_0: ARC_VDDPA_0 > VDDPA < ARC_VDDPA_1 |

**Table 8. ARC_VDDPA EEPROM configuration bit description**...*continued*

| Function | Bit | Description |
|---|---|---|
| | 7:0 | Byte[0] = ARC_VDDPA_0: 1.5 > VDDPA < ARC_VDDPA_0 |

**ARC lookup table:**

**VDDPA index** and **RF protocol/datarates** are input to ARC lookup. There are five Receiver settings entries for each protocol and data rates. ARC algorithm select one out of five entries (at current protocol and baud rate) based on VDDPA_range_index.

Table 9 shows ARC settings for Type A-106.

**Table 9. ARC_RM_A106 EEPROM configuration bit description**

| Function | Bit | Description |
|---|---|---|
| RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT,<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT,<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT,<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Table 9. ARC_RM_A106 EEPROM configuration bit description**...*continued*

| Function | Bit | Description |
|---|---|---|
| RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT,<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

*Note:* *For ISO14443-A: In case ARC is disabled, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default))*

*Note:* *For ISO14443-A: In case Bit[15] is configured to 0, it requires DPC_ SIGNAL_DETECT_TH_OVR_VAL larger than 0x50 (with MF_GAIN = 2 (default)) if the ARC is enabled.*

## 9.13 Energy-saving card detection

The low-power card detection (LPCD) is an energy-saving card polling configuration for the PN7220. During LPCD, a host microcontroller can be set into power-saving mode, as no host controller interaction is required.

A low frequency timer is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short pulse which allows to detect a detuning of the antenna. In case of a detected antenna detuning, the system is woken up from power-saving mode. It sends an interrupt signal to the connected host microcontroller to wake up the host microcontroller from power-saving mode and to indicate a change of the antenna detuning condition.

A low frequency timer is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short pulse which allows to detect a detuning of the antenna. In case of a detected antenna detuning and the system is woken up from power-saving mode.

There is no trimming for the Low Frequency Timer required.

The NCI configuration is enabled to enter the LPCD mode with a total duration once a RF_DISCOVER_CMD is issued by the DH.

### 9.13.1 Low-power card detection (LPCD)

The low-power card detection (LPCD) is an energy-saving card polling configuration for the PN7220. During LPCD, a host microcontroller can be set into power-saving mode, as no host controller interaction is required. The host microcontroller is woken up from power-saving mode by an IRQ send by the PN7220.

A low frequency oscillator (there is no trimming for the low frequency oscillator required) is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short RF pulse. This RF pulse allows to detect a detuning of the antenna by presence of conductive objects in proximity of the antenna (card, cell phone, metal).

In case of a detected antenna detuning, the system wakes up from power-saving mode. It sends an interrupt signal to the connected host microcontroller to wake up the host microcontroller from power-saving mode and to indicate a change of the antenna detuning condition.

A low frequency oscillator (LFO) is implemented to drive a wake-up counter, waking-up PN7220 from Standby mode. This allows implementation of low-power card detection polling loop at application level.

The host microcontroller can then perform a card polling sequence to verify if the technology of the object causing the antenna detuning is supported by the system.

Before entering the LPCD mode, ADC_I and ADC_Q reference value must be determined. This is done during the so-called calibration.

**LPCD calibration phase**

a) An initial calibration measurement is performed to set up the RX chain parameters namely HFATT, DCO_DAC_I_CTRL and DCO_DAC_Q_CTRL values.

b) The next measurement is done using the RX chain parameters that are set up, to arrive at the ADC_I and ADC_Q values which are used as reference values. All following LPCD measurements are done relative to the LPCD calibration measurement.

**The LPCD loop** itself works in two phases:

First the standby phase is controlled by the wake-up counter (timing defined in the instruction), which defines the duration of the standby of the PN7220.

Second phase is the detection-phase. The RF field is switched on for a defined time (EEPROM configuration) and then the ADC_I and ADC_Q values are compared to a reference value.

- If the ADC_I and ADC_Q values exceed the reference value, PN7220 will wake-up from standby and shall try to perform Technology detection and if successful RF_INTF_ACTIVATED_NTF shall be sent to Device Host.
- If the ADC_I and ADC_Q values do not exceed the thresholds of the reference value, then PN7220 will enter into standby mode again.

These two phases are executed in a loop until:

- Card / metal is detected (LPCD_IRQ is raised).

- Reset occurs, which resets all the system configurations. The LPCD is also terminated in this case.

- NTS on host interface

- RF Level Detected

The behavior of the generated field is different dependent on the activation state of the DPC function:

- If the DPC feature is not active, the ISO/IEC14443 type A 106 kbit/s settings are used during the sensing time.
- If the DPC is active, the RF_ON command is executed. The RF field is switched on as soon as the timer configured by the SWITCH_MODE command elapses. The RF field is switched on for a duration as defined

for an activated DPC. The timer for the LPCD_FIELD_ON_TIME starts to count as soon as the RF_ON command terminates.

**Table 10. Low-Power Card Detection: relevant EEPROM configuration**

| Name | Description |
|---|---|
| LPCD_AVG_SAMPLES | Defines how many samples of the I and Q values are used for the averaging. Used to optimize the system to achieve highest detection sensitivity versus false alarms. |
| LPCD_RSSI_TARGET | Value to be used as the RSSI target in the calibration phase to arrive at the RX chain parameters.<br>This parameter is used to arrive at an optimal target voltage level at RXP. |
| LPCD_RSSI_HYST | Value to be used as the RSSI hysteresis in the calibration phase to arrive at the RX chain parameters.<br>This is used to avoid oscillations while arriving at the target voltage level at RXP. |
| LPCD_THRESHOLD | If the difference between the measured value of I/Q and the reference value for I/Q is greater than the threshold on either channels, then a card is detected. |
| LPCD_VDDPA | VDDPA voltage when DC-DC (internal or external) or external power source is used to feed TXLDO |
| XTAL_CHECK_DELAY | Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18.8 us). For fastest startup this time, a check is performed at a time slightly higher than the expected startup time of the crystal. |

**Table 11. Low-Power Card Detection: relevant EEPROM configuration**

| Name | Description |
|---|---|
| LPCD_AVG_SAMPLES | Defines how many samples of the I and Q values are used for the averaging. Used to optimize the system to achieve highest detection sensitivity versus false alarms. |
| LPCD_RSSI_TARGET | Value to be used as the RSSI target in the calibration phase to arrive at the RX chain parameters.<br>This parameter is used to arrive at an optimal target voltage level at RXP. |
| LPCD_RSSI_HYST | Value to be used as the RSSI hysteresis in the calibration phase to arrive at the RX chain parameters.<br>This is used to avoid oscillations while arriving at the target voltage level at RXP. |
| LPCD_THRESHOLD | If the difference between the measured value of I/Q and the reference value for I/Q is greater than the threshold on either channels, then a card is detected. |
| LPCD_VDDPA | VDDPA voltage when DC-DC (internal or external) or external power source is used to feed TXLDO |
| XTAL_CHECK_DELAY | Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18,8us). For fastest startup this time, a check is performed at a time slightly higher than the expected startup time of the crystal. |

## 9.14 RF-level detection

The PN7220 implements an RF level detector (RFLD) and an NFC level detector (NFCLD) which allows to detect the presence of an external RF field.

The collision avoidance is not enabled for the EMVCo mode, and active for the NFC Forum mode.

**RF Level Detector:**

During low-power card detection (LPCD), the RF level detector (RFLD) acts as wake-up source from power-saving mode.

The purpose of the RFLD function is to detect any signal at 13.56 MHz in order to wake up the PN7220 from power-saving mode.

**NFC Level Detector:**

The NFC Level detector (NFCLD) is used during full power mode. The NFCLD function is required by NFC Forum to support the "RF collision avoidance".

The sensitivity of the NFCLD sensor can be configured by EEPROM register to meet the NFC Forum requirements.

It can be used as well in card mode to detect an external field.

## 9.15 Antenna connection

The PN7220 allows to connect antennas of different topology and matching to the transmitter.

Standard and recommended tuning of the antenna fitting to most applications is a symmetrical matched antenna connected to TX1, TX2 operating in push-pull operation.

VBAT is connected to VBATPWR.



*aaa-042788*
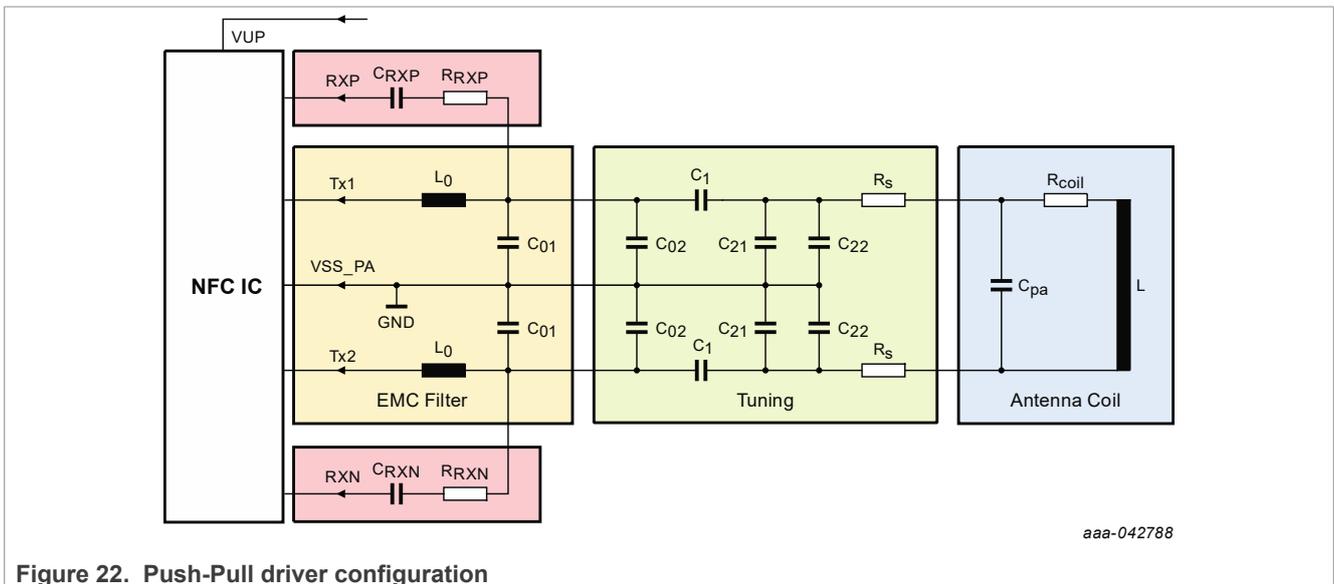
**Figure 22. Push-Pull driver configuration**

The PN7220 allows to operate the TX1, TX2 in common mode as well, which allows to use a single ended antenna. This configuration saves one EMC filter coil.

*Note:* *The RSSI target for SE must be calculated as follows and differs from the differential antenna:*

*RSSI target = Target RX Peak Voltage\*1024/ (1.8\*2)*

*Example: For a 1.2 V target: DGRM_RSSI_TARGET = 1.2 \* 1024 / (1.8\*2) = 341d = 0x155*
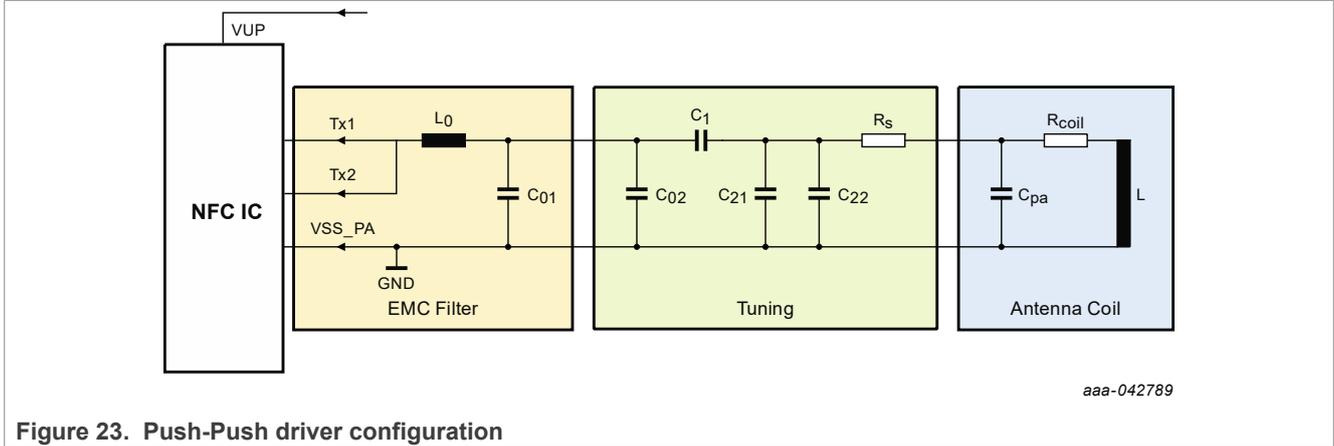


**Figure 23. Push-Push driver configuration**

**Table 12. Antenna register configuration**

| Register (Address) | Bit | Differential Antenna Push-Pull driver TX1, TX2 | Single-Ended Push-Push driver TX1, TX2 |
|---|---|---|---|
| SS_TX_CFG (0x15) | TX2_USE_TX1_CONF | 1b | 1b |
| SS_TX1_RMCFG (0x16) | TX1_CLK_MODE_TRANS_RM | 111b | 111b |
| SS_TX1_RMCFG (0x16) | TX1_CLK_MODE_MOD_RM | 111b | 111b |
| SS_TX1_RMCFG (0x16) | TX1_CLK_MODE_CW_RM | 111b | 111b |
| SS_TX2_RMCFG (0x17) | TX2_CLK_MODE_TRANS_RM | do not care | do not care |
| SS_TX2_RMCFG (0x17) | TX2_CLK_MODE_MOD_RM | do not care | do not care |
| SS_TX2_RMCFG (0x17) | TX2_CLK_MODE_CW_RM | do not care | do not care |
| DGRM_RSSI (0x30) | DGRM_RSSI_TARGET | direct entry | as per calculation for SE (RSSI target = Target RX Peak Voltage\*1024/ (1.8\*2)) |
| ANA_RX_CTRL (0x43) | RX_MIXER_SE_MODE_EN | 0 | 1 |
| ANACTRL_TX_CONFIG (0x44) | TX_INVP_RM | 10b | 00b |
| ANACTRL_TX_CONFIG (0x44) | TX_PWM_MODE_RM | 0b | 0b |

**Table 13. Antenna EEPROM configuration**

| EEPROM (Address) | Bit | Differential Antenna Push-Pull driver TX1, TX2 | Single-Ended Push-Push driver TX1, TX2 |
|---|---|---|---|
| TX_SHAPING_CONFIG (0x17) | 0 | 0 | 0 |

*Note:* *Recommendation is to use all the settings configured in EEPROM. For CLIF_SS_TX_CFG_REG, the value has to be configured in EEPROM for each technology and baud rate so that the value is loaded after every load protocol.*

## 9.16  RF debug signals

The following signals are available for debugging purposes:

The test signals are selected by sending a command string to the PN7220.

If used, **ADC-Q must be routed always to AUX1, ADC-I must be routed always to AUX2**.

The analog test signals are analog representation of an internal digital value. The internal digital signal is converted by an 8-bit wide DAC to the analog signal.

This overview indicates the signals which are available for debugging purposes (indicated by numbers):



*aaa-037146*
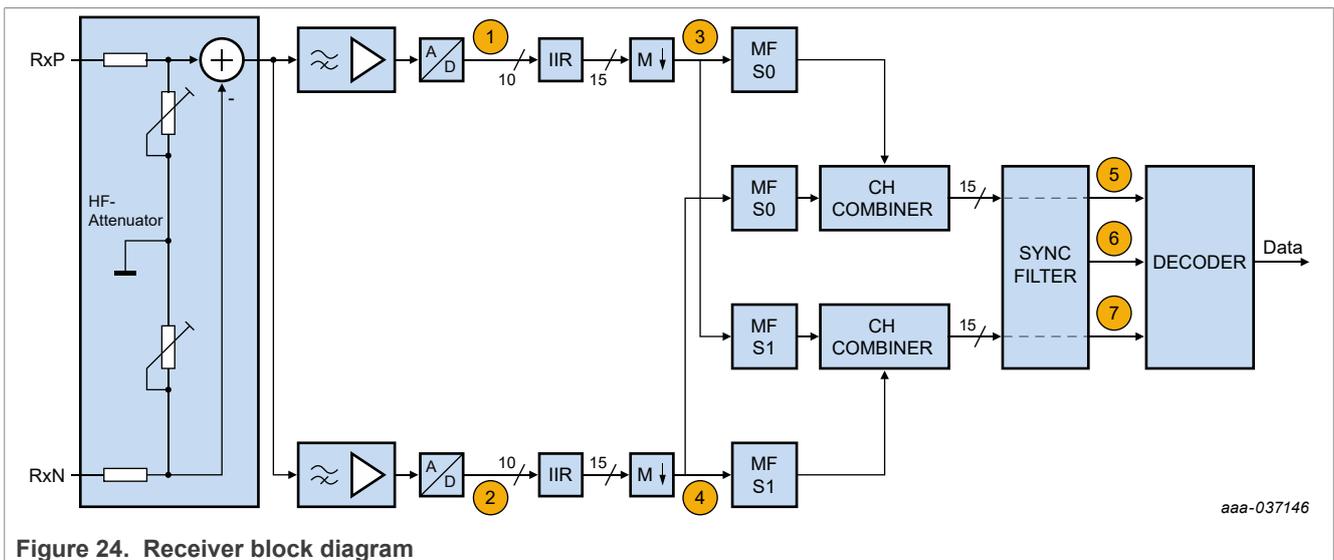
**Figure 24.  Receiver block diagram**

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**Table 14. DEBUG SIGNALS**

| Signal | REGISTER | SIGNAL NAME | BITS | Description |
|---|---|---|---|---|
| ADC Data I Channel (1) | obs_clif_ tbcontrol_ patchbox0 | adc_ data_i_i | 9:2 | Unfiltered I channel signal<br>upper 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9) |
| | obs_clif_ tbcontrol_ patchbox1 | | 9; 6:0 | Unfiltered I channel signal<br>lower 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9) |
| ADC Data Q Channel (2) | obs_clif_ tbcontrol_ patchbox2 | adc_ data_q_i | 9:2 | Unfiltered Q channel signal<br>upper 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9) |
| | obs_clif_ tbcontrol_ patchbox3 | | 9; 6:0 | Unfiltered Q channel signal<br>lower 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9) |
| Preprocessor Out I Channel (3) | obs_clif_sigpro_ rm0 | rm_cor_ adc_i_o | 14:8 | Pre-processed ADC data I channel<br>upper 7bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU |
| | obs_clif_sigpro_ rm1 | | 7:0 | Pre-processed ADC data I channel<br>lower 8bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling |
| Preprocessor Out Q Channel (4) | obs_clif_sigpro_ rm2 | rm_cor_ adc_q_o | 14:8 | Pre-processed ADC data I channel<br>upper 7bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU |
| | obs_clif_sigpro_ rm3 | | 7:0 | Pre-processed ADC data I channel<br>lower 8bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling |
| Output MF S0 (5) | obs_clif_sigpro_ rm4 | mf_pt_ s0_d | 14:8 | Delayed matched filter S0 output, after CH combiner<br>upper 7 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore) |
| | obs_clif_sigpro_ rm5 | | 7:0 | Delayed matched filter S0 output, after CH combiner<br>lower 8 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner |
| Output MF S1 (6) | obs_clif_sigpro_ rm6 | mf_pt_ s1_d | 14:8 | Delayed matched filter S1 output, after CH combiner<br>upper 7 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore) Remark: S1 is not relevant for type A 106 |
| | obs_clif_sigpro_ rm7 | | 7:0 | Delayed matched filter S1 output, after CH combiner<br>lower 8 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner Remark: S1 is not relevant for type A 106 |

**Table 14. DEBUG SIGNALS**...*continued*

| Signal | REGISTER | SIGNAL NAME | BITS | Description |
|---|---|---|---|---|
| Output Synchronization Filter (7) | obs_clif_sigpro_rm8 | sync_filt_out | 14:8 | Synchronization filter output<br>upper 7 bit of the 15 bit signed synchronization filter output including sign (bit14) bit 15: RFU (ignore) |
| | obs_clif_sigpro_rm9 | | 7:0 | Synchronization filter output<br>lower 8 bit of the 15 bit signed synchronization filter output |
| clif_status | transceive_state | | 7:5 | |
| | rx_cl_error | | 4 | |
| | tx_envelope | | 3 | |
| | rx_enevelope | | 2 | |
| | svalid | | 1 | |
| | sdata | | 0 | |
| clif_transceive | rx_start_receive | | 7 | |
| | rx_over_ok | | 6 | |
| | rx_over_term | | 5 | |
| | rx_resume | | 4 | |
| | sgp_msg_busy | | 3 | |
| | fig_reset_sigpro | | 2 | |
| | fig_reset_rxdec | | 1 | |
| | cfg_sw_reset_sigpro | | 0 | |

**Table 15. TRIGGER SIGNALS**

| TRIGGER | REGISTER | SIGNAL NAME | BITS | Description |
|---|---|---|---|---|
| TX Active | obs_clif_txenc1 | tx_active_o | 1 | high level indicates transmission of data Remark: Falling edge can be used to trigger on end of transmission. |
| RX Enable | obs_clif_sigpro_rm15 | rx_enable_o | 1 | high level indicates that the reception is ongoing Remark: can be used to trigger on the start /end of reception |
| RX collision detected | obs_clif_sigpro_rm14 | rm_scoll_o | 1 | high-level pulse indicates that the collision is detected during reception |

## 9.17 Polling loop

The polling loop and related configuration are described in the user manual.

## 9.18 System settings and configuration

The configuration and behavior of the device is controlled at a central place.

EEPROM settings are a collection of all available configuration parameters that are needed for different operation modes. EEPROM settings serve as the source for the register settings.

The following two chapters list down the registers that are available to the user, as well as all available EEPROM configuration options.

**This list of registers and EEPROM configuration is copied from PN5190 - it will be updated for the final product. Not all registers /EEPROM might be available on the PN7220.**

### 9.18.1 CLIF register description

The default setting of a bit within a register is indicated by the "*" or "Reset value". Value indicates the allowed range for the bits of a symbol.

Note that the firmware changes the content of some registers between an RF Exchange followed by an RF Reset command.

The detailed description of the registers is available in the User API documentation.

#### 9.18.1.1 List of CLIF registers

List of CLIF registers and its addresses

**Table 16. List of CLIF registers**

| Register Name | Register address (Hex) | Register address (Decimal) |
|---|---|---|
| SYSTEM_CONFIG (0x00) | 0x00 | 0 |
| CLIF_RX_STATUS (0x05) | 0x05 | 5 |
| CLIF_RX_STATUS_ERROR (0x06) | 0x06 | 6 |
| CLIF_STATUS (0x07) | 0x07 | 7 |
| CLIF_CRC_TX_CONFIG (0x12) | 0x12 | 18 |
| CLIF_SS_TX1_RMCFG (0x16) | 0x16 | 22 |
| CLIF_SIGPRO_RM_TECH (0x22) | 0x22 | 34 |
| CLIF_SIGPRO_IIR_CONFIG0 (0x2A) | 0x2A | 42 |
| CLIF_DGRM_BBA (0x2D) | 0x2D | 45 |
| CLIF_DGRM_RSSI (0x30) | 0x30 | 48 |
| CLIF_CRC_RX_CONFIG (0x31) | 0x31 | 49 |
| CLIF_RX_WAIT (0x32) | 0x32 | 50 |
| CLIF_SS_TX1_CMCFG (0x3B) | 0x3B | 59 |
| CLIF_TIMER1_CONFIG (0x3F) | 0x3F | 63 |
| CLIF_TIMER1_RELOAD (0x40) | 0x40 | 64 |
| TXLDO_VDDPA_CONFIG (0x54) | 0x54 | 84 |
| TXLDO_VOUT_CURR (0x56) | 0x56 | 84 |
| CLIF_RXM_FREQ (0x59) | 0x59 | 89 |

**Table 16.  List of CLIF registers**...*continued*

| Register Name | Register address (Hex) | Register address (Decimal) |
|---|---|---|
| INTERPOLATED_RSSI_REG (0x5C) | 0x5C | 92 |
| TX_NOV_CALIBRATE_AND_STORE_VAL_REG (0x5D) | 0x5D | 93 |
| CLIF_SS_TX1_RTRANS0 (0x80) | 0x80 | 128 |
| CLIF_SS_TX1_RTRANS1 (0x81) | 0x81 | 129 |
| CLIF_SS_TX1_RTRANS2 (0x82) | 0x82 | 130 |
| CLIF_SS_TX1_RTRANS3 (0x83) | 0x83 | 131 |
| CLIF_SS_TX2_RTRANS0 (0x84) | 0x84 | 132 |
| CLIF_SS_TX2_RTRANS1 (0x85) | 0x85 | 133 |
| CLIF_SS_TX2_RTRANS2 (0x86) | 0x86 | 134 |
| CLIF_SS_TX2_RTRANS3 (0x87) | 0x87 | 135 |
| CLIF_SS_TX1_FTRANS0 (0x88) | 0x88 | 136 |
| CLIF_SS_TX1_FTRANS1 (0x89) | 0x89 | 137 |
| CLIF_SS_TX1_FTRANS2 (0x8A) | 0x8A | 138 |
| CLIF_SS_TX1_FTRANS3 (0x8B) | 0x8B | 139 |
| CLIF_SS_TX2_FTRANS0 (0x8C) | 0x8C | 140 |
| CLIF_SS_TX2_FTRANS1 (0x8D) | 0x8D | 141 |
| CLIF_SS_TX2_FTRANS2 (0x8E) | 0x8E | 142 |
| CLIF_SS_TX2_FTRANS3 (0x8F) | 0x8F | 143 |

### 9.18.1.2  SYSTEM_CONFIG (0x00)

This register provides the system configuration on Autocoll, MFC Crypto bit generation, ISO15693 baud-rate, TXNOV calibration.

**Table 17.  SYSTEM_CONFIG (0x00) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:9] | RFU | rw | | Reserved |
| [8:8] | TX_NOV_CALIBRATE | rw | | One time calibration when the host writes a 1 into this register, a one time calibration will be performed. **Note:**The calibration is resulting a short RF-on. All the power configurations shall the configured before setting this bit. |
| [7:7] | RFU | rw | | Reserved |
| [6:5] | 15693_CHANGE_DATARATE | rw | | 15693_changedatarate. By default, the basic data rate of 26 kB/s will be loaded, switching to a different higher data rate requires this config register to be updated. All relevant related registers will be updated automatically. |
| | | | 0 | RFU |
| | | | 1 | Change Data Rate to 53 kB/s |
| | | | 2 | Change Data Rate to 106 kB/s |
| | | | 3 | Change Data Rate to 212 kB/s |
| [4:2] | RFU | rw | | Reserved |
| [1:1] | MFC_CRYPTO_ON | rw | | MIFARE crypto bit generation for MIFARE Classic en/de-cryption |
| | | | 0 | MIFARE - crypto bit is not generated for MIFARE Classic en-/de-cryption |
| | | | 1 | MIFARE - crypto bit is generated for MIFARE Classic en-/de-cryption |
| [0:0] | AUTOCOLL_STATE_A | rw | | Autocoll state for Type A |
| | | | 0 | TypeA Card mode: Autocoll entry with IDLE state of the card |
| | | | 1 | TypeA Card mode: Autocoll entry with HALT state of the card |

### 9.18.1.3 CLIF_RX_STATUS (0x05)

This register provides the CLIF RX status.

**Table 18. CLIF_RX_STATUS (0x05) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:27] | RESERVED | r- | 0x0 | Reserved |
| [26:20] | RX_COLL_POS | r- | 0x0 | Status indicating the bit position of the first collision detected in the data bit. The value is valid only when RX_COLLISION_DETECTED==1. The value of the RX_BIT_ALIGN is also taken intoaccount (RX_COLL_POS = physical bit position in the flow + RX_BIT_ALIGN value).Indicates the collision position in the first 8 bytes only. Can be used during the Type A/ICODE/EPC anticollision procedure.0x00 - 1st bit 0x01 - 2nd bit...0x7F - 128th bit.The status register is not updated by the collision detected on stop or parity bit. |
| [19:17] | RX_NUM_LAST_BITS | r- | 0x0 | Indicating the number of valid bits in the last byte received.This is generally used during ISO/IEC14443 type A anti-collision |
| | | | 0 | 0: all bits are valid |
| | | | 1 | 1: 1 bit is valid |
| | | | 2 | 2: 2 bits are valid |
| | | | 3 | 3: 3 bits are valid |
| | | | 4 | 4: 4 bits are valid |
| | | | 5 | 5: 5 bits are valid |
| | | | 6 | 6: 6 bits are valid |
| | | | 7 | 7: 7 bits are valid |
| [16:13] | RX_NUM_FRAMES_RECEIVED | r- | 0x0 | Indicates the number of frames received. The value is updated after every normal frame reception in RX_MULTIPLE mode.The value is valid only if the bit RX_MULTIPLE_ENABLE==1. |
| [12:0] | RX_NUM_BYTES_RECEIVED | r- | 0x0 | Number of bytes received on the RF interface. This field is not relevant when RX_MULTIPLE_ENABLE=='1'. |

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### 9.18.1.4 CLIF_RX_STATUS_ERROR (0x06)

This register provides the CLIF_RX_ERROR status.

**Table 19. CLIF_RX_STATUS_ERROR (0x06) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:30] | RESERVED | r- | 0x0 | Reserved |
| [29:29] | EMD_DETECTED_IN_RXDEC | r- | 0x0 | The high level indicates that the EMD was detected (in the SigPro or in the RxDecoder or in both) during the reception. |
| [28:28] | EMD_DETECTED_IN_SIGPRO | r- | 0x0 | The high level indicates that the EMD was detected on the Physical layer (in the SigPro) during the reception. |
| [27:27] | EXT_RFOFF_DETECTED | r- | 0x0 | The high level indicates that the received frame length violated the configured minimum limit. |
| [26:26] | RX_FRAME_MAXLEN_VIOL | r- | 0x0 | The high level indicates that the received frame length is less or equal to the expected CRC field length |
| [25:25] | RX_FRAME_MINLEN_VIOL | r- | 0x0 | The high level indicates that the last received character in the frame has less than 8 bits. |
| [24:24] | RX_FRAME_LE_CRC | r- | 0x0 | The high level indicates that the last received character in the frame has 8 data bits but the expected parity bit is absent. |
| [23:23] | RX_NOT_FULL_BYTE | r- | 0x0 | The high level indicates that the last received character in the frame has 8 data bits but the expected stop bit is absent. |
| [22:22] | RX_MISSING_PARBIT_ DETECTED | r- | 0x0 | The high level indicates that the collision was detected on the parity bit position. |
| [21:21] | RX_MISSING_STOPBIT_ DETECTED | r- | 0x0 | The high level indicates that the collision was detected on the stop bit position. |
| [18:18] | RX_COLLISION_DETECTED | r- | 0x0 | The high level indicates that the collision was detected during the frame reception. |
| [17:17] | RX_STOP_ON_RXOVER | r- | 0x0 | The high level indicates that the frame reception was stopped by SGP_MSG_RXOVER_* message reception. |
| [16:16] | RX_STOP_ON_RFOFF | r- | 0x0 | The high level indicates that the frame reception was interrupted by external RF-field vanishing event. |
| [15:15] | RX_STOP_ON_ERR | r- | 0x0 | The high level indicates that the frame reception was stopped by detected communication error event. |
| [14:14] | RX_STOP_ON_LEN | r- | 0x0 | The high level indicates that the frame reception was normally stopped by byte counter expiration event. Relates to the protocols where the LEN field is used in the frame format (Felica RM/CM, FWEC RM/CM). |

**Table 19.  CLIF_RX_STATUS_ERROR (0x06) register bit description**...*continued*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [13:13] | RX_STOP_ON_INVPAR | r- | 0x0 | The high level indicates that the frame reception was normally stopped by the inverted parity detection event. Relates to the TypeA RM 212 kbit/s - 848 kbit/s modes. 12 RX_STOP_ON_PATTERN R 0h The high level indicates that the frame reception was normally stopped by EOF pattern detection event. Relates to the TypeB RM/CM, B prime RM/CM modes. |
| [12:12] | RX_STOP_ON_PATTERN | r- | 0x0 | The high level indicates that the frame reception was normally stopped by EOF pattern detection event. Relates to the TypeB RM/CM, B prime RM/CM modes. |
| [11:11] | RX_STOP_ON_ANTICOLL | r- | 0x0 | The high level indicates that the frame reception was normally stopped by collision detected on data bit position. Relates to the bit-oriented frame reception in TypeA RM 106 kbit/s mode during the anticollision procedure. |
| [10:10] | RX_CRC_ERROR | r- | 0x0 | The high level indicates that the CRC error is detected in the received frame. |
| [9:9] | RX_LEN_ERROR | r- | 0x0 | The high level is set if the received frame is shorter than the length stated in the received frame LEN field OR if the LEN parameter in the received frame violates the configured [RX_FRAME_MINLEN:RX_FRAME_MAX LEN] limits. Can assert only in the mode swhere the LEN field is used in the frame format (Felica RM/CM, FWEC RM/CM). |
| [8:8] | RX_SIGPRO_ERROR | r- | 0x0 | The high level indicates that the communication error/errors were detected during the frame reception on physical layer(in the SigPro). |
| [7:7] | RX_PARITY_ERROR | r- | 0x0 | The high level indicates that the parity error was detected during the frame reception. |
| [6:6] | RX_STOPBIT_ERROR | r- | 0x0 | The high level indicates that the stop bit error (0 level instead of 1 on the stop bit position) was detected during the frame reception. |
| [5:5] | RX_WRITE_ERROR | r- | 0x0 | The high level indicates that the error acknowledge status was received on theCLIF-system interface during the received frame transmission to the System RAM. |
| [4:4] | RX_BUFFER_OVFL_ERROR | r- | 0x0 | The high level indicates that the data payload length in the received frame exceeds the 28 bytes limit. Relates to the PollReq procedure in the Felica RM mode only. |
| [3:3] | RX_LATENCY_ERROR | r- | 0x0 | The high level indicates that the write request flow was corrupted due to traffic congestion on the system interface during the received frame transmission to the System RAM. |
| [2:2] | RX_DATA_INTEGRITY_ERROR | r- | 0x0 | The high level indicates that the data integrity corruption (parity/CRC/etc error)was detected in the received frame. |

**Table 19. CLIF_RX_STATUS_ERROR (0x06) register bit description**...*continued*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [1:1] | RX_PROTOCOL_ERROR | r- | 0x0 | The high level indicates that the protocol requirements violation (stop bit error,missing parity bit, not full byte received, etc) was detected in the received frame. |
| [0:0] | RX_CL_ERROR | r- | 0x0 | The high level indicates that some protocol/data integrity erorr/errors were detected during the frame reception |

### 9.18.1.5 CLIF_STATUS (0x07)

This register provides the CLIF status.

**Table 20. CLIF_STATUS (0x07) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:30] | RESERVED | r- | 0x0 | Reserved |
| [29:29] | CRC_OK | r- | 0x1 | This bit indicates the status of the actual CRC calculation. If 1 the CRC is correct. meaning the CRC register has the value 0 or the residue value if inverted CRC is used. Note: This flag should only by evaluated at the end of a communication |
| [28:28] | RX_SC_DETECTED | r- | 0x0 | Status signal indicating that a sub-carrier is detected. |
| [27:27] | RX_SOF_DETECTED | r- | 0x0 | Status signal indicating that a SOF has been detected. |
| [26:26] | TX_RF_STATUS | r- | 0x0 | If set to 1 this bit indicates that the drivers are turned on. meaning an RF-Field is created by the device itself. |
| [25:25] | RF_DET_STATUS | r- | 0x0 | If set to 1 this bit indicates that an external RF-Field is detected by the rf level detectors (after digital filtering) |
| [24:24] | ADC_Q_CLIPPING | r- | 0x0 | Indicates that the Q-Channel ADC has clipped (value 0 or 63), This bit is reset with Rx-reset (enabling of receiver). |
| [23:23] | ADC_I_CLIPPING | r- | 0x0 | Indicates that the I-Channel ADC has clipped (value 0 or 63), This bit is reset with Rx-reset (enabling of receiver). |
| [22:22] | DPLL_SATURATED_LIMIT | r- | 0x0 | Status signal indicating that the DPLL has reached its locking limits (integrator is at 0 or maximum) |
| [21:21] | DPLL_SATURATED_LOCK_RANGE | r- | 0x0 | Status signal indicating that the DPLL has reached its locking limits. (Saturation range configured via DPLL_SATURATION_VAL) |
| [20:20] | DPLL_FREQ_LOCK_SUPER_FINE | r- | 0x0 | Status signal indicating that the DPLL has reached frequency-lock with ~1.4Hz accuracy |
| [19:19] | DPLL_FREQ_LOCK_FINE | r- | 0x0 | Status signal indicating that the DPLL has reached frequency-lock with ~5Hz accuracy |
| [18:18] | DPLL_FREQ_LOCK_COARSE | r- | 0x0 | Status signal indicating that the DPLL has reached frequency-lock with ~50Hz accuracy |

**Table 20. CLIF_STATUS (0x07) register bit description**...*continued*

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [17:17] | DPLL_PHASE_LOCK | r- | 0x0 | Status signal indicating that the DPLL has reached phase-lock (typically happens before DPLL_ FREQUENCY_LOCK_COARSE is set). |
| [16:16] | DPLL_ENABLE | r- | 0x0 | This bit indicates that the DPLL Controler has enabled the DPLL (RF on RF frequency ok PLL locked) |
| [15:15] | RESERVED | r- | 0x0 | Reserved |
| [14:14] | BMA_TRANSFER_ONGOING | r- | 0x0 | Status signal from Buffer Manager to indicate that a transfer is actually ongoing. |
| [13:13] | TX_READ_ERROR | r- | 0x0 | This error flag is set to 1 if for an ongoing transmission data is not copied from RAM in time (BMA encountered read error) and therefor the transmission is aborted.<br>**Note:** This case should not happen in normal operation |
| [12:12] | TX_LATENCY_ERROR | r- | 0x0 | This error flag is set to 1. if for an ongoing transmission data is not available in time (BMA latency to big) and therefor the transmission is aborted.<br>**Note:** This case should not happen in normal operation |
| [11:11] | TX_NO_DATA_ERROR | r- | 0x0 | This error flag is set to 1. in case a transmission is started but no data is available (register NumBytesTo Send == 0). |
| [10:8] | RF_ACTIVE_ERROR_CAUSE | r- | 0x00 | This status flag indicates the cause of an NFC-Active error.<br>**Note:** This bits are only valid when the RF_ACTIVE_ ERROR_IRQ is raised and will be cleared as soon as the bit TX_RF_ENABLE is set to 1. |
| | | | 0x00 | reset value |
| | | | 0x01 | External field was detected on within TIDT timing |
| | | | 0x02 | External field was detected on within TADT timing |
| | | | 0x03 | No external field was detected within TADT timings |
| | | | 0x04 | Peer did switch off RFField without but no Rx event was raised (no data received) |
| | | | 0x05-0x 07 | Reserved. |
| [7:6] | RESERVED | r- | 0x0 | Reserved |
| [5:5] | RX_ENABLE | r- | 0x0 | This bit indicates if the RxDecoder is enalbed. If 1 the RxDecoder was enabled by the Transceive Unit and is now ready for data reception |
| [4:4] | TX_ACTIVE | r- | 0x0 | This bit indicates activity of the TxEncoder. If 1 a transmission is ongoing otherwise the TxEncoder is in idle state. |

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**Table 20. CLIF_STATUS (0x07) register bit description**...*continued*

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [3:3] | RX_ACTIVE | r- | 0x0 | This bit indicates activity of the RxDecoder. If 1 a data reception is ongoing. otherwise the RxDecoder is in idle state. |
| [2:0] | TRANSCEIVE_STATE | r- | 0x0 | This registers hold the command bits |
| | | | 0 | 0: IDLE state |
| | | | 1 | 1: WaitTransmit state |
| | | | 2 | 2: Transmitting state |
| | | | 3 | 3: WaitReceive state |
| | | | 4 | 4: WaitForData state |
| | | | 5 | 5: Receiving state |
| | | | 6 | 6: LoopBack state |
| | | | 7 | 7: reserved |

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### 9.18.1.6 CLIF_CRC_TX_CONFIG (0x12)

This register provides the settings for CLIF_CRC_TX_CONFIG

**Table 21. CLIF_CRC_TX_CONFIG (0x12) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:16] | TX_CRC_PRESET_VALUE | rw | 0x0 | Arbitrary preset value for the Tx-Encoder CRC calculation. |
| [15:7] | RESERVED | r- | 0x0 | Reserved |
| [6:6] | TX_CRC_BYTE2_ENABLE | rw | 0x0 | If set. the CRC is calculated from the 2nd byte onwards (intended for HID). Note that this option is used in the Tx-Encoder. |
| [5:3] | TX_CRC_PRESET_SEL | rw | 0x000 | Preset value of the CRC register for the Tx-Encoder. For a CRC calculation using 5 bits, only the LSByte is used. |
| | | | 000b | 000b -> 0000h reset value |
| | | | 001b | 001b -> 6363h |
| | | | 010b | 010b -> A671h |
| | | | 011b | 011b -> FFFFh |
| | | | 100b | 100b -> 0012h |
| | | | 101b | 101b -> E012h |
| | | | 110b | 110b -> RFU |
| | | | 111b | 111b -> Use arbitrary preset value TX_CRC_PRESET_VALUE |
| [2:2] | TX_CRC_TYPE | rw | 0x0 | Controls the type of CRC calulation for the Tx-Encoder 0* 16-bit CRC calculation. reset value 1 5-bit CRC calculation |
| [1:1] | TX_CRC_INV | rw | 0x0 | Controls the sending of an inverted CRC value by the Tx-Encoder 0* Not inverted CRC checksum. reset value 1 Inverted CRC checksum |
| [0:0] | TX_CRC_ENABLE | rw | 0x0 | If set to one. the Tx-Encoder will compute and transmit a CRC. |

### 9.18.1.7 CLIF_SS_TX1_RMCFG (0x16)

This register provides the settings for CLIF_SS_TX1_RMCFG

**Table 22. CLIF_SS_TX1_RMCFG (0x16) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:25] | RESERVED | r- | 0x00 | Reserved |
| [24:22] | TX1_CLK_MODE_TRANS_RM | rw | 0x00 | TX1 clock mode in RM during transition |
| [21:19] | TX1_CLK_MODE_MOD_RM | rw | 0x00 | TX1 clock mode of modulated wave in RM |
| [18:16] | TX1_CLK_MODE_CW_RM | rw | 0x00 | TX1 clock mode of unmodulated wave in RM |
| [15:8] | TX1_AMP_MOD_RM | rw | 0x00 | TX1 amplitude of modulated wave in RM ( 0x00 = 0 %modulaton, 0xFF: 100 % modulation) |

**Table 22. CLIF_SS_TX1_RMCFG (0x16) register bit description**...*continued*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [7:0] | TX1_AMP_CW_RM | rw | 0xFF | TX1 amplitude of unmodulated wave in RM ( 0x00 = 0 % signal, 0xFF: 100 % signal) |

### 9.18.1.8 CLIF_SIGPRO_RM_TECH (0x22)

This register provides the settings for CLIF_SIGPRO_RM_TECH

**Table 23. CLIF_SIGPRO_RM_TECH (0x22) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:30] | RM_NCO_PERIOD_SEL | rw | 0x0 | Defines the reset value for the NCO counter |
| [29:27] | RM_WAIT_RES_PERIOD_SEL | rw | 0x0 | Defines the reset value for the Delay counter |
| [26:26] | RM_EGT_WINDOW_TH_SEL | rw | 0x0 | Defines the EGT window threshold for Type B |
| [25:25] | RM_DC_REMOVAL_ENABLE | rw | 0x0 | Reserved |
| [24:23] | RM_DOWNSAMPLE_RATE_SEL | rw | 0x0 | Defines the down sample rate for the reader demod. |
| [22:20] | RM_SOF_NUM_CYCLES_SEL | rw | 0x0 | Defines the number of samples in I-Code SOF. |
| [19:17] | RM_MF_SEL | rw | 0x0 | Defines the selection for the Matched-Filters |
| [16:15] | RM_MF_GAIN | rw | 0x0 | Defines the gain of the Matched-Filters |
| [14:13] | RM_MRC_WEIGHT_SEL | rw | 0x0 | Defines the channel combiner weight on the lower channel |
| [12:12] | RM_AVG_FILT_GAIN | rw | 0x0 | Defines the averaging filter gain |
| [11:10] | RM_AVG_FILT_SEL | rw | 0x0 | Defines the averaging filter selection |
| [9:8] | RM_SYNC_FILT_IN_SEL | rw | 0x0 | Defines the input selection for the sync filter. |
| [7:6] | RM_SYNC_FILT_SEL | rw | 0x0 | Defines the synchronization filter selection |
| [5:3] | RM_WATCH_DOG_PERIOD_SEL | rw | 0x0 | Defines the reset value for the watch-dog counter |
| [2:2] | RM_EST_RESTART_ENABLE | rw | 0x0 | Reserved |
| [1:0] | RM_OOK_STAT_LEN | rw | 0x3 | Defines the number of samples used to check for invalid at the beginning of a reception in A106 and Icode. Value 0x0 = 2 samples, value 0x1 = 4 samples, value 0x2 = 8 samples, value 0x3 = 16 samples |

### 9.18.1.9 CLIF_SIGPRO_IIR_CONFIG0 (0x2A)

This register provides the settings for CLIF_SIGPRO_IIR_CONFIG0

**Table 24. CLIF_SIGPRO_IIR_CONFIG0 (0x2A) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:20] | RESERVED | r- | 0x0 | Reserved |
| [19:19] | IIR_SIGN_A2 | rw | 0x0 | IIR A1 sign |
| [18:12] | IIR_COEF_A2 | rw | 0x0 | IIR A1 coef (unsigned, MSB unused) Value is coded value/64 |
| [11:11] | IIR_SIGN_A1 | rw | 0x0 | IIR A0 sign |

**Table 24. CLIF_SIGPRO_IIR_CONFIG0 (0x2A) register bit description**...*continued*

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [10:4] | IIR_COEF_A1 | rw | 0x0 | IIR A0 coef (unsigned, MSB unused) Value is coded value/64 |
| [3:1] | IIR_GAIN | rw | 0x0 | IIR filter gain |
| [0:0] | IIR_ENABLE | rw | 0x0 | Enable the IIR filter |

### 9.18.1.10 CLIF_DGRM_BBA (0x2D)

This register provides the settings for CLIF_DGRM_BBA

**Table 25. CLIF_DGRM_BBA (0x2D) register bit description**

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [31:30] | DGRM_FALSE_ALARM_WAIT | rw | 0x0 | False alarm wait in multiples of 256 cycles |
| [29:29] | DGRM_BBA_FAST_MODE_ENABLE | rw | 0x0 | Enables the BBA fast mode |
| [28:26] | DGRM_GAIN_SHIFT_DELAY | rw | 0x0 | Defines the delay for digital gain compensation to match the latency from BBA gain |
| [25:24] | DGRM_BBA_TH_SEL | rw | 0x0 | Defines the threshold for the max absolute ADC value |
| [23:22] | DGRM_MAX_SWING_TH_SEL | rw | 0x0 | Defines the maximum swing threshold for decreasing BBA gain |
| [21:20] | DGRM_MIN_SWING_TH_SEL | rw | 0x0 | Defines the minimum swing threshold for increasing BBA gain |
| [19:18] | DGRM_WATER_LEVEL_TH_SEL | rw | 0x0 | Defines the water level threshold |
| [17:17] | RESERVED | rw | 0x0 | RESERVED |
| [16:14] | DGRM_BBA_MIN_VAL | rw | 0x0 | Defines the minimum value of BBA gain. |
| [13:11] | DGRM_BBA_MAX_VAL | rw | 0x0 | Defines the maximum value of BBA gain. |
| [10:8] | DGRM_BBA_INIT_VAL | rw | 0x0 | Defines initial value of BBA gain. If BBA fast and slow modes are disabled, this value defines the forced value. |
| [7:7] | DGRM_GUESS_BBA_GAIN_ENABLE | rw | 0x0 | Enables the initial guess of BBA gain based on noise power estimate |
| [5:5] | DGRM_NOISE_POWER_EST_ENABLE | rw | 0x0 | Enables the noise power estimator in free running mode |
| [4:2] | DGRM_NOISE_POWER_SHIFT_VAL | rw | 0x0 | Defines the number of bits to shift right in order to scale the noise power. This is in addition to the scaling due to accumulation |
| [1:0] | RESERVED | r- | 0x0 | Reserved |

### 9.18.1.11 CLIF_DGRM_DCO (0x2E)

This register provides the settings for CLIF_DGRM_DCO

**Table 26. CLIF_DGRM_DCO (0x2E) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:30] | DGRM_DCO_TRACK_AVG_LEN_SEL | rw | 0x0 | Defines the number of ADC samples to average during TRACK mode |
| [29:28] | DGRM_DCO_INIT_AVG_LEN_SEL | rw | 0x0 | Defines the number of ADC samples to average during INIT mode |
| [27:26] | DGRM_DCO_WAIT_PERIOD_SEL | rw | 0x0 | Defines the wait period after DCO DAC update and before estimating DCO |
| [25:24] | DGRM_DCO_TH_SEL | rw | 0x0 | Defines the DCO DAC threshold |
| [23:22] | DGRM_DCO_MAX_ITER_SEL | rw | 0x0 | Defines the maximum number of iterations in DCO DAC fast mode |
| [21:21] | DGRM_DCO_DAC_SLOW_MODE_ENABLE | rw | 0x0 | Enables DCO DAC slow mode before card response. |
| [20:20] | DGRM_DCO_DAC_FAST_MODE_ENABLE | rw | 0x0 | Enables DCO DAC fast mode |
| [19:10] | DGRM_DCO_DAC_Q_INIT_VAL | rw | 0x0 | Defines the initial value of the composite DAC for the Q channel. This is also the forced value if DCO DAC fast and slow modes are disabled. The 5 MSBs control the coarse DAC and the 5 MSBs control the fine DAC. |
| [9:0] | DGRM_DCO_DAC_I_INIT_VAL | rw | 0x0 | Defines the initial value of the composite DAC for the I channel. This is also the forced value if DCO DAC fast and slow modes are disabled. The 5 MSBs control the coarse DAC and the 5 MSBs control the fine DAC. |

### 9.18.1.12  CLIF_DGRM_RSSI (0x30)

This register provides the settings for CLIF_DGRM_RSSI

**Table 27.  CLIF_DGRM_RSSI (0x30) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:31] | DGRM_DEMOD_EN_FORCE | rw | 0x0 | When set, forces demod_enable high |
| [30:30] | DGRM_NUM_GAIN_UPDT_FORCE | rw | 0x0 | When set, forces dgrm_num_gain_updt to be zero |
| [29:29] | DGRM_SIGNAL_DETECT_TH_OVR | rw | 0x0 | Enables the override of signal detect threshold. Override value is set based on DGRM_SIGNAL_DETECT_TH_OVR_VAL. |
| [28:27] | DGRM_RSSI_TRACK_AVG_LEN_SEL | rw | 0x0 | Defines the number of RSSI samples to average during track mode |
| [26:25] | DGRM_RSSI_INIT_AVG_LEN_SEL | rw | 0x0 | Defines the number of RSSI samples to average during INIT mode |
| [24:23] | DGRM_RSSI_WAIT_PERIOD | rw | 0x0 | Defines the number of RSSI samples to discard before averaging |
| [22:17] | DGRM_RSSI_HYST | rw | 0x0 | Hysteresis value for RSSI target |
| [16:7] | DGRM_RSSI_TARGET | rw | 0x0 | RSSI target value |
| [6:0] | DGRM_SIGNAL_DETECT_TH_OVR_VAL | rw | 0x0 | Defines the override value for signal detect threshold. when DGRM_SIGNAL_DETECT_TH_OVR is set. These bits are modified dynamically by the ARC algorithm based on the DPC voltage.Only if the ARC is disabled, the value written during LOAD_RF_CONFIGURATION(0x0D) is retained throughout the RF Field session |

### 9.18.1.13 CLIF_CRC_RX_CONFIG (0x31)

This register provides the settings for CLIF_CRC_RX_CONFIG

**Table 28. CLIF_CRC_RX_CONFIG (0x31) register bit description**

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [31:16] | RX_CRC_PRESET_VALUE | rw | 0x0 | Arbitrary preset value for the Rx-Decoder CRC calculation. |
| [15:8] | RESERVED | r- | 0x0 | Reserved |
| [7:7] | RX_FORCE_CRC_WRITE | rw | 0x0 | If set. the Rx-Decoder will send to the RAM the CRC bits as well. |
| [6:6] | RX_CRC_ALLOW_BITS | rw | 0x0 | If activated the frame with length less than or equal CRC_length will be always sent to the System RAM as is, without CRC bits removal. |
| [5:3] | RX_CRC_PRESET_SEL | rw | 0x000 | Preset value of the CRC register for the Rx-Decoder. For a CRC calculation using 5bits only the LSByte is used. |
| | | | 000b | 000b -> 0000h reset value Note that this configuration is set by the Mode detector for FeliCa. |
| | | | 001b | 001b -> 6363h Note that this configuration is set by the Mode detector for ISO14443 type A. |
| | | | 010b | 010b -> A671h |
| | | | 011b | 011b -> FFFFh Note that this configuration is set by the Mode detector for ISO14443 type B |
| | | | 100b | 100b -> 0012h |
| | | | 101b | 101b -> E012h |
| | | | 110b | 110b -> RFU |
| | | | 111b | 111b -> Use arbitrary preset value RX_CRC_PRESET_VALUE |
| [2:2] | RX_CRC_TYPE | rw | 0x0 | Controls the type of CRC calculation for the Rx Decoder 0* 16-bit CRC calc |
| [1:1] | RX_CRC_INV | rw | 0x0 | Controls the comparison of the CRC checksum for the Rx-Decoder 0* Not inverted CRC value: 0000h reset value Note that this nit is cleared by the Mode detector for ISO14443 type A and FeliCa. 1 Inverted CRC value: F0B8h Note that this bit is set by the Mode detector for ISO14443 type B. |
| [0:0] | RX_CRC_ENABLE | rw | 0x0 | If set. the Rx-Decoder will check the CRC for correctness.Note that this bit is set by the Mode Detector when ISO14443 type B. or FeliCa (212 kBd or 424 kBd) is detected. |

### 9.18.1.14 CLIF_RX_WAIT (0x32)

This register provides the settings for CLIF_RX_WAIT

**Table 29. CLIF_RX_WAIT (0x32) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:28] | RESERVED | r- | 0x0 | Reserved |
| [27:8] | RX_WAIT_VALUE | rw | 0x0 | Defines the rx_wait timer reload value. Note: If set to 00000h the rx_wait guard time is disabled |
| [7:0] | RX_WAIT_PRESCALER | rw | 0x0 | Defines the prescaler reload value for the rx_wait timer. |

### 9.18.1.15 CLIF_SS_TX1_CMCFG (0x3B)

This register provides the settings for CLIF_SS_TX1_CMCFG

**Table 30. CLIF_SS_TX1_CMCFG (0x3B) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:22] | RESERVED | r- | 0x00 | Reserved |
| [21:19] | TX1_CLK_MODE_MOD_CM | rw | 0x00 | TX1 clock mode of modulated wave in CM |
| [18:16] | TX1_CLK_MODE_CW_CM | rw | 0x00 | TX1 clock mode of unmodulated wave in CM |
| [15:8] | TX1_AMP_MOD_CM | rw | 0x00 | TX1 amplitude of modulated wave in CM |
| [7:0] | TX1_AMP_CW_CM | rw | 0xFF | TX1 amplitude of unmodulated wave in CM |

### 9.18.1.16 CLIF_TIMER1_CONFIG (0x3F)

This register provides the settings for CLIF_TIMER1_CONFIG

**Table 31. CLIF_TIMER1_CONFIG (0x3F) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:31] | RESERVED | r- | 0x0 | Reserved |
| [30:30] | T1_STOP_ON_RX_STARTED | rw | 0x0 | T1_STOP_EVENT: If set. the timer T1 is stopped when a data reception begins (1st bit is received). |
| [29:29] | T1_STOP_ON_TX_STARTED | rw | 0x0 | T1_STOP_EVENT: If set. the timer T1 is stopped when a data transmission begins. |
| [28:28] | T1_STOP_ON_RF_ON_EXT | rw | 0x0 | T1_STOP_EVENT: If set. the timer T1 is stopped when the external RF field is detected. |
| [27:27] | T1_STOP_ON_RF_OFF_EXT | rw | 0x0 | T1_STOP_EVENT: If set. the timer T1 is stopped when the external RF field vanishes. |
| [26:26] | T1_STOP_ON_RF_ON_INT | rw | 0x0 | T1_STOP_EVENT: If set. the timer T1 is stopped when the internal RF field is turned on. |
| [25:25] | T1_STOP_ON_RF_OFF_INT | rw | 0x0 | T1_STOP_EVENT: If set. the timer T1 is stopped when the internal RF field is turned off. |
| [24:24] | T1_STOP_ON_RX_ENDED | rw | 0x0 | T1_STOP_EVENT: If set the timer T1 is stopped when an activity on RX is detected. |
| [23:18] | RESERVED | r- | 0x0 | Reserved |

**Table 31. CLIF_TIMER1_CONFIG (0x3F) register bit description**...*continued*

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [17:17] | T1_START_ON_RX_STARTED | rw | 0x0 | T1_START_EVENT: If set. the timer T1 is started when a data reception begins (1st bit is received). |
| [16:16] | T1_START_ON_RX_ENDED | rw | 0x0 | T1_START_EVENT: If set. the timer T1 is started when a data reception ends. |
| [15:15] | T1_START_ON_TX_STARTED | rw | 0x0 | T1_START_EVENT: If set. the timer T1 is started when a data transmission begins. |
| [14:14] | T1_START_ON_TX_ENDED | rw | 0x0 | T1_START_EVENT: If set. the timer T1 is started when a data transmission ends. |
| [13:13] | T1_START_ON_RF_ON_EXT | rw | 0x0 | T1_START_EVENT: If set. the timer T1 is startedwhen the external RF field is detected. |
| [12:12] | T1_START_ON_RF_OFF_EXT | rw | 0x0 | T1_START_EVENT: If set. the timer T1 is started when the external RF field is not detected any more. |
| [11:11] | T1_START_ON_RF_ON_INT | rw | 0x0 | T1_START_EVENT: If set. the timer T1 is started when an internal RF field is turned on. |
| [10:10] | T1_START_ON_RF_OFF_INT | rw | 0x0 | T1_START_EVENT: If set. the timer T1 is started when an internal RF field is turned off. |
| [8:8] | T1_START_NOW | rw | 0x0 | T1_START_EVENT: If set. the timer T1 is started immediatly. |
| [7:7] | RESERVED | r- | 0x0 | Reserved |
| [6:6] | T1_ONE_SHOT_MODE | rw | 0x00 | When set to 1 the counter value does not reload again until the counter value has reached zero |
| [5:3] | T1_PRESCALE_SEL | rw | 0x00 | Controls input frequency/period of the timer T0 when the prescaler is activated in T1_MODE_SEL. |
| | | | 000b | 000b -> 6.78 MHz counter |
| | | | 001b | 001b -> 3.39 MHz counter |
| | | | 010b | 010b -> 1.70 MHz counter |
| | | | 011b | 011b -> 848 kHz counter |
| | | | 100b | 100b -> 424 kHz counter |
| | | | 101b | 101b -> 212 kHz counter |
| | | | 110b | 110b -> 106 kHz counter |
| | | | 111b | 111b -> 53 kHz counter |
| [2:2] | T1_MODE_SEL | rw | 0x00* | Configuration of the timer T1 clock. |
| | | | 0b | Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56MHz). |
| | | | 1b | Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T1_PRESCALE_SEL). |
| [1:1] | T1_RELOAD_ENABLE | rw | 0x00* | If set to 0.the timer T1 will stop on expiration. |
| | | | 0b | After expiration the timer T1 will stop counting. i.e.. remain zero. reset value. |
| | | | 1b | After expiration the timer T1 will reload its preset value and continue counting down. |

**Table 31. CLIF_TIMER1_CONFIG (0x3F) register bit description**...*continued*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [0:0] | T1_ENABLE | rw | 0x0 | Enables the timer T1 |

### 9.18.1.17 CLIF_TIMER1_RELOAD (0x40)

This register provides the settings for CLIF_TIMER1_RELOAD

**Table 32. CLIF_TIMER1_RELOAD (0x40) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:20] | RESERVED | r- | 0x0 | Reserved |
| [19:0] | T1_RELOAD_VALUE | rw | 0x0000 | Reload value of the timer T1. |

### 9.18.1.18 TXLDO_VDDPA_CONFIG (0x54)

This register provides the settings for TXLDO_VDDPA_CONFIG

**Table 33. TXLDO_VDDPA_CONFIG (0x54) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:8] | RESERVED | rw | | Reserved |
| [7:0] | VDDPA_CONFIG | rw | | VDDPALDO output voltage VDDPA_1V50 |

### 9.18.1.19 TXLDO_VOUT_CURR (0x56)

This register provides the settings for TXLDO_VOUT_CURR

**Table 34. TXLDO_VOUT_CURR (0x56) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [23:8] | TXLDO_CURRENT | r- | | Indicates the TXLDO Current, measured value is indicated in mA (1 bit = 1 mA) |
| [7:0] | VDDPA_VOUT | r- | | VDDPALDO output voltage VDDPA_1V50 |

### 9.18.1.20 CLIF_RXM_FREQ (0x59)

This register provides the settings for CLIF_RXM_FREQ

**Table 35. CLIF_RXM_FREQ (0x59) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:31] | RXM_FREQ_VALID | r- | 0x00 | CLIF_RXM_FREQ_REG fields are valid |
| [30:25] | RESERVED | r- | 0x00 | Reserved |
| [24:16] | RXM_FREQ | r- | 0x00 | frequence difference between the last two consecutive measures at 1.7 MHz (multiple of 13.56 MHz/4096). Signed. 2-Complement coded. |
| [15:9] | RESERVED | r- | 0x00 | Reserved |
| [8:0] | RXM_PHASE | r- | 0x00 | phase value |

### 9.18.1.21 INTERPOLATED_RSSI_REG (0x5C)

This register provides the settings for INTERPOLATED_RSSI_REG

**Table 36. INTERPOLATED_RSSI_REG (0x5C) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:0] | INTERPOLATED_RSSI | r- | | Callculated Interpolated RSSI |

### 9.18.1.22 TX_NOV_CALIBRATE_AND_STORE_VAL_REG (0x5D)

This register provides the settings for TX_NOV_CALIBRATE_AND_STORE_VAL_REG

**Table 37. TX_NOV_CALIBRATE_AND_STORE_VAL_REG (0x5D) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:2] | RFU | rw | | Reserved |
| [1:0] | TX_NOV_CALIBRATE_STORE | rw | | Perform TX_NOV Calibration and store in User Area |

### 9.18.1.23 CLIF_SS_TX1_RTRANS0 (0x80)

This register provides the settings for CLIF_SS_TX1_RTRANS0

**Table 38. CLIF_SS_TX1_RTRANS0 (0x80) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:24] | TX1_SS_RTRANS3 | rw | 0x00 | TX1 rising transition value 3 |
| [23:16] | TX1_SS_RTRANS2 | rw | 0x00 | TX1 rising transition value 2 |
| [15:8] | TX1_SS_RTRANS1 | rw | 0x00 | TX1 rising transition value 1 |
| [7:0] | TX1_SS_RTRANS0 | rw | 0x00 | TX1 rising transition value 0 |

### 9.18.1.24 CLIF_SS_TX1_RTRANS1 (0x81)

This register provides the settings for CLIF_SS_TX1_RTRANS1

**Table 39. CLIF_SS_TX1_RTRANS1 (0x81) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:24] | TX1_SS_RTRANS7 | rw | 0x00 | TX1 rising transition value 7 |
| [23:16] | TX1_SS_RTRANS6 | rw | 0x00 | TX1 rising transition value 6 |
| [15:8] | TX1_SS_RTRANS5 | rw | 0x00 | TX1 rising transition value 5 |
| [7:0] | TX1_SS_RTRANS4 | rw | 0x00 | TX1 rising transition value 4 |

### 9.18.1.25 CLIF_SS_TX1_RTRANS2 (0x82)

This register provides the settings for CLIF_SS_TX1_RTRANS2

**Table 40. CLIF_SS_TX1_RTRANS2 (0x82) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:24] | TX1_SS_RTRANS11 | rw | 0x00 | TX1 rising transition value 11 |
| [23:16] | TX1_SS_RTRANS10 | rw | 0x00 | TX1 rising transition value 10 |

**Table 40. CLIF_SS_TX1_RTRANS2 (0x82) register bit description**...*continued*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [15:8] | TX1_SS_RTRANS9 | rw | 0x00 | TX1 rising transition value 9 |
| [7:0] | TX1_SS_RTRANS8 | rw | 0x00 | TX1 rising transition value 8 |

### 9.18.1.26 CLIF_SS_TX1_RTRANS3 (0x83)

This register provides the settings for CLIF_SS_TX1_RTRANS3

**Table 41. CLIF_SS_TX1_RTRANS3 (0x83) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:24] | TX1_SS_RTRANS15 | rw | 0x00 | TX1 rising transition value 15 |
| [23:16] | TX1_SS_RTRANS14 | rw | 0x00 | TX1 rising transition value 14 |
| [15:8] | TX1_SS_RTRANS13 | rw | 0x00 | TX1 rising transition value 13 |
| [7:0] | TX1_SS_RTRANS12 | rw | 0x00 | TX1 rising transition value 12 |

### 9.18.1.27 CLIF_SS_TX2_RTRANS0 (0x84)

This register provides the settings for CLIF_SS_TX2_RTRANS0

**Table 42. CLIF_SS_TX2_RTRANS0 (0x84) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:24] | TX2_SS_RTRANS3 | rw | 0x00 | TX2 rising transition value 3 |
| [23:16] | TX2_SS_RTRANS2 | rw | 0x00 | TX2 rising transition value 2 |
| [15:8] | TX2_SS_RTRANS1 | rw | 0x00 | TX2 rising transition value 1 |
| [7:0] | TX2_SS_RTRANS0 | rw | 0x00 | TX2 rising transition value 0 |

### 9.18.1.28 CLIF_SS_TX2_RTRANS1 (0x85)

This register provides the settings for CLIF_SS_TX2_RTRANS1

**Table 43. CLIF_SS_TX2_RTRANS1 (0x85) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:24] | TX2_SS_RTRANS7 | rw | 0x00 | TX2 rising transition value 7 |
| [23:16] | TX2_SS_RTRANS6 | rw | 0x00 | TX2 rising transition value 6 |
| [15:8] | TX2_SS_RTRANS5 | rw | 0x00 | TX2 rising transition value 5 |
| [7:0] | TX2_SS_RTRANS4 | rw | 0x00 | TX2 rising transition value 4 |

### 9.18.1.29 CLIF_SS_TX2_RTRANS2 (0x86)

This register provides the settings for CLIF_SS_TX2_RTRANS2

**Table 44. CLIF_SS_TX2_RTRANS2 (0x86) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:24] | TX2_SS_RTRANS11 | rw | 0x00 | TX2 rising transition value 11 |
| [23:16] | TX2_SS_RTRANS10 | rw | 0x00 | TX2 rising transition value 10 |

**Table 44. CLIF_SS_TX2_RTRANS2 (0x86) register bit description**...*continued*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [15:8] | TX2_SS_RTRANS9 | rw | 0x00 | TX2 rising transition value 9 |
| [7:0] | TX2_SS_RTRANS8 | rw | 0x00 | TX2 rising transition value 8 |

### 9.18.1.30 CLIF_SS_TX2_RTRANS3 (0x87)

This register provides the settings for CLIF_SS_TX2_RTRANS3

**Table 45. CLIF_SS_TX2_RTRANS3 (0x87) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:24] | TX2_SS_RTRANS15 | rw | 0x00 | TX2 rising transition value 15 |
| [23:16] | TX2_SS_RTRANS14 | rw | 0x00 | TX2 rising transition value 14 |
| [15:8] | TX2_SS_RTRANS13 | rw | 0x00 | TX2 rising transition value 13 |
| [7:0] | TX2_SS_RTRANS12 | rw | 0x00 | TX2 rising transition value 12 |

### 9.18.1.31 CLIF_SS_TX1_FTRANS0 (0x88)

This register provides the settings for CLIF_SS_TX1_FTRANS0

**Table 46. CLIF_SS_TX1_FTRANS0 (0x88) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:24] | TX1_SS_FTRANS3 | rw | 0x00 | TX1 falling transition value 3 |
| [23:16] | TX1_SS_FTRANS2 | rw | 0x00 | TX1 falling transition value 2 |
| [15:8] | TX1_SS_FTRANS1 | rw | 0x00 | TX1 falling transition value 1 |
| [7:0] | TX1_SS_FTRANS0 | rw | 0x00 | TX1 falling transition value 0 |

### 9.18.1.32 CLIF_SS_TX1_FTRANS1 (0x89)

This register provides the settings for CLIF_SS_TX1_FTRANS1

**Table 47. CLIF_SS_TX1_FTRANS1 (0x89) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:24] | TX1_SS_FTRANS7 | rw | 0x00 | TX1 falling transition value 7 |
| [23:16] | TX1_SS_FTRANS6 | rw | 0x00 | TX1 falling transition value 6 |
| [15:8] | TX1_SS_FTRANS5 | rw | 0x00 | TX1 falling transition value 5 |
| [7:0] | TX1_SS_FTRANS4 | rw | 0x00 | TX1 falling transition value 4 |

### 9.18.1.33 CLIF_SS_TX1_FTRANS2 (0x8A)

This register provides the settings for CLIF_SS_TX1_FTRANS2

**Table 48. CLIF_SS_TX1_FTRANS2 (0x8A) register bit description**

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| [31:24] | TX1_SS_FTRANS11 | rw | 0x00 | TX1 falling transition value 11 |
| [23:16] | TX1_SS_FTRANS10 | rw | 0x00 | TX1 falling transition value 10 |

**Table 48. CLIF_SS_TX1_FTRANS2 (0x8A) register bit description**...*continued*

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [15:8] | TX1_SS_FTRANS9 | rw | 0x00 | TX1 falling transition value 9 |
| [7:0] | TX1_SS_FTRANS8 | rw | 0x00 | TX1 falling transition value 8 |

### 9.18.1.34  CLIF_SS_TX1_FTRANS3 (0x8B)

This register provides the settings for CLIF_SS_TX1_FTRANS3

**Table 49.  CLIF_SS_TX1_FTRANS3 (0x8B) register bit description**

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [31:24] | TX1_SS_FTRANS15 | rw | 0x00 | TX1 falling transition value 15 |
| [23:16] | TX1_SS_FTRANS14 | rw | 0x00 | TX1 falling transition value 14 |
| [15:8] | TX1_SS_FTRANS13 | rw | 0x00 | TX1 falling transition value 13 |
| [7:0] | TX1_SS_FTRANS12 | rw | 0x00 | TX1 falling transition value 12 |

### 9.18.1.35  CLIF_SS_TX2_FTRANS0 (0x8C)

This register provides the settings for CLIF_SS_TX2_FTRANS0

**Table 50.  CLIF_SS_TX2_FTRANS0 (0x8C) register bit description**

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [31:24] | TX2_SS_FTRANS3 | rw | 0x00 | TX2 falling transition value 3 |
| [23:16] | TX2_SS_FTRANS2 | rw | 0x00 | TX2 falling transition value 2 |
| [15:8] | TX2_SS_FTRANS1 | rw | 0x00 | TX2 falling transition value 1 |
| [7:0] | TX2_SS_FTRANS0 | rw | 0x00 | TX2 falling transition value 0 |

### 9.18.1.36  CLIF_SS_TX2_FTRANS1 (0x8D)

This register provides the settings for CLIF_SS_TX2_FTRANS1

**Table 51.  CLIF_SS_TX2_FTRANS1 (0x8D) register bit description**

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [31:24] | TX2_SS_FTRANS7 | rw | 0x00 | TX2 falling transition value 7 |
| [23:16] | TX2_SS_FTRANS6 | rw | 0x00 | TX2 falling transition value 6 |
| [15:8] | TX2_SS_FTRANS5 | rw | 0x00 | TX2 falling transition value 5 |
| [7:0] | TX2_SS_FTRANS4 | rw | 0x00 | TX2 falling transition value 4 |

### 9.18.1.37  CLIF_SS_TX2_FTRANS2 (0x8E)

This register provides the settings for CLIF_SS_TX2_FTRANS2

**Table 52.  CLIF_SS_TX2_FTRANS2 (0x8E) register bit description**

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [31:24] | TX2_SS_FTRANS11 | rw | 0x00 | TX2 falling transition value 11 |
| [23:16] | TX2_SS_FTRANS10 | rw | 0x00 | TX2 falling transition value 10 |

**Table 52. CLIF_SS_TX2_FTRANS2 (0x8E) register bit description**...*continued*

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [15:8] | TX2_SS_FTRANS9 | rw | 0x00 | TX2 falling transition value 9 |
| [7:0] | TX2_SS_FTRANS8 | rw | 0x00 | TX2 falling transition value 8 |

### 9.18.1.38  CLIF_SS_TX2_FTRANS3 (0x8F)

This register provides the settings for CLIF_SS_TX2_FTRANS3

**Table 53.  CLIF_SS_TX2_FTRANS3 (0x8F) register bit description**

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| [31:24] | TX2_SS_FTRANS15 | rw | 0x00 | TX2 falling transition value 15 |
| [23:16] | TX2_SS_FTRANS14 | rw | 0x00 | TX2 falling transition value 14 |
| [15:8] | TX2_SS_FTRANS13 | rw | 0x00 | TX2 falling transition value 13 |
| [7:0] | TX2_SS_FTRANS12 | rw | 0x00 | TX2 falling transition value 12 |

## 9.18.2 EEPROM configuration description

The settings done in EEPROM are used for basic configuration which does not change frequently. Typically it is performed once during trimming or configuration of a product. The EEPROM has a limited number of erase/write cycles that can be performed. This means, that configurations that change frequently must be performed in standard registers which do not keep their value during reset and power off.

This section describes the EEPROM configuration of the PN7220.

**Writing to the EEPROM has to be performed with Read-Modify-Write for all memory addresses which contain RFU bits.**

### 9.18.2.1 EEPROM configuration for power, TXLDO, XTAL and clocks

This section provides the configuration of different EEPROM parameters for the system.

#### 9.18.2.1.1 List of EEPROM configuration parameters for power, TXLDO, XTAL and clocks

**Table 54. List of EEPROM configuration parameters for power, TXLDO, XTAL and Clocks**

| Configuration Parameter | Address (Hex) | Address (Decimal) | Size (in bytes) | EEPROM_AREA |
|---|---|---|---|---|
| DCDC_PWR_CONFIG (0x0000) | 0x0000 | 0 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| DCDC_CONFIG (0x0001) | 0x0001 | 1 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| TXLDO_CONFIG (0x0002) | 0x0002 | 2 | 4 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| TXLDO_VDDPA_CONFIG (0x0006) | 0x0006 | 6 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| TXLDO_VDDPA_MAX_RDR (0x0007) | 0x0007 | 7 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| TXLDO_VDDPA_MAX_CARD (0x0008) | 0x0008 | 8 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| BOOST_DEFAULT_VOLTAGE (0x0009) | 0x0009 | 9 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| XTAL_CONFIG (0x000F) | 0x000F | 15 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| XTAL_TIMEOUT (0x0010) | 0x0010 | 16 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| CLK_INPUT_FREQ (0x0011) | 0x0011 | 17 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| XTAL_CHECK_DELAY (0x0012) | 0x0012 | 18 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |

### 9.18.2.1.2 DCDC_PWR_CONFIG (0x0000)

Configuration for power.

**Table 55. DCDC_PWR_CONFIG (0x0000)**

| Function | bit | Values | Description |
|---|---|---|---|
| DC-DC usage in card mode | [7] | 0x00 | DC-DC is not powered and set to bypass |
| | | 0x01 | DC-DC is powered and not bypassed |
| DC-DC usage in reader mode | [6] | 0x00 | DC-DC is not powered and set to bypass |
| | | 0x01 | DC-DC is powered and not bypassed |
| RFU | [5] | | Do not touch. Default value is 0x01 |
| VUP input voltage | [4:0] | 0x00 | Not connected or 0 V |
| | | 0x01 | No DC-DC and internal VDDPA_LDO: VUP supplied by VBAT / VBATPWR (pin VUP_TX connected to VBAT/VBATPWR) |
| | | 0x02 | Internal DC-DC used: with fixed VDDBOOST |
| | | 0x03 | RFU |
| | | 0x04 | Internal DC-DC used: with auto by pass and variable boost w.r.t VDDPA (internal DPC controls VDDBOOST): DC-DC goes into pass through mode when the VDDPA goes below 3.3 V. When VDDPA is greater than 3.3 V, the DC-DC is configured to boost voltage in range of 3.3 V to 6 V. |
| | | 0x05 - 0x09 | RFU |
| | | 0x10 | Internal VDDPA_LDO used, internal DC-DC not used: VUP supplied by external LDO (not connected to VBAT) |

### 9.18.2.1.3 DCDC_CONFIG (0x0001)

DCDC Configuration

**Table 56. DCDC_CONFIG (0x0001)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7:5] | | Reserved |
| DC-DC pass through feature | [4] | 0x00 | DC-DC pass through feature is not supported ($V_{out}$ = 0 V or 5 V) |
| | | 0x01 | DC-DC pass through feature is supported ($V_{out}$ = 0 V or 5 V) |
| DC-DC for LPCD | [3] | 0x00 | Use of DC-DC for LPCD disabled |
| | | 0x01 | Use of DC-DC for LPCD enabled |
| RFU | [2:0] | | Reserved |

### 9.18.2.1.4 TXLDO_CONFIG (0x0002)

**Table 57. TXLDO_CONFIG (0x0002)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [31:2] | | Reserved |
| Overcurrent protection | [1] | 0x00 | Overcurrent protection feature disabled |
| | | 0x01 | Overcurrent protection feature enabled |
| Enable Tx-LDO | [0] | 0x00 | TxLDO is disabled. No voltage output of the TXLDO |
| | | 0x01 | TxLDO is enabled. Regulated voltage output of the TXLDO |
| RFU | [2:0] | | Reserved |

### 9.18.2.1.5 TXLDO_VDDPA_CONFIG (0x0006)

**Table 58. TXLDO_VDDPA_CONFIG (0x0006)**

| Function | bit | Values | Description |
|---|---|---|---|
| VDDPA voltage level<br>TX_LDO output: initial voltage in case the DPC is used. Applies directly at the beginning of the RF-field-on before any DPC regulation takes place. (Initial VDDPA Voltage at RF ON). These values define as well the TX_LDO output voltage in case the DPC is disabled and not used. | [7:0] | 0x00 - 0x2A | Value 0 indicates 1.5 V. Further VDDPA voltage would be 1.5 V + 0.1 V × this parameter value. Maximum value of 0x2A indicates for 5.7 V |

### 9.18.2.1.6 TXLDO_VDDPA_MAX_RDR_NFC_FORUM (0x0007)

**Table 59. TXLDO_VDDPA_MAX_RDR_NFC_FORUM (0x0007)**

| Function | bit | Values | Description |
|---|---|---|---|
| VDDPA max voltage level for NFC Forum<br>VDDPA maximum output voltage in case the DPC is enabled in reader mode.<br>This is used only when DPC is enabled. This ensures the Maximum Voltage up to which VDDPA reached during DPC Regulation. | [7:0] | 0x00 - 0x2A | Value 0 indicates 1.5 V. Further VDDPA voltage would be 1.5 + 0.1 V × this parameter value. Maximum value of 0x2A indicates for 5.7 V |

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### 9.18.2.1.7 TXLDO_VDDPA_MAX_RDR_EMVCo (0x06A6)

**Table 60. TXLDO_VDDPA_MAX_RDR_EMVCo (0x06A6)**

| Function | bit | Values | Description |
|---|---|---|---|
| VDDPA max voltage level for EMVCo<br>VDDPA maximum output voltage in case the DPC is enabled in reader mode.<br>This is used only when DPC is enabled. This ensures the Maximum Voltage up to which VDDPA reached during DPC Regulation. | [7:0] | 0x00 - 0x2A | Value 0 indicates 1.5 V. Further VDDPA voltage would be 1.5 + 0.1 V × this parameter value. Maximum value of 0x2A indicates for 5.7 V |

### 9.18.2.1.8 TXLDO_VDDPA_MAX_CARD (0x0008)

**Table 61. TXLDO_VDDPA_MAX_CARD (0x0008)**

| Function | bit | Values | Description |
|---|---|---|---|
| VDDPA max voltage level for Cardmode | [7:0] | 0x00 - 0x2A | Value 0 indicates 1.5 V. Further VDDPA voltage would be 1.5 + 0.1 V × this parameter value. Maximum value of 0x2A indicates for 5.7 V |

### 9.18.2.1.9 BOOST_DEFAULT_VOLTAGE (0x0009)

**Table 62. BOOST_DEFAULT_VOLTAGE (0x0009)**

| Function | bit | Values | Description |
|---|---|---|---|
| VDDBOOST output voltage | [7:0] | 0x00 - 0x1D | Value 0 indicates 3.1 V. Further VDDBOOST voltage would be 3.1 V + 0.1 V × this parameter value. Maximum value of 0x1D indicates for 6 V |
|  |  | Other values | RFU |

### 9.18.2.1.10 XTAL_CONFIG (0x000F)

Configuration for the XTAL startup procedure

**Table 63. XTAL_CONFIG (0x000F)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7:1] |  | RFU |
| XTAL startup procedure | [0] | 0x00 | disable Crystal recalibration start after wake-up |
|  |  | 0x01 | enable Crystal recalibration start after wake-up |

### 9.18.2.1.11 XTAL_TIMEOUT (0x0010)

Timeout for XTAL to be ready

**Table 64. XTAL_TIMEOUT (0x0010)**

| Function | bit | Values | Description |
|---|---|---|---|
| Configuration for XTAL startup procedure | [7:0] | | Timeout for XTAL to be ready (in *128 μs). This configuration does not speed up the boot time. |

### 9.18.2.1.12 XTAL_DELAY (06B8h)

Used to configure the crystal start and stop timings.

**Table 65. XTAL_DELAY (address 06B8h) EEPROM configuration bit description**

| Address (hex) | Function | Bit | Description |
|---|---|---|---|
| 06B8 | XTAL_Delay | 7:0 | Configurable wait time to start the XTAL.<br>1 unit = 128 microsecond<br>Total delay = Unit x 50 loops<br>Default value = 1 = 6.4 millisecond |
| 06B9 | Delay-To-OFF | 7:0 | Delay before shutting down the LDO.<br>After DCDC shutdown, when DPC is enabled to allow the cap on the LDO to discharge.<br>1 unit = 128 microsecond<br>Default value = 1 = 128 microsecond |
| 06BA | - | 7:0 | RFU |
| 06BB | - | 7:0 | RFU |

### 9.18.2.1.13  CLK_INPUT_FREQ (0x0011)

Configuration for the PLL input clock frequency

**Table 66.  CLK_INPUT_FREQ (0x0011)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7:4] | | RFU |
| PLL clock configuration | [3:0] | 0x00 | RFU |
| | | 0x01 | RFU |
| | | 0x02 | 19,2 MHz - Low RF performance can be expected using this external clock frequency. |
| | | 0x03 | 24 MHz |
| | | 0x04 | 32 MHz |
| | | 0x05 | 48 MHz - Acceptable RF performance can be achieved using this external clock frequency. |
| | | 0x06 | RFU |
| | | 0x07 | RFU |
| | | 0x08 | XTAL 27.12 MHz - Best RF Performance - Recommended for EMVCo compliant applications |
| | | others | RFU |

### 9.18.2.1.14  XTAL_CHECK_DELAY (0x0012)

**Table 67.  XTAL_CHECK_DELAY (0x0012)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFRetry_numberU | [7:5] | | Max Number of retries before a clock error is raised |
| Interval | [4:0] | | Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18.8 μs). This is the time to try to lock the PLL, a stable crystal clock is required for locking. If the PLL is not locked, a next retry to lock the PLL will be done after this interval. This value can be used to optimize the startup time dependent on the crystal characteristics. This is important, e.g., for optimization of the LPCD. |

### 9.18.2.1.15 VDDPA_DISCHARGE (0x050D)

enable/disable fast VDDPA Discharge

**Table 68. VDDPA_DISCHARGE (0x050D)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7:1] | | Reserved |
| EnableFast VDDPADischarge | [0] | 0x00 | Disables fast discharge of VDDPA by setting VDDPA = 5.7 V and then to 1.5 V, during RF OFF |
| | | 0x01 | Enables fast discharge of VDDPA by setting VDDPA = 5.7 V and then to 1.5 V, during RF OFF (default) |

### 9.18.2.2 RM_TX_SHAPING - TX wave shaping for passive reader mode

This section provides the TX shaping for different type of cards in passive reader mode.

### 9.18.2.2.1 TX wave shaping for TypeA passive reader mode for all baud-rates.

This section provides the TX shaping for TypeA passive reader mode.

### 9.18.2.2.1.1 RESIDUAL_AMPL_LEVEL_A106 (0x0014)

Residual amplitude level for A106

**Table 69. RESIDUAL_AMPL_LEVEL_A106 (0x0014)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.1.2 EDGE_TYPE_A106 (0x0015)

Edge type for A106

**Table 70. EDGE_TYPE_A106 (0x0015)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | 0x01 | linear transition between two amplitude levels |
| | | 0x02 | two linear transitions between amplitude levels |
| | | 0x03 | three linear transitions between amplitude levels |
| | | Others | RFU |
| | | Lookup table based shaping | |
| | | 0x04 | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | 0x05 | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | 0x06 | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | Others | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | 0x01 | linear transition between two amplitude levels |
| | | 0x02 | two linear transitions between amplitude levels |
| | | 0x03 | three linear transitions between amplitude levels |
| | | Others | RFU |
| | | Lookup table based shaping | |
| | | 0x04 | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | 0x05 | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | 0x06 | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | Others | RFU |

### 9.18.2.2.1.3 EDGE_STYLE_A106 (0x0016)

Time constant Edge style configuration for A106

**Table 71. EDGE_STYLE_A106 (0x0016)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_A106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ A106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_A106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ A106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.1.4 EDGE_LENGTH_A106 (0x0017)

Edge length for A106

**Table 72. EDGE_LENGTH_A106 (0x0017)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.1.5 RESIDUAL_AMPL_LEVEL_A212 (0x0018)

**Table 73. RESIDUAL_AMPL_LEVEL_A212 (0x0018)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.1.6 EDGE_TYPE_A212 (0x0019)

**Table 74. EDGE_TYPE_A212 (0x0019)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.1.7 EDGE_STYLE_A212 (0x001A)

**Table 75. EDGE_STYLE_A212 (0x001A)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_A212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ A212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_A212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ A212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.1.8 EDGE_LENGTH_A212 (0x001B)

**Table 76. EDGE_LENGTH_A212 (0x001B)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) | |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.1.9 RESIDUAL_AMPL_LEVEL_A424 (0x001C)

**Table 77. RESIDUAL_AMPL_LEVEL_A424 (0x001C)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.1.10  EDGE_TYPE_A424 (0x001D)

**Table 78.  EDGE_TYPE_A424 (0x001D)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.1.11 EDGE_STYLE_A424 (0x001E)

**Table 79. EDGE_STYLE_A424 (0x001E)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_A424 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ A424 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_A424 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ A424 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.1.12 EDGE_LENGTH_A424 (0x001F)

**Table 80. EDGE_LENGTH_A424 (0x001F)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.1.13 RESIDUAL_AMPL_LEVEL_A848 (0x0020)

**Table 81. RESIDUAL_AMPL_LEVEL_A848 (0x0020)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.1.14 EDGE_TYPE_A848 (0x0021)

**Table 82. EDGE_TYPE_A848 (0x0021)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.1.15 EDGE_STYLE_A848 (0x0022)

**Table 83. EDGE_STYLE_A848 (0x0022)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_A848 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ A848 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_A848 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ A848 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.1.16 EDGE_LENGTH_A848 (0x0023)

**Table 84. EDGE_LENGTH_A848 (0x0023)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.2 TX wave shaping for Type B passive reader mode for all baud-rates.

This section provides the TX shaping for Type B passive reader mode.

### 9.18.2.2.2.1 RESIDUAL_AMPL_LEVEL_B106 (0x0024)

**Table 85. RESIDUAL_AMPL_LEVEL_B106 (0x0024)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.2.2  EDGE_TYPE_B106 (0x0025)

**Table 86. EDGE_TYPE_B106 (0x0025)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.2.3  EDGE_STYLE_B106 (0x0026)

**Table 87.  EDGE_STYLE_B106 (0x0026)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_B106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ B106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_B106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ B106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.2.4  EDGE_LENGTH_B106 (0x0027)

**Table 88.  EDGE_LENGTH_B106 (0x0027)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) | |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.2.5  RESIDUAL_AMPL_LEVEL_B212 (0x0028)

**Table 89.  RESIDUAL_AMPL_LEVEL_B212 (0x0028)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

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### 9.18.2.2.2.6  EDGE_TYPE_B212 (0x0029)

**Table 90.  EDGE_TYPE_B212 (0x0029)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.2.7 EDGE_STYLE_B212 (0x002A)

**Table 91. EDGE_STYLE_B212 (0x002A)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_B212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ B212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_B212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ B212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.2.8 EDGE_LENGTH_B212 (0x002B)

**Table 92. EDGE_LENGTH_B212 (0x002B)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.2.9 RESIDUAL_AMPL_LEVEL_B424 (0x002C)

**Table 93. RESIDUAL_AMPL_LEVEL_B424 (0x002C)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.2.10 EDGE_TYPE_B424 (0x002D)

**Table 94. EDGE_TYPE_B424 (0x002D)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.2.11 EDGE_STYLE_B424 (0x002E)

**Table 95. EDGE_STYLE_B424 (0x002E)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_B424 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ B424 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_B424 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ B424 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.2.12 EDGE_LENGTH_B424 (0x002F)

**Table 96. EDGE_LENGTH_B424 (0x002F)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) | |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.2.13 RESIDUAL_AMPL_LEVEL_B848 (0x0030)

**Table 97. RESIDUAL_AMPL_LEVEL_B848 (0x0030)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.2.14 EDGE_TYPE_B848 (0x0031)

**Table 98. EDGE_TYPE_B848 (0x0031)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

#### 9.18.2.2.2.15 EDGE_STYLE_B848 (0x0032)

**Table 99. EDGE_STYLE_B848 (0x0032)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_B848 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ B848 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_B848 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ B848 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

#### 9.18.2.2.2.16 EDGE_LENGTH_B848 (0x0033)

**Table 100. EDGE_LENGTH_B848 (0x0033)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.3 TX wave shaping for Type F passive reader mode for all baud-rates.

This section provides the TX shaping for Type F passive reader mode.

#### 9.18.2.2.3.1 RESIDUAL_AMPL_LEVEL_F212 (0x0034)

**Table 101. RESIDUAL_AMPL_LEVEL_F212 (0x0034)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.3.2 EDGE_TYPE_F212 (0x0035)

**Table 102. EDGE_TYPE_F212 (0x0035)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.3.3 EDGE_STYLE_F212 (0x0036)

**Table 103. EDGE_STYLE_F212 (0x0036)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_F212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_F212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_F212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_F212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.3.4 EDGE_LENGTH_F212 (0x0037)

**Table 104. EDGE_LENGTH_F212 (0x0037)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) | |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.3.5 RESIDUAL_AMPL_LEVEL_F424 (0x0038)

**Table 105. RESIDUAL_AMPL_LEVEL_F424 (0x0038)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.3.6  EDGE_TYPE_F424 (0x0039)

**Table 106.  EDGE_TYPE_F424 (0x0039)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.3.7 EDGE_STYLE_F424 (0x003A)

**Table 107. EDGE_STYLE_F424 (0x003A)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_F424 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_F424 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_F424 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_F424 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.3.8 EDGE_LENGTH_F424 (0x003B)

**Table 108. EDGE_LENGTH_F424 (0x003B)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) | |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.4 TX wave shaping for Type V (ISO15693) passive reader mode for all baud-rates.

This section provides the TX shaping for Type V (ISO15693) passive reader mode.

### 9.18.2.2.4.1 RESIDUAL_AMPL_LEVEL_V10_26 (0x004C)

**Table 109. RESIDUAL_AMPL_LEVEL_V10_26 (0x004C)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

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### 9.18.2.2.4.2 EDGE_TYPE_V10_26 (0x004D)

**Table 110. EDGE_TYPE_V10_26 (0x004D)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.4.3  EDGE_STYLE_V10_26 (0x004E)

Table 111.  EDGE_STYLE_V10_26 (0x004E)

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V10_26 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ V10_26 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V10_ 26 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ V10_26 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.4.4  EDGE_LENGTH_V10_26 (0x004F)

Table 112.  EDGE_LENGTH_V10_26 (0x004F)

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) | |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.4.5  RESIDUAL_AMPL_LEVEL_V10_53 (0x0050)

Table 113.  RESIDUAL_AMPL_LEVEL_V10_53 (0x0050)

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.4.6  EDGE_TYPE_V10_53 (0x0051)

**Table 114.  EDGE_TYPE_V10_53 (0x0051)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.4.7 EDGE_STYLE_V10_53 (0x0052)

**Table 115. EDGE_STYLE_V10_53 (0x0052)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V10_53 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ V10_53 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V10_ 53 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ V10_53 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.4.8 EDGE_LENGTH_V10_53 (0x0053)

**Table 116. EDGE_LENGTH_V10_53 (0x0053)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.4.9 RESIDUAL_AMPL_LEVEL_V10_106 (0x0054)

**Table 117. RESIDUAL_AMPL_LEVEL_V10_106 (0x0054)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.4.10  EDGE_TYPE_V10_106 (0x0055)

**Table 118.  EDGE_TYPE_V10_106 (0x0055)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.4.11 EDGE_STYLE_V10_106 (0x0056)

**Table 119. EDGE_STYLE_V10_106 (0x0056)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V10_106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_V10_106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V10_106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_V10_106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.4.12 EDGE_LENGTH_V10_106 (0x0057)

**Table 120. EDGE_LENGTH_V10_106 (0x0057)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.4.13 RESIDUAL_AMPL_LEVEL_V10_212 (0x0058)

**Table 121. RESIDUAL_AMPL_LEVEL_V10_212 (0x0058)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.4.14 EDGE_TYPE_V10_212 (0x0059)

**Table 122. EDGE_TYPE_V10_212 (0x0059)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | 0x01 | linear transition between two amplitude levels |
| | | 0x02 | two linear transitions between amplitude levels |
| | | 0x03 | three linear transitions between amplitude levels |
| | | Others | RFU |
| | | Lookup table based shaping | |
| | | 0x04 | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | 0x05 | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | 0x06 | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | Others | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | 0x01 | linear transition between two amplitude levels |
| | | 0x02 | two linear transitions between amplitude levels |
| | | 0x03 | three linear transitions between amplitude levels |
| | | Others | RFU |
| | | Lookup table based shaping | |
| | | 0x04 | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | 0x05 | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | 0x06 | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | Others | RFU |

### 9.18.2.2.4.15 EDGE_STYLE_V10_212 (0x005A)

**Table 123. EDGE_STYLE_V10_212 (0x005A)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V10_212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_V10_212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V10_212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_V10_212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.4.16 EDGE_LENGTH_V10_212 (0x005B)

**Table 124. EDGE_LENGTH_V10_212 (0x005B)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.4.17 RESIDUAL_AMPL_LEVEL_V100_26 (0x003C)

**Table 125. RESIDUAL_AMPL_LEVEL_V100_26 (0x003C)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.4.18  EDGE_TYPE_V100_26 (0x003D)

**Table 126.  EDGE_TYPE_V100_26 (0x003D)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.4.19 EDGE_STYLE_V100_26 (0x003E)

**Table 127. EDGE_STYLE_V100_26 (0x003E)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V100_ 26 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ V100_26 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V100_ 26 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ V100_26 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.4.20 EDGE_LENGTH_V100_26 (0x003F)

**Table 128. EDGE_LENGTH_V100_26 (0x003F)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) | |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.4.21 RESIDUAL_AMPL_LEVEL_V100_53 (0x0040)

**Table 129. RESIDUAL_AMPL_LEVEL_V100_53 (0x0040)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.4.22 EDGE_TYPE_V100_53 (0x0041)

**Table 130. EDGE_TYPE_V100_53 (0x0041)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.4.23 EDGE_STYLE_V100_53 (0x0042)

**Table 131. EDGE_STYLE_V100_53 (0x0042)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V100_53 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_V100_53 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V100_53 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_V100_53 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.4.24 EDGE_LENGTH_V100_53 (0x0043)

**Table 132. EDGE_LENGTH_V100_53 (0x0043)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.4.25 RESIDUAL_AMPL_LEVEL_V100_106 (0x0044)

**Table 133. RESIDUAL_AMPL_LEVEL_V100_106 (0x0044)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.4.26 EDGE_TYPE_V100_106 (0x0045)

**Table 134. EDGE_TYPE_V100_106 (0x0045)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | 0x01 | linear transition between two amplitude levels |
| | | 0x02 | two linear transitions between amplitude levels |
| | | 0x03 | three linear transitions between amplitude levels |
| | | Others | RFU |
| | | Lookup table based shaping | |
| | | 0x04 | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | 0x05 | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | 0x06 | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | Others | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | 0x01 | linear transition between two amplitude levels |
| | | 0x02 | two linear transitions between amplitude levels |
| | | 0x03 | three linear transitions between amplitude levels |
| | | Others | RFU |
| | | Lookup table based shaping | |
| | | 0x04 | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | 0x05 | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | 0x06 | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | Others | RFU |

### 9.18.2.2.4.27  EDGE_STYLE_V100_106 (0x0046)

**Table 135.  EDGE_STYLE_V100_106 (0x0046)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V100_106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_V100_106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V100_106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_V100_106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.4.28  EDGE_LENGTH_V100_106 (0x0047)

**Table 136.  EDGE_LENGTH_V100_106 (0x0047)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.2.4.29  RESIDUAL_AMPL_LEVEL_V100_212 (0x0048)

**Table 137.  RESIDUAL_AMPL_LEVEL_V100_212 (0x0048)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.2.4.30  EDGE_TYPE_V100_212 (0x0049)

**Table 138.  EDGE_TYPE_V100_212 (0x0049)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.2.4.31 EDGE_STYLE_V100_212 (0x004A)

**Table 139. EDGE_STYLE_V100_212 (0x004A)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V100_212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_V100_212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_V100_212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_V100_212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.2.4.32 EDGE_LENGTH_V100_212 (0x004B)

**Table 140. EDGE_LENGTH_V100_212 (0x004B)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) | |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

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**Product data sheet**

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Document feedback

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### 9.18.2.3 DPC NFC FORUM settings

This section provides the settings related to DPC configuration

#### 9.18.2.3.1 DPC_CONFIG (0x0068)

DPC configuration

**Table 141. DPC_CONFIG (0x0068)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7:3] | | RFU |
| DPC in Active target mode | [2] | | DPC configuration in active target mode |
| | | `0x00` | disabled |
| | | `0x01` | enabled |
| DPC in Active initiator mode | [1] | | DPC configuration in active initiator mode |
| | | `0x00` | disabled |
| | | `0x01` | enabled |
| DPC in Reader/Passive Initiator mode | [0] | | DPC configuration in Reader/ Passive Initiator mode |
| | | `0x00` | disabled |
| | | `0x01` | enabled |

#### 9.18.2.3.2 DPC_TARGET_CURRENT (0x0069)

DPC configuration unloaded VDDPA target current in mA

**Table 142. DPC_TARGET_CURRENT (0x0069)**

| Function | bit | Values | Description |
|---|---|---|---|
| DPC in Active target mode | [15:0] | | VDDPA target current in mA. The target current +/- hysteresis defines the limiting maximum current for the DPC. |

Note: This configuration shall not exceed 350 mA - hysteresis.

Note: The resulting current that is driven by the transmitter can be further reduced based on the current reduction lookup table entries.

### 9.18.2.3.3 DPC_HYSTERESIS_LOADING (0x006B)

The hysteresis (**bHysteresis** and **bHysteresis_Unloading**) together with the target current (**wTargetCurrent**) defines the current limit, at which the DPC automatically decreases or raises the VDDPA. The VDDPA is automatically reduced, as soon as the current exceeds the **wTargetCurrent + bHysteresis**, and the VDDPA is automatically increased again, as soon as the current is below **wTargetCurrent # bHysteresis_Unloading**.

**Table 143. DPC_HYSTERESIS_LOADING (0x006B)**

| Function | bit | Values | Description |
|---|---|---|---|
| DPC hysteresis loading | [7:0] | | Absolute difference to current Target Current in mA that triggers a DPC update event during loading. |

***Note:*** *If the hysteresis is configured too small, it might cause an oscillation of the transmitted field.*

*In most application, the default values work well and do not need to be modified.*

### 9.18.2.3.4 DPC_HYSTERESIS_UNLOADING (0x006E)

**Table 144. DPC_HYSTERESIS_UNLOADING (0x006E)**

| Function | bit | Values | Description |
|---|---|---|---|
| DPC hysteresis unloading | [7:0] | | Absolute difference to current Target Current in mA that triggers a DPC update event during unloading. |

### 9.18.2.3.5 DPC_TXLDOVDDPALow (0x006F)

**Table 145. DPC_TXLDOVDDPALow (0x006F)**

| Function | bit | Values | Description |
|---|---|---|---|
| TXLDOVDDPALow | [7:0] | | VDDPA Low Limit for RDON |

### 9.18.2.3.6 DPC_TXGSN (0x0070)

TXGSN configuration.

**Table 146. DPC_TXGSN (0x0070)**

| Function | bit | Values | Description |
|---|---|---|---|
| DPC hysterisis loading | [7:0] | Less than 20 | resistance = 10 Ω / (tx1_gsn + 1) |
| | | more than or equal 20 | 20: resistance = 0.5 Ω |

### 9.18.2.3.7 DPC_RDON_CONTROL (0x0071)

**Table 147. DPC_RDON_CONTROL (0x0071)**

| Function | bit | Values | Description |
|---|---|---|---|
| VDDPA low limit control | [7:0] | 0x00 | Disabled |
| | | 0x01 | RdON Control |
| | | 0x02 | PWM control |
| | | Others | RFU |

### 9.18.2.3.8 DPC_InitialRDOn_RFOn (0x0072)

**Table 148. DPC_InitialRDOn_RFOn (0x0072)**

| Function | bit | Values | Description |
|---|---|---|---|
| DPC_InitialRDOn_RFOn | [7:0] | | Initial GSP TX1/TX2 value during FieldON |

### 9.18.2.3.9 DPC_TXLDO_MAX_DROPOUT (0x0073)

**Table 149. DPC_TXLDO_MAX_DROPOUT (0x0073)**

| Function | bit | Values | Description |
|---|---|---|---|
| DPC_TXLDO_MAX_DROPOUT | [15:0] | | At DPC start (on initial RF ON), if TXLDO drop out is higher to this value then VDDPA is reduced to: e VddpaSafe if no boost bypass on going else Vddpa is stopped. Unit is mV. Default = E10h = 3600 mV. |

### 9.18.2.3.10 DPC_GUARD_TIME (0x0079)

**Table 150. DPC_GUARD_TIME (0x0079)**

| Function | bit | Values | Description |
|---|---|---|---|
| algointerval | [7:0] | | DPC guard time configuration. Guard time before tx. 1 unit = 1 µs. |

The DPC regulation is done once before TX and once after RX.

The guard time parameter is the time between DPC regulation completion and TX start.

The guard time parameter is the time between RX stop and DPC regulation start.

The guard time is always enabled for TX

**Note:** Recommendation is not to modify the default value.

### 9.18.2.3.11 DPC_ENABLE_DURING_FDT (0x007A)

DPC regulation enable during FDT.

**Table 151. DPC_ENABLE_DURING_FDT (0x007A)**

| Function | bit | Values | Description |
|---|---|---|---|
| Disable DPC during FDT | [7:0] | 0x00 | DPC disabled during FDT (debug purpose only) |
| | | 0x01 | DPC enabled during FDT (recommendation) |
| | | others | RFU |

### 9.18.2.3.12 DPC_GUARD_TIME_AFTER_RX (0x007B)

Enable DPC with guard time after RX

**Table 152. DPC_GUARD_TIME_AFTER_RX (0x007B)**

| Function | bit | Values | Description |
|---|---|---|---|
| Enable DPC guard time after RX | [7:0] | 0x00 | DPC disabled after RX (debug purpose only) |
| | | 0x01 | DPC enabled after RX (recommendation) |
| | | others | RFU |

### 9.18.2.3.13 DPC Lookup table entries

Table 153. DPC lookup table entries

| Entry | Address | Function | bit | Values | Description |
|---|---|---|---|---|---|
| ENTRY 0 for 1V5 | 0x7D | This below details are for entry 0. Similar is for all other entries. | | | |
| | | Target current reduction | [31:24] | - | Byte 0. Target current reduction in mA (unsigned) |
| | | AWC amp mod change | [23:16] | - | Byte 1. Relative change of modulated amplitude level (signed) |
| | | AWC edge time constant for ASK100 | [15:8] | - | Byte 2. Target current reduction in mA (unsigned) |
| | | | [15:12] | - | ASK100, Relative change of rising edge time constant (signed) |
| | | | [11:8] | - | ASK100, Relative change of falling edge time constant (signed) |
| | | AWC edge time constant for ASK100 | [7:0] | - | Byte 2. Target current reduction in mA (unsigned) |
| | | | [7:4] | - | ASK10, Relative change of rising edge time constant (signed) |
| | | | [3:0] | - | ASK10, Relative change of falling edge time constant (signed) |
| ENTRY_01 for 1.60V | 0x0081 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_02 for 1.70V | 0x0085 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_03 for 1.80V | 0x0089 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_04 for 1.90V | 0x008D | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_05 for 2.00V | 0x0091 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_06 for 2.10V | 0x0095 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_07 for 2.20V | 0x0099 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_08 for 2.30V | 0x009D | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_09 for 2.40V | 0x00A1 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_10 for 2.50V | 0x00A5 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_11 for 2.60V | 0x00A9 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_12 for 2.70V | 0x00AD | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_13 for 2.80V | 0x00B1 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_14 for 2.90V | 0x00B5 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_15 for 3.00V | 0x00B9 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_16 for 3.10V | 0x00BD | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_17 for 3.20V | 0x00C1 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_18 for 3.30V | 0x00C5 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_19 for 3.40V | 0x00C9 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_20 for 3.50V | 0x00CD | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_21 for 3.60V | 0x00D1 | Byte and bit-fields description, refer to Table 153 | | | |

**Table 153. DPC lookup table entries**...*continued*

| Entry | Address | Function | bit | Values | Description |
|-------|---------|----------|-----|--------|-------------|
| ENTRY_22 for 3.70V | 0x00D5 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_23 for 3.80V | 0x00D9 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_24 for 3.90V | 0x00DD | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_25 for 4.00V | 0x00E1 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_26 for 4.10V | 0x00E5 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_27 for 4.20V | 0x00E9 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_28 for 4.30V | 0x00ED | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_29 for 4.40V | 0x00F1 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_30 for 4.50V | 0x00F5 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_31 for 4.60V | 0x00F9 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_32 for 4.70V | 0x00FD | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_33 for 4.80V | 0x0101 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_34 for 4.90V | 0x0105 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_35 for 5.00V | 0x0109 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_36 for 5.10V | 0x010D | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_37 for 5.20V | 0x0111 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_38 for 5.30V | 0x0115 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_39 for 5.40V | 0x0119 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_40 for 5.50V | 0x011D | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_41 for 5.60V | 0x0121 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_42 for 5.70V | 0x0125 | Byte and bit-fields description, refer to Table 153 | | | |

#### 9.18.2.4 DPC EMVCo settings

This section provides the settings related to DPC configuration

##### 9.18.2.4.1 DPC_EMVCo_CONFIG (0x068E)

DPC EMVCo configuration

**Table 154. DPC_EMVCo_CONFIG (0x0077)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7:3] | | RFU |
| DPC in Active target mode | [2] | | DPC configuration in active target mode |
| | | `0x00` | disabled |
| | | `0x01` | enabled |
| DPC in Active initiator mode | [1] | | DPC configuration in active initiator mode |
| | | `0x00` | disabled |
| | | `0x01` | enabled |
| DPC in Reader/Passive Initiator mode | [0] | | DPC configuration in Reader/ Passive Initiator mode |
| | | `0x00` | disabled |
| | | `0x01` | enabled |

##### 9.18.2.4.2 DPC_EMVCo_TARGET_CURRENT (0x068F)

DPC configuration unloaded VDDPA target current in mA

**Table 155. DPC_EMVCo_TARGET_CURRENT (0x0132)**

| Function | bit | Values | Description |
|---|---|---|---|
| DPC in Active target mode | [15:0] | | VDDPA target current in mA. The target current +/- hysteresis defines the limiting maximum current for the DPC. |

Note: This configuration shall not exceed 350 mA - hysteresis.

Note: The resulting current that is driven by the transmitter can be further reduced based on the current reduction lookup table entries.

### 9.18.2.4.3  DPC_EMVCo_HYSTERESIS_LOADING (0x0691)

The hysteresis (**bHysteresis** and **bHysteresis_Unloading**) together with the target current (**wTargetCurrent**) defines the current limit, at which the DPC automatically decreases or raises the VDDPA. The VDDPA is automatically reduced, as soon as the current exceeds the **wTargetCurrent + bHysteresis**, and the VDDPA is automatically increased again, as soon as the current is below **wTargetCurrent # bHysteresis_Unloading**.

**Table 156.  DPC_EMVCo_HYSTERESIS_LOADING (0x006B)**

| Function | bit | Values | Description |
|---|---|---|---|
| DPC hysteresis loading | [7:0] | | Absolute difference to current Target Current in mA that triggers a DPC update event during loading. |

***Note:*** *If the hysteresis is configured too small, it might cause an oscillation of the transmitted field.*

***Note:*** *In most application, the default values work well and do not need to be modified.*

### 9.18.2.4.4  DPC_EMVCo_HYSTERESIS_UNLOADING (0x0694)

**Table 157.  DPC_EMVCo_HYSTERESIS_UNLOADING (0x006E)**

| Function | bit | Values | Description |
|---|---|---|---|
| DPC hysteresis unloading | [7:0] | | Absolute difference to current Target Current in mA that triggers a DPC update event during unloading. |

### 9.18.2.4.5  DPC_EMVCo_TXLDOVDDPALow (0x0695)

**Table 158.  DPC_EMVCo_TXLDOVDDPALow (0x006F)**

| Function | bit | Values | Description |
|---|---|---|---|
| TXLDOVDDPALow | [7:0] | | VDDPA Low Limit for RDON |

### 9.18.2.4.6  DPC_EMVCo_TXGSN (0x0696)

TXGSN configuration.

**Table 159.  DPC_EMVCo_TXGSN (0x0696)**

| Function | bit | Values | Description |
|---|---|---|---|
| DPC hysterisis loading | [7:0] | Less than 20 | resistance = 10 Ω / (tx1_gsn + 1) |
| | | more than or equal 20 | 20: resistance = 0.5 Ω |

### 9.18.2.4.7  DPC_EMVCo_RDON_CONTROL (0x0697)

**Table 160.  DPC_EMVCo_RDON_CONTROL (0x0697)**

| Function | bit | Values | Description |
|---|---|---|---|
| VDDPA low limit control | [7:0] | 0x00 | Disabled |
| | | 0x01 | RdON Control |
| | | 0x02 | PWM control |
| | | Others | RFU |

#### 9.18.2.4.8 DPC_EMVCo_InitialRDOn_RFOn (0x0698)

**Table 161. DPC_EMVCo_InitialRDOn_RFOn (0x0698)**

| Function | bit | Values | Description |
|---|---|---|---|
| DPC_InitialRDOn_RFOn | [7:0] | | Initial GSP TX1/TX2 value during FieldON |

#### 9.18.2.4.9 DPC_EMVCo_TXLDO_MAX_DROPOUT (0x099)

**Table 162. DPC_EMVCo_TXLDO_MAX_DROPOUT (0x0699)**

| Function | bit | Values | Description |
|---|---|---|---|
| DPC_TXLDO_MAX_DROPOUT | [15:0] | | At DPC start (on initial RF ON), if TXLDO drop out is higher to this value then VDDPA is reduced to: e VddpaSafe if no boost bypass on going else Vddpa is stopped. Unit is mV. Default = E10h = 3600 mV. |

#### 9.18.2.4.10 DPC_EMVCo_GUARD_TIME (0x09F)

**Table 163. DPC_EMVCo_GUARD_TIME (0x09F)**

| Function | bit | Values | Description |
|---|---|---|---|
| algointerval | [7:0] | | DPC guard time configuration. Guard time before tx. 1 unit = 1 μs. |

The DPC regulation is done once before TX and once after RX.

The guard time parameter is the time between DPC regulation completion and TX start.

The guard time parameter is the time between RX stop and DPC regulation start.

The guard time is always enabled for TX

*Note: The recommendation is not to modify the default value.*

#### 9.18.2.4.11 DPC_EMVCo_ENABLE_DURING_FDT (0x06A0)

DPC regulation enable during FDT.

**Table 164. DPC_EMVCo_ENABLE_DURING_FDT (0x06A0)**

| Function | bit | Values | Description |
|---|---|---|---|
| Disable DPC during FDT | [7:0] | 0x00 | DPC disabled during FDT (debug purpose only) |
| | | 0x01 | DPC enabled during FDT (recommendation) |
| | | others | RFU |

#### 9.18.2.4.12 DPC_EMVCo_GUARD_TIME_AFTER_RX (0x06A1)

Enable DPC with guard time after RX

**Table 165. DPC_EMVCo_GUARD_TIME_AFTER_RX (0x06A1)**

| Function | bit | Values | Description |
|---|---|---|---|
| Enable DPC guard time after RX | [7:0] | 0x00 | DPC disabled after RX (debug purpose only) |
| | | 0x01 | DPC enabled after RX (recommendation) |
| | | others | RFU |

### 9.18.2.4.13 DPC EMVCo Lookup table entries

**Table 166. DPC EMVCo lookup table entries**

| Entry | Address | Function | bit | Values | Description |
|---|---|---|---|---|---|
| ENTRY 0 for 1V5 | 0x7D | This below details are for entry 0. Similar is for all other entries. | | | |
| | | Target current reduction | [31:24] | - | Byte 0. Target current reduction in mA (unsigned) |
| | | AWC amp mod change | [23:16] | - | Byte 1. Relative change of modulated amplitude level (signed) |
| | | AWC edge time constant for ASK100 | [15:8] | - | Byte 2. Target current reduction in mA (unsigned) |
| | | | [15:12] | - | ASK100, Relative change of rising edge time constant (signed) |
| | | | [11:8] | - | ASK100, Relative change of falling edge time constant (signed) |
| | | AWC edge time constant for ASK100 | [7:0] | - | Byte 2. Target current reduction in mA (unsigned) |
| | | | [7:4] | - | ASK10, Relative change of rising edge time constant (signed) |
| | | | [3:0] | - | ASK10, Relative change of falling edge time constant (signed) |
| ENTRY_01 for 1.60V | 0x0081 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_02 for 1.70V | 0x0085 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_03 for 1.80V | 0x0089 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_04 for 1.90V | 0x008D | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_05 for 2.00V | 0x0091 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_06 for 2.10V | 0x0095 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_07 for 2.20V | 0x0099 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_08 for 2.30V | 0x009D | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_09 for 2.40V | 0x00A1 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_10 for 2.50V | 0x00A5 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_11 for 2.60V | 0x00A9 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_12 for 2.70V | 0x00AD | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_13 for 2.80V | 0x00B1 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_14 for 2.90V | 0x00B5 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_15 for 3.00V | 0x00B9 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_16 for 3.10V | 0x00BD | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_17 for 3.20V | 0x00C1 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_18 for 3.30V | 0x00C5 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_19 for 3.40V | 0x00C9 | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_20 for 3.50V | 0x00CD | Byte and bit-fields description, refer to Table 153 | | | |
| ENTRY_21 for 3.60V | 0x00D1 | Byte and bit-fields description, refer to Table 153 | | | |

**Table 166. DPC EMVCo lookup table entries***...continued*

| Entry | Address | Function | bit | Values | Description |
|-------|---------|----------|-----|--------|-------------|
| ENTRY_22 for 3.70V | `0x00D5` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_23 for 3.80V | `0x00D9` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_24 for 3.90V | `0x00DD` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_25 for 4.00V | `0x00E1` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_26 for 4.10V | `0x00E5` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_27 for 4.20V | `0x00E9` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_28 for 4.30V | `0x00ED` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_29 for 4.40V | `0x00F1` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_30 for 4.50V | `0x00F5` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_31 for 4.60V | `0x00F9` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_32 for 4.70V | `0x00FD` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_33 for 4.80V | `0x0101` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_34 for 4.90V | `0x0105` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_35 for 5.00V | `0x0109` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_36 for 5.10V | `0x010D` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_37 for 5.20V | `0x0111` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_38 for 5.30V | `0x0115` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_39 for 5.40V | `0x0119` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_40 for 5.50V | `0x011D` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_41 for 5.60V | `0x0121` | Byte and bit-fields description, refer to [Table 153](#) | | | |
| ENTRY_42 for 5.70V | `0x0125` | Byte and bit-fields description, refer to [Table 153](#) | | | |

### 9.18.2.5 ARC settings for passive reader modes

This section provides the ARC settings for Reader Mode TX wave shaping configuration

#### 9.18.2.5.1 ARC_SETTINGS_ARCCONFIG (0x0129)

ARC settings configuration.

**Table 167. ARC_SETTINGS_ARCCONFIG (0x0129)**

| Function | bit | Values | Description |
|---|---|---|---|
| ARC settings configuration | [7] | 0x00 | ARC algorithm is disabled. |
| | | 0x01 | ARC algorithm is enabled. |
| | [6:3] | | RFU |
| | [2:0] | | Number of entries in ARC table |
| | | 0x00 | one entry |
| | | 0x01 | two entries |
| | | 0x02 | three entries |
| | | 0x03 | four entries |
| | | 0x04 | five entries |
| | | others | RFU |

#### 9.18.2.5.2 ARC_SETTINGS_ARCVDDPA (0x012B)

VDDPA settings.

**Table 168. ARC_SETTINGS_ARCVDDPA (0x012B)**

| Function | byte | Values | Description |
|---|---|---|---|
| VDDPA settings | [4] | See below note | VDDPA range_index 4: if VDDPA voltage between VDDPA_3 to ARC_VDDPA_4 |
| | [3] | | VDDPA range_index 3: if VDDPA voltage between VDDPA_2 to ARC_VDDPA_3 - 0.1 |
| | [2] | | VDDPA_range_index 2: if VDDPA voltage between VDDPA_1 to ARC_VDDPA_2 - 0.1 |
| | [1] | | VDDPA_range_index 1: if VDDPA voltage between VDDPA_0 to (ARC_VDDPA_1 - 0.1) |
| | [0] | | VDDPA_range_index 0: if VDDPA voltage between 1.5 to (VDDPA_0 - 0.1) |

**Note:** *For above settings, value of 0x00 indicates for 1V50, 0x01 indicates for 1V60. Further increase with 100 mV and value of 0x2A corresponds to 5V70.*

### 9.18.2.5.3 ARC_SETTINGS_WRMARCA_106 (0x0130)

ARC table settings for reader mode Type A 106kbps

**Table 169. ARC_SETTINGS_WRMARCA_106 (0x0130)**

| Function | byte | bits | Values | Description |
|---|---|---|---|---|
| RM_RX_ARC_0 | [9:8] | [15] | | ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'. |
| | | | 0x00 | ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used. |
| | | | 0x01 | ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used. |
| | | [14] | | ARC enable/disable |
| | | | 0x00 | ARC disabled for this technology and baudrate |
| | | | 0x01 | ARC enabled for this technology and baudrate |
| | | [13:10] | | RFU |
| | | [9] | | Enable the IIR filter |
| | | [8:7] | | MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) |
| | | [6:0] | | DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| RM_RX_ARC_1 | [7:6] | [15] | | ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'. |
| | | | 0x00 | ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used. |
| | | | 0x01 | ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used. |
| | | [14] | | RFU |
| | | [13:10] | | RFU |
| | | [9] | | Enable the IIR filter |
| | | [8:7] | | MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) |
| | | [6:0] | | DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Table 169. ARC_SETTINGS_WRMARCA_106 (0x0130)**...*continued*

| Function | byte | bits | Values | Description |
|---|---|---|---|---|
| RM_RX_ARC_2 | [5:4] | [15] | | ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'. |
| | | | 0x00 | ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used. |
| | | | 0x01 | ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used. |
| | | [14] | | RFU |
| | | [13:10] | | RFU |
| | | [9] | | Enable the IIR filter |
| | | [8:7] | | MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) |
| | | [6:0] | | DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| RM_RX_ARC_3 | [3:2] | [15] | | ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'. |
| | | | 0x00 | ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used. |
| | | | 0x01 | ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used. |
| | | [14] | | RFU |
| | | [13:10] | | RFU |
| | | [9] | | Enable the IIR filter |
| | | [8:7] | | MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) |
| | | [6:0] | | DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Table 169.  ARC_SETTINGS_WRMARCA_106 (0x0130)**...*continued*

| Function | byte | bits | Values | Description |
|---|---|---|---|---|
| RM_RX_ARC_4 | [1:0] | [15] | | ARC settings applicability. Settings will be taken into account only if bit[14] of this settings is set to '1'. |
| | | | 0x00 | ARC settings applicable always. bits [9:0] of ARC_RM_A106 are used. |
| | | | 0x01 | ARC settings applicable during FDT. bits [9:0] of ARM_RM_A106_FDT are used else bits[9:0] of table ARC_RM_A106 are used. |
| | | [14] | | RFU |
| | | [13:10] | | RFU |
| | | [9] | | Enable the IIR filter |
| | | [8:7] | | MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) |
| | | [6:0] | | DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

### 9.18.2.5.4  ARC_SETTINGS_TABLE for other technologies

**Table 170.  ARC_SETTINGS_TABLE for other technologies**

| Technology | Address | Function | Byte | Description |
|---|---|---|---|---|
| ARC_SETTINGS_A_212 | 0x13A-0x143 | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_A_424 | 0x144-0x14D | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_A_848 | 0x14E-0x157 | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_B_106 | 0x158-0x161 | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |

**Table 170. ARC_SETTINGS_TABLE for other technologies**...*continued*

| Technology | Address | Function | Byte | Description |
|---|---|---|---|---|
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_B_212 | 0x162-0x16B | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_B_424 | 0x16C-0x175 | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_B_848 | 0x176-0x17F | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_F_424 | 0x180-0x189 | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_F_424 | 0x18A-0x193 | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_V_6P6 | 0x19E-0x1A7 | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_V_26 | 0x19E-0x1A7 | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |

**Table 170. ARC_SETTINGS_TABLE for other technologies**...*continued*

| Technology | Address | Function | Byte | Description |
|---|---|---|---|---|
| ARC_SETTINGS_V_53 | 0x1A8-0x1B1 | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_V_106 | 0x1B2-0x1BB | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_V_212 | 0x1BC-0x1C5 | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_RmArcEMVCoF212 | 0x1C6-1CF | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_RmArcEMVCoF424 | 0x1D0-1D9 | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_RmArcEMVCoA106 | 0x1DA-0x1E3 | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |
| ARC_SETTINGS_RmArcEMVCoB106 | 0x1E4-0x1ED | RM_RX_ARC_0 | [9:8] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_1 | [7:6] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_2 | [5:4] | Refer to Section 9.18.2.5.3 |
| | | RM_RX_ARC_3 | [3:2] | Refer to Section 9.18.2.5.3 |
| | 0x202-0x20B | RM_RX_ARC_4 | [1:0] | Refer to Section 9.18.2.5.3 |

### 9.18.2.5.5  ARC_RM_A106_FDT_NFC_FORUM (0x051B)

**Table 171. ARC_RM_A106_FDT_NFC_FORUM (0x051B)**

| Function | Address | Bytesn | Bits | Value | Description |
|---|---|---|---|---|---|
| RM_RX_ARC_FDT_0 | 0x51B | [1:0] | | | Settings for RM_RX_ARC_FDT_0 |
| | | | [15] | 0x00 | ARC settings apply always |
| | | | | 0x01 | ARC settings applicable during FDT |
| | | | [14] | 0x00 | ARC Disabled for this Tech and Baudrate |
| | | | | 0x01 | ARC Enabled for this Tech and Baudrate |
| | | | | NOTE | This bit is RFU for RM_RX_ARC_FDT_1, RM_RX_ARC_FDT_2, RM_RX_ARC_FDT_3, RM_RX_ARC_FDT_4. |
| | | | [13:10] | - | RFU. Reserved. |
| | | | [9] | - | Enable the IIR filter. |
| | | | [8:7] | - | MF_GAIN (ths value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) |
| | | | [6:0] | - | DPC_ SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| RM_RX_ARC_FDT_1 | 0x51D | [3:2] | | | Settings for RM_RX_ARC_FDT_1. Bit definitions is same as that of RM_RX_ARC_FDT_0 |
| RM_RX_ARC_FDT_2 | 0x51F | [5:4] | | | Settings for RM_RX_ARC_FDT_2. Bit definitions is same as that of RM_RX_ARC_FDT_0 |
| RM_RX_ARC_FDT_3 | 0x521 | [7:6] | | | Settings for RM_RX_ARC_FDT_3. Bit definitions is same as that of RM_RX_ARC_FDT_0 |
| RM_RX_ARC_FDT_4 | 0x523 | [9:8] | | | Settings for RM_RX_ARC_FDT_4. Bit definitions is same as that of RM_RX_ARC_FDT_0 |

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**Product data sheet**

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### 9.18.2.5.6 ARC_RM_A106_FDT_EMVCo (0x06A7)

**Table 172. ARC_RM_A106_FDT_EMVCo (0x06A7)**

| Function | Address | Bytesn | Bits | Value | Description |
|---|---|---|---|---|---|
| RM_RX_ARC_FDT_0 | 0x51B | [1:0] | Settings for RM_RX_ARC_FDT_0 | | |
| | | | [15] | 0x00 | ARC settings apply always |
| | | | | 0x01 | ARC settings applicable during FDT |
| | | | [14] | 0x00 | ARC Disabled for this Tech and Baudrate |
| | | | | 0x01 | ARC Enabled for this Tech and Baudrate |
| | | | | NOTE | This bit is RFU for RM_RX_ARC_FDT_1, RM_RX_ARC_FDT_2, RM_RX_ARC_FDT_3, RM_RX_ARC_FDT_4. |
| | | | [13:10] | - | RFU. Reserved. |
| | | | [9] | - | Enable the IIR filter. |
| | | | [8:7] | - | MF_GAIN (ths value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled) |
| | | | [6:0] | - | DPC_ SIGNAL_DETECT_TH_ OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| RM_RX_ARC_FDT_1 | 0x51D | [3:2] | Settings for RM_RX_ARC_FDT_1. Bit definitions is same as that of RM_RX_ARC_FDT_0 | | |
| RM_RX_ARC_FDT_2 | 0x51F | [5:4] | Settings for RM_RX_ARC_FDT_2. Bit definitions is same as that of RM_RX_ARC_FDT_0 | | |
| RM_RX_ARC_FDT_3 | 0x521 | [7:6] | Settings for RM_RX_ARC_FDT_3. Bit definitions is same as that of RM_RX_ARC_FDT_0 | | |
| RM_RX_ARC_FDT_4 | 0x523 | [9:8] | Settings for RM_RX_ARC_FDT_4. Bit definitions is same as that of RM_RX_ARC_FDT_0 | | |

### 9.18.2.6 RSSI configuration parameters (applicable for card emulation)

#### 9.18.2.6.1 EEPROM_APC_RSSI_LIST

List of RSSI settings for card emulation only

**Table 173. List of RSSI settings for card emulation only**

| Configuration Parameter | Address (Hex) | Address (Decimal) | Size (in bytes) | EEPROM_AREA |
|---|---|---|---|---|
| RSSI_TIMER (0x020C) | 0x020C | 524 | 2 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| RSSI_TIMER_FIRST_PERIOD (0x020E) | 0x020E | 526 | 2 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| RSSI_CTRL_00_AB (0x0210) | 0x0210 | 528 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| RSSI_NB_ENTRIES_AB (0x0211) | 0x0211 | 529 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| RSSI_THRESHOLD_AB entries table | 0x0212-0x271 | 530 | 2 | E_PN76_EEPROM_SECURE_LIB_CONFIG |

#### 9.18.2.6.2 RSSI_TIMER (0x020C)

RSSI timer

**Table 174. RSSI_TIMER (0x020C)**

| Function | bits | Values | Description |
|---|---|---|---|
| RSSI_TIMER | [15:0] | | RSSI timer. Default: 423d. |

#### 9.18.2.6.3 RSSI_TIMER_FIRST_PERIOD (0x020E)

First period duration after Rf field ON.

**Table 175. RSSI_TIMER_FIRST_PERIOD (0x020E)**

| Function | bits | Values | Description |
|---|---|---|---|
| RSSI | [15:0] | | First period duration after Rffield ON. Unit is 128/fc (106 kHz) if set to 0 it means feature is not used 0D2 => ~2 ms |

#### 9.18.2.6.4 RSSI_CTRL_00_AB (0x0210)

RSSI control.

**Table 176. RSSI_CTRL_00_AB (0x0210)**

| Function | bits | Values | Description |
|---|---|---|---|
| RSSI | [7:6] | - | Reserved |
| | [5:0] | - | (APC_ID_REF_AB) ID of APC_TX entry that is equiv to RSSI = 0 (for Type AB) |

### 9.18.2.6.5  RSSI_NB_ENTRIES_AB (0x0211)

For Initial RF ON, CEA and CEB.

**Table 177.  RSSI_NB_ENTRIES_AB (0x0211)**

| Function | bits | Values | Description |
|---|---|---|---|
| RSSI | [7:5] | | Reserved |
| | [4:0] | | Number of entries in RSSI look up table (it refers to RSSI_ENTRY_AB_01 to RSSI_ENTRY_AB_18); |

### 9.18.2.6.6  RSSI_THRESHOLD_PHASE_TABLE for Type-A and Type-B

**Table 178.  RSSI_THRESHOLD_PHASE_TABLE for Type-A and Type-B**

| Entry | Address | Function | bit | Values | Description |
|---|---|---|---|---|---|
| RSSI_THRESHOLD_AB_01 | 0x212 | RSSI | | | Threshold value for APC algorithm for TypeA and TypeB<br>***Note:*** *dwRssiEntryAB_00 = 0 (not in EEPROM) Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2)* |
| | | | [15:13] | - | Reserved |
| | | | [12:0] | - | RSSI Value |
| RSSI_PHASE_AB_01 | 0x214 | RSSI | [15:0] | - | Phase compensation value for APC algorithm for TypeA and TypeB.<br>Signed phase compensation with 1/4 degree resolution:16 bits signed value (using complement of 2) |
| RSSITHRESHOLDAB_02 | 0x0216 | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_02 | 0x0218 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_03 | 0x021A | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_03 | 0x021C | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_04 | 0x021E | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_04 | 0x0220 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_05 | 0x0222 | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_05 | 0x0224 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_06 | 0x0226 | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_06 | 0x0228 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_07 | 0x022A | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_07 | 0x022C | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_08 | 0x022E | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_08 | 0x0230 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_09 | 0x0232 | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_09 | 0x0234 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_0A | 0x0236 | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_0A | 0x0238 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |

**Table 178. RSSI_THRESHOLD_PHASE_TABLE for Type-A and Type-B**...*continued*

| Entry | Address | Function | bit | Values | Description |
|---|---|---|---|---|---|
| RSSITHRESHOLDAB_0B | 0x023A | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_0B | 0x023C | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_0C | 0x023E | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_0C | 0x0240 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_0D | 0x0242 | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_0D | 0x0244 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_0E | 0x0246 | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_0E | 0x0248 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_0F | 0x024A | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_0F | 0x024C | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_10 | 0x024E | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_10 | 0x0250 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_11 | 0x0252 | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_11 | 0x0254 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_12 | 0x0256 | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_12 | 0x0258 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_13 | 0x025A | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_13 | 0x025C | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_14 | 0x025E | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_14 | 0x0260 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_15 | 0x0262 | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_15 | 0x0264 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_16 | 0x0266 | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_16 | 0x0268 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_17 | 0x026A | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_17 | 0x026C | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |
| RSSITHRESHOLDAB_18 | 0x026E | Refer to the entry RSSI_THRESHOLD_AB_01 for bit-fields and description. | | | |
| ARBPHASEAB_18 | 0x0270 | Refer to the entry RSSI_PHASE_AB_01 for bit-fields and description. | | | |

### 9.18.2.6.7 RSSI_CTRL_00_F (0x0272)

**Table 179. RSSI_CTRL_00_F (0x0272)**

| Function | bits | Values | Description |
|---|---|---|---|
| RSSI | [7:6] | | Reserved |
| | [5:0] | | (APC_ID_REF_AB) ID of APC_TX entry that is equiv to RSSI = 0 (for Type F) |

### 9.18.2.6.8  RSSI_NB_ENTRIES_F (0x0273)

**Table 180.  RSSI_NB_ENTRIES_F (0x0273)**

| Function | bits | Values | Description |
|---|---|---|---|
| RSSI | [7:5] | | Reserved |
| | [4:0] | | Number of entries in RSSI look up table (it refers to RSSI_ENTRY_F_01 to RSSI_ENTRY_F_18); |

### 9.18.2.6.9  RSSI_THRESHOLD_PHASE_TABLE for Type-F

**Table 181.  RSSI_THRESHOLD_PHASE_TABLE for Type-F**

| Entry | Address | Function | bit | Values | Description |
|---|---|---|---|---|---|
| RSSI_THRESHOLD_F_01 | 0x276 | RSSI | Threshold value for APC algorithm for TypeF | | |
| | | | **Note:**  dwRssiEntryF_00 = 0 (not in EEPROM) Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2) | | |
| | | | [15:13] | - | Reserved |
| | | | [12:0] | - | RSSI Value |
| RSSI_PHASE_F_01 | 0x276 | RSSI | [15:0] | - | Phase compensation value for APC algorithm for TypeF. Signed phase compensation with 1/4 degree resolution:16 bits signed value (using complement of 2) |
| RSSITHRESHOLDF_02 | 0x0278 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_02 | 0x027A | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_03 | 0x027C | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_03 | 0x027E | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_04 | 0x0280 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_04 | 0x0282 | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_05 | 0x0284 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_05 | 0x0286 | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_06 | 0x0288 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_06 | 0x028A | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_07 | 0x028C | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_07 | 0x028E | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_08 | 0x0290 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_08 | 0x0292 | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_09 | 0x0294 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_09 | 0x0296 | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_0A | 0x0298 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_0A | 0x029A | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_0B | 0x029C | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_0B | 0x029E | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |

**Table 181. RSSI_THRESHOLD_PHASE_TABLE for Type-F**...*continued*

| Entry | Address | Function | bit | Values | Description |
|---|---|---|---|---|---|
| RSSITHRESHOLDF_0C | 0x02A0 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_0C | 0x02A2 | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_0D | 0x02A4 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_0D | 0x02A6 | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_0E | 0x02A8 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_0E | 0x02AA | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_0F | 0x02AC | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_0F | 0x02AE | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_10 | 0x02B0 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_10 | 0x02B2 | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_11 | 0x02B4 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_11 | 0x02B6 | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_12 | 0x02B8 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_12 | 0x02BA | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_13 | 0x02BC | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_13 | 0x02BE | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_14 | 0x02C0 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_14 | 0x02C2 | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_15 | 0x02C4 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_15 | 0x02C6 | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_16 | 0x02C8 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_16 | 0x02CA | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_17 | 0x02CC | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_17 | 0x02CE | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |
| RSSITHRESHOLDF_18 | 0x02D0 | Refer to the entry RSSI_THRESHOLD_F_01 for bit-fields and description. | | | |
| ARBPHASEF_18 | 0x02D2 | Refer to the entry RSSI_PHASE_F_01 for bit-fields and description. | | | |

### 9.18.2.7 RSSI APC algorithm table output settings TX_PARAM_ENTRY_TABLE. Applicable only for card emulation.

APC TX_PARAM_ENTRY for ID.

**Table 182. TX_PARAM_ENTRY_00_ID (0x02D4)**

| Entry ID | Address | Function | bits | Values | Description |
|---|---|---|---|---|---|
| ENTRY_00_ID | 0x2D4 | Driver count | [7] | - | Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT): |
| | | | | 0x00 | Dual driver |
| | | | | 0x01 | Single driver |
| | | BPSK mode | [6] | - | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE): |
| | | | | 0x00 | Dual driver |
| | | | | 0x01 | Single driver |
| | | ID | [5:0] | - | ID |
| ENTRY_00_Tx1 | 0x2D5 | RFU | [7:6] | - | Reserved |
| | | PMU VDDPA setting | [5:0] | - | VDDPA(V) = (val × 10) + 1,5 V 0x00 = 1.50 V ... 0x2Ah = 5.70 V |
| ENTRY_00_Tx2 | 0x2D6 | Scaling factor | [7:0] | - | Scaling factor for TX1 and TX2 |
| ENTRY_01_ID | 0x02D7 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_01_TX1 | 0x02D8 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_01_TX2 | 0x02D9 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_02_ID | 0x02DA | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_02_TX1 | 0x02DB | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_02_TX2 | 0x02DC | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_03_ID | 0x02DD | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_03_TX1 | 0x02DE | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_03_TX2 | 0x02DF | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_04_ID | 0x02E0 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_04_TX1 | 0x02E1 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_04_TX2 | 0x02E2 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_05_ID | 0x02E3 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_05_TX1 | 0x02E4 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_05_TX2 | 0x02E5 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_06_ID | 0x02E6 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_06_TX1 | 0x02E7 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_06_TX2 | 0x02E8 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_07_ID | 0x02E9 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_07_TX1 | 0x02EA | For bit-field values, refer to ENTRY_00_TX1 above | | | |

**Table 182.  TX_PARAM_ENTRY_00_ID (0x02D4)**...*continued*

| Entry ID | Address | Function | bits | Values | Description |
|---|---|---|---|---|---|
| ENTRY_07_TX2 | 0x02EB | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_08_ID | 0x02EC | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_08_TX1 | 0x02ED | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_08_TX2 | 0x02EE | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_09_ID | 0x02EF | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_09_TX1 | 0x02F0 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_09_TX2 | 0x02F1 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_0A_ID | 0x02F2 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_0A_TX1 | 0x02F3 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_0A_TX2 | 0x02F4 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_0B_ID | 0x02F5 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_0B_TX1 | 0x02F6 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_0B_TX2 | 0x02F7 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_0C_ID | 0x02F8 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_0C_TX1 | 0x02F9 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_0C_TX2 | 0x02FA | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_0D_ID | 0x02FB | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_0D_TX1 | 0x02FC | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_0D_TX2 | 0x02FD | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_0E_ID | 0x02FE | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_0E_TX1 | 0x02FF | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_0E_TX2 | 0x0300 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_0F_ID | 0x0301 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_0F_TX1 | 0x0302 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_0F_TX2 | 0x0303 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_10_ID | 0x0304 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_10_TX1 | 0x0305 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_10_TX2 | 0x0306 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_11_ID | 0x0307 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_11_TX1 | 0x0308 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_11_TX2 | 0x0309 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_12_ID | 0x030A | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_12_TX1 | 0x030B | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_12_TX2 | 0x030C | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_13_ID | 0x030D | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_13_TX1 | 0x030E | For bit-field values, refer to ENTRY_00_TX1 above | | | |

**Table 182. TX_PARAM_ENTRY_00_ID (0x02D4)***...continued*

| Entry ID | Address | Function | bits | Values | Description |
|---|---|---|---|---|---|
| ENTRY_13_TX2 | 0x030F | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_14_ID | 0x0310 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_14_TX1 | 0x0311 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_14_TX2 | 0x0312 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_15_ID | 0x0313 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_15_TX1 | 0x0314 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_15_TX2 | 0x0315 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_16_ID | 0x0316 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_16_TX1 | 0x0317 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_16_TX2 | 0x0318 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_17_ID | 0x0319 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_17_TX1 | 0x031A | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_17_TX2 | 0x031B | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_18_ID | 0x031C | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_18_TX1 | 0x031D | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_18_TX2 | 0x031E | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_19_ID | 0x031F | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_19_TX1 | 0x0320 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_19_TX2 | 0x0321 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_1A_ID | 0x0322 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_1A_TX1 | 0x0323 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_1A_TX2 | 0x0324 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_1B_ID | 0x0325 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_1B_TX1 | 0x0326 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_1B_TX2 | 0x0327 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_1C_ID | 0x0328 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_1C_TX1 | 0x0329 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_1C_TX2 | 0x032A | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_1D_ID | 0x032B | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_1D_TX1 | 0x032C | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_1D_TX2 | 0x032D | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_1E_ID | 0x032E | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_1E_TX1 | 0x032F | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_1E_TX2 | 0x0330 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_1F_ID | 0x0331 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_1F_TX1 | 0x0332 | For bit-field values, refer to ENTRY_00_TX1 above | | | |

**Table 182.  TX_PARAM_ENTRY_00_ID (0x02D4)**...*continued*

| Entry ID | Address | Function | bits | Values | Description |
|---|---|---|---|---|---|
| ENTRY_1F_TX2 | 0x0333 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_20_ID | 0x0334 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_20_TX1 | 0x0335 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_20_TX2 | 0x0336 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_21_ID | 0x0337 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_21_TX1 | 0x0338 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_21_TX2 | 0x0339 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_22_ID | 0x033A | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_22_TX1 | 0x033B | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_22_TX2 | 0x033C | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_23_ID | 0x033D | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_23_TX1 | 0x033E | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_23_TX2 | 0x033F | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_24_ID | 0x0340 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_24_TX1 | 0x0341 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_24_TX2 | 0x0342 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_25_ID | 0x0343 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_25_TX1 | 0x0344 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_25_TX2 | 0x0345 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_26_ID | 0x0346 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_26_TX1 | 0x0347 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_26_TX2 | 0x0348 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_27_ID | 0x0349 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_27_TX1 | 0x034A | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_27_TX2 | 0x034B | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_28_ID | 0x034C | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_28_TX1 | 0x034D | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_28_TX2 | 0x034E | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_29_ID | 0x034F | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_29_TX1 | 0x0350 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_29_TX2 | 0x0351 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_2A_ID | 0x0352 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_2A_TX1 | 0x0353 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_2A_TX2 | 0x0354 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_2B_ID | 0x0355 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_2B_TX1 | 0x0356 | For bit-field values, refer to ENTRY_00_TX1 above | | | |

**Table 182.  TX_PARAM_ENTRY_00_ID (0x02D4)**...*continued*

| Entry ID | Address | Function | bits | Values | Description |
|---|---|---|---|---|---|
| ENTRY_2B_TX2 | 0x0357 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_2C_ID | 0x0358 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_2C_TX1 | 0x0359 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_2C_TX2 | 0x035A | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_2D_ID | 0x035B | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_2D_TX1 | 0x035C | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_2D_TX2 | 0x035D | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_2E_ID | 0x035E | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_2E_TX1 | 0x035F | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_2E_TX2 | 0x0360 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_2F_ID | 0x0361 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_2F_TX1 | 0x0362 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_2F_TX2 | 0x0363 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_30_ID | 0x0364 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_30_TX1 | 0x0365 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_30_TX2 | 0x0366 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_31_ID | 0x0367 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_31_TX1 | 0x0368 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_31_TX2 | 0x0369 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_32_ID | 0x036A | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_32_TX1 | 0x036B | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_32_TX2 | 0x036C | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_33_ID | 0x036D | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_33_TX1 | 0x036E | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_33_TX2 | 0x036F | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_34_ID | 0x0370 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_34_TX1 | 0x0371 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_34_TX2 | 0x0372 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_35_ID | 0x0373 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_35_TX1 | 0x0374 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_35_TX2 | 0x0375 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_36_ID | 0x0376 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_36_TX1 | 0x0377 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_36_TX2 | 0x0378 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_37_ID | 0x0379 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_37_TX1 | 0x037A | For bit-field values, refer to ENTRY_00_TX1 above | | | |

**Table 182. TX_PARAM_ENTRY_00_ID (0x02D4)**...*continued*

| Entry ID | Address | Function | bits | Values | Description |
|---|---|---|---|---|---|
| ENTRY_37_TX2 | 0x037B | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_38_ID | 0x037C | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_38_TX1 | 0x037D | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_38_TX2 | 0x037E | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_39_ID | 0x037F | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_39_TX1 | 0x0380 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_39_TX2 | 0x0381 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_3A_ID | 0x0382 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_3A_TX1 | 0x0383 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_3A_TX2 | 0x0384 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_3B_ID | 0x0385 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_3B_TX1 | 0x0386 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_3B_TX2 | 0x0387 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_3C_ID | 0x0388 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_3C_TX1 | 0x0389 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_3C_TX2 | 0x038A | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_3D_ID | 0x038B | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_3D_TX1 | 0x038C | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_3D_TX2 | 0x038D | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_3E_ID | 0x038E | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_3E_TX1 | 0x038F | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_3E_TX2 | 0x0390 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_3F_ID | 0x0391 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_3F_TX1 | 0x0392 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_3F_TX2 | 0x0393 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_40_ID | 0x0394 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_40_TX1 | 0x0395 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_40_TX2 | 0x0396 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_41_ID | 0x0397 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_41_TX1 | 0x0398 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_41_TX2 | 0x0399 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_42_ID | 0x039A | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_42_TX1 | 0x039B | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_42_TX2 | 0x039C | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_43_ID | 0x039D | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_43_TX1 | 0x039E | For bit-field values, refer to ENTRY_00_TX1 above | | | |

**Table 182. TX_PARAM_ENTRY_00_ID (0x02D4)**...*continued*

| Entry ID | Address | Function | bits | Values | Description |
|---|---|---|---|---|---|
| ENTRY_43_TX2 | 0x039F | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_44_ID | 0x03A0 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_44_TX1 | 0x03A1 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_44_TX2 | 0x03A2 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_45_ID | 0x03A3 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_45_TX1 | 0x03A4 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_45_TX2 | 0x03A5 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_46_ID | 0x03A6 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_46_TX1 | 0x03A7 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_46_TX2 | 0x03A8 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_47_ID | 0x03A9 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_47_TX1 | 0x03AA | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_47_TX2 | 0x03AB | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_48_ID | 0x03AC | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_48_TX1 | 0x03AD | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_48_TX2 | 0x03AE | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_49_ID | 0x03AF | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_49_TX1 | 0x03B0 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_49_TX2 | 0x03B1 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_4A_ID | 0x03B2 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_4A_TX1 | 0x03B3 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_4A_TX2 | 0x03B4 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_4B_ID | 0x03B5 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_4B_TX1 | 0x03B6 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_4B_TX2 | 0x03B7 | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_4C_ID | 0x03B8 | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_4C_TX1 | 0x03B9 | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_4C_TX2 | 0x03BA | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_4D_ID | 0x03BB | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_4D_TX1 | 0x03BC | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_4D_TX2 | 0x03BD | For bit-field values, refer to ENTRY_00_TX2 above | | | |
| ENTRY_4E_ID | 0x03BE | For bit-field values, refer to ENTRY_00_ID above | | | |
| ENTRY_4E_TX1 | 0x03BF | For bit-field values, refer to ENTRY_00_TX1 above | | | |
| ENTRY_4E_TX2 | 0x03C0 | For bit-field values, refer to ENTRY_00_TX2 above | | | |

### 9.18.2.8 Autocol configuration settings

#### 9.18.2.8.1 List of Autocoll configuration settings

List of Autocoll configuration settings

**Table 183. List of Autocoll configuration settings**

| Configuration Parameter | Address (Hex) | Address (Decimal) | Size (in bytes) | EEPROM_AREA |
|---|---|---|---|---|
| RF_DEBOUNCE_TIMEOUT (0x03C4) | 0x03C4 | 964 | 1 | EEPROM_SECURE_LIB_CONFIG |
| SENSE_RES (0x03C5) | 0x03C5 | 965 | 2 | EEPROM_SECURE_LIB_CONFIG |
| NFC_ID1 (0x03C7) | 0x03C7 | 967 | 3 | EEPROM_SECURE_LIB_CONFIG |
| SEL_RES (0x03CA) | 0x03CA | 970 | 1 | EEPROM_SECURE_LIB_CONFIG |
| FELICA_POLLRES (0x03CB) | 0x03CB | 971 | 18 | EEPROM_SECURE_LIB_CONFIG |
| RANDOM_UID_ENABLE (0x03 DD) | 0x03DD | 989 | 1 | EEPROM_SECURE_LIB_CONFIG |

#### 9.18.2.8.2 RF_DEBOUNCE_TIMEOUT (0x03C4)

Debounce timeout

**Table 184. RF_DEBOUNCE_TIMEOUT (0x03C4)**

| Function | bits | Values | Description |
|---|---|---|---|
| DEBOUNCE_TIMEOUT | [7:0] | - | Timeout used after the RF detection during the AUTOCOLL to detect if there is a glitch or continuous RF. Value is entered in 1 µs. |

#### 9.18.2.8.3 SENSE_RES (0x03C5)

Response to ReqA / ATQA in order byte 0, byte 1.

**Table 185. SENSE_RES (0x03C5)**

| Function | bits | Values | Description |
|---|---|---|---|
| Response to ReqA / ATQA | [15:0] | | ATQA in order byte 0, byte 1 |
| | [15:8] | | Byte1 value |
| | [7:0] | | Byte0 value |

### 9.18.2.8.4 NFC_ID1 (0x03C7)

Response to ReqA / ATQA in order byte 0, byte 1

**Table 186. NFC_ID1 (0x03C7)**

| Function | bits | Values | Description |
|---|---|---|---|
| UID address generation | [31:0] | | If Random UID is disabled (EEPROM address 0x2CB), the content of these addresses is used to generate a Fixed UID. The order is byte 0, Byte 1, Byte 2; Byte3 - which is the first NFCID1 byte - is fixed to 08h, the check byte is calculated automatically. |
| | [31:24] | 0x08 | Byte3 value |
| | [23:16] | | Byte2 value |
| | [15:8] | | Byte1 value |
| | [7:0] | | Byte0 value |

### 9.18.2.8.5 SEL_RES (0x03CA)

Response to Select : SAK.

**Table 187. SEL_RES (0x03CA)**

| Function | bits | Values | Description |
|---|---|---|---|
| Response to Select | [7:0] | | Response to Select : SAK |

### 9.18.2.8.6 FELICA_POLLRES (0x03CB)

Response to Select : SAK

**Table 188. FELICA_POLLRES (0x03CB)**

| Function | byte | bits | Values | Description |
|---|---|---|---|---|
| Felica Poll response | [1:0] | [15:0] | 0x01FE | FeliCa polling response. Shall be the same value. |
| | [7:2] | [47:0] | | FeliCa polling response. NFCID2 (6 bytes). |
| | [15:8] | [63:0] | | FeliCa polling response. PAD (8 bytes). |
| | [17:16] | [15:0] | | FeliCa polling response. System code (2 bytes). |

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#### 9.18.2.8.7 RANDOM_UID_ENABLE (0x03DD)

Random UID enable

**Table 189. RANDOM_UID_ENABLE (0x03DD)**

| Function | bits | Values | Description |
|---|---|---|---|
| Random UID enable | [7:1] | | Reserved |
| | [0] | 0x00 | Use UID stored in EEPROM |
| | | 0x01 | Randomly generate the UID in which the first byte is fixed and the remaining 3 bytes are random A new random number is generated after each RF-OFF to RF-ON. |

### 9.18.2.9 LPCD related configuration parameters

#### 9.18.2.9.1 EEPROM_LPCD_SETTINGS_LIST

List of LPCD related configuration settings

**Table 190. List of LPCD related configuration settings**

| Configuration Parameter | Address (Hex) | Address (Decimal) | Size (in bytes) | EEPROM_AREA |
|---|---|---|---|---|
| LPCD_AVG_SAMPLES (0x03DE) | 0x03DE | 990 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| LPCD_RSSI_TARGET (0x03E0) | 0x03E0 | 992 | 2 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| LPCD_RSSI_HYST (0x03E2) | 0x03E2 | 994 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| LPCD_CONFIG (0x03E3) | 0x03E3 | 995 | 2 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| LPCD_THRESHOLD (0x03E6) | 0x03E6 | 998 | 4 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| LPCD_WAIT_RX_SETTLE (0x03F7) | 0x03F7 | 1015 | 2 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| LPCD_VDDPA (0x03FB) | 0x03FB | 1019 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| LPCD_CHECK_PERIOD (0x03FC) | 0x03FC | 1020 | 2 | E_PN76_EEPROM_SECURE_LIB_CONFIG |

### 9.18.2.9.2 LPCD_AVG_SAMPLES (0x03DE)

Number of samples used for averaging

**Table 191. LPCD_AVG_SAMPLES (0x03DE)**

| Function | bits | Values | Description |
|---|---|---|---|
| Random UID enable | [7:3] | | Reserved |
| LPCD_AVG_SAMPLES | [2:0] | | Defines how many samples of the I and Q values are used for the averaging. Average samples in power of 2. |
| | | 0x00 | 1 sample |
| | | 0x01 | 2 samples |
| | | 0x02 | 4 samples |
| | | 0x03 | 8 samples |
| | | 0x04 | 16 samples |
| | | 0x05 | 32 samples |
| | | 0x06 | 64 samples |
| | | 0x07 | RFU |

### 9.18.2.9.3 LPCD_RSSI_TARGET (0x03E0)

**Table 192. LPCD_RSSI_TARGET (0x03E0)**

| Function | bits | Values | Description |
|---|---|---|---|
| LPCD_RSSI_TARGET | [15:0] | | Value to be set in register DGRM_RSSI_REG_ DGRM_RSSI_TARGET. Typically the same values from the Type A106 LOAD_RF_CONFIGURATION API (DGRM_RSSI register) are used. |

### 9.18.2.9.4 LPCD_RSSI_HYST (0x03E2)

**Table 193. LPCD_RSSI_HYST (0x03E2)**

| Function | bits | Values | Description |
|---|---|---|---|
| LPCD_RSSI_HYST | [7:0] | | Value to be set in CLIF_DGRM_RSSI_REG_ DGRM_RSSI_HYST Typically the same values from the Type A106 LOAD_RF_CONFIGURATION API (DGRM_RSSI register) are used. |

### 9.18.2.9.5 LPCD_CONFIG (0x03E3)

Number of samples used for averaging

**Table 194. LPCD_CONFIG (0x03E3)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [15:8] | | Reserved |
| Enable LPCD | [7] | 0x00 | Enable (1) / Disable (0) the LPCD |
| RFU | [6] | | Reserved |
| RF OFF before TXLDO shutdown | [5] | 0x00 | Disables feature Immediate RF OFF before TXLDO shutdown to save power |
| | | 0x01 | Enables feature Immediate RF OFF before TXLDO shutdown to save power. For this feature, Enable VDDPA fast discharge must be enabled. |
| RFU | [4:0] | | Reserved |

### 9.18.2.9.6 LPCD_THRESHOLD (0x03E6)

LPCD threshold type depends upon the LPCD_CONFIG[2:0] value in Table 194

For 'I and Q' mode: $1^{st}$ threshold = I ch; $2^{nd}$ threshold = Q ch.

**Table 195. LPCD_THRESHOLD (0x03E6)**

| Function | bits | Values | Description |
|---|---|---|---|
| LPCD Q channel threshold | [31:16] | | ADC LSB granularity of threshold depends of avg_samples_meas value: |
| | | 0x00 | unit 1 |
| | | 0x01 | unit 1/2 |
| | | 0x02 | unit 1/4 |
| | | 0x03 | unit 1/8 |
| | | 0x04 | unit 1/16 |
| | | 0x05 | unit 1/32 |
| | | Other | Reserved |
| LPCD I channel threshold | [15:0] | - | ADC LSB granularity of threshold depends of avg_samples_meas value: |
| | | 0x00 | unit 1 |
| | | 0x01 | unit 1/2 |
| | | 0x02 | unit 1/4 |
| | | 0x03 | unit 1/8 |
| | | 0x04 | unit 1/16 |
| | | 0x05 | unit 1/32 |
| | | Other | Reserved |

**Note:** *If the difference between the measured value and the reference is greater than the threshold on either channels, then a card is detected.*

### 9.18.2.9.7 LPCD_WAIT_RX_SETTLE (0x03F7)

Delay between FieldOn and starting ADC data averaging.

**Table 196. LPCD_WAIT_RX_SETTLE (0x03F7)**

| Function | bits | Values | Description |
|---|---|---|---|
| LPCD DELAY | [15:0] | | Delay between FieldOn and starting ADC data averaging. Value in us, default 14h = 20 µs |

### 9.18.2.9.8 LPCD_VDDPA (0x03FB)

VDDPA voltage when DCDC (internal or external) or external power source is used to feed TXLDO.

**Table 197. LPCD_VDDPA (0x03FB)**

| Function | bits | Values | Description |
|---|---|---|---|
| VDDPA voltage LPCD DELAY | [7:0] | | TXLDO output voltage. |
| | | 0x00-0x2A | resultant voltage would be: 1V50 + this value × 0.1 V) |
| | | Others | Reserved |

### 9.18.2.9.9 WAIT_RX_SETTLE (0x03FC)

Timer value defining standby duration before calibration and reference measurement in LPCD single mode(Mode 4)

**Table 198. WAIT_RX_SETTLE (0x03FC)**

| Function | bits | Values | Description |
|---|---|---|---|
| LPCD DELAY | [15:0] | - | 2.63ms resolution, default 0x26 = ~100 ms |

### 9.18.2.10  CORRECTION_ENTRY_TABLE

**Table 199.  CORRECTION_ENTRY_TABLE**

| Entry | Address | Function | bit | Values | Description |
|---|---|---|---|---|---|
| CORRECTION_ENTRY 0 for 1V5 | 0x042B | PROP_CORRECTION_ ENTRY | [15:8] | | Correction applied for ASK10 Range would be -128 to +127. |
| | | | [7:0] | | Correction applied for ASK100. Range would be -128 to +127. |
| CORRECTION_ENTRY1 for 1.60V | 0x042D | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY2 for 1.70V | 0x042F | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY3 for 1.80V | 0x0431 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY4 for 1.90V | 0x0433 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY5 for 2.00V | 0x0435 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY6 for 2.10V | 0x0437 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY7 for 2.20V | 0x0439 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY8 for 2.30V | 0x043B | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY9 for 2.40V | 0x043D | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY10 for 2.50V | 0x043F | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY11 for 2.60V | 0x0441 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY12 for 2.70V | 0x0443 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY13 for 2.80V | 0x0445 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY14 for 2.90V | 0x0447 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY15 for 3.00V | 0x0449 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY16 for 3.10V | 0x044B | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY17 for 3.20V | 0x044D | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY18 for 3.30V | 0x044F | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY19 for 3.40V | 0x0451 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |

**Table 199. CORRECTION_ENTRY_TABLE**...*continued*

| Entry | Address | Function | bit | Values | Description |
|---|---|---|---|---|---|
| CORRECTION_ENTRY20 for 3.50V | 0x0453 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY21 for 3.60V | 0x0455 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY22 for 3.70V | 0x0457 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY23 for 3.80V | 0x0459 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY24 for 3.90V | 0x045B | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY25 for 4.00V | 0x045D | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY26 for 4.10V | 0x045F | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY27 for 4.20V | 0x0461 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY28 for 4.30V | 0x0463 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY29 for 4.40V | 0x0465 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY30 for 4.50V | 0x0467 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY31 for 4.60V | 0x0469 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY32 for 4.70V | 0x046B | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY33 for 4.80V | 0x046D | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY34 for 4.90V | 0x046F | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY35 for 5.00V | 0x0471 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY36 for 5.10V | 0x0473 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY37 for 5.20V | 0x0475 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY38 for 5.30V | 0x0477 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY39 for 5.40V | 0x0479 | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY40 for 5.50V | 0x047B | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |
| CORRECTION_ENTRY41 for 5.60V | 0x047D | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |

**Table 199. CORRECTION_ENTRY_TABLE**...*continued*

| Entry | Address | Function | bit | Values | Description |
|---|---|---|---|---|---|
| CORRECTION_ENTRY42 for 5.70V | `0x047F` | Byte and bit-fields description, refer to CORRECTION_ENTRY 0 | | | |

### 9.18.2.11 TX_SHAPING_RTRANS_FTRANS_TABLE TX wave shaping for proprietary correction configuration for rising edge and falling edges. (0x0481)

#### 9.18.2.11.1 TX_SHAPING_RTRANS_FTRANS_1 (0x0481)

The rising Transition register values loaded when Proprietary TX Shaping configuration is set in the RM_TECHNO_TX_SHAPING table to use proprietary TX shaping.

**Table 200. TX_SHAPING_RTRANS_FTRANS_1 (0x0481)**

| Function | Address | Bytes | Bits | Description |
|---|---|---|---|---|
| RTRANS0 | 0x0481 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| RTRANS1 | 0x0485 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| RTRANS2 | 0x0489 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| RTRANS3 | 0x048D | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| FTRANS0 | 0x0491 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| FTRANS1 | 0x0495 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| FTRANS2 | 0x0499 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| FTRANS3 | 0x049D | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |

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#### 9.18.2.11.2 TX_SHAPING_RTRANS_FTRANS_2 (0x4A1)

The rising Transition register values loaded when Proprietary TX Shaping configuration is set in the RM_TECHNO_TX_SHAPING table to use proprietary TX shaping.

**Table 201. TX_SHAPING_RTRANS_FTRANS_2 (0x4A1)**

| Function | Address | Bytes | Bits | Description |
|---|---|---|---|---|
| RTRANS0 | 0x4A1 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| RTRANS1 | 0x04A5 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| RTRANS2 | 0x04A9 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| RTRANS3 | 0x04AD | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| FTRANS0 | 0x04B1 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| FTRANS1 | 0x04B5 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| FTRANS2 | 0x04B9 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| FTRANS3 | 0x04BD | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |

#### 9.18.2.11.3 TX_SHAPING_RTRANS_FTRANS_3 (0x04C1)

The rising Transition register values loaded when Proprietary TX Shaping configuration is set in the RM_TECHNO_TX_SHAPING table to use proprietary TX shaping.

**Table 202. TX_SHAPING_RTRANS_FTRANS_3 (0x04C1)**

| Function | Address | Bytes | Bits | Description |
|---|---|---|---|---|
| RTRANS0 | 0x04C1 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| RTRANS1 | 0x04C5 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| RTRANS2 | 0x04C9 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| RTRANS3 | 0x04CD | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| FTRANS0 | 0x04D1 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| FTRANS1 | 0x04D5 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| FTRANS2 | 0x04D9 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| FTRANS3 | 0x04DD | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |

#### 9.18.2.11.4 TX_SHAPING_RTRANS_FTRANS_1 (0x04E1)

The rising Transition register values loaded when Proprietary TX Shaping configuration is set in the RM_TECHNO_TX_SHAPING table to use proprietary TX shaping.

**Table 203.  TX_SHAPING_RTRANS_FTRANS_1 (0x04E1)**

| Function | Address | Bytes | Bits | Description |
|---|---|---|---|---|
| RTRANS0 | 0x04E1 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| RTRANS1 | 0x04E5 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| RTRANS2 | 0x04E9 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| RTRANS3 | 0x04ED | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| FTRANS0 | 0x04F1 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| FTRANS1 | 0x04F5 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| FTRANS2 | 0x04F9 | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| FTRANS3 | 0x04FD | [3:0] | [31:0] | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |

### 9.18.2.12  TX driver NOV (non-overlap) settings configuration.

#### 9.18.2.12.1  EEPROM_TX_DRIVER_NOV_LIST

List of NOV configuration parameters

**Table 204.  List of NOV configuration parameters**

| Configuration Parameter | Address (Hex) | Address (Decimal) | Size (in bytes) | EEPROM_AREA |
|---|---|---|---|---|
| NOV_CFG_CAL (0x0501) | 0x0501 | 1281 | 1 | EEPROM_SECURE_LIB_CONFIG |
| NOV_CAL_VAL1 (0x0502) | 0x0502 | 1282 | 1 | EEPROM_SECURE_LIB_CONFIG |
| NOV_CAL_VAL2 (0x0503) | 0x0503 | 1283 | 1 | EEPROM_SECURE_LIB_CONFIG |
| NOV_CAL_THRESHOLD (0x0504) | 0x0504 | 1284 | 1 | EEPROM_SECURE_LIB_CONFIG |
| NOV_CAL_OFFSET1 (0x0505) | 0x0505 | 1285 | 4 | EEPROM_SECURE_LIB_CONFIG |
| NOV_CAL_OFFSET2 (0x0509) | 0x0509 | 1289 | 4 | EEPROM_SECURE_LIB_CONFIG |

### 9.18.2.12.2 NOV_CFG_CAL (0x0501)

NOV calibration type

**Table 205. NOV_CFG_CAL (0x0501)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7:2] | - | Reserved |
| NOV_CALIBRATION_TYPE | [1:0] | 0x00 | No calibration performed, needs to be updated to 01 or 10 before the first RF on of the chip is performed. |
| | | 0x01 | Enable FW calibration after every cold boot. |
| | | 0x02 | Use calibration value coming from EEPROM NOV_CAL_VAL1, NOV_CAL_VAL2 (Default) |
| | | 0x03 | RFU |

### 9.18.2.12.3 NOV_CAL_VAL1 (0x0502)

**Table 206. NOV_CAL_VAL1 (0x0502)**

| Function | bits | Values | Description |
|---|---|---|---|
| VDDPACALVAL1 | [7:0] | 0x03 | (1.8 V) |
| | | 0x0D | (2.8 V) |

### 9.18.2.12.4 NOV_CAL_VAL2 (0x0503)

**Table 207. NOV_CAL_VAL2 (0x0503)**

| Function | bits | Values | Description |
|---|---|---|---|
| VDDPACALVAL2 | [7:0] | 0x15 | (3.6 V) |
| | | 0x24 | (5.1 V) |

### 9.18.2.12.5 NOV_CAL_THRESHOLD (0x0504)

**Table 208. NOV_CAL_THRESHOLD (0x0504)**

| Function | bits | Values | Description |
|---|---|---|---|
| VDDPACALVAL2 | [7:0] | 0x08 | (2.3 V) |
| | | 0x16 | (3.7 V) |

### 9.18.2.12.6 NOV_CAL_OFFSET1 (0x0505)

**Table 209. NOV_CAL_OFFSET1 (0x0505)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [31:29] | | Reserved |
| VDDAPA MIN | [28:24] | | Group#1 (VDDPA min to CfgThreshold), offset_2l(1) |
| | [23:21] | | Reserved |
| | [20:16] | | Group#1 (VDDPA min to CfgThreshold), offset_2l(0) |
| | [15:13] | | Reserved |
| | [12:08] | | Group#1 (VDDPA min to CfgThreshold), offset_3l_p2 |
| | [07:05] | | Reserved |
| | [04:00] | | Group#1 (VDDPA min to CfgThreshold), offset_3l |

### 9.18.2.12.7 NOV_CAL_OFFSET2 (0x0509)

**Table 210. NOV_CAL_OFFSET2 (0x0509)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [31:29] | | Reserved |
| VDDAPA MAX | [28:24] | | Group#1 (VDDPA max to CfgThreshold), offset_2l(1) |
| | [23:21] | | Reserved |
| | [20:16] | | Group#1 (VDDPA max to CfgThreshold), offset_2l(0) |
| | [15:13] | | Reserved |
| | [12:08] | | Group#1 (VDDPA max to CfgThreshold), offset_3l_p2 |
| | [07:05] | | Reserved |
| | [04:00] | | Group#1 (VDDPA max to CfgThreshold), offset_3l |

### 9.18.2.13 Active reader mode TX wave shaping configuration

This section provides the active reader mode TX wave shaping configuration settings.

### 9.18.2.13.1 RESIDUAL_AMPL_LEVEL_ACTIVE_A106 (0X050E)

**Table 211. RESIDUAL_AMPL_LEVEL_ACTIVE_A106 (0X050E)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.13.2 EDGE_TYPE_ACTIVE_A106 (0X050F)

**Table 212. EDGE_TYPE_ACTIVE_A106 (0X050F)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

### 9.18.2.13.3 EDGE_STYLE_ACTIVE_A106 (0X0510)

**Table 213. EDGE_STYLE_ACTIVE_A106 (0X0510)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_A106 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ A106 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_A106 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_ A106 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.13.4 EDGE_LENGTH_ACTIVE_A106 (0X0511)

**Table 214. EDGE_LENGTH_ACTIVE_A106 (0X0511)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) | |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.13.5 RESIDUAL_AMPL_LEVEL_ACTIVE_F212 (0X0512)

**Table 215. RESIDUAL_AMPL_LEVEL_ACTIVE_F212 (0X0512)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.13.6 EDGE_TYPE_ACTIVE_F212 (0X0513)

**Table 216. EDGE_TYPE_ACTIVE_F212 (0X0513)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition style | [7:4] | | Defines style of edge transition of falling edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |
| | [3:0] | | Definition of edge transition style of rising edge, Defines style of edge transition: |
| | | Firmware based shaping | |
| | | `0x01` | linear transition between two amplitude levels |
| | | `0x02` | two linear transitions between amplitude levels |
| | | `0x03` | three linear transitions between amplitude levels |
| | | `Others` | RFU |
| | | Lookup table based shaping | |
| | | `0x04` | lookup table-based transition, no automatic adaptation based on VDDPA |
| | | `0x05` | lookup table-based transition, automatic adaptation based on VDDPA including Correction |
| | | `0x06` | lookup table-based transition, automatic adaptation based on VDDPA but no Correction |
| | | `Others` | RFU |

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### 9.18.2.13.7 EDGE_STYLE_ACTIVE_F212 (0X0514)

**Table 217. EDGE_STYLE_ACTIVE_F212 (0X0514)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [7] | RFU | |
| Edge style configuration falling edge | [6:4] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_F212 is 1, 2, or 3: time constant configuration of falling edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_F212 is 4, 5, or 6: This number is the lookup table which shall be used of falling edge (0,1,2,3) |
| RFU | [3] | | RFU |
| Edge style configuration rising edge | [2:0] | Defines edge style configuration | |
| | | | For Firmware based shaping ( bEdgeType_F212 is 1, 2, or 3: time constant configuration of rising edge (depends on edge style) |
| | | | For lookup table based shaping ( bEdgeType_F212 is 4, 5, or 6: This number is the lookup table which shall be used of rising edge (0,1,2,3) |

### 9.18.2.13.8 EDGE_LENGTH_ACTIVE_F212 (0X0515)

**Table 218. EDGE_LENGTH_ACTIVE_F212 (0X0515)**

| Function | bit | Values | Description |
|---|---|---|---|
| Edge transition length | [7] | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time) | |
| | | 0x00 | disabled (1 transition state = one carrier cycle) |
| | | 0x01 | enabled (1 transition state = two carrier cycles) |
| | [6:5] | | RFU |
| | [4:0] | | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time) |

### 9.18.2.13.9 RESIDUAL_AMPL_LEVEL_ACTIVE_F424 (0X0516)

**Table 219. RESIDUAL_AMPL_LEVEL_ACTIVE_F424 (0X0516)**

| Function | bit | Values | Description |
|---|---|---|---|
| Residual amplitude level | [7:0] | 0x00 | 0 % carrier |
| | | 0xFF | 100 % carrier |

### 9.18.2.14 Global TX_SHAPING configuration

This section provides configuration global TX waveform shaping settings.

#### 9.18.2.14.1 EEPROM_RM_GLOBAL_TX_SHAPING_LIST

List of Settings related TX_SHAPING configuration.

**Table 220. List of Settings related TX_SHAPING configuration.**

| Configuration Parameter | Address (Hex) | Address (Decimal) | Size (in bytes) | EEPROM_AREA |
|---|---|---|---|---|
| TX_SHAPING_CONIFG (0x058C) | 0x058C | 1420 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| TX_INV_RM (0x058D) | 0x058D | 1421 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| TX_CLK_MODE_1 (0x058E) | 0x058E | 1422 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| TX_CLK_MODE_2 (0x058F) | 0x058F | 1423 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| GSN_MOD_RM (0x0590) | 0x0590 | 1424 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| GSN_CW_RM (0x0591) | 0x0591 | 1425 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| GSP_RM (0x0592) | 0x0592 | 1426 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| TX_FRCZERO_THR (0x0593) | 0x0593 | 1427 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| SIGNAL_SCALING_CONFIG (0x0594) | 0x0594 | 1428 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| TX_PH_SHIFT_DIV10 (0x0595) | 0x0595 | 1429 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |
| TX_PH_SHIFT_MOD10 (0x0596) | 0x0596 | 1430 | 1 | E_PN76_EEPROM_SECURE_LIB_CONFIG |

#### 9.18.2.14.2 TX_SHAPING_CONIFG (0x058C)

PWM scheme for RM

**Table 221. TX_SHAPING_CONIFG (0x058C)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7:1] | | Reserved |
| PWM scheme for RM | [0] | 0x00 | defining 3-levels for drivers TX1/2 - required for balanced antenna (default) |
| | | 0x01 | defining 2-levels for drivers TX1/2 - required for single ended antenna |

### 9.18.2.14.3  TX_INV_RM (0x058D)

Transmitter configuration

**Table 222.  TX_INV_RM (0x058D)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7:6] | | Reserved |
| TX1 output configuration | [5] | 0x00 | TX1 non-inverted output (output zero remains zero) |
| | | 0x01 | TX1 inverted output (common mode operation, output zero becomes one) |
| TX2 output configuration | [4] | 0x00 | TX2 non-inverted output (output zero remains zero) |
| | | 0x01 | TX2 inverted output (common mode operation, output zero becomes one) |
| RFU | [3:2] | | Reserved |
| TX1 phase shift configuration | [1] | 0x00 | TX1 no phase shift, 0 deg |
| | | 0x01 | TX1 phase shifted by 180 deg |
| TX2 phase shift configuration | [0] | 0x00 | TX2 no phase shift, 0 deg |
| | | 0x01 | TX2 phase shifted by 180 deg |

### 9.18.2.14.4  TX_CLK_MODE_1 (0x058E)

Transmitter configuration

**Table 223.  TX_CLK_MODE_1 (0x058E)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7] | | Reserved |
| CLK_MODE_CW_RM | [6:4] | | CLK_MODE_CW_RM |
| RFU | [3] | | Reserved |
| CLK_MODE_MOD_RM | [2:0] | | CLK_MODE_MOD_RM |

### 9.18.2.14.5  TX_CLK_MODE_2 (0x058F)

CLK_MODE configuration

**Table 224.  TX_CLK_MODE_2 (0x058F)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7] | | Reserved |
| CLK_MODE_DEFAULT | [6:4] | | CLK_MODE_DEFAULT |
| RFU | [3] | | Reserved |
| CLK_MODE_TRANS_RM | [2:0] | | CLK_MODE_TRANS_RM |

### 9.18.2.14.6 GSN_MOD_RM (0x0590)

GSN_MOD_RM configuration

**Table 225. GSN_MOD_RM (0x0590)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7:5] | | Reserved |
| GSN_MOD_RM | [4:0] | | GSN_MOD_RM |

### 9.18.2.14.7 GSN_CW_RM (0x0591)

GSN_CW_RM configuration

**Table 226. GSN_CW_RM (0x0591)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7:5] | | Reserved |
| GSN_CW_RM | [4:0] | | GSN_CW_RM |

### 9.18.2.14.8 GSP_RM (0x0592)

GSP_RM configuration

**Table 227. GSP_RM (0x0592)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7:5] | | Reserved |
| GSP_RM | [4:0] | | GSP_RM |

### 9.18.2.14.9 TX_FRCZERO_THR (0x0593)

CLIF_SS_TX_CFG_REG configuration

**Table 228. TX_FRCZERO_THR (0x0593)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7] | | Reserved |
| CLIF_SS_TX_CFG_REG | [6:0] | | Defining CLIF_SS_TX_CFG_REG[12:6] |

### 9.18.2.14.10 SIGNAL_SCALING_CONFIG (0x0594)

Global TX_SS_TARGET_SCALE configuration

**Table 229. SIGNAL_SCALING_CONFIG (0x0594)**

| Function | bits | Values | Description |
|---|---|---|---|
| Global TX_SS_TARGET_SCALE | [7:0] | | Global TX_SS_TARGET_SCALE configuration for debugging purposes |

### 9.18.2.14.11  TX_PH_SHIFT_DIV10 (0x0595)

Global TX_SS_TARGET_SCALE configuration

**Table 230.  TX_PH_SHIFT_DIV10 (0x0595)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7:5] | | Reserved |
| CLIF_ANACTRL_TX_CONFIG_ REG | [4:0] | | CLIF_ANACTRL_TX_CONFIG_REG.TX_PH_ SHIFT_DIV10 |

### 9.18.2.14.12  TX_PH_SHIFT_MOD10 (0x0596)

Global CLIF_ANACTRL_TX_CONFIG_REG.TX_PH_SHIFT_MOD10 configuration

**Table 231.  TX_PH_SHIFT_MOD10 (0x0596)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7:4] | | Reserved |
| CLIF_ANACTRL_TX_CONFIG_ REG.TX_PH_SHIFT_MOD10 | [3:0] | | CLIF_ANACTRL_TX_CONFIG_REG.TX_PH_ SHIFT_MOD10 |

## 9.18.2.15  RFLD and NFCLD settings

### 9.18.2.15.1  EEPROM_RFLD_NFCLD_SETTINGS_LIST

List of settings related to RFLD and NFCLD

**Table 232.  List of settings related to RFLD and NFCLD**

| Configuration Parameter | Address (Hex) | Address (Decimal) | Size (in bytes) | EEPROM_AREA |
|---|---|---|---|---|
| NFCLD_RFLD_VALID (0x05 C5) | 0x05C5 | 1477 | 1 | EEPROM_SECURE_LIB_CONFIG |

### 9.18.2.15.2  NFCLD_RFLD_VALID (0x05C5)

**Table 233.  NFCLD_RFLD_VALID (0x05C5)**

| Function | bits | Values | Description |
|---|---|---|---|
| RFU | [7:1] | | Resreved. |
| NFCLD_RFLD_VALID | [0:0] | | If this bit is set to 1 then the NFCLD Threshold and RFLD Threshold is a valid data and calibration wont be done gain till this bit is cleared and POR is issued. |

### 9.18.2.16  TEMPERATURE related settings

This section provides the configuration of Temperature warning settings.

#### 9.18.2.16.1  EEPROM_TEMP_WARNING_LIST

List of settings for Temperature related cut-offs and notifications

**Table 234.  List of settings for Temperature related cut-offs and notifications**

| Configuration Parameter | Address (Hex) | Address (Decimal) | Size (in bytes) | EEPROM_AREA |
|---|---|---|---|---|
| TEMP_WARNING (0x0648) | 0x0648 | 1608 | 1 | EEPROM_SECURE_LIB_CONFIG |

#### 9.18.2.16.2  TEMP_WARNING (0x0648)

**Table 235.  TEMP_WARNING (0x0648)**

| Function | bits | Values | Description |
|---|---|---|---|
| PMU high threshold | [7:6] | 0x00 | Disabled |
| | | 0x01 | 114 °C |
| | | 0x02 | 125 °C |
| | | 0x03 | 130 °C |
| PMU low threshold | [5:4] | 0x00 | Disabled |
| | | 0x01 | 114 °C |
| | | 0x02 | 125 °C |
| | | 0x03 | 130 °C |
| CLIF high threshold | [3:2] | 0x00 | Disabled |
| | | 0x01 | 114 °C |
| | | 0x02 | 125 °C |
| | | 0x03 | 130 °C |
| CLIF low threshold | [1:0] | 0x00 | Disabled |
| | | 0x01 | 114 °C |
| | | 0x02 | 125 °C |
| | | 0x03 | 130 °C |

### 9.18.2.17 TESTBUS configuration settings

This section provides the configuration of Testbus related settings.

#### 9.18.2.17.1 DigitalTBSignalIndex (06A3h)

Test bus number to be configured. Selected from the list of exposed test buses described in the user manual.

**Table 236. DigitalTBSignalIndex (address 06A3h) EEPROM configuration bit description**

| Address (hex) | Function | Bit | Description |
|---|---|---|---|
| 6A3 | TB signal index | 7:0 | Digital signal test bus number from table "CTS and test bus signals" in the user manual<br>Valid data as described in table, all others: RFU |

#### 9.18.2.17.2 DigitalTBSignalBit (06A4h)

Test bus bit number to be configured. Selected from the list of exposed test buses described in the user manual.

**Table 237. DigitalTBSignalBit (address 06A4h) EEPROM configuration bit description**

| Address (hex) | Function | Bit | Description |
|---|---|---|---|
| 6A4 | TB signal bit | 7:0 | Digital signal test bus bit number from table "CTS and test bus signals" in the user manual<br>Valid data as described in table, all others: RFU |

#### 9.18.2.17.3 AnalogTBSignalIndex (06A5h)

Analog test bus to be configured. Selected from the list of exposed test buses described in the user manual.

**Table 238. AnalogTBSignalIndex (address 06A5h) EEPROM configuration bit description**

| Address (hex) | Function | Bit | Description |
|---|---|---|---|
| 6A5 | | 7:0 | Analog signal test bus number:<br>0x78 - obs_clif_tbcontrol_patchbox0<br>0x79 - obs_clif_tbcontrol_patchbox1<br>0x7A - obs_clif_tbcontrol_patchbox2<br>0x7B - obs_clif_tbcontrol_patchbox3<br>all others: RFU |

#### 9.18.2.18  Contact interface configuration settings

This section provides the configuration of the contact interface settings.

##### 9.18.2.18.1  CT_PROFILE_CONFIG (0x06B1)

Parameter to configure the Mode of CT interface profile

**Table 239.  CT_PROFILE_CONFIG (0x06B1)**

| Function | bit | Values | Description |
|---|---|---|---|
| | 15:8 | | 0x20: Slot 1<br>0x21: Slot 2<br>0x22: Slot 3<br>Other values => RFU |
| | 7:0 | | 0x00 => ISO Mode<br>0x01 => EMVCo Mode<br>0x02-0xFF => RFU |

##### 9.18.2.18.2  CT_CHIPSELECT_CONFIG (0x06B3)

Parameter to configure the number of CT slots:

**Table 240.  CT_CHIPSELECT_CONFIG (0x06B3)**

| Function | bit | Values | Description |
|---|---|---|---|
| RFU | [23:16] | | Byte 3 (LSB) value : RFU<br>0x01 => Default |
| Number of CT Slots Enabled | [15:8] | | 0x03 => Slot1, Slot2 & Slot3 enabled (all 3 CT slots enabled)<br>0x02 => Slot1 & Slot2 Enabled (2 CT slots enabled)<br>0x01 => Slot1 Enabled (only 1 CT slot enabled)<br>0x04-0xFF => RFU |
| RFU | [7:0] | | 1 (MSB) value : RFU<br>Default : 0xFF |

# 10  Limiting values

**Table 241.  Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD(VUP\_TX)}$ | supply voltage on pin VUP_TX | - | -0.3 | 6.3 | V |
| $V_{DD(VBAT)}$ | supply voltage on pin VBAT | - | -0.3 | 5.8 | V |
| $V_{DD(VDDIO)}$ | supply voltage on pin VDDIO | on pin VDDIO, power supply for host interface and GPIOs | -0.3 | 3.8 | V |
| $V_{DD(GPIO\_x)}$ | input voltage on pin used as GPIO | - | -0.3 | 3.8 | V |
| $V_{DD(VDDPA)}$ | supply voltage on pin VDDPA | maximum limiting values for $I_{DD(VDDPA)}$ and $T_{j(max)}$ not violated | - | 6.0 | V |
| $V_{i(RXP)}$ | input voltage on pin RXP | - | -0.3 | 2 | V |
| $V_{i(RXN)}$ | input voltage on pin RXN | - | -0.3 | 2 | V |
| $V_{ESD}$ | electrostatic discharge voltage | human body model (HBM)[1] | -2000 | 2000 | V |
| | | charge device model (CDM)[2] | -500 | 500 | V |
| $T_{j(max)}$ | junction temperature | - | - | 125 | °C |
| $T_{stg}$ | storage temperature | no supply voltage applied | -55 | 150 | °C |

[1]    According to ANSI/ESDA/JEDEC JS-001
[2]    According to ANSI/ESDA/JEDEC JS-002

Stress above one or more of the limiting values may cause permanent damage to the device or limit the lifetime.

Product might not behave according to specification.

# 11 Characteristics

This chapter describes the electrical characteristics for the usage of the product.

Functionality according to this specification and compliancy to referred standards is guaranteed if the device is operated within the limits.

For further information, refer to the PQP (product qualification package) which summarizes the results of the characterization and qualification performed.

## 11.1 Static characteristics

Table 242. Supply voltage

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD(VBAT\_PWR)}$ | supply voltage on pin VBAT_PWR (DC-DC input pin) | DC-DC disabled | 2.4 | - | 5.5 | V |
| | | DC-DC enabled | 2.8 | - | 4.8 | V |
| $V_{DD(VUP\_TX)}$ | supply voltage on pin VUP_TX (TX_LDO input pin) | Remark: If DC-DC is used, its output $V_{DD(BOOST)}$ Min is limited to 3.1 V | 2.4 | - | 6 | V |
| $V_{DD(VDDPA)}$ | supply voltage on pin VDDPA (input of the transmitter power amplifier) | - | 1.5 | - | 5.7 | V |
| $V_{DD(VDDPA)}$ | supply voltage on pin VDDPA | | 2.4 | - | 4.7 | V |
| $V_{DD(VBAT)}$ | supply voltage on pin VBAT (analog and digital supply) | VBAT >= VDDIO | 2.4 | - | 5.5 | V |
| $V_{DD(VDDIO)}$ | supply voltage on pin VDDIO (supply for host interface and GPIOs) | typical 1.8 V interface supply voltage | 1.62 | - | 1.98 | V |
| | | typical 3.3 V interface supply voltage | 2.4 | - | 3.6 | V |
| $V_{I(RXP)}$ | input voltage on pin RXP | - | -0.5 | - | 1.8 | V |
| $V_{I(RXN)}$ | input voltage on pin RXN | - | -0.5 | - | 1.8 | V |

*Note:* *The voltage on pin VDDIO must always be smaller or equal to the voltage on pin VBAT.*

Table 243. Current consumption in active mode

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(VBAT)}$ | system supply | | - | - | 20 | mA |
| $I_{DD(VDDIO)}$ | | This current depends on the output current of peripherals. At no time, the sum of the maximum output currents shall exceed $I_{DD(VDDIO)}$ max | - | - | 30 | mA |
| $I_{DD(BOOST\_IN)}$ | DC-DC boost supply | average input current | - | - | 1.0 | A |
| | | peak input current (short peak) | - | - | 1.7 | A |

**Table 243. Current consumption in active mode**...*continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(VUP\_TX)}$ | input supply for transmitter LDO | - | - | - | 350 | mA |
| $I_{DD(VDDPA)}$ | RF power amplifier (transmitter) current | supplied via VUP_TX (TX_LDO active) | - | - | 350 | mA |
| | | supplied without DC-DC and without TXLDO active | - | - | 400 | mA |

**Table 244. Current consumption during power-saving modes**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{OFF\ Plus\ Mode}$ (VDDIO+VBAT) | sum of supply current on pin VDDIO and VBAT in OFF Plus mode | 25 °C ambient operating temperature | - | 5 | - | µA |
| $I_{hard\ power\ down}$ (VDDIO+VBAT) | sum of supply current on pin VDDIO and VBAT in hard Power-down mode | 25 °C ambient operating temperature | - | 40 | 105 | µA |
| $I_{standby}$ (VDDIO +VBAT) | sum of supply current on pin VDDIO and VBAT in Standby mode | 25 °C ambient operating temperature | - | 45 | 110 | µA |
| $I_{suspend}$ (VBAT) | supply current on pin VBAT in suspend mode | 25 °C ambient operating temperature | - | 2.5 | - | mA |
| $I_{LPCD}$ (VDDIO+VBAT) | sum of supply current on pin VDDIO and VBAT in LPCD (Enhanced Low-Power Card Detection with highest sensitivity) mode, without DC-DC used | 25 °C ambient operating temperature, VBAT supply voltage 3.6 V, antenna matching 50 R, 3x RF-on per second | - | 250 | - | µA |

**Table 245. Overcurrent detection function**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(VUP\_TX)}$ | current of overcurrent detection becoming active | - | 450 | 550 | 650 | mA |

The Overcurrent detection function is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

**Table 246. VEN pin**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH-level input voltage | $V_{DD(VDDIO)} <= V_{DD(VBAT)}$ | $0.7 \times V_{DD(VDDIO)}$ | - | $V_{DD(VDDIO)}$ | V |
| $V_{IL}$ | LOW-level input voltage | | 0 | - | $0.3 \times V_{DD(VDDIO)}$ | V |
| $I_{IH}$ | HIGH-level input current | $V_I = V_{DD(VBAT)}$ | - | - | 1 | µA |
| $I_{IL}$ | LOW-level input current | $V_I = 0$ V | -1 | - | - | µA |

**Table 246. VEN pin** *...continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $C_i$ | input capacitance | | - | 5 | - | pF |

**Table 247. CLK1, CLK2 pins**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $V_{i(p-p)}$ | peak-to-peak input voltage | - | 0.4 | - | 1.65 | V |
| $I_{IH}$ | HIGH-level input current | VI= 1.65 V, no power saving, active mode | - | - | 5 | µA |
| $I_{IL}$ | LOW-level input current | VI = 0 V, no power saving, active mode | - | - | 1 | µA |
| δ | duty cycle | - | 35 | - | 65 | % |
| $C_{i(CLK1)}$ | input capacitance on pin CLK1 | VDD = 1.8 V, VDC = 0.65 V, VAC = 0.9 V (p-p) | - | 1 | - | pF |
| $C_{i(CLK2)}$ | input capacitance on pin CLK2 | VDD = 1.8 V, VDC = 0.65 V, VAC = 0.9 V (p-p) | - | 1 | - | pF |

**Table 248. IRQ1 pin**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ < 3 mA | $V_{DD(VDDIO)}$ -0.4 | - | $V_{DD(VDDIO)}$ | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ < 3 mA | 0 | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | | - | - | 3 | mA |
| $I_{OL}$ | LOW-level output current | | - | - | 3 | mA |
| $C_L$ | load capacitance | | - | - | 10 | pF |
| $t_f$ | fall time | $C_L$ = 12 pF max | 1 | - | 3 | ns |
| $t_r$ | rise time | $C_L$ = 12 pF max | 1 | - | 3 | ns |
| $R_{pd}$ | pull-down resistance | | 40 | - | 62 | kΩ |

**Table 249. SPI SCK / I2C1_SCL, SPI NSS / I2C Adr Bit 0 , SPI COTI / I2C Adr Bit 1 pins**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $V_{IH}$ | HIGH-level input voltage | | 0.65 × $V_{DD(VDDIO)}$ | - | $V_{DD(VDDIO)}$ | V |
| $V_{IL}$ | LOW-level input voltage | | - 0.5 | - | 0.35 × $V_{DD(VDDIO)}$ | V |
| $I_{IH}$ | HIGH-level input current | $V_I$ = $V_{VDDIO}$ | - | - | 1 | µA |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0 V | - | - | 1 | µA |
| $C_i$ | input capacitance | | - | 5 | - | pF |

**Table 250.  I2C1_ SDA pin**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH-level output voltage | $I_{OH} < 3$ mA | $V_{DD(VDDIO)}$ - 0.4 | - | $V_{DD(VDDIO)}$ | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL} < 3$ mA | 0 | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | | - | - | 3 | mA |
| $I_{OL}$ | LOW-level output current | | - | - | 3 | mA |
| $C_L$ | load capacitance | | - | - | 10 | pF |
| $t_f$ | fall time | $C_L = 12$ pF max | 1 | - | 3 | ns |
| $t_r$ | rise time | $C_L = 12$ pF max | 1 | - | 3 | ns |

**Table 251.  Mode selection, HOST_IF_SEL0, HOST_IF_SEL1, I2C2_IRQ, WAKEUP pins**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH-level input voltage | $V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6 | 0.65 × VDDIO | - | VDDIO + 0.5 V | V |
| $V_{IL}$ | LOW-level input voltage | $V_{DD(VDDIO)}$<= $V_{DD(VBAT)}$; 1.62 <= VDDIO <= 1.98 or 2.4 <= VDDIO <= 3.6 | - 0.5 | - | 0.35 × VDDIO | V |
| $V_{OH}$ | HIGH-level output voltage | $V_{DD(VDDIO)} = 3.3$ V | VDDIO - 0.4 | - | VDDIO | V |
| $V_{OH}$ | LOW-level output voltage | $V_{DD(VDDIO)} = 3.3$ V | 0 | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | $V_{DD(VDDIO)} = 3.3$ V | - | - | 3 | mA |
| $I_{OL}$ | LOW-level output current | $V_{DD(VDDIO)} = 3.3$ V | - | - | 3 | mA |
| $I_{IH}$ | HIGH-level input current | $V_{DD(VDDIO)} = 3.3$ V | - | - | 1 | µA |
| $I_{IL}$ | LOW-level input current | $V_{DD(VDDIO)} = 3.3$ V | - | - | 1 | µA |
| $R_{PU}$ | Weak pullup resistor | - | 40 | 50 | 62 | kΩ |
| $R_{PD}$ | Weak pulldown resistor | - | 40 | 50 | 62 | kΩ |

**Table 252.  RXp, RXn pins**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{i(dyn)}$ | dynamic input voltage | | - | - | 1.8 | V |
| $C_i$ | input capacitance | | - | 1 | - | pF |
| $Z_i$ | input impedance from RXN, RXP pins to VMID | Reader, card, and P2P modes | - | - | 15 | kΩ |

**Table 253. TX1, TX2 pins**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH-level output voltage | $V_{DD(VDDPA)}$ = 5 V; with internal VDDPA LDO | - | $V_{DD(VDDPA)}$ -150 mV | $V_{DD(VDDPA)}$ | V |
| $V_{OL}$ | LOW-level output voltage | $V_{DD(VDDPA)}$ = 5 V;with internal VDDPA LDO | 0 | 200 | - | mV |

**Table 254. AUX1, AUX2, AUX3 pins (Debug output)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{AUX\_OH}$ | HIGH-level output voltage | pin used as debug signal output | VDDIO - 0.4 | - | VDDIO | V |
| $V_{AUX\_OL}$ | LOW-level output voltage | pin used as debug signal output | 0 | - | 0.4 | mV |
| $I_{AUX\_OH}$ | HIGH-level output current | $V_{DD(VDDIO)}$ = 3.3 V | - | - | 3 | mA |
| $I_{AUX\_OL}$ | LOW-level output current | $V_{DD(VDDIO)}$ = 3.3 V | - | - | 3 | mA |
| $C_{O\_LOAD}$ | output capacitance load of pin | | - | 5 | 10 | pF |

## 11.2 Timing characteristics

**Table 255. Power supply connection timing**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{rise\_vbat}$ | VBAT supply ramp | VEN = Low | 0 | - | 2.75 | V/µs |
| $t_{vbat\_vddio}$ | time between ramping up VBAT and ramping VDDIO | vddio condition: VBAT>2.4 V, VDDIO supply (External), hpd_off_sel = x | 0 | 500 | 1000 | ms |
| $t_{vbat\_ven}$ | time between ramping VBAT and VEN | vddio condition: VBAT>2.4 V, VDDIO supply (External), hpd_off_sel = x | 0 | 500.5 | - | ms |
| $t_{boot}$ | start-up time[1] | vddio condition: VBAT>2.4 V, VDDIO supply (External), hpd_off_sel = x | 3.2 | 3.27 | dependent on configuration of XTAL_CHECK_DELAY (0013h) in EEPROM. This configuration can be used to optimize the boot time for crystals which allow a fast settling. This allows to optimize the average current consumption during LPCD. | ms |

[1] (PN7220 ready to receive commands on the host interface). For LPCD, the PN7220 indicates the ability to receive commands from a host by raising an IDLE IRQ.

**Table 256. Pulse length**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{(VEN)}$ | on Pin VEN, pulse width to reset the chip or exit from Hard power down State | - | 5 | - | - | ms |

**Table 257. I$^2$C timing specification: Standard, Fast Mode**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | Load capacitance < 400 pF | 0 | - | 0.4 | MHz |
| $t_{SU}$ START | Set-up time for a (repeated) START condition | Load capacitance < 400 pF | 600 | - | - | ns |
| $t_{HD}$ START | hold time of a (repeated) START condition | Load capacitance < 400 pF | 600 | - | - | ns |
| $t_{LOW}$ | Timing of the LOW period of the SCL clock | Load capacitance < 400 pF | 1.3 | - | - | µs |
| $t_{HIGH}$ | Timing of the HIGH period of the SCL clock | Load capacitance < 400 pF | 600 | - | - | ns |
| $t_{SU}$ DATA | DATA set-up time | Load capacitance < 400 pF | 100 | - | - | ns |
| $t_{HD}$ DATA | DATA hold-up time | Load capacitance < 400 pF | 0 | - | 900 | ns |
| $tr_{DA}$ | Rise time of SDA | Load capacitance < 400 pF | 30 | - | 250 | ns |
| $tf_{DA}$ | Fall time of SDA | Load capacitance < 400 pF | 30 | - | 250 | ns |

**Table 258. I$^2$C timing specification: High-Speed Mode**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | Load capacitance < 100 pF | 0 | - | 3.4 | MHz |
| $t_{SU}$ START | Set-up time for a (repeated) START condition | Load capacitance < 100 pF | 160 | - | - | ns |

**Table 258. I$^2$C timing specification: High-Speed Mode**...*continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| t$_{HD}$ START | hold time of a (repeated) START condition | Load capacitance < 100 pF | 160 | - | - | ns |
| t$_{LOW}$ | Timing of the LOW period of the SCL clock | Load capacitance < 100 pF | 160 | - | - | ns |
| t$_{HIGH}$ | Timing of the HIGH period of the SCL clock | Load capacitance < 100 pF | 60 | - | - | ns |
| t$_{SU}$ DATA | DATA set-up time | Load capacitance < 100 pF | 10 | - | - | ns |
| t$_{HD}$ DATA | DATA hold-up time | Load capacitance < 100 pF | 0 | - | - | ns |
| tr$_{DA}$ | Rise time of SDA | Load capacitance < 100 pF | 10 | - | 80 | ns |
| tf$_{DA}$ | Fall time of SDA | Load capacitance < 100 pF | 10 | - | 80 | ns |

**Table 259. I$^2$C timing specification: Fast + High-Speed-Mode**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| f$_{SCL}$ | SCL clock frequency | Load capacitance < 100 pF | 0 | - | 1 | MHz |
| t$_{SU}$ START | Set-up time for a (repeated) START condition | Load capacitance < 100 pF | 260 | - | - | ns |
| t$_{HD}$ START | hold time of a (repeated) START condition | Load capacitance < 100 pF | 260 | - | - | ns |
| t$_{LOW}$ | Timing of the LOW period of the SCL clock | Load capacitance < 100 pF | 500 | - | - | ns |
| t$_{HIGH}$ | Timing of the HIGH period of the SCL clock | Load capacitance < 100 pF | 260 | - | - | ns |
| t$_{SU}$ DATA | DATA set-up time | Load capacitance < 100 pF | 50 | - | - | ns |

**Table 259. I$^2$C timing specification: Fast + High-Speed-Mode***...continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| t$_{HD}$ DATA | DATA hold-up time | Load capacitance < 100 pF | 0 | - | - | ns |
| tr$_{DA}$ | Rise time of SDA | Load capacitance < 100 pF | - | - | 120 | ns |
| tf$_{DA}$ | Fall time of SDA | Load capacitance < 100 pF | - | - | 120 | ns |

## 11.3 Timing characteristics of host interface commands

**TIMING OF VEN TRIGGERED BOOT**

**Table 260. Timing of VEN and command processing (Single Host – HIF1 I2C)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{BOOT}$ | Boot time, chip initialization | VEN transition from L to H starts the chip initialization. During this time I2C commands/packets are not accepted and processed. | - | - | 2.0 | ms |
| $t_{FW\_DOWNLOAD\_CMD}$ | Time after VEN transition from L to H, at which firmware download commands can be processed | After boot System waits for incoming packets for secure firmware update, FW download commands are accepted | 2.0 | - | 4950.0 | ms |
| $t_{CMD\_MODE\_SWITCH}$ | Duration to switch from secure firmware download command mode to NCI handling command mode | Command are not accepted | 3.0 | - | 103.0 | ms |
| $t_{NCI\_CMD}$ | Time after VEN transition L to H at which NCI commands can be processed | NCI commands ares accepted | 5105.0 | - | - | ms |

**Table 261. Timing of VEN and command processing (Dual Host – HIF1 SPI)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{BOOT}$ | Boot time, chip initialization | VEN transition from L to H starts the chip initialization. During this time SPI commands/packets are not accepted and processed | - | - | 2.0 | ms |
| $t_{FW\_DOWNLOAD\_CMD}$ | Time after VEN transition from L to H, at which firmware download commands can be processed | After boot System waits for incoming packets for secure firmware update, FW download commands are accepted | 2.0 | - | 4950.0 | ms |
| $t_{CMD\_MODE\_SWITCH}$ | Duration to switch from secure firmware download command mode to NCI handling command mode | commands are not accepted | 3.0 | - | 103.0 | ms |
| $t_{NCI\_CMD}$ | Time after VEN transition L to H at which NCI commands can be processed | NCI commands are accepted | 5105.0 | - | - | ms |

**Table 262. Timing of VEN and command processing in NFC Forum mode (Dual Host – HIF2 I2C)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{BOOT}$ | Boot time, chip initialization | VEN transition from L to H starts the chip initialization. During this time I2C commands/packets are not accepted and processed | - | - | 5.0 | ms |
| $t_{FW\_DOWNLOAD\_CMD}$ | Time after VEN transition from L to H, at which firmware download commands can be processed | Firmware download not supported in dual-host configuration on the HIF2 | 0 | - | 0 | ms |
| $t_{NCI\_CMD}$ | Time after VEN transition L to H at which NCI commands can be processed | NCI commands are accepted | 5.0 | - | - | ms |

**TIMING OF CORE RESET COMMAND TRIGGERED BY COLD BOOT**

The core reset command can be used to shorten the time before the NCI commands are accepted.

**Table 263. Timing of CORE RESET command after COLD RESET command (Single Host – HIF1 I2C)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{NCI\_CORE\_RESET\_IRQ\_H}$ | duration from NCI core reset in firmware download mode until NCI command processing is entered. Indicated by IRQ transition to H | NCI core reset command sent min 2.0 ms after VEN transition from L to H and max 5052.0 ms after VEN transition from L to H and | - | - | 6.4 | ms |

**Table 264. Timing of CORE RESET command after COLD RESET command (Dual Host – HIF1 SPI)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{NCI\_CORE\_RESET\_IRQ\_H}$ | duration from NCI core reset in firmware download mode until NCI command processing is entered, indicated by IRQ transition to H | NCI core reset command sent min 2.0 ms after VEN transition from L to H and max 5052.0 ms after VEN transition from L to H and | - | - | 6.4 | ms |

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## TIMING OF NCI CORE RESET COMMAND TRIGGERED BY WARM BOOT

**Table 265.  Timing of NCI CORE RESET command to NCI command mode (Single Host – HIF1 I2C)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{NCI\_CORE\_RESET\_IRQ\_H}$ | duration from NCI core reset in NCI mode until NCI command processing is entered | NCI core reset command sent in NCI command mode | - | - | 4.1 | ms |

**Table 266.  Timing of NCI CORE RESET to NCI command mode (Dual Host – HIF1 SPI)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{NCI\_CORE\_RESET\_IRQ\_H}$ | duration from NCI core reset in NCI mode until NCI command processing is entered | NCI core reset command sent in NCI command mode on HIF1 | - | - | 4.1 | ms |

**Table 267.  Timing NCI CORE RESET to NCI command mode (Dual Host – HIF2 I2C )**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{NCI\_CORE\_RESET\_IRQ\_H}$ | duration from NCI core reset in NCI mode until NCI command processing is entered | NCI core reset command sent in NCI command mode on HIF2 | - | - | 4.1 | ms |

## TIMING OF VEN TRIGGEGRED BOOT TO SECURE FIRMWARE DOWNLOAD MODE

**Table 268.  Timing of VEN triggered boot to secure firmware download mode (single Host – HIF1 I2C )**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{DWL\_COMMAND\_PROCESSING}$ | duration from DWL GET SESSION command until download command processing is entered | | - | 0.7 | 1.0 | ms |

**Table 269.  Timing of VEN triggered boot to secure firmware download mode (single Host – HIF1 SPI )**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{DWL\_COMMAND\_PROCESSING}$ | duration from DWL GET SESSION command until download command processing is entered | | - | 0.7 | 1.0 | ms |

## 11.4  Clock input

**Table 270.  Crystal requirements for ISO/IEC14443 compliant operation**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{xtal}$ | crystal frequency | ISO/IEC compliancy | - | 27.12 | - | MHz |
| delta $f_{xtal}$ | crystal frequency accuracy | for full RF operating range | -40 | - | +40 | ppm |
| ESR | equivalent series resistance | - | 10 | 30 | 100 | Ω |
| $C_L$ | load capacitance | - | 6 | 8 | 10 | pF |
| $t_{startup}$ | crystal startup time | - | - | - | 1 | ms |
| $P_{xtal}$ | crystal power dissipation | - | - | - | 100 | µW |

**Table 271.  Frequency requirements for a direct clock input (no crystal)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{clk}$ | clock frequency | ISO/IEC compliancy | - | 24 | - | MHz |
| | | | - | 32 | - | |
| | | | - | 48 | - | |
| delta $f_{clk}$ | clock frequency accuracy | for full RF operating range | -40 | - | +40 | ppm |
| $\varphi_n$ | phase noise | input phase noise floor at 100 kHz offset | - | - 150 | -145 | dBc/Hz |
| $\varphi_n$ | phase noise | input phase noise floor at 1 MHz offset | - | - 152 | -149 | dBc/Hz |
| $V_i$ | Input voltage boundary | sinus signal | 0 | - | 1.8 | V |
| $V_{i(p-p)}$ | peak-to-peak Input voltage | sinus signal | 0.4 | - | 1.8 | V |
| $V_{i(clk)}$ | clock input voltage | square signal | 0 | - | 1.8 +/-10 % | V |

## 11.5 DPC characteristics

**Table 272. Dynamic power control characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Minimum hysteresis configured in EEPROM DPC_HYSTERESIS (address 079h) | depends on application target current | ApplicationTargetCurrent × 0.0609 + 2 mA | - | - | mA |
| | Max target current configured in EEPROM DPC_TARGET_CURRENT (077h) | hysteresis as configured in DPC_HYSTERESIS (address 079h) | | - | 350-Hysteresis | mA |

## 11.6 EEPROM characteristics

**Table 273. EEPROM characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $N_{endu(W)}$ | write endurance | at ambient temperature $T_a$ = +25 °C | 100 | - | - | Kcycle |
| $t_{ret}$ | retention time | at ambient temperature $T_a$ =+25 °C | 25 | - | - | year |

## 11.7 Thermal characteristics

**Table 274. Operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $T_{amb}$ | ambient operating temperature | in still air with exposed pins soldered on a 4 layer JEDEC PCB, transmitter output current up to 350 mA | -40 | 25 | 85 | °C |
|  |  | in still air with exposed pins soldered on a 4 layer JEDEC PCB, TX current = 120 mA @ VDDPA=3.6 V | -40 | 25 | 105 | °C |

**Table 275. Thermal characteristics VFBGA64 package**

| Symbol | Parameter | Conditions | Typ | Unit |
|--------|-----------|------------|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air with exposed pad soldered on a 4 layer JEDEC PCB, package VFBGA64 | 53 | K/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case | - | 22 | K/W |

**Table 276. Junction temperature**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|------------|-----|-----|------|
| $T_{j\_max}$ | maximum junction temperature | - | - | 125 | °C |

**Table 277. Thermal shutdown temperature**

| Symbol | Parameter | Conditions | Typ | Unit |
|--------|-----------|------------|-----|------|
| $T_{shutdown}$ | shutdown of chip due to high temperature detected by temp sensor | - | 125 | °C |

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# 12 Package outline

## 12.1 VFBGA64 package

**Table 278. Package outline VFBGA64 (SOT1307-2)**
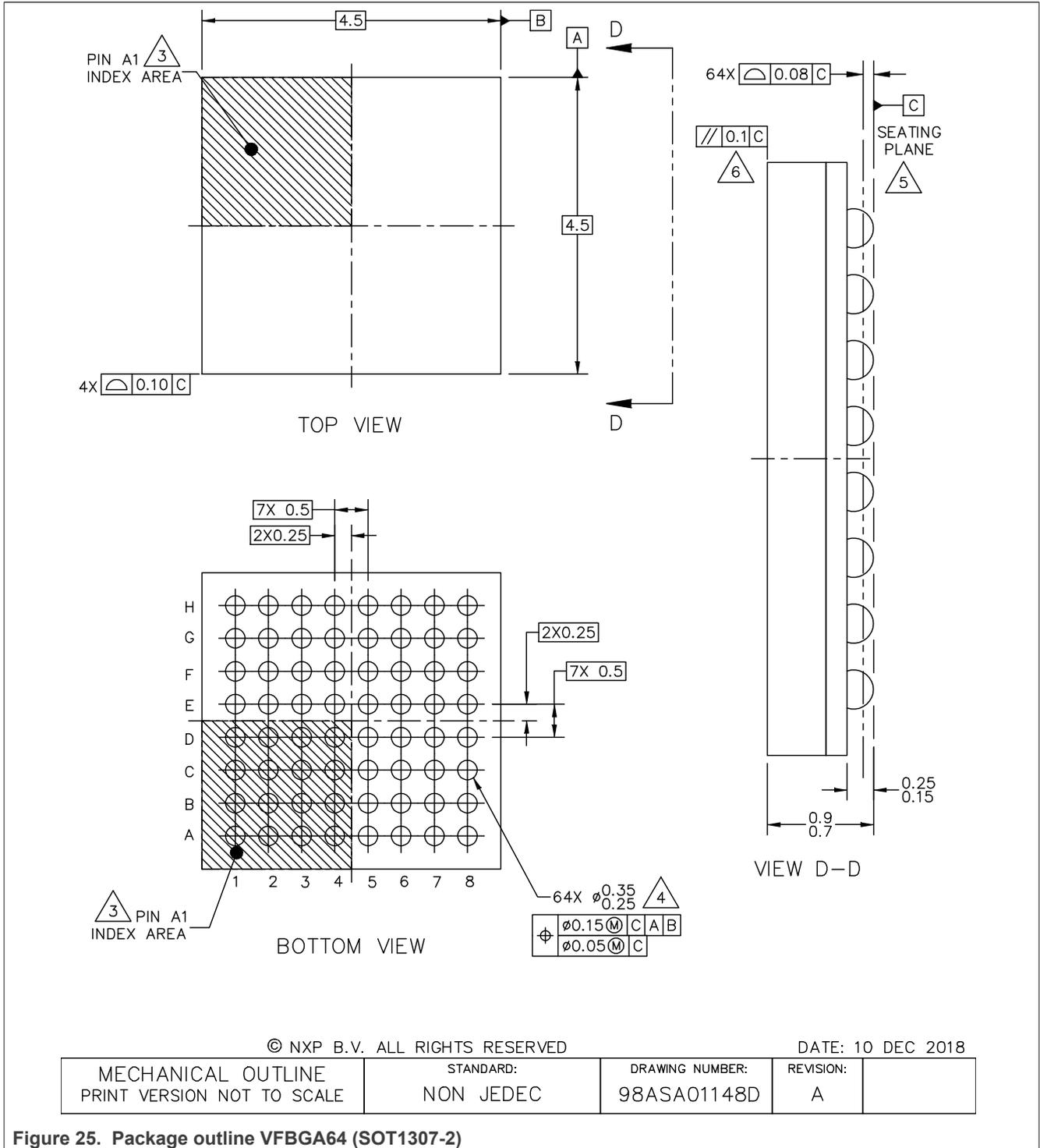


**Figure 25. Package outline VFBGA64 (SOT1307-2)**

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA01148D | REVISION:<br>A |
|---|---|---|---|

**Figure 26. Package outline note VFBGA64 (SOT1307-2)**

## 13 Package marking

### 13.1 Package marking drawing VFBGA64

Terminal 1 index area

A : 4
B : 4
C : 5
D : 8

0          5

*aaa-036197*

**Figure 27.  Marking of VFBGA64 package**
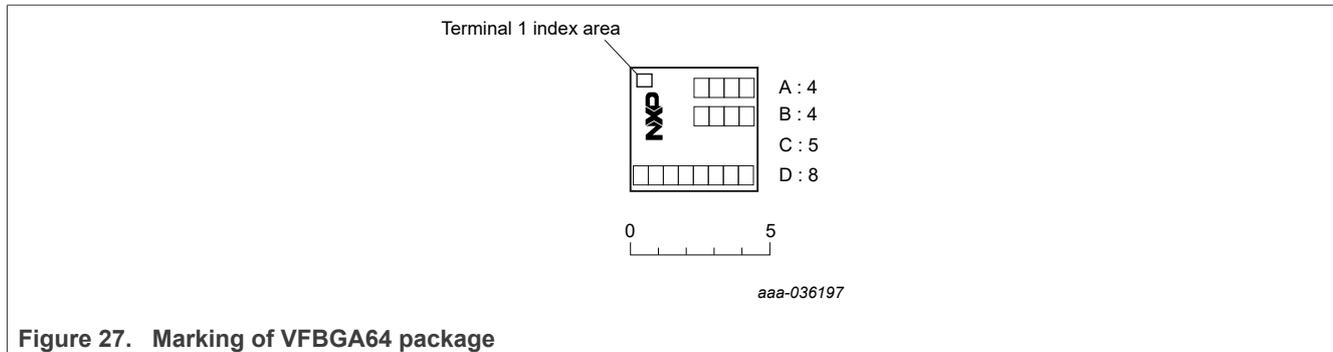
Line A: 4 characters; "**7220**"

Line B: 4 characters, contains the firmware version: C100 or C101

Line C: 5 characters; contains the diffusion batch identifier (DB ID), a blank " " and the assembly sequence identifier (AS ID)

Line D: 8 characters; stDYYWW(X) - contains information assembly center, date code, and maturity level ("X" = engineering samples, " " = released product)

## 14  Handling information

| CAUTION | |
|---|---|
|  | This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.<br><br>Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards. |

## 15 Abbreviations

**Table 279. Abbreviations**

| Acronym | Description |
|---------|-------------|
| AA | audio accelerator |
| ADC | analog-to-digital converter |
| AGC | automatic gain control |
| AHB | advanced high-performance bus |
| AHB-Lite | advanced high-performance bus (single-controller implementation) |
| AHB bus | advanced high-performance bus |
| APB | advanced peripheral bus |
| API | application programming interface |
| ARC | adaptive receiver control |
| Arm | Advanced RISC Machine |
| AWC | adaptive waveshape control |
| BBA | baseband amplifier |
| BOD | brownout detection |
| CITO | controller input target output (previously master input slave output) |
| CLIF | contactless interface |
| COTI | controller output target input (previously master output slave input) |
| CPU | central processing unit |
| CRC | cyclic redundancy check |
| CTR | current transfer ratio |
| CTS | clear to send |
| DAC | digital-to-analog converter |
| DC-DC | switch-mode voltage regulator which uses an inductor to store and transfer energy to the output, used for a power supply voltage conversion. PN7220 integrates a step-up/boost converter |
| DDR | double data rate |
| DMA | direct memory access |
| DPC | dynamic power control |
| ECC | elliptic curve cryptography |
| EEPROM | electrically erasable programmable read-only memory |
| EMC | electromagnetic compatibility |
| EMD | electromagnetic disturbance |
| ETB | Embedded Trace Buffer |
| ETM | Embedded Trace Macro |
| EOF | end-of-frame |
| Fm+ | Fast-mode Plus |
| FSM | finite state machine |

**Table 279. Abbreviations**...*continued*

| Acronym | Description |
|---------|-------------|
| GND | Ground |
| GPIO | general-purpose input output |
| HID | human interface device |
| HPD | hard power down |
| HW | hardware |
| IC | Integrated Circuit |
| IIR | infinite impulse response |
| IrDA | Infrared Data Association |
| IAP | In-Application Programming |
| ISP | In-System Programming |
| I/O | input/output |
| I/Q | in-phase/quadrature-phase |
| JEDEC | Joint Electron Device Engineering Council |
| LDO | low dropout regulator |
| LPCD | low-power card detection |
| LPUART | Low-Power Universal Asynchronous Receiver / Transmitter |
| LSB | least significant bit |
| LSByte | least significant byte |
| MISO | SPI interface controller in target out |
| MSL | moisture sensitivity level |
| MOSI | SPI interface controller out target In |
| NFC | near-field communication |
| NRZ | non-return-to-zero |
| NSS | SPI interface active-low target-select signal |
| NTS | not target select (previously not slave select) |
| NVIC | nested vectored interrupt controller |
| OS | operating system |
| OTP | one time programmable |
| PCB | printed-circuit board |
| PC | personal computer |
| PCD | power card detection |
| PICC | proximity inductive coupling card |
| PLL | phase-locked loop |
| PMU | power management unit |
| PWM | pulse width modulation |
| RAM | random-access memory |

**Table 279. Abbreviations**...*continued*

| Acronym | Description |
|---------|-------------|
| RF | radio frequency |
| RNG | random number generator |
| ROM | read-only memory |
| RSA | Rivest, Shamir, and Adleman public key cryptosystem |
| RSSI | receiver signal strength indicator |
| RTOS | real-time operating system |
| RTS | request to send |
| SCK | SPI interface serial clock |
| SCL | $I^2C$ interface serial clock |
| SDA | serial data |
| SMPS | switch mode power supply |
| SPI | serial peripheral interface |
| SRAM | static random-access memory |
| SWD | serial wire debug |
| TFT | display technology: thin-film transistor-display |
| TX | transmit |
| UART | universal asynchronous receiver transmitter |
| UID | Unique identifier of a card, used during anti-collision sequence to select one out of multiple cards. |
| USB | universal serial bus |
| VREF | voltage reference |

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# 16  Revision history

**Table 280.  Revision history**

| Document ID | Release date | Description |
|---|---|---|
| PN7220 v.3.4 | 12 November 2024 | Editorial change: removed references to ULPCD (not supported by PN7220)<br>• Section 9.10 "Dynamic power control (DPC)": Figure 16 "System overview: DPC, AWC, and ARC" updated<br>• Section 9.18.2.1.2 "DCDC_PWR_CONFIG (0x0000)": updated description<br>• Section 9.18.2.1.5 "TXLDO_VDDPA_CONFIG (0x0006)": updated description<br>• Section 9.18.2.1.6 "TXLDO_VDDPA_MAX_RDR_NFC_FORUM (0x0007)": updated description<br>• Section 9.18.2.1.8 "TXLDO_VDDPA_MAX_CARD (0x0008)": updated description<br>• Section 9.18.2.1.9 "BOOST_DEFAULT_VOLTAGE (0x0009)": updated description<br>• Section 15 "Abbreviations": updated |
| PN7220 v.3.3 | 16 April 2024 | • Section 5 "Firmware versions": added<br>• Section 9.5 "System power states": updated<br>• Section 9.12 "Adaptive receiver control (ARC)": updated<br>• Section 9.18.2.1.12 "XTAL_DELAY (06B8h)": added<br>• Section 9.18.2.1.13 "CLK_INPUT_FREQ (0x0011)": updated.<br>• Table 255 "Power supply connection timing ": updated $t_{boot}$ max value<br>• Section 11.3 "Timing characteristics of host interface commands": added<br>• Section 13.1 "Package marking drawing VFBGA64": updated |
| PN7220 v.3.2 | 24 November 2023 | • Section 6 "Ordering information": updated<br>• Section 8.1 "Pin description VFBGA64 ": updated |
| PN7220 v.3.1 | 20 September 2023 | • Section 8.1 "Pin description VFBGA64 ": Pin description for E7 and C7 corrected |
| PN7220 v.3.0 | 5 July 2023 | • Initial version |

# Legal information

## Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1]   Please consult the most recently issued document before initiating or completing a design.
[2]   The term 'short data sheet' is explained in section "Definitions".
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