**NXP Semiconductors**
Data Sheet: Technical Data

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# MPC5775K

# MPC5775K Data Sheet

## Supports MPC5774K and MPC5775K

### Features

- The MPC5775K is a microcontroller developed by NXP Semiconductors and built on Power Architecture® technology. It supports computation-intensive applications and targets chassis and safety applications that require a high Automotive Safety Integrity Level (ASIL). The MPC5775K is a SafeAssure solution. It is specifically designed for dealing with the following applications:
  - RADAR
  - Electrical Stability Control (ESC)
  - Higher-end Electrical Power Steering (EPS)
  - Airbag and sensor fusion applications
- MPC5775K is a multicore microcontroller unit
  - Contains one safety core consisting of an e200z420 with an e200z419 check core running in delayed Lockstep mode
  - Contains two e20z7260 cores, integrating both a SPE2 4-way integer SIMD engine and an EFP2 2-way single-precision floating point engine, running independently of each other
  - Supports Harvard bus architecture with 64-bit data/instructions and 32-bit addresses
  - Provides Nexus 3+ support
  - Provides VLE instruction support
  - Supports big-endian data format
  - Supports End-2-End ECC
- RADAR Analog-Front-End (AFE)
  - 8 Continuous-Time Sigma-Delta ADCs
  - 12-bit DAC
  - 40 MHz Crystal Oscillator
  - 320 MHz PLL
- Local core memories
  - Instruction cache (z7260: 16 KB, z420: 8 KB)
  - Data cache (z7260: 16 KB, z420: 4 KB)
  - TagRAMs for cache including ECC
  - DataRAMs for cache including EDC
  - Local data RAM (Data TCM: 64 KB) including ECC (z7260/z420)
- Four 37 external channel SAR ADCs
- Communication interfaces
  - Four FlexCAN modules
  - One Serial Interprocessor Interface (SIPI) module
  - Four DSPI modules
  - Four LINFlex modules
  - Three Inter-Integrated Circuit (I2C) modules
  - One dual-channel FlexRay module
  - One Ethernet module
  - One MCAN module
- Timers
  - Three Software Watchdog Timers (SWT)
  - Two Periodic Interval Timers (PITs)
  - Three 6-channel eTimers
- Security and integrity
  - Two Cyclic Redundancy Check (CRC) generator modules
  - Memory Error Management Unit (MEMU)
  - Fault Collection and Control Unit (FCCU)
  - Self-Test Control Unit (STCU2)
  - Error Injection Module (EIM)
- Clocks
  - Dual PLL Digital Interface (PLLDIG)
  - IRCOSC Digital Interface
- System
  - Direct Memory Access Controller (eDMA)
  - Direct Memory Access Multiplexer (DMAMUX)
  - Interrupt Controller (INTC)
  - Two Cross-Triggering Units (CTU)

# Table of Contents

# 1 Introduction

## 1.1 Device family feature summary table

**Table 1. Device family feature summary table**

| Part Number | MPC5775K | MPC5774K |
|---|---|---|
| CPU | e200z420 Lock-step<br>2 x e200z7260 + SPE2 + EFP2 | |
| SPT | Yes | |
| CTE | 1 x 10MHz | |
| Flash | 4M | 3M |
| SRAM | 1.5M | 1M |
| MPU | CoreMPU: 24 Entries per core<br>SystemMPU: 2 x 16 Entries | |
| Safe eDMA | 32 channels, 64 triggers | |
| PIT | 2x | |
| SWT | 3x | |
| STM | 3x | |
| CRC | 2x | |
| FCCU | Yes | |
| TSENS | 2x | |
| FlexRay | Dual channel | |
| Ethernet | 100MBits MII, RMII | |
| LFAST / SIPI | 1 x 320MHz | |
| SAR ADC (12bit) | 4x (37 external channels) | |
| SD ADC (12 bit) | 8 channels | |
| DAC / WGM | 1x @ 2MSamples / s | |
| eTimer | 3 x 6 Channels | |
| FlexPWM | 2x | |
| CTU | 2x | |
| LINFlex | 4x | |
| SPI | 4x | |
| FlexCAN | 4x | |
| MCAN-FD | 1x | |
| IIC | 3x | |
| PDI | Up to 100MHz, 12 bit, 3.3V or 1.8V (1.8V requires extra supply) | |
| SIUL2 | 1x | |
| BAM | 1x | |
| INTC | 1x | |

*Table continues on the next page...*

**Table 1. Device family feature summary table (continued)**

| Part Number | MPC5775K | MPC5774K |
|---|---|---|
| SSCM | 1x | |
| STCU | 1x | |
| MEMU | 1x | |
| Semaphore | 1x | |
| Mode Entry | 1x | |
| Clock Gen Module | 1x | |
| Reset Gen Module | 1x | |
| Supply | 3.3V IO (optional 1.8V I/O for PDI)<br>3.3V High Fidelity Analog<br>1.25V with internal switched regulator or external supply<br>(For internal switched regulator mode, 1.25V requires 3.8V external supply for pass transistor and driver supply) | |
| PLL | Dual PLL, 1 x FM modulated | |
| Internal RC | 16 MHz | |
| External xtal | 40 MHz | |
| JTAGM | 1x | |
| Debug | Nexus III / Aurora | |
| Junction Temperature | -40 to + 150 °C | |

## 1.2 Feature summary

The on-chip modules within the MPC5775K include the following features:

- 32-bit CPU (e200z420) based on Power Architecture technology with delayed lock step checker core, dual issue and Harvard bus architecture
  - 8 KB code cache
  - 4 KB data cache
  - 64 KB data local memory (0-wait state for all read and 32-/64-bit write accesses)
  - Wait states possible for backdoor accesses via the crossbar
  - Scalar single-precision Floating Point Unit
- Two 32-bit CPUs (e200z7260) based on Power Architecture technology with dual issue and Harvard bus architecture
  - 16 KB code cache with EDC and parity
  - 16 KB data cache with EDC and parity
  - 64 KB data local memory with ECC (0-wait state for all read and 32/64-bit write accesses)
  - Wait states possible for backdoor accesses via the crossbar

    - 4-way integer processing unit (SPE2)
    - 2-way single-precision Floating Point Unit (FPU)
- Up to 4 MB on-chip Code Flash (FMC Flash) with ECC including 96 KB EEPROM emulation
    - Three ports (one per CPU) shared between code and data flash with 4 × 256 bit buffer for code and data flash including prefetch functions
    - Code flash partitions:
        - Partition 0/1: 4 × 16 KB
        - Partition 2/3: 2 × 32 KB
        - Partition 4/5: 6 x 64 KB
        - Partition 6/7: up to 6 × 256 KB
    - Data flash is part of the code flash module and is partitioned as 2 × 32 KB + 2 × 16 KB
    - Single- and double-bit error visibility is supported
- Up to 1.5 MB on-chip SRAM with ECC
    - Single- and double-bit error visibility is supported
    - Up to 4 ports
    - Up to 8 banks allow simultaneous accesses from different masters to different banks
- Interrupt Controller (INTC)
    - 32 interrupt priority levels
- Dual Frequency Modulated Phase-Locked Loop (FMPLL)
    - One of the two PLLs supports frequency modulation
    - Up to ±2% modulation range with the option to switch off the frequency modulation
- 16 MHz Internal RC Oscillator (IRCOSC) with 8% precision after trimming
- Two PIT modules, each with four Periodic Interrupt Timers with 32-bit counter resolution per core
- Crossbar switch architecture with 64 bits allowing concurrent access to peripherals, flash memory, or RAM from multiple bus masters with end-to-end ECC
- Two AIPS bridges
    - These are 32-bit wide interfaces
    - Internal posted write buffer is not supported
- Two 32-channel Enhanced Direct Memory Access controllers (eDMA)
    - Safety enabled: Lockstep mode replication and ECC on DMA memory
    - DMA channel multiplexer with 64 input lines
    - Includes PIT trigger gate capability
    - Minor loop offset to support submodular IPs such as eTimer
    - Supports cancellation of a transfer either by hardware fault detection (safe mode signaled) or according to user selection

    - DMA channel MUX can support multiple synchronous clock domains and multiple acknowledged signals (ipd_ack, ipd_done, and so on)
    - Replicated DMA2× logic for safety
    - ECC protected DMA RAM for safety
- System Integration Unit Lite (SIUL2)
- Wake-up module to support single non-maskable interrupt (NMI)
- Boot Assist Module (BAM) enables booting via serial bootload through the asynchronous FlexCAN or LINFlex
    - Supports user programmable 64-bit password protection for serial boot mode
- Three eTimer modules (eTimer)
    - Each eTimer has six 16-bit general-purpose up/down identical counter/timer channels with dedicated motor control quadrature decode feature and DMA support
- Analog-to-digital converter system
    - Four separate 12-bit SAR analog converters with 16 precision channels each
- FFT and Signal Processing Accelerator
    - 16-bit integer FFT (point, twiddles, results)
    - 24-bit intermediate results
    - Complex-to-complex or real-to-complex
    - Two Radix-4 units with 50 M Radix-4 operations per second each
- PDI interface
    - Up to 100 MHz pixel clock
    - Additional mode to read in RADAR data from external ADC
- Fault Collection and Control Unit (FCCU)
- Ethernet port with PTP (IEEE1588 precision time stamps)
    - Data rate of 10/100 Mbit/s
    - Supports MII: MIILite and RMII interface to PHY
- FlexRay interface with 128 message buffers
- Four Controller Area Network (FlexCAN) modules with 64 message buffers
- Four Serial Peripheral Interface (SPI) modules with 8/8/4/4 chip selects and DMA support
- Three Inter-Integrated Circuit (IIC) buses
- Four Serial Communication Interface (LINFlex) modules with LIN and DMA support
- Nexus 5001 development interface (NDI) that complies with the IEEE-ISTO 5001-2003 standard
    - High-speed debug interface Nexus Aurora
- MCAN interface which supports CAN-FD protocol
- Device and board test support that complies with the Joint Test Action Group (JTAG) IEEE 1149.1 standard
- Support for software based debug using core accessible JTAGM

- On-chip voltage regulator controller manages the supply voltage for core logic or
- External core voltage supply for the core logic
  - Integrated LVD for POR, flash memory and I/O, and logic

## 1.3 Core features

MPC5775K is a multicore microcontroller unit that:

- Contains one safety core consisting of an e200z420 with an e200z419 checker core running in delayed Lockstep mode
- Contains two cores running independent of each other implemented as z7260 and adding:
  - SPE2 4-way integer SIMD engine
  - EFP2 2-way single precision floating point engine freedom of interference by placing cores in separate design lakes
- Supports Harvard bus architecture with 64-bit data/instructions and 32-bit addresses
- Provides Nexus 3+ support
- Contains the following local core memories
  - Instruction cache (e200z7260: 16 KB, e200z420: 8 KB)
  - Data cache (e200z7260: 16 KB, e200z420: 4 KB)
  - TagRAMs for cache including ECC
  - DataRAMs for cache including EDC
  - Local data RAM (Data TCM: 64 KB) including ECC (e200z7260/e200z420)
- Provides VLE instruction support
- Supports big-endian data format
- Supports End-2-End ECC
- Supports local core MPU with 24 entries:
  - 6 entries are dedicated to instructions
  - 12 entries are dedicated to data
  - 6 entries are selectable for instructions or data
- Does not support MMU
- Supports dual issue processing (excluding load/store, FPU, and SPE2)
- Provides a basic set of counters, including Periodic Interrupt Timer, System Timer Module, and Software Watchdog Timer
- Provides four 32-bit counter for software selectable events to support performance monitoring as also enhanced flow control monitoring

**NOTE**

MPC5775K does not support BookE.

## 1.4 Block diagram

The following figure shows a top-level block diagram of the MPC5775K device.

**NOTE**

"DTCM" in the figure below is referred to as "DMEM" in the Core Complex Overview and the Core description chapters.

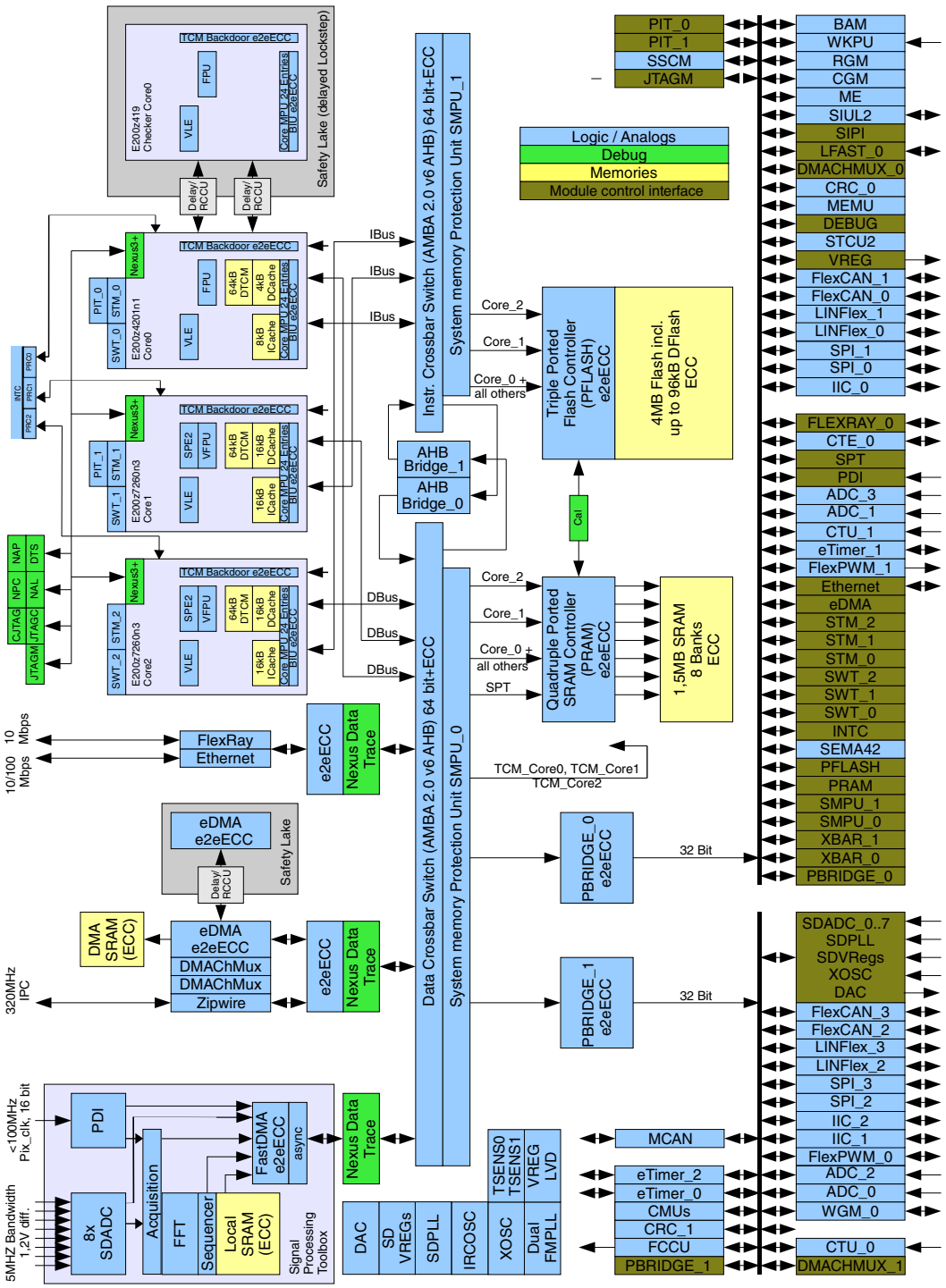



**Figure 1. MPC5775K block diagram**

# 2 Ordering parts

## 2.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the device number.

# 3 Part identification

## 3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 3.2 Format

Part numbers for this device have the following format: MPC5775K

## 3.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description |
|---|---|
| M | Qualification status<br>• P – Pre-qualification<br>• M – Fully spec. qualified, general market flow<br>• S – Fully spec. qualified, automotive flow |
| PC | Core code (Power Architecture) |
| 5775K | Device number |

# 4 General

## 4.1 Absolute maximum ratings

**NOTE**

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed.

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD\_HV\_PMU}$ | 3.3 V PMU supply voltage | — | –0.3 | 4.0[1,2] | V |
| $V_{DD\_HV\_REG3V8}$ | REG3V8 Supply Voltage | — | –0.3 | 5.5 | V |
| $V_{DD\_HV\_IOx}$ | 3.3 V input/output supply voltage | — | –0.3 | 3.63[1, 2] | V |
| $V_{SS\_HV\_IOx}$ | Input/output ground voltage | — | –0.1 | 0.1 | V |
| $V_{DD\_HV\_IO\_PDI}$ | PDI IO Supply Voltage | — | –0.3 | 3.63[1, 2] | V |
| $V_{DD\_HV\_FLA}$ | 3.3 V flash supply voltage | — | –0.3 | 3.63[1, 2] | V |
| $V_{DD\_HV\_RAW}$ | AFE RAW supply voltage | — | –0.1 | 4 | V |
| $V_{DD\_HV\_DAC}$ | AFE DAC supply voltage | — | –0.1 | 4 | V |
| $V_{DD\_LV\_IO*}$ | Aurora supply voltage | — | –0.3 | 1.5 | V |
| $V_{DD}$ | 1.25 V core supply voltage[3, 4, 5] | — | –0.3 | 1.5 | V |
| $V_{SS}$ | 1.25 V core supply ground[3, 4, 5] | — | –0.3 | 0.3 | V |
| $V_{SS\_LV\_OSC}$ | Oscillator amplifier ground | — | –0.1 | 0.1 | V |
| $V_{DD\_LV\_PLL0}$ | System PLL supply voltage | — | –0.3 | 1.5 | V |
| $V_{DD\_LV\_LFASTPLL}$ | LFAST PLL supply voltage | — | –0.3 | 1.5 | V |
| $V_{DD\_HV\_ADCREF0/2}$<br>$V_{DD\_HV\_ADCREF1/3}$ | 3.3 V ADC_0 and ADC_2 high reference voltage<br>3.3 V ADC_1 and ADC_3 high reference voltage | — | –0.3 | 4.0 | V |
| $V_{SS\_HV\_ADCREF0/2}$<br>$V_{SS\_HV\_ADCREF1/3}$ | ADC_0 and ADC_2 ground and low reference voltage<br>ADC_1 and ADC_3 ground and low reference voltage | — | –0.1 | 0.1 | V |
| $V_{DD\_HV\_ADC}$ | 3.3 V ADC supply voltage | — | –0.3 | 4.0[1, 2] | V |
| $V_{SS\_HV\_ADC}$ | 3.3 V ADC supply ground | — | –0.1 | 0.1 | V |
| $TV_{DD}$ | Supply ramp rate[6] | — | 0.00005 | 0.1 | V/µs |

*Table continues on the next page...*

**Table 2. Absolute maximum ratings (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IN\_XOSC}$ | Voltage on XOSC pins with respect to ground | — | -0.3 | 1.47 | V |
| $V_{INA}$ | Voltage on SAR ADC analog pin with respect to ground ($V_{SS\_HV\_ADCREFx}$) | — | –0.3 | $V_{DD\_HV\_ADCREFx}$ + 0.3 | V |
| $V_{INA\_SD}$ | Voltage on Sigma-Delta ADC analog pin with respect to ground[7] | Powered up | -0.3 | $V_{DD\_HV\_RAW}$ + 0.3 | V |
| | | Powered down | -0.3 | 1.47 | |
| $V_{IN}$ | Voltage on any digital pin with respect to ground ($V_{SS\_HV\_IOx}$) | Relative to $V_{DD\_HV\_IOx}$ | –0.3 | $V_{DD\_HV\_IOx}$ + 0.3[8] | V |
| $I_{INJPAD}$ | Injected input current on any pin during overload condition | — | –10 | 10 | mA |
| $I_{INJSUM}$ | Absolute sum of all injected input currents during overload condition | — | –50 | 50 | mA |
| $T_{STG}$ | Storage temperature | — | –55 | 150 | °C |

1. 5.3 V for 10 hours cumulative over lifetime of device; 3.3 V +10% for time remaining.
2. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
3. 1.45 V to 1.5 V allowed for 60 seconds cumulative time at maximum $T_J$=150°C; remaining time as defined in following notes
4. 1.375 V to 1.45 V allowed for 10 hours cumulative time at maximum $T_J$=150°C; remaining time as defined in following note
5. 1.32 V to 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum $T_J$=150°C.
6. $TV_{DD}$ is relevant for all external supplies
7. ADC inputs include an overvoltage detect function that detects any voltage higher than 1.2V with respect to ground on either ADC input and open circuit (disconnect) the input in order to prevent damage to the ADC internal circuitry. The ADC input remains disconnected until the inputs return to the normal operating range.
8. Only when $V_{DD\_HV\_IOx}$ < 3.63 V.

## 4.2 Operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the datasheet are valid, except where explicitly noted. The device operating conditions must not be exceeded, or the functionality of the device is not guaranteed.

**Table 3. Device operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| $V_{DD\_HV\_PMU}$ | 3.3V PMU Supply Voltage | — | 3.13 | 3.3 | 3.6 | V |
| $V_{DD\_HV\_REG3V8}$ | REG3V8 Supply Voltage | — | 3.13 | 3.8 | 5.5 | V |
| $V_{DD\_HV\_IO\_PDI}$ | PDI IO Supply Voltage | 1.8 V mode | 1.62 | 1.8 | 1.98 | V |
| | | 3.3 V mode | 3.0 | 3.3 | 3.6 | V |
| $V_{DD}$ | Core Supply Voltage | — | 1.19 | 1.25 | 1.31 | V |
| $V_{DD\_HV\_IO}$ | Main GPIO 3V Supply Voltage | — | 3.13 | 3.3 | 3.6 | V |
| $V_{DD\_LV\_IO\_*}$ | Aurora Supply Voltage | | 1.19 | 1.25 | 1.31 | V |

*Table continues on the next page...*

## Table 3. Device operating conditions (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| $V_{DD\_LV\_PLL0}$ | System PLL Supply Voltage | — | 1.19 | — | 1.31 | V |
| $V_{DD\_LV\_LFASTPLL}$ | LFAST PLL Supply Voltage | — | 1.19 | — | 1.31 | V |
| $V_{DD\_HV\_FLA}$[2] | Flash Supply Voltage | — | 3.13 | 3.3 | 3.6 | V |
| $V_{DD\_HV\_ADC}$ | SAR ADC Supply Voltage (HVD supervised) | — | 3.13 | 3.3 | 3.6 | V |
| $V_{DD\_HV\_RAW}$ | 3.3V AFE RAW Supply Voltage | — | 3.13 | 3.3 | 3.6 | V |
| $V_{DD\_HV\_DAC}$ | 3.3V AFE DAC Supply Voltage | — | 3.13 | 3.3 | 3.6 | V |
| $V_{DD\_HV\_ADCREF0/2}$<br>$V_{DD\_HV\_ADCREF1/3}$ | 3.3 V ADC_0 and ADC_2 high reference voltage<br><br>3.3 V ADC_1 and ADC_3 high reference voltage | — | 3.13 | 3.3 | 3.6 | V |
| $V_{IN}$ | Voltage on digital pin with respect to ground ($V_{SS\_HV\_IOx}$) | — | — | — | $V_{DD\_HV\_IOx}$ + 0.3 | V |
| $V_{INSDPP}$ | Sigma-Delta ADC Input Voltage (peak-peak) [3, 4] | Differential | — | — | 1.2 | V |
| $V_{INSR}$ | Sigma-Delta ADC Input Slew Rate[3] | — | — | — | 165 | V/µs |
| $R_{TRIM\_TOL}$ | External Trim Resistor tolerance | ±0.1% | 40.16 | 40.2 | 40.25 | kΩ |
| $R_{TRIM\_TEMPCO}$ | External Trim Resistor Temperature Coefficient | — | — | — | 25 | ppm/°C |
| $V_{INA}$[5] | Voltage on SAR ADC analog pin with respect to ground ($V_{SS\_HV\_ADCREFx}$) | — | — | — | $V_{DD\_HV\_ADCREFx}$ + 0.3 | V |
| $T_A$,[6] | Ambient temperature at full performance[7] | — | –40 | — | 105 | °C |
| $T_J$[6] | Junction temperature | — | –40 | — | 150 | °C |
| $F_{XTAL}$ | XOSC Crystal Frequency[8] | — | — | 40 | — | MHz |
| AFE Bypass Modes Only | | | | | | |
| $V_{INXOSCCLKVIL}$ | EXTAL external clock input low voltage | — | 0 | — | 0.4 | V |
| $V_{INXOSCCLKVIH}$ | EXTAL external clock input high voltage | — | 1 | — | 1.2 | V |
| $EXTAL_{clk}$ | EXTAL external clock frequency | — | — | 40 | — | MHz |
| $V_{inxoscjit}$ | EXTAL external clock Cycle to Cycle Jitter (peak – peak) | — | — | — | 2.5 | ps |
| $t_r/t_f$ | Rise/fall time of EXTAL external clock input | — | — | — | 1000 | ps |
| $t_{dc}$ | Duty Cycle of EXTAL external clock input | — | 49 | 50 | 51 | % |

1. Full functionality cannot be guaranteed when voltages are out of the recommended operating conditions.
2. The ground connection for the VDD_HV_FLA is shared with VSS
3. Around common mode voltage of 0.7V. Input voltage cannot exceed 1.4V prior to AFE start-up completion (VREF and VREGs on and LVDs cleared)
4. SDADC input voltage full scale is 1.2 Vpp
5. On channels shared between ADC0 and 1 or ADC2 and 3, $V_{DD\_HV\_ADCREFx}$ is the lower of $V_{DD\_HV\_ADCREF0/2}$ and $V_{DD\_HV\_ADCREF1/3}$

6. When determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is not necessary that both specifications be met at all times. However, it is critical that the junction temperature specification is not exceeded under any condition.
7. Full performance means Core0 running @ 133.33 MHz, Core1/2 running @ 266.66 MHz, SPT running @ 200 MHz, rich set of peripherals used.
8. Recommended Crystal 40 MHz (ESR≤30Ω)

## 4.3 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

**Table 4. Current consumption characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\_CORE}$ | Core current in run mode | All cores at max frequency. 1.31V. Tj = 150C | - | - | 1800[1] | mA |
| $I_{DD\_HV\_FLA}$ | Flash operating current | Tj = 150C. VDD_HV_FLA = 3.6V | - | 3[2] | 40[3] | mA |
| $I_{DD\_LV\_AURORA}$ | Aurora operating current | Tj = 150C. VDD_LV_AURORA = 1.31V. 4 TX lanes enabled. | - | - | 60 | mA |
| $I_{DD\_HV\_ADC}$ | ADC operating current | Tj = 150C. VDD_HV_ADC = 3.6V. 4 ADC operating at 80MHz. | - | 2 | 5 | mA |
| $I_{DD\_HV\_ADCREF}$ | Reference current per ADC[4]<br>Reference current per temp sensor[5] | Tj = 150C. VDD_HV_ADCREFx = 3.6V. ADC operating at 80MHz. | -<br>- | -<br>- | 1.5<br>0.75 | mA |
| $I_{DD\_HV\_RAW}$ | AFE SD and regulator operating current | Tj = 150C. VDD_HV_RAW = 3.6V. SD-PLL, AFE regulators and 8 SD enabled. | - | 114[6] | 150 | mA |
| $I_{DD\_HV\_DAC}$ | AFE DAC operating current | Tj = 150C. VDD_HV_DAC = 3.6V. DAC enabled. | - | 10 | 15 | mA |
| $I_{DD\_HV\_PMU}$ | PMU operating current | Tj = 150C. VDD_HV_PMU = 3.6V. Internal regulation enabled. | - | 2 | 10 | mA |

1. Strong dependence on use case, cache usage
2. Measured during flash read
3. Peak Flash current measured during read while write (RWW) operation
4. ADC0 and 2 on ADCREF0/2, ADC1 and 3 on ADCREF1/3
5. Temp sensor current when PMC_CTL_TD[TSx_AOUT_EN] = 1. TS0 on ADCREF0/2, TS1 on ADCREF1/3
6. Typically number is approximately 10mA per each SD-ADC enabled, 12mA for SD-PLL and 15mA for the AFE regulators

## 4.4 Voltage regulator electrical characteristics

**Table 5. Voltage regulator electrical specifications**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PORREG | POR VDD_HV_PMU | — | — | — | 2.45 | V |
| POR12R | POR VDD 1.25 V release | — | 0.97 | 1.02 | 1.06 | V |
| POR12E | POR VDD 1.25 V engage | — | 0.93 | 0.98 | 1.02 | V |

*Table continues on the next page...*

## Table 5. Voltage regulator electrical specifications (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LVD12R | Low-Voltage Detection 1.25 V release (Core VDD supply and PLL0/1 supply LVDs) | Untrimmed | 1.122 | 1.157 | 1.192 | V |
| LVD12R-trim | | Trimmed | 1.142 | 1.157 | 1.172 | V |
| LVD12E | Low-Voltage Detection 1.25 V engage (Core VDD supply and PLL0/1 supply LVDs) | Untrimmed | 1.102 | 1.137 | 1.172 | V |
| LVD12E-trim | | Trimmed | 1.122 | 1.137 | 1.152 | V |
| HVD12R-trim | High-Voltage Detection 1.25 V release (Core VDD) | Trimmed | 1.33 | 1.35 | 1.37 | V |
| HVD12E-trim | High-Voltage Detection 1.25 V engage (Core VDD supply) | Trimmed | 1.36 | 1.38 | 1.40 | V |
| APOR-R | PMC Analog POR Release Threshold (PMC) | — | 2.54 | 2.645 | 2.735 | V |
| APOR-E | PMC Analog POR Engage Threshold (PMC) | — | 2.50 | 2.60 | 2.695 | V |
| LVD33R | 3.3V Low-Voltage Detection Release Threshold (PMC, FLASH, IO, ADC) | Untrimmed | 2.90 | 3.02 | 3.13 | V |
| LVD33R-trim | | Trimmed | 3.00 | 3.05 | 3.10 | V |
| LVD33E | 3.3V Low-Voltage Detection Engage Threshold (PMC, FLASH, IO, ADC) | Untrimmed | 2.86 | 2.98 | 3.09 | V |
| LVD33E-trim | | Trimmed | 2.96 | 3.01 | 3.06 | V |
| HVD33R | 3.3V High-Voltage Detection Release Threshold (ADC) | Untrimmed | 3.45 | 3.61 | 3.75 | V |
| HVD33R-trim | | Trimmed | 3.47 | 3.53 | 3.58 | V |
| HVD33E | 3.3V High-Voltage Detection Engage Threshold (ADC) | Untrimmed | 3.51 | 3.65 | 3.79 | V |
| HVD33E-trim | | Trimmed | 3.51 | 3.57 | 3.62 | V |
| UVL30R | SMPS under-voltage lockout release threshold | Untrimmed | 2.75 | 2.90 | 3.05 | V |
| UVL25E | SMPS under-voltage lockout engage threshold | | 2.40 | 2.55 | 2.7 | V |
| DGLITCHE | Voltage Detector Deglitcher Filter Time - Engage | — | 2.0 | 3.5 | 5 | µs |
| DGLITCHR | Voltage Detector Deglitcher Filter Time - Release | — | 5 | 7 | 12 | µs |
| RSTDGLTC | VREG_POR_B Input Deglitch Filter Time | — | 200 | 320 | 500 | ns |
| RSTPUP | VREG_POR_B Pin Pull-up Resistance | — | 37 | 75 | 150 | kΩ |
| REGENPUP | VREG_SEL Pin Pull-up Resistance | — | 37 | 75 | 150 | kΩ |
| VSMPS | Internal switched regulator output voltage | Load Current from 10 mA to 1.8 A | 1.19 | 1.255 | 1.35 | V |
| FSMPS | Internal switched regulator operating frequency without modulation | Untrimmed | 0.65 | 1.00 | 1.35 | MHz |
| | | Trimmed | 0.93 | 1.00 | 1.07 | MHz |
| FSMPS-M7.5 | Internal switched regulator frequency modulation | — | — | 7.5 | — | % |
| FSMPS-M15 | | — | — | 15 | — | % |
| FSMPS-M30 | | — | — | 30 | — | % |

*Table continues on the next page...*

## Table 5. Voltage regulator electrical specifications (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VREGSWPUP | Internal switched regulator gate-driver pull-up resistance | maskset 0N38M,0N76P, 1N76P | 10 | 20 | 50 | kOhm |
| | | maskset 2N76P[1] | - | - | - | |
| VREF_BG_T | PMC bandgap reference voltage for SARADC | Trimmed | 1.20 | 1.22 | 1.237 | V |
| Vih (VREG_POR_B) | VREG_POR_B pin High Voltage level | — | 0.7*VDD_HV_PMU | — | VDD_HV_PMU + 0.3 | V |
| Vil (VREG_POR_B) | VREG_POR_B pin Low Voltage level | — | -0.3 | — | 0.3*VDD_HV_PMU | V |
| LVDAFER | Low Voltage Detection 3.3V Release (AFE VDD_HV_DAC and VDD_HV_RAW supplies) | maskset 0N76P, 1N76P, and 2N76P | 2.75 | 2.80 | 2.90 | V |
| | | maskset 0N38M | 2.78 | 2.86 | 3.00 | |
| LVDAFEE | Low Voltage Detection 3.3V Engage (AFE VDD_HV_DAC and VDD_HV_RAW supplies) | maskset 0N76P, 1N76P, and 2N76P | 2.68 | 2.77 | 2.86 | V |
| | | maskset 0N38M | 2.77 | 2.85 | 2.90 | |

1. There is a strong pull up from VREG_SWP to VDD_HV_REG3V8 which is connected when SMPS is disabled. The pullup has resistance less than 1Kohm, therefore VREG_SWP should not be connected to ground if unused.

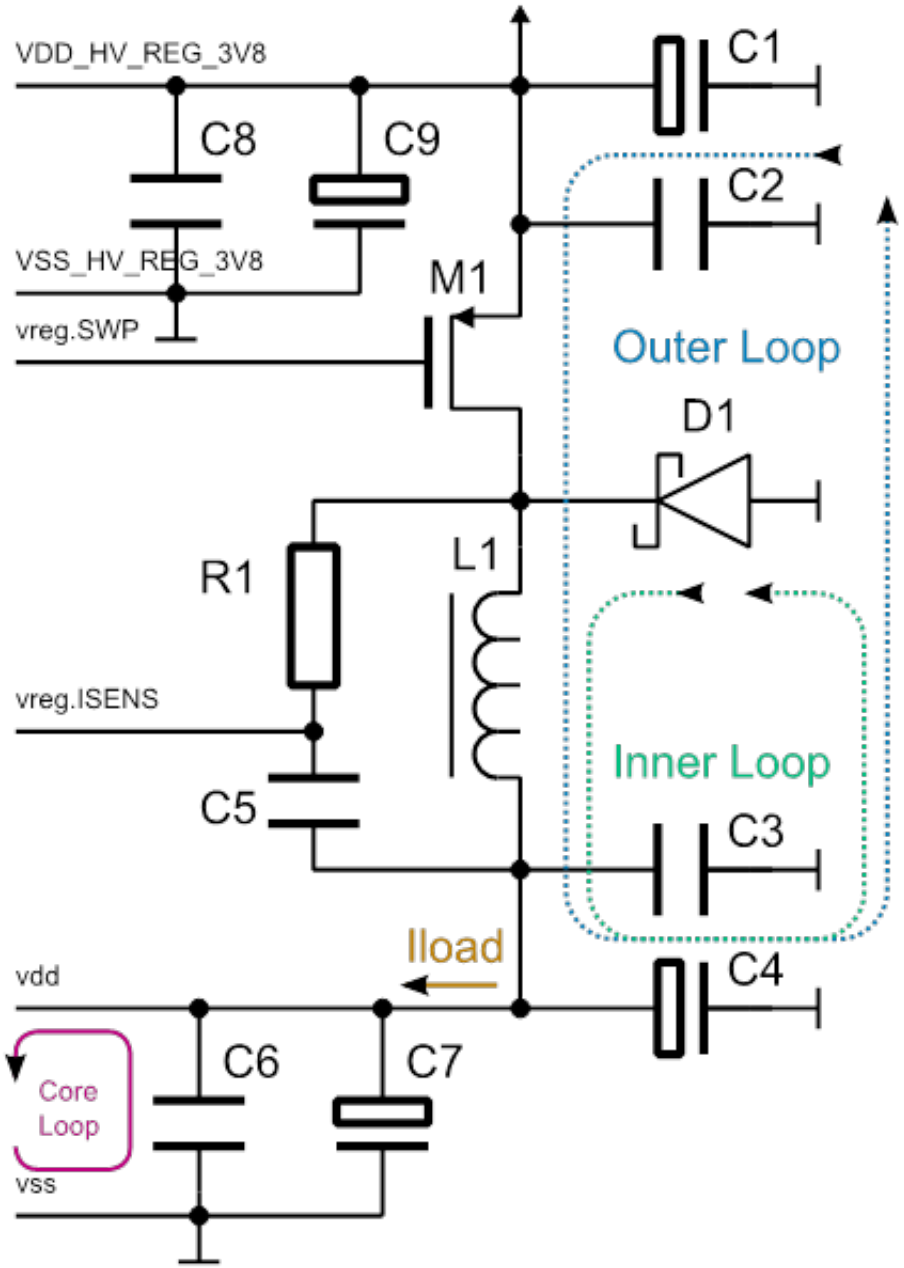



**Figure 2. SMPS External Components Configuration**

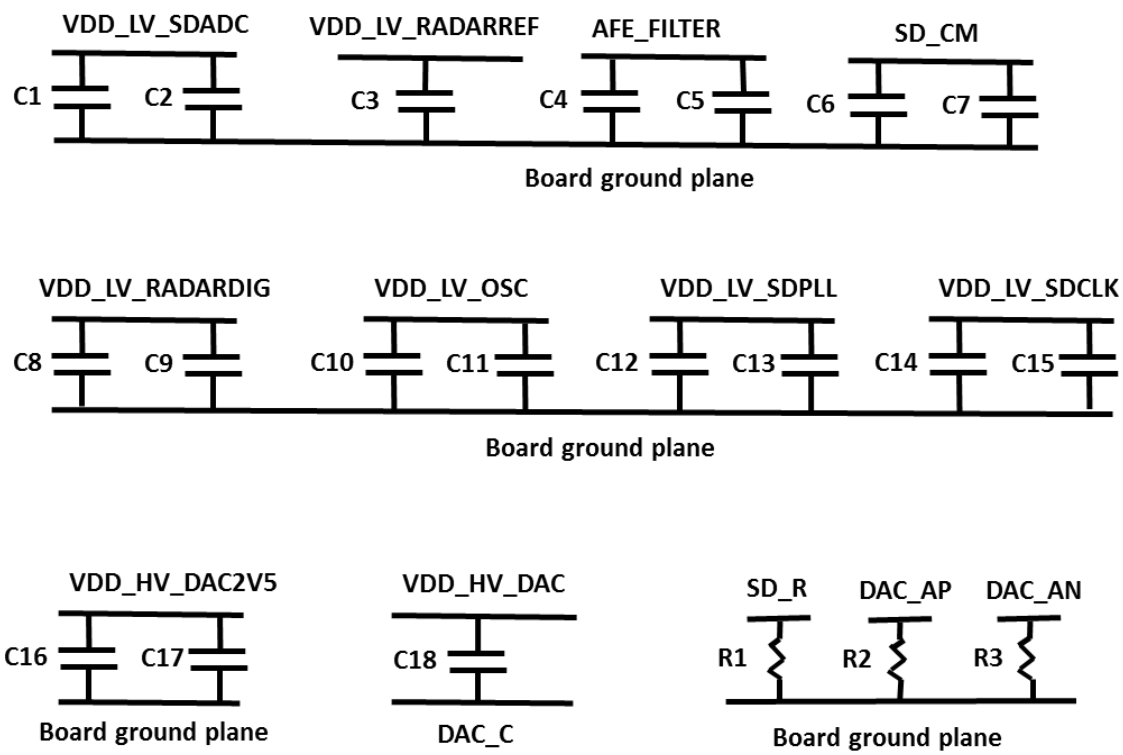
**Table 6. SMPS External Components**

| Ref | Description |
|---|---|
| M1 | SI3443, 2SQ2315 |
| L1 | 2.2 µH 3A < 100 mΩ series resistance (Ex. Bourns SRU8043-2R2Y) |
| D1 | SS8P3L 8A Schottcky Diode |
| R1 | 240 kΩ |
| C1 | 10 µF Ceramic |
| C2 | 100 nF Ceramic |

*Table continues on the next page...*

## Table 6. SMPS External Components (continued)

| Ref | Description |
|---|---|
| C3 | 100 nF Ceramic (place close to inductor) |
| C4 | 10 uF Ceramic (place close to inductor) |
| C5 | 100 pF Ceramic |
| C6 | 4 x 100 nF + 4 x 10nF Ceramic (place close to MCU supply pins) |
| C7 | 4 x 10 µF Ceramic (place close to MCU supply pins) |
| C8 | 100 nF Ceramic |
| C9 | 1 µF Ceramic (Unless C1 is really close to the pin) |




## Figure 3. Radar AFE External Components Configuration

## Table 7. Radar AFE External Components

| Component | Component Value | Tolerance | Placement Priority of larger cap. [1] | Placement Priority of smaller cap[1] | Special notes |
|---|---|---|---|---|---|
| C1 | 0.47µF | ±35% | 3 | — | — |
| C2 | 0.1µF | ±35% | — | 1 | — |
| C3 | 1.0µF | ±35% | 7 | — | — |
| C4 | 1.0µF | ±35% | 2 | — | — |
| C5 | 0.1µF | ±35% | — | 4 | — |
| C6 | 1.0µF | ±35% | 8 | — | — |

*Table continues on the next page...*

**Table 7. Radar AFE External Components (continued)**

| Component | Component Value | Tolerance | Placement Priority of larger cap. [1] | Placement Priority of smaller cap[1] | Special notes |
|---|---|---|---|---|---|
| C7 | 0.1µF | ±35% | — | 6 | — |
| C8 | 1.0µF | ±35% | 6 | — | — |
| C9 | 0.1µF | ±35% | — | 5 | — |
| C10 | 1.0µF | ±35% | 4 | — | — |
| C11 | 0.1µF | ±35% | — | 2 | — |
| C12 | 1.0µF | ±35% | 5 | — | — |
| C13 | 0.1µF | ±35% | — | 3 | — |
| C14 | 1.0µF | ±35% | 10 | — | — |
| C15 | 0.1µF | ±35% | — | 8 | — |
| C16 | 1.0µF | ±35% | 9 | — | — |
| C17 | 0.1µF | ±35% | — | 7 | — |
| C18 | 10µF | — | 1 | — | X7R type |
| C19 | 220nF | — | — | — | Sigma Delta ADC input capacitor. See Figure 9 |
| C20 | 220nF | — | — | — | Sigma Delta ADC input capacitor. See Figure 9 |
| R1 | 40.2kΩ | ±0.1% | — | — | tempco = 25ppm/C |
| R2 | 300Ω | — | — | — | DAC RI See Table 25 |
| R3 | 300Ω | — | — | — | DAC RI See Table 25 |
| Crystal | 40MHz | — | — | — | Connected between XOSC_EXTAL/ XOSC_XTAL, ESR ≤ 30Ω |

1. All Radar AFE external bypass capacitors should be placed as close as possible to the associated package pin. As shown in Radar AFE External Components Configuration, most pins have two values of bypass capacitor. >0.1 µF is referred to as the larger cap. 0.1 µF is referred to as the smaller cap

## 4.5 Electromagnetic Interference (EMI) characteristics

**Table 8. EMI emission testing specifications**

| Parameter | Conditions | Clocks | Frequency Range | Level (Typ) | Unit |
|---|---|---|---|---|---|
| VEME | Device Configuration, test conditions and EM testing per standard IEC 61967-2;<br>Supply voltages:<br>VDD_HV_REG3V8 = 3.8V | FSYS = 133 MHz<br>FBUS = 133 MHz<br>External Crystal = 40 MHz | 150 kHz – 50 MHz | 16 | dBuV |
| | | | 50 MHz – 150 MHz | 19 | |
| | | | 150 MHz – 500 MHz | 25 | |
| | | | 500 MHz – 1000 MHz | 16 | |
| | | | IEC Level | K | |

**Table 8. EMI emission testing specifications**

| Parameter | Conditions | Clocks | Frequency Range | Level (Typ) | Unit |
|---|---|---|---|---|---|
| | VDD33 = 3.3V<br>VDD = 1.25V<br>Temp = 25°C | | | | |

**NOTE**

1. Measurements were made per IEC 61967-2 while the device was running typical application code.
2. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
3. IEC Level Maximums: M ≤ 18 dBmV, L ≤ 24 dBmV, K ≤ 30 dBmV

## 4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × ($n$ + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

**NOTE**

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table 9. ESD ratings**

| No. | Symbol | Parameter | Conditions[1] | Class | Max value[2] | Unit |
|---|---|---|---|---|---|---|
| 1 | $V_{ESD(HBM)}$ | Electrostatic discharge (Human Body Model) | $T_A$ = 25 °C conforming to AEC-Q100-002 | H1C | 2000 | V |
| 2 | $V_{ESD(CDM)}$ | Electrostatic discharge (Charged Device Model) | $T_A$ = 25 °C conforming to AEC-Q100-011 | C3A | 500 [3]<br>750 (corners) | V |

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.
3. 500v for non AFE pins, 400v for AFE pins. "AFE pins" here are not just pins labeled as such in the Muxing Ballmap spreadsheet attached to the Reference Manual but also includes the associated power and grounds for the AFE block. Pin A1 (VSS_HV_RAW) is considered an AFE pin and not a corner pin.

# 5 I/O Parameters

## 5.1 DC electrical characteristics @ 3.3V Range

NMI, TCK, TMS, JCOMP are treated as GPIO.

**Table 10. GPIO DC electrical specifications**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Vih_hys | CMOS Input Buffer High Voltage (with hysteresis enabled) | 0.65*$V_{DD\_HV\_IO}$ | $V_{DD\_HV\_IO}$ + 0.3 | V |
| Vil_hys | CMOS Input Buffer Low Voltage (with hysteresis enabled) | -0.3 | 0.35*$V_{DD\_HV\_IO}$ | V |
| Vih | CMOS Input Buffer High Voltage (with hysteresis disabled) | 0.55 * $V_{DD\_HV\_IO}$ | $V_{DD\_HV\_IO}$ + 0.3 | V |
| Vil | CMOS Input Buffer Low Voltage (with hysteresis disabled) | -0.3 | 0.40 * $V_{DD\_HV\_IO}$ | V |
| Vhys | CMOS Input Buffer Hysteresis | 0.1 * $V_{DD\_HV\_IO}$ | — | V |
| $Vih_{TTL}$ | TTL Input high level voltage (All SAR_ADC input pins) | 2 | $V_{DD\_HV\_ADCREFx}$ + 0.3 | V |
| $Vil_{TTL}$ | TTL Input low level voltage (All SAR_ADC input pins) | -0.3 | 0.56 | V |
| $Vhyst_{TTL}$ | TTL Input hysteresis voltage (All SAR_ADC input pins) | 0.3 | — | V |
| Pull_Ioh | Weak Pullup Current[1] | 10 | 50 | µA |
| Pull_Iol | Weak Pulldown Current[2] | 10 | 50 | µA |
| Iinact_d | Digital Pad Input Leakage Current (weak pull inactive) [3] | -2.5 | 2.5 | µA |
| Voh | Output High Voltage[4] | 0.8 * $V_{DD\_HV\_IO}$ | — | V |
| Vol | Output Low Voltage[5] | — | 0.2 * $V_{DD\_HV\_IO}$ | V |
| Ioh_f | Full drive Ioh[6] (ipp_sre[1:0] = 11) | 18 | 70 | mA |
| Iol_f | Full drive Iol[6] (ipp_sre[1:0] = 11) | 21 | 120 | mA |
| Ioh_h | Half drive Ioh[6] (ipp_sre[1:0] = 10) | 9 | 35 | mA |
| Iol_h | Half drive Iol[6] (ipp_sre[1:0] = 10) | 10.5 | 60 | mA |

1. Measured when pad = 0 V
2. Measured when pad = $V_{DD\_HV\_IO}$
3. Specificed values no not apply to PD[7]. PD[7] leakage current specification are -15 µA min and 15 µA max.
4. Measured when pad is sourcing 2 mA
5. Measured when pad is sinking 2 mA
6. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

## 5.2 DC electrical characteristics @ 1.8V Range

**Table 11. 1.8 V Input Buffer DC Electrical Specifications**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Vih_hys | CMOS Input Buffer High Voltage (with hysteresis enabled) | 0.75*$V_{DD\_HV\_IO\_PDI}$ | $V_{DD\_HV\_IO\_PDI}$ + 0.3 | V |
| Vil_hys | CMOS Input Buffer Low Voltage (with hysteresis enabled) | -0.3 | 0.3*$V_{DD\_HV\_IO\_PDI}$ | V |
| Vih | CMOS Input Buffer High Voltage (with hysteresis disabled) | 0.65 * $V_{DD\_HV\_IO\_PDI}$ | $V_{DD\_HV\_IO\_PDI}$ + 0.3 | V |
| Vil | CMOS Input Buffer Low Voltage (with hysteresis disabled) | -0.3 | 0.40 * $V_{DD\_HV\_IO\_PDI}$ | V |
| Vhys | CMOS Input Buffer Hysteresis | 0.1 * $V_{DD\_HV\_IO\_PDI}$ | — | V |
| Pull_Ioh | Weak Pullup Current[1] | 1.5 | 35 | µA |
| Pull_Iol | Weak Pulldown Current[2] | 1.5 | 35 | µA |

1. Measured when pad = 0 V
2. Measured when pad = $V_{DD\_HV\_IO\_PDI}$

## 5.3 AC specifications@ 3.3 V Range

AC Parameters are specified over the full operating junction temperature range of -40°C to +150°C and for the full operating range of the $V_{DD\_HV\_IO}$ supply defined in Table 3.

**Table 12. Functional Pad AC Specifications**

| Symbol | Prop. Delay (ns)[1] L>H/H>L | | Rise/Fall Edge (ns)[2] | | Drive Load (pF) | SIUL2_MSCR[SRC] |
|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | MSB,LSB |
| pad_sr_hv (output) | 2.5/2.5 | 7.5/7.5 | 0.7/0.6 | 3/3 | 50 | 11 |
| | 6.4/5 | 19.5/19.5 | 2.5/2.0 | 12/12 | 200 | |
| | 2.2/2.5 | 8/8 | 0.4/0.3 | 3.5/3.5 | 25 | 10 |
| | 2.9/3.5 | 11.5/11.5 | 1.0/0.8 | 6.5/6.5 | 50 | |
| | 11/8 | 35/31 | 6.5/3.0 | 25/21 | 200 | |
| | 8.3/9.6 | 45/45 | 4/3.5 | 25/25 | 50 | 01[3] |
| | 13.5/15 | 65/65 | 6.3/6.2 | 30/30 | 200 | |
| | 13/13 | 75/75 | 6.8/6 | 40/40 | 50 | 00[3] |
| | 21/22 | 100/100 | 11/11 | 51/51 | 200 | |
| pad_sr_hv (input)[4] | | 2/2 | | | | NA |

1. As measured from 50% of core side input to Voh/Vol of the output

2. Measured from 20% - 80% of output voltage swing
3. Slew rate control modes
4. Input slope = 2ns

**NOTE**

Data based on characterization results, not tested in production.

**Table 13. Functional Pad AC Specifications**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| pad_sr_hv(Cp) | Parasitic Input Pin Capacitance | 4.5 | 4.7 | 5.0 | pF |

## 5.4 AC specifications@ 1.8 V Range

AC Parameters are specified over the full operating junction temperature range of -40°C to +150°C and for the full operating range of the $V_{DD\_HV\_IO}$ supply defined in Table 3.

**Table 14. Functional Pad AC Specifications**

| Symbol | Prop. Delay (ns)[1] L>H/H>L | |
|---|---|---|
| | Min | Max |
| pad_sr_hv (input)[2] | | 3.5/3 |

1. As measured from 50% of core side input to Voh/Vol of the output
2. Input slope = 2ns

**NOTE**

Data based on characterization results, not tested in production.

## 5.5 Aurora LVDS driver electrical characteristics

**NOTE**

The Aurora interface is AC coupled, so there is no common-mode voltage specification.

**Table 15. Aurora LVDS driver electrical characteristics**

| Symbol | Parameter[1] | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $F_{TXRX}$ | Data rate | — | — | 1.25 | Gbps |

*Table continues on the next page...*

**Table 15. Aurora LVDS driver electrical characteristics (continued)**

| Symbol | Parameter[1] | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Transmitter Specifications | | | | | |
| $V_{diffout}$ | Differential output voltage swing (terminated) | +/- 400 | +/- 600 | +/- 800 | mV |
| $T_{rise}/T_{fall}$ | Rise/Fall time (10% - 90% of swing) | 60 | | | ps |
| Receiver Specifications | | | | | |
| $V_{diffin}$ | Differential voltage | +/- 100 | | +/- 800 | mV |
| Termination | | | | | |
| $R_{V\_L}$ | Terminating Resistance (external) | 99 | 100 | 101 | Ohms |
| $C_P$ | Parasitic Capacitance (pad + bondwire + pin) | | | 1 | pF |
| $L_P$ | Parasitic Inductance | | | 7 | nH |
| STARTUP | | | | | |
| $T_{STRT\_BIAS}$ | Bias startup time[2] | — | — | 5 | µs |
| $T_{STRT\_TX}$ | Transmitter startup time[2] | — | — | 5 | µs |
| $T_{STRT\_RX}$ | Receiver startup time[2] | — | — | 5 | µs |
| LVDS_RXOUT[3] | Receiver o/p duty cycle | 30 | | 70 | % |

1. Conditions for these values are $V_{DD\_LV\_IO\_AURORA}$ = 1.19V to 1.32V, $T_J$ = –40 / 150 °C
2. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
3. Receiver o/p duty cycle is measured with 1.25Gbps, 50% duty cycle, max 1ns rise/fall time, 100mV voltage swing signal applied at the receiver input

## 5.6 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET_B pin.

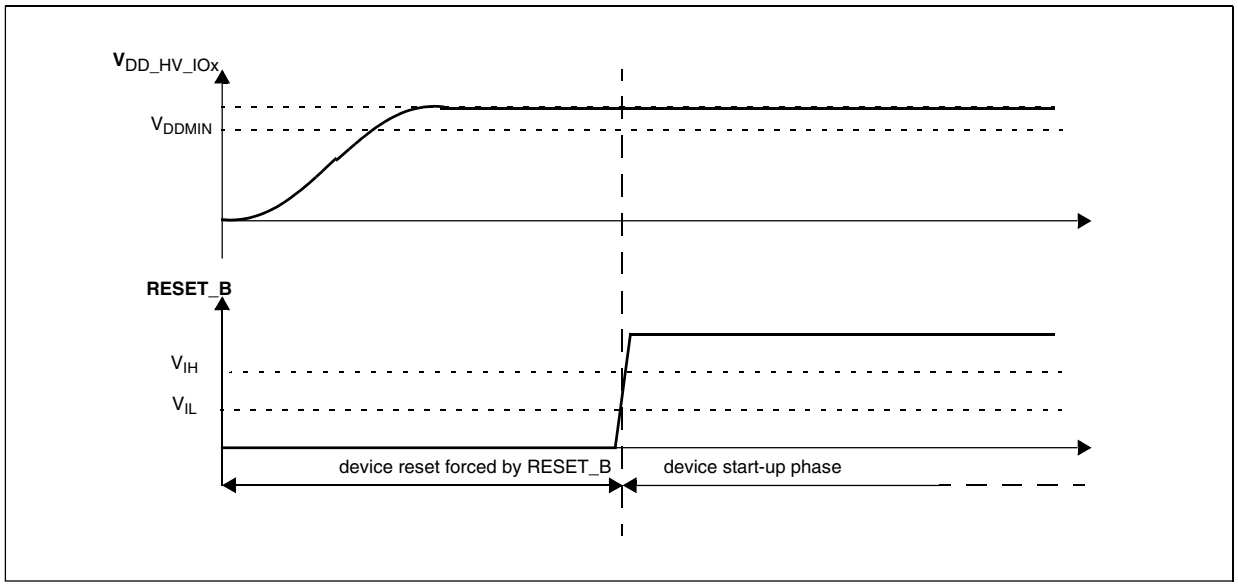



**Figure 4. Start-up reset requirements**

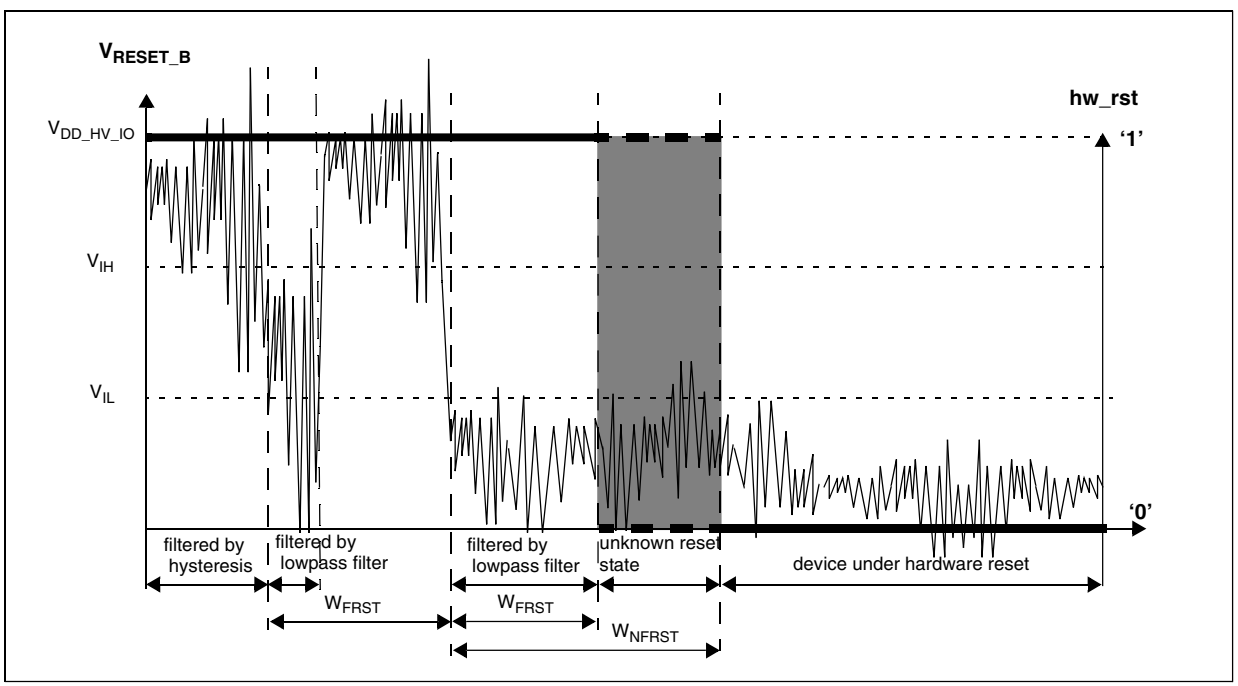



**Figure 5. Noise filtering on reset signal**

## Table 16. RESET_B electrical characteristics

| Symbol | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | Input high level TTL (Schmitt Trigger) | — | 2.0 | — | $V_{DD\_HV\_IOx}$ + 0.4 | V |
| $V_{IL}$ | Input low level TTL (Schmitt Trigger) | — | –0.4 | — | 0.56 | V |
| $V_{HYS}$,[2] | Input hysteresis TTL (Schmitt Trigger) | — | 300 | — | — | mV |

*Table continues on the next page...*

**Table 16. RESET_B electrical characteristics (continued)**

| Symbol | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{OL\_R}$ | Strong pull-down current | Device under power-on reset<br>$V_{DD\_HV\_IO}$=1.2 V<br>$V_{OL}$ = 0.35*$V_{DD\_HV\_IO}$ | 0.2 | — | — | mA |
| | | Device under power-on reset<br>$V_{DD\_HV\_IO}$=3.0 V<br>$V_{OL}$ = 0.35*$V_{DD\_HV\_IO}$ | 15 | — | — | mA |
| $W_{FRST}$ | (RESET_B)-input filtered pulse | — | — | — | 500 | ns |
| $W_{NFRST}$ | (RESET_B)-input not filtered pulse | — | 2400 | — | — | ns |
| $\|I_{WPD}\|$ | Weak pull-down current absolute value | $V_{IN}$ = $V_{DD\_HV\_IOx}$ | 30 | — | 100 | µA |

1. $V_{DD\_HV\_IOx}$ = 3.3 V -5%,+10%, $T_J$ = –40 / 150°C, unless otherwise specified
2. Data based on characterization results, not tested in production

# 6 Peripheral operating requirements and behaviours

## 6.1 Clocks and PLL Specifications

### 6.1.1 40 MHz Oscillator (XOSC) electrical characteristics

The device provides an oscillator/resonator driver.

**NOTE**

XTAL/EXTAL must not be directly used to drive external circuits.

**Table 17. XOSC electrical characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $XOSC_{fout}$ | Oscillator frequency | | | 40 | | MHz |
| $t_{stab}$ | Oscillator start-up time | | | | 2 | ms |
| $T_{jitcc}$ | Cycle to cycle jitter (peak – peak) | — | | | 2.5 | ps |
| | Output Duty Cycle | | 45 | 50 | 55 | % |
| Cin | Input Capacitance | Extal and Xtal each | 8.9 | 10.4 | 11.9 | pF |
| $PN_{XOSC}$ | Phase Noise | @ 100 Hz | | | -92 | dBc/Hz |
| | | @ 1 KHz | | | -112 | |

*Table continues on the next page...*

**Table 17. XOSC electrical characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | @ 10 KHz | | | -132 | |
| | | @ 40 KHz | | | -142 | |
| | | @ 100 KHz | | | -147 | |

## 6.1.2 FMPLL electrical characteristics

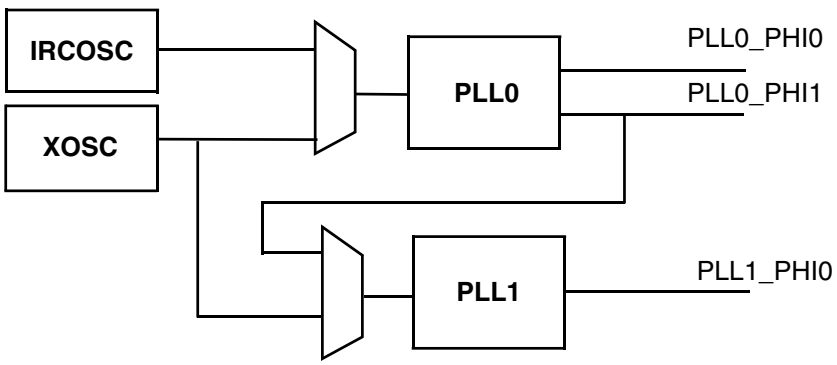



**Figure 6. PLL integration**

**Table 18. PLL0 electrical characteristics**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL0IN}$ | PLL0 input clock[2, 3] | — | 14 | — | 44 | MHz |
| $\Delta_{PLL0IN}$ | PLL0 input clock duty cycle[2] | — | 40 | — | 60 | % |
| $f_{PLL0VCO}$ | PLL0 VCO frequency | — | 600 | — | 1250 | MHz |
| $f_{PLL0PHI0}$ | PLL0 output clock PHI0 | — | 4.76 | — | 625[4] | MHz |
| $f_{PLL0PHI1}$ | PLL0 output clock PHI1 | — | 20 | — | 156 | MHz |
| $t_{PLL0LOCK}$ | PLL0 lock time | — | — | — | 100 | µs |
| $\Delta_{PLL0LTJ}$ | PLL0 long term jitter $f_{PLL0IN}$ = 8 MHz (resonator)[5] | $f_{PLL0PHI0}$ = 40 MHz, 1 µs | | | ± 1 | ns |
| | | $f_{PLL0PHI0}$ = 40 MHz, 13 µs | | | ± 1 | ns |
| $I_{PLL0}$ | PLL0 consumption | | — | — | 5 | mA |

1. $V_{DD\_LV\_PLL0}$ =1.25 V ± 5%, $T_J$ = -40 / 150 °C unless otherwise specified.
2. PLL0IN clock retrieved directly from either IRCOSC or external XOSC clock.
3. fPLL0IN frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure the reference clock to the PLL analog loop is in the range 8MHz-20MHz
4. The maximum clock outputs are limited by the design clock frequency requirements as per recommended operating conditions.
5. $V_{DD\_LV\_PLL0}$ noise due to application in the range $V_{DD\_LV\_PLL0}$ = 1.25 V±5%, with frequency below PLL bandwidth (40 kHz) will be filtered

**Table 19. FMPLL1 electrical characteristics**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL1IN}$ | PLL1 input clock[2] | — | 38 | — | 78 | MHz |
| $\Delta_{PLL1IN}$ | PLL1 input clock duty cycle[2] | — | 35 | — | 65 | % |
| $f_{PLL1VCO}$ | PLL1 VCO frequency | — | 600 | — | 1250 | MHz |
| $f_{PLL1PHI0}$ | PLL1 output clock PHI0 | — | 4.76 | — | 625 | MHz |
| $t_{PLL1LOCK}$ | PLL1 lock time | — | — | — | 100 | µs |
| $f_{PLL1MOD}$ | PLL1 modulation frequency | — | — | — | 250 | kHz |
| $\lvert\delta_{PLL1MOD}\rvert$ | PLL1 modulation depth (when enabled) | Center spread | 0.25 | — | 2 | % |
| | | Down spread | 0.5 | — | 4 | % |
| $I_{PLL1}$ | PLL1 consumption | | — | — | 6 | mA |

1. $V_{DD\_LV\_PLL0}$ = 1.25 V ± 5%, $T_J$ = -40 / 150°C unless otherwise specified.
2. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock.

## 6.1.3 16 MHz Internal RC Oscillator (IRCOSC) electrical specifications

**Table 20. Internal RC Oscillator electrical specifications**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{Target}$ | IRC target frequency | — | — | 16 | — | MHz |
| $F_{untrimmed}$ | IRC frequency (untrimmed) | — | 9.6 | — | 24 | MHz |
| $\delta F_{var}$ | IRC trimmed frequency variation [1] | — | -8 | — | 8 | % |
| $T_{startup}$ | Startup time | | — | — | 5 | µs |
| $I_{VDD3}$ | Current consumption on 3.3 V power supply ($V_{DD\_HV\_IO}$) | After $T_{startup}$ | — | — | 55 | µA |
| $I_{VDD12}$ | Current consumption on 1.25 V power supply ($V_{DD\_LV\_COR}$) | After $T_{startup}$ | — | — | 270 | µA |

1. The typical user trim step size ($\delta f_{TRIM}$) is 0.3% of current frequency for application of positive trim and 0.26% of current frequency for application of negative trim, based on characterization results.

## 6.1.4 320 MHz AFE PLL

**Table 21. 320 MHz AFE PLL parameters**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $PLL_{fout}$ | Output Frequency | | — | 320 | — | MHz |
| $N_{PLL}$<br>@100 Hz<br>@1 kHz<br>@10 kHz<br>@100 kHz | Phase Noise | | — | — | <br>-54<br>-74<br>-94<br>-114 | dBc/Hz |
| $t_{cal}$ | Calibration Time | LW64 = 1 | — | — | 150 | µs |

*Table continues on the next page...*

**Table 21. 320 MHz AFE PLL parameters (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | LW64 = 0 | | | 500 | |
| $t_{lock}$ | Lock Time | after calibration | — | — | 75 | µs |
| $t_{jitcc}$ | Cycle to cycle jitter (peak – peak) | | — | — | 10 | ps |
| | Output Duty Cycle | | 48 | 50 | 52 | % |

## 6.1.5 LFAST PLL electrical characteristics

The specifications in the following table apply to the interprocessor bus LFAST interface.

**Table 22. LFAST PLL electrical characteristics**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{RF\_REF}$ | PLL reference clock frequency | — | 10 | — | 26 | MHz |
| $ERR_{REF}$ | PLL reference clock frequency error | — | –1 | — | 1 | MHz |
| $DC_{REF}$ | PLL reference clock duty cycle | — | 45 | — | 55 | % |
| PN | Integrated phase noise (single side band) | $f_{RF\_REF}$ = 20 MHz | — | — | –58 | dBc |
| | | $f_{RF\_REF}$ = 10 MHz | — | — | –64 | |
| $f_{VCO}$ | PLL VCO frequency | — | — | 640[1] | — | MHz |
| $t_{LOCK}$ | PLL phase lock[2] | — | — | — | 40 | µs |
| $\Delta PER_{REF}$ | Input reference clock jitter (peak to peak) | Single period, $f_{RF\_REF}$ = 10 MHz | — | — | 300 | ps |
| | | Long term, $f_{RF\_REF}$ = 10 MHz | –500 | — | 500 | |
| $\Delta PER_{EYE}$ | Output Eye Jitter (peak to peak)[3] | Random Jitter (Rj) | — | 84 | 101 | ps |
| | | Deterministic Jitter (Dj) | — | 80 | 96 | ps |
| | | Total Jitter @BER $10^{-9}$ | — | 1.09 | 1.31 | bits per second |
| $I_{VDD\_LV\_LFASTPLL}$ | $V_{DD\_LV\_LFASTPLL}$ Supply Current | Normal Mode | — | 6 | 10 | mA |
| | | Peak | — | 7 | 11 | mA |
| | | Power Down | — | 0.5 | 27 | µA |

1. The 640 MHz frequency is achieved with a 10 MHz or 20 MHz reference clock. With a 26 MHz reference, the VCO frequency is 624 MHz.
2. The time from the PLL enable bit register write to the start of phase locks is maximum 2 clock cycles of the peripheral bridge clock that is connected to the PLL on the device.
3. Measured at the transmitter output across a 100 Ω termination resistor on a device evaluation board.

# 6.2 Analog

## 6.2.1 ADC electrical characteristics

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

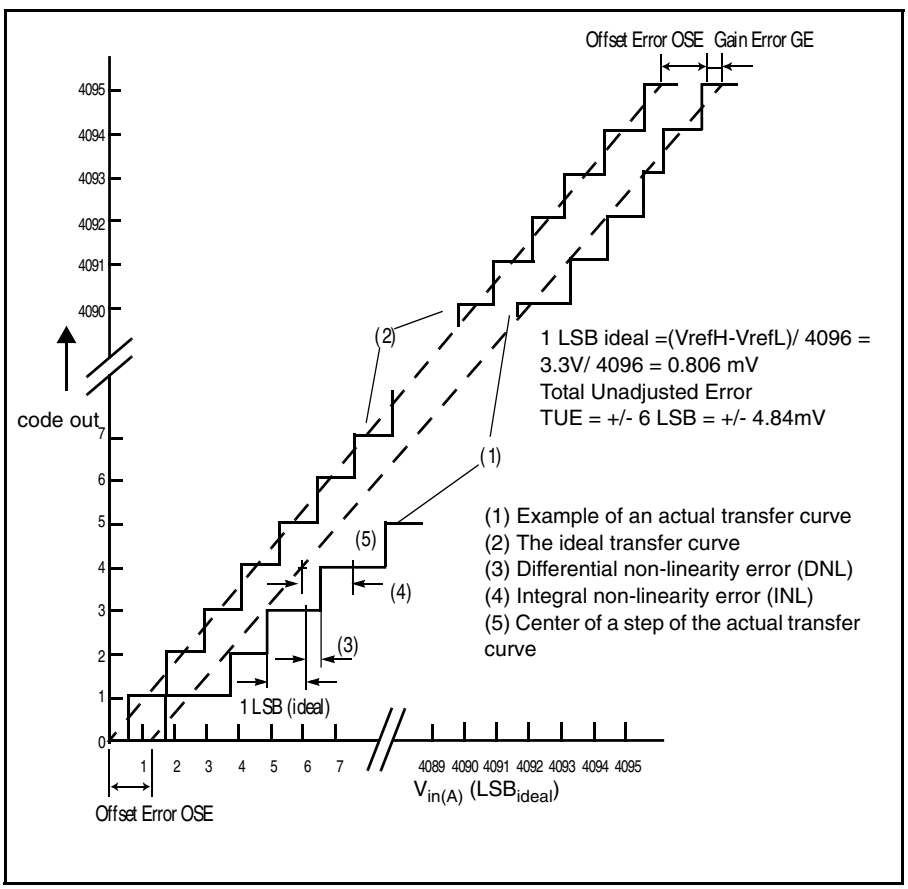



**Figure 7. ADC characteristics and error definitions**

### 6.2.1.1 Input equivalent circuit

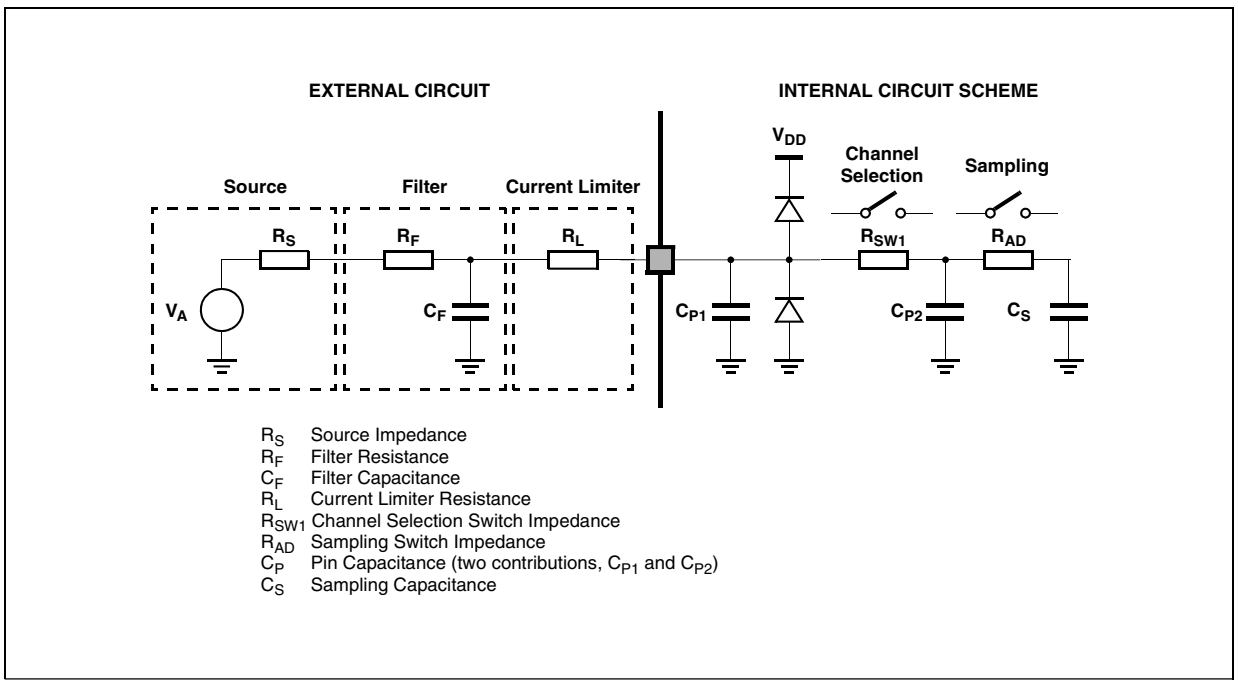



**Figure 8. Input equivalent circuit**

**Table 23. ADC conversion characteristics**

| Symbol | Parameter | Conditions[1, 2] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CK}$ | ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[3] frequency.) | — | 20 | 80 | 80 | MHz |
| $f_s$ | Sampling frequency | — | — | — | 1.00 | MHz |
| $t_{sample}$ | Sample time[4] | — | 250 | — | — | ns |
| $t_{sampleC}$ | SAR selftest C-algorithm sample time | — | 300 | — | — | ns |
| $t_{sampleS}$ | SAR selftest S-algorithm sample time | — | 1 | — | — | µs |
| $t_{sampleBG}$ | Bandgap sample time | — | 1.87 | — | — | µs |
| $t_{sampleTS}$ | Temperature sensor sample time | — | 3.18 | — | — | µs |
| $t_{conv}$ | Conversion time[5] | 80 MHz | 700 | — | — | ns |
| $C_{S'}$[6] | ADC input sampling capacitance | — | — | 3 | 5 | pF |
| $C_{P1}$[6] | ADC input pin capacitance 1 | — | — | — | 5 | pF |
| $C_{P2}$[6] | ADC input pin capacitance 2 | — | — | — | 0.8 | pF |
| $R_{SW1}$[6] | Internal resistance of analog source | $V_{REF}$ range = 3.0 to 3.6 V | — | — | 875 | Ω |
| $R_{AD}$[6] | Internal resistance of analog source | — | — | — | 825 | Ω |
| INL | Integral non-linearity | — | –2 | — | 2 | LSB |
| DNL | Differential non-linearity[7] | — | –1 | — | 1 | LSB |
| OFS | Offset error | — | –4 | — | 4 | LSB |
| GNE | Gain error | — | –4 | — | 4 | LSB |
| $TUE_{IS1WINJ}$ | Total unadjusted error for IS1WINJ | — | –6 | — | 6 | LSB |

*Table continues on the next page...*

## Table 23. ADC conversion characteristics (continued)

| Symbol | Parameter | Conditions[1, 2] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $TUE_{IS1WWINJ}$ | Total unadjusted error for IS1WWINJ | — | –6 | — | 6 | LSB |
| IS1WINJ (pad going to one ADC) | (single ADC channel) | — | | | | |
| | Max leakage | 150 °C | — | — | 250 | nA |
| | Max positive/negative injection[8] | — | –3 | — | 3[9] | mA |
| IS1WWINJ (pad going to two ADCs) | (double ADC channel) | — | | | | |
| | Max leakage | 150 °C | — | — | 300 | nA |
| | Max positive/negative injection [8] | \|Vref_ad0 - Vref_ad1\| < 150 mV | –3.6 | — | 3.6 | mA |
| SNR | Signal-to-noise ratio | 3.3 V reference voltage | 67 | — | — | dB |
| THD | Total harmonic distortion | @ 125 kHz | 65 | — | — | dB |
| ENOB | Effective number of bits | Fin < 125 kHz | 10.5 | — | — | bits |
| SINAD | Signal-to-noise and distortion[10] | Fin < 125 kHz | 65 | — | — | dB |

1. $V_{DD\_HV\_ADC}$ = 3.3 V -5%,+10%, $T_J$ = –40 to +150°C, unless otherwise specified and analog input voltage from $V_{AGND}$ to $V_{DD\_HV\_ADCREFx}$.
2. Performance specifications achieved with a full-scale input
3. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
4. During the sample time the input capacitance $C_S$ can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_{sample}$. After the end of the sample time $t_{sample}$, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock $t_{sample}$ depend on programming.
5. This parameter does not include the sample time $t_{sample}$, but only the time for determining the digital result and the time to load the result register with the conversion result.
6. See Input equivalent circuit.
7. No missing codes.
8. ADC specifications are met only if injection is within these specified limits
9. Max injection current for all ADC IOs is ± 10 mA
10. SINAD = (6.02 × ENOB) + 1.76

**NOTE**

The ADC performance specifications are not guaranteed if two or more ADCs simultaneously sample the same shared channel.

**NOTE**

General Purpose Input (GPI) functionality should not be used on any of the SAR-ADC channels when SARADC is functional.

### 6.2.2 Sigma Delta ADC

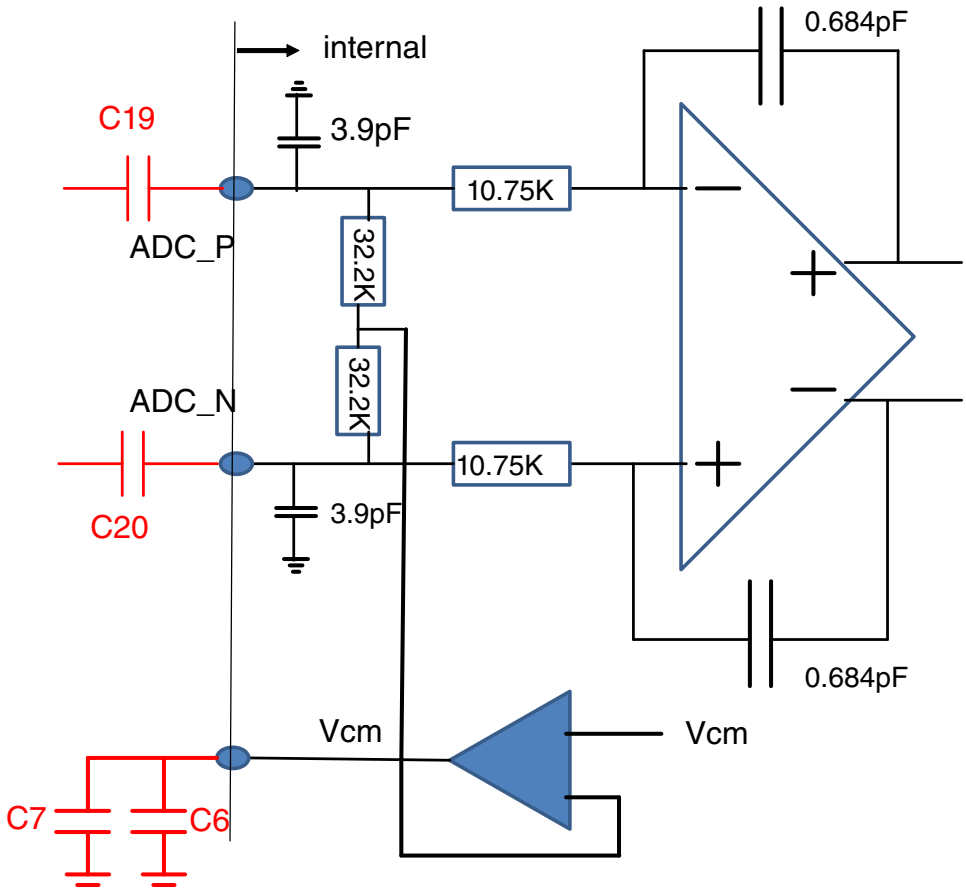



**Figure 9. ADC0-6 input equivalent circuit**

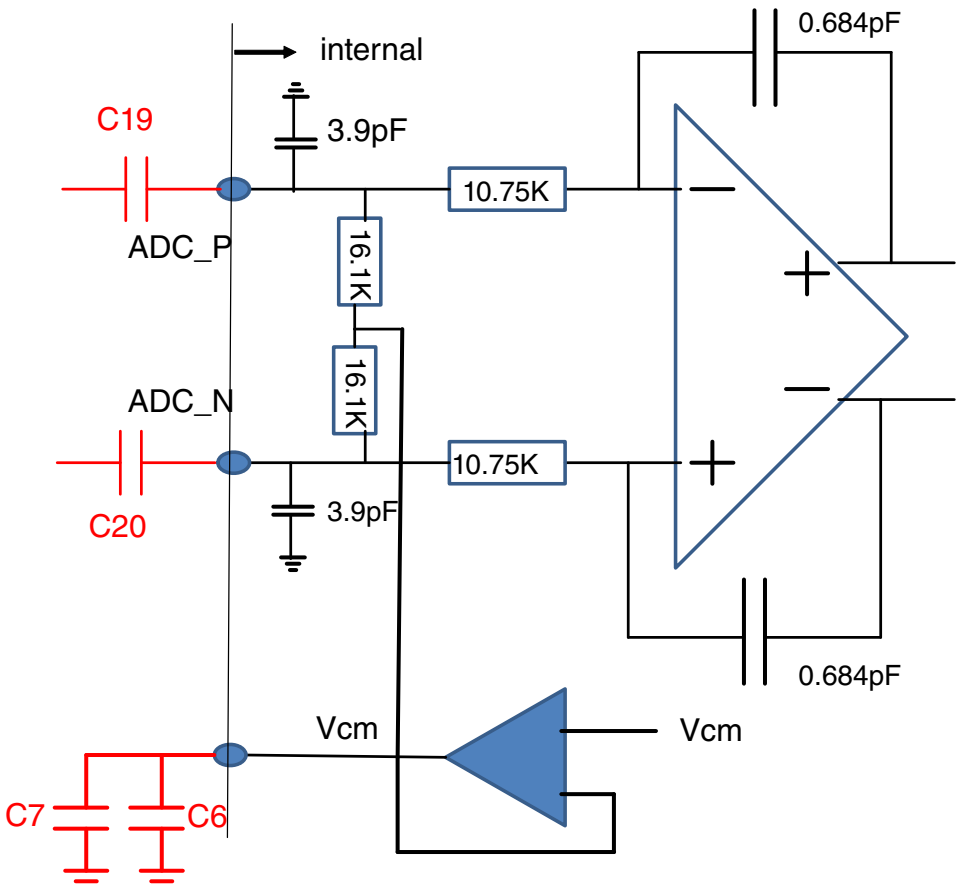



**Figure 10. ADC7 input equivalent circuit**

**Table 24. Sigma Delta ADC Parameters**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $SPS_{SDA}$ | Sample Rate | After Decimation Filtering | — | 10 | 10 | MS/S |
| $L_{SDA}$ | Latency | @ 10 MS/s, full step input to 50% output. Decimation filter delay not included | — | — | 0.1 | µS |
| $RT_{SDA}$ | Recovery Time | After overload condition | — | — | 0.5 | µS |
| $SNR_{SDA\_MM\_ON}$ | Signal-to-Noise Ratio Mismatch shaper on | Input Frequency Range and integration bandwidth are from 20kHz to 5MHz. Characterized under the following conditions: 1.2Vpp input signals at the following frequencies are applied one at a time: 20.77 KHz, 317.7 KHz, 857.7 KHz, 1.411 MHz, 2.95 MHz, 3.897 MHz, and 4.997 MHz and the SNR calculated. SNR at 5 MHz will be reduced by 5 dB due to decimation filter roll off. The SNR is specified to be 67 dBFS typical for input frequencies between 20 KHz and 4 MHz. Mismatch shaper on. | 65 | 67 | — | dBFS |
| $SNR_{SDA\_MM\_OFF}$ | Signal-to-Noise Ratio Mismatch shaper off | Input Frequency Range and integration bandwidth are from 20kHz to 5MHz. Characterized under the following conditions: 1.2Vpp input signals at the following frequencies are applied one at a time: | 66 | 67 | — | dBFS |

*Table continues on the next page...*

## Table 24. Sigma Delta ADC Parameters (continued)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 20.77 KHz, 317.7 KHz, 857.7 KHz, 1.411 MHz, 2.95 MHz, 3.897 MHz, and 4.997 MHz and the SNR calculated. SNR at 5 MHz will be reduced by 5 dB due to decimation filter roll off. The SNR is specified to be 67 dBFS typical for input frequencies between 20 KHz and 4 MHz. Mismatch shaper off. | | | | |
| $SNDR_{SDA\_MM\_ON}$ | Signal-to-Noise-and-Distortion Ratio Mismatch shaper on | Input Frequency Range and integration bandwidth are from 20kHz to 5MHz. Characterized under the following conditions: 1.2Vpp input signals at the following frequencies are applied one at a time: 20.77 KHz, 317.7 KHz, 857.7 KHz, 1.411 MHz, 2.95 MHz, 3.897 MHz, and 4.997 MHz and the SNR calculated. SNR at 5 MHz will be reduced by 5 dB due to decimation filter roll off. The SNDR is specified to be 64 dBFS typical for input frequencies between 20 KHz and 4 MHz. Mismatch shaper on. | 62 | 64 | — | dBFS |
| $SNDR_{SDA\_MM\_OFF}$ | Signal-to-Noise-and-Distortion Ratio Mismatch shaper off | Input Frequency Range and integration bandwidth are from 20kHz to 5MHz. Characterized under the following conditions: 1.2Vpp input signals at the following frequencies are applied one at a time: 20.77 KHz, 317.7 KHz, 857.7 KHz, 1.411 MHz, 2.95 MHz, 3.897 MHz, and 4.997 MHz and the SNR calculated. SNR at 5 MHz will be reduced by 5 dB due to decimation filter roll off. The SNDR is specified to be 62 dBFS typical for input frequencies between 20 KHz and 4 MHz. Mismatch shaper off. | 60 | 62 | — | dBFS |
| $IFDR_{SDA}$ | Interference Free Dynamic Range | 20 ms integration, ADC inputs tied together at the package pin. One side of the AC coupling capacitors associated with each input should remain connected to the ADC input and the other side of the capacitor should connected to ground. | 90 | — | — | dBFS |
| $IMD_{SDA\_MM\_ON}$ | Intermodulation Distortion Mismatch Shaper on | Input Frequency Range and integration bandwidth are from 20kHz to 5MHz. Characterized under the following conditions: Two distinct sets of signal pairs at the specified frequencies and at an amplitude of -8 dBFs (i.e. 0.23886 Vpeak = 0.47772 Vpp differential) are applied one signal pair at a time. Signal pair #1 is f1 = 1 MHz and f2 = 1.1 MHz and signal pair #2 is f1 = 390.625 KHz and f2 = 546.875 KHz. All inter modulation products are checked. Mismatch Shaper on. | 64 | — | — | dBc |
| $IMD_{SDA\_MM\_OFF}$ | Intermodulation Distortion Mismatch Shaper off | Input Frequency Range and integration bandwidth are from 20kHz to 5MHz. Characterized under the following conditions: Two distinct sets of signal pairs at the specified frequencies and at an amplitude of -8 dBFs (i.e. 0.23886 Vpeak = 0.47772 Vpp differential) are applied one signal pair at a time. Signal pair #1 is f1 = 1 MHz and f2 = 1.1 MHz and signal pair #2 is f1 = 390.625 KHz and f2 = 546.875 KHz. All inter modulation products are checked. Mismatch Shaper off. | 60 | — | — | dBc |

*Table continues on the next page...*

## Table 24. Sigma Delta ADC Parameters (continued)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| GM | Gain Mismatching | (ADCx to ADCy) | –3.5 | — | 3.5 | % |
| OE | Input Offset Error | — | -25 | — | 25 | mV |
| OEV | Offset Variation | t = 50 ms, T = constant, Data averaged in 1ms increments | -0.07 | — | 0.07 | mV |
| Vcm | Common Mode Voltage | SDADC switched on or off | — | approx. vdda/2 | — | V |
| xtalk | Crosstalk (from any ADC to the other ADCs) | Processing a full scale signal. | — | — | -40 | dB |
| Zin (ADC0-6) | Input Impedance | Maximum input impedance occurs for input signals at 20 KHz and minimum input impedance occurs at input frequencies greater than 1 MHz [1] | 7.3 | — | 33.5 | kΩ |
| Zin (ADC7) | Input Impedance | Maximum input impedance occurs for input signals at 20 KHz and minimum input impedance occurs at input frequencies greater than 1 MHz [1] | 7.3 | — | 16.75 | kΩ |
| $R_{cm}$ (ADC0-6) | Resistance from each SDADC input to vcm (see Figure 9) | - | 27.3 | 32.2 | 37.0 | kΩ |
| $R_{cm}$ (ADC7) | Resistance from each SDADC input to vcm (see Figure 10) | - | 13.65 | 16.1 | 18.5 | kΩ |
| R_SDADC | Resistance from each SDADC input pin to differential amplifier input (see Figure 9 and Figure 10) | - | 9.0 | 10.75 | 12.5 | kΩ |
| C_SDADC | SDADC integrator capacitors (see Figure 9 and Figure 10) | - | 0.636 | 0.684 | 0.732 | pF |
| DT[2] | Analog Delay Variation | (ADCx to ADCy) | | — | 1 | ns |
| AA[3] | Alias Suppression | ADC input frequency between 315 and 325 MHz | 50 | — | — | dB |
| STFoob | ADC out of band Signal Transfer Function peaking | Out of band Signal Transfer function peaking from 20 MHz to 40 MHz | 0 | 2 | 3 | dB |
| PR | passband ripple | From 20 kHz to 4 MHz (default decimation filter coefficients must be used) | -0.5 | 0.0 | 0.5 | dB |
| OOBA[3] | Out Of Band Attenuation | Default decimation filter coefficients must be used<br>5 MHz<br>6 MHz<br>7 MHz<br>10 MHz<br>15 MHz | <br>-4.5<br>-10<br>-20<br>-40<br>-60 | — | — | dB |

1. The input structure of the ADC is an active RC integrator which has a frequency dependent input impedance as indicated above see ADC0-6 input equivalent circuit and ADC7 input equivalent circuit.

2. Analog Delay Variation between ADC channels is less than 1ns for channels 0 through 6. The channel 7 ADC has an additional fixed delay of approximately 2ns so the total variation in analog delay through ADC7 is 3ns or less relative to the other ADC channels.
3. All attenuation values are relative to 0dB in the ADC passband

## 6.2.3 DAC electrical specifications

**NOTE**

- All data is measured in single ended mode. Differential mode is guaranteed by design.
- Specifications guaranteed only if factory trims are not overridden.

**Table 25. DAC parameters**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $N_{BIT}$ | Bits | Base bits | — | 12 | — | Bits |
| $SPS_{DAC}$ | Sample rate | — | — | 2 | — | MSample s/s |
| DNL | Linearity[1, 2] | — | -24 | — | 4 | LSB |
| $V_{out}$ | Output Voltage[1, 3, 2] | Single-Ended, Rl = 300 Ω | 1.2 | — | 1.35 | V |
| $I_{out}$ | Full-Scale Output Current | DAC full-scale adjust bits set to 01 or 10 | 4.0 | — | 4.5 | mA |
| $N_{DAC}$ | DAC output noise[4, 1] | @250 kHz<br>@100 kHz<br>@10 kHz<br>@1 kHz | | — | 20<br>30<br>65<br>170 | nV/ sqrt(Hz) |
| SOE | Static Offset Error[1, 2] | Single-Ended<br>Differential with the full-scale adjust bits set to either 01 or 10[5] | 60<br>-30<br>0 | 75<br>0 | 100<br>30 | mV |
| TOE | Transient Offset Error[6, 1, 2] | After low-pass filter and averaging | — | — | 0.05 | LSB |
| $t_{DV}$ | Transient Time Delay Variation[7, 1, 2] | LSB step<br>MSB step | — | — | 1<br>10 | ns |
| Oc | Output compliance | single-ended, only the DNL specification is guaranteed. The TOE and Tdv may be degraded. | 0 | — | 1.35 | V |
| tempco | Temperature coefficient | — | –1 | — | 1.0 | LSB/K[2] |
| PSRR | Power Supply Rejection Ratio | Freq < 250kHz | 40 | — | — | dB |

1. DAC linearity, output swing, noise, TOE, and Tdv specifications are all based upon a 300 Ω DAC output load resistor and assume that the full-scale adjust bits are set to either 01 or 10. These specifications will NOT be met for other DAC output load resistor values.
2. Once all of the LVDs have cleared and the DAC is powered on, a one-time wait time of 300ms is required before the DAC output signal is valid.

3. The full-scale DAC output is trimmed to 1.30 V ±10 mV with all DAC inputs set to 1 including both full-scale adjust bits.
4. Rl = 300 Ω, 10uF capacitor between Vdd_HV_DAC and DAC_C, ideal supply
5. Differential offset measured with DAC code of 2047.
6. Difference between ideal and real (Va+Vb/2), for all base LSBs
7. Falling edge to falling edge or rising edge to rising edge. Any transition DACn -> DACn + 1

## 6.2.4 Flash memory program and erase specifications

**NOTE**

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 26 shows the estimated Program/Erase times.

**Table 26. Flash memory program and erase specifications**

| Symbol | Characteristic[1] | Typ[2] | Factory Programming[3, 4] | | Field Update | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Initial Max | Initial Max, Full Temp | Typical End of Life[5] | Lifetime Max[6] | | |
| | | | 20°C ≤$T_A$ ≤30°C | -40°C ≤$T_J$ ≤150°C | -40°C ≤$T_J$ ≤150°C | ≤ 1,000 cycles | ≤ 250,000 cycles | |
| $t_{dwpgm}$ | Doubleword (64 bits) program time | 43 | 100 | 150 | 55 | 500 | | µs |
| $t_{ppgm}$ | Page (256 bits) program time | 73 | 200 | 300 | 108 | 500 | | µs |
| $t_{qppgm}$ | Quad-page (1024 bits) program time | 268 | 800 | 1,200 | 396 | 2,000 | | µs |
| $t_{16kers}$ | 16 KB Block erase time | 168 | 290 | 320 | 250 | 1,000 | | ms |
| $t_{16kpgm}$ | 16 KB Block program time | 34 | 45 | 50 | 40 | 1,000 | | ms |
| $t_{32kers}$ | 32 KB Block erase time | 217 | 360 | 390 | 310 | 1,200 | | ms |
| $t_{32kpgm}$ | 32 KB Block program time | 69 | 100 | 110 | 90 | 1,200 | | ms |
| $t_{64kers}$ | 64 KB Block erase time | 315 | 490 | 590 | 420 | 1,600 | | ms |
| $t_{64kpgm}$ | 64 KB Block program time | 138 | 180 | 210 | 170 | 1,600 | | ms |
| $t_{256kers}$ | 256 KB Block erase time | 884 | 1,520 | 2,030 | 1,080 | 4,000 | — | ms |
| $t_{256kpgm}$ | 256 KB Block program time | 552 | 720 | 880 | 650 | 4,000 | — | ms |

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ $T_J$ ≤ 150°C, full spec voltage.

### 6.2.5 Flash memory Array Integrity and Margin Read specifications

**Table 27. Flash memory Array Integrity and Margin Read specifications**

| Symbol | Characteristic | Min | Typical | Max[1] | Units[2] |
|---|---|---|---|---|---|
| $t_{ai16kseq}$ | Array Integrity time for sequential sequence on 16 KB block. | — | — | 512 x Tperiod x Nread | — |
| $t_{ai32kseq}$ | Array Integrity time for sequential sequence on 32 KB block. | — | — | 1024 x Tperiod x Nread | — |
| $t_{ai64kseq}$ | Array Integrity time for sequential sequence on 64 KB block. | — | — | 2048 x Tperiod x Nread | — |
| tai256kseq | Array Integrity time for sequential sequence on 256 KB block. | — | — | 8192 x Tperiod x Nread | — |
| $t_{mr16kseq}$ | Margin Read time for sequential sequence on 16 KB block. | 73.81 | — | 110.7 | µs |
| $t_{mr32kseq}$ | Margin Read time for sequential sequence on 32 KB block. | 128.43 | — | 192.6 | µs |
| $t_{mr64kseq}$ | Margin Read time for sequential sequence on 64 KB block. | 237.65 | — | 356.5 | µs |
| $t_{mr256kseq}$ | Margin Read time for sequential sequence on 256 KB block. | 893.01 | — | 1,339.5 | µs |

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

### 6.2.6 Flash memory module life specifications

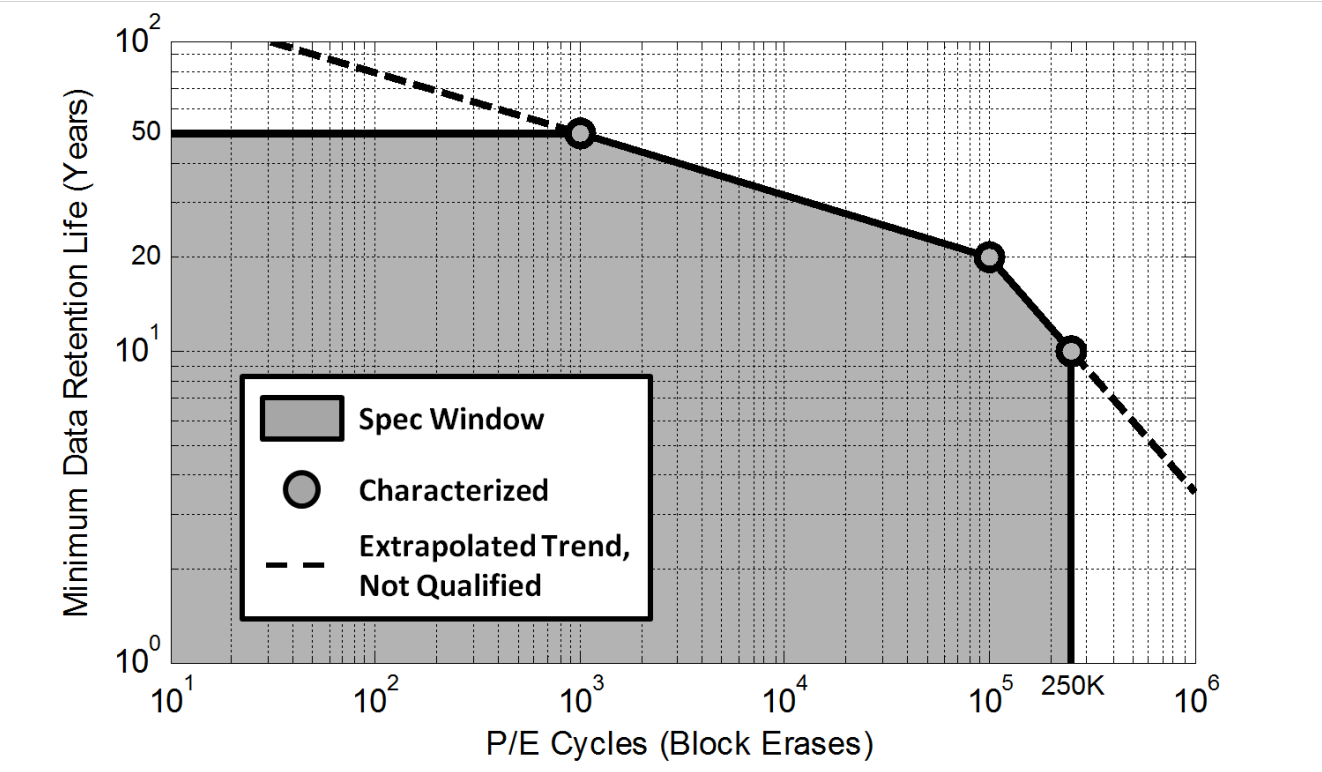
**Table 28. Flash memory module life specifications**

| Symbol | Characteristic | Conditions | Min | Typical | Units |
|---|---|---|---|---|---|
| Array P/E cycles | Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1] | — | 250,000 | — | P/E cycles |
| | Number of program/erase cycles per block for 256 KB blocks.[2] | — | 1,000 | 250,000 | P/E cycles |
| Data retention | Minimum data retention. | Blocks with 0 - 1,000 P/E cycles. | 50 | — | Years |
| | | Blocks with 100,000 P/E cycles. | 20 | — | Years |
| | | Blocks with 250,000 P/E cycles. | 10 | — | Years |

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

### 6.2.7 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.




### 6.2.8 Flash memory AC timing specifications

**Table 29. Flash memory AC timing specifications**

| Symbol | Characteristic | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| $t_{psus}$ | Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1. | — | 9.4<br>plus four system clock periods | 11.5<br>plus four system clock periods | µs |
| $t_{esus}$ | Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1. | — | 16<br>plus four system clock periods | 20.8<br>plus four system clock periods | µs |
| $t_{res}$ | Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low. | — | — | 100 | ns |

*Table continues on the next page...*

**Table 29. Flash memory AC timing specifications (continued)**

| Symbol | Characteristic | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| $t_{done}$ | Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared. | — | — | 5 | ns |
| $t_{dones}$ | Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1. | — | 16 plus four system clock periods | 20.8 plus four system clock periods | µs |
| $t_{drcv}$ | Time to recover once exiting low power mode. | 16 plus seven system clock periods. | — | 45 plus seven system clock periods | µs |
| $t_{aistart}$ | Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP | — | — | 5 | ns |
| $t_{aistop}$ | Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request. | — | — | 80 plus fifteen system clock periods | ns |
| $t_{mrstop}$ | Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request. | 10.36 plus four system clock periods | — | 20.42 plus four system clock periods | µs |

## 6.2.9 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1,2,3[RWSC] and PCRC1,2,3[APC] fields at various operating frequencies, based on specified intrinsic flash memory access timed of the Flash memory.

**Table 30. Flash read wait state and address pipeline control guidelines**

| Operating frequency (fsys) | RWSC | APC | Flash read latency on mini-cache miss (# of sys clock periods) | Flash read latency on mini-cache hit (# of sys clock periods) |
|---|---|---|---|---|
| 100 MHz | 2 | 1 | 5 | 1 |
| 133 MHz | 3 | 1 | 6 | 1 |

# 6.3 Communication

## 6.3.1 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

### 6.3.1.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

**Table 31. MII signal switching specifications**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| — | RXCLK frequency | — | 25 | MHz |
| MII1 | RXCLK pulse width high | 35% | 65% | RXCLK period |
| MII2 | RXCLK pulse width low | 35% | 65% | RXCLK period |
| MII3 | RXD[3:0], RXDV, RXER to RXCLK setup | 5 | — | ns |
| MII4 | RXCLK to RXD[3:0], RXDV, RXER hold | 5 | — | ns |
| — | TXCLK frequency | — | 25 | MHz |
| MII5 | TXCLK pulse width high | 35% | 65% | TXCLK period |
| MII6 | TXCLK pulse width low | 35% | 65% | TXCLK period |
| MII7 | TXCLK to TXD[3:0], TXEN, TXER invalid | 2 | — | ns |
| MII8 | TXCLK to TXD[3:0], TXEN, TXER valid | — | 25 | ns |

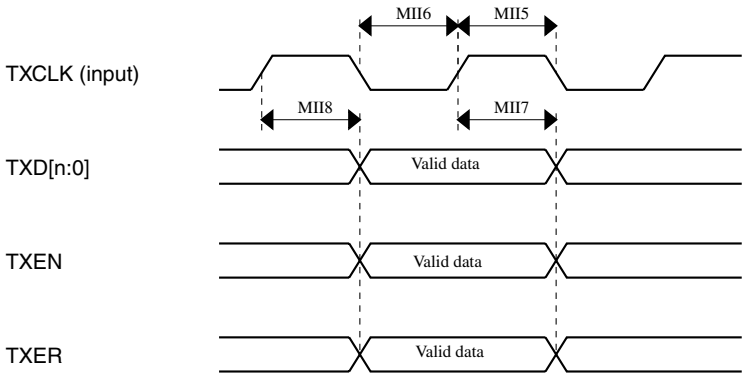



**Figure 11. RMII/MII transmit signal timing diagram**

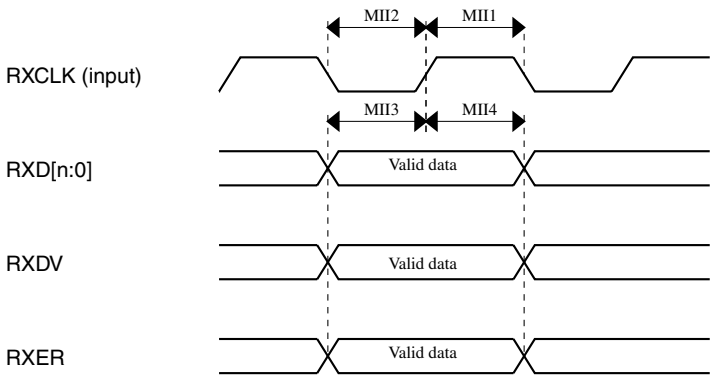



**Figure 12. RMII/MII receive signal timing diagram**

### 6.3.1.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

**Table 32. RMII signal switching specifications**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| — | EXTAL frequency (RMII input clock RMII_CLK) | — | 50 | MHz |
| RMII1 | RMII_CLK pulse width high | 35% | 65% | RMII_CLK period |
| RMII2 | RMII_CLK pulse width low | 35% | 65% | RMII_CLK period |
| RMII3 | RXD[1:0], CRS_DV, RXER to RMII_CLK setup | 4 | — | ns |
| RMII4 | RMII_CLK to RXD[1:0], CRS_DV, RXER hold | 2 | — | ns |
| RMII7 | RMII_CLK to TXD[1:0], TXEN invalid | 4 | — | ns |
| RMII8 | RMII_CLK to TXD[1:0], TXEN valid | — | 15 | ns |

#### 6.3.1.3 MII/RMII Serial Management channel timing (MDC/MDIO)

Ethernet works with maximum frequency of MDC at 2.5 Mhz. Output pads configured with SRC=0b11. MDIO Pin must have external pullup.

**Table 33. Ethernet MDIO timing table**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| MDC10 | MDC falling edge to MDIO output invalid (minimum propagation delay) | - 0.8 | | ns |
| MDC11 | MDC falling edge to MDIO output valid (maximum propagation delay) | | 13 | ns |
| MDC12 | MDIO (input) to MDC rising edge setup | 13 | | ns |
| MDC13 | MDIO (input) to MDC rising edge hold | 0 | | ns |
| MDC14 | MDC pulse width high | 40% | | MDC Period |
| MDC15 | MDC pulse width low | 40% | | MDC Period |

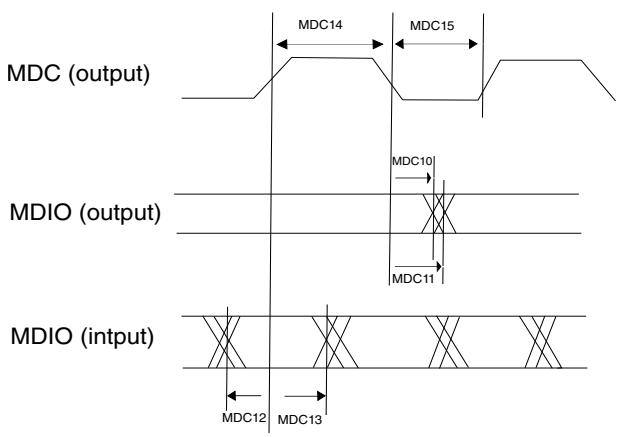



**Figure 13. RMII/MII serial management channel timing diagram**

### 6.3.2 FlexRay

#### 6.3.2.1 FlexRay timing parameters

This section provides the FlexRay interface timing characteristics for the input and output signals. These numbers are recommended per the FlexRay Electrical Physical Layer Specification, Version 3.0.1, and subject to change per the final timing analysis of the device.

#### 6.3.2.1.1 TxEN

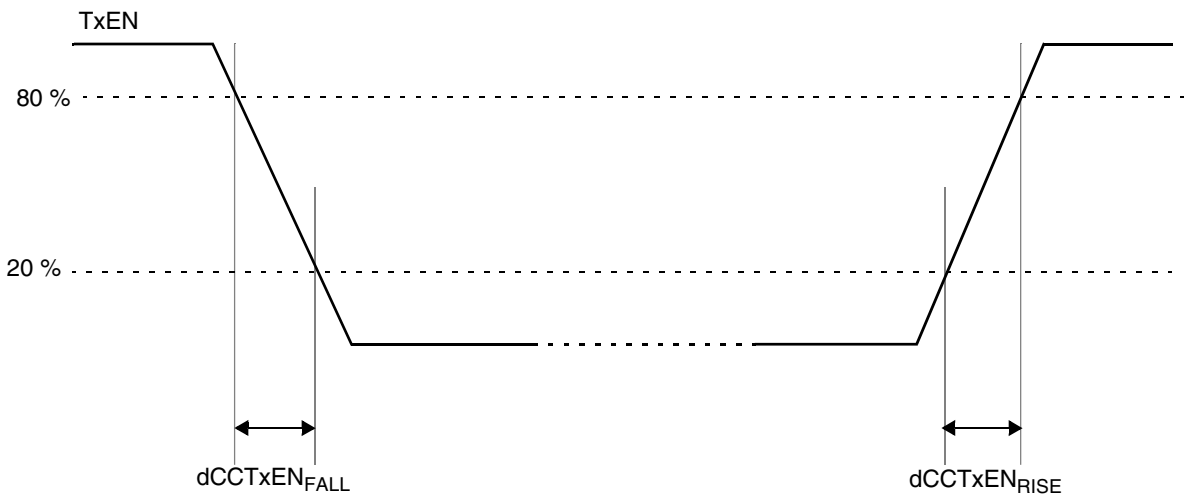



**Figure 14. FlexRay TxEN signal**

**Table 34. TxEN output characteristics[1]**

| Name | Description | Min | Max | Unit |
|---|---|---|---|---|
| $dCCTxEN_{RISE25}$ | Rise time of TxEN signal at CC | — | 9 | ns |
| $dCCTxEN_{FALL25}$ | Fall time of TxEN signal at CC | — | 9 | ns |
| $dCCTxEN_{01}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge | — | 25 | ns |
| $dCCTxEN_{10}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge | — | 25 | ns |

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +10%, $T_J$ = –40 °C / 150 °C, TxEN pin load maximum 25 pF

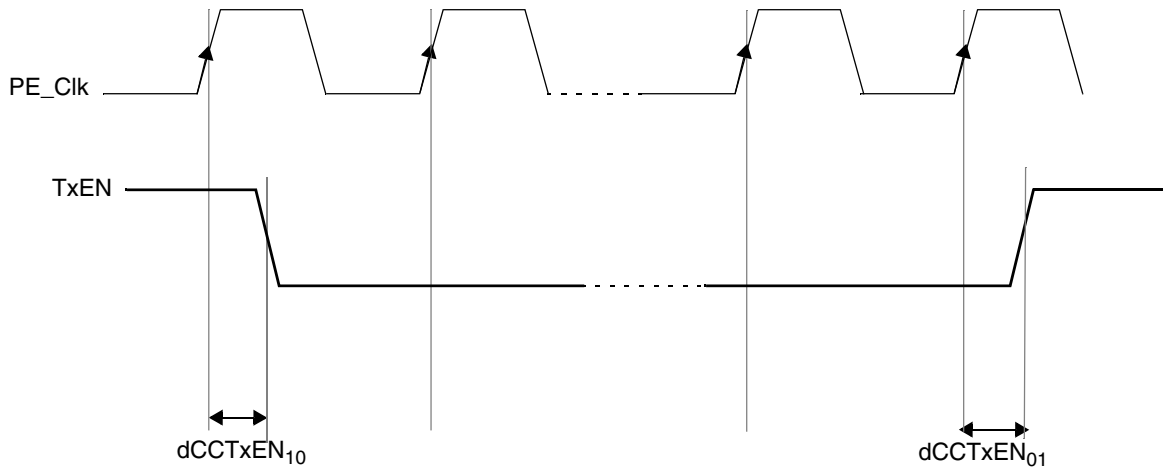



**Figure 15. FlexRay TxEN signal propagation delays**

#### 6.3.2.1.2 TxD

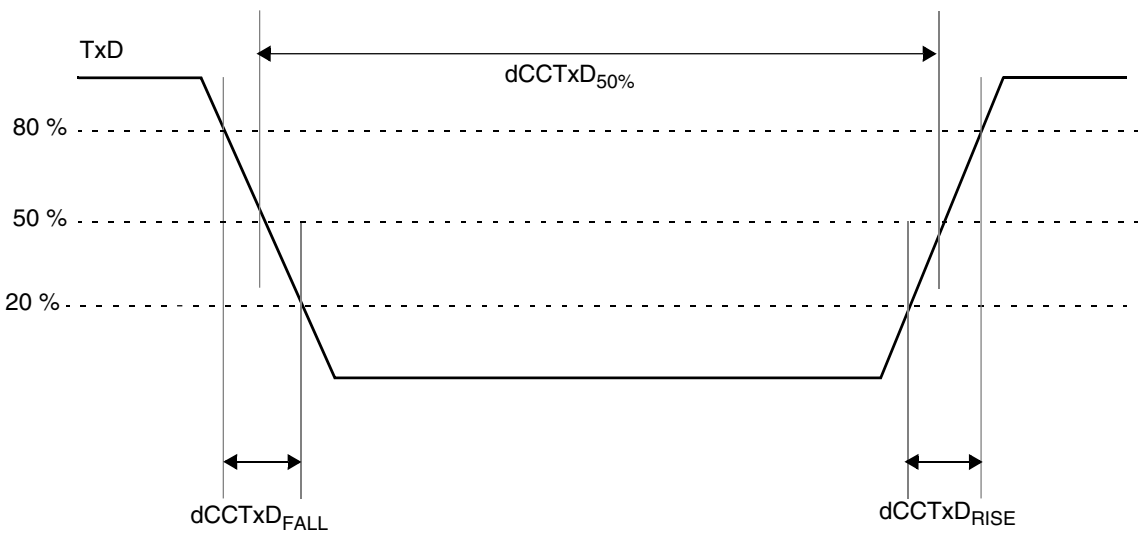



**Figure 16. FlexRay TxD signal**

Flexray TxD output specs are only valid for non slew rate control settings (MSCR[SRC] = 2 or 3).

**Table 35. TxD output characteristics**

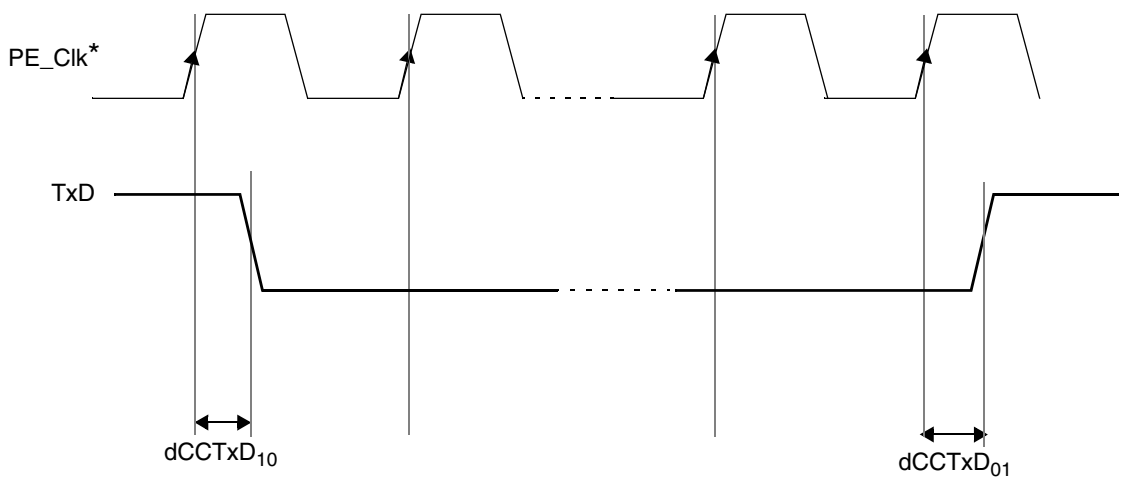
| Name | Description[1] | Min | Max | Unit |
|---|---|---|---|---|
| $dCCT_{xAsym}$ | Asymmetry of sending CC @ 25 pF load | –2.45 | 2.45 | ns |

*Table continues on the next page...*

**Table 35. TxD output characteristics (continued)**

| Name | Description[1] | Min | Max | Unit |
|---|---|---|---|---|
| | (=$dCCTxD_{50\%}$ - 100 ns) | | | |
| $dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$ | Sum of Rise and Fall time of TxD signal at the output | — | 9 | ns |
| $dCCTxD_{01}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge | — | 25 | ns |
| $dCCTxD_{10}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge | — | 25 | ns |

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +10%, $T_J$ = –40 °C / 150°C, TxD pin load maximum 25 pF




*FlexRay Protocol Engine Clock

**Figure 17. FlexRay TxD signal propagation delays**

### 6.3.2.1.3 RxD

**Table 36. RxD input characteristic**

| Name | Description[1] | Min | Max | Unit |
|---|---|---|---|---|
| C_CCRxD | Input capacitance on RxD pin | — | 7 | pF |
| uCCLogic_1 | Threshold for detecting logic high | 35 | 70 | % |
| uCCLogic_0 | Threshold for detecting logic low | 30 | 65 | % |
| $dCCRxD_{01}$ | Sum of delay from actual input to the D input of the first FF, rising edge | — | 10 | ns |
| $dCCRxD_{10}$ | Sum of delay from actual input to the D input of the first FF, falling edge | — | 10 | ns |

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +10%, $T_J$ = –40 / 150 °C

#### 6.3.2.1.4 Receiver asymmetry

**Table 37. Receiver asymmetry**

| Name | Description | Min | Max | Unit |
|---|---|---|---|---|
| $dCCRxAsymAccept_{15}$ | Acceptance of asymmetry at receiving CC with 15 pF load (*) | –31.5 | +44.0 | ns |
| $dCCRxAsymAccept_{25}$ | Acceptance of asymmetry at receiving CC with 25 pF load (*) | –30.5 | +43.0 | ns |

## 6.3.3 Parallel Digital Interface (PDI)

**Table 38. Parallel Digital Interface electrical parameters**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{PDISetup}$[1] | — | 2 | — | — | ns |
| $t_{PDIHold}$ | — | 2 | — | — | ns |

1. Valid for PDI Data 11 to PDI Data 0. PDI Data 15 to PDI Data 12 tPDISetup is 8

## 6.3.4 LVDS Fast Asynchronous Transmission (LFAST) electrical characteristics

### 6.3.4.1 LFAST IO electrical specifications

The following table provides output driver characteristics for LFAST I/Os.

**Table 39. LFAST output buffer electrical characteristics**

| Symbol | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $\lvert\Delta_{VO\_L}\rvert$ | Absolute value for differential output voltage swing (terminated) | — | 100 | 200 | 285 | mV |
| $V_{ICOM\_L}$ | Common mode voltage | — | 1.08 | 1.2 | 1.32 | V |
| $T_{tr\_L}$ | Transition time output pin LVDS configuration | — | 0.2 | — | 1.5 | ns |

1. $V_{DD\_HV\_IOx}$ = 3.3 V (–5%, +10%), $T_J$ = –40 / 150 °C, unless otherwise specified.

**NOTE**

Fast IOs must be specified only as fast (and not as high current). See GPIO DC electrical specification.

### 6.3.4.2 LFAST interface timing diagrams

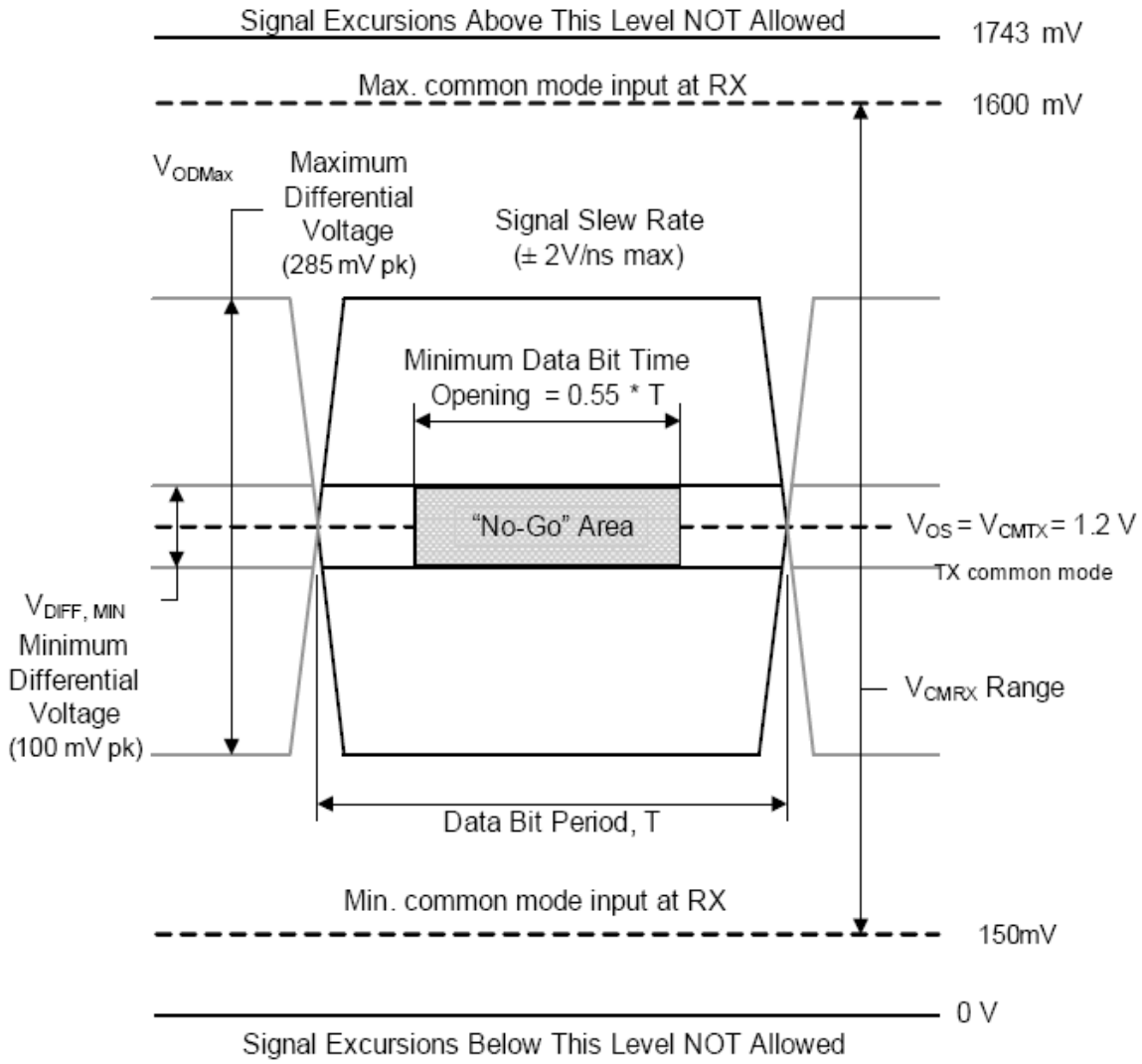



**Figure 18. LFAST timing definition**

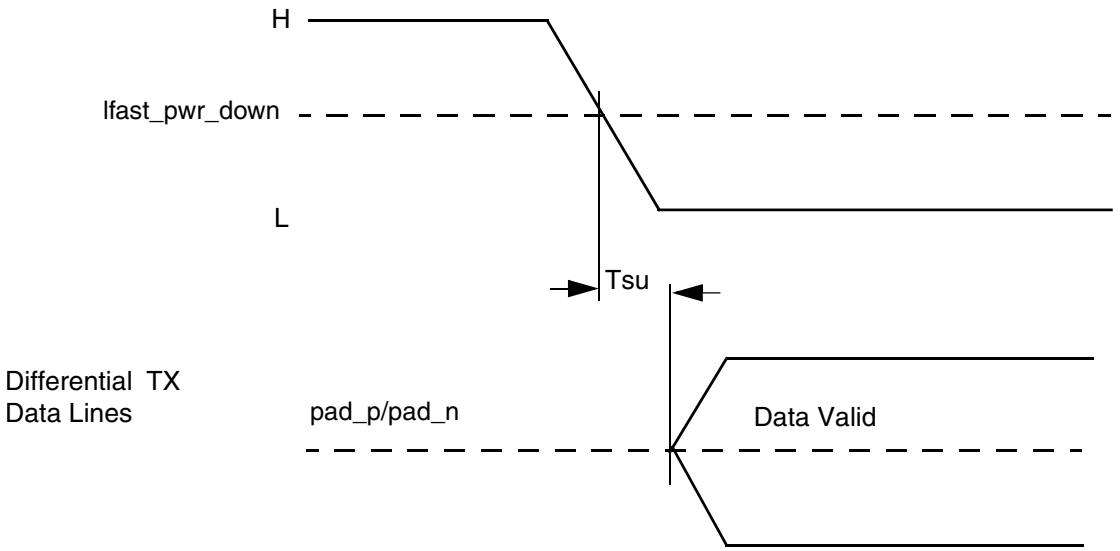



**Figure 19. Power-down exit time**

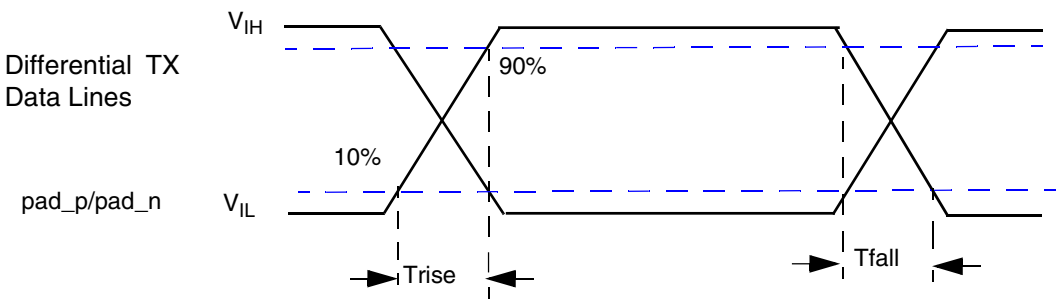



**Figure 20. Rise/fall time**

### 6.3.4.3 LFAST interface electrical characteristics

**Table 40. LFAST electrical characteristics**

| Symbol | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Data Rate | | | | | | |
| DATARATE | Data rate | — | — | 312/320 | Typ+0.1% | Mbps |
| STARTUP | | | | | | |
| $T_{STRT\_BIAS}$ | Bias startup time[2] | — | — | 0.5 | 3 | µs |
| $T_{PD2NM\_TX}$ | Transmitter startup time (power down to normal mode)[3] | — | — | 0.2 | 2 | µs |
| $T_{SM2NM\_TX}$ | Transmitter startup time (sleep mode to normal mode)[4] | — | — | 0.2 | 0.5 | µs |
| $T_{PD2NM\_RX}$ | Receiver startup time[5] (Power down to Normal mode) | — | — | 20 | 40 | ns |

*Table continues on the next page...*

## Table 40. LFAST electrical characteristics (continued)

| Symbol | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $T_{PD2SM\_RX}$ | Receiver startup time[4] (Power down to Sleep mode) | — | — | 20 | 50 | ns |
| TRANSMITTER | | | | | | |
| $V_{OS\_DRF}$ | Common mode voltage | — | 1.08 | — | 1.32 | V |
| $\lvert\Delta V_{OD\_DRF}\rvert$ | Differential output voltage swing (terminated) | — | ±100 | ±200 | ± 285 | mV |
| $T_{TR\_DRF}$ | Rise/Fall time (10% - 90% of swing) | — | 0.26 | — | 1.5 | ns |
| $R_{OUT\_DRF}$ | Terminating resistance | | 67 | — | 198 | Ω |
| $C_{OUT\_DRF}$ | Capacitance[6] | — | — | — | 5 | pF |
| RECEIVER | | | | | | |
| $V_{ICOM\_DRF}$ | Common mode voltage | — | 0.15[7] | — | 1.6[8] | V |
| $\lvert D_{VI\_DRF}\rvert$ | Differential input voltage | — | 100 | — | — | mV |
| $V_{HYS\_DRF}$ | Input hysteresis | — | 25 | — | — | mV |
| $R_{IN\_DRF}$ | Terminating resistance | | 80 | 115 | 150 | Ω |
| $C_{IN\_DRF}$ | Capacitance[9] | — | — | 3.5 | 6 | pF |
| $L_{IN\_DRF}$ | Parasitic Inductance[10] | — | — | 5 | 10 | nH |
| TRANSMISSION LINE CHARACTERISTICS (PCB Track) | | | | | | |
| $Z_0$ | Transmission line characteristic impedance | — | 47.5 | 50 | 52.5 | Ω |
| $Z_{DIFF}$ | Transmission line differential impedance | — | 95 | 100 | 105 | Ω |

1. $V_{DD\_VH\_IOx}$ = 3.3 V -5%,+10%, $T_J$ = –40 / 150 °C, unless otherwise specified
2. Startup time is defined as the time taken by LFAST current reference block for settling bias current after its pwr_down (power down) has been deasserted. LFAST functionality is guaranteed only after the startup time.
3. Startup time is defined as the time taken by LFAST transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
4. Startup time is defined as the time taken by LFAST transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
5. Startup time is defined as the time taken by LFAST receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
6. Total lumped capacitance including silicon, package pin and bond wire. Application board simulation is needed to verify LFAST template compliancy.
7. Absolute min = 0.15 V – (285 mV / 2) = 0 V
8. Absolute max = 1.6 V + (285 mV / 2) = 1.743 V
9. Total capacitance including silicon, package pin and bond wire
10. Total inductance including silicon, package pin and bond wire

### 6.3.5 DSPI timing

The following table describes the SPI electrical characteristics.

MTEF=1 Mode timing values given below are only applicable when external SPI is in classic mode. Slave mode timing values given below are applicable when device is in MTFE=0.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured as SRE = 11.

**Table 41. DSPI timing**

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | $t_{SCK}$ | DSPI cycle time | Master (MTFE = 0) | 60 | — | ns |
| | | | Slave (MTFE = 0) | 60 | — | |
| | | | Slave Receive Only mode[1] | 16 | — | |
| 2 | $t_{CSC}$ | PCS to SCK delay | Master | 20[2] | — | ns |
| 3 | $t_{ASC}$ | After SCK delay | Master | 27[3] | — | ns |
| 4 | $t_{SDC}$ | SCK duty cycle | Master[4] | $t_{SCK}/2 - 1.5$ | $t_{SCK}/2 + 1.5$ | ns |
| | | | Slave[5] | $t_{SCK}/2 - 1.5$ | $t_{SCK}/2 + 1.5$ | ns |
| | | | Slave Receive only Mode[6] | $t_{SCK}/2 - 1.0$ | $t_{SCK}/2 + 1.0$ | ns |
| 5 | $t_A$ | Slave access time | $\overline{SS}$ active to SOUT valid | — | 32 | ns |
| 6 | $t_{DIS}$ | Slave SOUT disable time | $\overline{SS}$ inactive to SOUT High-Z or invalid | — | 32 | ns |
| 7 | $t_{PCSC}$ | PCSx to $\overline{PCSS}$ time | — | 13 | — | ns |
| 8 | $t_{PASC}$ | $\overline{PCSS}$ to PCSx time | — | 13 | — | ns |
| 9 | $t_{SUI}$ | Data setup time for inputs | Master (MTFE = 0) | 20 | — | ns |
| | | | Slave | 2 | — | |
| | | | Master (MTFE = 1, CPHA = 0)[7] | 20-N x DSPI IPG clock period[8] | — | |
| | | | Master (MTFE = 1, CPHA = 1) | 20 | — | |
| 10 | $t_{HI}$ | Data hold time for inputs | Master (MTFE = 0) | –5 | — | ns |
| | | | Slave | 4 | — | |
| | | | Master (MTFE = 1, CPHA = 0)[7] | -5 + N x DSPI IPG clock period[8] | — | |
| | | | Master (MTFE = 1, CPHA = 1) | –5 | — | |
| 11 | $t_{SUO}$ | Data valid (after SCK edge) | Master (MTFE = 0) | — | 7[9] | ns |
| | | | Slave | — | 23 | |

*Table continues on the next page...*

## Table 41. DSPI timing (continued)

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| | | | Master (MTFE = 1, CPHA = 0)[10] | — | 7 + DSPI IPG Clock Period | |
| | | | Master (MTFE = 1, CPHA = 1) | — | 7 | |
| 12 | $t_{HO}$ | Data hold time for outputs | Master (MTFE = 0) | –4[11] | — | ns |
| | | | Slave | 3.8 | — | |
| | | | Master (MTFE = 1, CPHA = 0)[10] | -4 + DSPI IPG Clock Period | — | |
| | | | Master (MTFE = 1, CPHA = 1) | –4 | — | |

1. Slave Receive Only mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.
2. For SPI_CTARn[PCSSCK] - 'PCS to SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[CSSCK] - 'PCS to SCK Delay Scaler' configuration is '2' (0000h).
3. For SPI_CTARn[PASC] - 'After SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[ASC] - 'After SCK Delay Scaler' configuration is '2' (0000h).
4. The numbers are valid when DSPI is configured for 50/50 . Refer to Reference manual for the mapping of duty cycle to each configuration. A change in duty cycle changes the parameter here. For example a configuration providing duty cycle of 33/66 at DSPI translates to Min tSCK/3 - 1.5 ns Max tSCK/3 + 1.5 ns.
5. In slave mode any input duty cycle variation must be seen along with setup and hold timing would be datasheet parameters (input setup hold/output data valid setup/hold) of both master and slave. If the duty cycle is not as per spec it needs to be compensated by master timings.
6. In slave receive only mode any input duty cycle variation must be seen along with setup and hold timing would be datasheet parameters (input setup hold/output data valid setup/hold) of both master and slave. Must meet for min tSCK and for higher tSCK any degrdation in duty cyle needs to be compensated by master timings but still cannot be less than tSCKmin/2+1 ns and tSCK/2min-1 ns for slave receive only mode.
7. For SPI_CTARn[BR] - 'Baud Rate Scaler' configuration is >= 4.
8. N=Configured sampling point value in MTFE=1 Mode.
9. Same value is applicable for PCS timing in continuous SCK mode.
10. SMPL_PTR should be set to 1
11. Same value is applicable for PCS timing in continuous SCK mode

**NOTE**

For numbers shown in the following figures, see Table 41.

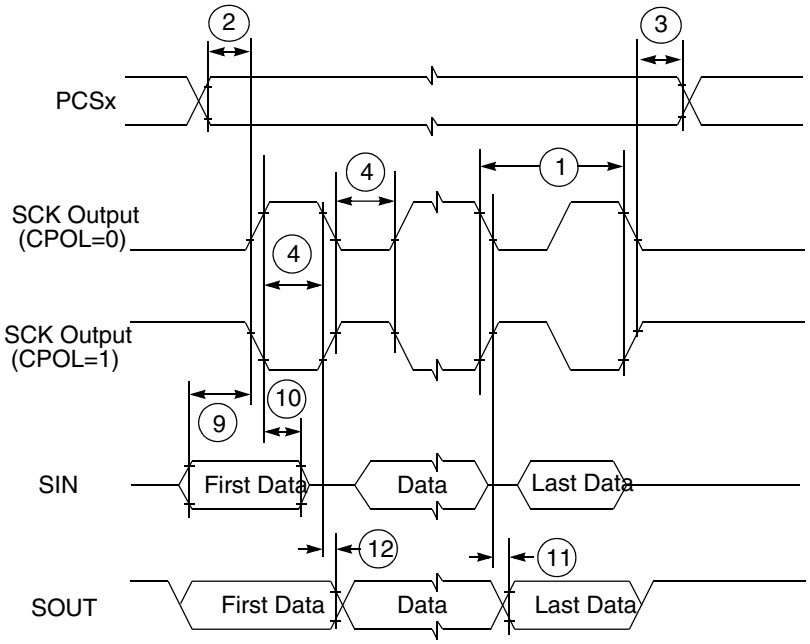



**Figure 21. DSPI classic SPI timing — master, CPHA = 0**

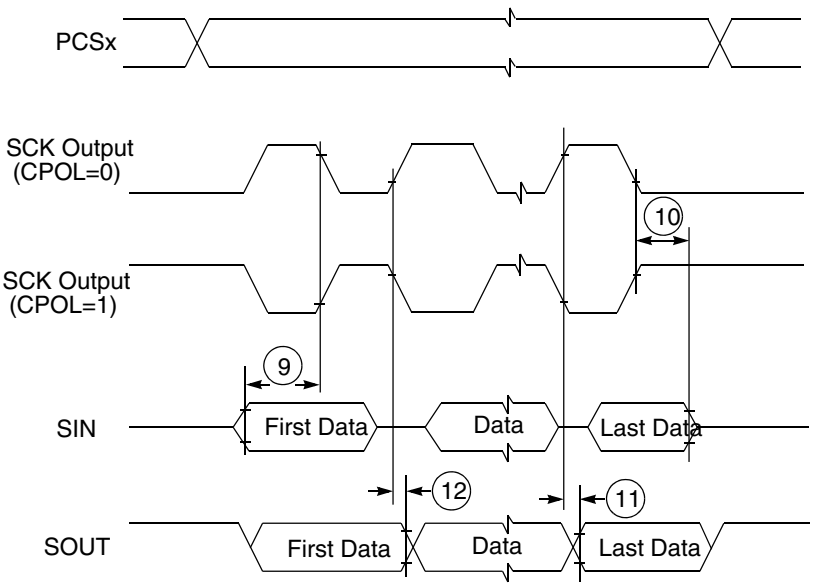



**Figure 22. DSPI classic SPI timing — master, CPHA = 1**

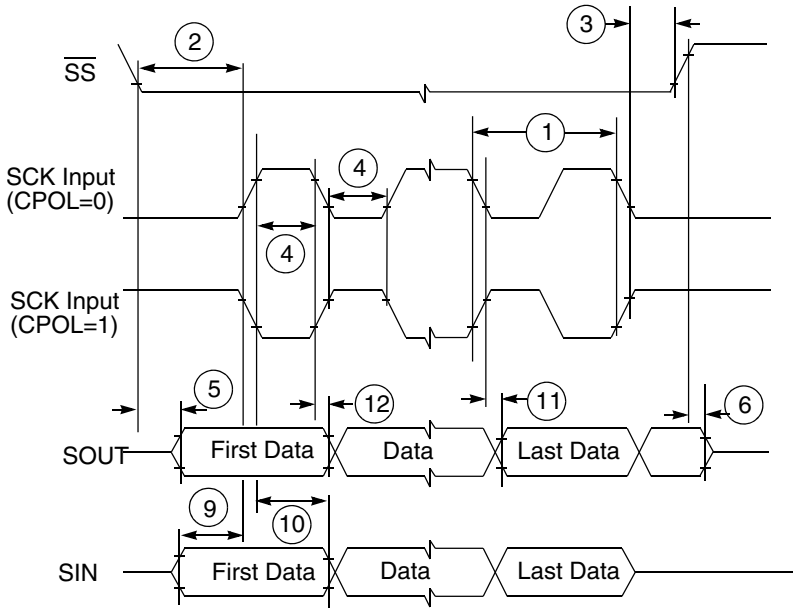



**Figure 23. DSPI classic SPI timing — slave, CPHA = 0**

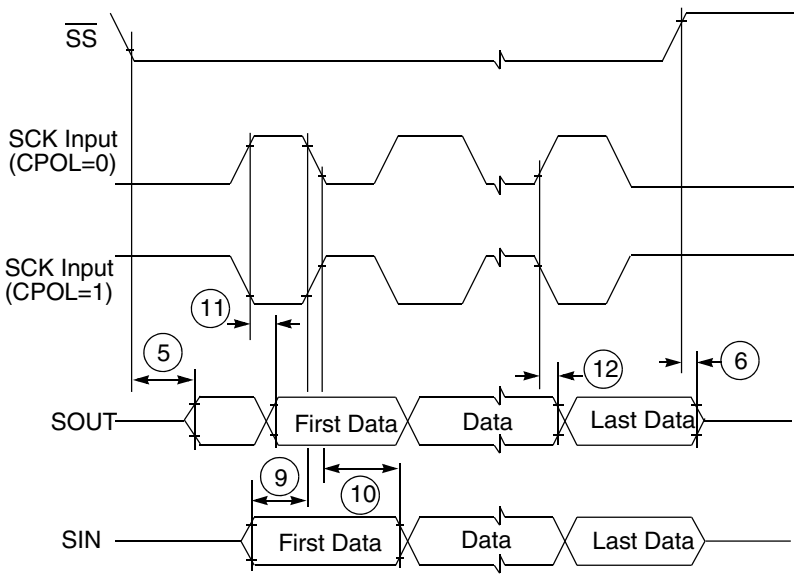



**Figure 24. DSPI classic SPI timing — slave, CPHA = 1**

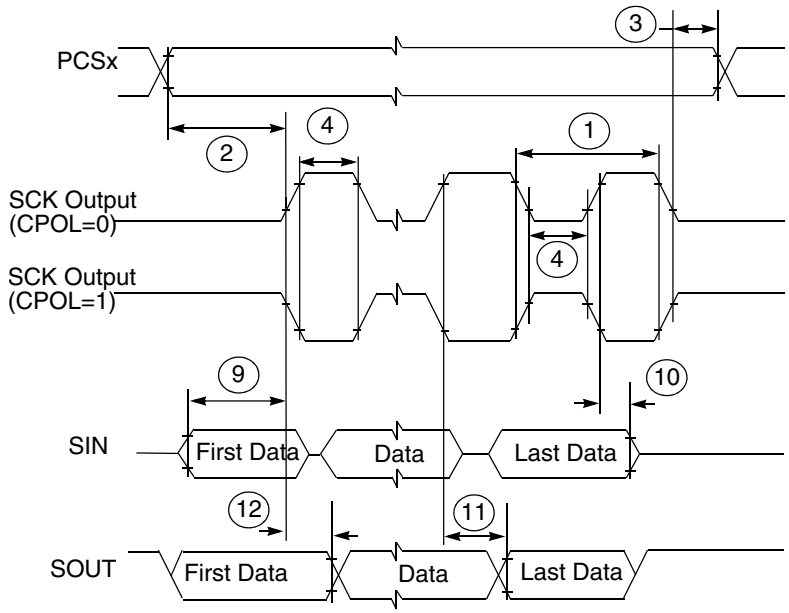



**Figure 25. DSPI modified transfer format timing — master, CPHA = 0**

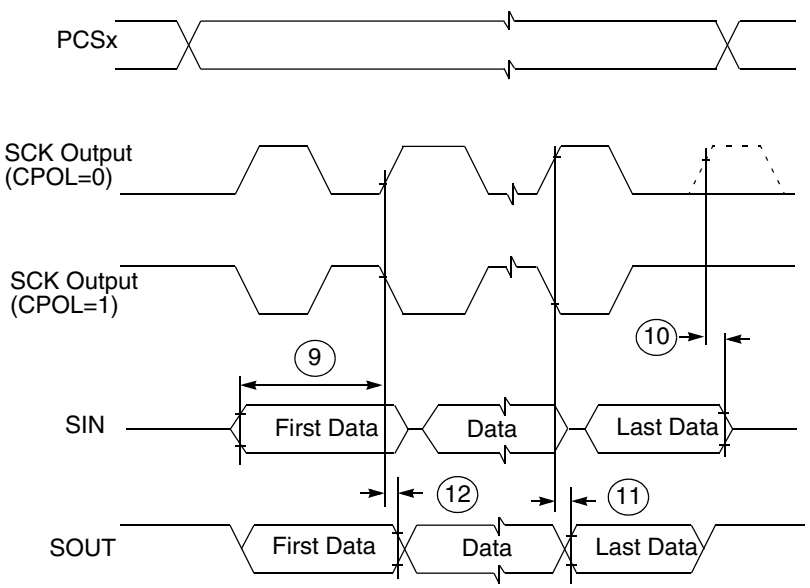



**Figure 26. DSPI modified transfer format timing — master, CPHA = 1**

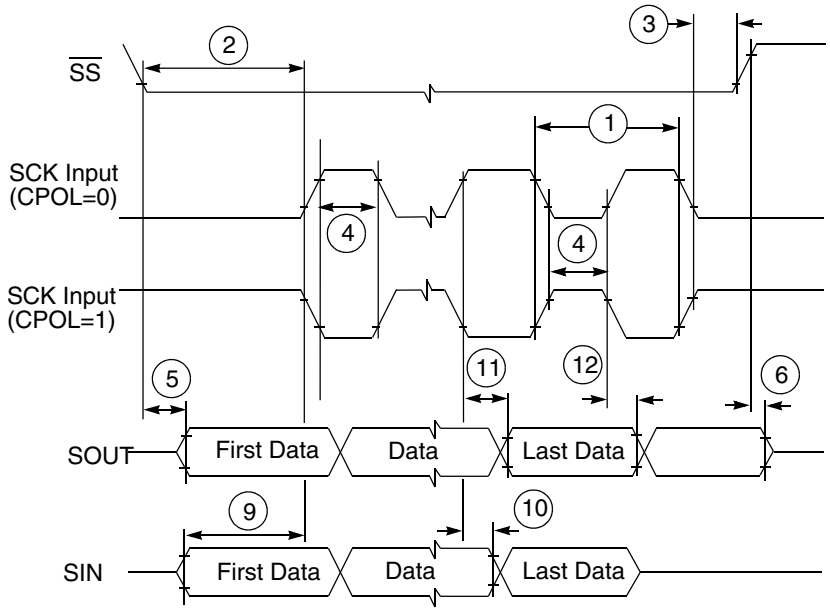



**Figure 27. DSPI modified transfer format timing – slave, CPHA = 0**

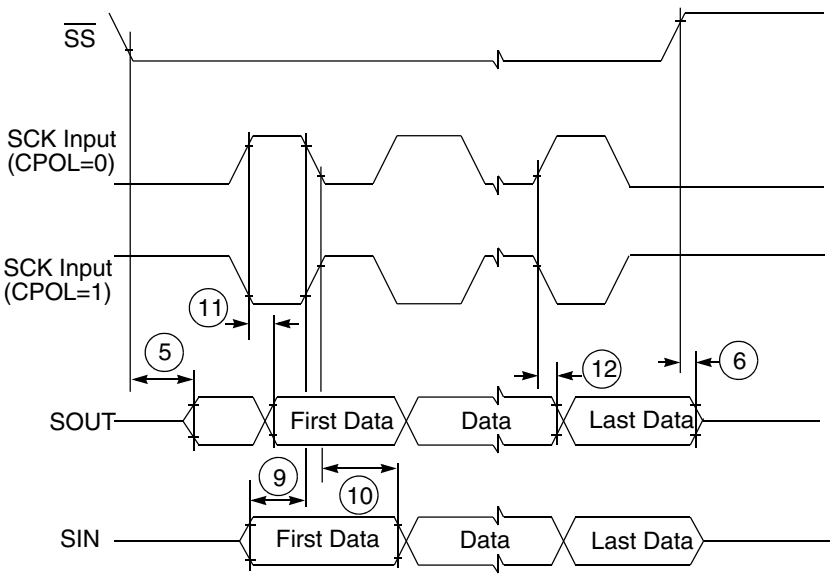



**Figure 28. DSPI modified transfer format timing — slave, CPHA = 1**

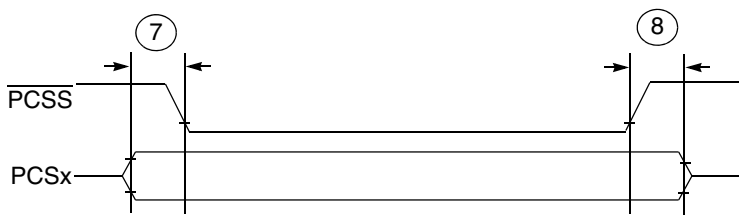



**Figure 29. DSPI PCS strobe (PCSS) timing**

### 6.3.6 LINFlex timing

The maximum bit rate is 1.875 MBit/s.

## 6.4 Debug

### 6.4.1 JTAG/CJTAG interface timing

The following table lists JTAGC/CJTAG electrical characteristics.

- Measurements are with input transition of 1 ns, output load of 50 pF and pads configured with SRE=11.

**Table 42. JTAG/CJTAG pin AC electrical characteristics [1]**

| # | Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | $t_{JCYC}$ [2] | TCK Cycle Time (JTAG) | 36 | — | ns |
| | | TCK Cycle Time (CJTAG) | 50 | — | ns |
| 2 | $t_{JDC}$ | TCK Clock Pulse Width | 40 | 60 | % |
| 3 | $t_{TCKRISE}$ | TCK Rise and Fall Times (40% - 70%) | — | 3 | ns |
| 4 | $t_{TMSS}$, $t_{TDIS}$ | TMS, TDI Data Setup Time | 5 | — | ns |
| 5 | $t_{TMSH}$, $t_{TDIH}$ | TMS, TDI Data Hold Time | 5 | — | ns |
| 6 | $t_{TDOV}$ | TCK Low to TDO/TMS Data Valid [3] | — | 15[4] | ns |
| 7 | $t_{TDOI}$ | TCK Low to TDO/TMS Data Invalid[3] | 0 | — | ns |
| 8 | $t_{TDOHZ}$ | TCK Low to TDO/TMS High Impedance[3] | — | 22 | ns |
| 9 | $t_{JCMPPW}$ | JCOMP Assertion Time | 100 | — | ns |
| 10 | $t_{JCMPS}$ | JCOMP Setup Time to TCK Low | 40 | — | ns |
| 11 | $t_{BSDV}$ | TCK Falling Edge to Output Valid | — | 600[5] | ns |
| 12 | $t_{BSDVZ}$ | TCK Falling Edge to Output Valid out of High Impedance | — | 600 | ns |
| 13 | $t_{BSDHZ}$ | TCK Falling Edge to Output High Impedance | — | 600 | ns |
| 14 | $t_{BSDST}$ | Boundary Scan Input Valid to TCK Rising Edge | 15 | — | ns |
| 15 | $t_{BSDHT}$ | TCK Rising Edge to Boundary Scan Input Invalid | 15 | — | ns |

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. TMS timing is applicable only in CJTAG mode
4. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
5. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

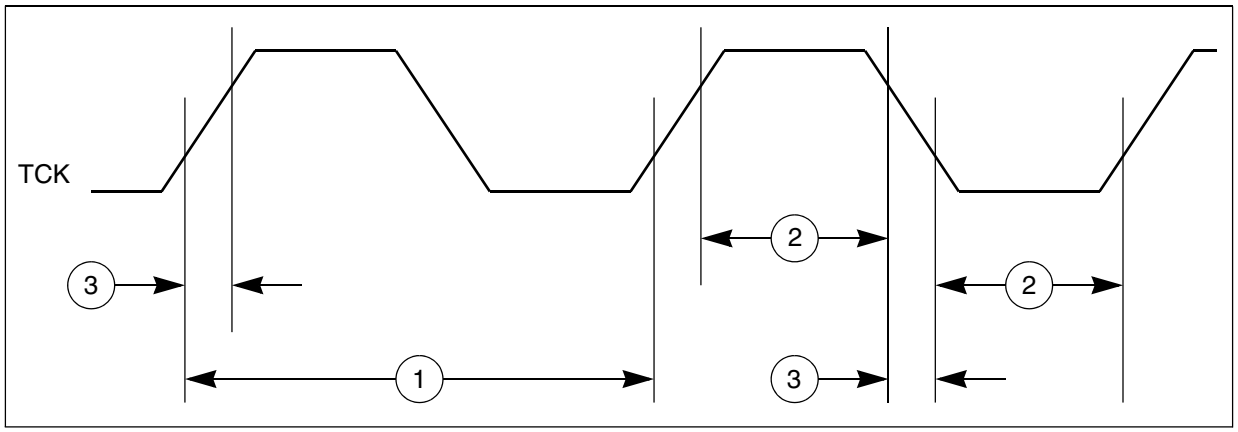



**Figure 30. JTAG test clock input timing**

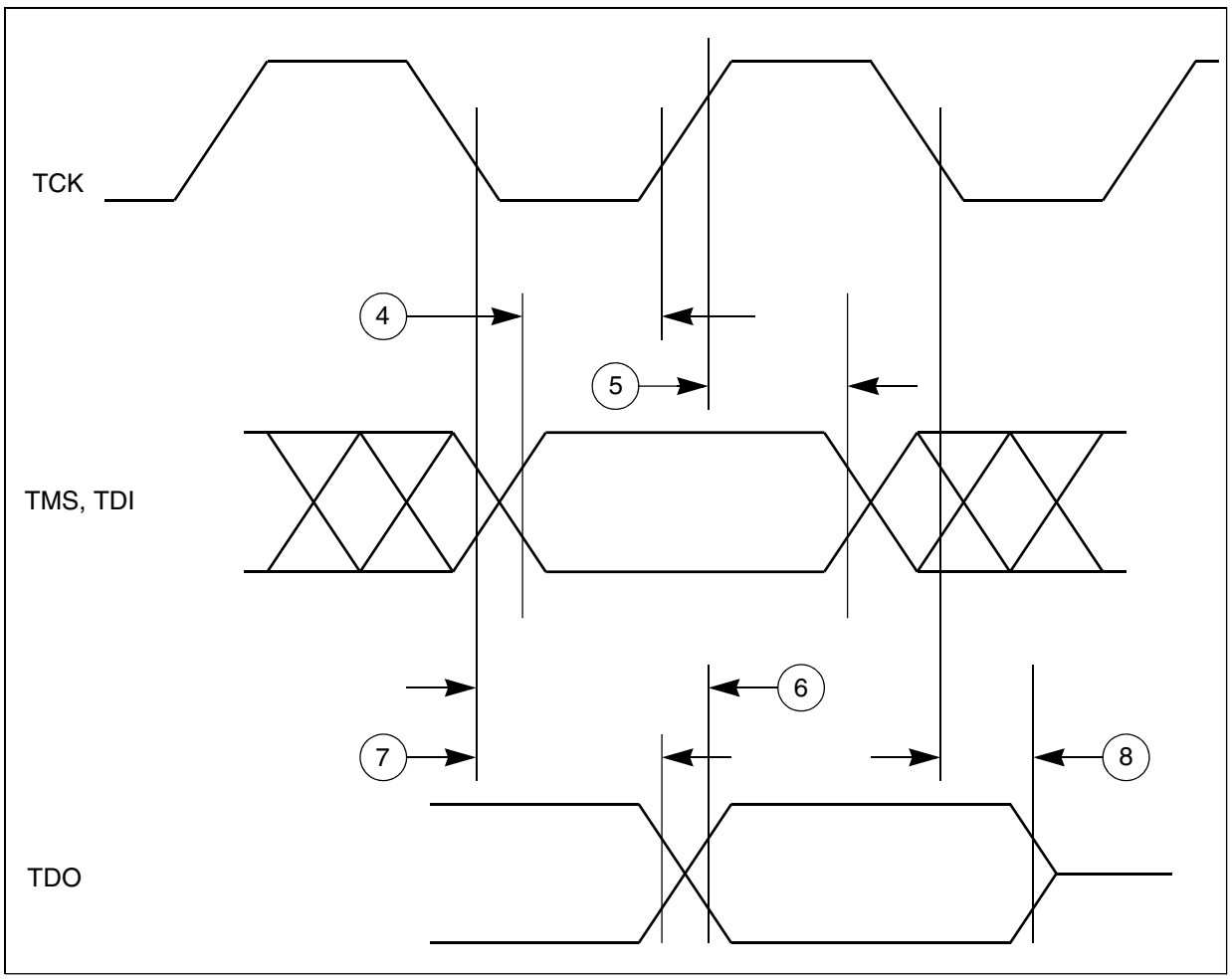



**Figure 31. JTAG test access port timing**

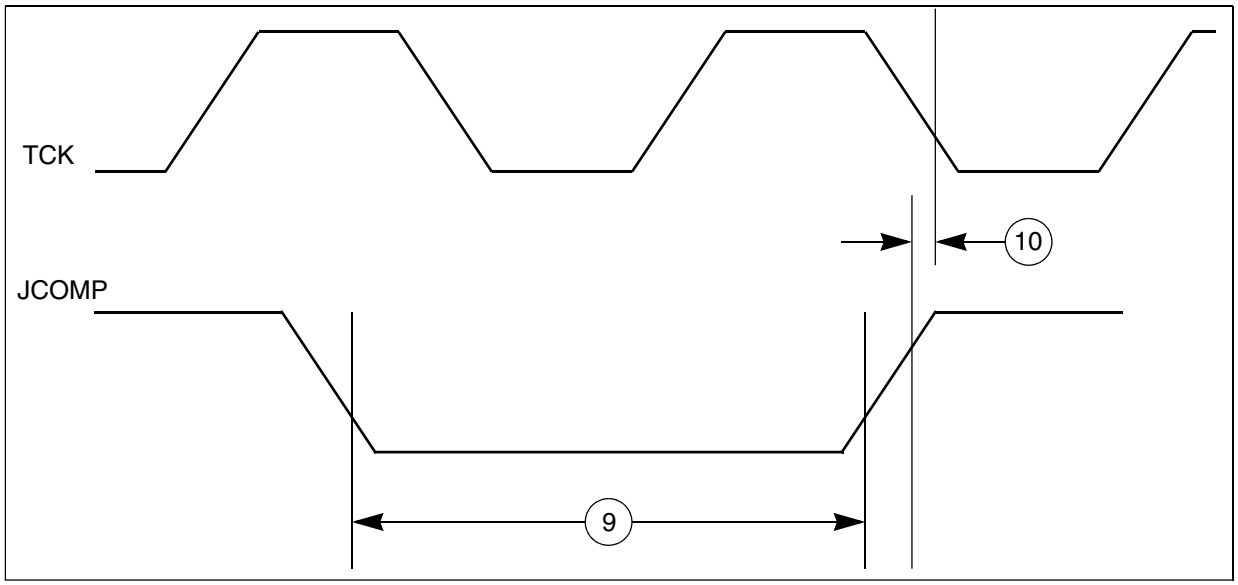



**Figure 32. JTAG JCOMP timing**

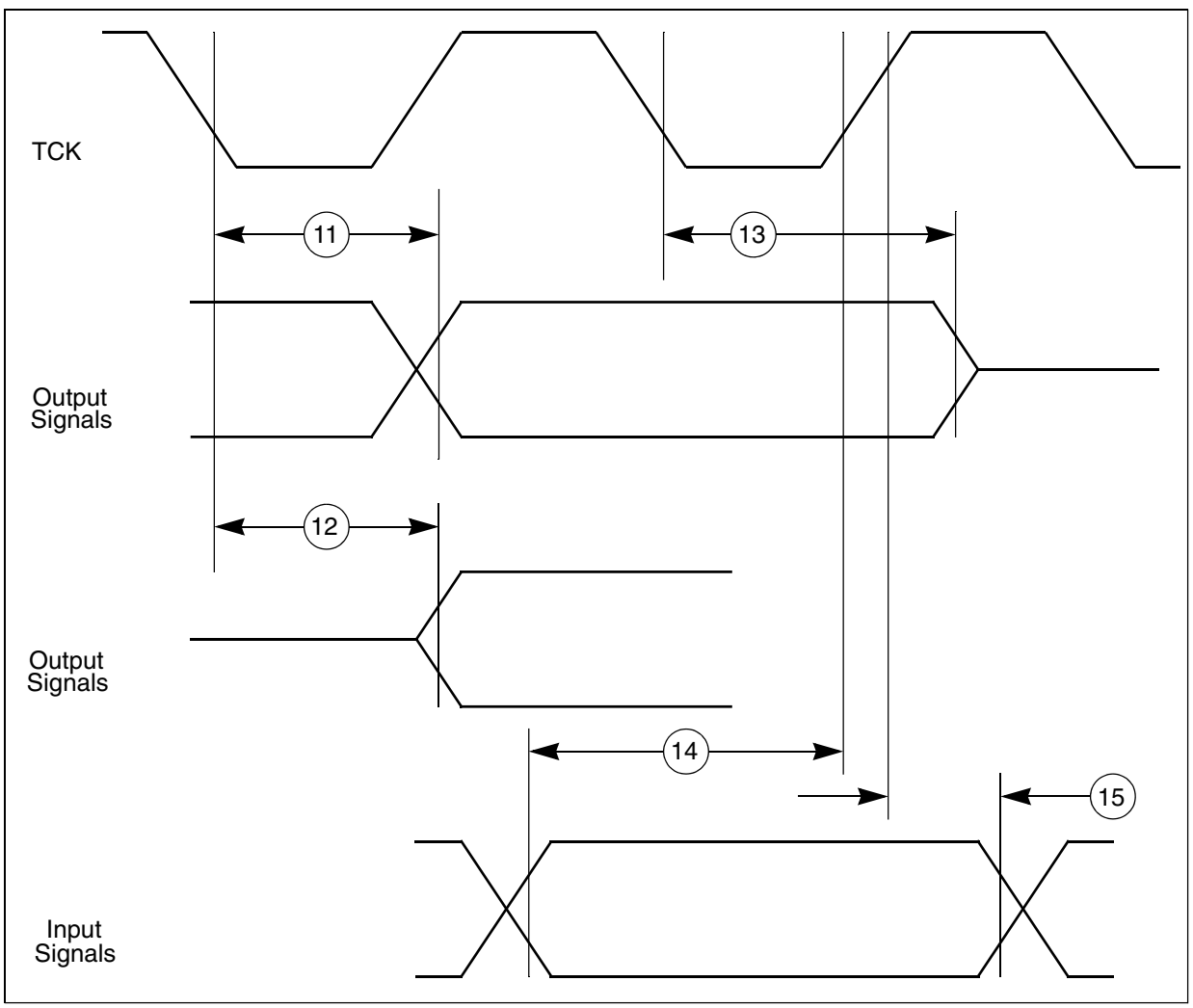



**Figure 33. JTAG boundary scan timing**

## 6.4.2 Nexus Aurora debug port timing

**Table 43. Nexus Aurora debug port timing**

| # | Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | $t_{REFCLK}$ | Reference clock frequency | 625 | 1250 | MHz |
| 1a | $t_{MCYC}$ | Reference Clock rise/fall time | — | 400 | ps |
| 2 | $t_{RCDC}$ | Reference Clock Duty Cycle | 45 | 55 | % |
| 3 | $J_{RC}$ | Reference Clock jitter | — | 40 | ps |
| 4 | $t_{STABILITY}$ | Reference Clock Stability | 50 | — | PPM |
| 5 | BER | Bit Error Rate | — | $10^{-12}$ | — |
| 6 | $J_D$ | Transmit lane Deterministic Jitter | — | 0.17 | OUI |
| 7 | $J_T$ | Transmit lane Total Jitter | — | 0.35 | OUI |
| 8 | $S_O$ | Differential output skew | — | 20 | ps |
| 9 | $S_{MO}$ | Lane to lane output skew | — | 1000 | ps |
| 10 | OUI | Aurora lane Unit Interval | 800 | 800 | ps |

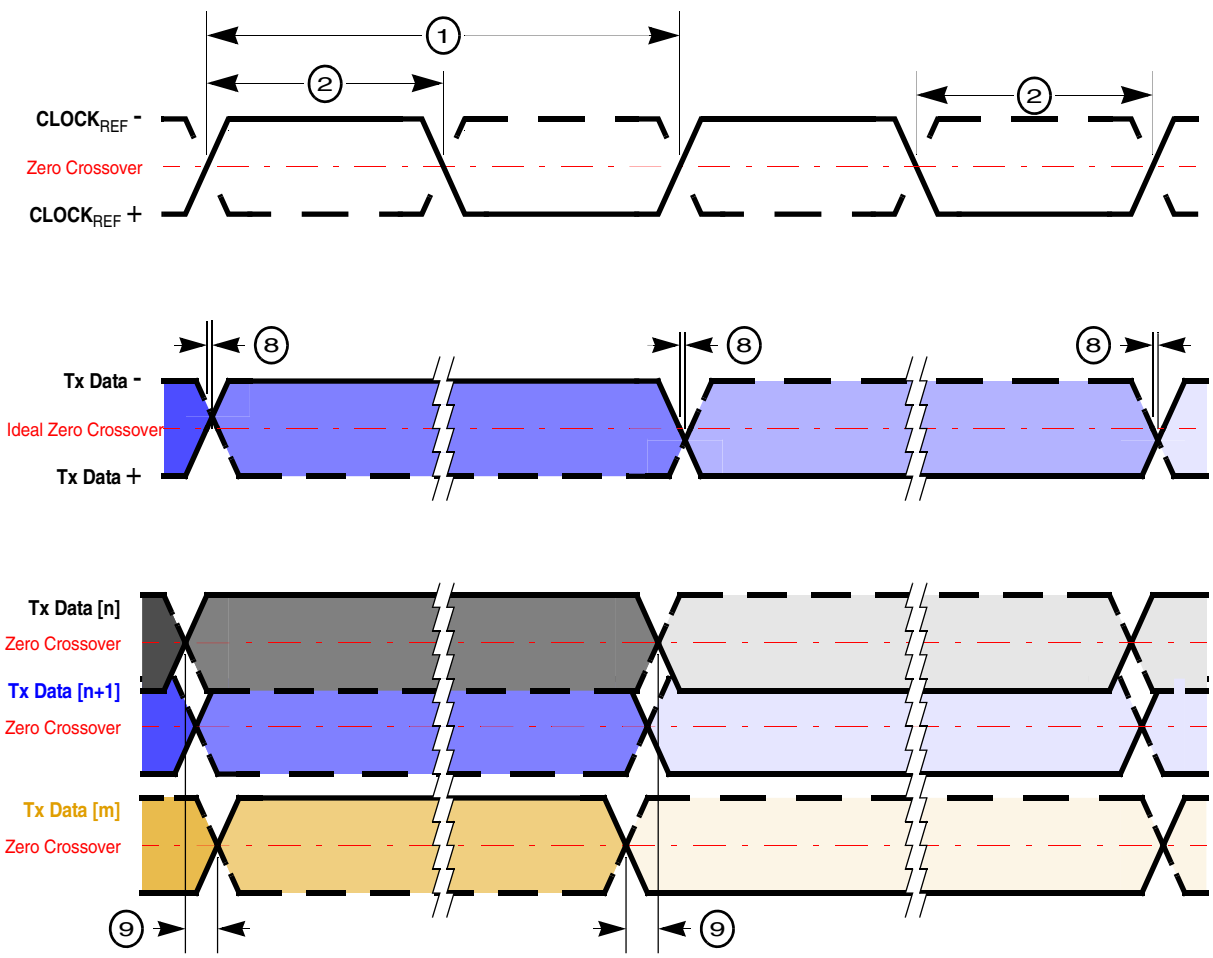



**Figure 34. Nexus Aurora timings**

## 6.5 WKPU/NMI timing

**Table 44. WKPU/NMI glitch filter**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $W_{FNMI}$ | NMI pulse width that is rejected | — | — | 20 | ns |
| $W_{NFNMI}$ | NMI pulse width that is passed | 400 | — | — | ns |

## 6.6 External interrupt timing (IRQ pin)

**Table 45. External interrupt timing**

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | $t_{IPWL}$ | IRQ pulse width low | — | 3 | — | $t_{CYC}$ |
| 2 | $t_{IPWH}$ | IRQ pulse width high | — | 3 | — | $t_{CYC}$ |
| 3 | $t_{ICYC}$ | IRQ edge to edge time[1] | — | 6 | — | $t_{CYC}$ |

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both

**NOTE**

tCYC is equivalent to TCK given in SIUL2 chapter of the reference manual.

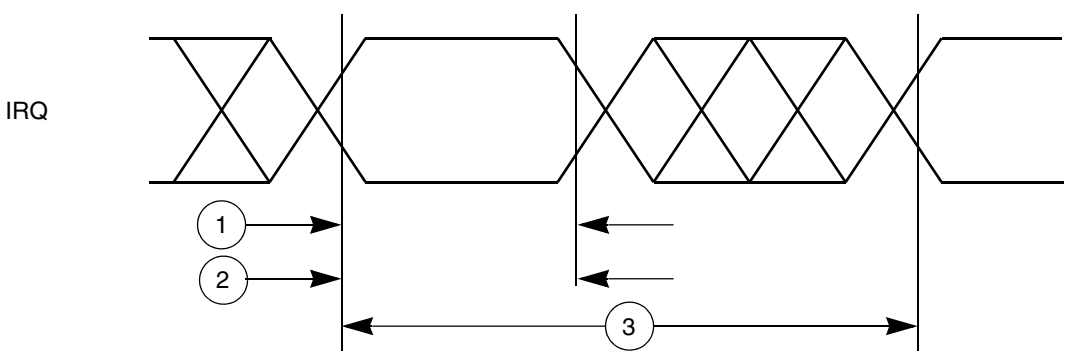



**Figure 35. External interrupt timing**

## 6.7 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

### Table 46. Temperature sensor electrical characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| — | Temperature monitoring range | | -40 | — | 150 | °C |
| $T_{SENS}$ | Sensitivity | | — | 5.18 | — | mV/°C |
| $T_{ACC}$ | Accuracy | $T_J$ = -40 to 150°C | 5 | — | 5 | °C |

# 7 I²C timing

### Table 47. I²C SCL and SDA input timing specifications

| Number | Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | I_tHD:STA | Start Condition hold time | 2 | - | Peripheral clock |
| 2 | I_t_LOW | Clock low time | 8 | - | |
| 3 | I_tHD:DAT | Data hold time | 2 | - | |
| 4 | I_tHIGH | Clock high time | 4 | - | |
| 5 | I_tSU:DAT | Data setup time | 4 | - | |
| 6 | I_tSU:STA | Start condition setup time (for repeated start condition only) | 2 | - | |
| 7 | I_tSU:STOP | Stop condition setup time | 2 | - | |

### Table 48. I²C SCL and SDA output timing specifications

| Number | Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | O_tHD:STA | Start condition hold time[1] | 6 | - | Peripheral clock |
| 2 | O_t_LOW | Clock low time[1] | 10 | - | |
| 3 | O_tHD:DAT | Data hold time[1] | 7 | - | |
| 4 | O_t_HIGH | Clock high time[1] | 10 | - | |
| 5 | O_tSU:DAT | Data setup time[1] | 2 | - | |
| 6 | O_tSU:STA | Start condition setup time (for repeated start condition only)[1] | 20 | - | |
| 7 | O_tSU:STOP | Stop condition setup time[1] | 10 | - | |
| 8 | O_tr | SCL/SDA rise time[2] | - | 99.6 | ns |
| 9 | O_tf | SCL/SDA fall time[1] | - | 99.6 | |

1. Programming IBFD (I²C Bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IBDR.
2. Serial data (SDA) and Serial clock (SCL) reaches peak level depending upon the external signal capacitance and pull up resistor values as SDA and SCL are open-drain type outputs which are only actively driven low by the I²C module.

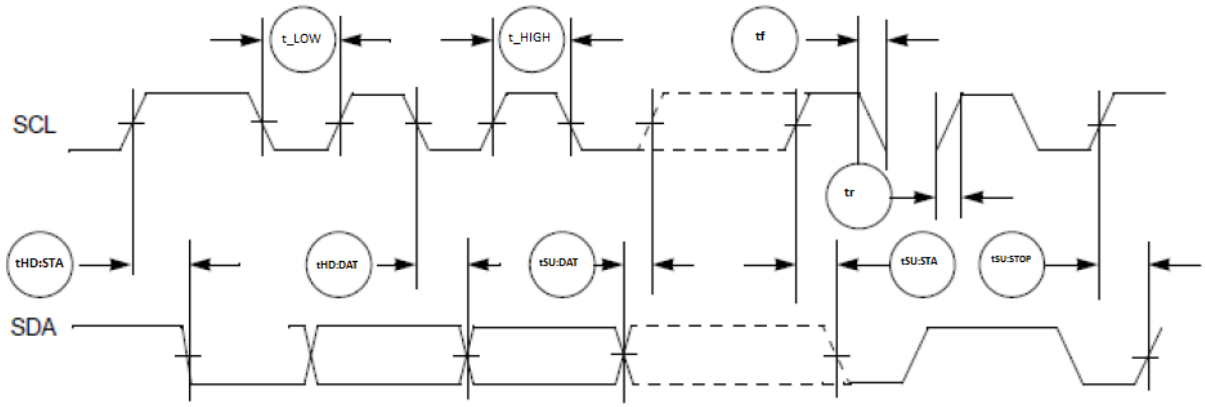



**Figure 36. I²C input/output timing**

# 8 Thermal Specifications

## 8.1 Thermal characteristics

**NOTE**

Thermal characteristics are targets based on simulation that are subject to change per device characterization.

**Table 49. Thermal characteristics for 356 MAPBGA package**

| Symbol | Parameter | Conditions | 356 MAPBGA | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient natural convection[1, 2] | Single layer board - 1s[3] | 36.7 | °C/W |
| | | Four layer board - 2s2p[4] | 22.1 | |
| $R_{\theta JMA}$ | Thermal resistance, junction-to-ambient forced convection at 200 ft/min[1] | Single layer board - 1s[3] | 26.8 | °C/W |
| | | Four layer board - 2s2p[4] | 17.0 | |
| $R_{\theta JB}$ | Thermal resistance junction-to-board[5] | — | 12.1 | °C/W |
| $R_{\theta JC}$ | Thermal resistance junction-to-case[6] | — | 5.0 | °C/W |
| $\Psi_{JT}$ | Junction-to-package-top natural convection[7] | — | 0.1 | °C/W |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. Board temperature is measured on the top surface of the board near the package.
6. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

7. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

### 8.1.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, $T_J$, can be obtained from this equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

- $T_A$ = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $P_D$ = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

- $T_T$ = thermocouple temperature on top of the package (°C)
- $\Psi_{JT}$ = thermal characterization parameter (°C/W)
- $P_D$ = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

### 8.1.2 References

Semiconductor Equipment and Materials International; 3081 Zanker Road; San Jose, CA 95134 USA; (408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the Web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

# 9 Packaging

The MPC5775K is offered in the following package types.

| If you want the drawing for this package | Then use this document number |
|---|---|
| 356-ball MAPBGA | 98ASA00478D |

**NOTE**

For detailed information regarding package drawings, refer to www.nxp.com

# 10 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

## 10.1 Reset sequence duration

Table 51 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Reset sequence description.

**Table 51. RESET sequences**

| No. | Symbol | Parameter | $T_{Reset}$ | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max[1] | |
| 1 | $T_{DRB}$ | Destructive Reset Sequence, BIST enabled | 15 | | 50 | ms |
| 2 | $T_{DR}$ | Destructive Reset Sequence, BIST disabled | 400 | | 2000 | µs |
| 3 | $T_{ERLB}$ | External Reset Sequence Long, BIST enabled | 15 | | 50 | ms |
| 4 | $T_{FRL}$ | Functional Reset Sequence Long, BIST disabled | 400 | | 2000 | µs |
| 5 | $T_{FRS}$ | Functional Reset Sequence Short, BIST disabled | 1 | | 500 | µs |

1. The maximum value is applicable only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

## 10.2 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The doted lines in the figures indicate the starting point and the end point for which the duration is specified in Table 51.

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The SMPS self test is always triggered during Phase3 after a destructive reset so that duration is included into Phase3 below.

In external regulation mode, the VREG_POR_B pin should be de-asserted only when all the design supplies are in operating range. Deassertion of VREG_POR_B pin triggers the start of reset sequence in internal as well as external regulation modes.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

**NOTE**

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in Table 51 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

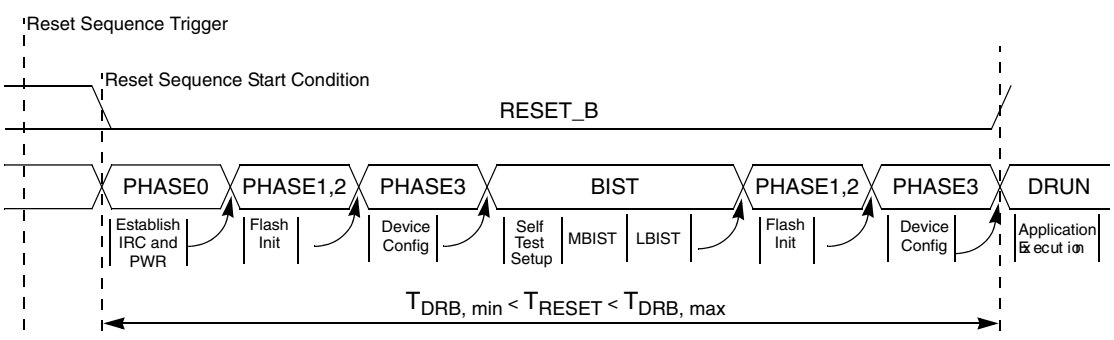



**Figure 37. Destructive reset sequence, BIST enabled**

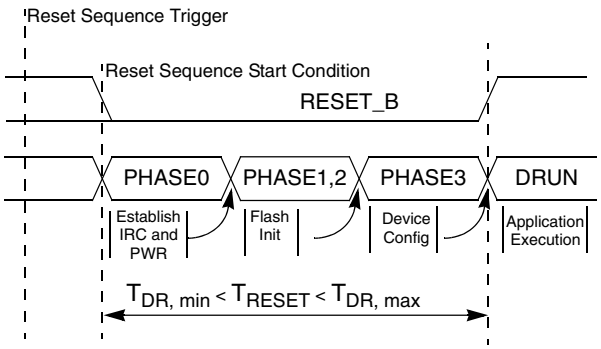



**Figure 38. Destructive reset sequence, BIST disabled**

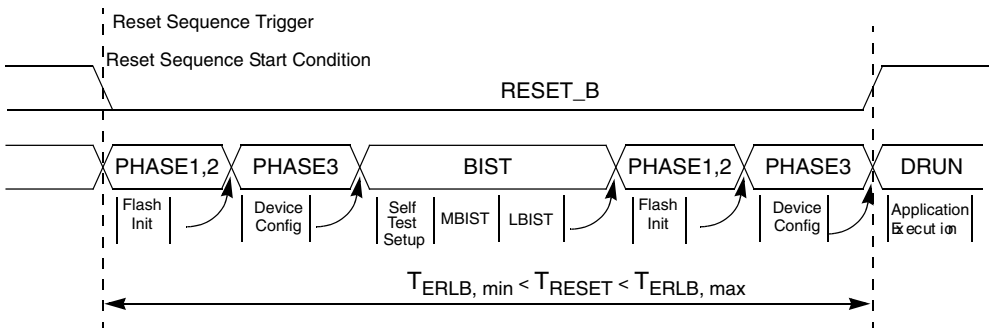



**Figure 39. External reset sequence long, BIST enabled**

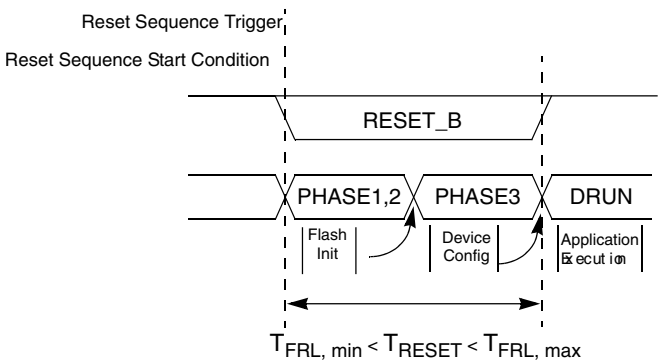



**Figure 40. Functional reset sequence long**

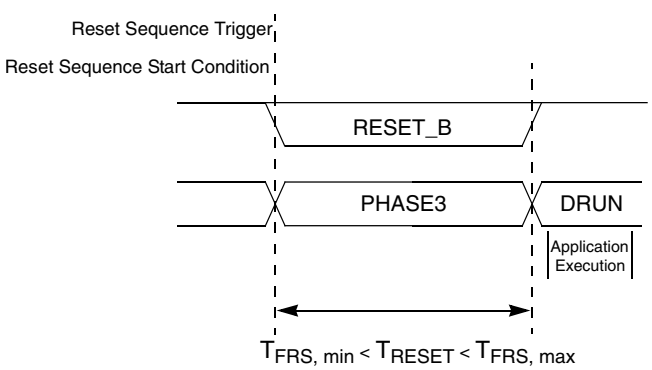



**Figure 41. Functional reset sequence short**

The reset sequences shown in Figure 40 and Figure 41 are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

# 11 Power sequencing requirements

The device does not require any specific power sequencing as far as user follows recommendations in this section.

As mentioned in the previous section, it is expected that the external ASIC which powers up the device in external regulation mode deasserts VREG_POR_B pin only when all the power supplies to the design are in operating range.

It should be noted that LVD and HVD detectors on VDD supply are disabled by default in external regulation mode for preventing a conflict with external regulator operation but they can be enabled by software once design is powered up.

While designing the system, it is important to ensure that AFE supplies are powered up before data is sent on its input pads.

# 12 Release Notes

- Editorial changes
- Changed freescale.com to nxp.com throughout the document
- Added sub document title "Supports MPC5774K and MPC5775K".
- In Table 2, updated footnote for Supply ramp rate from “$TV_{DD}$ is relevant for all supplies” to “$TV_{DD}$ is relevant for all external supplies”. Deleted footnote "Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined".
- In Table 3, modified “Input voltages on EXTAL, XTAL” to “EXTAL external clock input low voltage” and “EXTAL external clock input high voltage”. Also, updated max value of “Rise/fall time of EXTAL external clock Input” from 250 to 1000 ps.
- In Table 4, updated footnote in maximum value of Flash operating current from “Peak Flash current measured during read while write (RWW)” to “Peak Flash current measured during read while write (RWW) operation.”
- In Table 5, added Internal switched regulator gatedriver pull-up resistance (VREGSWPUP) specifications and conditions; deleted the footnote “Gate driver pin VREG_SWP should NOT be pulled to ground on board".
- In Table 12, changed maximum value of Rise/Fall Edge of SRC=10@25 pF from 3.9/3.5 ns to 3.5/3.5 ns.
- In Table 16, maximum value for Weak pull-down current absolute value (Iwpd) has been changed from 80 to 100 µA.
- In Table 38 added footnote “Valid for PDI Data 11 to PDI Data 0. PDI Data 15 to PDI Data 12 tPDISetup is 8” in $t_{PDISetup}$.
- In Table 41, minimum values of “Data setup time for inputs” for Master (MTFE = 1, CPHA = 0), "Data hold time for outputs" for Master (MTFE = 1, CPHA = 0), and "Data hold time for inputs" for Master (MTFE = 1, CPHA = 0) have been modified. Also, updated SCK duty cycle.
- Updated the topic DSPI timing by adding introductory paragraph and updated the table "DSPI timing".

| |
|---|
| • In JTAG/CJTAG interface timing , added the paragraph “The following table lists JTAGC/CJTAG electrical characteristics...” and updated TCK Cycle Time.<br>• Added topic $I^2C$ timing .<br>• In Power sequencing requirements, deleted the statement "Design may experience 1 mA crossover currents if VDD supply is ramped up before VDD_HV_FLA supply rail and a 30 mA crossover current if VDD is ramped after VDD_HV_FLA. This current is only an electrical crossover but has no functional implication". |
| • Changed footer throughout the document |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Revision 9.1 10/2016