IW610

1x1 Wi-Fi 6 and Bluetooth Low Energy/802.15.4 Solution Family

Rev. 7.0 — 5 December 2024 Product data sheet

1 Product overview

The IW610 family is a highly integrated, low-power single-chip solution with Wi-Fi 6 + Bluetooth Low Energy (LE) 5.4 / 802.15.4 radios designed for a broad array of applications. Applications include imaging, connected smart home devices, smart accessories, smart energy, enterprise industrial, and building automation.

The IW610 includes a 1x1 20 MHz Wi-Fi 6 (802.11ax) subsystem bringing higher throughput, better network efficiency, lower latency, and improved range over previous generation Wi-Fi standards. The Bluetooth LE radio supports 2 Mbit/s high-speed data rate, long range, and extended advertising. The on-chip 802.15.4 radio can support Thread mesh networking protocol. The IW610 is an ideal device for Matter applications running over Wi-Fi and Thread. The IW610 can operate as a Matter Controller as well as Thread Border Router. This capability enables full Matter functionality for local and cloud-based control, and for monitoring of IoT products seamlessly across major ecosystems.

EdgeLock™ security technology of NXP is incorporated, providing secure boot, secure debug, secure firmware download, and secure life cycle management. Asymmetric and symmetric cryptography is hardware accelerated and a Physically Unclonable Function (PUF) enables secure key management. IW610 targets SESIP Level 3 security certification, IEC-62443 and EU RED, article 3(3) cybersecurity compliance, and is UN R155 ready.

The advanced design of the IW610 delivers tight integration, low power, and highly secure operation in a space- and cost-efficient single-chip requiring only a single 3.3 V power supply.

Table 1 lists IW610 variants.

Table 1. IW610 variants

Product name	Features	Package
IW610B	1x1 Single-band 2.4 GHz Wi-Fi 6+ Bluetooth LE	DRQFN, WLCSP
IW610C	1x1 Single-band 2.4 GHz Wi-Fi 6 + Bluetooth LE/802.15.4	DRQFN, WLCSP
IW610F	1x1 Dual-band (2.4 GHz / 5 GHz) Wi-Fi 6 + Bluetooth LE	DRQFN, WLCSP
IW610G[1]	1x1 Dual-band (2.4 GHz / 5 GHz) Wi-Fi 6 + Bluetooth LE/802.15.4	DRQFN, WLCSP

[1] IW610G is used as example in most figures and tables in the data sheet.

Figure 1 and Figure 2 show the application diagrams for one-antenna configuration and the super-set parts (IW610G and IW610C).

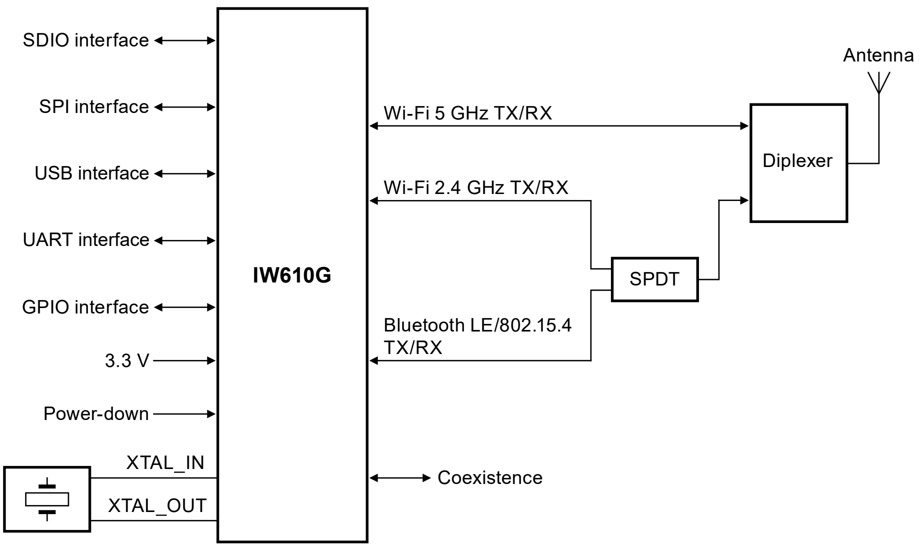

Figure 1. IW610G application diagram – One antenna and dual-band Wi-Fi

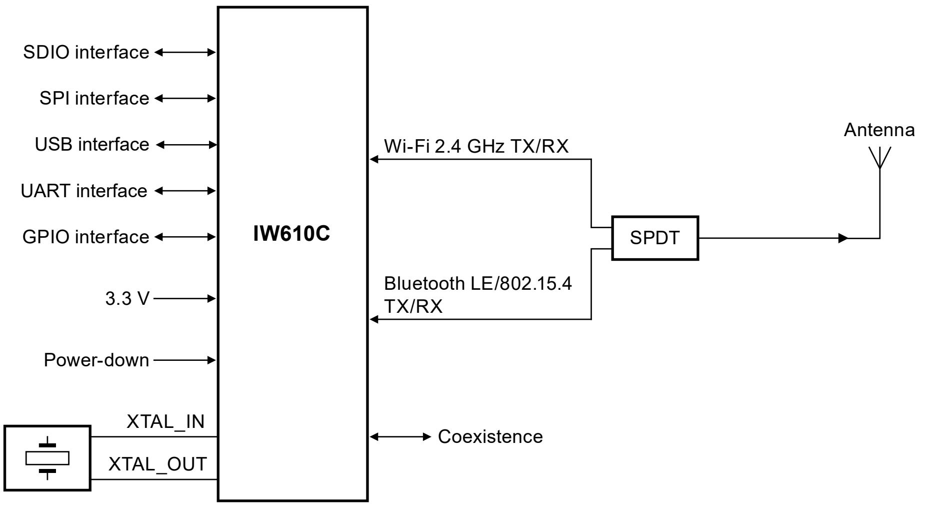

Figure 2. IW610C application diagram – One antenna and single-band Wi-Fi

Figure 3 and Figure 4 show the application diagrams for the two-antenna configuration and the super-set parts (IW610G and IW610C).

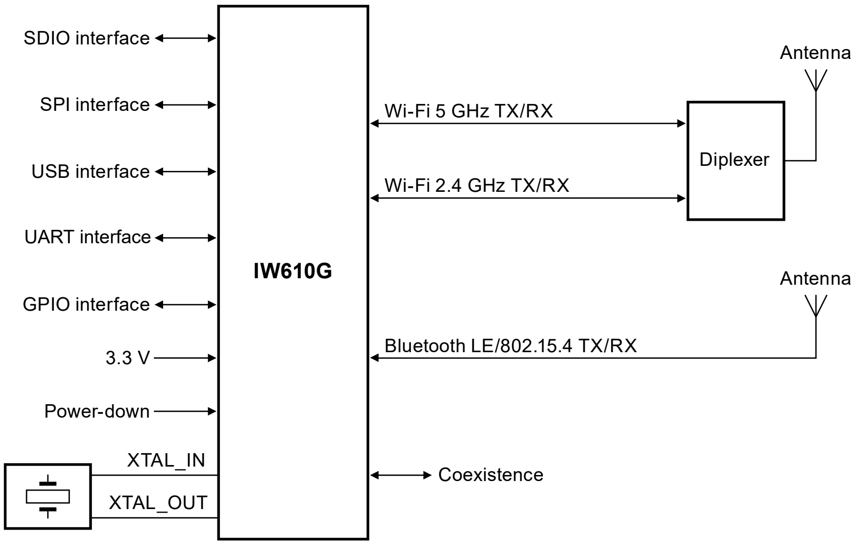

Figure 3. IW610G application diagram – Two antennas and dual-band Wi-Fi

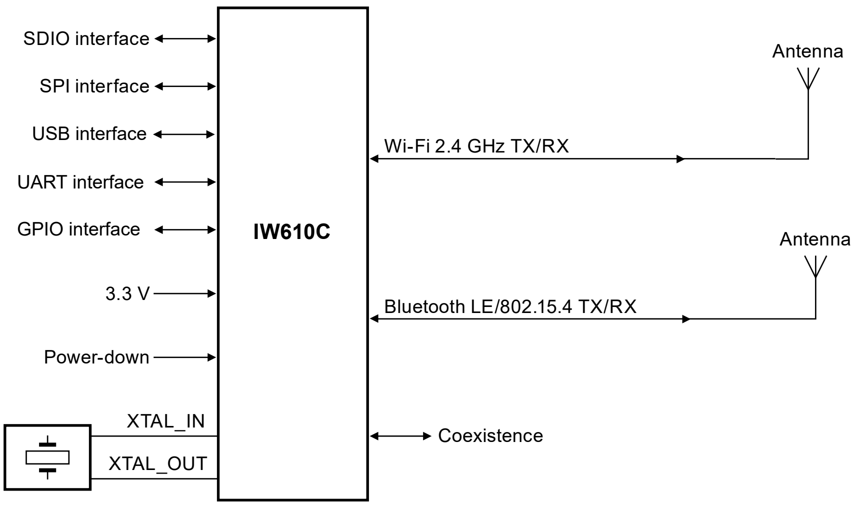

Figure 4. IW610C application diagram – Two antennas and single-band Wi-Fi

1.1 Applications

- **Smart home**: smart outlet, light switch, security camera, thermostat, sprinkler controller, door lock, door bell, garage door, security system, and smart display
- **Imaging**: printer, digital still camera (DSC)
- **Industrial**: building management, smart lighting, security / physical access, Point of Sale (POS) terminals, EV chargers, smart meters, solar inverters, heat pumps
- **Smart devices**—air purifier, pet monitor, weighing scale, glucometer, blood pressure monitor, fitness equipment
- **Smart appliances**—refrigerator, washer, dryer, oven range, microwave, dishwasher, water heater, air conditioner, robotic vacuum cleaner
- **Smart accessories**— alarm clock, remote control
- **Gateways**—Multi-radio hub/smart device gateway to/for Internet/IP connectivity

1.2 Wi-Fi 6 (802.11ax) key features

- 1x1 dual-band 2.4 GHz/5 GHz Wi-Fi 6 radio
- Integrated Wi-Fi PA, LNA, and T/R switch, up to +23 dBm TX power
- 20 MHz channel operation
- Wi-Fi 6 Target Wake Time (TWT) support
- Wi-Fi 6 Extended Range (ER) and Dual Carrier Modulation (DCM)
- Low-power Wi-Fi idle, standby, and sleep modes
- WPA2/WPA3 security
- Support for Matter over Wi-Fi
- Antenna diversity

1.3 Narrowband key features

- Integrated PA / LNA / Switch with up to +15 dBm TX output

1.3.1 Bluetooth LE key features

- Bluetooth Low Energy 5.4
- Bluetooth LE 1 Mbps and 2 Mbps high-speed uncoded modes, and Long Range operation (125 kbps and 500 kbps coded data rates)

1.3.2 802.15.4 radio key features

- IEEE 802.15.4-2015 compliant MAC
- Support for Matter over Thread

1.4 Host interfaces

Table 2 shows the host interface options for IW610 variants.

Table 2. IW610 host interfaces

Variant	Wi-Fi	Bluetooth LE	802.15.4
IW610C	SDIO 3.0	UART	SPI
	USB 2.0	USB 2.0	SPI
IW610F, IW610B	SDIO 3.0	UART	—
	USB 2.0	USB 2.0	—
IW610G	SDIO 3.0	UART	SPI
	USB 2.0	USB 2.0	SPI

1.5 Operating characteristics

- Supply voltage: 3.3 V
- Operating temperature
  - Industrial: -40 to 85°C
- Storage temperature: -55 to 125°C

1.6 General features

1.6.1 Package options

- DRQFN: 8 mm x 7.5 mm x 0.85 mm with 0.4 mm pitch (single rows and corners) or 0.5 mm pitch (dual rows)
- WLCSP: 4.495 mm x 4.0 mm x 0.455 mm with 0.33 mm pitch

1.6.2 Coexistence

- Internal coexistence between Wi-Fi and Bluetooth LE or 802.15.4
- External coexistence interface for connection to external radios such as LTE

1.6.3 Power management

- Efficient power management system
- Deep-sleep low-power mode
- Integrated high-efficiency buck DC-DC converter
- Wake-up through GPIO, host interface, and timers

1.6.4 Memory

- One Time Programmable (OTP) memory to store the MAC address and calibration data

1.6.5 Security

- Targeting SESIP Level 3 security certification
- IEC-62443 and Radio Equipment Directorate (RED) article 3(3) cybersecurity compliance
- Targeting NXP EdgeLock™ assurance program
- Hardware root of trust
- Authenticated and secured boot
- Secure debug
- Hardware cryptography accelerators (for example symmetric, asymmetric, secure hash, and key management)
- True random number generator (TRNG)
- Physically unclonable function (PUF)
- OTP-based secure device configuration and life cycle management
- Resistant to supply voltage glitching attacks

1.7 Internal block diagram

Figure 5 shows IW610G internal block diagram.

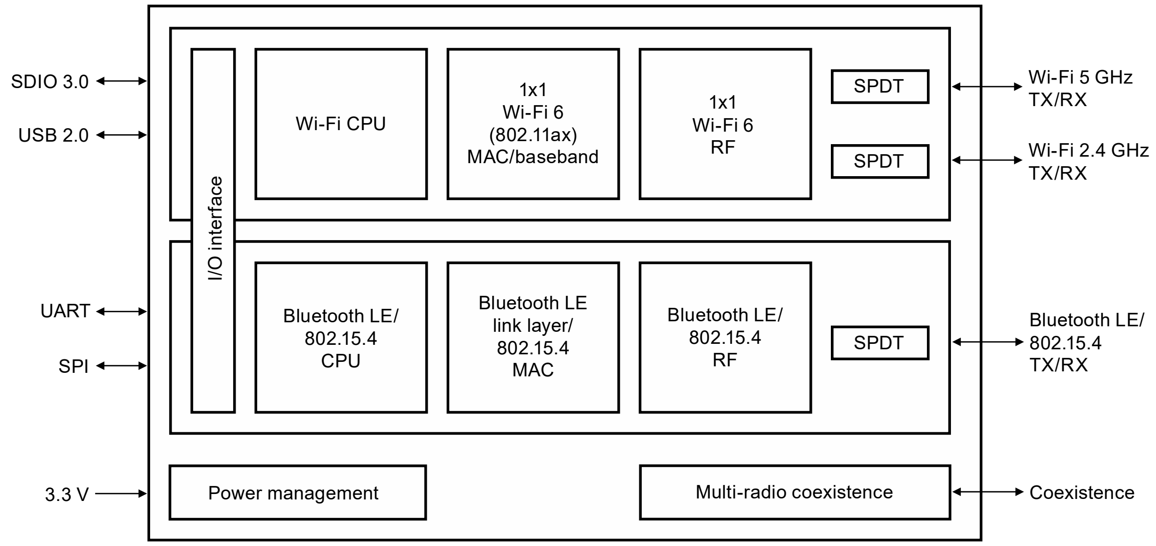

Figure 5. IW610G internal block diagram

2 Ordering information

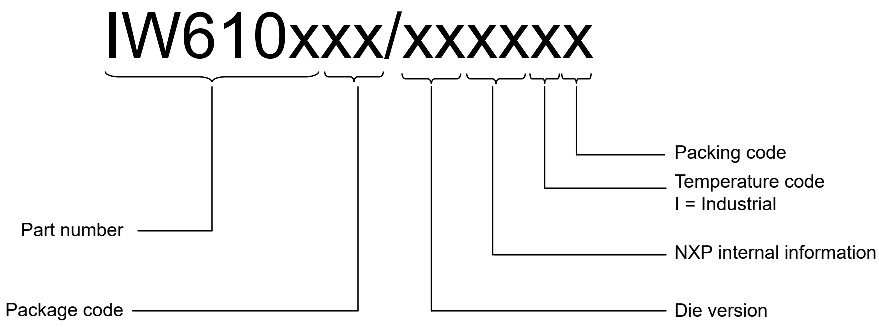

Figure 6. Part numbering scheme

Table 3. Part order codes

Part order code	Package type	Operating temperature range	Packing
IW610B			
IW610BHN/A1ZDIK	DRQFN 8 mm x 7.5 mm x 0.85 mm with 0.4/0.5 mm pitch	Industrial	Tray
IW610BHN/A1ZDIMP	DRQFN 8 mm x 7.5 mm x 0.85 mm with 0.4/0.5 mm pitch	Industrial	Tape and reel
IW610BUK/A1ZDIZ	WLCSP 4.495 mm x 4.0 mm x 0.455 mm with 0.33 mm pitch	Industrial	Tape and reel
IW610C			
IW610CHN/A1ZDIK	DRQFN 8 mm x 7.5 mm x 0.85 mm with 0.4/0.5 mm pitch	Industrial	Tray
IW610CHN/A1ZDIMP	DRQFN 8 mm x 7.5 mm x 0.85 mm with 0.4/0.5 mm pitch	Industrial	Tape and reel
IW610CUK/A1ZDIZ	WLCSP 4.495 mm x 4.0 mm x 0.455 mm with 0.33 mm pitch	Industrial	Tape and reel
IW610F			
IW610FHN/A1ZDIK	DRQFN 8 mm x 7.5 mm x 0.85 mm with 0.4/0.5 mm pitch	Industrial	Tray
IW610FHN/A1ZDIMP	DRQFN 8 mm x 7.5 mm x 0.85 mm with 0.4/0.5 mm pitch	Industrial	Tape and reel
IW610FUK/A1ZDIZ	WLCSP 4.495 mm x 4.0 mm x 0.455 mm with 0.33 mm pitch	Industrial	Tape and reel
IW610G			
IW610GHN/A1ZDIK	DRQFN 8 mm x 7.5 mm x 0.85 mm with 0.4/0.5 mm pitch	Industrial	Tray
IW610GHN/A1ZDIMP	DRQFN 8 mm x 7.5 mm x 0.85 mm with 0.4/0.5 mm pitch	Industrial	Tape and reel
IW610GUK/A1ZDIZ	WLCSP 4.495 mm x 4.0 mm x 0.455 mm with 0.33 mm pitch	Industrial	Tape and reel

3 Wi-Fi subsystem

3.1 IEEE 802.11 standards

- 802.11ax 1x1 MU-MIMO (STA mode)
- 802.11ac Wave 1/2
- 802.11n/a/g/b
- 802.11e quality of service
- 802.11i enhanced security
- 802.11k radio resource measurement
- 802.11r fast hand-off for AP roaming
- 802.11v Basic Service Set (BSS) Transition Management (BTM) for frame transmission and/or reception
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode
- 802.1X Wi-Fi security and authentication

3.2 Wi-Fi MAC

- 802.11ax 1x1 MU-MIMO MAC
- Trigger frame formats
  - Basic trigger frame
  - MU-BAR, MU-RTS, Beamforming Report Poll (BFRP), BSR Poll (BSRP) trigger variant
  - Trigger frame MAC padding
- HE Variants of HT Control
  - Basic format
  - UL Power Headroom
  - Receive Operation Mode control sub-field
- HE MU Frame Exchange Sequences
- MU Acknowledgment (ACK)
- M-BA and C-BA Variants in BA Frames
- Target Wait Time Scheduling
- HE Dual-NAV
- UL Carrier Sensing
- Buffer Status Reports in response to BSRP trigger frame
- Operating Mode Indication (OMI)
- Multiple-BSS/Station
- A-MPDU Rx (de-aggregation) and Tx (aggregation) (supports single-MPDU A-MPDU)
- Management information base counters

3.3 Wi-Fi baseband

- 802.11ax 1x1 baseband, backward compatible with 802.11ac/n/a/g/b technology
- Bandwidth support
  - 20 MHz
- Modulation and coding schemes (MCS)
  - 802.11ax—MCS0~9
  - 802.11ac—MCS0~8
  - 802.11n—MCS0~7
  - Dual sub-carrier modulation (DCM)
    . MCS0
  - BCC coding
- Frame formats
  - 802.11ax HE_SU (UL/DL)
  - 802.11ax HE_MU (DL)
  - 802.11ax HE_ER_SU (UL/DL)
  - 802.11ax HE_TB (UL)
  - 802.11ac VHT
  - 802.11n HT
  - 802.11a
  - 802.11g
  - 802.11b
  - Channel state information (CSI)

- UL MU-MIMO and OFDMA (STA to AP transmit)
- DL MU-MIMO and OFDMA (AP to STA receive)
- Aggressive packet extension
- Extended range (ER)
  - Target wait time (TWT)
  - Dual carrier modulation (DCM)
- Receiver beam change
- Guard interval (GI) modes
  - 1x HE-LTF with 1.6 us GI (for UL TB PPDU)
  - 2x HE-LTF with 0.8 us GI
  - 2x HE-LTF with 1.6 us GI
  - 4x HE-LTF with 3.2 us GI
  - 4x HE-LTF with 0.8 us GI
- Optional 802.11ac and 802.11n MIMO features:
  - 20 MHz coexistence with middle-packet detection (GI detection) for enhanced clear channel assessment (CCA)
  - Short guard interval (0.4 us)
  - RIFS on receive path for 802.11n packets
  - VHT MU-PPDU (receive)
- Spectral intelligence
  - Spectrum monitoring
  - Interference identification/classification
- Power save features

3.4 Wi-Fi radio

- 5 GHz and 2.4 GHz Wi-Fi band operation
- 802.11ax 1x1 on-chip RF radio
- Integrated PA, LNA and T/R switch

3.5 Wi-Fi encryption

- Data Frame Encryption/Decryption
  - WPA/WPA2/WPA3-enterprise
  - AES/CCMP
  - AES/GCMP
- Management Frame Encryption/Decryption for broadcast/multicast packets
  - AES/CMAC
  - AES/GMAC
- Management Frame Encryption/Decryption for unicast packets
  - AES/CCMP
  - AES/GCMP

3.6 Transmit beamforming (TxBF)

- 802.11ax/ac/n Explicit Beamformee
  - Supports sounding feedback for up to 4x4 Beamformer

3.7 RF channels

Table 4 shows the list of supported 2.4 GHz and 5 GHz channels.

Table 4. Wi-Fi channel list

Channel number	Frequency	Channel number	Frequency	Channel number	Frequency
2.4 GHz channel					
1	2412 MHz	2	2417 MHz	3	2422 MHz
4	2427 MHz	5	2432 MHz	6	2437 MHz
7	2442 MHz	8	2447 MHz	9	2452 MHz
10	2457 MHz	11	2462 MHz	12	2467 MHz
13	2472 MHz	—	—	—	—
5 GHz channel					
36	5180 MHz	40	5200 MHz	44	5220 MHz
48	5240 MHz	52	5260 MHz	56	5280 MHz
60	5300 MHz	64	5320 MHz	100	5500 MHz
104	5520 MHz	108	5540 MHz	112	5560 MHz
116	5580 MHz	120	5600 MHz	124	5620 MHz
128	5640 MHz	132	5660 MHz	136	5680 MHz
140	5700 MHz	144	5720 MHz	149	5745 MHz
153	5765 MHz	157	5785 MHz	161	5805 MHz
165	5825 MHz	169	5845 MHz	173	5865 MHz
177	5885 MHz	—	—	—	—

3.8 Wi-Fi host interfaces

- SDIO 3.0 (4-bit SDIO) with transfer rates up to SDR104 (208 MHz)
- USB 2.0 Device

4 Narrowband subsystem

The narrowband radio can be configured to be either Bluetooth Low Energy or IEEE 802.15.4.

4.1 Bluetooth LE features

- Bluetooth LE 5.4 certified
- Bluetooth LE 5.2 features supported
- Supports up to 16 simultaneous central/peripheral connections
- Wi-Fi/Bluetooth coexistence protocol support
- Encryption (AES-CCM) support
- Intelligent Adaptive Frequency Hopping (AFH)
- Bluetooth LE Privacy 1.2
- Bluetooth LE Secure Connection
- Bluetooth LE Data Length Extension
- Bluetooth LE Advertising Extension
- Bluetooth LE Long Range
- Bluetooth LE Power Control
- Bluetooth LE 2 Mbps
- Bluetooth LE Isochronous Channels

4.2 802.15.4 radio features (IW610G and IW610C only)

- IEEE 802.15.4-2015 compliant supporting Matter over Thread in 2.4 GHz band
- MAC accelerator with packet formatting, CRCs, address check, auto-acks and timers
- Programmable packet filtering for lower power consumption
- Timestamp for transmit and receive packets using a free running microsecond timer
- Enhanced Acknowledgment support
- Wi-Fi/802.15.4 coexistence protocol support
- Received Signal Strength Indication (RSSI) of received packets
- 128-bit AES security

4.3 Narrowband subsystem host interfaces

Host interfaces for Bluetooth LE

- High-Speed UART with support up to 4 Mbps baud rate

Host interfaces for 802.15.4 radio (IW610G and IW610C only)

- SPI with maximum clock speed of 10 MHz

5 Coexistence (Wi-Fi and Bluetooth LE/802.15.4)

5.1 Antenna configurations

The IW610 supports two antenna configurations: single-antenna and dual-antenna configurations.

5.1.1 Dual-antenna configuration

The two separate antennas allow simultaneous independent operation of the Wi-Fi and narrowband (Bluetooth LE/802.15.4) radios.

Table 5 shows the supported TX and/or RX operations with IW610G dual-antenna configuration and high antenna isolation of ≥36 dB.

Table 5. Wi-Fi, Bluetooth LE, and 802.15.4 supported TX and or RX operations - Dual-antenna configuration (IW610G)

Row number	Bluetooth LE	802.15.4	Wi-Fi 2.4 GHz	Wi-Fi 5 GHz
1	TX/RX	—	—	TX/RX
2	—	TX/RX	—	TX/RX
3	TX/RX	—	TX/RX	—
4	—	TX/RX	TX/RX	—

5.1.2 Single-antenna configuration

In single-antenna configuration, there is arbitration for the transmit operation of the Wi-Fi 2.4 GHz and narrowband radios.

Table 6 shows the supported TX and/or RX operations with IW610G single-antenna configuration.

Table 6. Wi-Fi and narrowband supported TX and or RX operations - Single-antenna configuration (IW610G)

Row #	narrowband (Bluetooth LE or 802.15.4)	Wi-Fi 2.4 GHz	Wi-Fi 5 GHz
1	TX	—	TX/RX
2	—	TX	—
3	—	RX	—
4	RX	—	TX/RX

In single-antenna configuration:

- Wi-Fi 2.4 GHz and narrowband TX operations are arbitrated (rows 1 and 2)
- Wi-Fi 2.4 GHz and narrowband RX operations are arbitrated (rows 3 and 4)
- Wi-Fi 5 GHz TX/RX and narrowband RX or TX operations are simultaneous (rows 1 and 4)
- Only one of the narrowband radios (Bluetooth LE or 802.15.4) can perform TX or RX operation

5.2 Central hardware packet traffic arbiter

The central hardware packet traffic arbiter arbitrates the transmit and/or receive operations between the on-chip Wi-Fi and narrowband radios as per the supported hardware configuration. See Section 5.1.

In addition to the on-chip radios, the central hardware packet traffic arbiter arbitrates one external radio. Refer to Section 5.3.

5.3 Coexistence with an external radio

WCI-2 and PTA external coexistence interfaces are used for the coexistence with an external radio.

Note: *The WCI-2 coexistence interface and the PTA external coexistence interface share the same multi-function pins (MFP). Refer to Section 6.6.1 "General purpose I/O (GPIO)" for more details.*

WCI-2 external coexistence interface

WCI-2 is the two-wire wireless coexistence interface 2 protocol defined in the Bluetooth Core Specification (Vol 7 Part C).

Figure 7 illustrates the hardware coexistence interface between the central hardware packet traffic arbiter and the external radio. In the figure, Wireless SoC is IW610G.

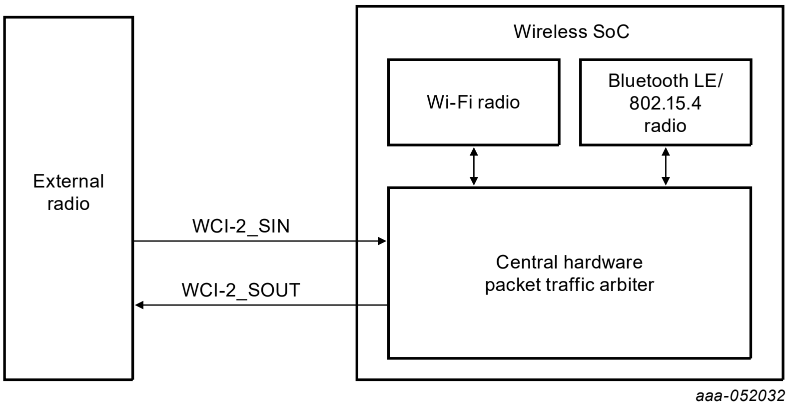

Figure 7. Hardware coexistence interface - WCI-2 coexistence interface

Note: *Refer to Section 6.6.9 for the description of WCI-2 coexistence interface signals.*

PTA external coexistence interface

Figure 8 illustrates the hardware coexistence interface between the central hardware packet traffic arbiter and the external radio. In the figure, Wireless SoC is IW610G.

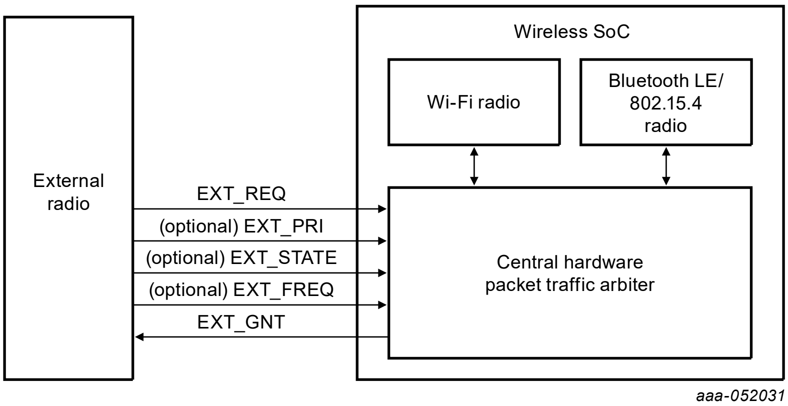

Figure 8. Hardware coexistence interface - PTA external coexistence interface

Note: *Refer to Section 6.6.10 for the description of PTA external coexistence interface signals.*

6 Pin information

6.1 Signal diagram

Note: *Some signals are muxed on dedicated pins. See [Section 6.6 "Pin description"] for the dedicated pin/ muxed signal descriptions.*

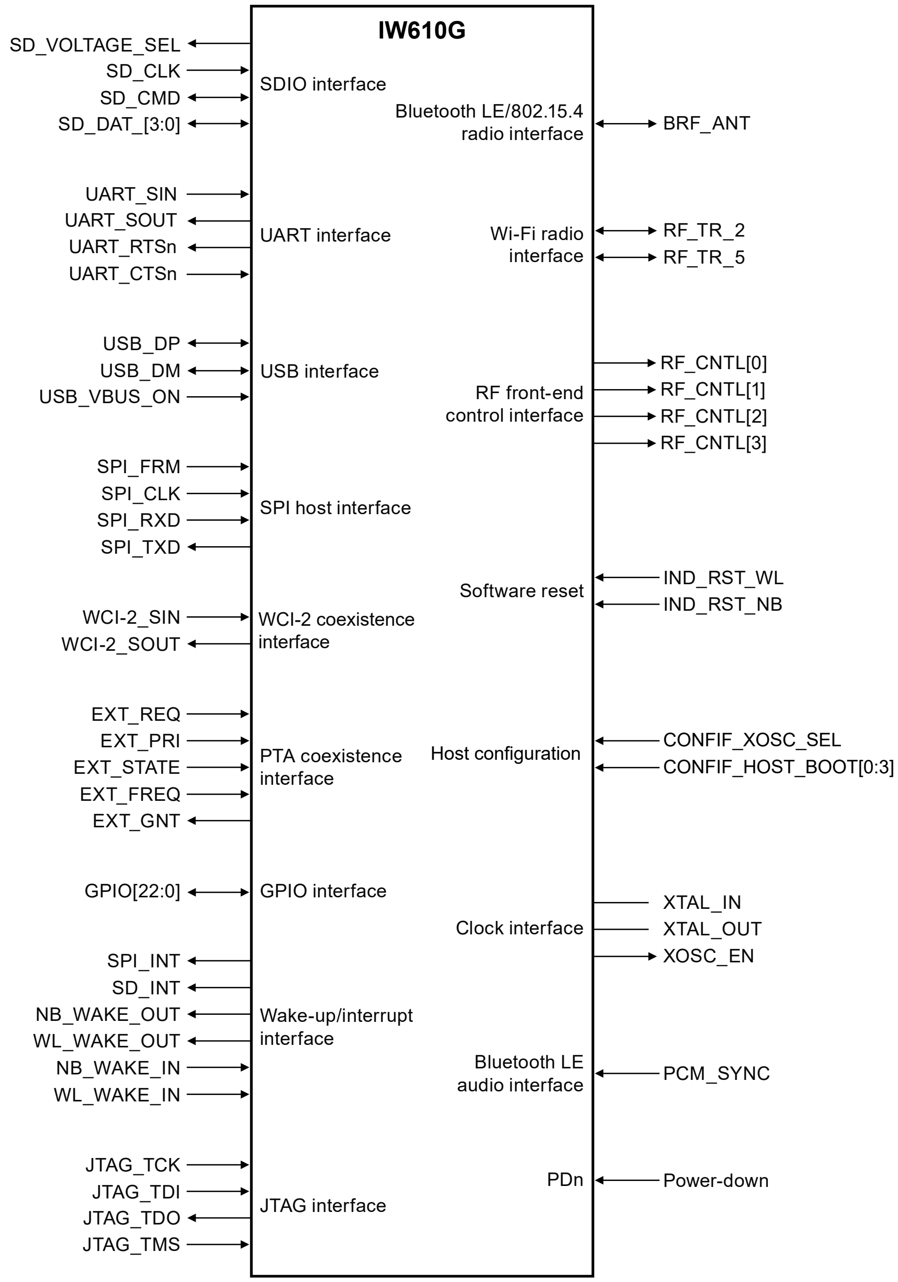

Figure 9. Signal diagram for IW610G

6.2 Pin assignment

Table 7 shows the signals and modes supported by IW610 variants.

Table 7. Signals and modes supported by IW610 variants

Signal or mode	IW610B	IW610C	IW610F	IW610G
BRF_ANT	BRF_ANT	BRF_ANT	BRF_ANT	BRF_ANT
USB_DP	USB_DP	USB_DP	USB_DP	USB_DP
USB_DM	USB_DM	USB_DM	USB_DM	USB_DM
PTA/WCI-2 coexistence modes	Supported	Supported	Supported	Supported
Wake-up interrupt mode	Wi-Fi and Bluetooth	Wi-Fi and Bluetooth/802.15.4	Wi-Fi and Bluetooth	Wi-Fi and Bluetooth/802.15.4
UART interface mode	Supported	Supported	Supported	Supported
SPI interface mode	—	Supported	—	Supported
JTAG mode	Supported	Supported	Supported	Supported
SDIO interface mode	Supported	Supported	Supported	Supported
USB interface mode	Supported	Supported	Supported	Supported
Oscillator enable mode	Supported	Supported	Supported	Supported

6.2.1 Pin assignment – QFN package

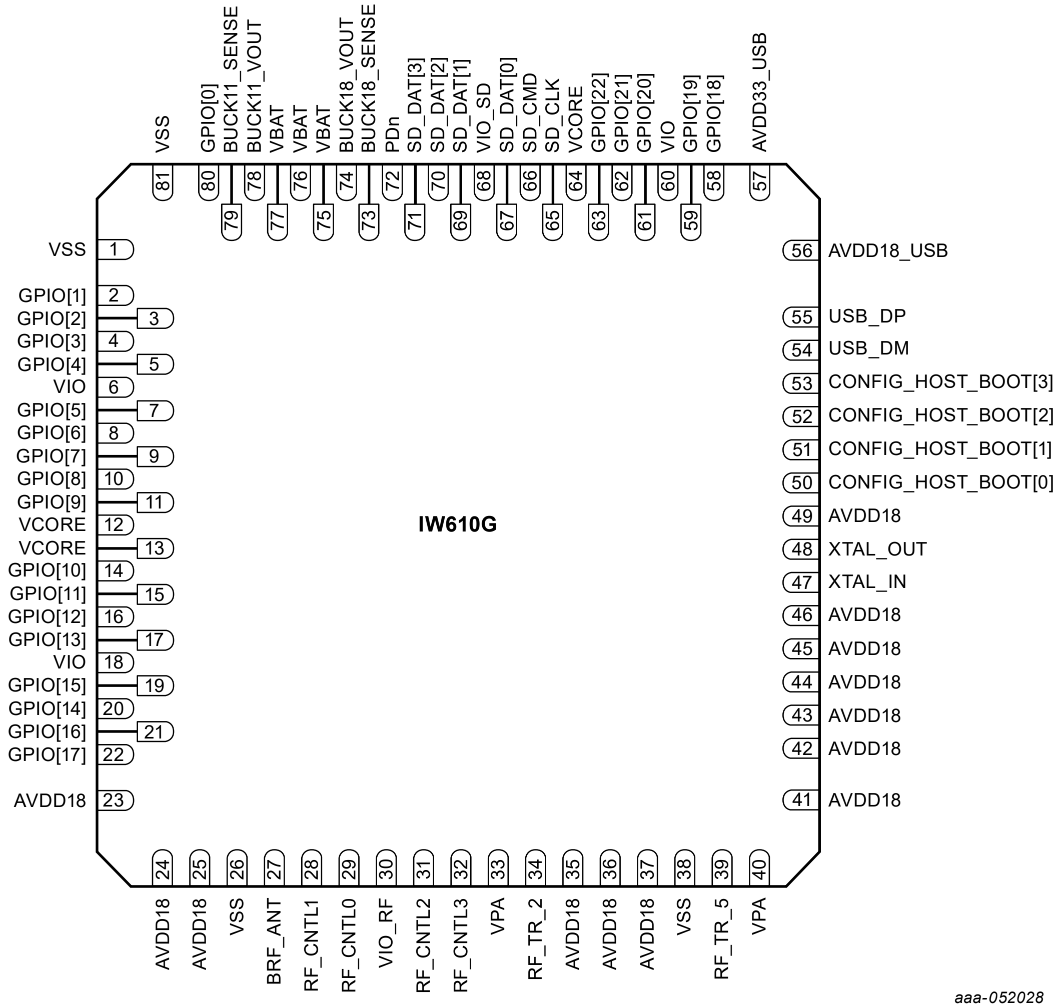

Figure 10. Pin assignment for IW610G - QFN package (top view)

6.2.2 Bump assignment - WLCSP package

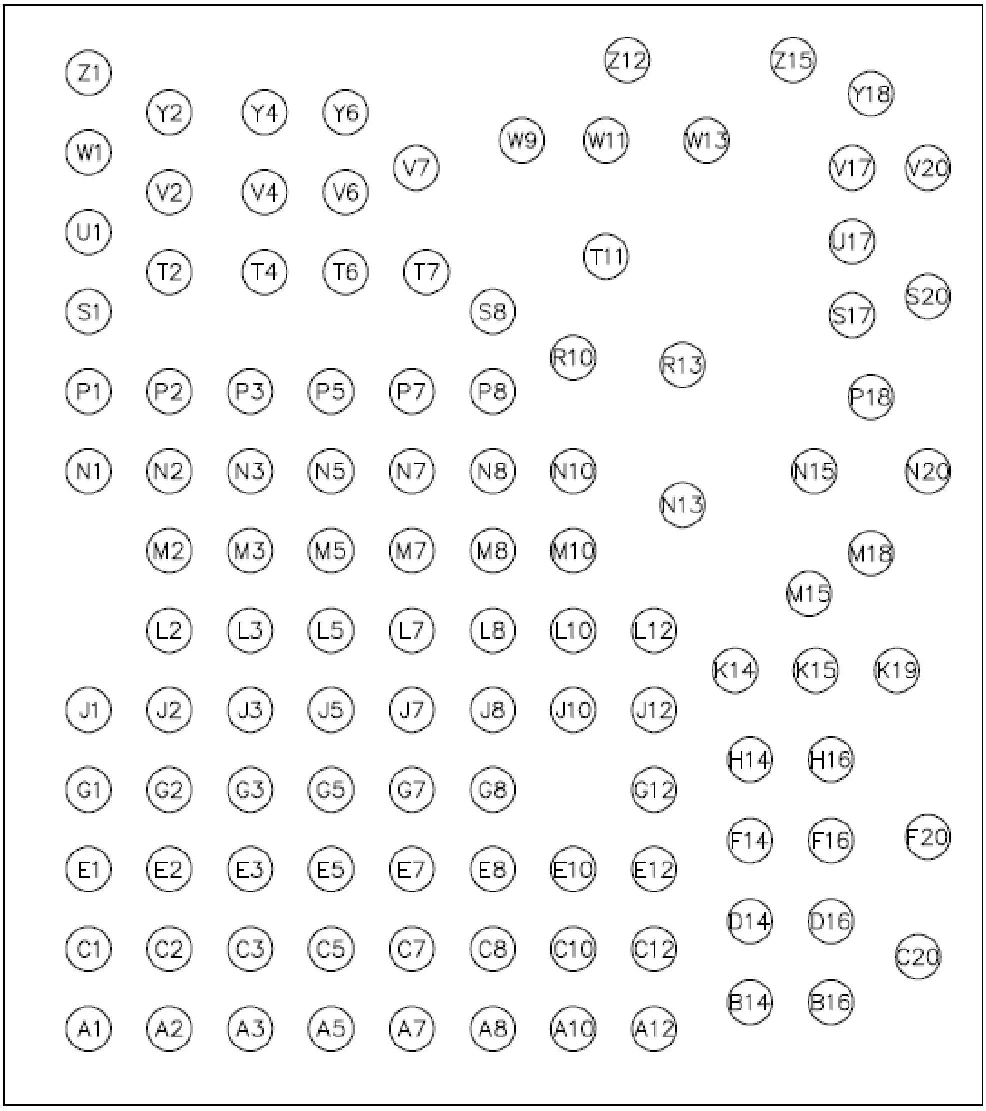

Figure 11. Bump assignment - WLCSP package (bottom view)

6.3 Pin types

Table 8. Pin types

Pin type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A, O	Analog output
A, I/O	Analog input/output
NC	Not connected
Power	Power
Ground	Ground

6.4 Pin states

The pin states information provided in the tables includes:

- **No pad power state** indicates the state when there is no power.
- **PwrDwn state** denotes the power-down state in the default configuration. Many pads have programmable power-down values which can be set by firmware.
- **Reset state**: the state after the power-on-reset state and before the hardware state (HW state).
- **HW state** (hardware state) is the state after the boot code finishes and before the firmware download begins (firmware may change the pin state). The hardware state may differ with the pin muxing or the configuration setting.
- **PwrDwn prog.** indicates whether the power-down state can be programmed or not.
- **Internal PU/PD** indicates:
  - The type of PU/PD (weak or nominal)
  - The polarity (PU or PD)

  The internal pull-up or pull-down applies when the pin is in input mode.
- **PU** denotes whether the pull-up can be programmed or not.
- **PD** denotes whether the pull-down can be programmed or not.
- Pull-up and pull-down are only effective when the pad is in input mode.
- At the end of the firmware download, the pads (for example GPIO and RF control) are programmed in the functional mode corresponding to the functionality of the pins.

6.5 Pin lists

6.5.1 List by number for QFN package

Table 9 shows the pin list for the super-set part IW610G. Refer to Table 7 for the other variants.

Table 9. Pin list by number for IW610G - QFN package

Pin number	Pin name	Power supply	Pin type
1	VSS	—	Ground
2	GPIO[1]	VIO	I/O
3	GPIO[2]	VIO	I/O
4	GPIO[3]	VIO	I/O
5	GPIO[4]	VIO	I/O
6	VIO	—	Power
7	GPIO[5]	VIO	I/O
8	GPIO[6]	VIO	I/O
9	GPIO[7]	VIO	I/O
10	GPIO[8]	VIO	I/O
11	GPIO[9]	VIO	I/O
12	VCORE	—	Power
13	VCORE	—	Power
14	GPIO[10]	VIO	I/O
15	GPIO[11]	VIO	I/O
16	GPIO[12]	VIO	I/O
17	GPIO[13]	VIO	I/O
18	VIO	—	Power
19	GPIO[15]	VIO	I/O
20	GPIO[14]	VIO	I/O
21	GPIO[16]	VIO	I/O
22	GPIO[17]	VIO	I/O
23	AVDD18	—	Power
24	AVDD18	—	Power
25	AVDD18	—	Power
26	VSS	—	Ground
27	BRF_ANT	AVDD18	A, I/O
28	RF_CNTL1	VIO_RF	O
29	RF_CNTL0/CONFIG_XOSC_SEL	VIO_RF	I/O
30	VIO_RF	—	Power
31	RF_CNTL2	VIO_RF	O
32	RF_CNTL3	VIO_RF	O

Table 9. Pin list by number for IW610G - QFN package*...continued*

Pin number	Pin name	Power supply	Pin type
33	VPA	—	Power
34	RF_TR_2	AVDD18	A, I/O
35	AVDD18	—	Power
36	AVDD18	—	Power
37	AVDD18	—	Power
38	VSS	—	Ground
39	RF_TR_5	AVDD18	A, I/O
40	VPA	—	Power
41	AVDD18	—	Power
42	AVDD18	—	Power
43	AVDD18	—	Power
44	AVDD18	—	Power
45	AVDD18	—	Power
46	AVDD18	—	Power
47	XTAL_IN	AVDD18	A, I
48	XTAL_OUT	AVDD18	A, O
49	AVDD18	—	Power
50	CONFIG_HOST_BOOT[0]	AVDD18	I
51	CONFIG_HOST_BOOT[1]	AVDD18	I
52	CONFIG_HOST_BOOT[2]/SD_VOLTAGE_SEL	AVDD18	I/O
53	CONFIG_HOST_BOOT[3]/SPI_INT	AVDD18	I/O
54	USB_DM	AVDD33_USB	A, I/O
55	USB_DP	AVDD33_USB	A, I/O
56	AVDD18_USB	—	Power
57	AVDD33_USB	—	Power
58	GPIO[18]	VIO	I/O
59	GPIO[19]	VIO	I/O
60	VIO	—	Power
61	GPIO[20]	VIO	I/O
62	GPIO[21]	VIO	I/O
63	GPIO[22]	VIO	I/O
64	VCORE	—	Power
65	SD_CLK	VIO_SD	I
66	SD_CMD	VIO_SD	I/O
67	SD_DAT[0]	VIO_SD	I/O
68	VIO_SD	—	Power

Table 9. Pin list by number for IW610G - QFN package*...continued*

Pin number	Pin name	Power supply	Pin type
69	SD_DAT[1]	VIO_SD	I/O
70	SD_DAT[2]	VIO_SD	I/O
71	SD_DAT[3]	VIO_SD	I/O
72	PDn	VBAT	I
73	BUCK18_SENSE	—	Power
74	BUCK18_VOUT	—	Power
75	VBAT	—	Power
76	VBAT	—	Power
77	VBAT	—	Power
78	BUCK11_VOUT	—	Power
79	BUCK11_SENSE	—	Power
80	GPIO[0]	VIO	I/O
81	VSS	—	Ground

6.5.2 Bump list by number for WLCSP package

Table 10 shows the pin list for the super-set part IW610G. Refer to Table 7 for the other variants.

Table 10. Bump list by number for IW610G - WLCSP package

Bump number	Bump name	X (µm)	Y (µm)
A1	BUCK11_VSS	-1653.1	-1932.3
A10	VIO	326.9	-1932.3
A12	AVDD18	656.9	-1932.3
A2	GPIO[3]	-1323.1	-1932.3
A3	VIO	-993.1	-1932.3
A5	VSS	-663.1	-1932.3
A7	GPIO[9]	-333.1	-1932.3
A8	VSS	-3.1	-1932.3
B14	AVDD18	1047.3	-1824.2
B16	AVDD18	1377.3	-1824.2
C1	BUCK11_VX	-1653.1	-1607.3
C10	GPIO[14]	326.9	-1607.3
C12	VSS	656.9	-1607.3
C2	BUCK11_SENSE	-1323.1	-1607.3
C20	VSS	1731.8	-1638.9
C3	GPIO[2]	-993.1	-1607.3
C5	GPIO[6]	-663.1	-1607.3
C7	GPIO[7]	-333.1	-1607.3
C8	GPIO[13]	-3.1	-1607.3
D14	VSS	1047.3	-1494.2
D16	VSS	1377.3	-1494.2
E1	VBAT	-1653.1	-1282.2
E10	GPIO[15]	326.9	-1282.2
E12	GPIO[17]	656.9	-1282.2
E2	VBAT	-1323.1	-1282.2
E3	GPIO[1]	-993.1	-1282.2
E5	GPIO[5]	-663.1	-1282.2
E7	GPIO[8]	-333.1	-1282.2
E8	GPIO[11]	-3.1	-1282.2
F14	VSS	1047.3	-1164.2
F16	AVDD18	1377.3	-1164.2
F20	BRF_ANT	1772	-1150.1
G1	BUCK18_VX	-1653.1	-957.2
G12	GPIO[16]	656.9	-957.2

Table 10. Bump list by number for IW610G - WLCSP package*...continued*

Bump number	Bump name	X (µm)	Y (µm)
G2	BUCK18_SENSE	-1323.1	-957.2
G3	GPIO[0]	-993.1	-957.2
G5	GPIO[4]	-663.1	-957.2
G7	VSS	-333.1	-957.2
G8	GPIO[10]	-3.1	-957.2
H14	VSS	1047.3	-834.2
H16	VSS	1377.3	-834.2
J1	BUCK18_VSS	-1653.1	-632.1
J10	VSS	326.9	-632.1
J12	VSS	656.9	-632.1
J2	PDn	-1323.1	-632.1
J3	SD_DAT[3]	-993.1	-632.1
J5	VSS	-663.1	-632.1
J7	VSS	-333.1	-632.1
J8	GPIO[12]	-3.1	-632.1
K14	RF_CNTL0	986.9	-469.6
K15	RF_CNTL1	1316.9	-469.6
K19	VIO_RF	1646.9	-469.6
L10	RF_CNTL3	326.9	-307.1
L12	RF_CNTL2	656.9	-307.1
L2	SD_DAT[1]	-1323.1	-307.1
L3	SD_DAT[2]	-993.1	-307.1
L5	VSS	-663.1	-307.1
L7	VCORE	-333.1	-307.1
L8	VCORE	-3.1	-307.1
M10	VSS	326.9	18
M15	VPA	1288.9	-157.7
M18	VSS	1540.6	6.8
M2	SD_DAT[0]	-1323.1	18
M3	SD_CMD	-993.1	18
M5	VSS	-663.1	18
M7	VCORE	-333.1	18
M8	VCORE	-3.1	18
N1	VIO_SD	-1653.1	343
N10	VSS	326.9	343
N13	VSS	771.1	205.1

Table 10. Bump list by number for IW610G - WLCSP package*...continued*

Bump number	Bump name	X (µm)	Y (µm)
N15	VSS	1309.9	342.1
N2	SD_CLK	-1323.1	343
N20	RF_TR_2	1772	342.1
N3	GPIO[21]	-993.1	343
N5	GPIO[22]	-663.1	343
N7	VCORE	-333.1	343
N8	VCORE	-3.1	343
P1	VSS	-1653.1	668.1
P18	AVDD18	1540.6	644.3
P2	GPIO[19]	-1323.1	668.1
P3	GPIO[20]	-993.1	668.1
P5	CONFIG_HOST[3]	-663.1	668.1
P7	VSS	-333.1	668.1
P8	CONFIG_HOST[2]	-3.1	668.1
R10	VSS	325.1	806.2
R13	VSS	771.1	776.4
S1	GPIO[18]	-1653.1	993.1
S17	VSS	1464	978.3
S20	AVDD18	1772	1056
S8	CONFIG_HOST[1]	-3.1	993.1
T11	VSS	458.8	1219.1
T2	USB_DP	-1323.1	1155.6
T4	AVDD18	-932.7	1155.6
T6	VSS	-602.7	1155.6
T7	CONFIG_HOST[0]	-272.8	1155.6
U1	VIO	-1653.1	1318.2
U17	VSS	1464	1279.4
V17	VSS	1464	1579.7
V2	USB_DM	-1323.1	1480.7
V20	RF_TR_5	1772	1579.7
V4	XTAL_OUT	-932.7	1480.7
V6	VSS	-602.7	1480.7
V7	VSS	-315.1	1579.7
W1	AVDD18_USB	-1653.1	1643.2
W11	VSS	458.8	1693.1
W13	VSS	870.3	1693.1

Table 10. Bump list by number for IW610G - WLCSP package*...continued*

Bump number	Bump name	X (µm)	Y (µm)
W9	AVDD18	115.9	1693.1
Y18	VPA	1540.6	1882
Y2	VSS	-1323.1	1805.7
Y4	XTAL_IN	-932.7	1805.7
Y6	AVDD18	-602.7	1805.7
Z1	AVDD33_USB	-1653.1	1968.3
Z12	AVDD18	545	2019.5
Z15	AVDD18	1222.4	2019.5

6.6 Pin description

6.6.1 General purpose I/O (GPIO)

Table 11 shows the pin list for the super-set part IW610G. Refer to Table 7 for the modes supported by the other variants.

Table 11. GPIO[1] (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin name	Supply	No Pad Power State	Reset state	HW state	PwrDwn state	PwrDwn Prog	Internal PU/ PD	PU	PD
GPIO[22]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[22] (input/output) **PTA coexistence mode**: EXT_STATE - External radio state signal (input). See Section 6.6.10 "PTA coexistence interface". **WCI-2 coexistence mode**: WCI-2_SIN (input). See Section 6.6.9 "WCI-2 coexistence interface".									
GPIO[21]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[21] (input/output) **PTA coexistence mode**: EXT_PRI - External radio priority signal (input). See Section 6.6.10 "PTA coexistence interface".									
GPIO[20]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[20] (input/output) **PTA coexistence mode**: EXT_GNT- External radio grant signal (output). See Section 6.6.10 "PTA coexistence interface" .									
GPIO[19]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[19] (input/output) **PTA coexistence mode**: EXT_REQ - External radio request signal (input). See Section 6.6.10 "PTA coexistence interface".									
GPIO[18]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[18] (input/output) **PTA coexistence mode**: EXT_FREQ - External radio frequency signal (input). See Section 6.6.10 "PTA coexistence interface" . **WCI-2 coexistence mode**: WCI-2_SOUT (output). See Section 6.6.9 "WCI-2 coexistence interface".									
GPIO[17]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[17] (input/output) **Wake-up/interrupt mode**: NB_WAKE_IN - Out-of-band host-to-device wake-up signal (input) for Bluetooth LE/802.15.4 radios. See Section 6.6.16 "Wake-up/interrupt interface".									
GPIO[16]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[16] (input/output) **Wake-up/interrupt mode**: WL_WAKE_IN - Out-of-band host-to-device wake-up signal for Wi-Fi radio (input). See Section 6.6.16 "Wake-up/interrupt interface".									
GPIO[15]	VIO	tristate	input	input/ output high[2]	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[15] (input/output) **UART interface mode**: UART_SOUT - UART serial output signal. See Section 6.6.7 "UART host interfaces".									

Table 11. GPIO[1] (MFP) *...continued*

Pins may be Multi-Functional Pins (MFP).

Pin name	Supply	No Pad Power State	Reset state	HW state	PwrDwn state	PwrDwn Prog	Internal PU/ PD	PU	PD
GPIO[14]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[14] (input/output) **UART interface mode**: UART_SIN - UART serial input signal. See Section 6.6.7 "UART host interfaces".									
GPIO[13]	VIO	tristate	input	input/ output high[2]	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[13] (input/output) **UART interface mode**: UART_RTSn output. See Section 6.6.7 "UART host interfaces".									
GPIO[12]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[12] (input/output) **UART interface mode**: UART_CTSn (input). See Section 6.6.7 "UART host interfaces".									
GPIO[11]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[11] (input/output) **Software reset mode**: IND_RST_NB - independent software reset for Bluetooth Low Energy (LE) / 802.15.4 radio (input). See Section 6.6.17 "Software reset".									
GPIO[10]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[10] (input/output) **Software reset mode**: IND_RST_WL - independent software reset for Wi-Fi radio (input). See Section 6.6.17 "Software reset".									
GPIO[9]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[9] (input/output) **SPI host interface mode**: SPI_CLK - SPI clock signal (input) . See Section 6.6.8 "SPI host interface".									
GPIO[8]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[8] (input/output) **SPI host interface mode**: SPI_FRM - SPI data frame signal (input). See Section 6.6.8 "SPI host interface". **Bluetooth LE host trigger mode**: BLE_HOST_TRIG0 - Host trigger pin 0 for Bluetooth LE (input/output)									
GPIO[7]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[7] (input/output) **SPI host interface mode**: SPI_RXD - SPI receive signal (input). See Section 6.6.8 "SPI host interface". **Bluetooth LE audio mode**: PCM_SYNC - PCM frame sync signal (input). Refer to Section 6.6.12 "Bluetooth LE audio interface". **Bluetooth LE host trigger mode**: BLE_HOST_TRIG2 - Host trigger pin 2 for Bluetooth LE (input/output)									
GPIO[6]	VIO	tristate	input	input/ output low[3]	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[6] (input/output) **SPI host interface mode**: SPI_TXD - SPI transmit signal (output). See Section 6.6.8 "SPI host interface". **Bluetooth LE host trigger mode**: BLE_HOST_TRIG1 - Host trigger pin 1 for Bluetooth LE (input/output)									

Table 11. GPIO[1] (MFP) *...continued*

Pins may be Multi-Functional Pins (MFP).

Pin name	Supply	No Pad Power State	Reset state	HW state	PwrDwn state	PwrDwn Prog	Internal PU/ PD	PU	PD
GPIO[5]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[5] (input/output) **JTAG mode:** JTAG_TDO - JTAG test data (output) (default mode). See Section 6.6.18 "JTAG interface". **Wake-up/interrupt mode**: NB_WAKE_OUT - Out-of-band device-to-host wake-up signal (output) for Bluetooth LE/802.15.4 radios. See Section 6.6.16 "Wake-up/interrupt interface".									
GPIO[4]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[4] (input/output) **JTAG mode:** JTAG_TDI - JTAG test data (input). See Section 6.6.18 "JTAG interface". **Wake-up/interrupt mode**: WL_WAKE_OUT - Out-of-band device-to-host wake-up signal (output) for the Wi-Fi radio. See Section 6.6.16 "Wake-up/interrupt interface".									
GPIO[3]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[3] (input/output) **JTAG mode**: JTAG_TMS - JTAG test mode select (input) (default mode) . See Section 6.6.18 "JTAG interface".									
GPIO[2]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[2] (input/output) **JTAG mode**: JTAG_TCK - JTAG test clock (input). See Section 6.6.18 "JTAG interface".									
GPIO[1]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[1] (input/output) **USB mode**: USB voltage indicator (input) . See Section 6.6.6 "USB host interface". **SDIO mode**: SD_INT - SDIO interrupt signal (output) . See Section 6.6.16 "Wake-up/interrupt interface".									
GPIO[0]	VIO	tristate	output high	output high	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[0] (input/output) **Oscillator enable mode**: XOSC_EN - Oscillator Enable (output) (active high). See Section 6.6.11 "Clock control interface".									

[1] Not all GPIO pins can be used for Host-to-SoC wake-up signals.
[2] Output high for UART interface
[3] Output high for SPI interface

6.6.2 Wi-Fi RF front-end interface

Note: *This interface is used to control RF front-end components such as switches or FEMs.*

Table 12. Wi-Fi RF front-end control interface

Pin name	Supply	No pad power state	Reset state	HW state	PwrDwn state	PwrDwn prog	Internal PU/PD	PU	PD
RF_CNTL0	VIO_RF	tristate	input	input	drive low	yes	weak PU	yes	yes
RF control mode: RF control 0 - RF control line 0 (output) CONFIG_XOSC_SEL: Reference clock frequency selection (input) - see Section 6.7 "Configuration pins".									
RF_CNTL1	VIO_RF	tristate	input	input	drive high	yes	weak PU	yes	yes
RF control mode: : RF control 1 - RF control line 1 (output)									
RF_CNTL2	VIO_RF	tristate	input	input	drive low	yes	weak PU	yes	yes
RF control mode: RF control 2 - RF control line 2 (output)									
RF_CNTL3	VIO_RF	tristate	input	input	drive high	yes	weak PU	yes	yes
RF control mode: RF Control 3 - RF control line 3 (output)									

6.6.3 Wi-Fi radio interface

Table 13. Wi-Fi radio interface

Pin Name	Type	Supply	Description
RF_TR_2	A, I/O	AVDD18	Wi-Fi Transmit/Receive (2.4 GHz)
RF_TR_5	A, I/O	AVDD18	Wi-Fi Transmit/Receive (5 GHz)

6.6.4 Bluetooth LE/802.15.4 radio interface

Table 14. Bluetooth LE/802.15.4 radio interface

Pin Name	Type	Supply	Description
BRF_ANT	A, I/O	AVDD18	Bluetooth LE/802.15.4 Transmit/Receive

6.6.5 SDIO interface

Table 15. SDIO host interface

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Supply	No Pad Power State	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
SD_CLK	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Clock input									
SD_CMD	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Command/response (input/output)									
SD_DAT[3]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Data line Bit[3]									
SD_DAT[2]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Data line Bit[2] or read wait (optional)									
SD_DAT[1]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Data line Bit[1]									
SD_DAT[0]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Data line Bit[0]									

6.6.6 USB host interface

Table 16. USB host interface

Pin name	Type	Supply	Description
USB_DP	I/O	AVDD33_USB	USB 2.0 Serial Differential Data Plus
USB_DM	I/O	AVDD33_USB	USB 2.0 Serial Differential Data Minus
USB_VBUS_ON	I	VIO	USB voltage indicator. Muxed with GPIO[1]. See Section 6.6.1 "General purpose I/O (GPIO)".

6.6.7 UART host interfaces

Table 17. UART host interface (MFP)
Pins may be Multi-Functional Pins (MFP).

Pin name	Type	Supply	Description
UART_SIN	I	VIO	UART serial input signal - Muxed with GPIO[14].
UART_SOUT	O	VIO	UART serial output signal - Muxed with GPIO[15].
UART_RTSn	O	VIO	UART request-to-send output signal - Active low - Muxed with GPIO[13].
UART_CTSn	I	VIO	UART clear-to-send input signal - Active low - Muxed with GPIO[12].

6.6.8 SPI host interface

Table 18. SPI host interface (MFP)
Pins may be Multi-Functional Pins (MFP).

Pin name	Type	Supply	Description
SPI_FRM	I	VIO	SPI data frame signal, driven by the SPI controller. The signal is active low and also known as SPI chip select. Muxed with GPIO[8]
SPI_CLK	I	VIO	SPI clock input signal. Muxed with GPIO[9]
SPI_RXD	I	VIO	SPI receive input signal. Muxed with GPIO[7]
SPI_TXD	O	VIO	SPI transmit output signal. Muxed with GPIO[6]

6.6.9 WCI-2 coexistence interface

Table 19. WCI-2 coexistence interface
Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Type	Supply	Description
WCI-2_SOUT	O	VIO	WCI-2 output signal - muxed with GPIO[18]. See Section 6.6.1 "General purpose I/O (GPIO)".
WCI-2_SIN	I	VIO	WCI-2 input signal - muxed with GPIO[22]. See Section 6.6.1 "General purpose I/O (GPIO)".

6.6.10 PTA coexistence interface

Table 20. PTA coexistence interface (MFP)
Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Type	Supply	Description
EXT_STATE	I	VIO	External radio state input signal (optional) - muxed with GPIO[22]. See Section 6.6.1 "General purpose I/O (GPIO)". External radio traffic direction (Tx/Rx): • 1: Tx • 0: rx
EXT_GNT	O	VIO	External radio grant output signal (mandatory) - muxed with GPIO[20]
EXT_FREQ	I	VIO	External radio frequency input signal (optional) - muxed with GPIO[18]. See Section 6.6.1 "General purpose I/O (GPIO)". Frequency overlap between external radio and Wi-Fi: • 1: overlap • 0: non-overlap This signal is useful when the external radio is a frequency hopping device.
EXT_PRI	I	VIO	External radio input priority signal (optional) - muxed with GPIO[21] Priority of the request from the external radio. Can support 1 bit priority (sample once) and 2 bit priority (sample twice). Can also have Tx/Rx info following the priority info if EXT_STATE is not used.
EXT_REQ	I	VIO	Request from the external radio (mandatory) - muxed with GPIO[19]

6.6.11 Clock control interface

Table 21. Clock interface

Pin Name	Supply	No Pad Power State	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
XTAL_IN	AVDD18	—	—	—	—	—	—	—	—
Reference clock input The reference clock signal frequency from an external crystal or external crystal oscillator must be 40 MHz or 38.4 MHz. To achieve lower power consumption in sleep mode, it is recommended to use an external crystal instead of an external crystal oscillator. See Section 11.9 "Reference clock specifications".									
XTAL_OUT	AVDD18	—	—	—	—	—	—	—	—
Connect this pin to an external crystal when an external crystal is used. When an external crystal oscillator is used, connect this pin to ground with resistance less than 100 Ω.									
XOSC_EN	VIO	—	—	—	—	—	—	—	—
Oscillator enable (output) (active high) XOSC_EN signal can be used ONLY when an external sleep clock is used. Used to enable an external oscillator. 0 = disable external oscillator 1 = enable external oscillator ***Note:*** *Muxed with GPIO[0].*									

6.6.12 Bluetooth LE audio interface

Table 22. Bluetooth LE audio interface pins

Pins may be Multi-Functional Pins (MFP).

Pin name	Type	Supply	Description
PCM_SYNC	I	VIO	PCM frame sync pulse signal (input). Muxed with GPIO[7]. See Section 6.6.1 "General purpose I/O (GPIO)".

6.6.13 Host configuration

Table 23. Host configuration

Pin name	Supply	No pad power state	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/PD	PU	PD
CONFIG_HOST_BOOT[0]	AVDD18	tristate	input	output high	tristate	no	weak PU	yes	yes
CONFIG_HOST_BOOT[0]: see Section 6.7 "Configuration pins".									
CONFIG_HOST_BOOT[1]	AVDD18	tristate	input	output low	tristate	no	weak PU	yes	yes
CONFIG_HOST_BOOT[1]: see Section 6.7 "Configuration pins".									
CONFIG_HOST_BOOT[2]/ SD_VOLTAGE_SEL	AVDD18	tristate	input	input/output high/output low[1]	tristate	no	weak PD	yes	yes
CONFIG_HOST_BOOT[2]: see Section 6.7 "Configuration pins". **SDIO interface mode**: SD_VOLTAGE_SEL: SDIO voltage select signal (output).									
CONFIG_HOST_BOOT[3]/ SPI_INT	AVDD18	tristate	input	output high/ output low[2]	tristate	no	weak PU	yes	yes
CONFIG_HOST_BOOT[3]: see Section 6.7 "Configuration pins". **Wake-up/interrupt mode** - SPI_INT - SPI interrupt output signal. See Section 6.6.16 "Wake-up/interrupt interface".									

[1] Input low/high for SDIO interface
[2] Output high for SPI interface

6.6.14 Power down pin

Table 24. Power down pin

Pin name	Supply	No pad power state	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/ PD	PU	PD
PDn	VBAT	—	—	—	—	—	weak PD	—	—
Full Power-down (input) (active low) 0 = full power-down mode 1 = normal mode • PDn can accept an input of 1.75 V to 3.63 V • PDn may be driven by the host • PDn must be high for normal operation No internal pull-up on this pin. This pin has an always-on internal weak pull-down.									

6.6.15 Power supply and ground pins

Note: *See Section 9 "Recommended operating conditions" for ratings.*

Table 25. Power and ground pins

Pin Name	Type	Description
VCORE	Power	Nominal 1.05V core power supply
VIO	Power	1.8V/3.3V digital I/O power supply
VIO_SD	Power	1.8V/3.3V digital I/O SDIO power supply
VIO_RF	Power	1.8V/3.3V analog I/O RF power supply
AVDD33_USB	Power	3.3V analog USB power supply
AVDD18	Power	1.8V analog power supply
AVDD18_USB	Power	1.8V analog USB power supply
VPA	Power	3.3V analog power supply
VBAT	Power	Input power supply to internal buck regulators
BUCK_VOUT	Power	Internal buck voltage output See Internal buck connections in Section 7.1 "Internal buck regulators ".
BUCK_SENSE	Power	Internal buck voltage sense This pin senses the output voltage of the internal Buck. See internal buck connections in Section 7.1 "Internal buck regulators ".
VSS	Ground	Ground
NC	NC	No Connect
DNC	DNC	Do Not Connect Do not connect these pins. Leave them floating.

6.6.16 Wake-up/interrupt interface

Table 26. Wake-up/interrupt pins (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin name	Type	Supply	Description
NB_WAKE_OUT	O	VIO	Bluetooth LE/802.15.4 radio wake-up output signal. Muxed with GPIO[5].
NB_WAKE_IN	I	VIO	Bluetooth LE/802.15.4 radio wake-up input signal. Muxed with GPIO[17].
WL_WAKE_OUT	O	VIO	Wi-Fi radio wake-up output signal. Muxed with GPIO[4].
WL_WAKE_IN	I	VIO	Wi-Fi radio wake-up input signal. Muxed with GPIO[16].
SPI_INT	O	VIO	SPI interrupt output signal. Muxed with CONFIG_HOST_BOOT[3]. See Section 6.6.13 "Host configuration".
SD_INT	O	VIO	SDIO interrupt output signal. Muxed with GPIO[1].

6.6.17 Software reset

Table 27. Software reset pins (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin Name	Type	Supply	Description
IND_RST_NB	I	VIO	Independent software reset for Bluetooth LE/802.15.4 radio. Muxed with GPIO[11]
IND_RST_WL	I	VIO	Independent software reset for Wi-Fi. Muxed with GPIO[10]

6.6.18 JTAG interface

Table 28. JTAG interface pins (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin Name	Type	Supply	Description
JTAG_TDO	O	VIO	JTAG test data output signal. Muxed with GPIO[5].
JTAG_TDI	I	VIO	JTAG test data input signal. Muxed with GPIO[4].
JTAG_TMS	I	VIO	JTAG test mode select input signal. Muxed with GPIO[3].
JTAG_TCK	I	VIO	JTAG test clock input signal. Muxed with GPIO[2].

6.7 Configuration pins

Table 29 shows the pins used as configuration inputs to set parameters following a reset. The definition of these pins changes immediately after reset to their usual function. To set a configuration bit to 0, attach a resistor value of 51 kΩ from the pin to ground. No external circuitry is required to set a configuration bit to 1, except on CON[2].

Table 29. Configuration pins

Configura bits	Pin name	Configuration function
CON[5]	RF_CNTL0/ CONFIG_XOSC_SEL	Reference clock frequency selection 0 = 38.4 MHz 1 = 40 MHz (default)
CON[3]	CONFIG_HOST_BOOT[3]	Reserved. Set to 1.
CON[2:0]	CONFIG_HOST_BOOT[2:0]	Host configuration options. Selects the host interface used for Wi-Fi, Bluetooth LE and 802.15.4 radio. 011 = (default). See the tables below.

Table 30. Host configuration options (IW610G and IW610C variants)

CONFIG_MODE[2:0]	Wi-Fi	Bluetooth LE	802.15.4
011 (default)	SDIO	UART	SPI
101	USB	USB	SPI
Others	Reserved	Reserved	Reserved

Table 31. Host configuration options (IW610F and IW610B variants)

CONFIG_MODE[2:0]	Wi-Fi	Bluetooth LE
011 (default)	SDIO	UART
101	USB	USB
Others	Reserved	Reserved

7 Power information

7.1 Internal buck regulators

VCORE and AVDD18 pins must be supplied by the internal Buck regulators. Figure 12 shows the application circuit for VCORE and AVDD18 supply using the internal Buck regulators. The power inductor in the application is chosen to maximize the internal Buck efficiency. Wireless SoC is IW610 in the figure.

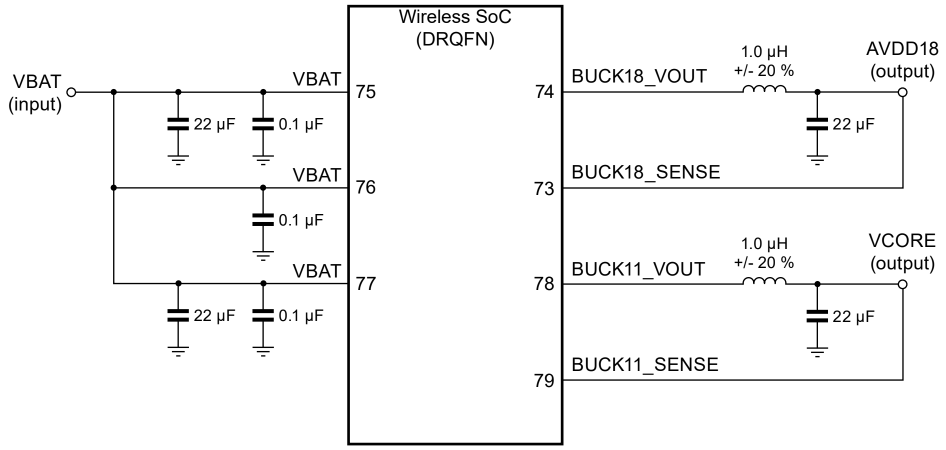

Figure 12. Internal buck regulators - DRQFN package

7.2 Power-up sequence

The IW610 does not have power-up sequence requirements other than VBAT and VPA to be powered up no later than the other external supply rails. The power-down pin (PDn) must be held low (asserted) until all external clock and power supply rails are stable. See Figure 13.

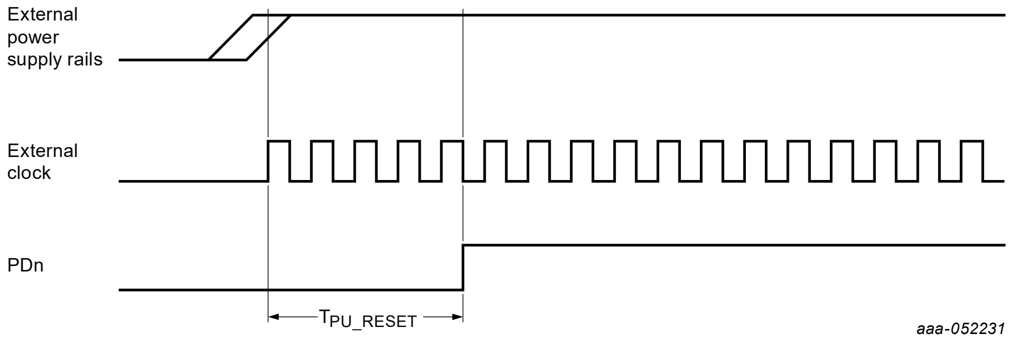

Figure 13. PDn held low (asserted) [1]

[1] T_{PU_RESET} is defined in Section 11.10.1.

All information provided in this document is subject to legal disclaimers.

8 Absolute maximum ratings

CAUTION: The absolute maximum ratings table defines the limitations for electrical and thermal stresses. These limits prevent permanent damage to the device. Exposure to conditions at or beyond these ratings is not guaranteed and can damage the device.

Table 32. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
VCORE[1]	Nominal 1.05 V Vcore power supply	—	1.155	V
VIO	1.8 V/3.3 V digital I/O power supply	—	2.16	V
		—	3.96	V
VIO_RF	1.8 V/3.3 V digital I/O power supply	—	2.16	V
		—	3.96	V
VIO_SD	1.8 V/3.3 V digital I/O power supply	—	2.16	V
		—	3.96	V
AVDD18	1.8 V analog power supply	—	2.16	V
AVDD18_USB	1.8 V analog power supply	—	2.16	V
AVDD33_USB	3.3 V analog power supply	—	3.96	V
VPA	3.3 V analog power supply	—	3.96	V
VBAT	Input power supply to internal buck regulators	—	3.96	V
$T_{STORAGE}$	Storage temperature	-55	+125	°C

[1] VCORE must be powered from the internal buck as illustrated in Section 7.1 "Internal buck regulators "

Table 33. Limiting values

Symbol	Parameter	Condition	Min	Max	Unit
V_{ESD}	Electrostatic discharge	human body model (HBM)[1]	-2	+2	kV
		charged device model (CDM)[2]	-500	+500	V

[1] According to ANSI/ESDA/JEDEC JS-001.
[2] According to ANSI/ESDA/JEDEC JS-002

9 Recommended operating conditions

Note: *Operation beyond the recommended operating conditions is neither recommended nor guaranteed.*

Table 34. Recommended operating conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCORE [1]	Nominal 1.05 V Vcore power supply[2]	—	1.02	—	1.155	V
VIO	1.8 V digital I/O power supply	—	1.71	1.8	1.89	V
	3.3 V digital I/O power supply	—	3.14	3.3	3.46	V
VIO_RF	1.8 V digital I/O power supply	—	1.71	1.8	1.89	V
	3.3 V digital I/O power supply	—	3.14	3.3	3.46	V
VIO_SD	1.8 V digital I/O power supply	—	1.71	1.8	1.89	V
	3.3 V digital I/O power supply	—	3.14	3.3	3.46	V
AVDD18	1.8 V analog power supply	—	1.71	1.8	1.89	V
	1.8 V analog supply ripple	Peak-to-peak	—	—	10	mV
AVDD33_USB	3.3 V analog power supply	—	3.14	3.3	3.46	V
VBAT	Input power supply to internal buck regulators	—	2.25	3.3	3.63	V
VPA	3.3 V analog power supply	—	3.14	3.3	3.46	V
T_A	Ambient operating temperature	Industrial	-40	—	85	°C
T_J	Maximum junction temperature	--	—	--	125	°C

[1] VCORE must be powered by the internal Buck as illustrated in Section 7.1 "Internal buck regulators ".
[2] Operating voltage set by firmware

10 Radio specifications

10.1 Wi-Fi radio specifications

10.1.1 Wi-Fi performance measurement

The Wi-Fi transmit/receive performance is measured either at the antenna port or at the chip port. In Figure 14, the Wireless SoC is IW610.

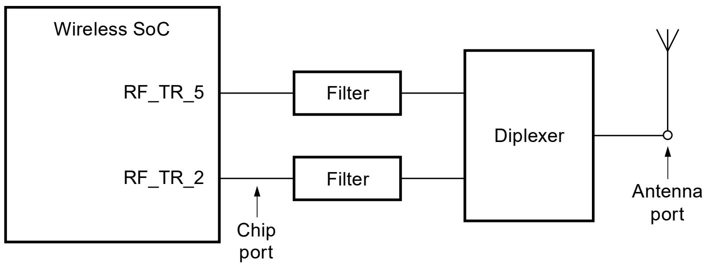

Figure 14. RF performance measurement points

10.1.2 2.4 GHz Wi-Fi receiver performance

Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_2 pin.

Table 35. 2.4 GHz Wi-Fi receiver performance

The performance values are preliminary information subject to change based on the final device characterization results

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	—	2400	—	2483.5	MHz
RF signal bandwidth	—	20	—	20	MHz
S11	—	—	-10	—	dB
Image rejection	After calibration	—	—	-48	dBc
Receiver sensitivity					
Receiver sensitivity 802.11b	20 MHz 1 Mbps	—	-99.1	—	dBm
Receiver sensitivity 802.11b	20 MHz 11 Mbps	—	-91	—	dBm
Receiver sensitivity 802.11g	20 MHz 6 Mbps	—	-94.7	—	dBm
Receiver sensitivity 802.11g	20 MHz 54 Mbps	—	-77	—	dBm
Receiver sensitivity 802.11n	20 MHz MCS0 Nss1 BCC	—	-93.2	—	dBm
Receiver sensitivity 802.11n	20 MHz MCS7 Nss1 BCC	—	-74.2	—	dBm
Receiver sensitivity 802.11ac	20 MHz MCS0 Nss1 BCC	—	-93.1	—	dBm
Receiver sensitivity 802.11ac	20 MHz MCS8 Nss1 BCC	—	-70.5	—	dBm
Receiver sensitivity 802.11ax	4x3.2 20 MHz MCS0 Nss1 BCC	—	-93	—	dBm
Receiver sensitivity 802.11ax	4x3.2 20 MHz MCS9 Nss1 BCC	—	-68.4	—	dBm
Receiver maximum input level (MIL)					
Receiver maximum input level DSSS	802.11b DSSS MIL	—	-0.2	—	dBm
Receiver maximum input level CCK	802.11b CCK MIL	—	2	—	dBm
Receiver maximum input level OFDM	OFDM MIL	—	-2	—	dBm
Receiver adjacent channel interference (ACI)					
Receiver ACI 802.11b	20 MHz 1 Mbps	—	53	—	dB
Receiver ACI 802.11b	20 MHz 11 Mbps	—	48	—	dB
Receiver ACI 802.11g	20 MHz 6 Mbps	—	31	—	dB
Receiver ACI 802.11g	20 MHz 54 Mbps	—	26	—	dB
Receiver ACI 802.11n	20 MHz MCS0 Nss1 BCC	—	31	—	dB
Receiver ACI 802.11n	20 MHz MCS7 Nss1 BCC	—	26	—	dB
Receiver ACI 802.11ac	20 MHz MCS0 Nss1 BCC	—	39	—	dB
Receiver ACI 802.11ac	20 MHz MCS8 Nss1 BCC	—	23	—	dB
Receiver ACI 802.11ax	4x3.2 20 MHz MCS0 Nss1 BCC	—	30	—	dB
Receiver ACI 802.11ax	4x3.2 20 MHz MCS9 Nss1 BCC	—	9	—	dB

Table 35. 2.4 GHz Wi-Fi receiver performance*...continued*

The performance values are preliminary information subject to change based on the final device characterization results

Parameter	Condition	Min	Typ	Max	Unit
Receiver alternate adjacent channel interference (AACI)					
Receiver AACI 802.11b	20 MHz 1 Mbps	—	53	—	dB
Receiver AACI 802.11b	20 MHz 11 Mbps	—	49	—	dB
Receiver AACI 802.11g	20 MHz 6 Mbps	—	50	—	dB
Receiver AACI 802.11g	20 MHz 54 Mbps	—	34	—	dB
Receiver AACI 802.11n	20 MHz MCS0 Nss1 BCC	—	50	—	dB
Receiver AACI 802.11n	20 MHz MCS7 Nss1 BCC	—	32	—	dB
Receiver AACI 802.11ac	20 MHz MCS0 Nss1 BCC	—	51	—	dB
Receiver AACI 802.11ac	20 MHz MCS8 Nss1 BCC	—	28	—	dB
Receiver AACI 802.11ax	4x3.2 20 MHz MCS0 Nss1 BCC	—	49	—	dB
Receiver AACI 802.11ax	4x3.2 20 MHz MCS9 Nss1 BCC	—	24	—	dB

10.1.3 5 GHz Wi-Fi receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_5 pin.*

Table 36. 5 GHz Wi-Fi receiver performance

The performance values are preliminary information subject to change based on the final device characterization results.

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	—	4900	—	5895	MHz
RF signal bandwidth	—	20	—	20	MHz
S11	—	—	-10	—	dB
Receiver sensitivity					
Receiver sensitivity 802.11a	20 MHz 6 Mbps	—	-93.8	—	dBm
Receiver sensitivity 802.11a	20 MHz 54 Mbps	—	-76.1	—	dBm
Receiver sensitivity 802.11n	20 MHz MCS0 Nss1 BCC	—	-92.4	—	dBm
Receiver sensitivity 802.11n	20 MHz MCS7 Nss1 BCC	—	-73.5	—	dBm
Receiver sensitivity 802.11ac	20 MHz MCS0 Nss1 BCC	—	-92.4	—	dBm
Receiver sensitivity 802.11ac	20 MHz MCS8 Nss1 BCC	—	-69.7	—	dBm
Receiver sensitivity 802.11ax	4x3.2 20 MHz MCS0 Nss1 BCC	—	-92.3	—	dBm
Receiver sensitivity 802.11ax	4x3.2 20 MHz MCS9 Nss1 BCC	—	-67.4	—	dBm
Receiver adjacent channel interference (ACI)					
Receiver ACI 802.11a	20 MHz 6 Mbps	—	24	—	dB
Receiver ACI 802.11a	20 MHz 54 Mbps	—	16	—	dB
Receiver ACI 802.11n	20 MHz MCS0 Nss1 BCC	—	24	—	dB
Receiver ACI 802.11n	20 MHz MCS7 Nss1 BCC	—	11	—	dB
Receiver ACI 802.11ac	20 MHz MCS0 Nss1 BCC	—	28	—	dB
Receiver ACI 802.11ac	20 MHz MCS8 Nss1 BCC	—	8	—	dB
Receiver ACI 802.11ax	4x3.2 20 MHz MCS0 Nss1 BCC	—	30	—	dB
Receiver ACI 802.11ax	4x3.2 20 MHz MCS9 Nss1 BCC	—	9	—	dB
Receiver alternate adjacent channel interference (AACI)					
Receiver AACI 802.11a	20 MHz 6 Mbps	—	48	—	dB
Receiver AACI 802.11a	20 MHz 54 Mbps	—	28	—	dB
Receiver AACI 802.11n	20 MHz MCS0 Nss1 BCC	—	46	—	dB
Receiver AACI 802.11n	20 MHz MCS7 Nss1 BCC	—	28	—	dB
Receiver AACI 802.11ac	20 MHz MCS0 Nss1 BCC	—	47	—	dB
Receiver AACI 802.11ac	20 MHz MCS8 Nss1 BCC	—	25	—	dB
Receiver AACI 802.11ax	4x3.2 20 MHz MCS0 Nss1 BCC	—	49	—	dB
Receiver AACI 802.11ax	4x3.2 20 MHz MCS9 Nss1 BCC	—	24	—	dB

10.1.4 2.4 GHz Wi-Fi transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_2 pin.*

Table 37. 2.4 GHz Wi-Fi transmitter performance

The performance values are preliminary information subject to change based on the final device characterization results.

Parameter	Condition	Min	Typ	Max	Units
RF frequency range	2.4 GHz	2400	—	2483.5	MHz
Maximum linear output power with 20 MHz bandwidth	802.11b 1 Mbps	—	22	—	dBm
	802.11b 11 Mbps	—	22	—	dBm
	802.11g 6 Mbps	—	22	—	dBm
	802.11g 54 Mbps	—	19	—	dBm
	802.11n MCS7	—	19	—	dBm
	802.11ax MCS9	—	18	—	dBm
Transmit I/Q suppression with IQ calibration	802.11b 1 Mbps	—	—	-55	dBc
Second harmonic (HD2)	At 21 dBm, CW	—	-45	—	dBr
Third harmonic (HD3)	At 21 dBm, CW	—	-35	—	dBr
Transmit power accuracy	With manufacturing-time calibration per board	-2	—	2	dB
Transmit power control resolution	—	—	0.5	—	dB
Out-of-band noise floor at different operation standard frequency range Transmit 1 Mbps at 18 dBm with 100% duty cycle	—	—	-137	—	dBm/Hz
Transmit carrier suppression	802.11b 1 Mbps	—	-31	—	dBc
Transmit frequency error	—	-7	—	7	PPM
Transmit output power control step	—	—	1	—	dB
Transmit output power level control range	—	-10	—	22	dBm
Transmit general spurs, harmonics and sub-harmonics[1] 1 Mbps Tx at 20 dBm with 100% duty cycle	< 1 GHz	—	-80	—	dBm/100 kHz
	1 GHz to 18 GHz	—	-78	—	dBm/100 kHz
	Second harmonic	—	-54	—	dBm/1 MHz
	Third harmonic	—	-49	—	dBm/1 MHz
	LO leakage	—	-31	—	dBm

[1] Spurious and harmonics are measured with the front-end configuration of the reference design.

10.1.5 5 GHz Wi-Fi transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_5 pin.*

Table 38. 5 GHz Wi-Fi transmitter performance
The performance values are preliminary information subject to change based on the final device characterization results.

Parameter	Condition	Min	Typ	Max	Units
RF frequency range	5 GHz	4900	—	5895	MHz
Maximum linear output power with 20 MHz bandwidth	802.11a 6 Mbps	—	23	—	dBm
	802.11a 54 Mbps	—	20	—	dBm
	802.11n MCS0	—	22	—	dBm
	802.11n MCS7	—	20	—	dBm
	802.11ac MCS0	—	22	—	dBm
	802.11ac MCS8	—	19	—	dBm
	802.11ax MCS0	—	22	—	dBm
	802.11ax MCS9	—	19	—	dBm
Transmit I/Q suppression with IQ calibration	802.11a 6 Mbps	—	—	-48	dBc
Second harmonic (HD2)	At 20 dBm, CW	—	—	-25	dBr
Third harmonic (HD3)	At 20 dBm, CW	—	—	-45	dBr
Transmit power accuracy	With manufacturing-time calibration per board	-2	—	2	dB
Transmit power control resolution	—	—	0.5	—	dB
Out-of-band noise floor at different operation standard frequency range Transmit 1 Mbps at 18 dBm with 100% duty cycle	—	—	-147	—	dBm/Hz
Transmit carrier suppression	802.11a 6 Mbps	—	-34	—	dBc
Transmit frequency error	—	-5	—	5	PPM
Transmit output power control step	—	—	1	—	dB
Transmit output power level control range	—	-10	—	22	dBm
Transmit general spurs, harmonics and sub-harmonics[1] 6 Mbps Tx at 18 dBm with 100% duty cycle	< 1 GHz	—	-85	—	dBm/100 kHz
	1 GHz to 18 GHz	—	-74	—	dBm/100 kHz
	Second harmonic	—	-47	—	dBm/1 MHz
	Third harmonic	—	-50	—	dBm/1 MHz
	LO leakage	—	-34	—	dBm

[1] Spurious and harmonics are measured with the front-end configuration of the reference design.

10.2 Bluetooth LE radio specifications

10.2.1 Bluetooth LE receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF_ANT pin.*

Table 39. Bluetooth LE receiver performance [1]

The performance values are preliminary information subject to change based on the final device characterization results.

Parameter	Conditions	Min	Typ.	Max	Unit
RF frequency range	—	2400	—	2483.5	MHz
S11	—	—	-10	—	dB
Receiver sensitivity					
Bluetooth LE 1 Mbps	—	—	-99.1	—	dBm
Bluetooth LE 2 Mbps	—	—	-97.1	—	dBm
Bluetooth LR 500 Kbps	—	—	-100.7	—	dBm
Bluetooth LR 125 Kbps	—	—	-107.5	—	dBm
Receiver maximum input level (MIL)[2]					
Bluetooth LE 1 Mbps	—	—	-3	—	dBm
Bluetooth LE 2 Mbps	—	—	-3	—	dBm
Bluetooth LR 125 Kbps	—	—	-3	—	dBm
Bluetooth LR 500 Kbps	—	—	-3	—	dBm
Receiver interference/selectivity performance[3]					
Bluetooth LE 1 Mbps					
Receiver selectivity @ -5 MHz (image -1)	Bluetooth LE 1 Mbps selectivity	—	-43	—	dB
Receiver AACS @ -4 MHz (image)	Bluetooth LE 1 Mbps alternate adjacent channel selectivity	—	-32	—	dB
Receiver selectivity @ -3 MHz (image +1)	Bluetooth LE 1 Mbps selectivity	—	-35	—	dB
Receiver ACS @ -2 MHz	Bluetooth LE 1 Mbps adjacent channel selectivity	—	-40	—	dB
Receiver selectivity @ -1 MHz	Bluetooth LE 1 Mbps selectivity	—	-3	—	dB
Receiver CCS	Bluetooth LE 1 Mbps co-channel selectivity	—	9	—	dB
Receiver selectivity @ +1 MHz	Bluetooth LE 1 Mbps selectivity	—	-5	—	dB
Receiver ACS @ +2 MHz	Bluetooth LE 1 Mbps adjacent channel selectivity	—	-43	—	dB
Receiver selectivity @ +3 MHz	Bluetooth LE 1 Mbps selectivity	—	-50	—	dB

Table 39. Bluetooth LE receiver performance [1] *...continued*

The performance values are preliminary information subject to change based on the final device characterization results.

Parameter	Conditions	Min	Typ.	Max	Unit
Bluetooth LE 2 Mbps					
Receiver selectivity @ -6 MHz (image -2)	Bluetooth LE 2 Mbps 3rd adjacent channel selectivity	—	-52	—	dB
Receiver AACS @ -4 MHz (image)	Bluetooth LE 2 Mbps alternate adjacent channel selectivity	—	-30	—	dB
Receiver ACS @ -2 MHz (image +2)	Bluetooth LE 2 Mbps adjacent channel selectivity	—	-20	—	dB
Receiver CCS	Bluetooth LE 2 Mbps co-channel selectivity	—	8	—	dB
Receiver ACS @ +2 MHz	Bluetooth LE 2 Mbps adjacent channel selectivity	—	-26	—	dB
Receiver AACS @ +4 MHz	Bluetooth LE 2 Mbps alternate adjacent channel selectivity	—	-50	—	dB
Receiver selectivity @ +6 MHz	Bluetooth LE 2 Mbps 3rd adjacent channel selectivity	—	-55	—	dB
Bluetooth LR 125 Kbps					
Receiver selectivity @ -5 MHz (image -1)	Bluetooth LR 125 kbps selectivity	—	-46	—	dB
Receiver AACS @ -4 MHz (image)	Bluetooth LR 125 kbps alternate adjacent channel selectivity	—	-35	—	dB
Receiver selectivity @ -3 MHz (image +1)	Bluetooth LR 125 kbps selectivity	—	-39	—	dB
Receiver ACS @ -2 MHz	Bluetooth LR 125 kbps adjacent channel selectivity	—	-50	—	dB
Receiver selectivity @ -1 MHz	Bluetooth LR 125 kbps selectivity	—	-6	—	dB
Receiver CCS	Bluetooth LR 125 kbps co-channel selectivity	—	8	—	dB
Receiver selectivity @ +1 MHz	Bluetooth LR 125 kbps selectivity	—	-10	—	dB
Receiver ACS @ +2 MHz	Bluetooth LR 125 kbps adjacent channel selectivity	—	-50	—	dB
Receiver selectivity @ +3 MHz	Bluetooth LR 125 kbps selectivity	—	-56	—	dB

Table 39. Bluetooth LE receiver performance [1] *...continued*

The performance values are preliminary information subject to change based on the final device characterization results.

Parameter	Conditions	Min	Typ.	Max	Unit
Bluetooth LR 500 Kbps					
Receiver selectivity @ -5 MHz (image -1)	Bluetooth LR 500 kbps selectivity	—	-49	—	dB
Receiver AACS @ -4 MHz (image)	Bluetooth LR 500 kbps alternate adjacent channel selectivity	—	-40	—	dB
Receiver selectivity @ -3 MHz (image +1)	Bluetooth LR 500 kbps selectivity	—	-40	—	dB
Receiver ACS @ -2 MHz	Bluetooth LR 500 kbps adjacent channel selectivity	—	-50	—	dB
Receiver selectivity @ -1 MHz	Bluetooth LR 500 kbps selectivity	—	-9	—	dB
Receiver CCS	Bluetooth LR 500 kbps co-channel selectivity	—	5	—	dB
Receiver selectivity @ +1 MHz	Bluetooth LR 500 kbps selectivity	—	-10	—	dB
Receiver ACS @ +2 MHz	Bluetooth LR 500 kbps adjacent channel selectivity	—	-55	—	dB
Receiver selectivity @ +3 MHz	Bluetooth LR 500 kbps selectivity	—	-60	—	dB

[1] Bluetooth/Bluetooth LE receiver refers to Dirty Tx. That is, the transmitter has impairments as specified by the Bluetooth SIG standard. The Packet length is 255 bytes.
[2] The true MIL numbers are higher than -3 dBm. The measurements are limited by the setup capability.
[3] The selectivity numbers show C/I ratio (in dB).

10.2.2 Bluetooth LE transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF_ANT pin.*

Table 40. Bluetooth LE transmitter performance

The performance values are preliminary information subject to change based on the final device characterization results.

Parameter	Conditions	Min	Typ.	Max	Unit
RF frequency range	—	2400	—	2483.5	MHz
Bluetooth LE maximum transmit power	—	—	15	—	dBm
Out-of band noise floor at different operation standard frequency range Transmit at 15 dBm with 100% duty cycle	—	—	-137	—	dBm/Hz
Transmit frequency error	Includes XTAL error	—	1.2	—	kHz
Transmit output power accuracy	At maximum power	-2	—	2	dBm
Transmit output power control step	—	—	0.5	—	dB
Transmit output power level control range	—	-20	—	15.2	dBm
Transmit general spurs, harmonics and sub-harmonics[1] Transmit at 15 dBm with 100% duty cycle	< 1 GHz	—	-72	—	dBm/100 kHz
	1 GHz to 18 GHz	—	-69	—	dBm/100 kHz
	Second harmonic	—	-66	—	dBm/1 MHz
	Third harmonic	—	-68	—	dBm/1 MHz
	LO leakage	—	-54	—	dBm

[1] Spurious and harmonics are measured with the front-end configuration of the reference design.

10.3 802.15.4 radio performance

10.3.1 802.15.4 radio receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF_ANT pin.*

Table 41. 802.15.4 radio receiver performance

The performance values are preliminary information subject to change based on the final device characterization results

Parameter	Conditions	Min	Typ.	Max	Unit
RF frequency range	—	2400	—	2483.5	MHz
S11	—	—	-10	—	dB
Receiver sensitivity					
Receiver sensitivity	Nominal conditions	—	-105.7	—	dBm
Receiver maximum input level (MIL)[1]					
Receiver MIL	—	—	7	—	dBm
Receiver adjacent channel selectivity (ACS)/co-channel selectivity (CCS) performance[2]					
Receiver 4th ACS 2.4 GHz -20 MHz	Desired signal 3 dB above sensitivity. Interferer is a PRBS OQPSK modulated signal at the indicated offset	—	66	—	dB
Receiver 3rd ACS 2.4 GHz -15 MHz		—	65	—	dB
Receiver 2nd ACS 2.4 GHz -10 MHz		—	40	—	dB
Receiver 1st ACS 2.4 GHz -5 MHz		—	37	—	dB
Receiver CCS		—	-2	—	dB
Receiver 1st ACS 2.4 GHz +5 MHz		—	41	—	dB
Receiver 2nd ACS 2.4 GHz +10 MHz		—	40	—	dB
Receiver 3rd ACI 2.4 GHz +15 MHz		—	65	—	dB
Receiver 4th ACI 2.4 GHz +20 MHz		—	65	—	dB

[1] The true MIL numbers are higher than 7 dBm. The measurements are limited by the setup capability.
[2] The selectivity numbers indicate the I/C ratio [in dB].

10.3.2 802.15.4 radio transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF_ANT pin.*

Table 42. 802.15.4 radio transmitter performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	—	2400	—	2483.5	MHz
Transmit maximum power	—	—	14.3	—	dBm
Out-of band noise floor at different operation standard frequency range Transmit at 15 dBm with 100% duty cycle	—	—	-139	—	dBm/Hz
Transmit frequency error	—	-10	—	10	kHz
Transmit output power accuracy	—	-2	—	2	dBm
Transmit output power control step	—	—	1	—	dB
Transmit output power level control range	—	-20	—	15	dBm
Transmit general spurs, harmonics and sub-harmonics[1] Transmit at 15 dBm with 100% duty cycle	< 1 GHz	—	-83	—	dBm/100 kHz
	1 GHz to 18 GHz	—	-84	—	dBm/100 kHz
	Second harmonic	—	-66	—	dBm/1 MHz
	Third harmonic	—	-63	—	dBm/1 MHz
	LO leakage	—	-62	—	dBm

[1] Spurious and harmonics are measured with the front-end configuration of the reference design.

10.4 Current consumption

Note: *The power consumption values refer to 3.3 V supply source (85% eff) and 25°C.*

Table 43 shows the current consumption values for SDIO-UART-SPI mode with SDIO 2.0/ 3.0 and 50 MHz clock.

Table 43. SDIO-UART-SPI mode, SDIO 2.0 or SDIO 3.0 50 MHz (clock gating enabled)

Mode	Conditions	Min	Typ	Max	Unit
Power down					
Power down	Wi-Fi and narrowband powered down [1]	—	0.015	—	mA
Sleep					
Sleep	Wi-Fi and narrowband in sleep mode	—	0.31	—	mA
Sleep	Wi-Fi subsystem in sleep mode, RAM retention, narrowband powered down	—	0.23	—	mA
Bluetooth LE only (Wi-Fi in sleep mode)					
Bluetooth LE in sleep mode	RAM retention	—	0.18	—	mA
Bluetooth LE advertising	1.28 interval	—	0.20	—	mA
Bluetooth LE scanning	1.28 interval, 11.25 ms window	—	0.31	—	mA
Bluetooth LE receive	Bluetooth LE RX 1 Mbps	—	21	—	mA
Bluetooth LE transmit	Bluetooth LE TX 0 dBm	—	24	—	mA
	Bluetooth LE TX 4 dBm	—	28	—	mA
	Bluetooth LE TX 15 dBm	—	64	—	mA
802.15.4 only (Wi-Fi in sleep mode)					
802.15.4 receive	—	—	24	—	mA
802.15.4 transmit	802.15.4 TX 0 dBm	—	25	—	mA
	802.15.4 TX 4 dBm	—	30	—	mA
	802.15.4 TX 15 dBm	—	65	—	mA
IEEE Wi-Fi power save mode (Partial RAM retention for Wi-Fi subsystem, narrowband subsystem powered down, beacon interval = 102.4 ms, short beacon frame)[2]					
DTIM 1 (2.4 GHz, 20 MHz)	2.4 GHz basic rate for beacon transmit: 1 Mbps	—	0.88	—	mA
DTIM 3 (2.4 GHz, 20 MHz)		—	0.49	—	mA
DTIM 5 (2.4 GHz, 20 MHz)		—	0.44	—	mA
DTIM 10 (2.4 GHz, 20 MHz)		—	0.36	—	mA
DTIM 1 (5 GHz, 20 MHz)	5 GHz basic rate for beacon transmit: 6 Mbps	—	0.75	—	mA
DTIM 3 (5 GHz, 20 MHz)		—	0.47	—	mA
DTIM 5 (5 GHz, 20 MHz)		—	0.36	—	mA
DTIM 10 (5 GHz, 20 MHz)		—	0.33	—	mA

Table 43. SDIO-UART-SPI mode, SDIO 2.0 or SDIO 3.0 50 MHz (clock gating enabled)*...continued*

Mode	Conditions	Min	Typ	Max	Unit
IEEE 802.11ax target wake-up time (TWT) (Partial RAM retention for Wi-Fi subsystem, narrowband subsystem powered down)[3]					
TWT 1 min	2.4 GHz, 20 MHz	—	0.32	—	mA
TWT 5 min		—	0.31	—	mA
TWT 10 min		—	0.30	—	mA
TWT 30 min		—	0.29	—	mA
TWT 1 min	5 GHz, 20 MHz	—	0.32	—	mA
TWT 5 min		—	0.31	—	mA
TWT 10 min		—	0.30	—	mA
TWT 30 min		—	0.29	—	mA
Wi-Fi mode (narrowband subsystem powered down)					
Wi-Fi in sleep mode	RAM retention	—	0.23	—	mA
Wi-Fi idle mode	2.4 GHz, RX, 802.11n, 20 MHz, listening	—	51	—	mA
	2.4 GHz, RX, 802.11ax, 20 MHz, listening	—	52	—	mA
	5 GHz, RX, 802.11n, 20 MHz, listening	—	61	—	mA
	5 GHz, RX, 802.11ax, 20 MHz, listening	—	61	—	mA
Wi-Fi receive mode	2.4 GHz, 802.11n, 20 MHz, MCS7	—	52	—	mA
	2.4 GHz, 802.11ax, 20 MHz, MCS9	—	58	—	mA
	5 GHz, 802.11n, 20 MHz, MCS7	—	59	—	mA
	5 GHz, 802.11ax, 20 MHz, MCS9	—	59	—	mA
Wi-Fi transmit mode, max power	2.4 GHz, 802.11n, 20 MHz, MCS7 @ 20 dBm	—	255	—	mA
	2.4 GHz, 802.11ax, 20 MHz, MCS9 @ 20 dBm	—	253	—	mA
	5 GHz, 802.11n, 20 MHz, MCS7 @ 20 dBm	—	348	—	mA
	5 GHz, 802.11ax, 20 MHz, MCS9 @ 20 dBm	—	348	—	mA
Wi-Fi transmit mode	2.4 GHz, 802.11n, 20 MHz, MCS0 @ 15 dBm	—	194	—	mA
	5 GHz, 802.11n, 20 MHz, MCS0 @ 15 dBm	—	286	—	mA
Peak current during device initialization					
Peak digital pre-distortion (DPD) current	2.4 GHz digital pre-distortion (DPD) at 85°C	—	289	—	mA
Peak digital pre-distortion (DPD) current	5 GHz digital pre-distortion (DPD) at 85°C	—	474	—	mA
Maximum power consumption	5 GHz, 802.11ax, 20 MHz, MCS9 TX at 20 dBm, at 85°C	—	413	—	mA

[1] Refer to [1].
[2] Frame duration for short beacon IEEE-PS current measurement:
- 2.4 GHz: 1000 µs
- 5 GHz: 300 µs

[3] Nominal TWT receive window duration: 50 ms

Table 44 shows the current consumption values for SDIO-UART-SPI mode with SDIO 3.0 and 200 MHz clock. Refer to Table 43 for the values not shown in this table.

Table 44. SDIO-UART-SPI mode, SDIO 3.0 200 MHz (clock gating enabled)

Mode	Conditions	Min	Typ	Max	Unit
Sleep					
Sleep	Wi-Fi and narrowband in sleep mode	—	0.59	—	mA
Sleep	Wi-Fi subsystem in sleep mode, RAM retention, narrowband powered down	—	0.51	—	mA
IEEE Wi-Fi power save mode (Partial RAM retention for Wi-Fi subsystem, narrowband subsystem powered down, beacon interval = 102.4 ms, short beacon frame) [1]					
DTIM 1 (2.4 GHz, 20 MHz)	2.4 GHz basic rate for beacon transmit: 1 Mbps	—	1.18	—	mA
DTIM 3 (2.4 GHz, 20 MHz)		—	0.80	—	mA
DTIM 5 (2.4 GHz, 20 MHz)		—	0.75	—	mA
DTIM 10 (2.4 GHz, 20 MHz)		—	0.67	—	mA
DTIM 1 (5 GHz, 20 MHz)	5 GHz basic rate for beacon transmit: 6 Mbps	—	1.05	—	mA
DTIM 3 (5 GHz, 20 MHz)		—	0.75	—	mA
DTIM 5 (5 GHz, 20 MHz)		—	0.69	—	mA
DTIM 10 (5 GHz, 20 MHz)		—	0.64	—	mA
IEEE 802.11ax target wake-up time (TWT) (Partial RAM retention for Wi-Fi subsystem, narrowband subsystem powered down[2]					
TWT 1 min	2.4 GHz, 20 MHz	—	0.62	—	mA
TWT 5 min		—	0.61	—	mA
TWT 10 min		—	0.60	—	mA
TWT 30 min		—	0.59	—	mA
TWT 1 min	5 GHz, 20 MHz	—	0.62	—	mA
TWT 5 min		—	0.61	—	mA
TWT 10 min		—	0.60	—	mA
TWT 30 min		—	0.59	—	mA

[1] Frame duration for short beacon IEEE-PS current measurement:
- 2.4 GHz: 1000 µs
- 5 GHz: 300 µs

[2] Nominal TWT receive window duration: 50 ms

In USB suspend mode, there is a current consumption of 200 µA, based on USB 2.0 specification.

Table 45. USB-USB-SPI mode, USB 2.0

Mode	Conditions	Min	Typ	Max	Unit
Power down					
Power down	Wi-Fi and narrowband powered down[1]	—	0.015	—	mA
Sleep					
Sleep	Wi-Fi and narrowband in sleep mode	—	0.38	—	mA
Bluetooth LE only (Wi-Fi in sleep mode)					
Bluetooth LE in sleep mode	RAM retention	—	0.38	—	mA
Bluetooth LE advertising	1.28 interval	—	0.45	—	mA
Bluetooth LE scanning	1.28 interval, 11.25 ms window	—	0.58	—	mA
Bluetooth LE receive	Bluetooth LE RX 1 Mbps	—	32	—	mA
Bluetooth LE transmit	Bluetooth LE TX 0 dBm	—	35	—	mA
	Bluetooth LE TX 4 dBm	—	39	—	mA
	Bluetooth LE TX 15 dBm	—	78	—	mA
802.15.4 only (Wi-Fi in sleep mode)					
802.15.4 receive	—	—	38	—	mA
802.15.4 transmit	802.15.4 TX 0 dBm	—	38	—	mA
	802.15.4 TX 4 dBm	—	45	—	mA
	802.15.4 TX 15 dBm	—	82	—	mA
IEEE Wi-Fi power save mode (Partial RAM retention for Wi-Fi subsystem, narrowband subsystem powered down, beacon interval = 102.4 ms, short beacon frame)[2]					
DTIM 1 (2.4 GHz, 20 MHz)	2.4 GHz basic rate for beacon transmit: 1 Mbps	—	0.93	—	mA
DTIM 3 (2.4 GHz, 20 MHz)		—	0.58	—	mA
DTIM 5 (2.4 GHz, 20 MHz)		—	0.50	—	mA
DTIM 10 (2.4 GHz, 20 MHz)		—	0.42	—	mA
DTIM 1 (5 GHz, 20 MHz)	5 GHz basic rate for beacon transmit: 6 Mbps	—	0.77	—	mA
DTIM 3 (5 GHz, 20 MHz)		—	0.55	—	mA
DTIM 5 (5 GHz, 20 MHz)		—	0.45	—	mA
DTIM 10 (5 GHz, 20 MHz)		—	0.40	—	mA

Table 45. USB-USB-SPI mode, USB 2.0 *...continued*

Mode	Conditions	Min	Typ	Max	Unit
IEEE 802.11ax target wake-up time (TWT) (Partial RAM retention for Wi-Fi subsystem, narrowband subsystem powered down)[3]					
TWT 1 min	2.4 GHz, 20 MHz	—	0.51	—	mA
TWT 5 min		—	0.46	—	mA
TWT 10 min		—	0.45	—	mA
TWT 30 min		—	0.43	—	mA
TWT 1 min	5 GHz, 20 MHz	—	0.49	—	mA
TWT 5 min		—	0.45	—	mA
TWT 10 min		—	0.44	—	mA
TWT 30 min		—	0.42	—	mA
Wi-Fi mode (narrowband subsystem in sleep mode)					
Wi-Fi in sleep mode	RAM retention	—	0.38	—	mA
Wi-Fi idle mode	2.4 GHz, RX, 802.11n, 20 MHz, listening	—	64	—	mA
	2.4 GHz, RX, 802.11ax, 20 MHz, listening	—	64	—	mA
	5 GHz, RX, 802.11n, 20 MHz, listening	—	79	—	mA
	5 GHz, RX, 802.11ax, 20 MHz, listening	—	79	—	mA
Wi-Fi receive mode	2.4 GHz, 802.11n, 20 MHz, MCS7	—	62	—	mA
	2.4 GHz, 802.11ax, 20 MHz, MCS9	—	63	—	mA
	5 GHz, 802.11n, 20 MHz, MCS7	—	71	—	mA
	5 GHz, 802.11ax, 20 MHz, MCS9	—	70	—	mA
Wi-Fi transmit mode, max power	2.4 GHz, 802.11n, 20 MHz, MCS7 @ 20 dBm	—	273	—	mA
	2.4 GHz, 802.11ax, 20 MHz, MCS9 @ 20 dBm	—	264	—	mA
	5 GHz, 802.11n, 20 MHz, MCS7 @ 20 dBm	—	404	—	mA
	5 GHz, 802.11ax, 20 MHz, MCS9 @ 20 dBm	—	361	—	mA
Wi-Fi transmit mode	2.4 GHz, 802.11n, 20 MHz, MCS0 @ 15 dBm	—	207	—	mA
	5 GHz, 802.11n, 20 MHz, MCS0 @ 15 dBm	—	302	—	mA
Peak current during device initialization					
Peak digital pre-distortion (DPD) current	2.4 GHz digital pre-distortion (DPD) at 85°C	—	308	—	mA
Peak digital pre-distortion (DPD) current	5 GHz digital pre-distortion (DPD) at 85°C	—	469	—	mA
Maximum power consumption	5 GHz, 802.11ax, 20 MHz, MCS9 TX at 20 dBm, at 85°C	—	451	—	mA

[1] Refer to [1].
[2] Frame duration for short beacon IEEE-PS current measurement:
- 2.4 GHz: 1000 µs
- 5 GHz: 300 µs

[3] Nominal TWT receive window duration: 50 ms

11 Electrical specifications

11.1 General purpose I/O specifications

11.1.1 DC characteristics

11.1.1.1 VIO 1.8V operation

Table 46. DC electricals—1.8V operation (VIO)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions".

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIO	I/O pad supply voltage	—	1.71	1.8	1.89	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO	V
V_{IH}	Input high voltage	—	0.7*VIO	—	VIO+0.4	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.1.1.2 VIO 3.3V operation

Table 47. DC electricals—3.3V operation (VIO)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIO	I/O pad supply voltage	—	3.14	3.3	3.46	V
V_{IH}	Input high voltage	—	0.7*VIO	—	VIO+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.2 RF front-end specifications

11.2.1 DC characteristics

11.2.1.1 1.8 V operation

Table 48. DC electrical characteristics—1.8V operation (VIO_RF)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	—	0.7*VIO_RF	—	VIO_RF+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO_RF	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO_RF-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.2.1.2 3.3V operation

Table 49. DC electricals—3.3V operation (VIO_RF)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	—	0.7*VIO_RF	—	VIO_RF+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO_RF	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO_RF-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.3 SDIO interface specifications

11.3.1 DC characteristics

11.3.1.1 1.8V operation

Table 50. DC electricals—1.8V operation (VIO_SD)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	—	0.7*VIO_SD	—	VIO_SD+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO_SD-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.3.1.2 3.3V operation

Table 51. DC electricals—3.3V operation (VIO_SD)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	—	0.7*VIO_SD	—	VIO_SD+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO_SD-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.3.2 Default speed, high-speed modes

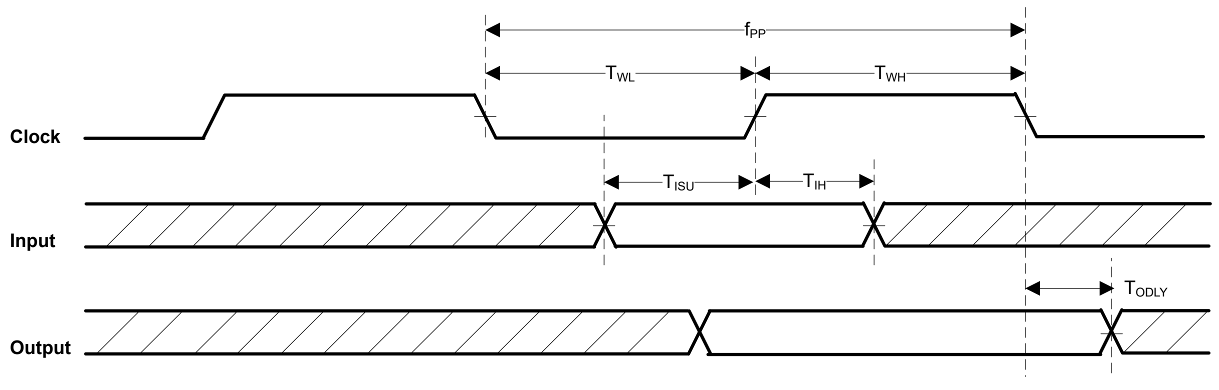

Figure 15. SDIO protocol timing diagram—Default speed mode

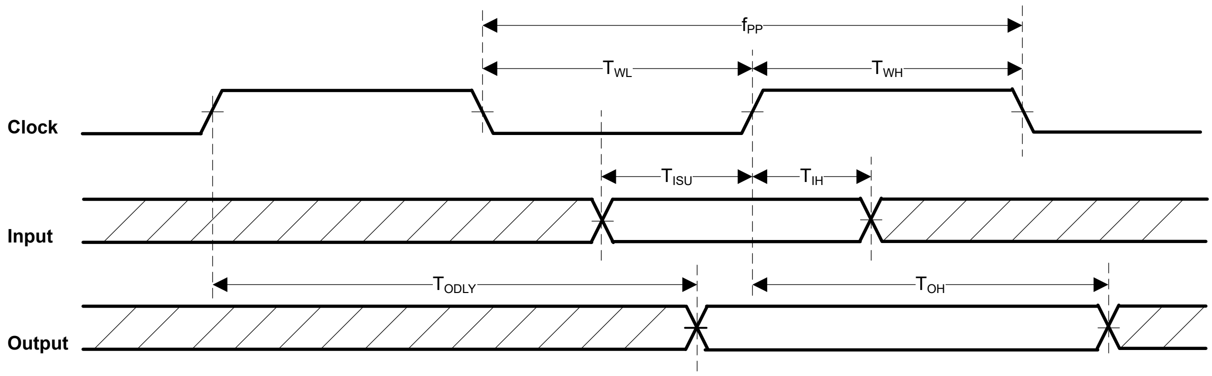

Figure 16. SDIO protocol timing diagram—High-speed mode

Table 52. SDIO timing data—Default speed, high-speed modes (3.3 V)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	Normal	0	—	25	MHz
		High-speed	0	—	50	MHz
T_{WL}	Clock low time	Normal	10	—	—	ns
		High-speed	7	—	—	ns
T_{WH}	Clock high time	Normal	10	—	—	ns
		High-speed	7	—	—	ns
T_{ISU}	Input setup time	Normal	5	—	—	ns
		High-speed	6	—	—	ns
T_{IH}	Input hold time	Normal	5	—	—	ns
		High-speed	2	—	—	ns
T_{ODLY}	Output delay time	Normal	—	—	14	ns
	CL ≤ 40 pF (1 card)	High-speed	—	—	14	ns
T_{OH}	Output hold time	High-speed	2.5	—	—	ns

11.3.3 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

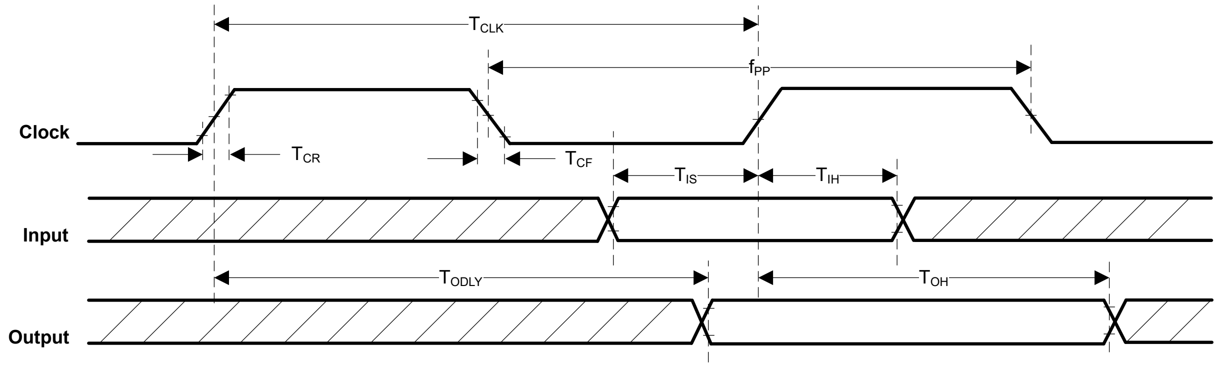

Figure 17. SDIO protocol timing diagram—SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

Table 53. SDIO timing data—SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR12/25/50	25	—	100	MHz
T_{IS}	Input setup time	SDR12/SDR25/SDR50	3	—	—	ns
T_{IH}	Input hold time	SDR12/SDR25/SDR50	0.8	—	—	ns
T_{CLK}	Clock time	SDR12/SDR25/SDR50	10	—	40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/SDR25/SDR50	—	—	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time $C_L \leq 30$ pF	SDR12	—	—	14	ns
	Output delay time $C_L \leq 30$ pF	SDR25	—	—	14	ns
	Output delay time $C_L \leq 30$ pF	SDR50	—	—	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12/SDR25/SDR50	1.5	—	—	ns

11.3.4 SDR104 mode (208 MHz) (1.8V)

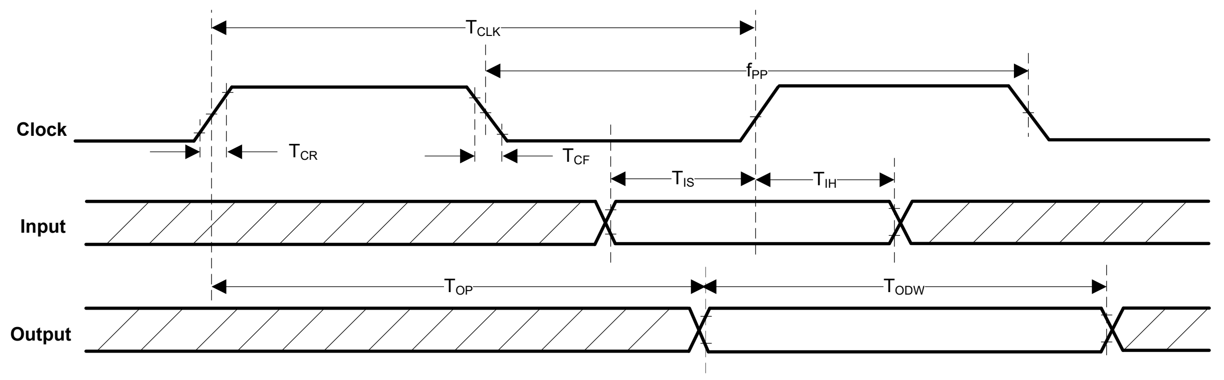

Figure 18. SDIO protocol timing diagram—SDR104 mode (208 MHz)

Table 54. SDIO timing data—SDR104 mode (208 MHz)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR104	0	—	208	MHz
T_{IS}	Input setup time	SDR104	1.4	—	—	ns
T_{IH}	Input hold time	SDR104	0.8	—	—	ns
T_{CLK}	Clock time	SDR104	4.8	—	—	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104	—	—	$0.2*T_{CLK}$	ns
T_{OP}	Card output phase	SDR104	0	—	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	—	—	ns

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11.3.5 DDR50 mode (50 MHz) (1.8V)

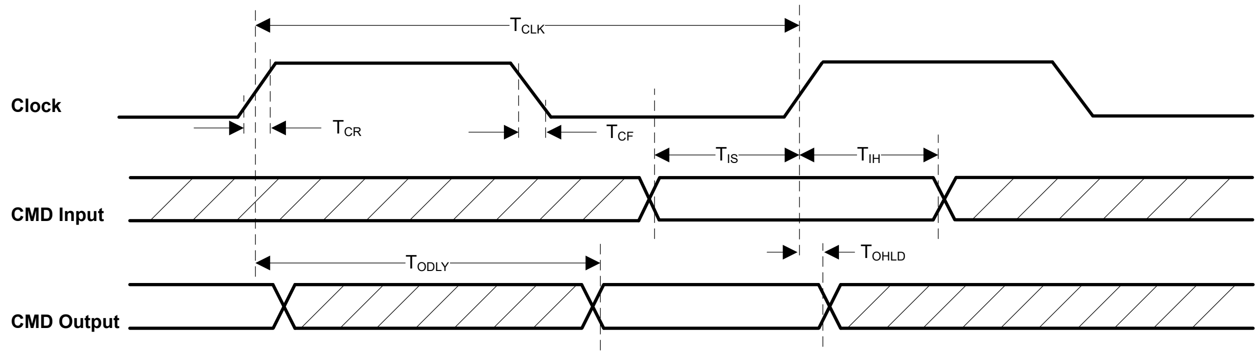
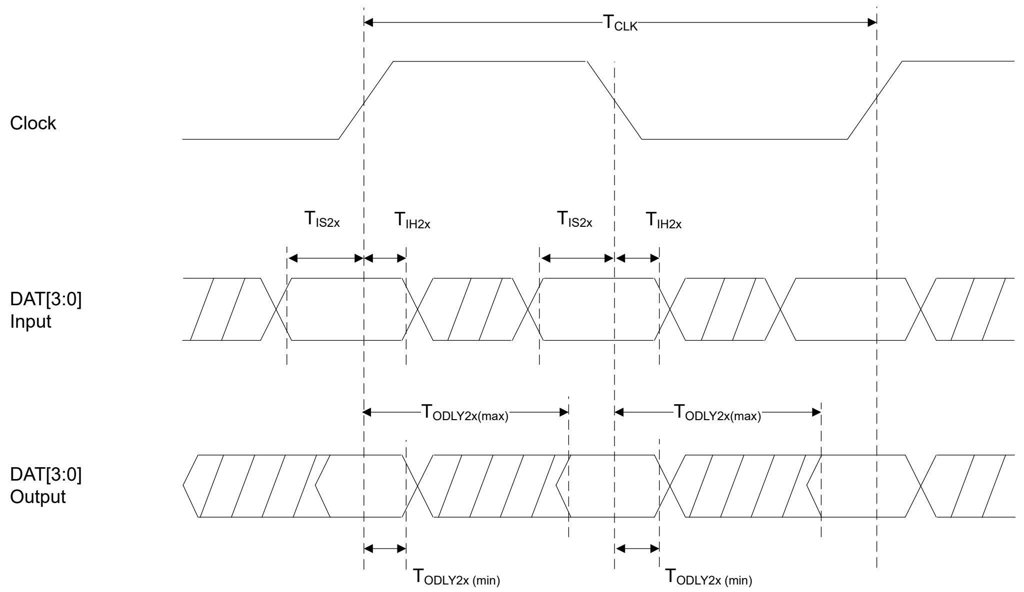


Figure 19. SDIO CMD timing diagram—DDR50 mode (50 MHz)



In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

Figure 20. SDIO DAT[3:0] timing diagram—DDR50 mode (50 MHz)

Table 55. SDIO timing data—DDR50 mode (50 MHz)

Unless otherwise specified, the values apply per *Section 9 "Recommended operating conditions"*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	—	—	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD} = 10 pF	DDR50	—	—	0.2*T_{CLK}	ns
Clock duty	—	DDR50	45	—	55	%
CMD input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	6	—	—	ns
T_{IH}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	—	—	ns
CMD output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode C_L ≤ 30 pF (1 card)	DDR50	—	—	13.7	ns
T_{OHLD}	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	—	—	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	3	—	—	ns
T_{IH2x}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	—	—	ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
$T_{ODLY2x\ (max)}$	Output delay time during data transfer mode C_L ≤ 25 pF (1 card)	DDR50	—	—	7.0	ns
$T_{ODLY2x\ (min)}$	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	—	—	ns

11.3.6 SDIO internal pull-up/pull-down specifications

Table 56. SDIO internal pull-up/pull-down specifications

Unless otherwise specified, the values apply per *Section 9 "Recommended operating conditions"*

Parameter	Condition	Min	Typ	Max	Unit
Internal nominal pull-up/pull-down resistance	--	70	100	140	kΩ

11.4 USB device interface specifications

11.4.1 USB LS driver and receiver parameters

Table 57. USB LS driver and receiver specifications data

Note: *In accordance with Universal Serial Bus 2.0 Specification, Revision 2.0, April 2000.*

Note: *Over full range of values specified in Section 9 "Recommended operating conditions", unless otherwise specified.*

Note: *The load is 100Ω differential for these parameters, unless other specified.*

Note: *Contact NXP representatives for register associated with table values.*

Symbol	Parameter	Min	Typ	Max	Unit
BR	Baud rate	—	1.5	—	Mbit/s
BR_{PPM}	Baud rate tolerance	-15000.0	—	15000.0	ppm
Driver specifications					
V_{OH}	Output single ended high Defined with 1.425 kΩ pull-up resistor to 3.6V.	2.8	—	3.6	V
V_{OL}	Output single ended low Defined with 1.425 kΩ pull-down resistor to ground.	0.0	—	0.3	V
V_{CRS}	Output single crossover voltage See Figure 21 "USB LS/FS data rise and fall time diagram".	1.3	—	2.0	V
T_{LR}	Data fall time • See Figure 21 "USB LS/FS data rise and fall time diagram". • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75.0	—	300.0	ns
T_{LF}	Data rise time • See Figure 21 "USB LS/FS data rise and fall time diagram". • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75.0	—	300.0	ns
T_{LRFM}	Rise and fall time matching	80.0	—	125.0	%
T_{UDJ1}	Source jitter total: to next transition • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-95.0	—	95.0	ns
T_{UDJ2}	Source jitter total: for paired transitions • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-150.0	—	150.00	ns
Receiver specifications					
V_{IH}	Input single ended high	2.0	—	—	V
V_{IL}	Input single ended low	—	—	0.8	V
V_{DI}	Differential input sensitivity	0.2	—	—	V

11.4.2 USB FS driver and receiver parameters

Table 58. USB FS driver and receiver specifications data

Note: *In accordance with Universal Serial Bus 2.0 Specification, Revision 2.0, April 2000.*

Note: *Over full range of values specified in Section 9 "Recommended operating conditions", unless otherwise specified.*

Note: *The load is 100Ω differential for these parameters, unless other specified.*

Note: *Contact NXP representatives for register associated with table values.*

Symbol	Parameter	Min	Typ	Max	Unit
BR	Baud rate	—	12.0	—	Mbit/s
BR_{PPM}	Baud rate tolerance	-2500.0	—	2500.0	ppm
Driver specifications					
V_{OH}	Output single ended high Defined with 1.425 kΩ pull-up resistor to 3.6V.	2.8	—	3.6	V
V_{OL}	Output single ended low Defined with 1.425 kΩ pull-down resistor to ground.	0.0	—	0.3	V
V_{CRS}	Output single crossover voltage See Figure 21 "USB LS/FS data rise and fall time diagram".	1.3	—	2.0	V
T_{FR}	Output rise time • See Figure 21 "USB LS/FS data rise and fall time diagram". • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4.0	—	20.0	ns
T_{FL}	Output fall time • See Figure 21 "USB LS/FS data rise and fall time diagram". • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4.0	—	20.0	ns
T_{DJ1}	Source jitter total: to next transition • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-3.5	—	3.5	ns
T_{DJ2}	Source jitter total: for paired transitions • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-4.0	—	4.0	ns
T_{FDEOP}	Source jitter for differential transition to SE0 transition Defined at crossover point of differential data signals.	-2.0	—	5.0	ns
Receiver specifications					
V_{IH}	Input single ended high	2.0	—	—	V
V_{IL}	Input single ended low	—	—	0.8	V
V_{DI}	Differential input sensitivity	0.2	—	—	V
T_{JR1}	Receiver jitter: to next transition Defined at crossover point of differential data signals.	-18.5	—	18.5	ns
T_{JR2}	Receiver jitter: for paired transitions Defined at crossover point of differential data signals.	-9.0	—	9.0	ns

11.4.3 USB HS driver and receiver parameters

Table 59. USB HS driver and receiver specifications data

Note: *In accordance with Universal Serial Bus 2.0 Specification, Revision 2.0, April 2000.*

Note: *Over full range of values specified in Section 9 "Recommended operating conditions", unless otherwise specified.*

Note: *The load is 100Ω differential for these parameters, unless other specified.*

Note: *Contact NXP representatives for register associated with table values.*

Symbol	Parameter	Min	Typ	Max	Unit
BR	Baud rate	—	480.0	—	Mbit/s
BR_{PPM}	Baud rate tolerance	-500.0	—	500.0	ppm
Driver specifications					
V_{HSOH}	Data signaling high	360.0	—	440.0	mV
V_{HSOL}	Data signaling low	-10.0	—	10.0	mV
T_{HSR}	Data rise time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	500.0	—	—	ns
T_{HSF}	Data fall time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-500.0	—	—	ns
—	Source jitter See Figure 22 "USB HS Tx eye diagram pattern template diagram".	—	—	—	—
Receiver specifications					
—	Differential input signaling levels See Figure 22 "USB HS Tx eye diagram pattern template diagram".	—	—	—	—
V_{HSCM}	Input single ended low	-50	—	500.00	mV
—	Receiver jitter tolerance. See Figure 22 "USB HS Tx eye diagram pattern template diagram".	—	—	—	—

11.4.4 USB interface driver waveforms

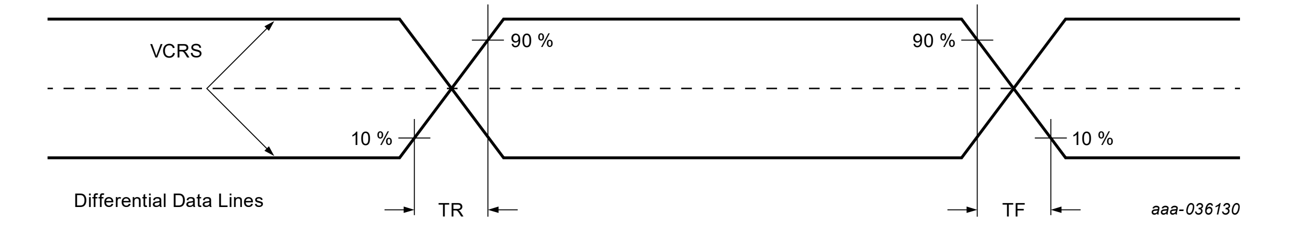


Figure 21. USB LS/FS data rise and fall time diagram

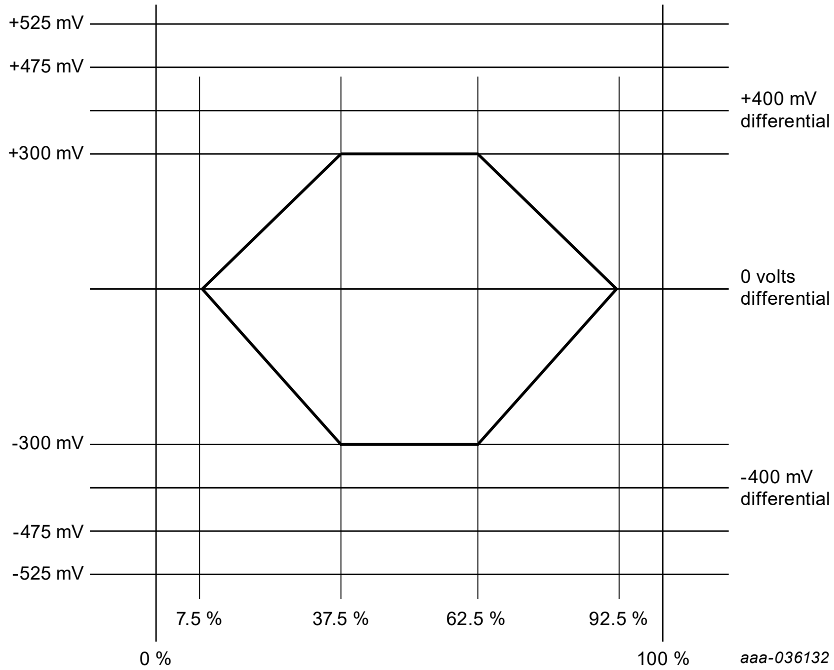


Figure 22. USB HS Tx eye diagram pattern template diagram

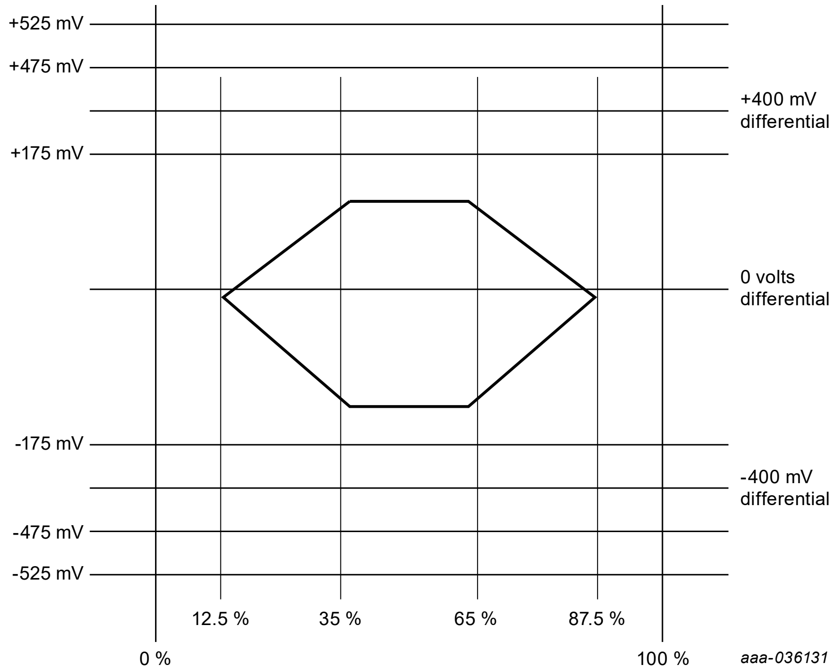


Figure 23. USB HS Rx eye diagram pattern template diagram

11.5 UART interface specifications

The UART TX and RX pins are powered from the VIO voltage supply.

See Section 11.1.1 "DC characteristics" for DC specifications.

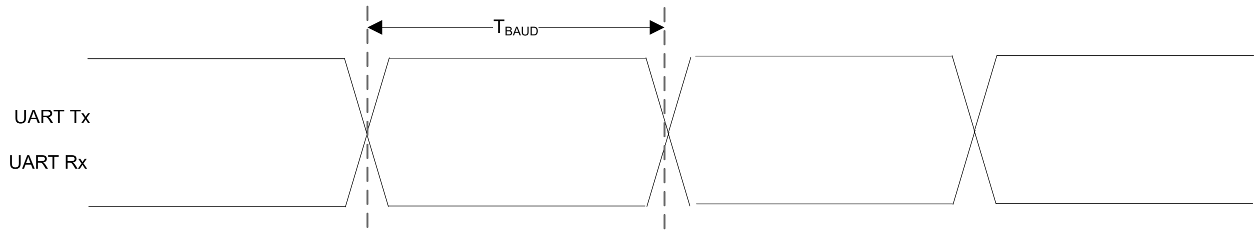


Figure 24. UART timing diagram

Table 60. UART timing data[1] [2]

Over full range of values specified in Section 9 "Recommended operating conditions" unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{BAUD}	Baud time	40 MHz (38.4 MHz) input clock	250	—	—	ns

[1] The acceptable deviation from the UART Rx target baud rate is ±3%.
[2] UART TX baud rate deviation is determined by the external crystal accuracy. See Section 11.9.2.

11.6 SPI host interface specifications

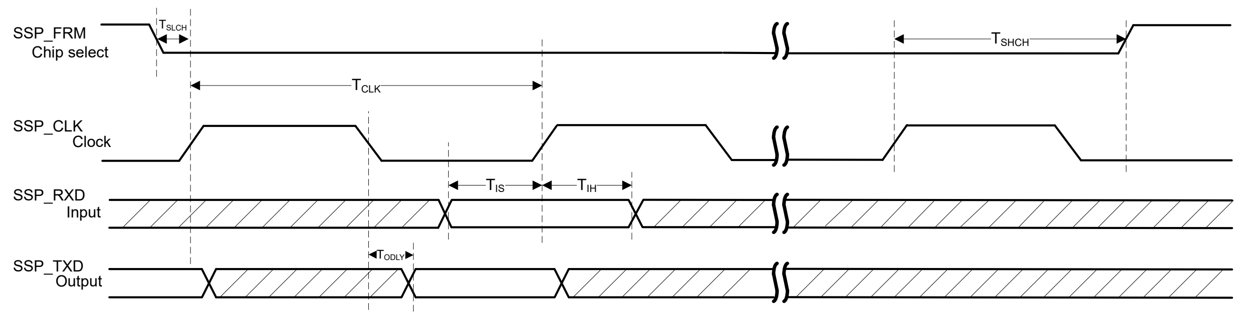


Figure 25. SPI host interface timing diagram

Table 61. SPI host interface timing data

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{SLCH}	Chip select setup time	—	12	—	—	ns
T_{SHCH}	Chip select hold time	—	12	—	—	ns
T_{CLK}	Clock period	—	100	—	—	ns
T_{IS}	Input setup time	—	12	—	—	ns
T_{IH}	Input hold time	—	0	—	—	ns
T_{ODLY}	Output delay	—	—	—	12	ns

11.7 External coexistence interface specifications

11.7.1 WCI-2 coexistence interface specifications

11.7.1.1 WCI-2 interface

WCI-2 is a simplified 2-wire UART interface defined in Bluetooth Core Spec Vol 7 Part C.

Figure 26 shows UART waveform.

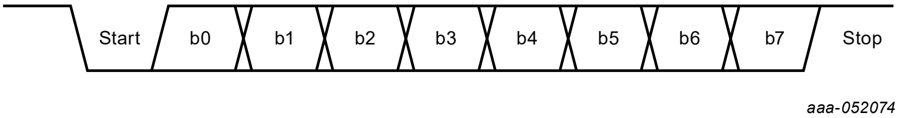


Figure 26. UART waveform

Figure 27 illustrates WCI-2 hardware coexistence interface between the wireless SoC (IW610) and the external radio.

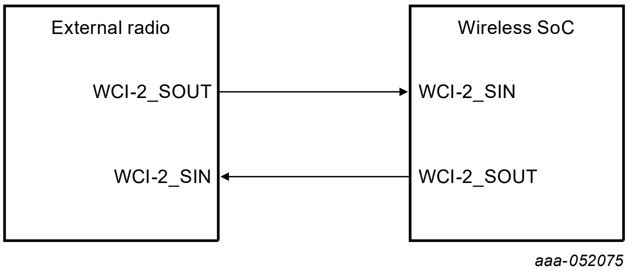


Figure 27. WCI-2 coexistence interface

11.7.1.2 WCI-2 messages

WCI-2 coexistence interface supports the messages defined in Bluetooth Core Specification Vol 7 Part C for request and grant, where:

- The real time message from the external radio to IW610 indicates the request to operate (Figure 28)
  - MWS_Rx=1 indicates an external radio request to Rx
  - MWS_Tx=1 indicates an external radio request to Tx

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	0	FRAME_SYNC	MWS_RX	MWS_TX	MWS_PATTERN[0]	MWS_PATTERN[1]

aaa-052076

Figure 28. Type 0: Real time signaling message - external radio to IW610

- The external radio can send an optional second message following the real time message to indicate the traffic priority using the vendor specific message (Figure 29). Otherwise, the priority is set via a BCA register.

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
1	1	1	0	MWS_TX_PRI[0]	MWS_TX_PRI[1]	MWS_RX_PRI[0]	MWS_RX_PRI[1]

aaa-052077

Figure 29. Type 7: Vendor specific message - external radio to IW610

- The real time message from IW610 to the external radio indicates the arbitration results (Figure 30)
  - NB_Rx_Pri = 1: the narrowband radio Rx wins the arbitration and is in operation
  - NB_Tx_On = 1: the narrowband radio Tx wins the arbitration and is in operation
  - 802_Rx_Pri = 1: Wi-Fi Rx wins the arbitration and is in operation
  - 802_Tx_On = 1: Wi-Fi Tx wins the arbitration and is in operation
  - Otherwise, the external radio is granted

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	0	NB_RX_PRI	NB_TX_ON	802_RX_PRI	802_TX_ON	RFU

aaa-052078

Figure 30. Type 0: Real time signaling message - IW610 to external radio

WCI-2 coexistence interface supports the messages defined in Bluetooth Core Specification Vol 7 Part C for other purposes, such as:

- Transport control message from IW610 to the external radio to request real time message upon wake up (Figure 31)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	1	Resend_real_time	RFU	RFU	RFU	RFU

aaa-052079

Figure 31. Type 1: Transport control message time signaling message - IW610 to external radio

- MWS inactivity duration message from the external radio to IW610 indicates the inactivity duration to IW610 before going to sleep (Figure 32)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	1	1	Duration[0]	Duration[1]	Duration[2]	Duration[3]	Duration[4]

aaa-052081

Figure 32. MWS inactivity duration message

- MWS scan frequency message from the external radio to IW610 indicates the external radio scan frequency to IW610 (Figure 33)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
1	0	0	Freq[0]	Freq[1]	Freq[2]	Freq[3]	Freq[4]

aaa-052080

Figure 33. Type 5: MWS scan frequency message

11.7.1.3 WCI-2 signal waveform format

The messaging is based on a standard UART format.

Figure 34 shows the waveform for the transmit signal (UART_SOUT to UART_SIN).

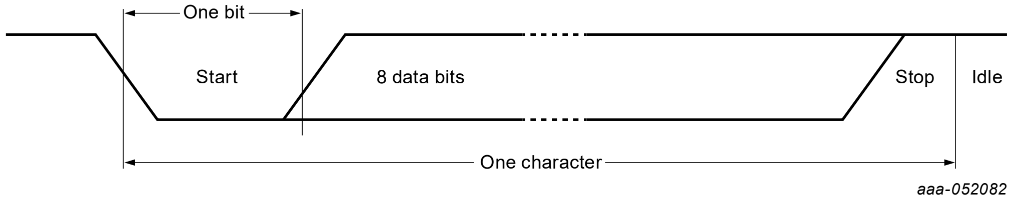


Figure 34. WCI-2 transmit signal waveform

Table 62. WCI-2 interface transport settings

Parameter	Range	Note
Baud rate	921600 ~ 4000000	Baud
Data bits	8	LSB first
Parity bits	0	No parity
Stop bit	1	One stop bit
Flow control	No	No flow control

11.7.2 PTA interface coexistence specifications

Figure 35 shows PTA coexistence interface signal timing diagram for the example where:

- Input: request, 1-bit priority
  - Priority ready at Request signal assertion
- Output: grant

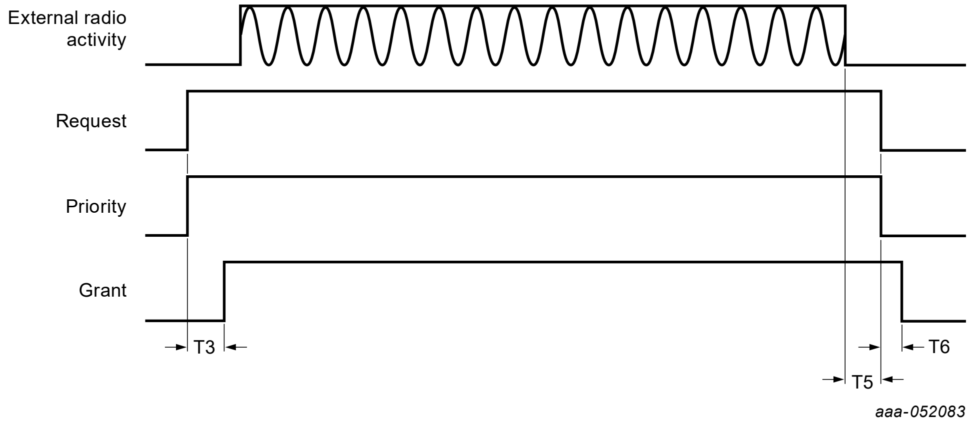


Figure 35. PTA coexistence interface timing diagram - Example 1

Figure 36 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority, state
  - Priority signal and State signal are ready at Request signal assertion
- Output: grant

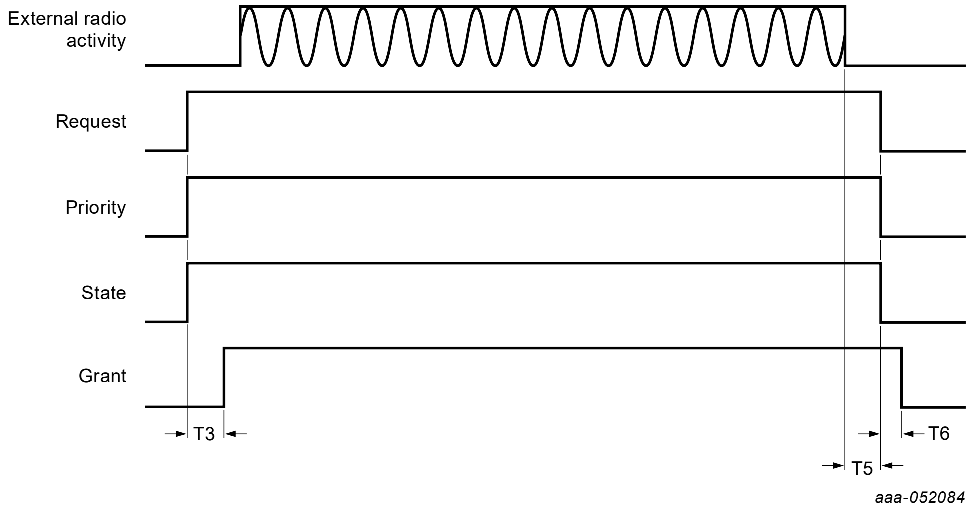


Figure 36. PTA coexistence interface timing diagram - Example 2

Figure 37 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority, frequency, state
  - Priority, State, and Frequency ready at Request assertion
- Output: grant

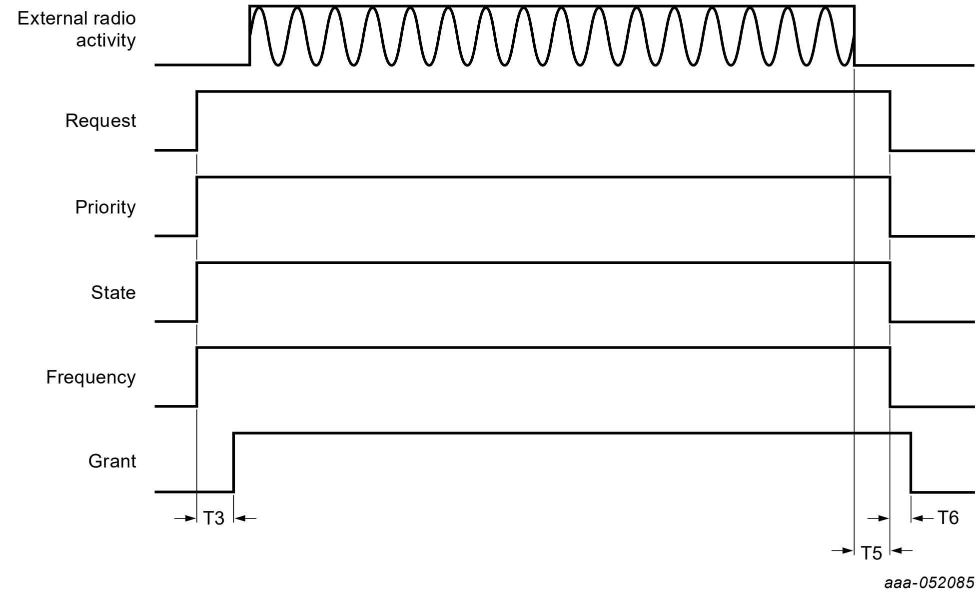


Figure 37. PTA coexistence interface timing diagram - Example 3

Figure 38 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority
  - Priority signal is ready at Request signal assertion
- Output: grant
  - Grant signal is de-asserted before Request signal de-assertion due to a traffic abort caused by other traffic with higher priority

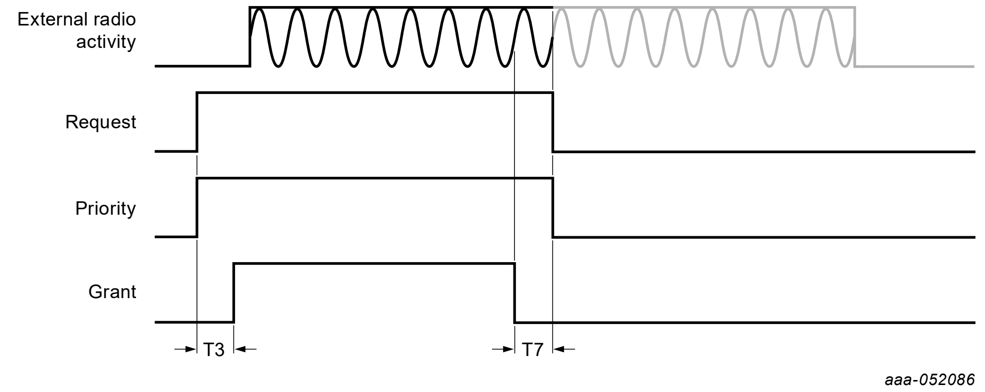


Figure 38. PTA coexistence interface timing diagram - Example 4

Figure 39 shows PTA coexistence interface timing diagram for the example where:

- Input: request and priority
  - Priority pin is sampled three times to obtain two priority bits and Tx/Rx info. No input from State pin.
- Output: grant

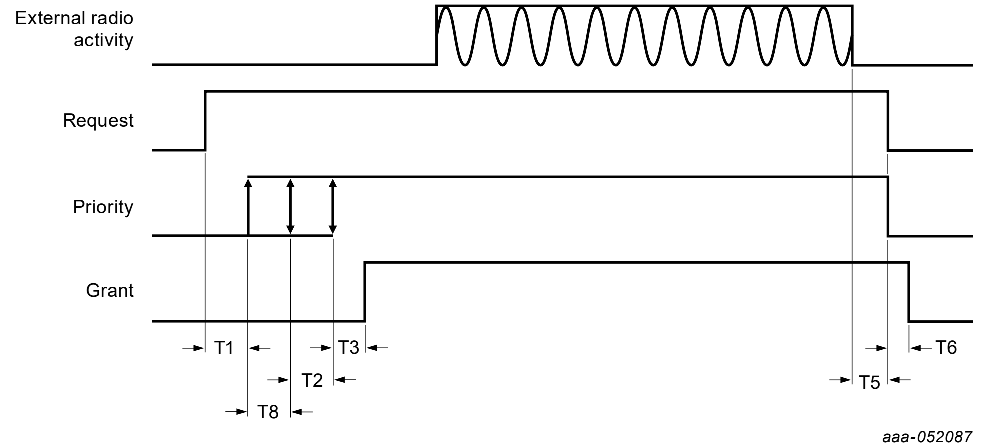


Figure 39. PTA coexistence interface timing diagram - Example 5

Table 63 provides the timing specifications for PTA coexistence interface signals.

Table 63. PTA coexistence interface signal timing data

Paramete	Conditions	Min	Typ.	Max	Unit
T1[1]	Priority[0] is sampled on Priority pin at T1 from Request assertion.	0	—	100	µs
T8[1]	Optional: priority[1], if present on Priority pin, is sampled at T1+T8 from Request assertion.	0.025	—	100	µs
T2[1]	Optional: Tx/Rx Info, if present on Priority pin, is sampled at T1+T2 (one priority bit on Priority pin) or T1+T8+T2 (two priority bits on Priority pin) from Request assertion.	0.025	—	100	µs
T3[2]	Time from all information available to BCA to grant decision ready	0.1	—	0.4	µs
T5[2]	The Request signal de-asserts T5 after the last symbol is done	—	—	—	µs
T6[2]	The Grant signal de-asserts T6 after the Request de-assertion	0.1	—	0.3	µs
T7[2]	The Request signal de-asserts T7 after the grant de-assertion due to a traffic abort.	—	—	—	µs

[1] Valid for serially sampled Priority pin
[2] Valid for all implementations

11.8 Host configuration specifications

For a list of configuration pins, see Section 6.7 "Configuration pins".

Table 64. Configuration pin specifications[1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Units
Internal weak pull-up resistance	Around 1 ms following any reset	—	800	—	kΩ
Internal weak pull-down resistance	Around 1 ms following any reset	—	700	—	kΩ
Internal nominal pull-up resistance	Around 1 ms following any reset	—	100	—	kΩ
Internal nominal pull-down resistance	Around 1 ms following any reset	—	90	—	kΩ

[1] After approximately 1 ms, the configuration pins become functional pins.

11.9 Reference clock specifications

11.9.1 Crystal oscillator specifications

Table 65. 40 MHz (38.4 MHz) crystal oscillator (XTAL) specifications

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Fundamental frequencies	—	—	40 (38.4)[1]	—	MHz
Equivalent differential load capacitance	—	—	8	—	pF
Shunt capacitance	—	—	2	—	pF
Frequency stability	Over operating temperature	—	±20	—	ppm
Aging	—	—	±2	—	ppm/ 5 years
Series resistance (ESR)	40 MHz/38.4 MHz XTAL	—	—	40	Ω
Insulation resistance	at DC 100V	500	—	—	MΩ
Maximum drive level	—	120	—	—	µW

[1] 40 MHz or 38.4 MHz are supported.

11.9.2 External crystal oscillator specifications

The reference clock from external crystal oscillator requires CMOS input signal.

Table 66. Clock DC specifications[1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Single-ended high-level voltage	—	—	—	1.8	V
Single-ended low-level voltage	—	0	—	—	V
Clock amplitude (pk-pk)	—	0.5	—	1	V
Mid-point slope	—	125	—	--	MV/s

[1] AC-coupling capacitor is integrated into the SoC.

Table 67. 38.4 MHz clock timing

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
XO38_4 period	—	26.04 - 20 ppm	26.04	26.04 + 20 ppm	ns
XO38_4 rise time	—	—	—	2.50	ns
XO38_4 fall time	—	—	—	2.50	ns
XO38_4 duty cycle	—	47.12	50	52.88	%

Table 68. 40 MHz clock timing

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
XO40 period	—	25.00 - 20 ppm	25.00	25.00 + 20 ppm	ns
XO40 rise time	—	—	—	2.00	ns
XO40 fall time	—	—	—	2.00	ns
XO40 duty cycle	—	47	50	53	%

Table 69. Phase noise

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Test Conditions	Min	Typ	Max	Unit
Fref = 38.4 MHz	Offset = 1 kHz	—	—	-130	dBc/Hz
	Offset = 10 kHz	—	—	-145	dBc/Hz
	Offset = 100 kHz	—	—	-155	dBc/Hz
	Offset > 1 MHz	—	—	-162	dBc/Hz
Fref = 40 MHz	Offset = 1 kHz	—	—	-130	dBc/Hz
	Offset = 10 kHz	—	—	-145	dBc/Hz
	Offset = 100 kHz	—	—	-155	dBc/Hz
	Offset > 1 MHz	—	—	-162	dBc/Hz

11.10 Power-down specifications

11.10.1 PDn asserted Low

Figure 40 and Table 70 show the specifications for the PDn signal when it is asserted (low) while AVDD18 ramps down.

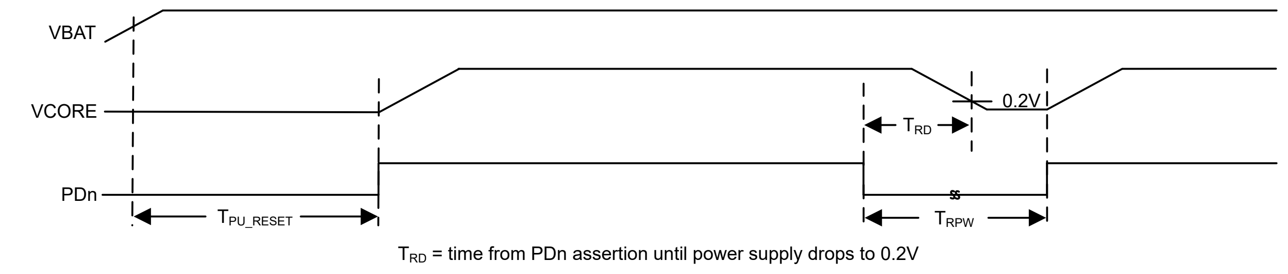


Figure 40. Power-down (PDn) pin timing—Power ramps down at PDn assertion

Table 70. Power-down (PDn) pin specifications—Power ramps down at PDn assertion

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{PU_RESET}	Valid power to PDn de-asserted	--	0	—	—	ms
T_{RPW}	PDn pulse width	--	T_{RD}[1]	—	—	µs
V_{IH}	Input high voltage	--	1.75	—	3.63	V
V_{IL}	Input low voltage	--	-0.4	—	0.2	V

[1] Minimum value guaranteed for a valid reset. Smaller values may put the device in an undefined state.

11.11 JTAG interface specifications

The test interface pins are powered by VIO voltage supply.

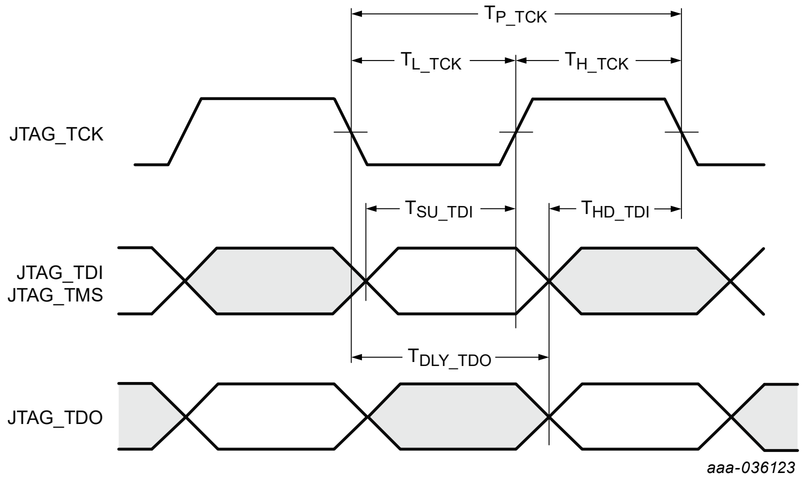


Figure 41. JTAG timing diagram

Table 71. JTAG interface protocol timing[1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK period	—	25	—	—	ns
T_{H_TCK}	TCK high	—	12	—	—	ns
T_{L_TCK}	TCK low	—	12	—	—	ns
T_{SU_TDI}	TDI, TMS to TCK setup time	—	5	—	—	ns
T_{HD_TDI}	TDI, TMS to TCK hold time	—	5	—	—	ns
T_{DLY_TDO}	TCK to TDO delay	—	0	—	7.5	ns

[1] Does not apply to JTAG enabled by the JTAG_TMS pin.

12 Package information

12.1 Package thermal conditions

12.1.1 QFN thermal conditions

Table 72. Package thermal conditions—QFN

Symbol	Rating	Board type[1]	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance[2]	JESD51-7, 2s2p	36.1	°C/W
$R_{\psi JT}$	Junction to top of package thermal characterization parameter[2]	JESD51-7, 2s2p	7.3	°C/W
$R_{\theta JC}$	Junction to case thermal resistance[2]	JESD51-7, 2s2p	12.0	°C/W

[1] The thermal test board meets JEDEC specification for this package (JESD51-7).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

12.1.2 WLCSP thermal conditions

Table 73. Package thermal conditions—WLCSP

Symbol	Rating	Board type[1]	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance[2]	JESD51-7, 2s2p	48.9	°C/W
$R_{\psi JT}$	Junction to top of package thermal characterization parameter[2]	JESD51-7, 2s2p	4.2	°C/W
$R_{\theta JC}$	Junction to case thermal resistance[2]	JESD51-7, 2s2p	12.6	°C/W

[1] The thermal test board meets JEDEC specification for this package (JESD51-7).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

12.2 WLCSP underfill

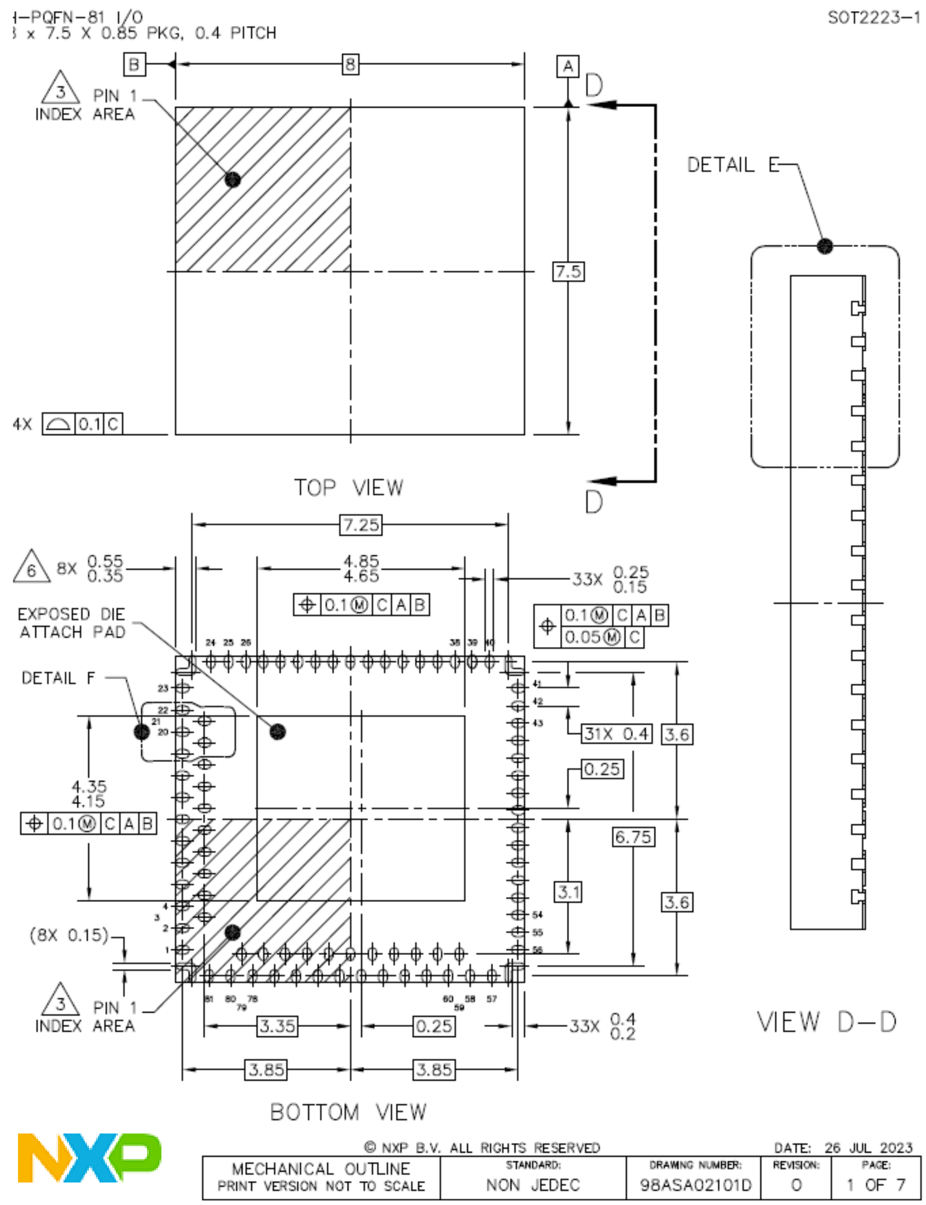
To meet NXP board level reliability (BLR) requirements of 500 temperature cycles between -40°C to +125°C (Ta), and prevent WLCSP reliability issues, it is mandatory to select a molded underfill (for molded module application) or capillary underfill material (for unmolded module applications). The molded underfill or capillary underfill material must have less than 20 ppm halide like chloride as per the material supplier specifications.

12.3 Package mechanical drawings

Table 74. Package information

Package name	Link to package information on NXP website
DRQFN-81	SOT2223-1 (link to be added)
WLCSP-114	SOT2235-1 (link to be added)

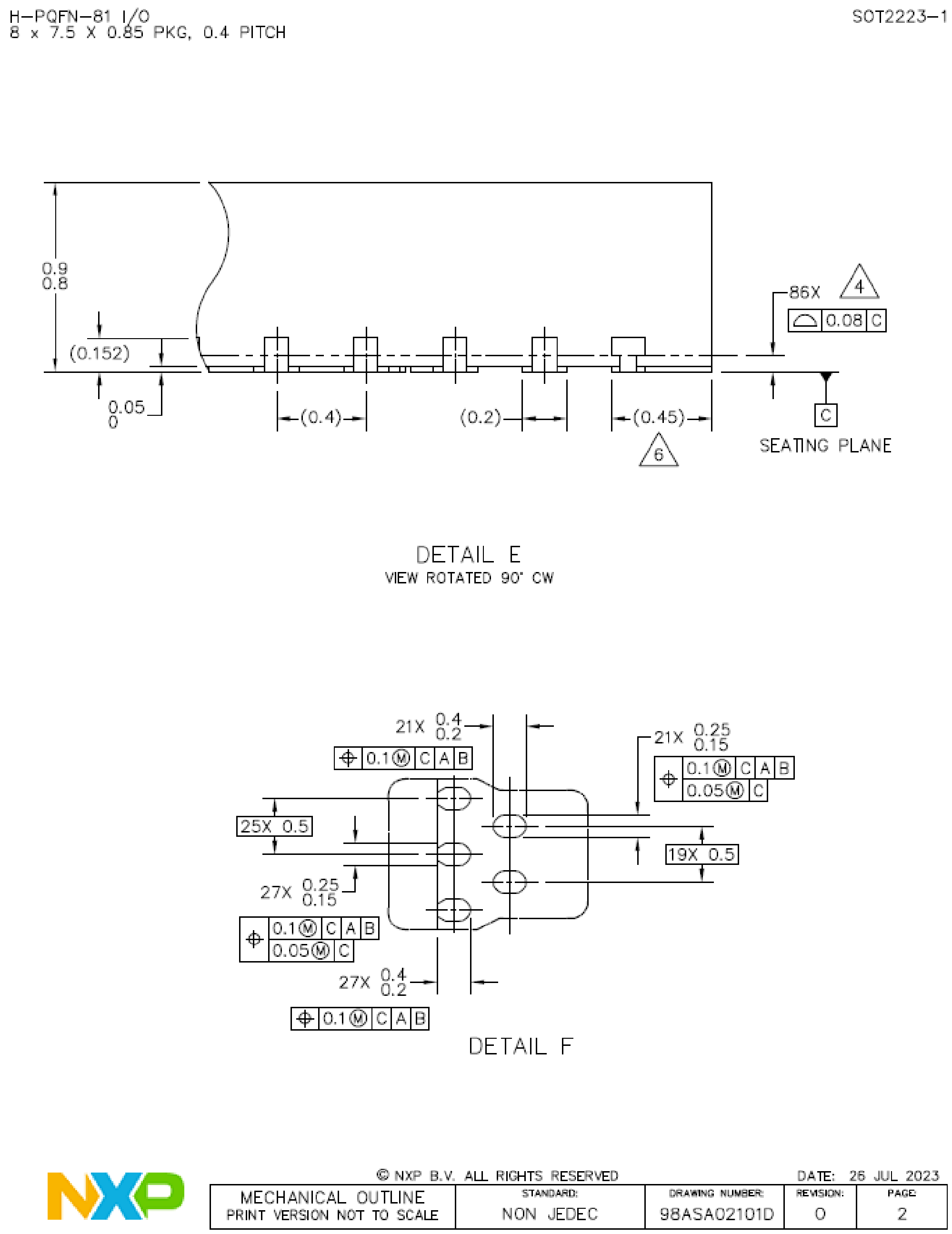
12.3.1 QFN package mechanical drawing



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.
6. ANCHORING PADS.

Figure 42. QFN package drawing



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.

5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.

6. ANCHORING PADS.

Figure 43. QFN package drawing - Details E

12.3.2 WLCSP package mechanical drawing

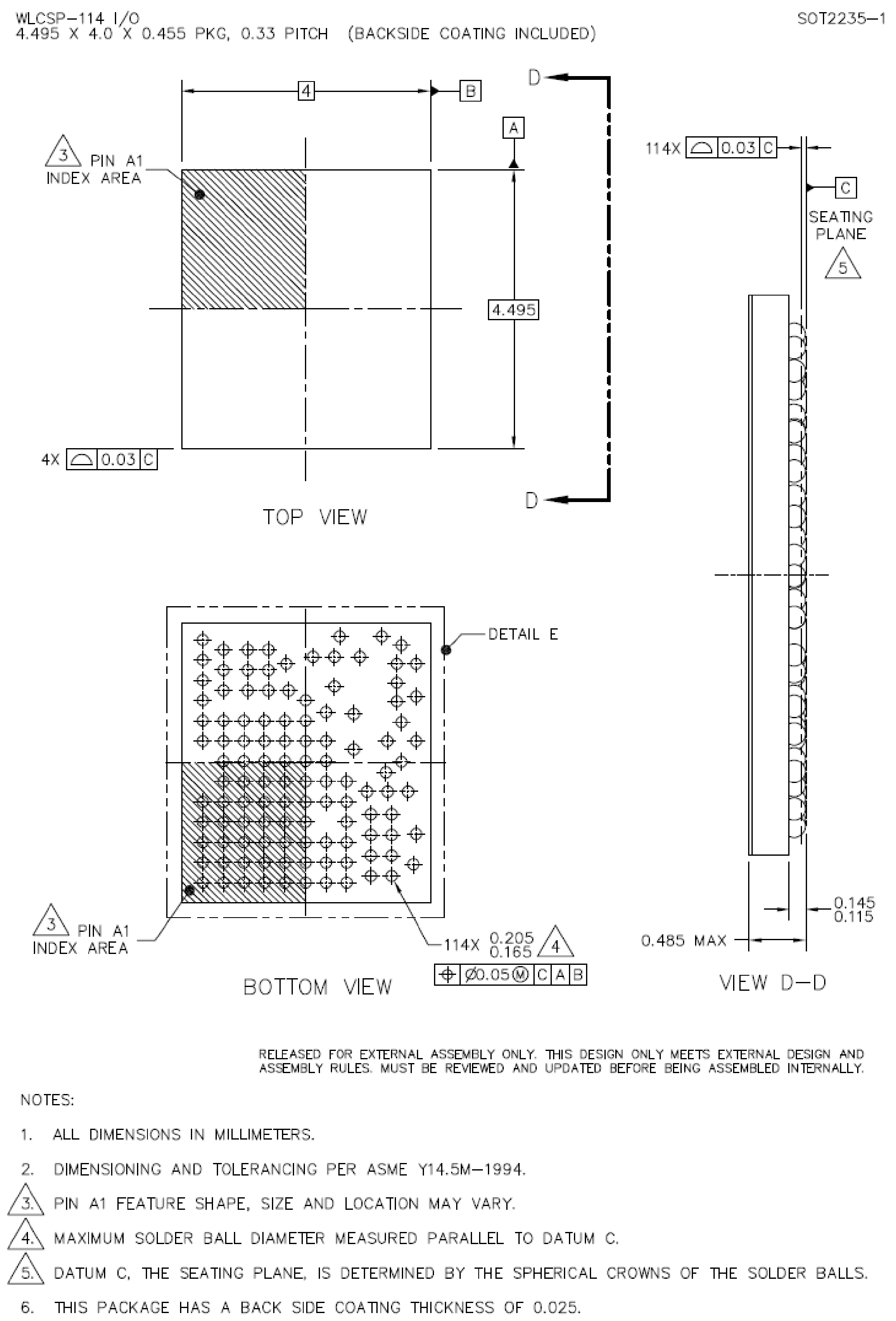
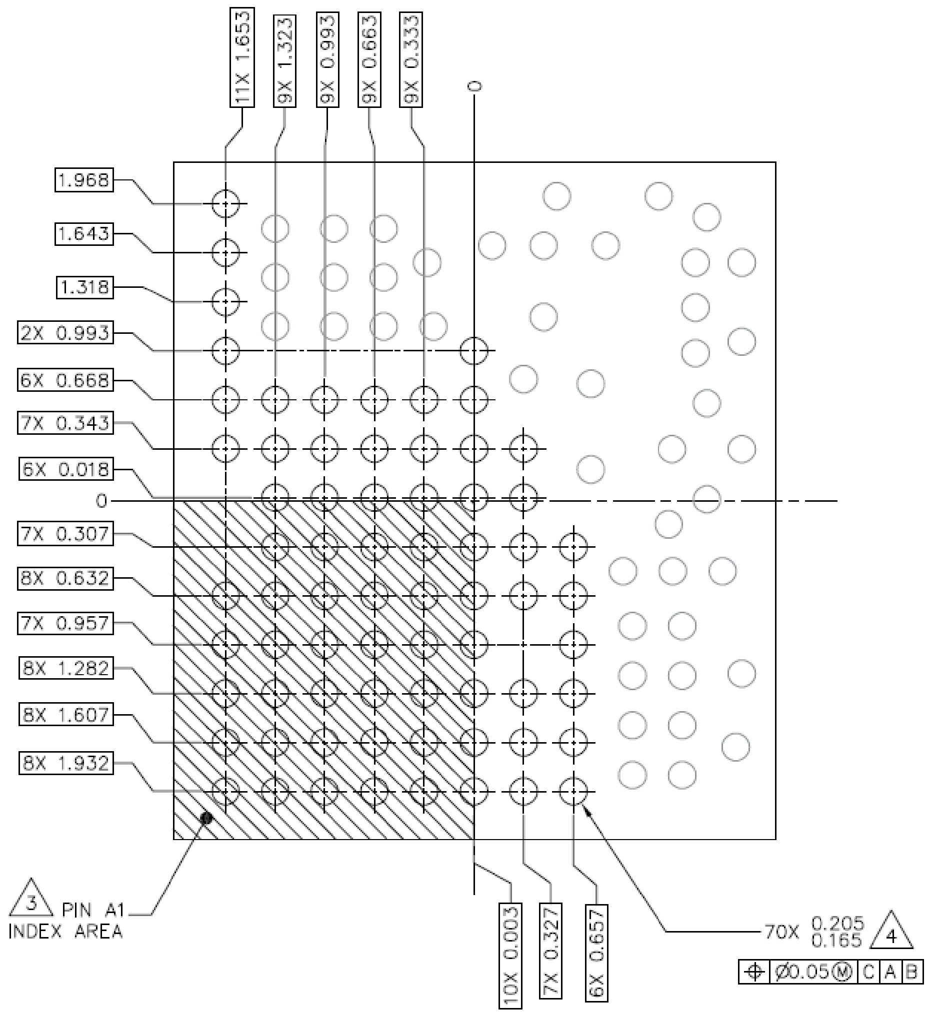


Figure 44. WLCSP package drawing

WLCSP–114 I/O
4.495 X 4.0 X 0.455 PKG, 0.33 PITCH (BACKSIDE COATING INCLUDED)

SOT2235–1

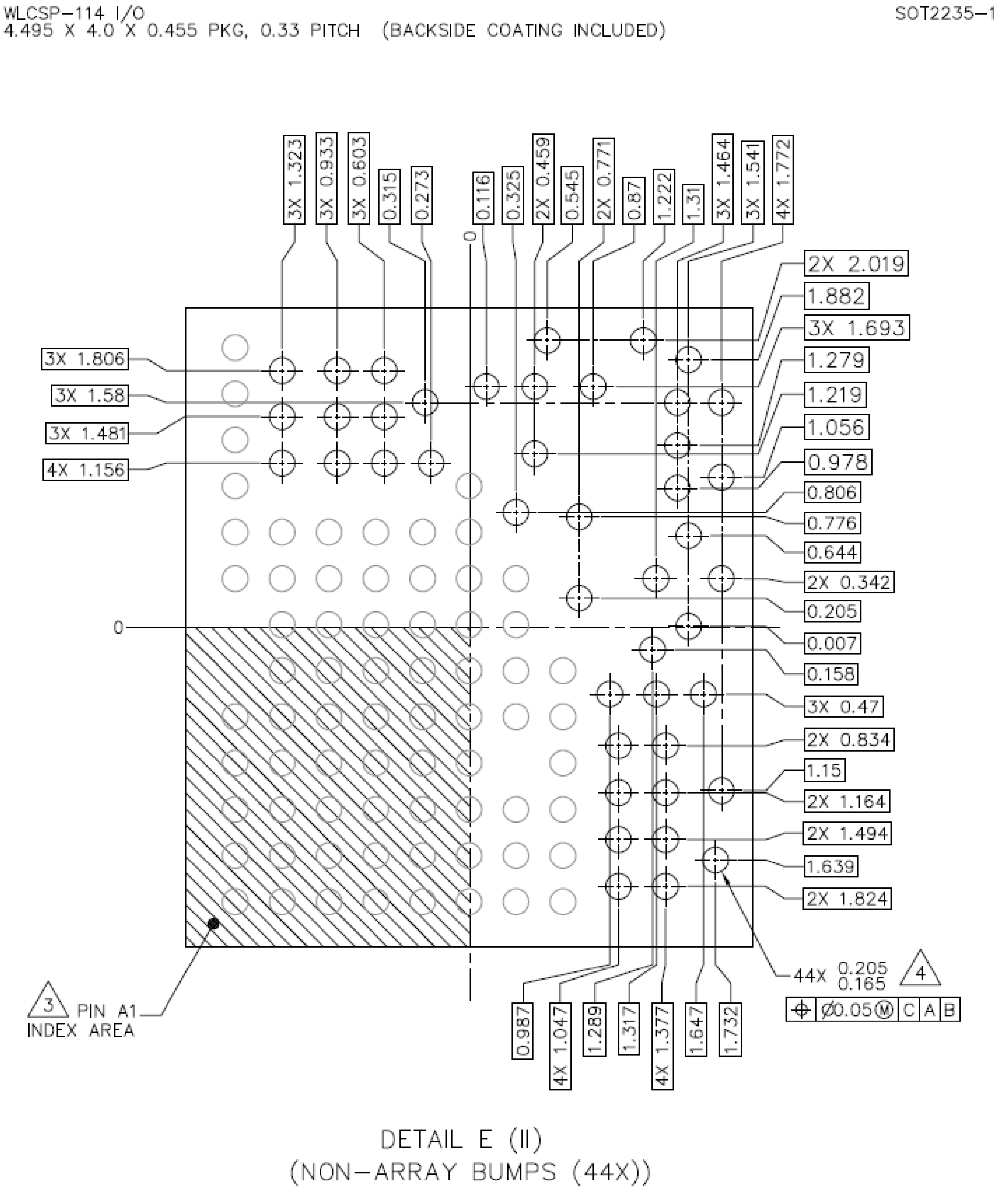


DETAIL E (I)
(ARRAY BUMPS (70X))

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

Figure 45. WLCSP package drawing - Details E (array bumps)



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

Figure 46. WLCSP package drawing - Details E (non-array bumps)

12.4 Package markings

12.4.1 QFN package marking

Figure 47 illustrates the location of pin 1 and marking on the QFN package for IW610G variant.

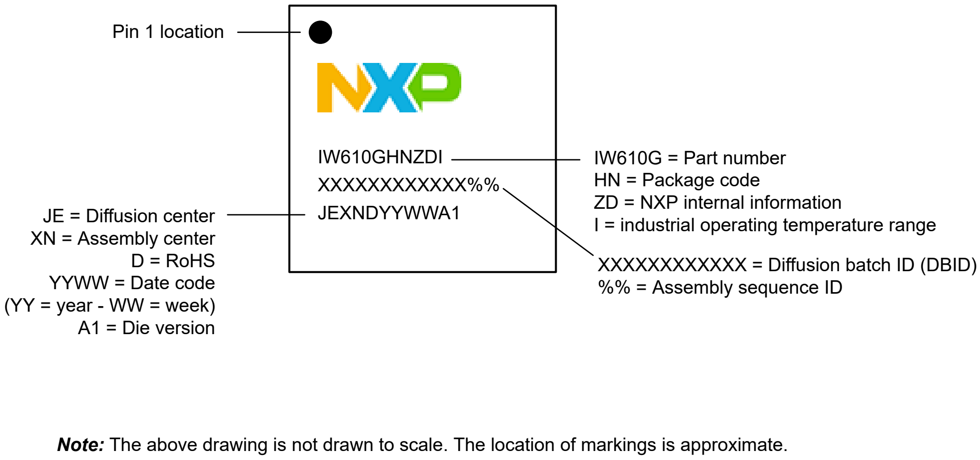


Figure 47. Marking and pin 1 location on QFN package—industrial operating temperature (12 digits max per line)

12.4.2 WLCSP package marking

Figure 48 illustrates the location of pin 1 and marking on WLCSP package for IW610G variant.

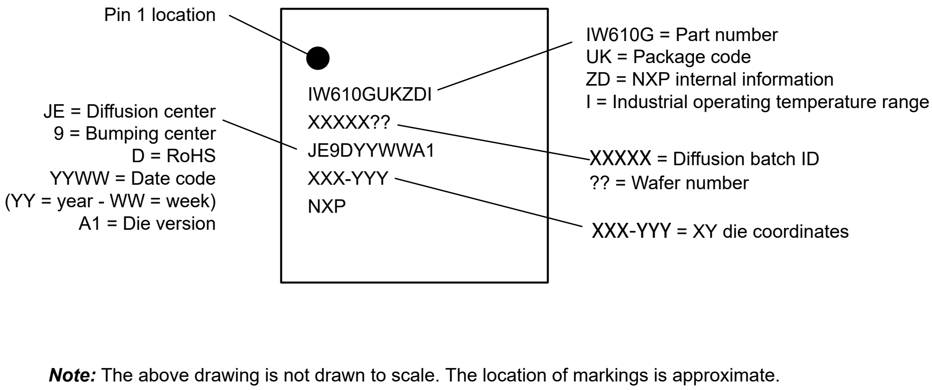


Figure 48. Marking and pin 1 location on WLCSP package—industrial operating temperature (12 digits max per line)

13 Abbreviations

Table 75. Abbreviations

Acronym	Definition
A2DP	Advanced audio distribution profiles
ACK	Acknowledgment
ADC	Analog-to-digital converter
AES	Advanced encryption standard
AFH	Adaptive frequency hopping
AGC	Automatic gain control
AP	Access point
Arm	Advanced RISC machine
BDR	Basic data rate
BOM	Bill of materials
BRF	Bluetooth RF unit
BSS	Basic service set
BTM	BSS transition management
CBC	Cipher block chaining
CCA	Clear channel assessment
CCK	Complementary code keying
CCMP	Counter mode CBC-MAC protocol
CMD	Command
CRC	Cyclic redundancy check
CTS	Clear to send
DAC	Digital-to-analog converter
DCF	Distributed coordination function
DFS	Dynamic frequency selection
DMA	Direct memory access
DPD	Digital pre distortion
DQPSK	Differential quadrature phase shift keying
DTIM	Delivery traffic indication message
EAP	Extensible authentication protocol
ED	Energy detect
EDCA	Enhanced distributed channel access
FIFO	First in first out
GATT	Generic attribute profile
GCMP	Galois/counter mode protocol
GI	Guard interval

Table 75. Abbreviations*...continued*

Acronym	Definition
GPIO	General purpose input/output
HID	Human interface device
HT	High throughput
HVQFN	Thermal enhanced very thin quad flat package
HW	Hardware
I/F	Interface
I/Q	In-phase/quadrature
IEEE	Institute of electrical and electronics engineers
JEDEC	Joint electronic device engineering council
JTAG	Joint test action group
LC3	Low complexity communication codec
LDPC	Low density parity check
LE	Low energy
LED	Light emitting diode
LNA	Low noise amplifier
LSB	Least significant byte
LTE	Long term evolution
MAC	Media/medium access controller
MCS	Modulation and coding scheme
MFP	Multi functional pin
MIMO	Multiple input multiple output
MPDU	MAC protocol data unit
MSb	Most significant bit
MSB	Most significant byte
MU-MIMO	Multi user MIMO
MU-PPDU	Multi user PPDU
MWS	Mobile wireless system Multimedia wireless system
NAV	Network allocation vector
NBS	Narrowband speech
NDP	Null data packet
Nsts	Number of space time streams
OFDM	Orthogonal frequency division multiplexing
OFDMA	Orthogonal frequency division multiple access
OTP	One time programmable
OTT	Over-the-top (device)

Table 75. Abbreviations*...continued*

Acronym	Definition
PA	Power amplifier
PCI	Peripheral component interconnect
PCM	Pulse code modulation
PDn	Power down
PHY	Physical layer
POS	Point of sale
PPDU	PHY protocol data unit
PSK	Pre shared keys
PTA	Packet traffic arbitration
QAM	Quadrature amplitude modulation
QFN	Quad flat non-leaded package
RF	Radio frequency
RIFS	Reduced inter frame space
RISC	Reduced instruction set computer
RSSI	Receiver signal strength indication
RTC	Real time clock
RTS	Request to send
SISO	Single input single output
SoC	System-on-chip
SPDT	Single pole double throw
SPI	Serial peripheral interface
STA	Station
TA	Transmitter address
TCP/IP	Transmission control protocol/internet protocol
TWT	Target wait time
UART	Universal asynchronous receiver/transmitter
UDP	User datagram protocol
VHT	Very high throughput
WAP	Wireless application protocol
WBS	Wide band speech
WCI-2	Wireless coexistence interface 2
WEP	Wired equivalent privacy
Wi-Fi	Hardware implementation of IEEE 802.11 for wireless connectivity
WLAN	Wireless local area network
WLCSP	Wafer level chip scale package
WPA	Wi-Fi protected access

Table 75. Abbreviations*...continued*

Acronym	Definition
WPA2	Wi-Fi protected access 2
WPA2-PSK	Wi-Fi protected access 2 - pre shared key
WPA3	Wi-Fi protected access 3
WPA-PSK	Wi-Fi protected access - pre shared key
XOSC	Crystal oscillator

14 References

[1] Application note – AN14384: IW610x USB Current Leakage (link)

15 Revision history

Table 76. Revision history

Document ID	Release date	Description
IW610 v.7.0	5 December 2024	Product data sheet
IW610x v.6.0	13 August 2024	Objective data sheet
IW610x v.5.0	11 July 2024	Objective data sheet
IW610x v.4.0	3 July 2024	Objective data sheet
IW610x v.3.0	5 March 2024	Objective data sheet.
IW610G v.2.0	12 October 2023	Objective data sheet.
IW610G v.1.0	27 June 2023	Objective data sheet – Initial release
IW610 v.1.0	6 April 2023	Objective data sheet – Early access release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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Contents

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