NXP Semiconductors
Data Sheet: Technical Data

Document Number: IMXRT1180IEC
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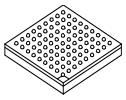
MIMXRT1189CVM8B **MIMXRT1187CVM8B**
MIMXRT1182CVP2B **MIMXRT1181CVP2B**

i.MX RT1180 Crossover Processors Data Sheet for Industrial Products



Package Information
Plastic Package
289-pin MAPBGA, 14 x 14 mm, 0.8 mm pitch
144-pin MAPBGA, 10 x 10 mm, 0.8 mm pitch

Ordering Information
See Table 1 on page 6

1 i.MX RT1180 introduction

The i.MX RT1180 is a high-performance processor of the i.MX RT family, which features a high performance Arm® Cortex®-M7 core operating at speeds up to 800 MHz and a power efficient Cortex®-M33 core up to 240 MHz.

i.MX RT1180 features industrial gateway capabilities that enable the support of Industrial Real-time protocol (Profinet, EtherCAT, EtherNet/IP, and etc) as well as the latest TSN based protocols through a state of the art Ethernet switch subsystem and a large 1.5 MB on-chip RAM protected with ECC.

The i.MX RT1180 further integrates advanced power management module with DCDC and LDO regulators that reduce complexity of external power supply and simplifies power sequencing, as well as a large subsystem to enable a large set of application: memory interfaces, connectivity interfaces (CAN-FD, LPUART, LPSPI, LPI2C, FlexIO, etc.). i.MX RT1180 also integrate an advance Secure Enclave subsystem.

The i.MX RT1180 is designed for applications over various segments such as Industrial automation,

Building automation, Energy, or IoT for example. It supports applications such as:

- AC Drives
- Servo Drive
- Gateway
- Motor Control
- Industrial Network companion chips

1.1 Features

The i.MX RT1180 processors are based on Arm® Cortex®-M7 Core™ Platform, which has the following features:

- The Arm Cortex-M7 Core Platform:
  - 32 KB L1 Instruction Cache and 32 KB L1 Data Cache
  - Floating Point Unit (FPU) with single-precision and double-precision supports of the Armv7-M architecture FPv5
  - Support the Armv7-M Thumb instruction set, defined in the Armv7-M architecture
  - Integrated Memory Protection Unit (MPU), up to 16 individual protection regions
  - Up to 512 KB I-TCM and D-TCM in total
  - Frequency of 800 MHz at 1.1 V (over drive) with Forward Body Biasing (FBB)
  - ECC support for both Cache and Tightly Coupled Memory (TCM)
  - Frequency of the core, as per Table 11, "Operating ranges," on page 26.
- The Arm Cortex-M33 Core platform:
  - Micro-controller available both for boot and customer application
  - 16 KB Code Cache, 16 KB System Cache, and 256 KB TCM (also accessible as SRAM by the rest of the system)
  - Frequency is 240 MHz at 1.0 V without body biasing
  - ECC support for both Cache and TCM
- On-chip memory:
  - Boot ROM (160 KB)
  - 512 KB TCM for CM7 with ECC
  - 256 KB TCM for CM33 with ECC
  - Dedicated 768 KB OCRAM with ECC
- External memory interfaces:
  - Smart External Memory Controller (SEMC)
    - 8/16/32-bit SDRAM interface, 4 Chip Selects (CS) and each CS up to 1024 Mb
    - 8/16-bit NAND FLASH interface with hardware ECC
    - 8/16-bit NOR FLASH interface
    - SRAM: supports SRAM and Pseudo SRAM, 8-bit and 16-bit modes, ADMUX, AADM, and Non-ADMUX modes, up to 4 CS, up to 4096 Mb memory size

  - 2x FlexSPI
    - Single/Dual channel Quad SPI FLASH with XIP support
    - Hyper RAM/FLASH
    - PSRAM
    - OCT RAM/FLASH
    - OTFAD is supported for decryption with 0 cycle delay

Each i.MX RT1180 processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Audio:
  - 1x SPDIF input and output
  - 4x Synchronous Audio Interface (SAI) modules supporting I2S, AC97, TDM, and codec/DSP interfaces
  - Digital microphone input, 8-channel PDM
  - Asynchronous Sample Rate Converter (ASRC)
- Connectivity:
  - 2x USB 2.0 OTG controllers with integrated PHY interfaces
  - 2x Ultra Secure Digital Host Controller (uSDHC) interfaces
    - uSDHC2 with boot support for eMMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec
    - uSDHC1 with boot support for SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100 MB/sec
    - Support for SDXC (extended capacity)
  - 12x low power universal asynchronous receiver/transmitter (LPUARTs) modules
  - 6x LPI2C modules
  - 2x I3C modules
  - 6x LPSPI modules
  - 3x Control Area Network (FlexCAN) modules, each with support in hardware to support Flexible Datarate (FD), with enhanced RX FIFO.
  - 2x FlexIO modules
  - Advanced and flexible Ethernet
    - Third version of NXP TSN switch IP (NETC 3.0)
    - Port virtualization support on ENETC0 MAC for dual Access (CM33/CM7)
    - Extended support of TSN standards over flexible architecture
    - 1x independent 1 Gbps TSN MAC endpoint
    - 5-port (4 external + 1 internal) TSN Switch with 1 Gbps TSN MAC
    - OPC UA Frame Summation HW acceleration integrated in switch
    - Up to 5 RGMII/MII/RMII external ports
  - 1x FlexSPI follower

  - Dual ports EtherCAT Slave Controller
- ADC/CMP
  - 2x 16-bit dual-channel SAR ADC (16 channels on ADC1 and 14 channels on ADC2), 3.5 Msps, each ADC can proceed 2 conversions simultaneously
  - 1x 12-bit DAC
  - 4x Analog Comparators (ACMP)
  - 3x SINC filters (4-channel) to interface to external sigma-delta ADC
  - Voltage Reference (VREF)
- GPIO and Pin Multiplexing:
  - General-purpose input/output (GPIO) modules with interrupt capability
  - Input/output multiplexing controller (IOMUXC) to provide centralized pad control

The i.MX RT1180 processors integrate advanced power management unit and controllers:

- Full PMIC integration, including on-chip DCDC and LDOs
- Temperature sensor with programmable trim points
- GPC Hardware power management controller
- Timers and PWMs:
  - 2x General Programmable Timer (GPT) modules
    - 4-channel generic 32-bit resolution timer for each
    - Each supports standard capture and compare operation
  - 3x Low Power Periodical Interrupt Timer (LPIT) modules
    - 4-channel
    - 4 external trigger sources
    - Generic 32-bit resolution timer
    - Periodical interrupt generation
  - 6x Timer/PWM modules (TPM)
    - Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
    - 16-bit counter, support free-running counter or modulo counter mode, counting up or down
    - Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
  - 3x Low-Power Timer (LPTMR) modules
  - 8x Quad Timer (TMR) modules
    - 4-channel generic 16-bit resolution timer for each
    - Each supports standard capture and compare operation
    - Enhanced Quadrature decoder integrated
  - 4x FlexPWM modules
    - Up to 8 individual PWM channels for each
    - 16-bit resolution PWM suitable for Motor Control applications

  - 4x Enhanced Quadrature Decoders (eQDC)
  - 6x Watchdog Timer (WDOG)
    - 1x for the Cortex-M33 non-secure, 1x for Cortex-M33 secure, 1x for the Cortex-M7 and 2x additional for customer usage
    - 1x External Watchdog Monitor (EWM)

The i.MX RT1180 processors support the following system debug:

- Arm Cortex-M7 CoreSight™ debug and trace architecture
- CoreSight Serial Wire Output (SWO) and Embedded Trace Router (ETR) can allow routing trace data to system memory
- Support for 5-pin (JTAG) and SWD debug interfaces

Security functions are enabled and accelerated by the following hardware:

- Trusted Resource Domain Controller (TRDC)
  - Supports up to 16 resource domains
- TrustZone®-M (TZ-M) on Cortex-M33
- Physical Unclonable Function (PUF)
- EdgeLock® secure enclave
  - Advanced security: AES, AES-GCM, PKA, ECDSA/ECDH, TRNG, AES-256, SHA, DES, 3DES, RSA4096, ECC1024, UniqueID, Secure Boot, Secure RTC, Tamper Monitor
  - Public Key co-processor
  - Symmetric Crypto Accelerators
  - Random number generator
  - One-Time Programmable electrical fuse used for security keys and configuration other security related functions
  - Physically Unclonable Function based master secrets as an option
- Battery Backed Security Module (BBSM)
  - Monotonic counter
  - Secure real-time clock (RTC)
  - Zeroizable Master Key
- Inline Encryption Engine (IEE)
  - External memory encryption and decryption
  - I/O direct encrypted storage and retrieval (Stream Support)
- On-The-Fly AES Decryption (OTFAD)
  - Support OTFAD with 4 keys

NOTE

The actual feature set depends on the part numbers as described in Table 1. Functions such as CM7 core platform, SEMC, connectivity interfaces, and SINC are not offered on all derivatives.

1.2 Ordering information

Table 1 provides examples of orderable part numbers covered by this Data Sheet.

Table 1. Ordering information

	Attribute	MIMXRT1189CVM8B	MIMXRT1187CVM8B	MIMXRT1182CVP2B	MIMXRT1181CVP2B
Qualification tier	—	Industrial			
Core platform	Cortex®-M7	800 MHz		—	
	M7 Cache	32 KB I-Cache 32 KB D-Cache		—	
	TCM (I/D/O)	512 KB (I/D) with ECC		—	
	Cortex®-M33	240 MHz			
	M33 Cache	16 KB C-Cache 16KB S-Cache			
	TCM (C/S)	256 KB with ECC			
On chip RAM	OCRAM	768 KB with ECC			
External memory	SEMC	1x 32-bit		—	
	FlexSPI	2			
	SRAMC	Yes			
Security	EdgeLock® Secure enclave	Yes			
	IEE	1			
	OTFAD	Yes			
	TRDC	Yes			
	BBSM	Yes			
	Secure key management	PUF			
	Tamper monitor	Yes			
	Tamper pin	10		4	
Audio	SPDIF	1			
	SAI	4			
	PDM	8			
	ASRC	1			
GPIO	Pin number	173		82	
	GPIO	Yes			
	FlexIO	2			

Table 1. Ordering information

	Attribute	MIMXRT1189CVM8B	MIMXRT1187CVM8B	MIMXRT1182CVP2B	MIMXRT1181CVP2B
Connectivity	USB 2.0 OTG controller	2		—	
	USB HS PHY	2		—	
	uSDHC	2		1	
	NETC 3.0	5-port		3-port[1]	
	EtherCAT slave controller	2-port	—	2-port	—
	FlexSPI follower	1			
	LPUART	12		8	
	LPI2C	6		3	
	I3C	2			
	KPP	1			
	LPSPI	6		4	
	CANFD	3		1	
Timer	GPT	2			
	LPIT	3			
	TMR	8		4	
	FlexPWM	4		2	
	eQDC	4		4	
	TPM	6		3	
	LPTMR	3		1	
	WDOG	5			
	EWM	1			
	TSTMR	1			
	SCTR	1			
Analog	SINC	3		—	
	16-bit ADC	2		1	
	VREF	1			
	DAC	1			
	ACMP	4			
Trigger	XBAR	3			
	AOI	4			

Table 1. Ordering information

	Attribute	MIMXRT1189CVM8B	MIMXRT1187CVM8B	MIMXRT1182CVP2B	MIMXRT1181CVP2B
Package	—	289 MAPBGA, 14 mm x 14 mm, 0.8 mm pitch		144 MAPBGA, 10 mm x 10 mm, 0.8 mm pitch	
Junction temperature T_j (°C)	—	-40 to 105			

1 See RT1182 and RT1181 PINMUX information about port MAC interface type and speed limitations.

Figure 1 describes the part number nomenclature so that characteristics of a specific part number can be identified (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which data sheet applies to a specific part is the temperature grade (junction) field.

- The i.MX RT1180 Crossover Processors for Industrial Products Data Sheet (IMXRT1180IEC) covers parts listed with a “C (Industrial temp)”

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there is any question, visit the web page nxp.com/IMXRT or contact an NXP representative for details.

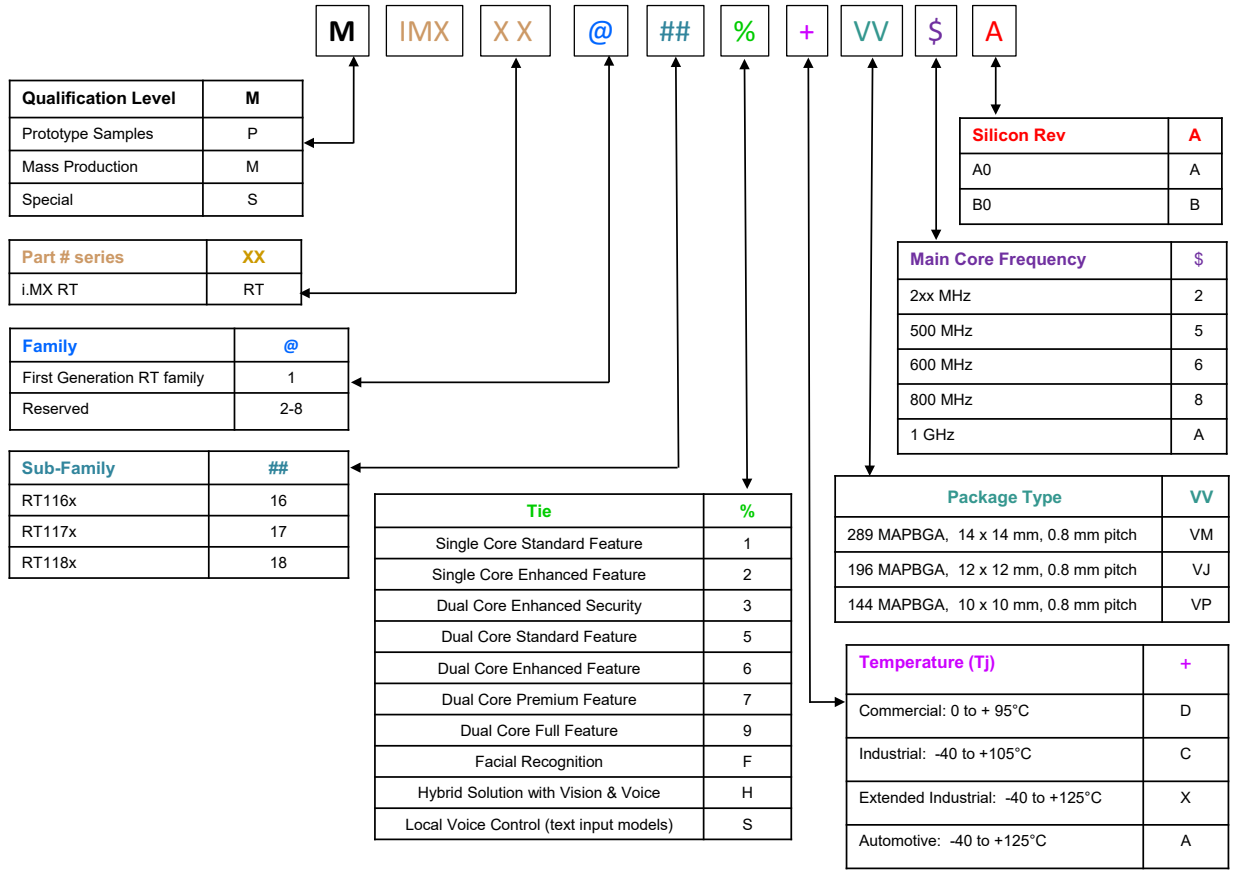


Figure 1. Part number nomenclature—i.MX RT1180

1.3 Package marking information

Figure 2 describes the package marking format about the i.MX RT1180 Crossover Processors.

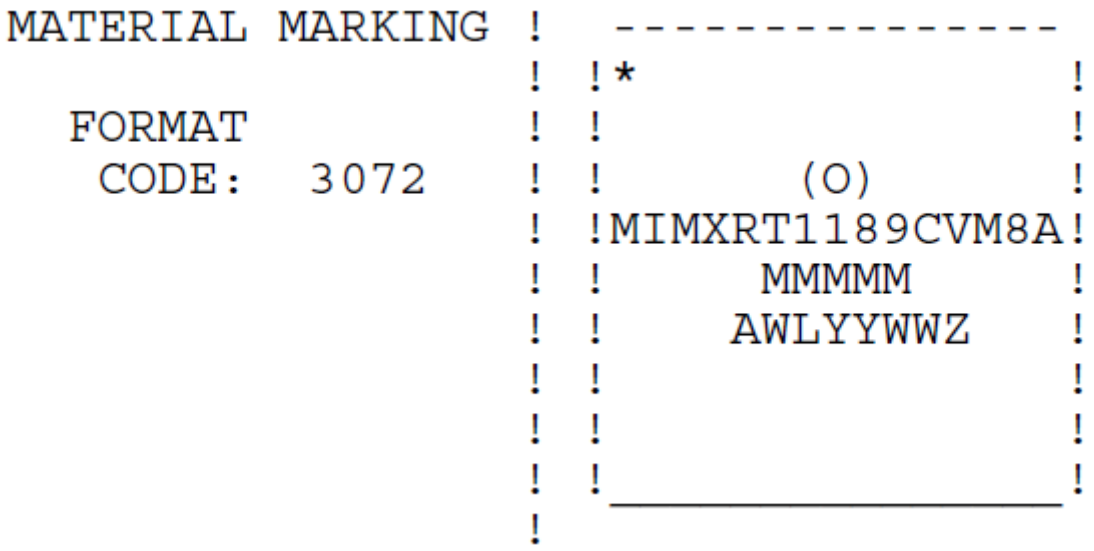


Figure 2. Package marking format

i.MX RT1180 packages have following top-side marking:

- First line: aaaaaaaaaaaaaa
- Second line: mmmmm
- Third line: xxxyywwx

Table 2 lists the identifier decoder.

Table 2. Identifier decoder for package

Identifier	Description
a	Part number code, refer to Section 1.2, Ordering information
m	Mask set
y	Year
w	Work week
x	NXP internal use

2 Architectural overview

The following subsections provide an architectural overview of the i.MX RT1180 processor system.

2.1 Block diagram

Figure 3 shows the functional modules in the i.MX RT1180 processor system[1].

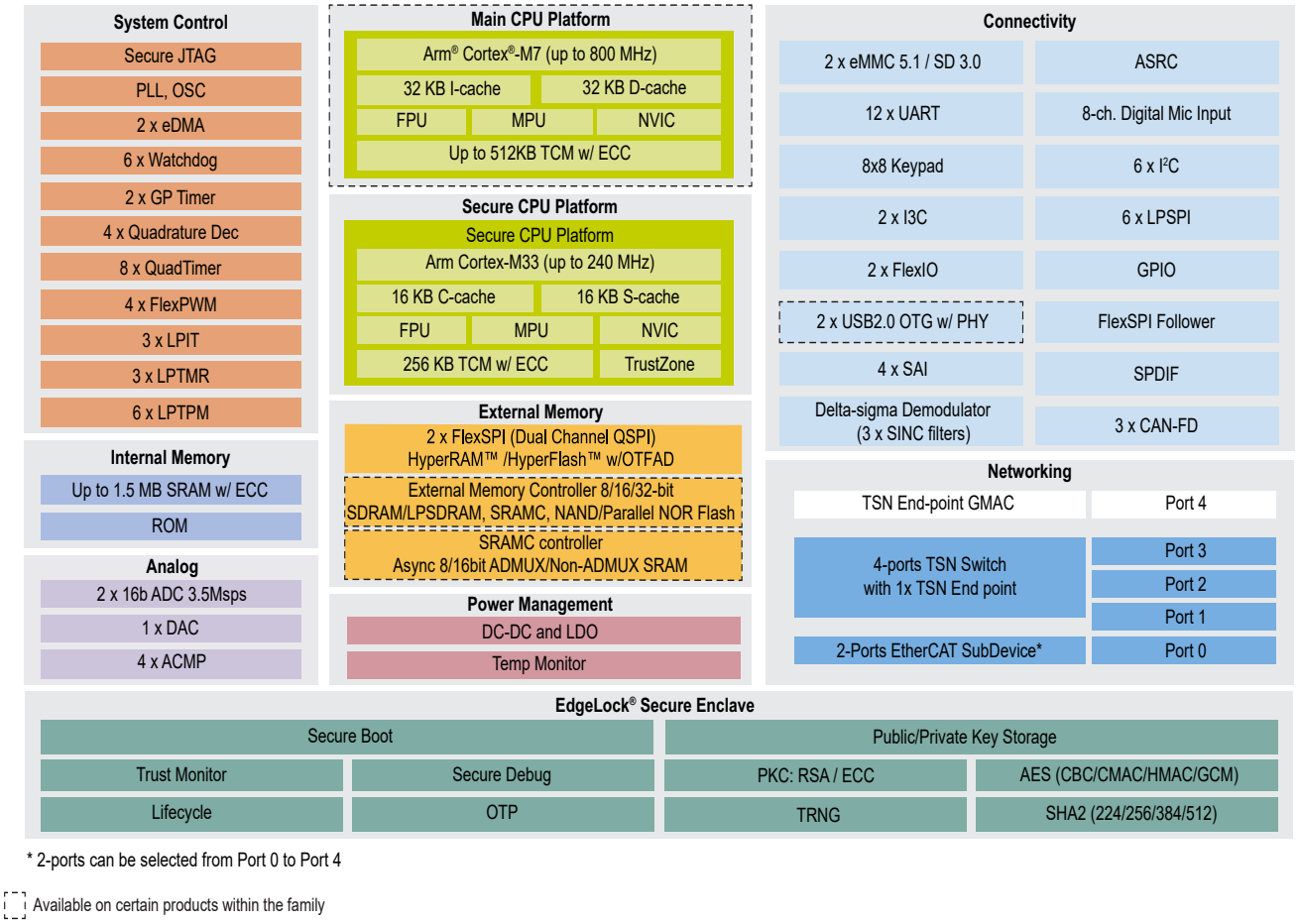


Figure 3. i.MX RT1180 system block diagram

1. Some modules shown in this block diagram are not offered on all derivatives. See Table 1 for details.

3 Modules list

The i.MX RT1180 processors contain a variety of digital and analog modules. Table 3 describes these modules in alphabetical order.

Table 3. i.MX RT1180 modules list

Block Mnemonic	Block Name	Subsystem	Brief Description
ACMP1 ACMP2 ACMP3 ACMP4	Analog Comparator	Analog	Comparator (CMP) provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail-to-rail operation).
ADC1 ADC2	Analog to Digital Converter	Analog	ADC is a 16-bit general purpose analog to digital converter.
AOI1 AOI2 AOI3 AOI4	And-Or-Inverter	Cross Trigger	AOI provides a universal Boolean function generator using a four-term sum of products expression with each product term containing true or complement values of the four selected inputs (A, B, C, D).
Arm	Arm Platform	Arm	Arm Core Platform includes one Cortex-M7 core. It includes associated sub-blocks, such as Nested Vectored Interrupt Controller (NVIC), Floating-Point Unit (FPU), Memory Protection Unit (MPU), CoreSight debug modules, and 512 KB TCM. The Cortex-M33 platform has following features: • Cortex-M33 processor with FPU • Local memory – 16 KB Code Cache and 16 KB System Cache – TCM memories support ECC – Cache memories support ECC
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	ASRC can process groups of audio channels with an independent time-based simultaneously.
BBSM	Battery backed security module	Security	BBSM is in the low power section in the battery backed by the VBAT (or RTC) power domain. This enables it to keep this data valid and continue to increment the time counter when the power goes down in the rest of device. The always-powered up part of the module is isolated from the rest of the logic to ensure that it is not corrupted when the device is powered down.
BBNSM	Battery Backed non-Secure Module	Security	BBNSM works with BBSM to keep this data valid and continue to increment the time counter when the power goes down in the rest of the device.
CANFD1 CANFD2 CANFD3	Flexible Controller Area Network	Connectivity and Communications	CAN with Flexible Data rate (CAN FD) module is a communication controller implementing the CAN protocol according to the ISO11898-1 and CAN 2.0B protocol specification.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.

Table 3. i.MX RT1180 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DAC	Digital-Analog-Converter	Analog	DAC is a 12-bit general purpose digital to analog converter.
DAP	Debug Access Port	System Control Peripherals	DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-M7 Core Platform and Cortex-M33 Core Platform.
DCDC	DCDC Converter	Analog	DCDC module is used for generating power supply for core logic. Main features are: • Adjustable high efficiency regulator • Over current and over/under voltage detection
eDMA	enhanced Direct Memory Access	System Control Peripherals	There are two enhanced DMAs (eDMA). • The eDMA is a 32-channel DMA engine, which is capable of performing complex data transfers with minimal intervention from a host processor.
EdgeLock® Secure Enclave	EdgeLock® Secure Enclave	Security	EdgeLock® secure enclave is preconfigured to help ease the complexity of implementing robust, system-wide intelligent security and avoid costly errors. This fully integrated built-in security subsystem is a standard feature.
eQDC1 eQDC2 eQDC3 eQDC4	Enhanced Quadrature Decoder	Timer Peripherals	Enhanced quadrature decoder module provides interfacing capability to position/speed sensors. There are five input signals: PHASEA, PHASEB, INDEX, TRIGGER, and HOME. This module is used to decode shaft position, revolution count, and speed.
EIM	Error Injection Module	Memory and Memory Controller	Error Injection Module (EIM) is mainly used for diagnostic purposes. It provides a method for diagnostic coverage of internal memories (for example, system RAM, Cache RAMs, and peripheral memories). See the chip-specific EIM information to determine which functional safety features are supported by this method.
ERM	Error Reporting Module	Memory and Memory Controller	Error Reporting Module (ERM) provides information and optional interrupt notification on memory error events associated with ECC and parity. The ERM collects error events on memory accesses for memory arrays, such as flash memory, system RAM, or peripheral RAMs. ERM supports various channels for memory sources where each ERM channel is associated with a different memory module. See the chip-specific ERM information for details about supported memory sources and specific memory channel assignments. If memory supports ECC then ERM syndrome and error address information is captured along with error event. ERM does not receive this information in case of Cache or memory with parity along with error event.

Table 3. i.MX RT1180 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EtherCAT	Ethernet for Control Automation Technology	Connectivity and Communication	An EtherCAT Slave Controller (ESC) takes care of the EtherCAT communication as an interface between the EtherCAT fieldbus and the slave application.
EWM	External Watchdog Monitor	Timer Peripherals	EWM modules is designed to monitor external circuits, as well as the software flow. This provides a back-up mechanism to the internal WDOG that can reset the system. The EWM differs from the internal WDOG in that it does not reset the system. The EWM, if allowed to time-out, provides an independent trigger pin that when asserted resets or places an external circuit into a safe mode.
FlexIO1 FlexIO2	Flexible Input/output	Connectivity and Communications	FlexIO is capable of supporting a wide range of protocols, including but not limited to UART, I2C, SPI, I2S, camera interface, display interface, PWM waveform generation, etc. The module can remain functional when the chip is in a low power mode provided the clock it is using remain active.
FlexPWM1 FlexPWM2 FlexPWM3 FlexPWM4	Pulse Width Modulation	Timer Peripherals	Pulse-width modulator (PWM) contains four PWM sub-modules, each of which is set up to control a single half-bridge power stage. Fault channel support is provided. The PWM module can generate various switching patterns, including highly sophisticated waveforms.
FlexSPI1 FlexSPI2	Flex Serial Peripheral Interface	Memory and Memory Controller	FlexSPI acts as an interface to external serial memory devices such as NOR/NAND Flash, PSRAM and HyperRAM etc. Each FlexSPI supports two ports: A and B. Each port of FlexSPI1 supports Single/Dual/Quad/Octal mode data transfer (1/2/4/8 bidirectional data lines), while each port of FlexSPI2 supports Single/Dual/Quad mode data transfer (1/2/4 bidirectional data lines).
FlexSPI Follower	Flex Serial Peripheral Interface Follower	Connectivity and Communications	FlexSPI follower provides a FlexSPI interface, which can be act as a FlexSPI device. FlexSPI follower module act as a gasket between FlexSPI and AXI bus, As AXI master, FlexSPI can access all memory mapped register and memory.
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6	General Purpose I/O Modules	Human Machine Interfaces	HMI is used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.

Table 3. i.MX RT1180 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPT1 GPT2	General Purpose Timer	Timer Peripherals	General Purpose Timer (GPT) is a 32-bit up-counter with clock source and frequency scaling options to provide a wide range of timing rates for various system applications. External hardware can send the GPT a “capture event” signal on an input pin to load the current timer value into a register for software to read. This capture signal can be configured to trigger the GPT on a rising or/and falling edge. Also, when the timer matches a preset value, the GPT can generate an interrupt for software and a “compare event” signal on output pins for external hardware.
I3C1 I3C2	Improved Inter Integrated Circuit	Connectivity and Communications	I3C is a control bus interface for connecting peripherals to an application processor.
IOMUXC	IOMUX Control	IOMUX Control	IOMUXC together with the IOMUX, enables the IC to share one pad to several functional blocks. This sharing is done by multiplexing the pad’s input and output signals.
JTAGC	JTAG Controller	System Control Peripherals	JTAGC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX RT1180 processors use JTAG port for production, testing, and system debugging. In addition, the JTAGC provides BSR (Boundary Scan Register) standard support, which complies with IEEE 1149.1 and IEEE 1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX RT1180 JTAGC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
KPP	Keypad Port	Human Machine Interfaces	KPP is a 16-bit peripheral that can be used as a keypad matrix interface or as general purpose input/output (I/O). It supports 8 x 8 external key pad matrix. Main features are: • Multiple-key detection • Long key-press detection • Standby key-press detection • Supports a 2-point and 3-point contact key matrix
LPI2C1 LPI2C2 LPI2C3 LPI2C4 LPI2C5 LPI2C6	Low Power Inter-integrated Circuit	Connectivity and Communications	LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus. The LPI2C provides a method of communication between a number of external devices. More detailed information, see Section 4.8.2, LPI2C module timing parameters.

Table 3. i.MX RT1180 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LPIT1 LPIT2 LPIT3	Low Power Periodical Interrupt Timer	Timer Peripherals	LPIT features 32-bit counter timer, programmable count modules, clock division features, interrupt generation, and a slave mode to synchronize count enable for multiple LPITs.
LPSPI1 LPSPI2 LPSPI3 LPSPI4 LPSPI5 LPSPI6	Low Power Serial Peripheral Interface	Connectivity and Communications	LPSPI is a low power Serial Peripheral Interface (SPI) module that support an efficient interface to an SPI bus as a master and/or a slave. • It can continue operating while the chip is in stop modes, if an appropriate clock is available • Designed for low CPU overhead, with DMA off loading of FIFO register access
LPTMR	Low Power Timer	Timer Peripherals	Low power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.
LPUART1 LPUART2 LPUART3 LPUART4 LPUART5 LPUART6 LPUART7 LPUART8 LPUART9 LPUART10 LPUART11 LPUART12	UART Interface	Connectivity and Communications	Each of the UART modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 20 Mbps.
MECC64	Memory ECC Controller	Memory and Memory Controller	Memory ECC Controller (MECC64) module supports Single Error Correction and Double Error Detection (SEC-DED) ECC functions to On-Chip RAM (OCRAM) access. It can generate a 8-bit ECC code by Hsiao Hamming algorithm for 64-bit data. Corresponding OCRAM space is available to store ECC code. When ECC function is disabled, ECC OCRAM can also be used to store data.
MU	Messaging Unit	System Control Peripherals	Messaging Unit module (MU) enables two processors within the SoC to communicate and coordinate by passing messages (e.g. data, status and control) through the MU interface. The MU also provides the ability for one processor to signal the other processor using interrupts.

Table 3. i.MX RT1180 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
NETC	Ethernet Controller	Connectivity and Communications	NETC complex is comprised of two main parts: • The PCIe Integrated Endpoint Root Complex (iEPRC) • The NET Controller (NETC) NETC exists as an Integrated End-Point (iEP) in the Root Complex and is optionally discoverable by software using standard PCIe device drivers. iEPRC is described in general terms as a host for one or more iEPs with its own address map. As an iEP, NETC is required to respond to PCIe configure requests by implementing a PCIe Config Type0 header.
PDM	Pulse Density Modulation	Multimedia Peripherals	PDM supports up to 8-channels (4 lanes).
RTC OSC	Real Time Clock Oscillator	Clock Sources and Control	RTC OSC provides the clock source for the Real-Time Clock module. The RTC OSC module, in conjunction with an external crystal, generates a 32.768 kHz reference clock for the RTC.
SAI1 SAI2 SAI3 SAI4	Synchronous Audio Interface	Multimedia Peripherals	SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.
SCTR	System Counter	Timer Peripherals	System Counter (SCTR) is a programmable system counter, which provides a shared time base to multiple processors. It is intended for applications where the counter is always powered on, and supports multiple clocks.
SEMA42	Semaphores	System Control Peripherals	SEMA42 is a memory-mapped module that provides robust hardware support needed in multi-core systems for implementing semaphores and provides a simple mechanism to achieve “lock and unlock” operations via a single-write access. The hardware semaphore module provides hardware-enforced gates as well as other useful system functions related to the gating mechanisms.
SEMC	Smart External Memory Controller	Memory and Memory Controller	SEMC is a multi-standard memory controller optimized for both high-performance and low pin-count. It can support multiple external memories in the same application with shared address and data pins. The interface supports SDRAM, NOR Flash, SRAM, and NAND Flash, as well as 8080 display.
SINC1 SINC2 SINC3	SINC filter	Analog	SINC filter is an integrated module to convert external sigma-delta ADC modulator bit stream to data stream.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.

Table 3. i.MX RT1180 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SRAMC	SRAM Controller	Memory and Memory Controller	i.MX RT1180 provides a memory mapped SRAMC to CM7 AHBBP to achieve fast access.
SYS OSC	System Clock Oscillator	Clock Sources and Control	SYS OSC provides the primary clock source for all PLLs to generate the clock for CPU, BUS, and high-speed interfaces. The SYS OSC module, in conjunction with an external crystal, generates a 24 MHz reference clock.
TEMPSNS	Temperature Sensor	Analog	Temperature sensor implements a temperature sensor/conversion function based on a temperature-dependent voltage to time conversion.
TMR1 TMR2 TMR3 TMR4 TMR5 TMR6 TMR7 TMR8	Quad Timer (TMR)	Timer Peripherals	Quad timer provides four time channels with a variety of controls affecting both individual and multi-channel features. Specific features include up/down count, cascading of counters, programmable module, count once/repeated, counter preload, compare registers with preload, shared use of input signals, prescaler controls, independent capture/compare, fault input control, programmable input filters, and multi-channel synchronization.
TSTMR	Time Stamp Timer	Timer Peripherals	Time Stamp Timer (TSTMR) is a 56-bit clock cycle counter, reset by system reset.
TPM1 TPM2 TPM3 TPM4 TPM5 TPM6	Timer/PWM Module	Timer Peripherals	TPM is a 2-channel to 8-channel timer, which supports input capture, output compare, and generation of PWM signals to control electric motor and power management applications.
USB1 USB2	Universal Serial Bus 2.0	Connectivity and Communications	USB OTG modules (USB OTG1 and USB OTG2) contains: • Two high-speed OTG 2.0 modules with integrated HS USB PHYs • Support eight Transmit (TX) and eight Receive (Rx) endpoints, including endpoint 0
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity and Communications	Ultra Secured Digital Host Controller (uSDHC) provides the interface between the host system and the eMMC, SD card, and SDIO card. The module acts as a bridge, passing host bus transactions to the eMMC, SD card, and SDIO card by sending commands and performing data accesses to/from the cards. It handles the SD card/SDIO card/eMMC protocols at the transmission level.
VREF	Reference voltage	Analog	VREF can be used in applications to provide a reference voltage to external devices, or used internally in the device as a reference to analog peripherals (such as the ADC, DAC, or CMP).

Table 3. i.MX RT1180 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG1 WDOG2 WDOG3 WDOG4 WDOG5	Watchdog	Timer Peripherals	Watchdog (WDOG) Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
XBAR1 XBAR2 XBAR3	Cross BAR	Cross Trigger	Each crossbar switch is an array of muxes with shared inputs. Each mux output provides one output of the crossbar. The number of inputs and the number of muxes/outputs are user configurable and registers are provided to select which of the shared inputs are routed to each output.

3.1 Special signal considerations

Table 4 lists special signal considerations for the i.MX RT1180 processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, Package information and contact assignments." Signal descriptions are provided in the *i.MX RT1180 Reference Manual* (IMXRT1180RM).

Table 4. Special signal considerations

Signal Name	Remarks
GPIO_AON_00, GPIO_AON_01, GPIO_AON_02	If not using eFuse setting, these I/Os level determine the boot mode. In case of boot mode pins immediately change state after POR_B released, user must ensure POR_B remains asserted until the last power rail reach its working voltage.
CLK1_P/ CLK1_N	It is used only for internal test, please keep CLK1_N/P pairs unconnected.
DCDC_PSWITCH	PAD is in DCDC_IN domain and connected the ground to bypass DCDC. To enable DCDC function, assert to DCDC_IN with at least 1ms delay after the DCDC_IN reaches the stable working voltage.
RTC_XTALI/RTC_XTALO	To hit the exact oscillation frequency, the board capacitors must be reduced to account for the board and chip parasitics. The integrated oscillation amplifier is self-biasing, but relatively weak. Care must be taken to limit the parasitic leakage from RTC_XTALI and RTC_XTALO to either the power or the ground (> 100 MΩ). This de-biases the amplifier and reduces the start-up margin. If you want to feed an external low-frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven by a complementary signal. The logic level of this forcing clock must not exceed the VDD_BBSM_ANA level and the frequency shall be < 100 kHz under the typical conditions. When a high-accuracy real-time clock is not required, the system may use the on-chip RTC oscillator. The tolerance is ±25%. The ring oscillator starts faster than the external crystal and is used until the external crystal reaches a stable oscillation. The ring oscillator also starts automatically if no clock is detected at RTC_XTALI at any time.
XTALI/XTALO	The system requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, refer to section of Bypass Configuration (24 MHz) from the reference manual. The logic level of this forcing clock must not exceed the VDD_AON_ANA level.
JTAG_*nnnn*	External resistors can be used with all JTAG signals except for JTAG_TDO, but they are not required as the internal pull resistors design. See Table 5 for a summary of the JTAG interface.
NC	These signals are No Connect (NC) and should be disconnected by the user.
POR_B	See the System Boot chapter in the reference manual for the correct boot configuration. Note that an incorrect setting may result from an improper boot sequence. POR_B signal has internal 100 kΩ pull-up resistor in BBSM domain, can pull up to VDD_BBSM_ANA if need to add external pull-up resistor, otherwise it will cause additional leakage during BBSM (Battery) mode. It is recommended to add the external reset IC to the circuit to guarantee POR_B is properly processed during power up/down, please refer to the EVK design for details. Note: • As the Low DCDC_IN detection threshold is 2.6 V, the reset IC's reset threshold must be higher than 2.6 V, then the whole chip is reset before the internal DCDC module reset to guarantee the chip safety during power down. • For power on reset, on any condition ones need to make sure the voltage on DCDC_PSWITCH pin is below 0.5 V before power-up.

Table 4. Special signal considerations (continued)

Signal Name	Remarks
ONOFF	A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately five seconds (or more) to GND causes a forced OFF.
TEST_MODE	This input is reserved for NXP manufacturing use. The user must tie this pin directly to GND.
WAKEUP	A GPIO powered by BBSM domain power supply which can be configured as wakeup source in BBSM (Battery) mode.

Table 5. JTAG Controller interface summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	20–50 kΩ pull-down
JTAG_TMS	Input	20–50 kΩ pull-up
JTAG_TDI	Input	20–50 kΩ pull-up
JTAG_TDO	3-state output	None
JTAG_TRSTB	Input	20–50 kΩ pull-up

3.2 Recommended connections for unused analog interfaces

Table 6 shows the recommended connections for unused analog interfaces.

Table 6. Recommended connections for unused analog interfaces

Module	Pad Name	Recommendations if Unused
RTC OSC	RTC_XTALI, RTC_XTALO	Not connected It is recommended that RTC_XTALI ties to GND if external crystal is not connected.
ADC	ADC_VREFH	10 kΩ resistor to ground
	VDDA_ADC_1P8	10 kΩ resistor to ground
	VDDA_ADC_3P3	10 kΩ resistor to ground
CCM	CLK1_N, CLK1_P	Not connected
DAC	DAC_OUT	Not connected
DCDC	DCDC_IN, DCDC_IN_Q	Not connected
	DCDC_SENSE, DCDC_LP	Not connected
	DCDC_PSWITCH, DCDC_MODE	To ground

Table 6. Recommended connections for unused analog interfaces (continued)

Module	Pad Name	Recommendations if Unused
USB	USB1_DN, USB1_DP, USB1_VBUS, USB2_DN, USB2_DP, USB2_VBUS	Not connected
	VDD_USB_1P8	Powered with 1.8 V
	VDD_USB_3P3	Powered with 3.3 V
SYS OSC	XTALI, XTALO	Not connected

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX RT1180 processors.

4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 7 for a quick reference to the individual tables and sections.

Table 7. i.MX RT1180 **chip-Level conditions**

For these characteristics	Topic appears
Absolute maximum ratings	on page 22
Thermal characteristics	on page 24
Operating ranges	on page 26
Maximum supply currents	on page 28
Typical power mode supply currents	on page 29
System power and clocks	on page 33

4.1.1 Absolute maximum ratings

CAUTION

Stress beyond those listed under Table 8 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 8 shows the absolute maximum operating ratings.

Table 8. Absolute maximum ratings

Parameter Description	Symbol	Min	Max	Unit
Power for digital logics	VDD_SOC	-0.3	1.2	V
Power for AON domain	VDD_AON_IN	-0.3	3.96	V
Power for DCDC	DCDC_IN	-0.3	3.96	V
Power for PLL, OSC, and LDOs	VDDA_1P8_IN	-0.3	1.98	V
Power for BBSM and Real Time Clock	VDD_BBSM_IN	-0.3	3.96	V
Power for USB OTG PHYs	VDD_USB_1P8	-0.3	1.98	V
	VDD_USB_3P3	-0.3	3.96	V
USB VBUS supply	USB1_VBUS USB2_VBUS	-0.3	5.6	V

Table 8. Absolute maximum ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
Power for ADC, DAC, and ACMP	VDDA_ADC_1P8	-0.3	1.98	V
	VDDA_ADC_3P3	-0.3	3.96	V
	ADC_VREFH	-0.3	1.98	V
IO supply for GPIO in SDIO1 bank (3.3 V mode)	NVCC_SD1	-0.3	3.96	V
IO supply for GPIO in SDIO1 bank (1.8 V mode)		-0.3	1.98	V
IO supply for GPIO in SDIO2 bank (3.3 V mode)	NVCC_SD2	-0.3	3.96	V
IO supply for GPIO in SDIO2 bank (1.8 V mode)		-0.3	1.98	V
IO supply for GPIO in EMC bank1 (3.3 V mode)	NVCC_EMC1	-0.3	3.96	V
IO supply for GPIO in EMC bank1 (1.8 V mode)		-0.3	1.98	V
IO supply for GPIO in EMC bank2 (3.3 V mode)	NVCC_EMC2	-0.3	3.96	V
IO supply for GPIO in EMC bank2 (1.8 V mode)		-0.3	1.98	V
IO power for GPIO in GPIO AD bank (3.3 V mode)	NVCC_GPIO_AD	-0.3	3.96	V
IO power for GPIO in GPIO AD bank (1.8 V mode)		-0.3	1.98	V
IO supply for GPIO in GPIO_B1 bank (3.3 V mode)	NVCC_GPIO1	-0.3	3.96	V
IO supply for GPIO in GPIO_B1 bank1 (1.8 V mode)		-0.3	1.98	V
IO supply for GPIO in GPIO_B2 bank (3.3 V mode)	NVCC_GPIO2	-0.3	3.96	V
IO supply for GPIO in GPIO_B2 bank1 (1.8 V mode)		-0.3	1.98	V
IO power for GPIO in AON bank (3.3 V mode)	NVCC_AON	-0.3	3.96	V
IO power for GPIO in AON bank (1.8 V mode)		-0.3	1.98	V
IO power for GPIO in BBSM bank (1.8 V mode)	NVCC_BBSM	-0.3	1.98	V
Input/Output Voltage range	V_{in}/V_{out}	-0.5	NVCC + 0.3[1]	V
Storage Temperature range	$T_{STORAGE}$	-55	150	^{o} C

1 NVCC is the I/O supply voltage.

Table 9. Electrostatic discharge and latch-up characteristics

Symbol	Description	Min	Max	Unit	Notes
V_{HBM}	Electrostatic discharge voltage: human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage: charged-device model	-500	+500	V	2
I_{LAT}	Immunity level • Class II @105 ^{o}C ambient temperature	-100	+100	mA	3

1 Determined according to JEDEC Standard JS001, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).*

2 Determined according to JEDEC Standard JS002, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.*

3 Determined according to JEDEC Standard JESD78, *IC Latch-up Test*.

4.1.2 Thermal characteristics

Table 10 displays the package thermal characteristics.

Table 10. Thermal characteristics

Rating	Board Type[1]	Symbol	Value		Unit
			10 x 10 mm	14 x 14 mm	
Junction to Ambient Thermal Resistance	JESD51-9, 2s2p	$R_{\theta JA}$[2]	28.1	26.3	°C/W
Junction-to-Top of Package Thermal Characterization Parameter[3]	JESD51-9, 2s2p	Ψ_{JT}[4]	0.8	0.8	°C/W
Junction to Case Thermal Resistance[5]	JESD51-9, 1s	$R_{\theta JC}$[6]	10.7	9.6	°C/W

1 Thermal test board meets JEDEC specification for this package (JESD51-9).

2 $R_{\theta JA} = (T_j - T_a)/P$ [unit: °C/W], where T_j = junction temperature, T_a = ambient temperature, P = device power.

3 Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

4 $\Psi_{JT} = (T_j - T_x)/P$ [unit: °C/W], where T_j = junction temperature, T_x = temperature at top of package, P = device power.

5 Junction-to-Case thermal resistance determined using an isothermal topside heat extraction. Case temperature is the package topside temperature.

6 $R_{\theta JC} = (T_j - T_c)/P$ [unit: °C/W], where T_j = junction temperature, Tc = case temperature, P = device power.

4.1.3 Power architecture

Full PMIC integration is the key advantage of i.MX RT1180 architecture. It simplifies hardware design and also reduces BOM cost.

- Integrated one DCDC to generated core power supply with dynamic voltage scaling capability
- Integrated LDOs to generate power for internal logics
- Integrated multiple Power Switches for sophisticated power mode management

The power architecture of i.MX RT1180 is as below, which shows the typical use case that the whole system works with a single 3.3 V power supply and a coin cell, similar to the power system of traditional MCU. For some other applications, i.MX RT1180 can have different power supply scheme. For example, with DCDC bypassed.

Figure 4 shows the power architecture of i.MX RT1180.

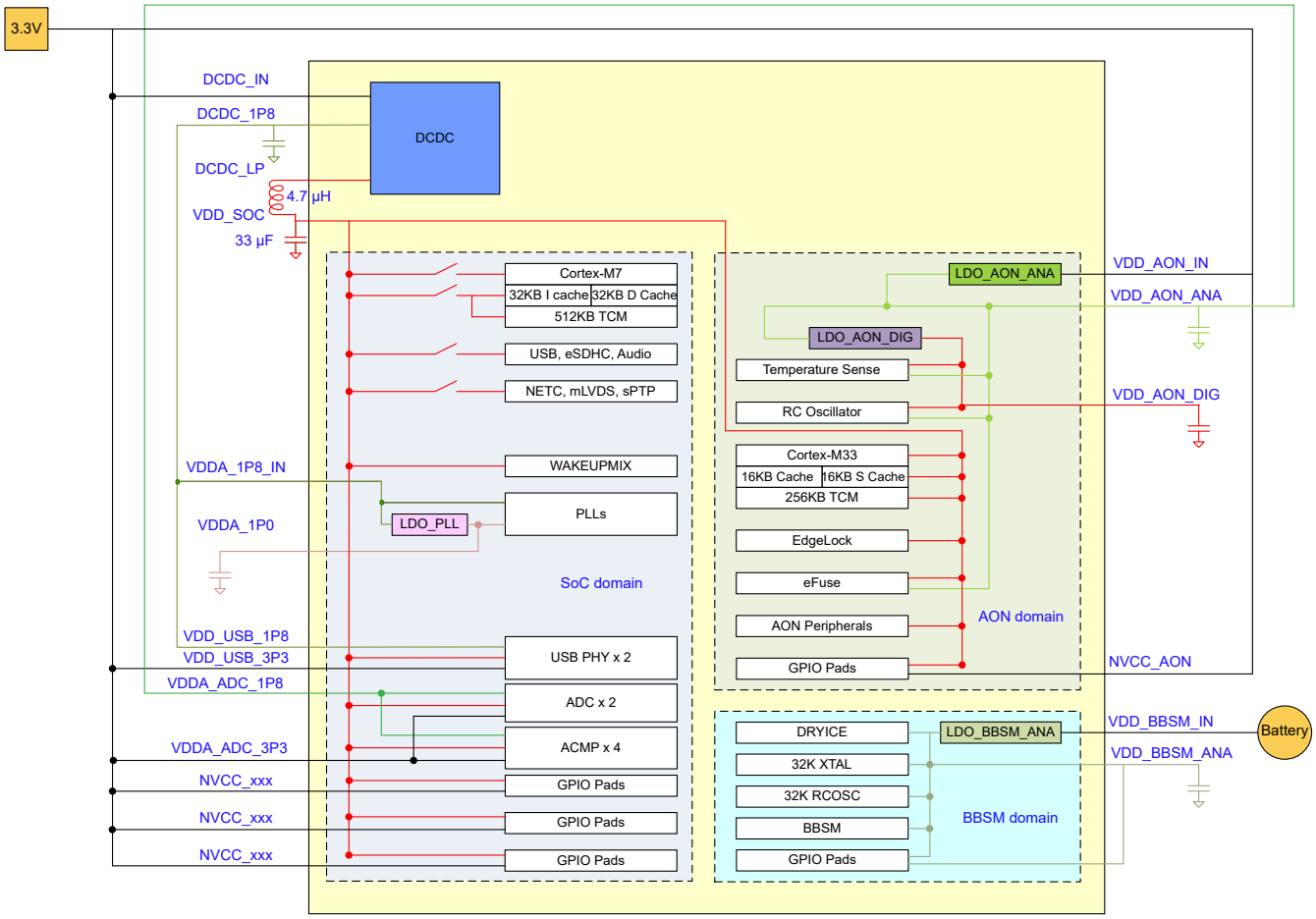


Figure 4. The power architecture

4.1.4 Operating ranges

Table 11 provides the operating ranges of the i.MX RT1180 processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX RT1180 Reference Manual* (IMXRT1180RM).

Table 11. Operating ranges

Parameter Description	Symbol	Operating Conditions	Min	Max[1]	Unit	Comment
Run Mode	VDD_SOC	M7 core at 800 MHz	1.1	1.15	V	Enable FBB when the frequency is higher than 600 MHz.
		M7 core at 600 MHz	1.0	1.15	V	—
		M7 core at 360 MHz	0.9	1.15	V	—
		M33 core at 240 MHz	1.0	1.15	V	—
		M33 core at 100 MHz	0.9	1.15	V	—
Standby Mode	VDD_SOC	—	0.8	1.15	V	See Table 13. Typical power modes current and power consumption (Dual core) and Table 14. Typical power modes current and power consumption (Single core)
Power for DCDC	DCDC_IN	—	3.0	3.6	V	—
Power for PLL, OSC, and LDOs	VDDA_1P8_IN	—	1.71	1.89	V	—
Power for AON domain	VDD_AON_IN	—	3.0	3.6	V	—
Power for BBSM and RTC	VDD_BBSM_IN	—	2.4	3.6	V	—
Power for USB OTG PHYs	VDD_USB_1P8	—	1.65	1.95	V	—
	VDD_USB_3P3	—	3.0	3.6	V	—
USB VBUS supply	USB_VBUS	—	2.4	5.5	V	—
Power for ADC, DAC, and ACMP	VDDA_ADC_1P8	—	1.65	1.95	V	—
	VDDA_ADC_3P3	—	3.0	3.6	V	—
	ADC_VREFH	—	1.0	1.98	V	—

Table 11. Operating ranges (continued)

Parameter Description	Symbol	Operating Conditions	Min	Max[1]	Unit	Comment
GPIO supplies	NVCC_SD1	—	3.0	3.6	V	IO power for GPIO in SDIO1 bank (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in SDIO1 bank (1.8 V mode)
	NVCC_SD2	—	3.0	3.6	V	IO power for GPIO in SDIO2 bank (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in SDIO2 bank (1.8 V mode)
	NVCC_EMC1	—	3.0	3.6	V	IO power for GPIO in EMC bank1 (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in EMC bank1 (1.8 V mode)
	NVCC_EMC2	—	3.0	3.6	V	IO power for GPIO in EMC bank2 (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in EMC bank2 (1.8 V mode)
	NVCC_GPIO_AD	—	3.0	3.6	V	IO power for GPIO in GPIO bank (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in GPIO bank (1.8 V mode)
	NVCC_GPIO1	—	3.0	3.6	V	IO power for GPIO in GPIO B1 bank (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in GPIO B1 bank (1.8 V mode)
	NVCC_GPIO2	—	3.0	3.6	V	IO power for GPIO in GPIO B2 bank (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in GPIO B2 bank (1.8 V mode)
	NVCC_AON	—	3.0	3.6	V	IO power for GPIO in AON bank (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in AON bank (1.8 V mode)
	NVCC_BBSM	—	1.65	1.95	V	IO power for GPIO in BBSM bank (1.8 V mode)
Temperature Operating Ranges						
Junction temperature	Tj	Standard Industrial	-40	105	°C	See the application note, i.MX RT1180 Product Lifetime Usage Estimates for information on product lifetime (power-on years) for this processor.

[1] Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V_{min} + the supply tolerance). This results in an optimized power/speed ratio.

4.1.5 Maximum supply currents

The data shown in Table 12 represents a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 Cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention were to specifically show the worst case power consumption.

Table 12. Maximum supply currents

Power Rail	Comments	Max Current	Unit
DCDC_IN	Maximum current for chip at 105 °C	1000	mA
VDDA_1P8_IN	1.8 V power supply for PLL, OSC, and LDOs	50	mA
VDD_SOC	1.0 V power supply for digital logics	1000	mA
VDD_AON_IN	3.3 V power supply for AON domain	75	mA
VDD_BBSM_IN	Power supply for BBSM domain	1	mA
VDD_USB_1P8	1.8 V power supply for USB OTG PHYs	50	mA
VDD_USB_3P3	3.3 V power supply for USB OTG PHYs	60	mA
VDDA_ADC_1P8	1.8 V power supply for ADC, DAC, and ACMP	10	mA
VDDA_ADC_3P3	3.3 V power supply for ADC, DAC, and ACMP	2	mA
NVCC_SD1 NVCC_SD2 NVCC_EMC1 NVCC_EMC2 NVCC_GPIO1 NVCC_GPIO2 NVCC_GPIO_AD NVCC_AON NVCC_BBSM	Imax = N x C x V x (0.5 x F) Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F) In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.		

4.1.6 Typical power mode supply currents

Table 13 shows the current and power consumption (not including I/O) of i.MX RT1180 processors in selected power modes.

Table 13. Typical power modes current and power consumption (Dual core)

Modes	Test conditions	Power supplies at 3.3 V (Typical)[1]			Units
			25 °C Tj	105 °C Tj	
Over Drive Run — Dual Cores	• CM7 runs at 800 MHz, overdrive voltage to 1.1 V with FBB mode; CM33 runs at 240 MHz, overdrive voltage to 1.1 V • CM7 domain bus frequency at 240 MHz; CM33 domain bus frequency at 133 MHz • ECC with Cache, TCM, and OCRAM • DCDC, LDO_AON_ANA, and LDO_AON_DIG are turned on • 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled • All PLLs are enabled • All peripherals are enabled and run at their maximum clock root frequency under overdrive mode	DCDC_IN	137.8	172.1	mA
		VDD_AON_IN	30.7	31.1	mA
		VDD_BBSM_IN	4.9	9.7	µA
		Total	556.066	670.592	mW
Normal Drive Run — Dual Cores	• CM7 runs at 600 MHz, drive voltage to 1.0 V; CM33 runs at 240 MHz, drive voltage to 1.0 V • CM7 domain bus frequency at 200 MHz; CM33 domain bus frequency at 133 MHz • ECC with Cache, TCM, and OCRAM • DCDC, LDO_AON_ANA, and LDO_AON_DIG are turned on • 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled • All PLLs are enabled • All peripherals are enabled and run at their maximum clock root frequency under normal drive mode	DCDC_IN	96.6	110.7	mA
		VDD_AON_IN	32.6	33	mA
		VDD_BBSM_IN	4.7	9.4	µA
		Total	426.376	474.241	mW
Under Drive Run — Dual Cores	• CM7 runs at 360 MHz, lower voltage to 0.9 V; CM33 runs at 100 MHz, lower voltage to 0.9 V • CM7 domain bus frequency at 100 MHz; CM33 domain bus frequency at 50 MHz • ECC with Cache, TCM, and OCRAM • DCDC, LDO_AON_ANA, and LDO_AON_DIG are turned on • 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled • All PLLs are enabled • All peripherals are enabled and run at their maximum clock root frequency under underdrive mode	DCDC_IN	60.8	69.8	mA
		VDD_AON_IN	30.3	30.6	mA
		VDD_BBSM_IN	4.6	9.2	µA
		Total	300.645	331.350	mW

Table 13. Typical power modes current and power consumption (Dual core) (continued)

Modes	Test conditions	Power supplies at 3.3 V (Typical)[1]			Units
			25 °C Tj	105 °C Tj	
Normal Drive Run — Single Core	• CM7 is power off; CM33 runs at 240 MHz, drive voltage to 1.0 V • CM33 domain bus frequency at 133 MHz • ECC with Cache, TCM, and OCRAM • DCDC, LDO_AON_ANA, and LDO_AON_DIG are turned on • 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled • All PLLs are enabled • All peripherals are controlled by CM33 core run at their maximum clock root frequency under normal drive mode	DCDC_IN	74.8	83.6	mA
		VDD_AON_IN	32.6	33	mA
		VDD_BBSM_IN	4.4	9.4	µA
		Total	354.435	384.811	mW
Under Drive Run — Single Core	• CM7 is power off; CM33 runs at 100 MHz, lower voltage to 0.9 V • CM33 domain bus frequency at 50 MHz • ECC with Cache, TCM, and OCRAM • DCDC, LDO_AON_ANA, and LDO_AON_DIG are turned on • 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled • All PLLs are enabled • All peripherals are controlled by CM33 core run at their maximum clock root frequency under underdrive mode	DCDC_IN	50.7	56.5	mA
		VDD_AON_IN	30.3	30.6	mA
		VDD_BBSM_IN	4.6	9.3	µA
		Total	267.315	287.461	mW
Normal Drive Wait	• Both CM7 and CM33 are on WAIT mode, drive voltage to 1.0 V • CM7 domain bus frequency at 200 MHz, CM33 domain bus frequency at 133 MHz • ECC with TCM and OCRAM • DCDC, LDO_AON_ANA, and LDO_AON_DIG are turned on • 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled • All PLLs are enabled • All peripherals are enabled and run at their maximum clock root frequency under normal drive mode	DCDC_IN	76.1	88.9	mA
		VDD_AON_IN	32.6	33	mA
		VDD_BBSM_IN	4.6	9.5	µA
		Total	358.725	402.301	mW

Table 13. Typical power modes current and power consumption (Dual core) (continued)

Modes	Test conditions	Power supplies at 3.3 V (Typical)[1]			Units
			25 °C Tj	105 °C Tj	
System Sleep Stop	• System is on Sleep mode • Both CM7 and CM33 are on STOP mode, lower voltage to 0.8 V • TCM and OCRAM with ECC is on retention • DCDC, LDO_AON_ANA, and LDO_AON_DIG are turned on • All clock sources are turned off except for 32 kHz RTC • All PLLs are power gated • The MEGAMIX domain and NETCMIX domain are power gated • All peripherals in both AONMIX domain and WAKEUPMIX domain are clocked.	DCDC_IN	5.3	7	mA
		VDD_AON_IN	1.1	1.2	mA
		VDD_BBSM_IN	4.5	8.4	µA
		Total	21.135	27.088	mW
System Sleep Suspend	• System is on Sleep mode • CM7 is on SUSPEND mode and CM33 is on STOP mode, lower voltage to 0.8 V • TCM with ECC is on retention • DCDC, LDO_AON_ANA, and LDO_AON_DIG are turned on • All clock sources are turned off except 32 kHz RTC • All PLLs are power gated • The MEGAMIX domain and NETCMIX domain are power gated • All peripherals in both AONMIX domain and WAKEUPMIX domain are clock gated, but remain powered	DCDC_IN	0.372	2.6	mA
		VDD_AON_IN	222	351.7	µA
		VDD_BBSM_IN	4.2	8.4	µA
		Total	1.974	9.768	mW
Battery Mode	• Only BBSM domain is powered • 32 kHz RTC is alive • DCDC_IN and VDD_AON_IN are power gated	DCDC_IN	0	0	µA
		VDD_AON_IN	0	0	µA
		VDD_BBSM_IN	4.1	8.2	µA
		Total	13.53	27.06	µW

[1] Code runs in the ITCM; typical values are the average values on typical process wafers.

Table 14 shows the current and power consumption (Single core) of i.MX RT1180 processors in selected power modes.

Table 14. Typical power modes current and power consumption (Single core)

Modes	Test conditions	Power supplies at 3.3 V (Typical)[1]			Units
			25 °C Tj	105 °C Tj	
Normal Drive Run	• CM33 runs at 240 MHz, drive voltage to 1.0 V • CM33 domain bus frequency at 133 MHz • ECC with Cache, TCM, and OCRAM • DCDC, LDO_AON_ANA, and LDO_AON_DIG are turned on • 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled • All PLLs are enabled • All peripherals are enabled and run at their maximum clock root frequency under normal drive mode	DCDC_IN	72.1	82.8	mA
		VDD_AON_IN	29	29.8	mA
		VDD_BBSM_IN	4.2	9.3	µA
		Total	333.644	371.611	mW
Under Drive Run	• CM33 runs at 100 MHz, lower voltage to 0.9 V • CM33 domain bus frequency at 50 MHz • ECC with Cache, TCM, and OCRAM • DCDC, LDO_AON_ANA, and LDO_AON_DIG are turned on • 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled • All PLLs are enabled • All peripherals are enabled and run at their maximum clock root frequency under underdrive mode	DCDC_IN	45.2	52.7	mA
		VDD_AON_IN	29	29.7	mA
		VDD_BBSM_IN	4.1	9.3	µA
		Total	244.874	271.951	mW
Normal Drive Wait	• CM33 is on WAIT mode, drive voltage to 1.0 V • CM33 domain bus frequency at 133 MHz • ECC with TCM and OCRAM • DCDC, LDO_AON_ANA, and LDO_AON_DIG are turned on • 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled • All PLLs are enabled • All peripherals are enabled and run at their maximum clock root frequency under normal drive mode	DCDC_IN	68.9	78.6	mA
		VDD_AON_IN	29	29.8	mA
		VDD_BBSM_IN	4.1	9.3	µA
		Total	323.084	357.751	mW

Table 14. Typical power modes current and power consumption (Single core) (continued)

Modes	Test conditions	Power supplies at 3.3 V (Typical)[1]			Units
			25 °C Tj	105 °C Tj	
System Sleep Stop	• System is on Sleep mode • CM33 is on STOP mode, lower voltage to 0.8 V • TCM and OCRAM with ECC is on retention • DCDC, LDO_AON_ANA, and LDO_AON_DIG are turned on • All clock sources are turned off except 32 kHz RTC • All PLLs are power gated • The MEGAMIX domain and NETCMIX domain are power gated • All peripherals in both AONMIX domain and WAKEUPMIX domain are clock gated, but remain powered	DCDC_IN	0.329	2.6	mA
		VDD_AON_IN	211.1	351.2	µA
		VDD_BBSM_IN	4.1	8.7	µA
		Total	1.796	9.768	mW
Battery Mode	• Only BBSM domain is powered • 32 kHz RTC is alive • DCDC_IN and VDD_AON_IN are power gated	DCDC_IN	0	0	µA
		VDD_AON_IN	0	0	µA
		VDD_BBSM_IN	4.1	8.4	µA
		Total	13.53	27.72	µW

[1] Code runs in the ITCM; typical values are the average values on typical process wafers.

Table 15 lists the typical wakeup time.

Table 15. Typical wakeup time

Description	Typical wakeup time	Unit
From Battery Mode to ROM exit	34.64	ms
From System Sleep Suspend to Over Drive Run	13.29	ms
From System Sleep Stop to Over Drive Run	10.76	ms
From Normal Drive Wait to Normal Drive Run	6.2	µs

4.2 System power and clocks

This section provides the information about the system power and clocks.

4.2.1 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

Figure 5 shows the power sequence.

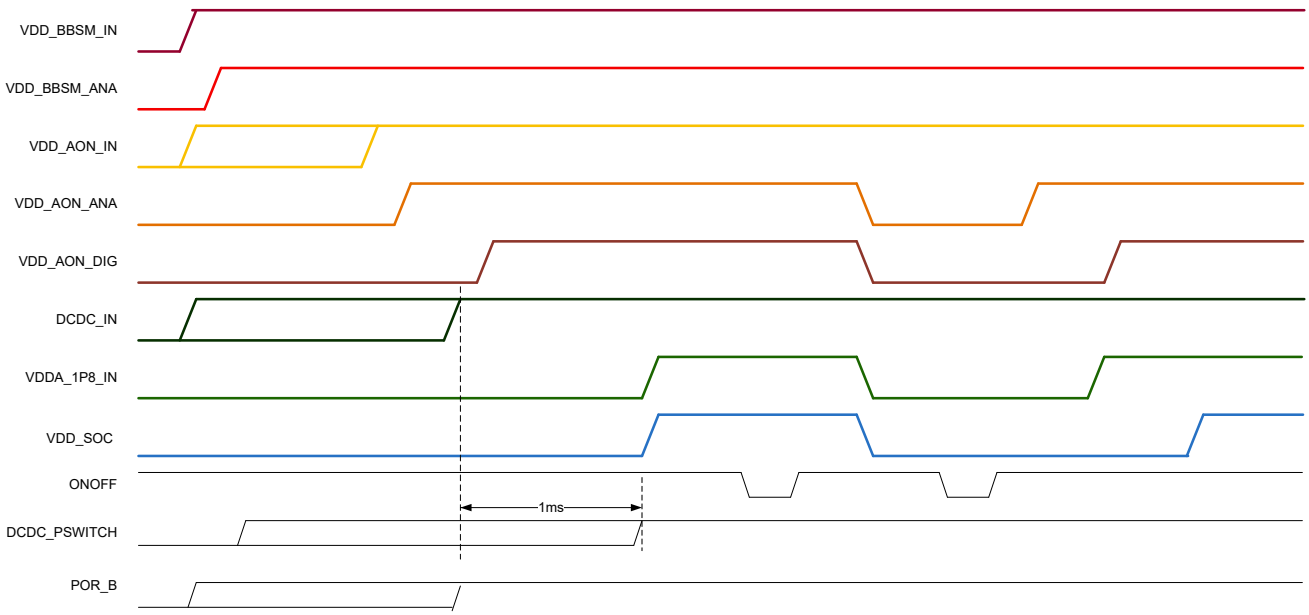


Figure 5. Power sequence

4.2.1.1 Power-up sequence

The below restrictions must be followed:

- VDD_BBSM_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_AON_IN and DCDC_IN supply.
- If a coin cell is used to power VDD_BBSM_IN, then ensure that it is connected before any other supply is switched on.
- An RC delay circuit is recommended for providing the delay between DCDC_IN stable and DCDC_PSWITCH. The total RC delay should be 5 – 40 ms.
- DCDC_IN must reach a minimum 3.0 V within 0.3 x RC.
- Delay from DCDC_IN stable at 3.0 V min to DCDC_PSWITCH reaching 0.5 x DCDC_IN (1.5 V) must be at least 1 ms.
- Power up slew rate specification for other power domains is 360 V/s – 36 KV/s.

NOTE

If expect to release MCU by POR_B signal, the POR_B input must be immediately asserted at power-up and remain asserted until the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX RT1180 Reference Manual* (IMXRT1180RM) for further details and to ensure that all necessary requirements are being met.

NOTE

The voltage on DCDC_PSWITCH pin should be below 0.5 V before ramping up the voltage on DCDC_PSWITCH.

NOTE

Ensure there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

Ensure VDDA_ADC_1P8 is powered prior to VDDA_ADC_3P3.

NOTE

USB1_VBUS, USB2_VBUS, and VDDA_ADC_3P3 are not part of the power supply sequence and may be powered at any time.

NOTE

Ensure VDD_AON_DIG is powered up prior to VDD_SOC_IN.

4.2.1.2 Power-down sequence

The following restrictions must be followed:

- VDD_BBSM_IN supply must be turned off after any other power supply, or be connected (shorted) with VDD_AON_IN and DCDC_IN supply.
- If a coin cell is used to power VDD_BBSM_IN, then ensure that it is removed after any other supply is switched off.

NOTE

Ensure VDD_AON_DIG is powered down after VDD_SOC_IN.

4.2.1.3 Power supplies usage

I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see "Power Rail" columns in pin list tables of Section 6, Package information and contact assignments."

4.2.2 Internal POR and power detect

Internal detector monitors VDD_SOC. Internal POR will be asserted whenever VDD_SOC is lower.

Table 16. Internal POR and power detect

Symbol	Description	Value	Unit
$V_{detsoc1p0\_H}$	1.0 V supply valid	0.75	V
$Hyst_{det1p0}$	The detector hysteresis	100	mV

4.2.3 Integrated LDO voltage regulator parameters

Various internal supplies can be powered from internal LDO voltage regulators. The on-chip LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX RT1180 Reference Manual* (IMXRT1180RM) for details on the power tree scheme.

4.2.3.1 LDO_BBSM_ANA

Table 17 shows the parameters of LDO_BBSM_ANA.

Table 17. LDO_BBSM_ANA specification

Specification	Min	Typ	Max	Unit
VDD_BBSM_IN	2.4	3	3.6	V
VDD_BBSM_ANA	1.65	1.75	1.95	V
I_out	—	—	1	mA
External decoupling capacitor	—	2.2	—	μF

4.2.3.2 LDO_PLL

Table 18 shows the parameters of LDO_PLL.

Table 18. LDO_PLL specification

Specification	Min	Typ	Max	Unit
VDDA_1P8_IN	1.71	1.8	1.89	V
VDDA_1P0	0.9	1	1.2	V
I_out	—	—	70	mA
External decoupling capacitor	—	2.2	—	μF

4.2.3.3 LDO_AON_DIG

LDO_AON_DIG provides 1.0 V power source from 1.8V power domain (VDD_AON_ANA). The trim voltage range of LDO output is from 0.7 V to 1.15 V. There are two work modes: Low Power mode and High Power mode. In typical PVT case, the static current consumption is less than 3 μA in Low Power mode. The maximum drive strength of this LDO regulator is 50 mA in High Power mode.

Table 19. LDO_AON_DIG specification

Specification	Min	Typ	Max	Unit
VDD_AON_ANA	1.71	1.8	1.89	V
VDD_AON_DIG	0.7	1	1.15	V
I_out: low power mode	—	—	1.5	mA
I_out: high power mode	—	—	50	mA
External decoupling capacitor	—	2.2	—	μF

4.2.3.4 LDO_AON_ANA

LDO_AON_ANA provides 1.8 V power source from 3.3 V power domain. Its default output value is 1.8 V, and can be trimmed with 50 mV step, but it is recommended to only use the default value 000 in real application. Two work modes are supported by this LDO: Low Power mode and High Power mode. In Low Power mode, the LDO provides 3 mA (maximum value) by consuming only 4 μA current. In High Power mode, the LDO provides 75 mA current capacity with 40 μA static power dissipation.

Table 20. LDO_AON_ANA specification

Specification	Min	Typ	Max	Unit
VDD_AON_IN	3	3.3	3.6	V
VDD_AON_ANA	—	1.8	—	V
I_out: low power mode	—	—	3	mA
I_out: high power mode	—	—	75	mA
External decoupling capacitor	—	4.7	—	μF

4.2.4 DCDC

DCDC can be configured to operate on power-save mode when the load current is less than 50 mA. During the power-save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

DCDC can detect the peak current in the P-channel switch. When the peak current exceeds the threshold, DCDC will give an alert signal, and the threshold can be configured. By this way, DCDC can roughly detect the current loading.

DCDC also includes the following protection functions:

- Over current protection. In run mode, DCDC shuts down when detecting abnormal large current in the P-type power switch.
- Over voltage protection. DCDC shuts down when detecting the output voltage is too high.
- Low voltage detection. DCDC shuts down when detecting the input voltage is too low.
- Low voltage warning. DCDC gives an alert signal, and triggers the interrupt if enabled when detecting the input voltage is lower than the threshold.

Table 21 shows DCDC characteristics.

Table 21. DCDC characteristics[1]

Description	Min	Typ	Max	Unit	Comments
Input voltage	3.0	3.3	3.6	V	—
Output voltage					
• 1.0 V output	0.6	1	1.375	V	25 mV one step
• 1.8 V output	1.5	1.8	2.275	V	25 mV one step
Loading					

Table 21. DCDC characteristics[1]

Description	Min	Typ	Max	Unit	Comments
• 1.0 V output	—	150	1000	mA	—
• 1.8 V output	—	100	150	mA	—
Efficiency					
• DCDC run mode	—	80%	—	—	150 mA@vdd1p0
• DCDC low power mode	—	80%	—	—	300 μA@vdd1p0
Output voltage accuracy[2]					
• DCDC Run mode	-2%	—	2%	—	—
• DCDC Low power mode	-6%	—	6%	—	—
Over current detection	—	2	—	A	—
Over voltage detection					
• Output 1.8 V	—	2.5	—	V	—
• Output 1.0 V	—	1.5	—	V	—
Low DCDC_IN detection	—	2.6	—	V	—
Low DCDC_IN warning	—	2.8	—	V	—
Leakage current	—	1	—	μA	DCDC off
Quiescent current					
• DCDC Run mode	—	375	—	μA	—
• DCDC Low power mode	—	80	—	μA	—
Capacitor value on 1.0 V output	—	33	—	μF	High frequency capacitor are also need in paralleled
Capacitor value on 1.8 V output	—	10	—	μF	15 μF can get better ripple
Inductor value	—	4.7	—	μH	—
• Saturation current	—	2	—	A	—

1 Values in this table are based on CZ test with limited matrix samples in lab environment.

2 Accuracy is only measured on bench with matrix samples under full operating ranges of voltage, loading, and temperature.

For additional information, see the *i.MX RT1180 Reference Manual* (IMXRT1180RM).

4.2.5 PLL's electrical characteristics

4.2.5.1 Audio PLL's electrical parameters

Table 22. Audio PLL's electrical parameters

Parameter	Min	Typ	Max	Unit
Clock output range[1]	650	—	786.43	MHz
Reference clock	—	24	—	MHz
Lock time	—	—	11250	reference cycles
Period jitter (p2p)	—	50	—	ps
Duty cycle	48.5	—	51.5	%

1 In UD mode, the maximum frequency of output clock cannot exceed 480 MHz.

4.2.5.2 528 MHz PLL (SYS_PLL2)

Table 23. 528 MHz PLL's electrical parameters

Parameter	Min	Typ	Max	Unit
Clock output range[1]	—	—	528	MHz
Reference clock	—	24	—	MHz
Lock time	—	—	11250	reference cycles
Period jitter (p2p)	—	50	—	ps
PFD period jitter (p2p)	—	100	—	ps
Duty cycle	45	—	55	%

1 In UD mode, the maximum frequency of output clock cannot exceed 480 MHz.

4.2.5.3 Ethernet PLL (SYS_PLL1)

Table 24. Ethernet PLL's electrical parameters

Parameter	Min	Typ	Max	Unit
Clock output range[1]	—	—	1000	MHz
Reference clock	—	24	—	MHz
Lock time	—	—	11250	reference cycles
Period jitter (p2p)	—	50	—	ps
Duty cycle	47.5	—	52.5	%

1 In UD mode, the maximum frequency of output clock cannot exceed 480 MHz.

4.2.5.4 480 MHz PLL (SYS_PLL3)

Table 25. 480 MHz PLL's electrical parameters

Parameter	Min	Typ	Max	Unit
Clock output range[1]	—	—	480	MHz
Reference clock	—	24	—	MHz
Lock time	—	—	383	reference cycles
Period jitter (p2p)	—	40	—	ps
PFD period jitter (p2p)	—	125	—	ps
Duty cycle	45	—	55	%

1 In UD mode, the maximum frequency of output clock cannot exceed 480 MHz.

4.2.5.5 Arm PLL

Table 26. Arm PLL's electrical parameters

Parameter	Min	Typ	Max	Unit
Clock output range[1]	156	—	798	MHz
Reference clock	—	24	—	MHz
Lock time	—	—	2250	reference cycles
Period jitter (p2p)	—	15	—	ps
Duty cycle	45	—	55	%

1 In UD mode, the maximum frequency of output clock cannot exceed 480 MHz.

4.2.6 On-chip oscillators

Each i.MX RT1180 processor has two external input clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, real time clock operation, and slow system and watchdog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the clock source from RTC_XTALI. The internal ring oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP recommends using an external crystal as the clock source for RTC_XTALI. If the internal clock oscillator is used instead, careful consideration should be given to the timing implications on all of the SoC modules dependent on this clock.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

The RTC OSC module provides the clock source for the Real-Time Clock module. The RTC OSC module, in conjunction with an external crystal, generates a 32.768 kHz reference clock for the RTC.

The system oscillator (SYS OSC) is a crystal oscillator. The SYS OSC, in conjunction with an external crystal or resonator, generates a reference clock for this chip.

Table 27. 24 MHz system oscillator specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VDDA} (Low power mode)	Analog supply current	24 MHz	—	0.5	—	mA
I_{VDDA} (High gain mode)	Analog supply current	24 MHz	—	1.3	—	mA
R_F	Feedback resistor	Low-power mode	No need			
		High-gain mode	—	1	—	MΩ
R_S	Series resistor[1]	—	—	0	—	kΩ
C_XC_Y	XTALI/XTALO load capacitance	See crystal or resonator manufacture's recommendation				
C_{para}	Parasitically capacitance of XTALI and XTALO	—	—	1.5	2.0	pF
Clock output						
F_{OSC}	Oscillator crystal or resonator frequency	—	—	24	—	MHz
t_{dcy}	Duty-cycle of the output clock	—	40	50	60	%
Dynamic parameters						
V_{PP}	Peak-peak amplitude of oscillation	Low-power mode	—	0.8	—	V
		High gain mode	0.75 x VDD_AON_ANA	0.8 x VDD_AON_ANA	—	V
t_{start}	Start-up time from OSC_24M_CNTL[OSC_EN] set to oscillator stable[2]	24 MHz low-power mode	—	250	—	µs
		24 MHz high-gain mode	—	250	—	µs

1 Depends on the drive level of external crystal device

2 Oscillator hardware default is OFF at power-up, so requires firmware or software to enable.

Table 28. 32 kHz oscillator specifications

Symbol	Description	Min	Typ	Max	Unit	Note
C_{para}	Parasitically capacitance of RTC_XTALI and RTC_XTALO	—	1.5	2.0	pF	—
V_{pp}	Peak-to-peak amplitude of oscillator	—	0.6	—	V	1
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	—

Table 28. 32 kHz oscillator specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Note
t_{start}	Crystal startup time from VDD_BBSM_ANA ramp-up to minimum operating voltage to oscillator stable	—	500	—	ms	1
$V_{ec\_extal32}$	Externally provided input clock amplitude	0.7	—	VDD_BBSM_ANA	V	2,3

1 Proper PCB layout procedures must be followed to achieve specifications.

2 This specification is for an externally supplied clock driven to RTC_XTALI and does not apply to any other clock input. The oscillator remains enabled and RTC_XTALO must be left unconnected.

3 The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to VDD_BBSM_ANA.

Table 29. RC oscillator with 24 MHz internal reference frequency

Symbol	Parameter	Condition	Min	Typ	Max	Unit
General						
I_{VDDA}	Analog supply current	—	—	350	500	µA
Clock output						
F_{clkout}	Clock frequency	—	—	24	—	MHz
Dynamic parameters						
T_{start}	Start-up time from VDD_AON_ANA ramp-up to minimum operating voltage to oscillator stable	—	—	2.5	—	µs
Accuracy						
T_{target}	Trimmed	—	-2	—	2	%

Table 30. RC oscillator with 400 MHz internal reference frequency

Symbol	Parameter	Condition	Min	Typ	Max	Unit
General						
$I_{VDD\_1P8V\_ON}$	Analog supply current	—	—	60	—	µA
I_{VDD_ON}	Digital supply current	—	—	80	—	µA
Clock output						
F_tuned	Tuned clock frequency	—	—	400	—	MHz
ΔF/F	Frequency error after tuning	—	—	0.1	—	%
Dynamic parameters						
J_{PP-CC}	Peak-peak, period jitter	—	—	50	—	ps

Table 30. RC oscillator with 400 MHz internal reference frequency (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{start}	Start-up time from OSC_400M_CTRL1[PWD] is cleared to oscillator stable[1]	—	—	1	—	µs
t_{tune}	Tuning time	—	1	—	256	µs

1 Oscillator hardware default is OFF at power-up, so requires firmware or software to enable.

Table 31. RC oscillator with 32 kHz internal reference frequency

Symbol	Description	Min	Typ	Max	Unit	Note
f_{irc32k}	Internal reference frequency	—	32	—	kHz	—
Δf_{irc32k}	Deviation of IRC32K frequency	-25%	—	25%	f_{irc32k}	—

4.3 I/O parameters

This section provides parameters on I/O interfaces.

4.3.1 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- XTALI and RTC_XTALI (Clock Inputs) DC Parameters
- General Purpose I/O (GPIO)

NOTE

The term ‘NVCC_XXXX’ in this section refers to the associated supply rail of an input or output.

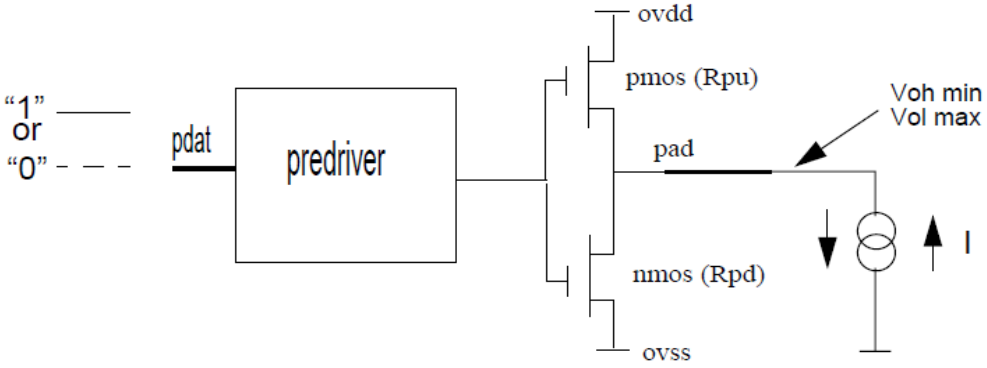


Figure 6. Circuit for parameters Voh and Vol for I/O cells

4.3.1.1 XTALI and RTC_XTALI (clock inputs) DC parameters

Table 32 shows the DC parameters for the clock inputs.

Table 32. XTALI and RTC_XTALI DC parameters[1]

Parameter	Symbol	Test Conditions	Min	Max	Unit
XTALI high-level DC input voltage	Vih	—	VDD_AON_ANA - 0.5	VDD_AON_ANA	V
XTALI low-level DC input voltage	Vil	—	0	0.5	V
RTC_XTALI high-level DC input voltage	Vih	—	VDD_BBSM_ANA - 0.5	VDD_BBSM_ANA	V
RTC_XTALI low-level DC input voltage	Vil	—	0	0.5	V

1 The DC parameters are for external clock input only.

4.3.1.2 General purpose I/O (GPIO) DC parameters

Following section introduces the GPIO DC parameters, respectively, for GPIO pads. These parameters are guaranteed per the operating ranges in Table 11 unless otherwise noted.

Table 33. DC specification for GPIO_EMC_B1/GPIO_EMC_B2/GPIO_B1/GPIO_B2/GPIO_SD1/GPIO_SD2 bank

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Receiver 3.3 V						
High level input voltage	V_{IH}	0.625 x NVCC	—	NVCC + 0.3	V	—
Low level input voltage	V_{IL}	-0.3	—	0.25 x NVCC	V	—
Receiver 1.8 V						
High level input voltage	V_{IH}	0.65 x NVCC	—	NVCC + 0.3	V	—
Low level input voltage	V_{IL}	-0.3	—	0.35 x NVCC	V	—
Driver 3.3 V and driver 1.8 V for PDRV = L and PDRV = H						
Output high current	I_{OH}	-6	—	—	mA	V_{OH} = 0.8 x NVCC
Output low current	I_{OL}	6	—	—	mA	V_{OL} = 0.2 x NVCC
Output low/high current total for each IO bank	I_{OCT}	—	—	100	mA	—
Weak pull-up and pull-down						
Pull-up / pull-down resistance	R_{High}	10	—	100	kΩ	High voltage range (2.7 V - 3.6 V)
Pull-up / pull-down resistance	R_{Low}	20	—	50	kΩ	Low voltage range (1.65 V - 1.95 V)

Table 34. DC specifications for GPIO_AD/GPIO_AON bank

NO.	Characteristics	Test Conditions	Min	Max	Units
1	High-level input voltage (V_{IH})	All voltage range	0.75 x NVCC	NVCC	V
2	Low-level input voltage (V_{IL})	All voltage range	0	0.3 x NVCC	V
3	Input Hysteresis (VHYSN)	All voltage range	0.06 x NVCC	—	V
4	Output high voltage (V_{OH}) DSE = 1	Normal voltage range I_{OH} = -10 mA	NVCC - 0.5	—	V
		Derated voltage range I_{OH} = -6 mA	NVCC - 0.5	—	V
		Derated2 voltage range I_{OH} = -5 mA	NVCC - 0.5	—	V
		Low voltage range I_{OH} = -10 mA	NVCC - 0.5	—	V
		High voltage range I_{OH} = -10 mA	NVCC - 0.5	—	V
5	Output high voltage (V_{OH}) DSE = 0	Normal voltage range I_{OH} = -5 mA	NVCC - 0.5	—	V
		Derated voltage range I_{OH} = -3 mA	NVCC - 0.5	—	V
		Derated2 voltage range I_{OH} = -2.5 mA	NVCC - 0.5	—	V
		Low voltage range I_{OH} = -5 mA	NVCC - 0.5	—	V
		High voltage range I_{OH} = -5 mA	NVCC - 0.5	—	V
6	Output low voltage (V_{OL}) DSE = 1	Normal voltage range I_{OL} = 10 mA	—	0.5	V
		Derated voltage range I_{OL} = 6 mA	—	0.5	V
		Derated2 voltage range I_{OL} = 5 mA	—	0.5	V
		Low voltage range I_{OL} = 10 mA	—	0.5	V
		High voltage range I_{OL} = 10 mA	—	0.5	V

Table 34. DC specifications for GPIO_AD/GPIO_AON bank (continued)

NO.	Characteristics	Test Conditions	Min	Max	Units
7	Output low voltage (V_{OL}) DSE = 0	Normal voltage range I_{OL} = 5 mA	—	0.5	V
		Derated voltage range I_{OL} = 3 mA	—	0.5	V
		Derated2 voltage range I_{OL} = 2.5 mA	—	0.5	V
		Low voltage range I_{OL} = 5 mA	—	0.5	V
		High voltage range I_{OL} = 5 mA	—	0.5	V
8	NVCC	Normal voltage range	2.7	3.6	V
		Derated voltage range	1.98	2.7	V
		Derated2 voltage range	1.71	1.98	V
		Low voltage range	1.71	1.98	V
		High voltage range	3	3.6	V
11	Pull-up resistor range (R_{PU}) Measure @V_{DD}	All voltage range	25	50	kΩ
12	Pull-down resistor range (R_{PD}) Measure @V_{SS}	All voltage range	25	50	kΩ
13	Input leakage current	All voltage range	—	1	μA
14	Output capacitance (CL)	All voltage range	—	15	pF
15	Input capacitance (Cin)	All voltage range	—	5	pF
16	Output low/high current total for each IO bank (I_{OCT})	All voltage range	—	100	mA

Table 35. Additional leakage parameters

Parameter	Symbol	Pins	Min	Max	Unit
High level input current	IIH	GPIO_AON_15		1	μA
		GPIO_AON_20		1	
		GPIO_AD_19		1	
		GPIO_AD_35		1	

4.3.2 I/O AC parameters

The GPIO and DDR I/O load circuit and output transition time waveform are shown in Figure 7 and Figure 8.

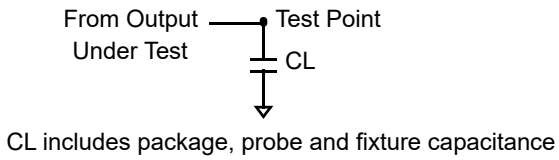


Figure 7. Load circuit for output

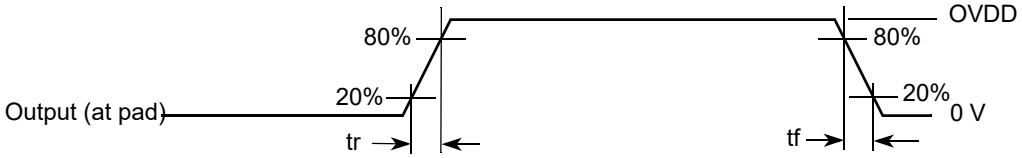


Figure 8. Output transition time waveform

4.3.2.1 General purpose I/O (GPIO) AC parameters

The I/O AC parameters for GPIO are presented in the Table 36, Table 37, and Table 38 respectively.

Table 36. AC specification for GPIO_EMC_B1/GPIO_EMC_B2/GPIO_B1/GPIO_B2/GPIO_SD1/GPIO_SD2 bank

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Driver 1.8 V application						
f_{max}	Maximum frequency	Load = 21 pF (PDRV = L, high drive, 33 Ω)	—	—	208	MHz
		Load = 15 pF (PDRV = H, low drive, 50 Ω)				
tr	Rise time	Measured between V_{OL} and V_{OH}	0.4	—	1.32	ns
tf	Fall time	Measured between V_{OH} and V_{OL}	0.4	—	1.32	ns
Driver 3.3 V application						
f_{max}	Maximum frequency	Load = 20 pF	—	—	200	MHz
tr	Rise time	Measured between V_{OL} and V_{OH}	—	—	3	ns
tf	Fall time	Measured between V_{OH} and V_{OL}	—	—	3	ns

Table 37. Dynamic input characteristics for GPIO_EMC_B1/GPIO_EMC_B2/GPIO_B1/GPIO_B2/GPIO_SD1/GPIO_SD2

Symbol	Parameter	Test Condition[1, 2]	Min	Max	Unit
Dynamic Input Characteristics for 3.3 V Application					
f_{op}	Input frequency of operation	—	—	200	MHz
Dynamic Input Characteristics for 1.8 V Application					
f_{op}	Input frequency of operation	—	—	208	MHz

1 For all supply ranges of operation.

[2] The dynamic input characteristic specifications are applicable for the digital bidirectional cells.

Table 38. AC specifications for GPIO_AD/GPIO_AON bank

NO.	Characteristic	Condition		Max	Unit
1	f_{max}	Cload = 15 pF	—	104	MHz
2	Pad rise/fall time (DSE = 0, SRE = 0)	Normal voltage range (Cload = 15 pF)	—	3	ns
		Derated voltage range (Cload = 15 pF)	—	5	ns
		Derated2 voltage range (Cload = 15 pF)	—	6	ns
		Low voltage range (Cload = 15 pF)	—	3	ns
		High voltage range (Cload = 15 pF)	—	3	ns
3	Pad rise/fall time (DSE = 0, SRE = 1)	Normal voltage range (Cload = 15 pF)	—	6	ns
		Derated voltage range (Cload = 15 pF)	—	10	ns
		Derated2 voltage range (Cload = 15 pF)	—	12	ns
		Low voltage range (Cload = 15 pF)	—	6	ns
		High voltage range (Cload = 15 pF)	—	6	ns
4	Pad rise/fall time (DSE = 1, SRE = 0)	Normal voltage range (Cload = 15 pF)	—	2.5	ns
		Derated voltage range (Cload = 15 pF)	—	4.5	ns
		Derated2 voltage range (Cload = 15 pF)	—	5	ns
		Low voltage range (Cload = 15 pF)	—	2.5	ns
		High voltage range (Cload = 15 pF)	—	2.5	ns

Table 38. AC specifications for GPIO_AD/GPIO_AON bank (continued)

NO.	Characteristic	Condition		Max	Unit
5	Pad rise/fall time (DSE = 1, SRE = 1)	Normal voltage range (Cload = 15 pF)	—	5	ns
		Derated voltage range (Cload = 15 pF)	—	9	ns
		Derated2 voltage range (Cload = 15 pF)	—	10	ns
		Low voltage range (Cload = 15 pF)	—	5	ns
		High voltage range (Cload = 15 pF)	—	5	ns
6	IPP_DO to pad propagation delay: (DSE = 0, SRE = 0)	Normal voltage range (Cload = 15 pF)	—	2.5	ns
		Derated voltage range (Cload = 15 pF)	—	4.5	ns
		Derated2 voltage range (Cload = 15 pF)	—	5	ns
		Low voltage range (Cload = 15 pF)	—	2.5	ns
		High voltage range (Cload = 15 pF)	—	4	ns
7	IPP_DO to pad propagation delay: (DSE = 0, SRE = 1)	Normal voltage range (Cload = 15 pF)	—	7	ns
		Derated voltage range (Cload = 15 pF)	—	12	ns
		Derated2 voltage range (Cload = 15 pF)	—	14	ns
		Low voltage range (Cload = 15 pF)	—	7	ns
		High voltage range (Cload = 15 pF)	—	8.5	ns
8	IPP_DO to pad propagation delay: (DSE = 1, SRE = 0)	Normal voltage range (Cload = 15 pF)	—	2	ns
		Derated voltage range (Cload = 15 pF)	—	3.6	ns
		Derated2 voltage range (Cload = 15 pF)	—	4	ns
		Low voltage range (Cload = 15 pF)	—	2	ns
		High voltage range (Cload = 15 pF)	—	4	ns

Table 38. AC specifications for GPIO_AD/GPIO_AON bank (continued)

NO.	Characteristic	Condition		Max	Unit
9	IPP_DO to pad propagation delay: (DSE = 1, SRE = 1)	Normal voltage range (Cload = 15 pF)	—	6	ns
		Derated voltage range (Cload = 15 pF)	—	11	ns
		Derated2 voltage range (Cload = 15 pF)	—	12	ns
		Low voltage range (Cload = 15 pF)	—	6	ns
		High voltage range (Cload = 15 pF)	—	7.5	ns

Figure 9 is the GPIO block diagram.

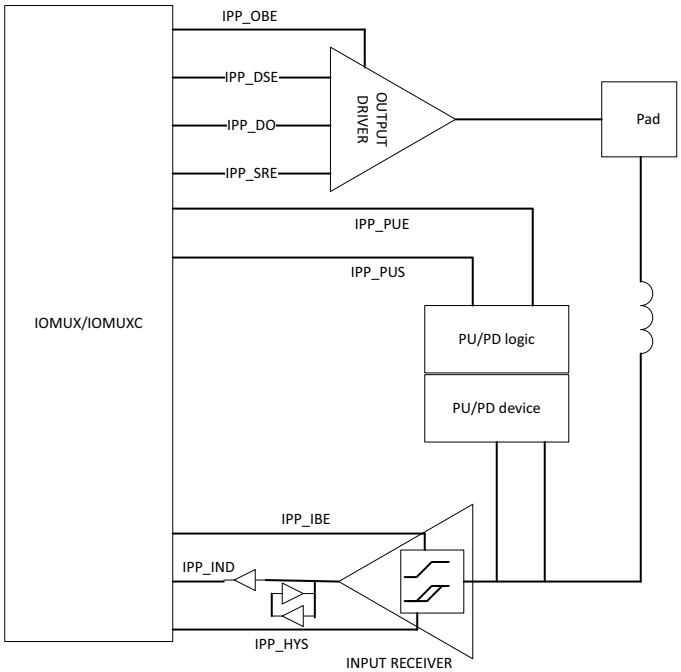


Figure 9. GPIO block diagram

4.4 System modules

This section contains the timing and electrical parameters for the modules in the i.MX RT1180 processor.

4.4.1 Reset timings parameters

Figure 10 shows the reset timing and Table 39 lists the timing parameters.

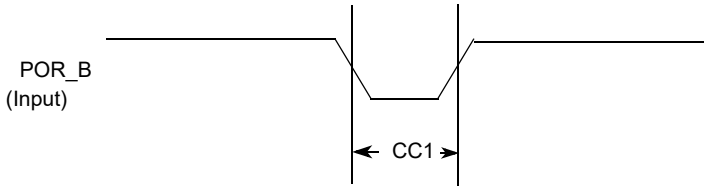


Figure 10. Reset timing diagram

Table 39. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	RTC_XTALI cycle

4.4.2 JTAG Controller timing parameters

Figure 11 depicts the JTAG controller timing. Figure 12 depicts the JTAG TRST_B timing.

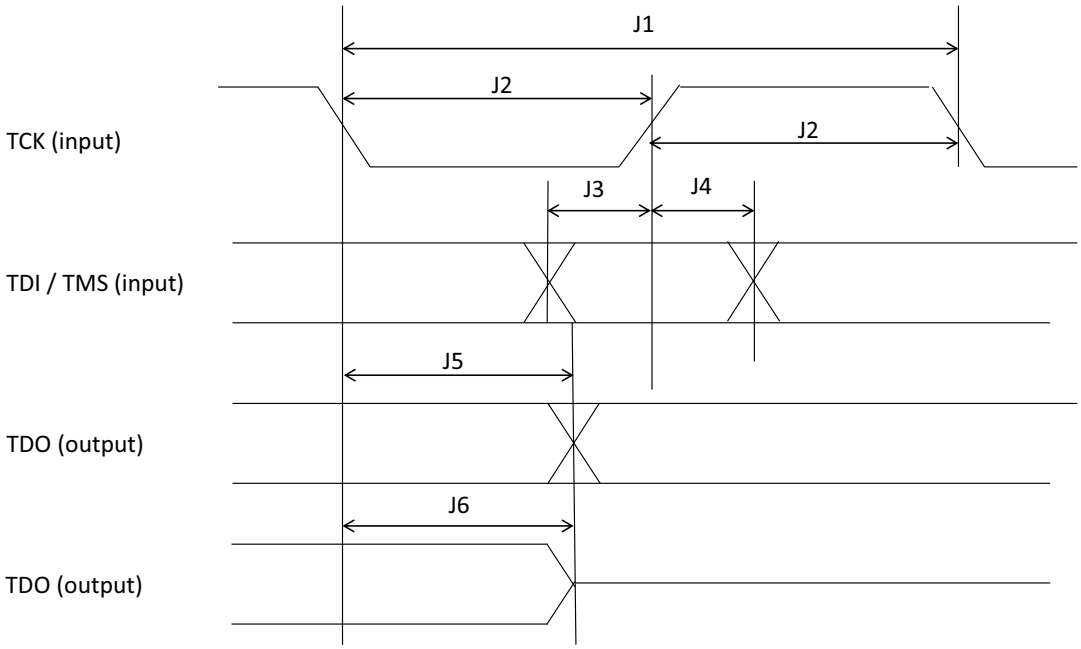


Figure 11. JTAG controller timing

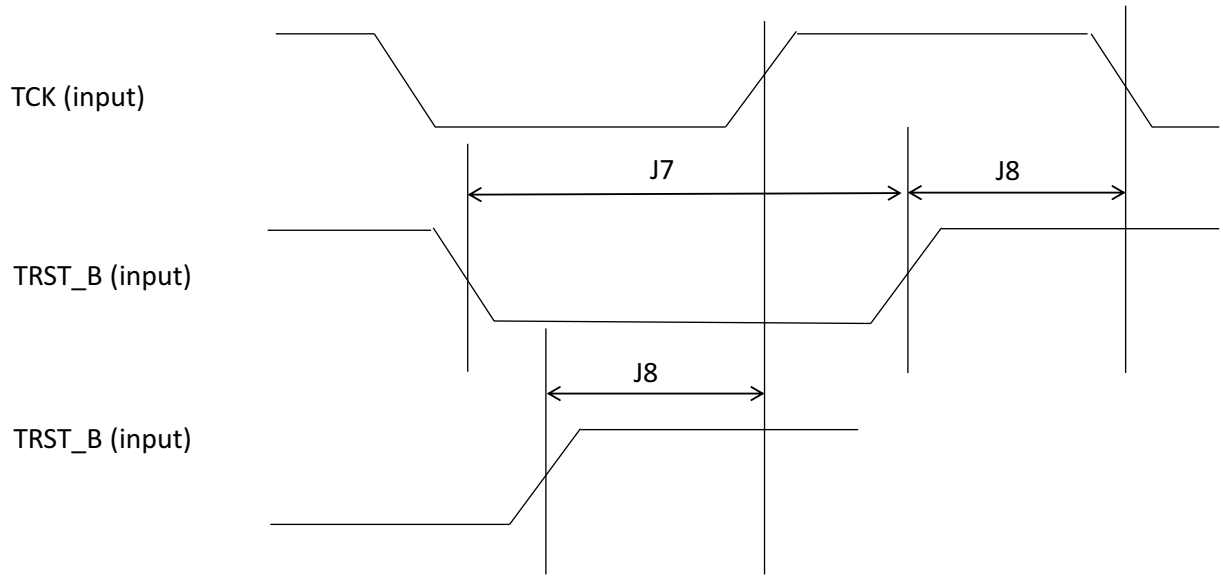


Figure 12. JTAG_TRST_B timing

Table 40. JTAG timing parameters

ID	Parameter	Value		Unit
		Min	Max	
J0	TCK frequency	—	25	MHz
J1	TCK cycle time	40	—	ns
J2	TCK pulse width	20	—	ns
J3	Input data setup time	5	—	ns
J4	Input data hold time	5	—	ns
J5	Output data valid time	—	15.2	ns
J6	Output high impedance time	—	15.2	ns
J7	TRST_B assert time	100	—	ns
J8	TRST_B setup time to TCK edge	18	—	ns

4.4.3 SWD timing parameters

Figure 13 depicts the SWD timing.

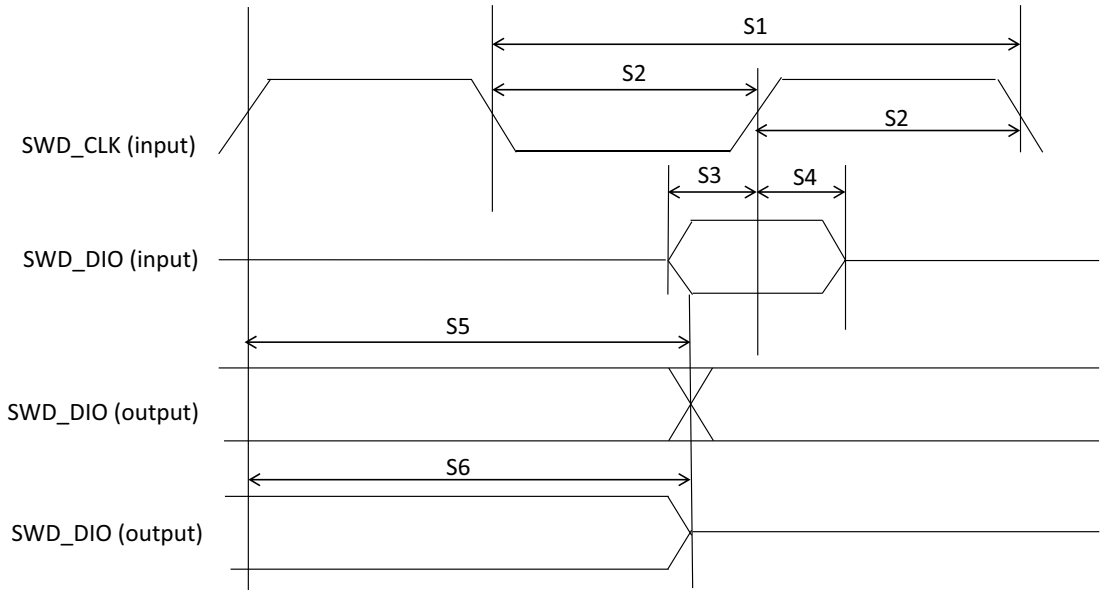


Figure 13. SWD timing

Table 41 shows SWD timing parameters.

Table 41. SWD timing parameters

Symbol	Description	Min	Max	Unit
S0	SWD_CLK frequency	—	50	MHz
S1	SWD_CLK cycle time	20	—	ns
S2	SWD_CLK pulse width	10	—	ns
S3	Input data setup time	5	—	ns
S4	Input data hold time	1	—	ns
S5	Output data valid time	—	14.4	ns
S6	Output high impedance time	—	14.4	ns

4.5 External memory interface

The following sections provide information about external memory interfaces.

4.5.1 SEMC specifications

The following sections provide information on SEMC interface.

Measurements are with a load of 15 pf and an input slew rate of 1 V/ns.

4.5.1.1 SEMC output timing

There are ASYNC and SYNC modes for SEMC output timing.

4.5.1.1.1 SEMC output timing in ASYNC mode

Table 42 shows SEMC output timing in ASYNC mode.

Table 42. SEMC output timing in ASYNC mode

Symbol	Parameter	Min.	Max.	Unit	Comment
	Frequency of operation	—	200	MHz	
T_{CK}	Internal clock period	5	—	ns	
T_{AVO}	Address output valid time	—	2	ns	These timing parameters apply to Address and ADV# for NOR/PSRAM in ASYNC mode.
T_{AHO}	Address output hold time	(TCK - 2) [1]	—	ns	
T_{ADVL}	Active low time	(TCK - 1) [2]			
T_{DVO}	Data output valid time	—	2	ns	These timing parameters apply to Data/CLE/ALE and WE# for NAND, apply to Data/DM/CRE for NOR/PSRAM, apply to Data/DCX and WRX for DBI interface.
T_{DHO}	Data output hold time	(TCK - 2) [3]	—	ns	
T_{WEL}	WE# low time	(TCK - 1) [4]		ns	

1 Address output hold time is configurable by SEMC_*CR0.AH. AH field setting value is 0x0 in above table. When AH is set with value N, T_{AHO} min time should be ((N + 1) x T_{CK}). See the *i.MX RT1180 Reference Manual* (IMXRT1180RM) for more detail about SEMC_*CR0.AH register field.

2 ADV# low time is configurable by SEMC_*CR0.AS. AS field setting value is 0x0 in above table. When AS is set with value N, T_{ADL} min time should be ((N + 1) x T_{CK} - 1). See the *i.MX RT1180 Reference Manual* (IMXRT1180RM) for more detail about SEMC_*CR0.AS register field.

3 Data output hold time is configurable by SEMC_*CR0.WEH. WEH field setting value is 0x0 in above table. When WEH is set with value N, T_{DHO} min time should be ((N + 1) x T_{CK}). See the *i.MX RT1180 Reference Manual* (IMXRT1180RM) for more detail about SEMC_*CR0.WEH register field.

4 WE# low time is configurable by SEMC_*CR0.WEL. WEL field setting value is 0x0 in above table. When WEL is set with value N, T_{WEL} min time should be ((N + 1) x T_{CK} - 1). See the *i.MX RT1180 Reference Manual* (IMXRT1180RM) for more detail about SEMC_*CR0.WEL register field.

Figure 14 shows the output timing in ASYNC mode.

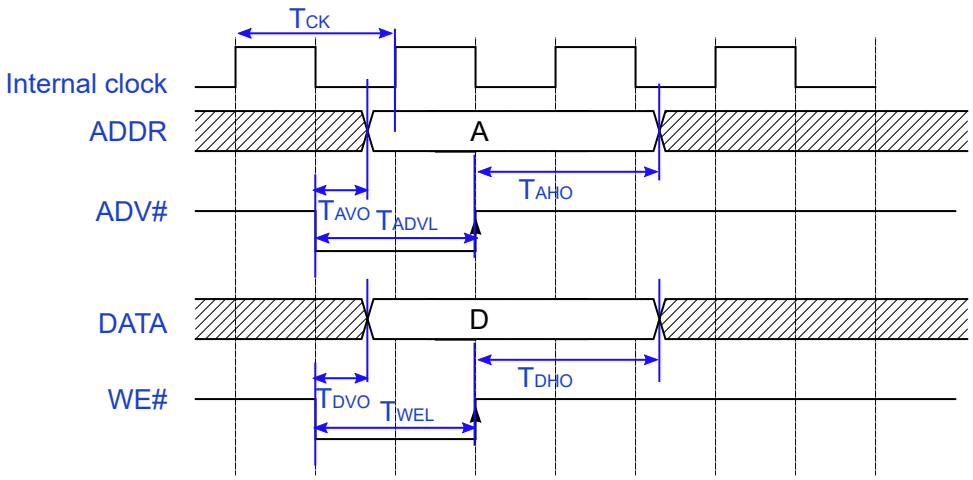


Figure 14. SEMC output timing in ASYNC mode

4.5.1.1.2 SEMC output timing in SYNC mode

Table 43 shows SEMC output timing in SYNC mode.

Table 43. SEMC output timing in SYNC mode

Symbol	Parameter	Min.	Max.	Unit	Comment
	Frequency of operation	—	200	MHz	—
T_{CK}	Internal clock period	5	—	ns	—
T_{DVO}	Data output valid time	—	0.6	ns	These timing parameters apply to Address/Data/DM/CKE/control signals with SEMC_CLK for SDRAM.
T_{DHO}	Data output hold time	-0.7	—	ns	

Figure 15 shows the output timing in SYNC mode.

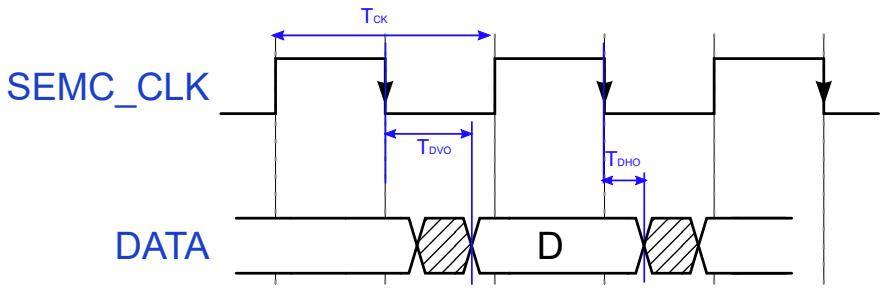


Figure 15. SEMC output timing in SYNC mode

4.5.1.2 SEMC input timing

There are ASYNC and SYNC modes for SEMC input timing.

4.5.1.2.1 SEMC input timing in ASYNC mode

Table 44 shows SEMC input timing in ASYNC mode.

Table 44. SEMC input timing in ASYNC mode

Symbol	Parameter	Min.	Max.	Unit	Comment
T_{IS}	Data input setup	7.1	—	ns	For NAND/NOR/PSRAM/DBI, these timing parameters apply to RE# and Read Data.
T_{IH}	Data input hold	0	—	ns	

Figure 16 shows the input timing in ASYNC mode.

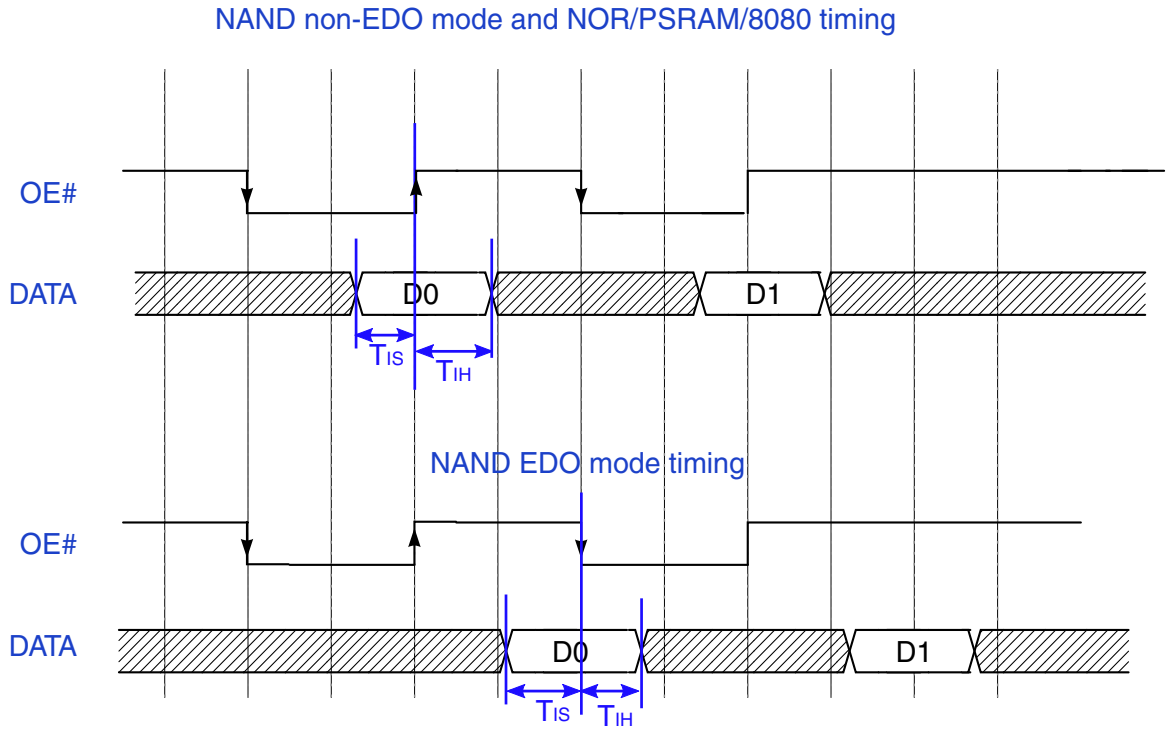


Figure 16. SEMC input timing in ASYNC mode

4.5.1.2.2 SEMC input timing in SYNC mode

Table 45 and Table 46 show SEMC input timing in SYNC mode.

Table 45. SEMC input timing in SYNC mode (SEMC_MCR.DQSMD = 0x0)

Symbol	Parameter	Min.	Max.	Unit	Comment
T_{IS}	Data input setup	8.67	—	ns	—
T_{IH}	Data input hold	0	—	ns	

Table 46. SEMC input timing in SYNC mode (SEMC_MCR.DQSMD = 0x1)

Symbol	Parameter	Min.	Max.	Unit	Comment
T_{IS}	Data input setup	0.6	—	ns	—
T_{IH}	Data input hold	1	—	ns	

Figure 17 shows the input timing in SYNC mode.

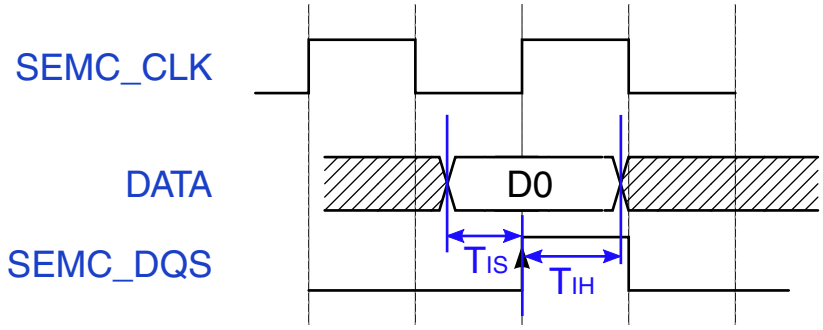


Figure 17. SEMC input timing in SYNC mode

4.5.2 SRAMC parameters

The following sections provide information on SRAMC interface.

Measurements are with a load of 15 pf and an input slew rate of 1 V/ns.

4.5.2.1 SRAMC output timing

There is ASYNC mode for SRAMC output timing.

4.5.2.1.1 SRAMC output timing in ASYNC mode

Table 42 shows SRAMC output timing in ASYNC mode.

Table 47. SRAMC output timing in ASYNC mode

Symbol	Parameter	Min.	Max.	Unit	Comment
	Frequency of operation	—	133	MHz	
T_{CK}	Internal clock period	7.5	—	ns	

Table 47. SRAMC output timing in ASYNC mode (continued)

Symbol	Parameter	Min.	Max.	Unit	Comment
T_{AVO}	Address output valid time	—	2	ns	These timing parameters apply to Address and ADV# for SRAM in ASYNC mode.
T_{AHO}	Address output hold time	(TCK - 2) [1]	—	ns	
T_{ADVL}	Active low time	(TCK - 1) [2]			
T_{DVO}	Data output valid time	—	2	ns	These timing parameters apply to Data and DM for SRAM interface.
T_{DHO}	Data output hold time	(TCK - 2) [3]	—	ns	
T_{WEL}	WE# low time	(TCK - 1) [4]		ns	

1 Address output hold time is configurable by BLK_CTRL_WAKEUPMIX register's SRAMCR0[AH]. AH field setting value is 0x0 in above table. When AH is set with value N, T_{AHO} min time should be ((N + 1) x T_{CK} - 2). See the *i.MX RT1180 Reference Manual* (IMXRT1180RM) for more detail about SRAMCR0[AH] register field.

2 ADV# low time is configurable by BLK_CTRL_WAKEUPMIX register's SRAMCR0[AS]. AS field setting value is 0x1 in above table. When AS is set with value N, T_{ADVL} min time should be ((N + 1) x T_{CK} - 1). See the *i.MX RT1180 Reference Manual* (IMXRT1180RM) for more detail about SRAMCR0[AS] register field.

3 Data output hold time is configurable by BLK_CTRL_WAKEUPMIX register's SRAMCR1[WEH]. WEH field setting value is 0x0 in above table. When WEH is set with value N, T_{DHO} min time should be ((N + 1) x T_{CK} - 2). See the *i.MX RT1180 Reference Manual* (IMXRT1180RM) for more detail about SRAMCR1[WEH] register field.

4 WE# low time is configurable by BLK_CTRL_WAKEUPMIX register's SRAMCR1[WEL]. WEL field setting value is 0x0 in above table. When WEL is set with value N, T_{WEL} min time should be ((N + 1) x T_{CK} - 1). See the *i.MX RT1180 Reference Manual* (IMXRT1180RM) for more detail about SRAMCR1[WEL] register field.

Figure 14 shows the output timing in ASYNC mode.

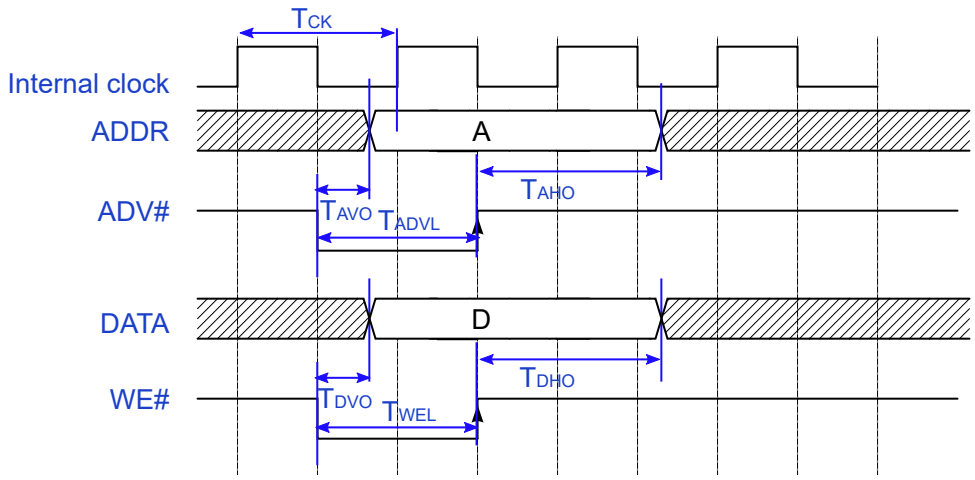


Figure 18. SRAMC output timing in ASYNC mode

4.5.2.2 SRAMC input timing

There is ASYNC mode for SRAMC input timing.

4.5.2.2.1 SRAMC input timing in ASYNC mode

Table 48 shows SRAMC input timing in ASYNC mode.

Table 48. SRAMC input timing in ASYNC mode

Symbol	Parameter	Min.	Max.	Unit	Comment
T_{IS}	Data input setup	7.1	—	ns	For SRAM, these timing parameters apply to RE# and Read Data.
T_{IH}	Data input hold	0	—	ns	

Figure 16 shows the input timing in ASYNC mode.

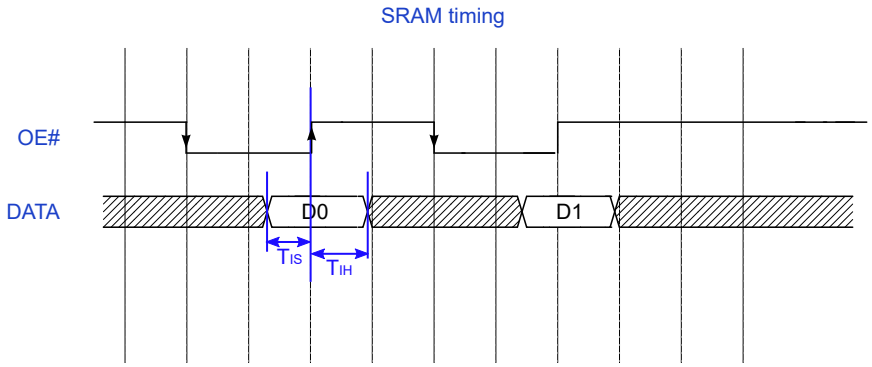


Figure 19. SRAMC input timing in ASYNC mode

4.5.3 FlexSPI parameters

Measurements are with a load 15 pf and input slew rate of 1 V/ns.

FlexSPI1 pin multiplex options performance specifications:

1. GPIO_B1_XX and GPIO_B2_XX support the maximum 200 MHz operation frequency;
2. GPIO_SD_B2_XX only supports the maximum 166 MHz operation frequency.

FlexSPI2 pin multiplex options performance specifications:

1. GPIO_EMC_B1_XX supports the maximum 166 MHz operation frequency;
2. GPIO_AON_XX only supports the maximum 104 MHz operation frequency.

4.5.3.1 FlexSPI input/read timing

There are three sources for the internal sample clock for FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPI*n*_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x1)

- Read strobe provided by memory device and input from DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x3)

The following sections describe input signal timing for each of these three internal sample clock sources.

4.5.3.1.1 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1

Table 49. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X0

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	60	MHz
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time for incoming data	0	—	ns

Table 50. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X1

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	133	MHz
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time for incoming data	1	—	ns

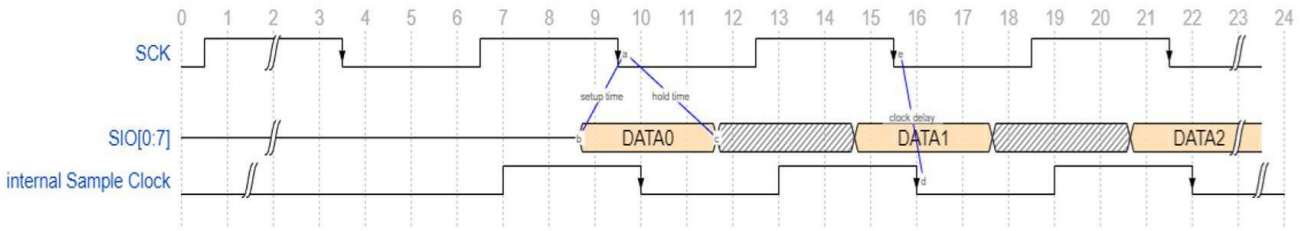


Figure 20. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X0, 0X1

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.

4.5.3.1.2 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in SDR mode:

- A1—Memory generates both read data and read strobe on SCK rising edge (or falling edge)
- A2—Memory generates read data on SCK falling edge and generates read strobe on SCK rising edge

Table 51. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case A1)

Symbol	Parameter	Value		Unit
		Min	Max	
	Frequency of operation	—	166	MHz
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-2	2	ns

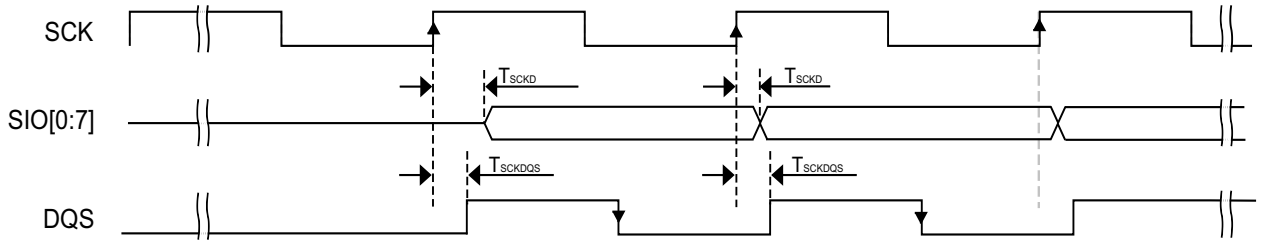


Figure 21. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X3 (case A1)

NOTE

Timing shown is based on the memory generating read data and read strobe on the SCK rising edge. The FlexSPI controller samples read data on the DQS falling edge.

Table 52. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case A2)

Symbol	Parameter	Value		Unit
		Min	Max	
	Frequency of operation	—	166	MHz
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-2	2	ns

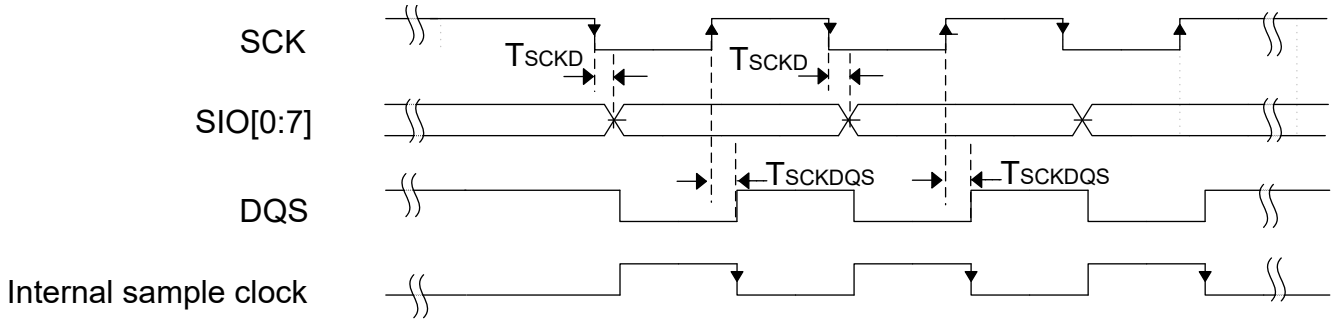


Figure 22. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X3 (case A2)

NOTE

Timing shown is based on the memory generating read data and DQS on the SCK falling edge and read strobe on the SCK rising edge. The FlexSPI controller samples read data on a half cycle delayed DQS falling edge.

Table 53 shows the input timing in SDR200M Read mode.

Table 53. FlexSPI input timing in SDR200M Read mode[1]

Description	Min	Max	Unit
Input delay	-1.5	+1.5	ns

1 This mode is only supported in FlexSPI1.

4.5.3.1.3 DDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1

Table 54. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	30	MHz
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time for incoming data	0	—	ns

Table 55. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x1

Symbol	Parameter	Min	Max	Unit
	Frequency of operation[1]	—	66	MHz
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time for incoming data	1	—	ns

1 Note: GPIO_AON_XX maximum frequency of operation in DDR mode is 52 MHz where FlexSPI*n*_MCR0[RXCLKSRC] = 0x1.

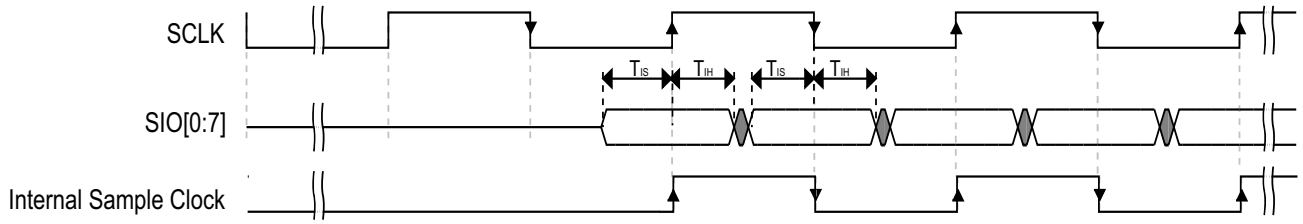


Figure 23. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1

4.5.3.1.4 DDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in DDR mode:

- B1–Memory generates both read data and read strobe on SCK edges
- B2–Memory generates read data on SCK edges and generates read strobe on SCK2 edges

Table 56. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B1)

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	166	MHz
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-1	1	ns

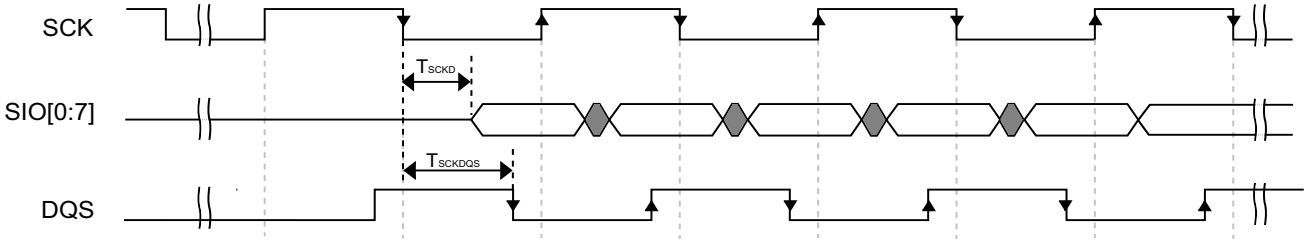


Figure 24. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B1)

Table 57. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B2)

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	166	MHz
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-1	1	ns

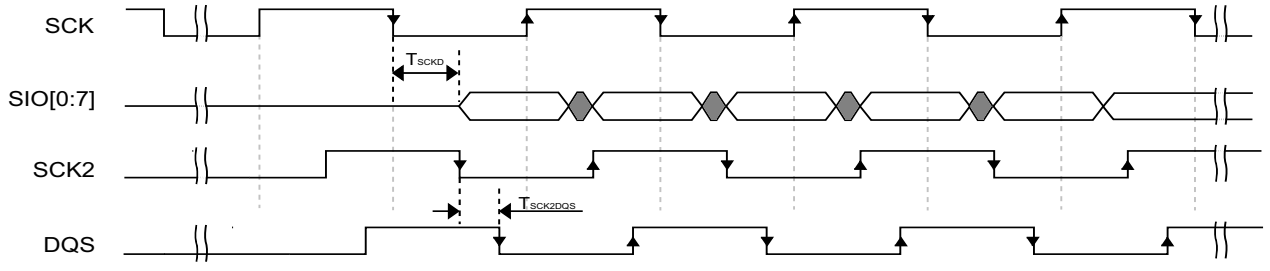


Figure 25. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B2)

Table 58 shows the input timing in DDR200M Read mode.

Table 58. FlexSPI input timing in DDR200M Read mode[1]

Description	Min	Max	Unit
Input delay	-0.6	+0.6	ns

1 This mode is only supported in FlexSPI1.

4.5.3.2 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

4.5.3.2.1 SDR mode

Table 59. FlexSPI output timing in SDR mode

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	166[1]	MHz
T_{ck}	SCK clock period	6.0	—	ns
T_{DVO}	Output data valid time	—	4	ns
T_{DHO}	Output data hold time	2	—	ns
T_{CSS}	Chip select output setup time	3 x T_{CK} - 1	—	ns
T_{CSH}	Chip select output hold time	3 x T_{CK} + 2	—	ns

1 The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used. Please refer to the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHA*x*CR1/FlexSPI*n*_FLSHB*x*CR1 register, the default values are shown above. Please refer to the *i.MXRT1180 Reference Manual* (IMXRT1180RM) for more details.

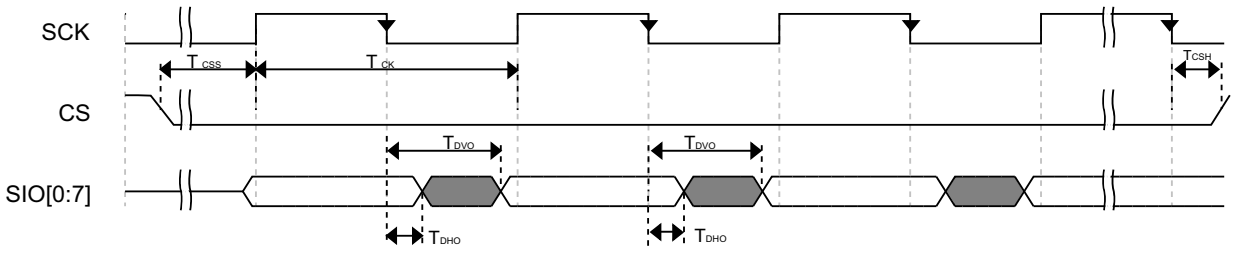


Figure 26. FlexSPI output timing in SDR mode

Table 60 shows the SDR200M Write mode.

Table 60. FlexSPI output timing in SDR200M Writing mode[1]

Description	Min	Max	Unit
Output delay	-1.5	+1.5	ns

1 This mode is only supported in FlexSPI1.

4.5.3.2.2 DDR mode

Table 61. FlexSPI output timing in DDR mode

Symbol	Parameter	Min	Max	Unit
	Frequency of operation[1]	—	166	MHz
T_{ck}	SCK clock period	6.0	—	ns
T_{DVO}	Output data valid time	—	2.2	ns
T_{DHO}	Output data hold time	0.8	—	ns
T_{CSS}	Chip select output setup time	3 x T_{CK} / 2 - 0.7	—	ns
T_{CSH}	Chip select output hold time	3 x T_{CK} / 2 + 0.8	—	ns

1 The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used. Please refer to the FlexSPI DDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHA*x*CR1/FlexSPI*n*_FLSHB*x*CR1 register, the default values are shown above. Please refer to the *i.MXRT1180 Reference Manual* (IMXRT1180RM) for more details.

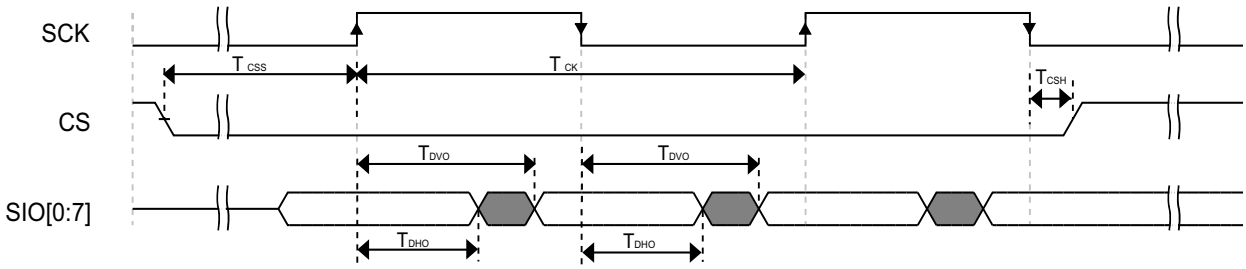


Figure 27. FlexSPI output timing in DDR mode

Table 62 shows the DDR200M Write mode.

Table 62. FlexSPI output timing in DDR200M Writing mode[1]

Description	Min	Max	Unit
Output delay	-0.6	+0.6	ns

1 This mode is only supported in FlexSPI1.

4.5.4 FlexSPI Follower parameters

Table 63 shows the AC electrical characteristics about FlexSPI follower.

Table 63. FlexSPI Follower AC electrical characteristics[1, 2]

Description	Symbol	ALT	Specification			Unit
			Min	Typ	Max	
Clock frequency except for Read Data (03h) instructions (3.0 – 3.6 V)	F_R	f_C	D.C.	—	133	MHz
Clock frequency except for Read Data (03h) instructions (2.7 – 3.0 V)	F_R	f_C	D.C.	—	104	MHz
Clock frequency except for Read Data instruction (03h)	F_R	—	D.C.	—	50	MHz
Clock High, Low Time for all instructions except for Read Data (03h)[3]	t_{CLH}, t_{CLL}	—	45%Pc	—	—	ns
Clock High, Low Time for Read Data (03h) instruction[3]	t_{CRLH}, t_{CRLL}	—	45%Pc	—	—	ns
Clock Rise Time peak to peak[4]	t_{CLCH}	—	0.1	—	—	V/ns
Clock Fall Time peak to peak[4]	t_{CHCL}	—	0.1	—	—	V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	3	—	—	ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}	—	3	—	—	ns
Data In Setup Time	t_{DVCH}	t_{DSU}	1	—	—	ns
Data In Hold Time	t_{CHDX}	t_{DH}	3	—	—	ns
/CS Active Hold Time relative to CLK	t_{CHSH}	—	3	—	—	ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}	—	3	—	—	ns
/CS Deselect Time (During Read)	t_{SHSL1}	t_{CSH}	10	—	—	ns
/CS Deselect Time (During Erase or Program or Write)	t_{SHSL2}	t_{CSH}	50	—	—	ns
Output Disable Time[4]	t_{SHQZ}	t_{DIS}	—	—	7	ns
Clock Low to Output Valid	t_{CLQV}	t_V	—	—	6	ns
Output Hold Time	t_{CLQX}	t_{HO}	1.5	—	—	ns
Write Protect Setup Time Before /CS Low[5]	t_{WHSL}	—	20	—	—	ns
Write Protect Hold Time After /CS High[5]	t_{SHWL}	—	100	—	—	ns
/CS High to Power-down Mode[4]	t_{DP}	—	—	—	3	µs
/CS High to Standby Mode without ID Read[4]	t_{RES1}	—	—	—	3	µs
/CS High to Standby Mode with ID Read[4]	t_{RES2}	—	—	—	1.8	µs

Table 63. FlexSPI Follower AC electrical characteristics[1, 2] (continued)

Description	Symbol	ALT	Specification			Unit
			Min	Typ	Max	
/CS High to next Instruction after Suspend[4]	t_{SUS}	—	—	—	20	µs
/CS High to next Instruction after Reset[4]	t_{RST}	—	—	—	30	µs
/Reset pin Low period to reset the device[4,6]	t_{RESET}	—	1	—	—	µs
Write Status Register Time	t_W	—	—	10	15	ms
Page Program Time	t_{PP}	—	—	0.4	3	ms
Sector Erase Time (4 KB)	t_{SE}	—	—	50	400	ms
Block Erase Time (32 KB)	t_{BE1}	—	—	120	1,600	ms
Block Erase Time (64 KB)	t_{BE2}	—	—	150	2,000	ms
Chip Erase Time	t_{CE}	—	—	80	400	s

1 Tested on samples basis and specified through design and characterization data. TA = 25 °C, VCC = 3.0 V.

2 4-bytes address alignment for Quad Read: read address start from A1,A0 = 0,0

3 Clock high + Clock low must be less than or equal to Pc. Pc = 1/fc (max.)

4 Value guaranteed by design and/or characterization, not 100% tested in production.

5 Only applicable as a constraint for a Write Status Register instruction when SRP = 1.

6 It is possible to reset the device with shorter t_{RESET} (as short as a few hundred ns), a 1 µs minimum is recommended to ensure reliable operation.

4.6 Audio

This section provides information about audio module.

4.6.1 PDM Microphone interface timing parameters

NOTE

These timing requirements apply only if the clock divider is enabled (PDM_CTRL2[CLKDIV] = 0), otherwise there are no special timing requirements.

The PDM microphones must meet the setup and hold timing requirements shown in the following table. The "k" factor value in Table 64 depends on the selected quality mode as shown in Table 65.

Table 64. PDM timing parameters

Parameter	Value
trs, tfs	[1] $<= \frac{\text{floor (kxCLKDIV) - 1}}{\text{@(moduleNickname)\_CLK\_ROOTrate}}$
trh, tfh	>= 0

1 @moduleNickname = PDM. Depending on K value, user must make sure floor (K x CLKDIV) > 1 to avoid timing problems.

Table 65. K factor value

Quality factor	K factor
High Quality	1/2
Medium Quality, Very Low Quality 0	1
Low Quality, Very Low Quality 1	2
Very Low Quality 2	4

Figure 28 illustrates the timing requirements for the PDM.

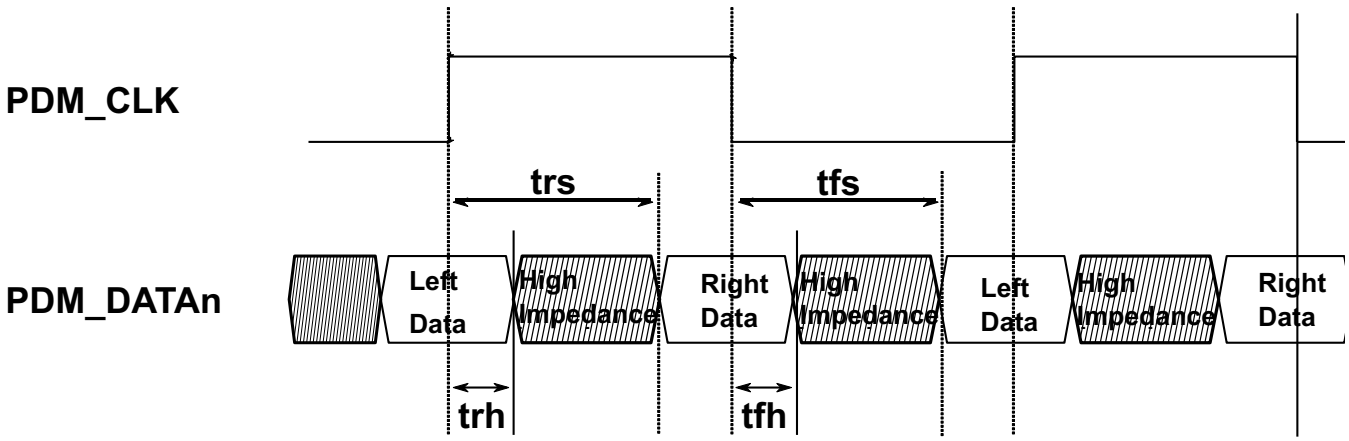


Figure 28. PDM input/output timing requirements

4.6.2 SAI/I2S switching specifications

This section provides the AC timings for the SAI in master (clocks driven) and slave (clocks input) modes. All timings are given for non-inverted serial clock polarity (SAI_TCR2[BCP] = 0, SAI_RCR2[BCP] = 0) and non-inverted frame sync (SAI_TCR4[FSP] = 0, SAI_RCR4[FSP] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 66. Master mode SAI timing

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	15	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	40	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period

Table 66. Master mode SAI timing (continued)

Num	Characteristic	Min	Max	Unit
S5	SAI_BCLK to SAI_FS output valid	—	8.4	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	10	ns
S8	SAI_BCLK to SAI_TXD invalid	1	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	14	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

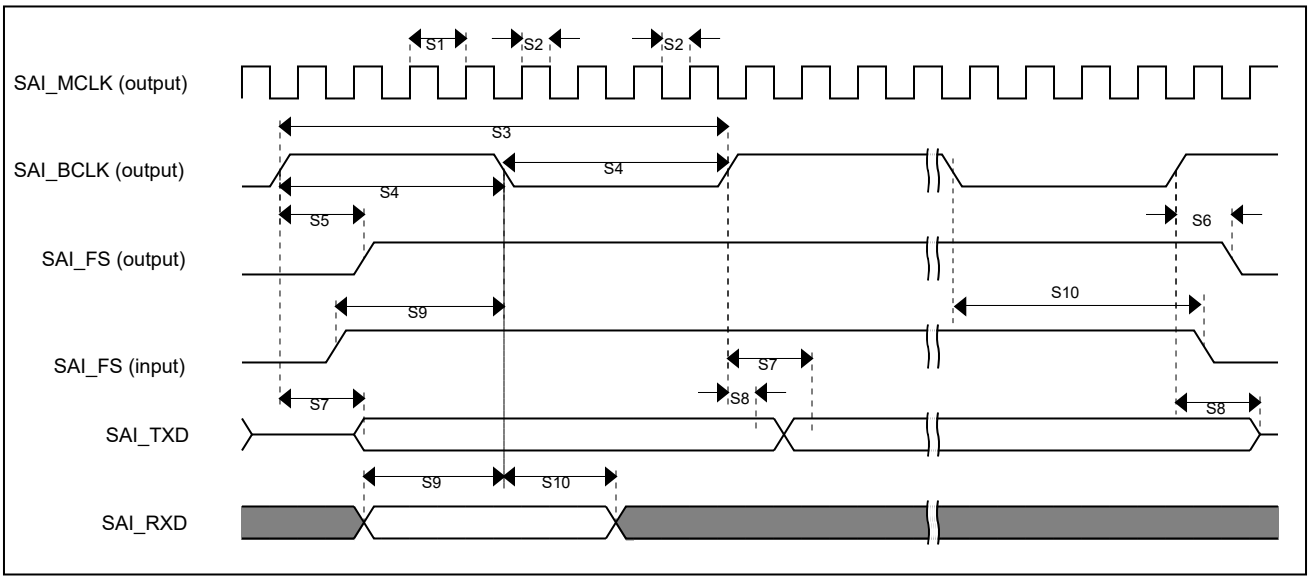


Figure 29. SAI timing—Master modes

Table 67. Slave mode SAI timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	40	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	6	—	ns
S14	SAI_FS input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	-1.5	—	ns
S17	SAI_RXD setup before SAI_BCLK	6	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns
S19	SAI_FS input assertion to SAI_TXD output[1]	—	18.5	ns

1 Applies to first bit in each frame and only if the TCR4[FSE] bit is clear.

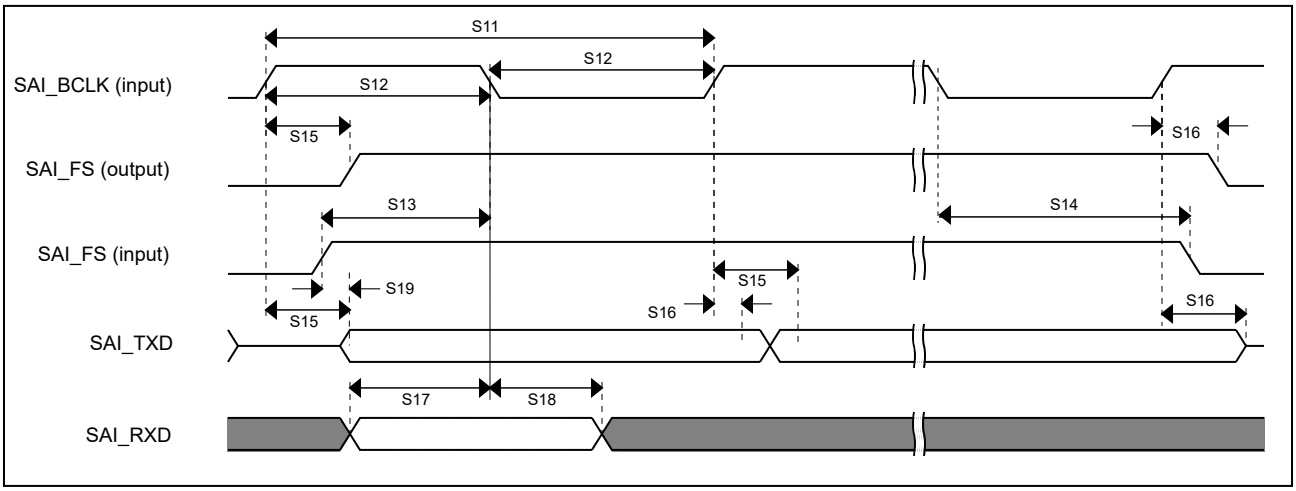


Figure 30. SAI timing—Slave mode

4.6.3 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 68 and Figure 31 and Figure 32 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 68. SPDIF timing parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT1 output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

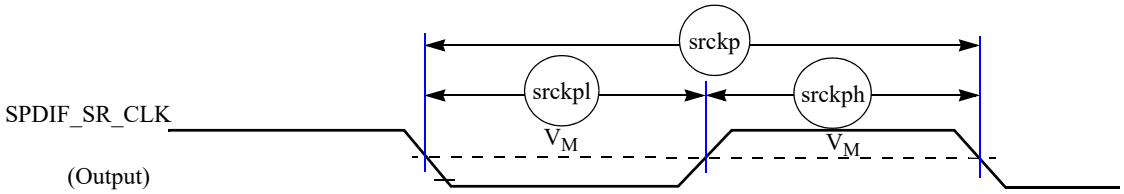


Figure 31. SPDIF_SR_CLK timing diagram

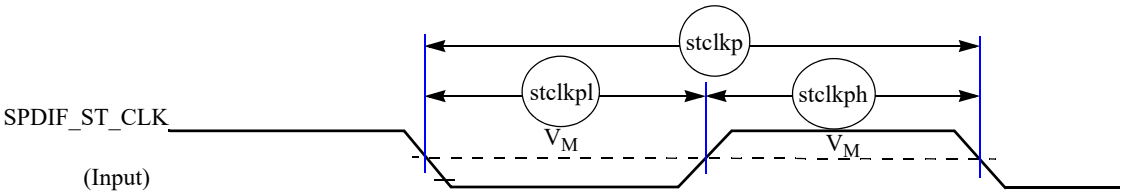


Figure 32. SPDIF_ST_CLK timing diagram

4.7 Analog

The following sections provide information about analog interfaces.

4.7.1 16-bit ADC electrical specifications

Table 69 lists the ADC operation conditions.

Table 69. 16-bit ADC operating conditions

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit	Notes
3.3 V supply voltage	—	V_{DDA33}[1]	2.7	3.3	3.6	V	—
Supply voltage	—	VDDAD[2]	1.62	1.8	1.98	V	—
Ground voltage	—	V_{SSAD}	-0.1	0	+0.1	V	—
Reference voltage High	—	V_{REFH}	1.0	V_{DDAD}	V_{DDAD}	V	—
Reference voltage Low	—	V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	—
Input voltage	—	V_{ADIN}	V_{REFL}	—	3.6	V	3
Sample cycles	—	C_{SMP}	3.5[4]	—	131.5	Cycles	—
ADC conversion clock frequency[5]	16b Mode	F_{ADCK}	6	—	88	MHz	—
	12b Mode		6	—	88		—
Conversion cycles	16b Mode	C_{CONV}	24	—	152	Cycles	—
	12b Mode		19	—	147		—
Conversion Rate	16b Mode	R_{CONV}	—	—	3.14	MS/s	6
	12b Mode		—	—	3.8		7

Table 69. 16-bit ADC operating conditions (continued)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Maximum Conversion Rate for internal channels	—	R_{CONV_int}	—	—	0.55	MS/s	8
Input Capacitance	3.6 V mode (CSCALE = 0)	C_{ADIN}	—	1.9	2.375	pF	—
	1.8 V mode (CSCALE = 1)		—	3.8	4.75		—
Input Resistance	3.6 V mode (CSCALE = 0)	R_{ADIN}	—	—	2.54	KΩ	—
	1.8 V mode (CSCALE = 1)		—	—	1.27		—
Parasitic Capacitance	—	C_P	—	3	5	pF	9
Analog source Resistance	—	R_{AS}	—	—	5	KΩ	10

1 Power rail pin is VDDA_ADC_3P3.

2 Power rail pin is VDDA_ADC_1P8.

3 CSCALE bit must be clear for >1.8 V inputs.

4 Must meet min T_{SMP}

5 Only valid when VDDA_ADC_1P8 is selected as ADC voltage reference. If ADC_VREFH is selected as ADC voltage reference, the maximum ADC conversion clock frequency is 20 MHz to meet the listed specifications.

6 F_{ADCK} = 88 MHz, STS = 010

7 F_{ADCK} = 88 MHz, STS = 010

8 F_{ADCK} = 88 MHz, STS = 111

9 Includes Pad, Pin

10 This resistance is external to the MCU. To achieve the best results, the analog source resistance should be kept as low as possible.

Table 70 lists the ADC electrical characteristics.

Table 70. 16-bit ADC electrical characteristics

Characteristic	Conditions[1]	Symbol	Min	Typ[2]	Max	Unit	Notes
Current consumption	Power Enabled (PWREN = 1) No Conversions	I_{DDAD}	—	75	—	µA	—
	12b, Single-Enabled Mode		—	542	—	µA	3
	12b, Differential or Dual-SE Mode		—	807	—	µA	4
	16b, Single-Enabled Mode		—	789	—	µA	3
	16b, Differential or Dual-SE Mode		—	1329	—	µA	4
Temperature sensor supply current	Temp sensor adder	I_{DDTS}	—	60	—	µA	—
Required sample time	Use equation based on R_{AS}, R_{ADIN}, C_{ADIN}, C_{AS}, C_P, and desired accuracy	T_{SMP_REQ}	See note	—	—	ns	5
Required Auto-Zero time	12b Mode	T_{AZ_REQ}	65.5	—	—	ns	6
	16b Mode		89.3	—	—	ns	7
Sample time	External inputs	T_{SMP}	See note	—	—	ns	8
Internal channel sample time	Internal inputs	T_{SMP_INT}	1.5	—	—	µs	—
Differential Nonlinearity	12b Mode	DNL	—	—	±1	LSB	9
Integral Nonlinearity	12b Mode	INL	—	—	±1.5	LSB	—
Offset Error[10]	12b Mode, $V_{ADIN} = V_{REFL}$	E_O	—	—	±0.02	%FSR	11,12, 13
Gain Error[14]	12b Mode, $V_{ADIN} = V_{REFH}$	E_G	—	—	±0.05	%FSR	—

Table 70. 16-bit ADC electrical characteristics (continued)

Characteristic	Conditions[1]	Symbol	Min	Typ[2]	Max	Unit	Notes
ENOB, 12b Differential Mode	0.95 MS/s (F_{adc} = 88 MHz, AVGS = 0010)	$ENOB_{DIFF}$	—	12.0	—	—	11
	3.8 MS/s (F_{adc} = 88 MHz, AVGS = 0000)		—	11.4	—	—	
ENOB, 12b Single Ended Mode	0.95 MS/s (F_{adc} = 88 MHz, AVGS = 0010)	$ENOB_{SE}$	—	11.3	—	—	
	3.8 MS/s (F_{adc} = 88 MHz, AVGS = 0000)		—	10.8	—	—	
THD	12b Mode	THD	—	88	—	dB	—
SFDR	12b Mode	SFDR	—	89	—	dB	—
Differential Nonlinearity	16b Mode	DNL	—	—	±3	LSB	—
Integral Nonlinearity	16b Mode	INL	—	—	±16	LSB	—
Offset Error	16b Mode, $V_{ADIN} = V_{REFL}$	E_O	—	—	±0.01	%FSR	11,12,13
Gain Error	16b Mode, $V_{ADIN} = V_{REFH}$	E_G	—	—	±0.03	%FSR	—
Total Unadjusted Error	16b Mode	TUE	—	—	±52	LSB	—
ENOB, 16b Differential Mode	0.785 MS/s (F_{adc} = 88 MHz, AVGS = 0010)	$ENOB_{DIFF}$	—	13.3	—	—	11
	3.14 MS/s (F_{adc} = 88 MHz, AVGS = 0000)		—	12.5	—	—	
ENOB, 16b Single Ended Mode	0.785 MS/s (F_{adc} = 88 MHz, AVGS = 0010)	$ENOB_{SE}$	—	12.8	—	—	
	3.14 MS/s (F_{adc} = 88 MHz, AVGS = 0000)		—	11.9	—	—	
THD	16b Mode	THD	—	95	—	dB	—
SFDR	16b Mode	SFDR	—	88	—	dB	—
Start-up time	—	$t_{ADCSTUP}$	5	—	—	µs	15
Temperature Sensor Error	—	E_{TS}	—	±1.5	±3.5	°C	
Slope factor constant	—	A	—	789.2	—	—	—
Offset constant	—	B	—	319.2	—	—	—
Bandgap constant	—	α	—	11.2	—	—	—

[1] All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$ and using a high speed dedicated input channel.
[2] Typical values assume V_{DDA} = 1.8 V, Temp = 25 °C, f_{ADCK} = 88 MHz unless otherwise stated. Typical values are for reference only, and are not tested in production.
[3] 88 MHz clock, CTYPE = 0X
[4] 88 MHz clock, CTYPE = 1X
[5] $T_{SMP\_REQ} = B * ln(2) * [R_{AS} * (C_{AS} + C_P + C_{ADIN}) + (R_{AS}+R_{ADCtotal}) * C_{ADIN}]$, B = desired sampling accuracy in bits
[6] 5.5 cycles at 88 MHz
[7] 7.5 cycles at 88 MHz
[8] $T_{SMP} = max (T_{SMP\_REQ}, T_{AZ\_REQ})$
[9] Monotonic with no missing codes in 12b Mode
[10] Offset error is same as ZSE, error measured at 0 V with zero scale.
[11] F_{in} = 1 kHz, half factor mode
[12] For 3.6 V tolerant input channels
[13] FSR = VREFH - VREFL
[14] Gain error is FSE - ZSE (same as FSE - E_O)
[15] Delay required

4.7.1.1 16-bit ADC input impedance equivalent circuit diagram

There is an additional R_{IOMUX} of 350 Ω (from 295 Ω to 405 Ω) resistance if an input goes through the MUX inside the IO and C_P of 3 pF as shown in Figure 33.

To calculate the sample request time, using the following equation where $R_{ADCtotal} = R_{ADIN} + R_{IOMUX}$, R_{IOMUX} = 350 Ω, Cp = 3 pF as shown in Figure 33.

$$T_{SMP\_REQ} = B * ln(2) * [R_{AS} * (C_{AS} + C_P + C_{ADIN}) + (R_{AS} + R_{ADCtotal}) * C_{ADIN}]$$

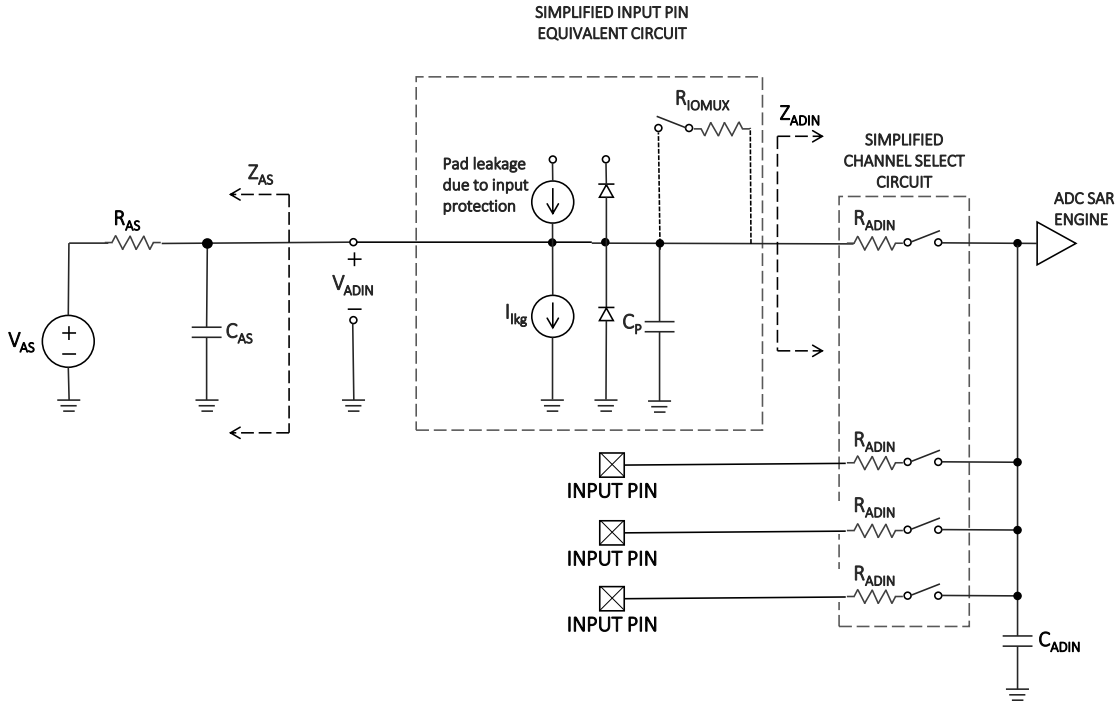


Figure 33. ADC input impedance equivalent circuit diagram

4.7.2 Voltage Reference (VREF)

Table 71 lists the electrical specification of VREF.

Table 71. VREF electrical specifications

Symbol	Description	Min	Typ	Max	Unit
VDDA	Analog supply voltage	1.71	—	1.98	V
VDD	Digital supply voltage	—	1.1	—	V
V_{STEP}	Fine trim step	—	0.5	—	mV
T_{STUP}	Start-up time	—	400	—	μs
T_C	Temperature coefficient	—	15	—	ppm/°C
I_{OUT}	Drive strength	±1	—	—	mA
ΔV_{LOAD}	Load regulation	—	100	200	μV/mA
V_{OUT}	Buffered output voltage	—	1.2	—	V
I_Q	Quiescent	—	750	—	μA
C	Capacitance	—	220	—	nF

4.7.3 12-bit DAC electrical characteristics

4.7.3.1 12-bit DAC operating requirements

Table 72. 12-bit DAC operating conditions

Symbol	Description	Min	Typ	Max	Unit	Notes
C_L	Output load capacitance	—	50	100	pF	1
I_L	Output load current	—	—	1	mA	2

1 The DAC output can drive R and C loading. The user should consider both DC and dynamic application requirements. 50 pF C_L provides the best dynamic performance, while 100 pF provides the best DC performance.

2 Sink or source current ability.

Table 73. DAC characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit	Notes
VDACOUTL	DAC low level output voltage	ADC_VREFH selected, Rload = 18 kΩ, Cload = 50 pF	VSS	—	0.15	V	1
VDACOUTH	DAC high level output voltage		VDDA_ADC_1P8 - 0.15	—	VDDA_ADC_1P8	V	
DNL	Differential nonlinearity error	Code 100h — F00h best fit curve	—	±0.5	±1	LSB	—
INL	Integral nonlinearity error	Code 100h — F00h best fit curve	—	±2	—	LSB	—

Table 73. DAC characteristics (continued)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit	Notes
EO	Offset error	Code 100h	—	±0.6	—	%FSR (Full-scale range)	—
TEO	Offset error temperature coefficient	Code 100h	—	±30	—	μV/°C	—
EG	Gain error	Code F00h	—	±0.4	—	%FSR	—
TEG	Gain error temperature coefficient	Code F00h	—	±10	—	ppm of FSR/°C	—
TFS_LS	Full scale setting time in Low Speed mode	Code 100h — F00h or F00h — 100h @ Zero Temperature Coefficient (ZTC) current	—	5	—	μs	2
TFS_MS	Full scale setting time in Middle Speed mode	Code 100h — F00h or F00h — 100h @ZTC current	—	1	—		
TFS_HS	Full scale setting time in High Speed mode	Code 100h — F00h or F00h — 100h @ZTC current	—	0.5	—		
TCC_LS	Code to code setting time in Low Speed mode	Code 7F7h — 807h or 807h — 7F7h @ZTC current	—	1	—		
TCC_MS	Code to code setting time in Middle Speed mode	Code 7F7h — 807h or 807h — 7F7h @ZTC current	—	0.5	—		
TCC_HS	Code to code setting time in High Speed mode	Code 7F7h — 807h or 807h — 7F7h @ZTC current	—	0.3	—		
SR_LS	Slew rate in Low Speed mode	Code 100h — F00h or F00h — 100h @ZTC current	—	0.24	—	V/μs	3
SR_MS	Slew rate in Middle Speed mode	Code 100h — F00h or F00h — 100h @ZTC current	—	1.2	—		
SR_HS	Slew rate in High Speed mode	Code 100h — F00h or F00h — 100h @ZTC current	—	2.4	—		
PSRR	Power supply rejection ratio	Code 800h, ∆VDDA_1P8 (powered by VDDA_ADC_1P8) = 100 mV, DAC Reference Select (DACRFS) = 1	—	70	—	dB	4

Table 73. DAC characteristics (continued)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit	Notes
Glitch	Glitch energy	Code 100h — F00h — 100h	—	30	—	nV-s	—
		Code 7FFh — 800h — 7FFh	—	30	—		
CT	Channel to channel crosstalk	—	—	—	-80	dB	5
ROP	Output resistance	Code 100h — F00h and Rload = 18 kΩ	—	200	—	Ω	6

1 It is recommended to operate the DAC in the output voltage range between 0.15 V and (VDDA_ADC_1P8 - 0.15 V) for best accuracy. Linearity of the output voltage outside this range will be affected as current load increases.

2 The DAC output remains within ±0.5 LSB of the final measured value for digital input code change. Noise on the power supply can cause this performance to degrade to ±1 LSB. This parameter represents both rising edge and falling edge settling time.

3 Time for the DAC output to transition from 10% to 90% signal amplitude (rising edge or falling edge).

4 PSRR = 20 x lg{ΔVDDA_ADC_1P8 /ΔVDAC_OUT}

5 If two DACs are used and sharing the same VREFH.

6 Based on design simulation.

4.7.4 ACMP electrical specifications

Table 74 lists the characteristics of ACMP.

Table 74. ACMP characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
VAIN	Analog input voltage	—	0	—	NVCC_GPIO_AD[1]	V
VAIO	Analog input offset voltage	—	—	—	20	mV
VH	Analog comparator hysteresis	Hystrl[1:0] = 00	—	5	—	mV
		Hystrl[1:0] = 01	—	10	—	mV
		Hystrl[1:0] = 10	—	20	—	mV
		Hystrl[1:0] = 11	—	30	—	mV
TDHS	Propagation delay, high-speed mode	Normal supply	—	—	50	ns
	Propagation delay, low-speed mode	—	—	—	5	μs
—	Analog comparator initialization delay	—	—	—	20	μs
INL	8-bit DAC integral non-linearity	—	-1	—	1	LSB
DNL	8-bit DAC differential non-linearity	—	-1	—	1	LSB

[1] The maximum input voltage for CMP analog inputs associated with GPIO_AD bank is NVCC_GPIO_AD. RDIVE bit must be set for greater than 1.8 V inputs.

4.7.5 SINC filter

Table 75 lists the timing parameters of SINC.

Table 75. SINC timing parameters

Symbol	Description	Condition	Min	Typ	Max	Unit
MCLK	External modulator clock frequency	—	0.02	—	33	MHz
MMCLK	Manchester modulator clock frequency	Clock recovered internally using External Modulator bit	—	—	22	MHz
TS1	Setup time from data valid to clock high	—	2	—	—	ns
TH1	Hold time from clock high to data valid	—	2	—	—	ns
TS2	Setup time from data valid to clock low	—	2	—	—	ns
TH2	Hold time from clock low to data valid	—	2	—	—	ns
TS3	Setup time from data valid to clock low	—	2	—	—	ns
TH3	Hold time from clock low to data valid	—	2	—	—	ns
TS4	Setup time from data valid to clock high	—	2	—	—	ns
TH4	Hold time from clock high to data valid	—	2	—	—	ns

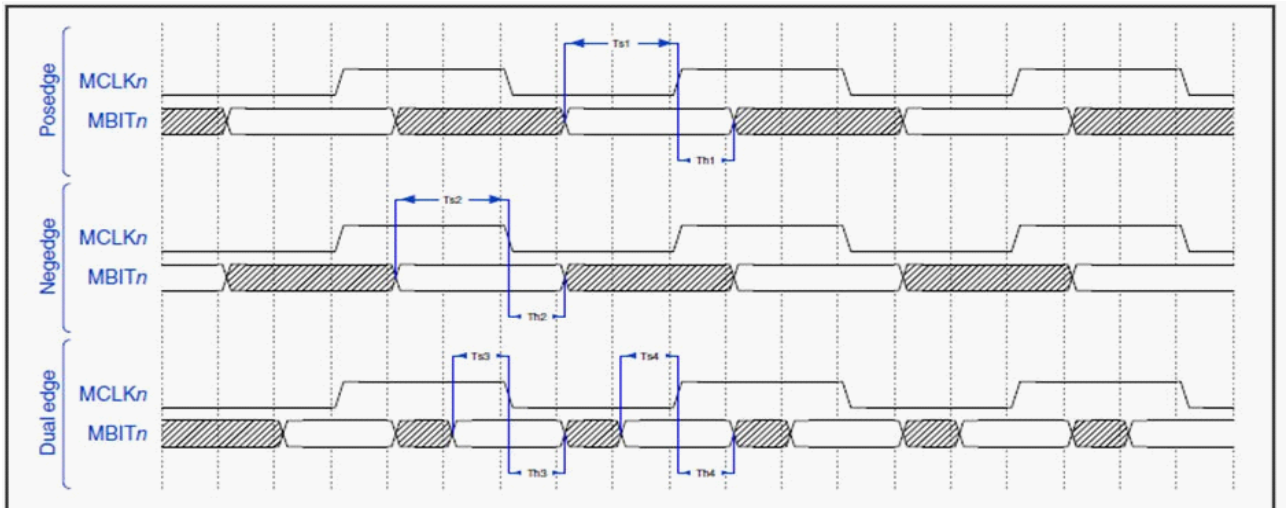


Figure 34. SINC timing

4.7.6 Temperature sensor

Table 76 lists the parameters of temperature sensor.

Table 76. Temperature sensor parameters

Parameter	Min	Max	Unit
Temperature range[1]	-40	125	°C

1 Accuracy of measurement: ± 5°C for 25°C and above, while ± 10°C for below 25°C.

4.8 Communication interfaces

The following sections provide the information about communication interfaces.

4.8.1 LPSPI timing parameters

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

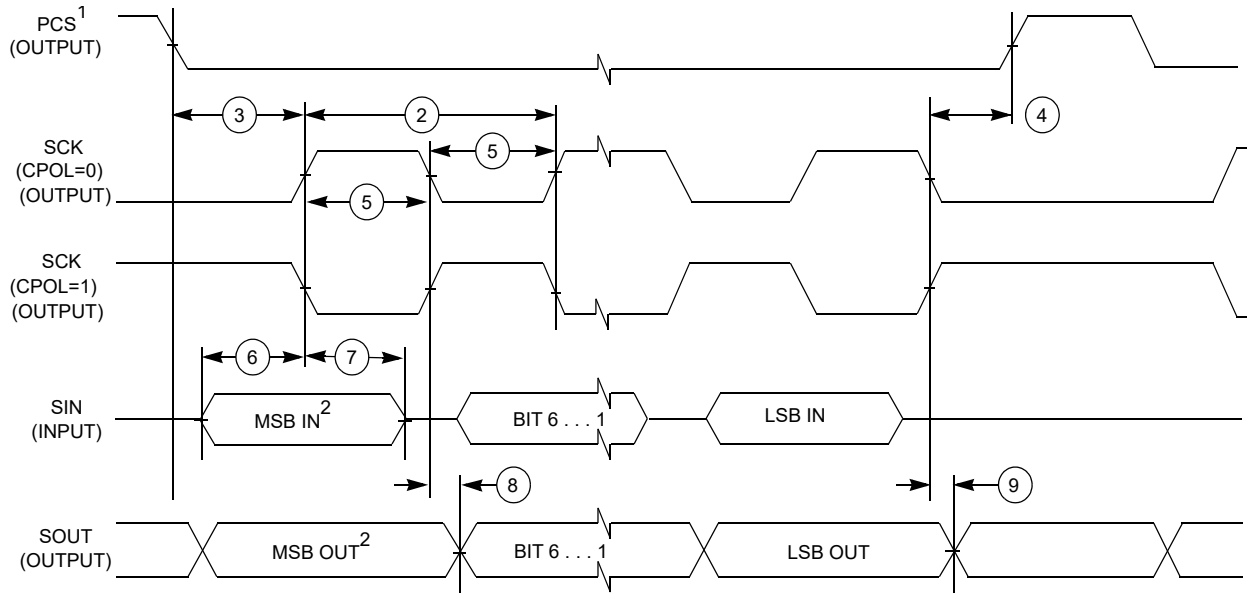
Table 77. LPSPI Master mode timing

Number	Symbol	Description	Min.	Max.	Units	Note
1	f_{SCK}	Frequency of LPSPI clock root	—	f_{periph} / 2	MHz	1
2	t_{SCK}	SCK period	2 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSCK}	Clock (SCK) high or low time	t_{SCK} / 2 - 3	—	ns	—
6	t_{SU}	Data setup time (inputs)	3	—	ns	3
7	t_{HI}	Data hold time (inputs)	2	—	ns	—
8	t_V	Data valid (after SCK edge)	—	4.5	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—

1 Absolute maximum frequency of operation (fop) is 60 MHz. The clock driver in the LPSPI module for f_{periph} must guaranteed this limit is not exceeded.

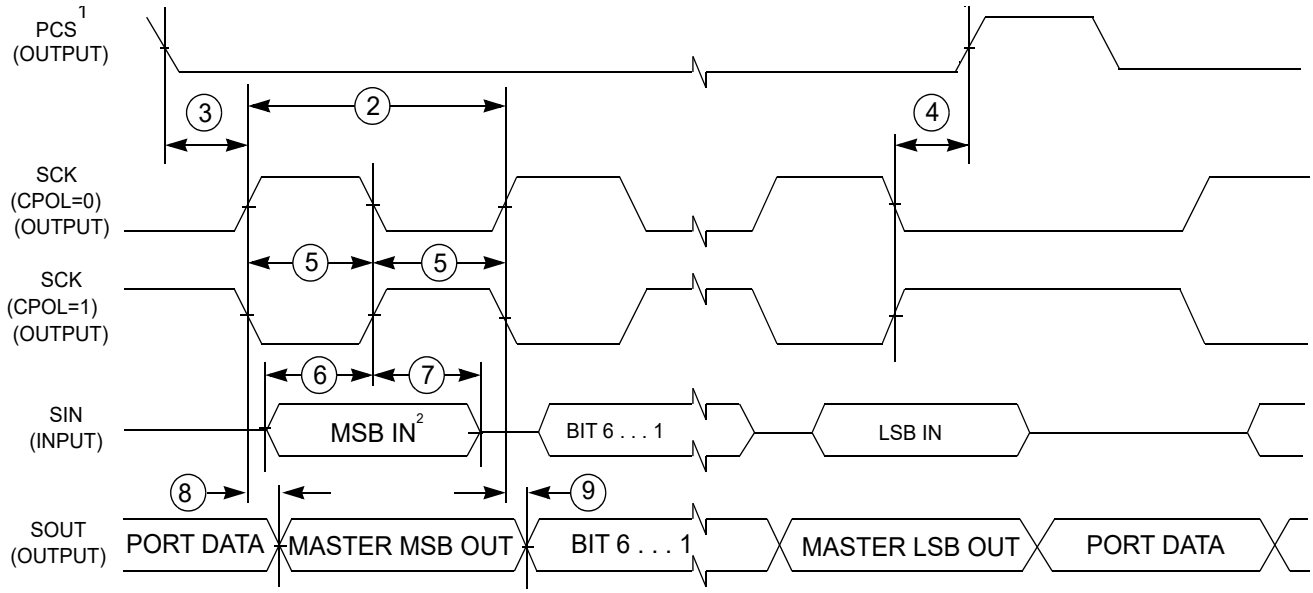
2 $t_{periph} = 1000 / f_{periph}$

3 If enable sample = 1, the data setup specification is same with the one in Slave mode.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 35. LPSPI Master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 36. LPSPI Master mode timing (CPHA = 1)

Table 78. LPSPI Slave mode timing

Number	Symbol	Description	Min.	Max.	Units	Note
1	f_{SCK}	Frequency of LPSPI clock root	0	f_{periph} / 2	MHz	1
2	t_{SCK}	SCK period	2 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSCK}	Clock (SCK) high or low time	t_{SCK} / 2 - 5	—	ns	—
6	t_{SU}	Data setup time (inputs)	3	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.8	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_V	Data valid (after SCK edge)	—	12.8	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—

1 Absolute maximum frequency of operation (fop) is 30 MHz. The clock driver in the LPSPI module for f_{periph} must be guaranteed this limit is not exceeded.

2 $t_{periph} = 1000 / f_{periph}$

3 Time to data active from high-impedance state

4 Hold time to high-impedance state

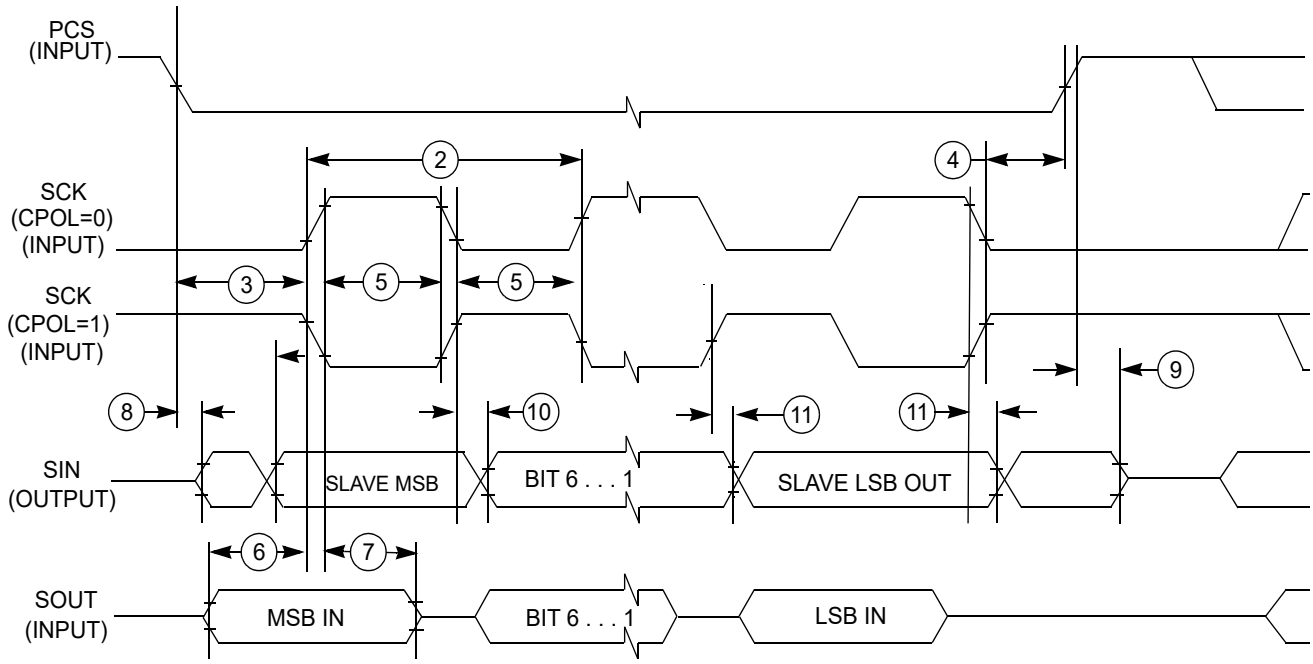


Figure 37. LPSPI Slave mode timing (CPHA = 0)

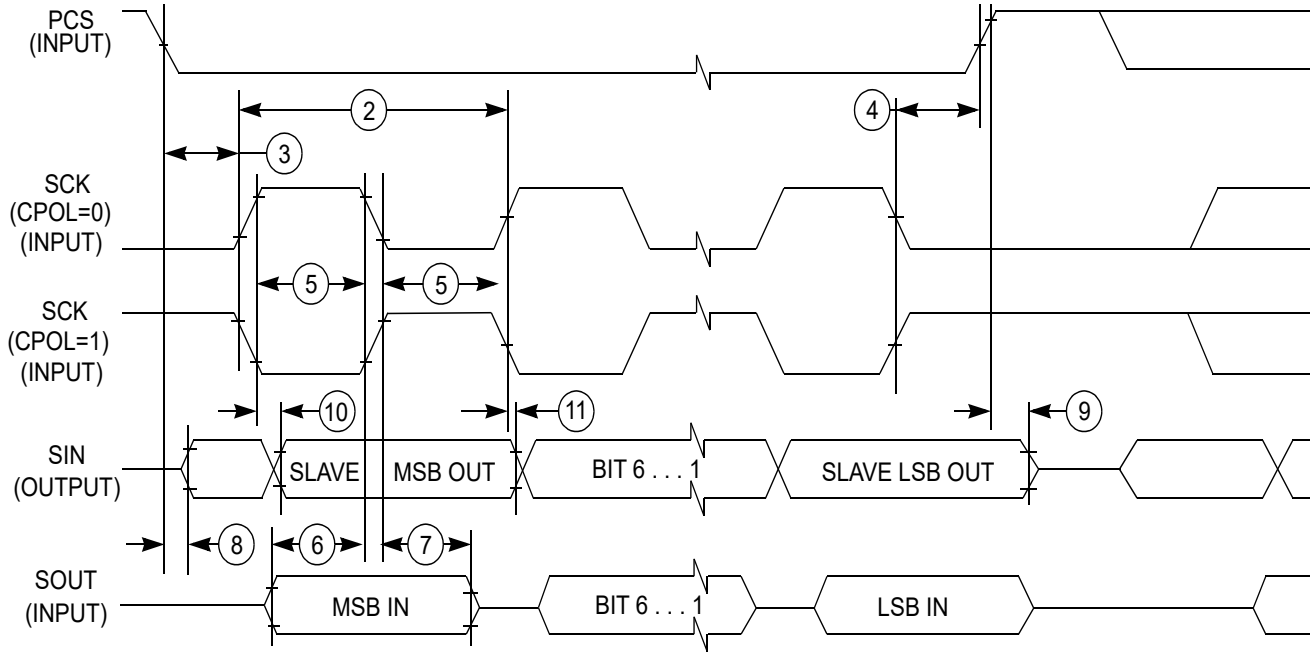


Figure 38. LPSPI Slave mode timing (CPHA = 1)

4.8.2 LPI2C module timing parameters

This section describes the timing parameters of the LPI2C module.

Table 79. LPI2C module timing parameters[1]

Symbol	Description		Min	Max	Unit	Notes
f_{SCL}	SCL clock frequency	Standard mode (Sm)	0	100	kHz	[2]
		Fast mode (Fm)	0	400		
		Fast mode Plus (Fm+)	0	1000		
		High speed mode (Hs-mode)	0	3400		
		Ultra Fast mode (UFm)	0	5000		

1 For more details, see *UM10204 I2C-bus specification and user manual*.

2 Standard, Fast, Fast+, and Ultra Fast modes are supported; High speed mode (HS) in slave mode.

4.8.3 Improved Inter-Integrated Circuit Interface (I3C) specifications

I3C conforms to the MIPI I3C v1.1.1 and I3C Basic v1.1.1.

I3C interface is not supported on GPIO-Standard-plus pad type for 5 V operation. Measurements are with maximum output load of 30 pf, input transition of 1 ns. GPIO-Standard-plus pad configured with DSE = 1'b1 and GPIO-Medium pad with DSE = 1'b1 and SRE = 1'b1. SCL, SDA and PUR combination should be of same pad type. For e.g. I3C medium Data Pads to be used with I3C Medium Clock and PUR Pads Only. I3C Standard plus Data Pads to be used with I3C standard plus Clock and PUR pads only.

Table 80. I3C Push-Pull timing parameters (SDR)

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
f_{SCL}	SCL clock frequency	0.01	12.5	12.9	MHz	—
t_{DIG_L}	SCL clock low period[1, 2]	32	—	—	ns	—
t_{DIG_H}	SCL clock high period[1]	32	—	—	ns	—
t_{SCO}	Clock in to data out for Slave[3, 4]	—	—	12	ns	—
t_{CR}	SCL clock rise time[5]	—	—	150 x 1 / f_{SCL} (capped at 60 ns)	ns	—
t_{CF}	SCL clock fall time[5]	—	—	150 x 1 / f_{SCL} (capped at 60 ns)	ns	—
t_{HD_PP}	SDA signal data hold in Push-Pull Mode, Slave[6]	0	—	—	ns	—
t_{SU_PP}	SDA signal setup in Push-Pull Mode	3	—	—	ns	—

1 tDIG_L and tDIG_H are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH.

2 As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., tCF + 3 for falling edge clocks, and tCR + 3 for rising edge clocks.

3 Devices with more than 12 ns of t_{SCO} delay shall set the limitation bit in the BCR, and shall support the GETMXDS CCC to allow the Master to read this value and adjust computations accordingly. For purposes of system design and test conformance, this parameter should be considered together with pad delay, bus capacitance, propagation delay, and clock triggering points.

4 Pad delay based on 90 Ω / 4 mA driver and 50 pF load. Note that Master may be a Slave in a multi-Master system, and thus shall also adhere to this requirement.

5 The clock maximum rise/fall time is capped at 60 ns. For lower frequency rise and fall the maximum value is limited at 60 ns, and is not dependent upon the clock frequency.

6 tHD_PP is a Hold time parameter for Push-Pull Mode that has a different value for Master mode vs. Slave mode. In SDR Mode the Hold time parameter is referred to as tHD_SDR.

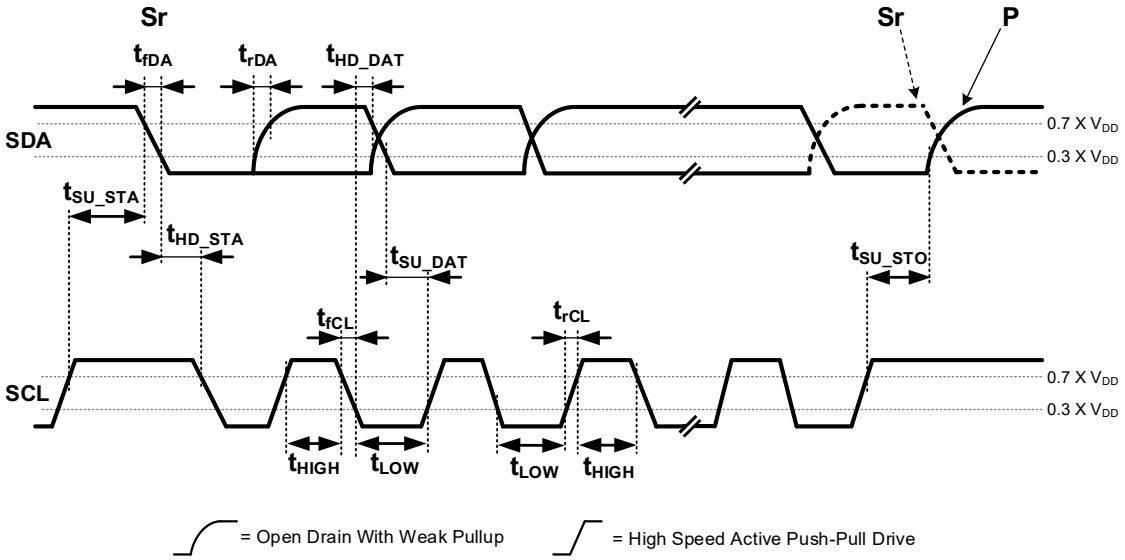


Figure 39. I3C legacy mode timing

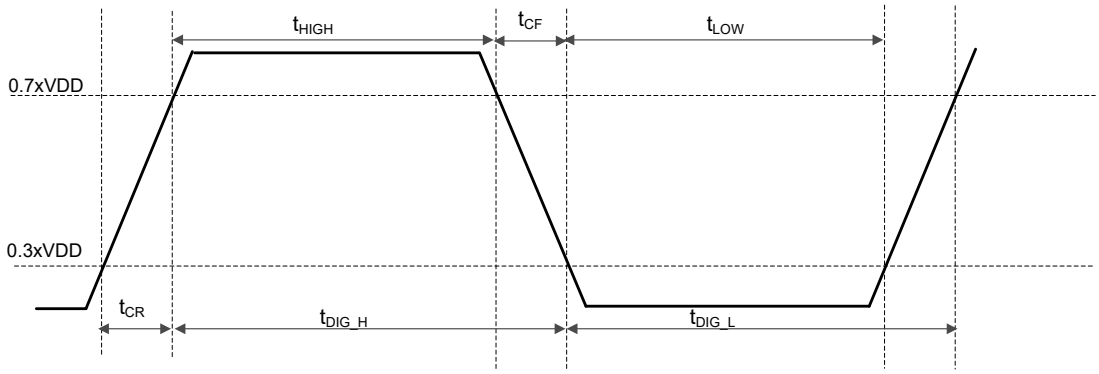


Figure 40. t_{DIG_H} and t_{DIG_L}

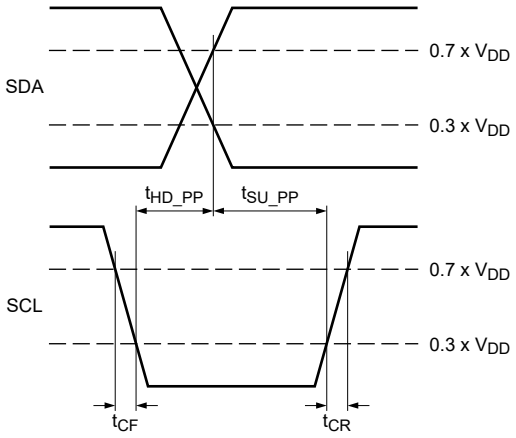


Figure 41. Master out timing

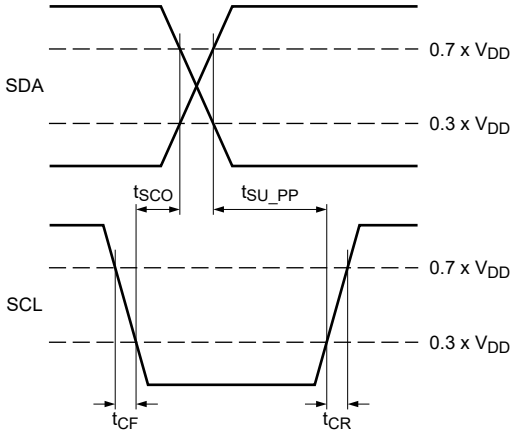


Figure 42. Slave out timing

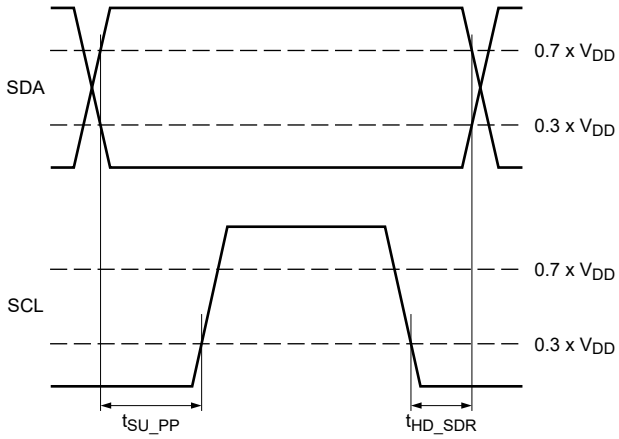


Figure 43. Master SDR timing

4.8.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC5.1 (single data rate) timing, eMMC5.1/SD3.0 (dual data rate) timing and SDR50/SDR104 AC timing.

4.8.4.1 SD3.0/eMMC4.3 (Single Data Rate) specifications

Figure 44 depicts the timing of SD3.0/eMMC4.3, and Table 81 lists the SD/eMMC4.3 timing characteristics.

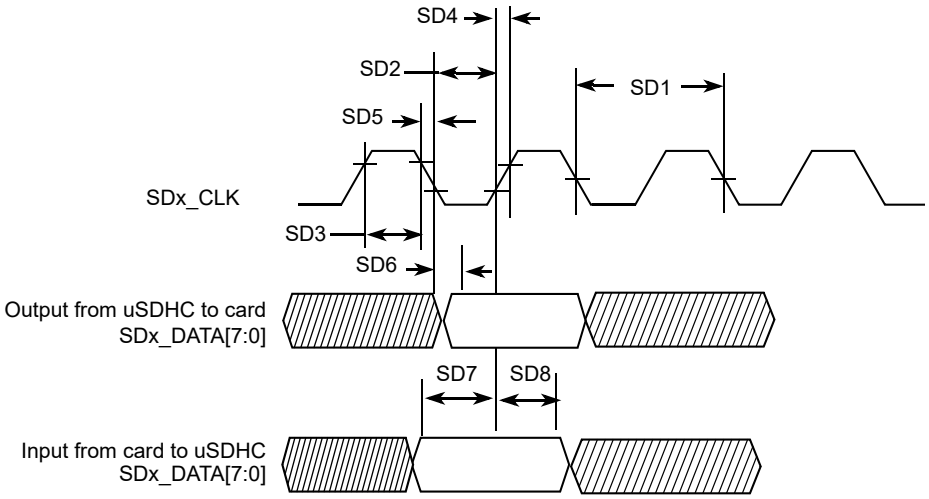


Figure 44. SD/eMMC4.3 timing

Table 81. SD/eMMC4.3 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed) Push-pull	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode) Open-drain	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns

Table 81. SD/eMMC4.3 interface timing specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.8.4.2 eMMC4.4/4.41/SD3.0 (Dual Data Rate) AC timing)

Figure 45 depicts the timing of eMMC4.4/4.41/SD3.0. Table 82 lists the eMMC4.4/4.41/SD3.0 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

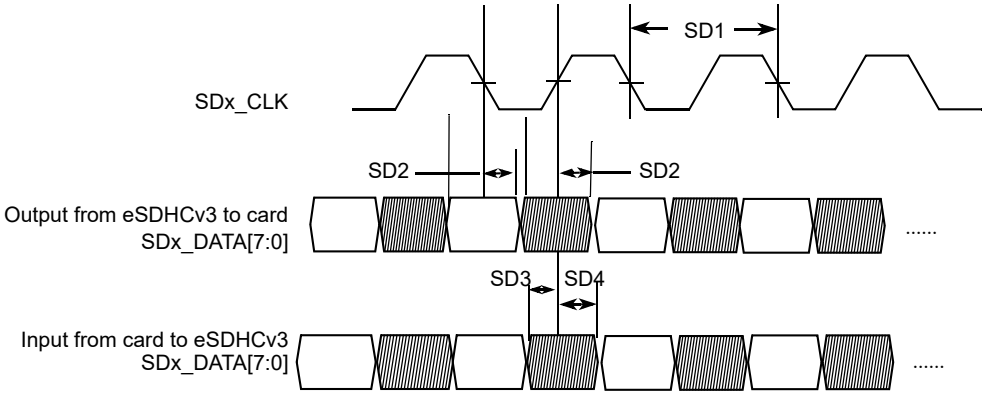


Figure 45. eMMC4.4/4.41/SD3.0 timing

Table 82. eMMC4.4/4.41/SD3.0 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.8	6.8	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.2	—	ns

4.8.4.3 SDR50/SDR104 AC timing

Figure 46 depicts the timing of SDR50/SDR104, and Table 83 lists the SDR50/SDR104 timing characteristics.

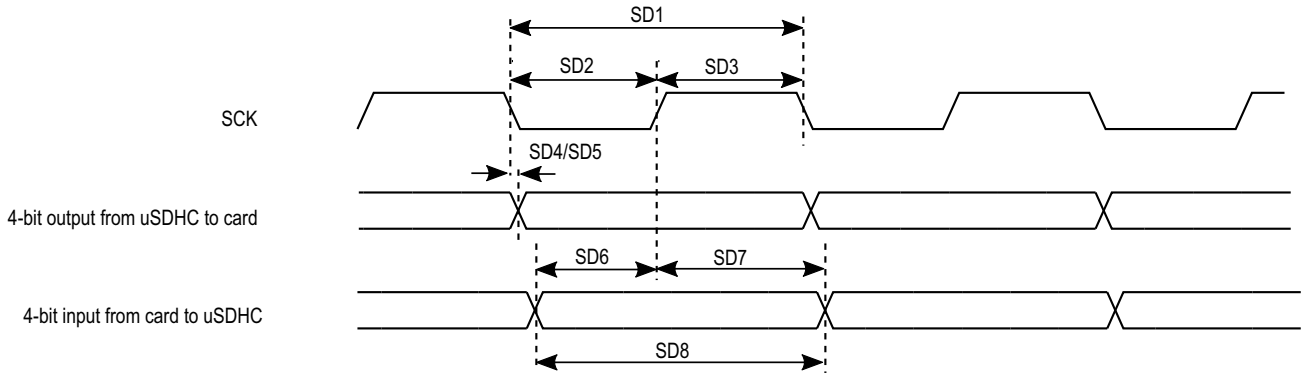


Figure 46. SDR50/SDR104 timing

Table 83. SDR50/SDR104 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]Data window in SDR104 mode is variable.

4.8.4.4 HS200 mode timing

Figure 47 depicts the timing of HS200 mode, and Table 84 lists the HS200 timing characteristics.

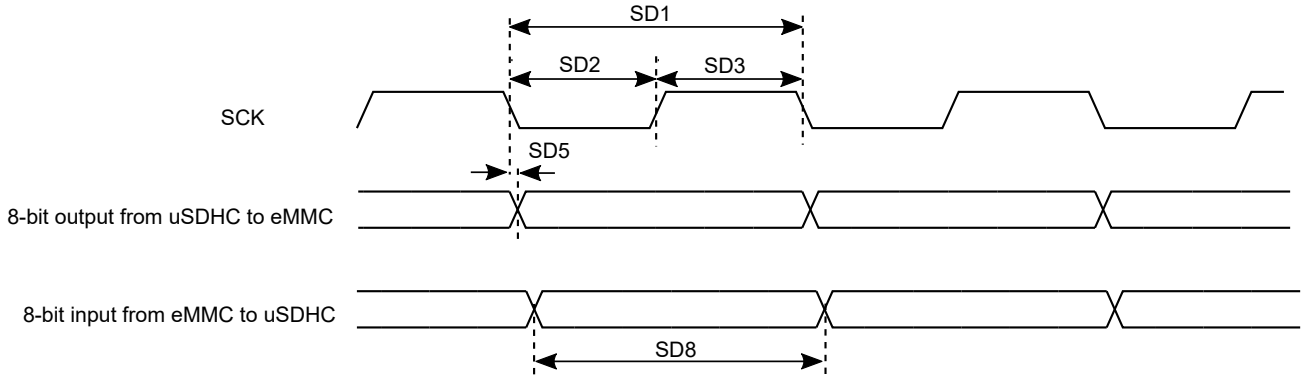


Figure 47. HS200 mode timing

Table 84. HS200 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]HS200 is for 8 bits while SDR104 is for 4 bits.

4.8.4.5 HS400 specifications - eMMC 5.0 only

Be aware that only data are sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for HS200 mode. Check SD5 and SD8 parameters in the HS200 interface timing specifications table for CMD input/output timing of HS400 mode.

Table 84 lists the HS400 timing characteristics.

Table 85. HS400 interface timing specification

Symbol	Description	Min	Max	Unit
	Operating voltage	1.71	1.95	V
Card input clock				
	Clock frequency	0	200	MHz
SD1	Clock period	5.0	—	ns
SD2	Clock Low time	0.46 x SD1	0.54 x SD1	ns
SD3	Clock High time	0.46 x SD1	0.54 x SD1	ns
SDHC output / card Inputs SDHC_CMD, SDHC_Dn (reference to SDHC_CLK)				
SD4	Output skew from data to edge of SCK	0.45	—	ns
SD5	Output skew from edge of SCK to data	0.45	—	ns
SDHC input / card outputs (reference to strobe)				
SD6	SDHC input skew	—	0.45	ns
SD7	SDHC hold skew	—	0.45	ns

Figure 47 depicts the timing of HS400.

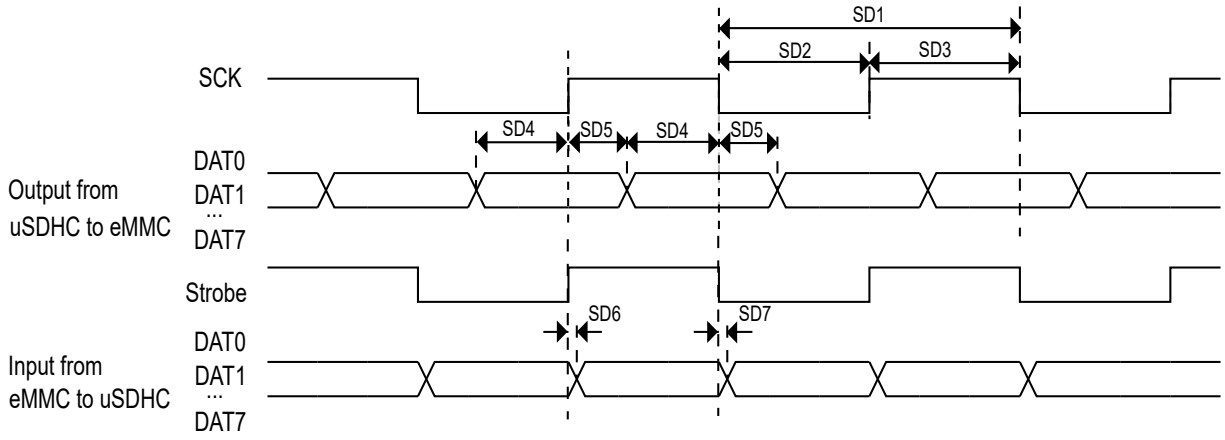


Figure 48. HS400 timing

4.8.4.6 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50/HS200/HS400 mode is 1.8 V.

4.8.5 Network AC electrical specifications

This section describes MII, RMII, RGMII, 1588 and management interface timing parameters.

4.8.5.1 ENET MII mode timing

Table 86 describes the MII timing parameters.

Table 86. MII timing Parameters

Symbol	Description	Min.	Typ	Max.	Unit	Condition	Spec number
tCYC_RX	RX_CLK period	—	40 / 400	—	ns	10/100 Mbps	—
∆tCYC_RX	RX_CLK duty cycle (tPWH / tCYC)	45	—	55	%	—	—
tS	Input setup time to RX_CLK[1]	5	—	—	ns	10/100 Mbps	—
tH	Input hold time to RX_CLK[1]	5	—	—	ns	10/100 Mbps	—
tCYC_TX	TX_CLK period[2]	—	40 / 400	—	ns	10/100 Mbps	—
∆tCYC_TX	TX_CLK duty cycle (tPWH / tCYC)[2]	45	—	55	%	—	—
tD	Output delay from TX_CLK[2]	2	—	25	ns	10/100 Mbps	—

1 Input timing assumes an input signal slew rate of 3 ns (20%/80%).

2 Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 Ohm, un-terminated, 5-inch microstrip trace on standard FR4 (1.5 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.

Figure 49 shows MII receive timing.

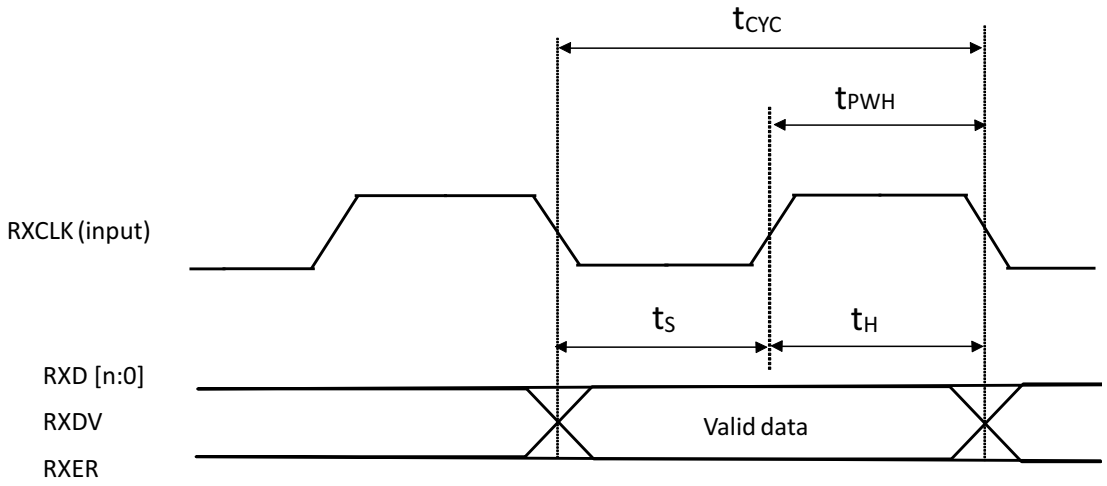


Figure 49. MII receive timing

Figure 50 shows MII transmit timing.

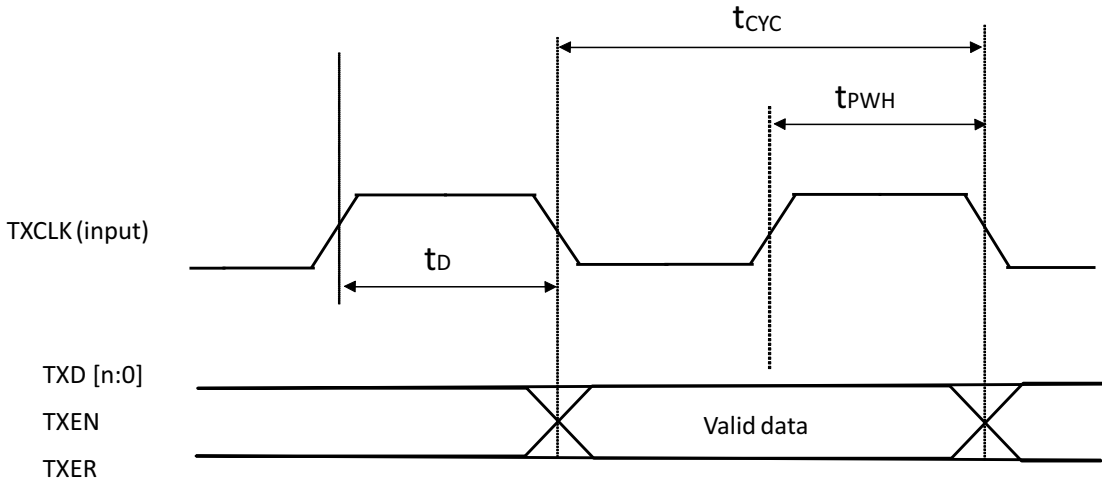


Figure 50. MII transmit timing

4.8.5.2 RMII mode timing

Table 87 describes the RMII timing parameters.

Table 87. RMII timing Parameters

Symbol	Description	Min.	Typ	Max.	Unit	Condition	Spec number
fRMII_CLK	RMII input clock frequency (RMII_CLK)	—	—	50	MHz	—	—
∆ tRMII_CLK	RMII_CLK duty cycle (tPWH / tCYC)	35	—	65	%	—	E3, E4, E7, E8
tS	RXD[1:0], CRS_DV, RXER to RMII_CLK setup time	4	—	—	ns	—	E1
tH	RMII_CLK to RXD[1:0], CRS_DV, RXER hold time[1]	2	—	—	ns	—	E2
tDATA_VALID	RMII_CLK to TXD[1:0], TXN data valid[2]	—	—	14	ns	CLOAD = 25 pF	E6
tDATA_INVALID	RMII_CLK to TXD[1:0], TXN data invalid[2]	2	—	—	ns	CLOAD = 25 pF	E5

1 Input timing assumes an input signal slew rate of 3 ns (20%/80%).

2 Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 Ohm, un-terminated, 5-inch microstrip trace on standard FR4 (1.5 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.

Figure 51 shows RMII receive timing.

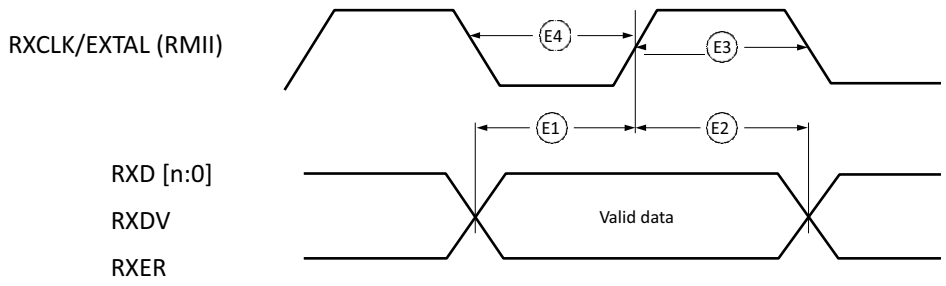


Figure 51. RMII receive timing

Figure 52 shows RMII transmit timing.

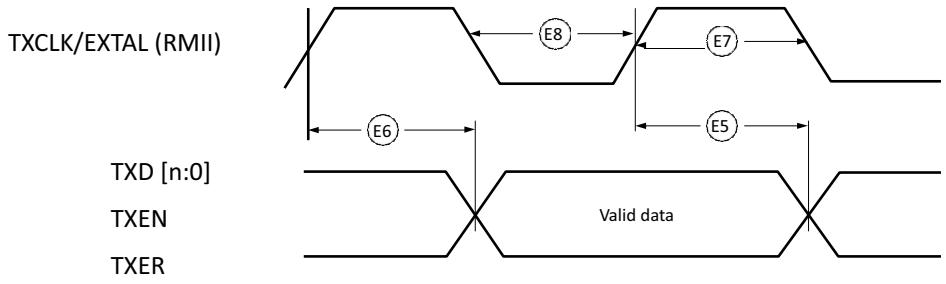


Figure 52. RMII transmit timing

4.8.5.3 RGMII mode specifications

Table 88 describes the RGMII timing parameters.

Table 88. RGMII timing Parameters

Symbol	Description	Min.	Typ	Max.	Unit	Condition	Spec number
T_{CYC}	Clock cycle duration[1,2,3,4]	7.2	—	8.8	ns	—	—
TskewT	Data to clock output skew (at transmitter)[2,3,4,5]	-500	—	500	ps	—	—
TskewR	Data to clock output skew (at receiver)[2,4,5]	1	—	2.6	ns	—	—
Duty_G	Clock duty cycle for Gigabit[2,4,6]	45	—	55	%	—	—
Duty_T	Clock duty cycle for 10/100T[2,4,6]	40	—	60	%	—	—

1 For 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

2 Measured as defined in EIA/JESD 8-6 1995 with a timing threshold voltage of VDDQ/2

3 Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 8 pF load at the end of a 50 Ω, un-terminated, 2 inch microstrip trace on standard FR4 (1.5 pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.

4 RGMII timing specifications are valid for both 1.8 V and 3.3 V nominal I/O pad supply voltage.

5 For all versions prior to RGMII v2.0 specifications; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.5 ns and less than 2 ns will be added to the associated clock signal. For 10/100,the max value is unspecified.

6 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

Figure 53 shows RGMII receive timing.

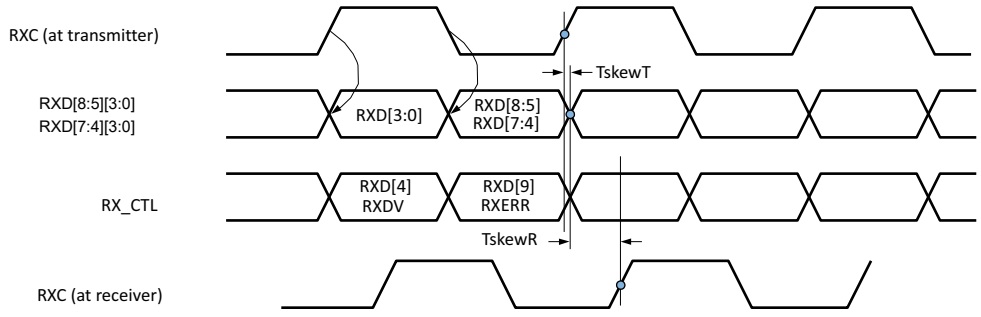


Figure 53. RGMII receive timing

Figure 54 shows RGMII transmit timing.

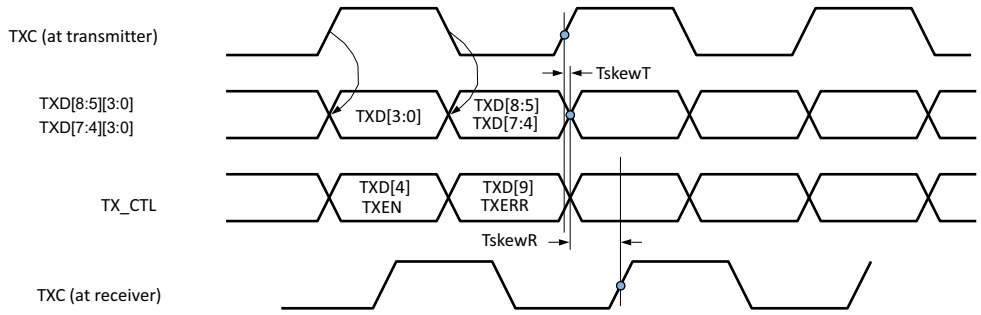


Figure 54. RGMII transmit timing

4.8.5.4 NETC 1588 specifications

Table 89 describes the NETC 1588 timing parameters.

Table 89. NETC 1588 timing Parameters

Symbol	Description	Min.	Typ	Max.	Unit	Condition	Spec number
tT1588CLK	TMR_1588_CLK_IN clock period	5	—	—	ns	—	—
tT1588CLKL/ tT1588CLK	TMR_1588_CLK_IN duty cycle	40	50	60	%	—	—
tT1588CLKINJ	TMR_1588_CLK_IN peak-to-peak jitter	—	—	250	ps	—	—
tT1588CLKINR	Rise time TMR_1588_CLK_IN (20% to 80%)	1.0	—	2.0	ns	—	—
tT1588CLKINF	Fall time TMR_1588_CLK_IN (80% to 20%)	1.0	—	2.0	ns	—	—
tT1588CLKOUT	TMR_1588_CLK_OUT clock period	2 x t1588CLK	—	—	ns	—	—
tT1588CLKOTH/ tT1588CLKOUT	TMR_1588_CLK_OUT duty cycle	30.0	50.0	70.0	%	—	—
tT1588TRIGH	TMR_1588_TRIG_IN1/2 pulse width	2 x t1588CLK	—	—	ns	—	—

Figure 55 shows NETC 1588 input AC timing.

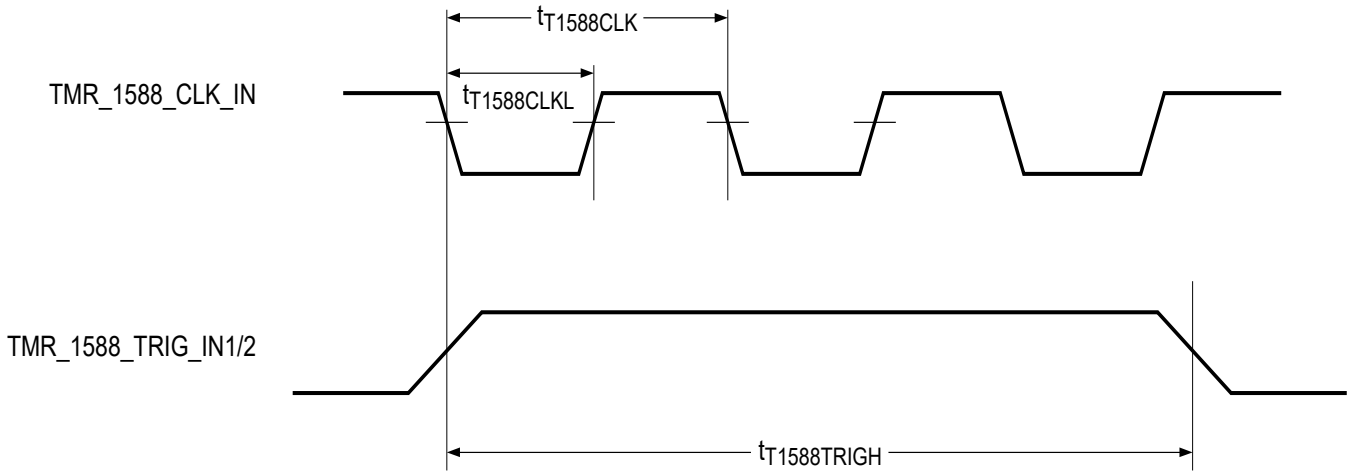
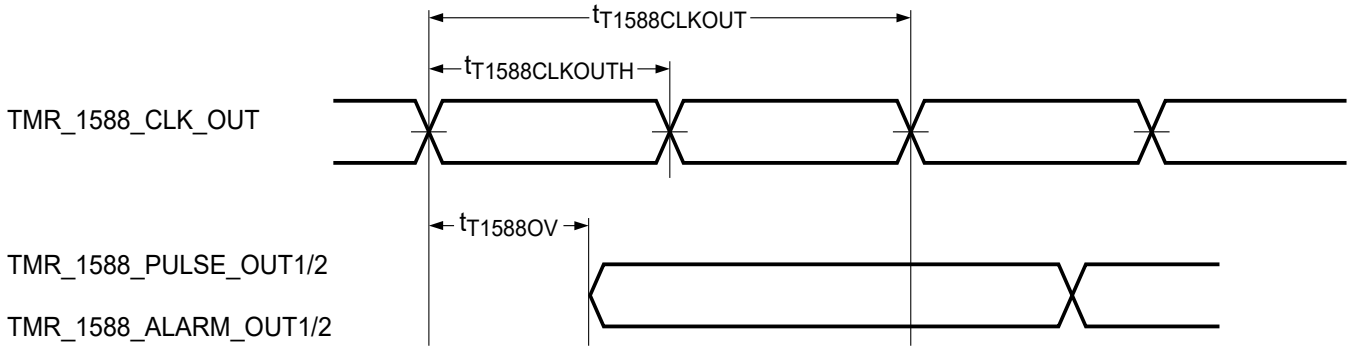


Figure 55. IEEE 1588 input AC timing

Figure 56 shows NETC 1588 output AC timing.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 56. IEEE 1588 output AC timing

4.8.5.5 NETC management specifications

Table 90 describes the NETC management timing parameters.

Table 90. NETC management timing Parameters

Symbol	Description	Min.	Typ	Max.	Unit	Condition	Spec number
fMDC	MDC clock frequency	—	—	5	MHz	—	—
MDIO_CH	MDC pulse width high time	40	—	60	%	—	MDC14
MDIO_CL	MDC pulse width low time	40	—	60	%	—	MDC15
tMDKHDX	MDC to MDIO dalay[1]	(Y + 5) x tenet_clk - 4	—	(Y + 5) x tenet_clk + 4	ns	—	—
MDIO_ISU	MDIO (input) to MDC rising edge setup time	8	—	—	ns	—	MDC12
MDIO_IH	MDIO (input) to MDC rising edge hold time	0	—	—	ns	—	MDC13

[1] tenet_clk is NETC system clock. Y is the value programmed to adjust hold time by EMDIO_CFG[MDIO_HOLD].

Figure 55 shows MDC / MDIO timing.

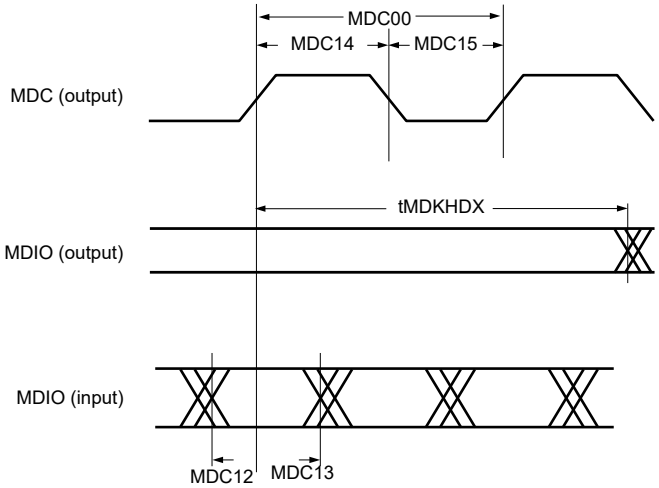


Figure 57. MDC / MDIO timing

4.8.5.6 Ethernet Time Sensitive Networking (TSN) electrical specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

It also supports the following TSN features:

- 802.1AS Timing and Synchronization
- 802.1CB (switch only) Frame Replication and Elimination for Reliability (FRER)
- 802.1Qav Forwarding and Queuing Enhancements for Time Sensitive Streams
- 802.1Qbu Frame preemption

- 802.1Qbv Enhancements to Scheduling Traffic
- 802.1Qch Cyclic Queuing and Forwarding (CQF)
- 802.1Qci Per Stream Filtering and Policing (PSFP)
- Time based Scheduling

4.8.5.7 EtherCAT

4.8.5.7.1 ENET MII mode timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.8.5.7.2 MII receive signal timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 58 shows MII receive signal timings. Table 91 describes the timing parameters (M1–M4) shown in the figure.

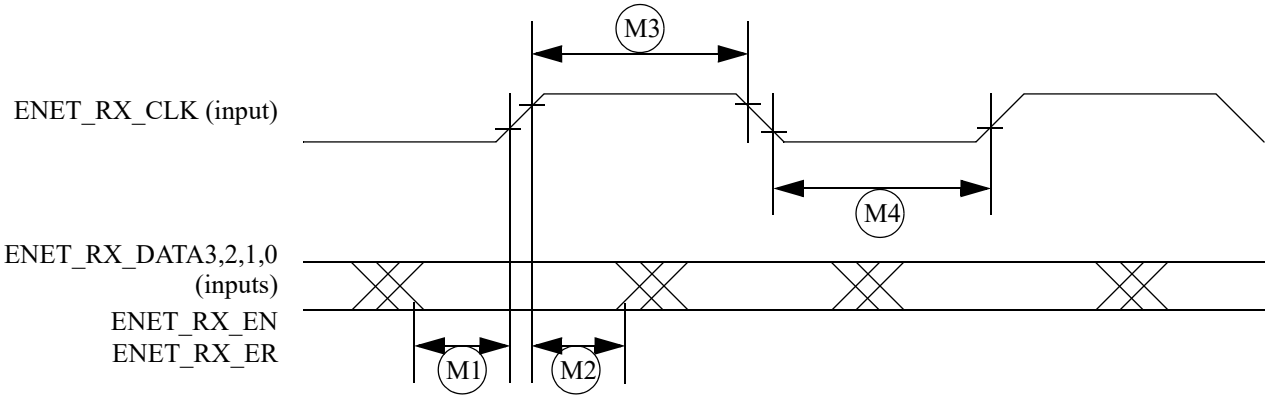


Figure 58. MII receive signal timing diagram

Table 91. MII receive signal timing

ID	Characteristic[1]	Min.	Max.	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.8.5.7.3 MII transmit signal timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 59 shows MII transmit signal timings. Table 92 describes the timing parameters (M5–M8) shown in the figure.

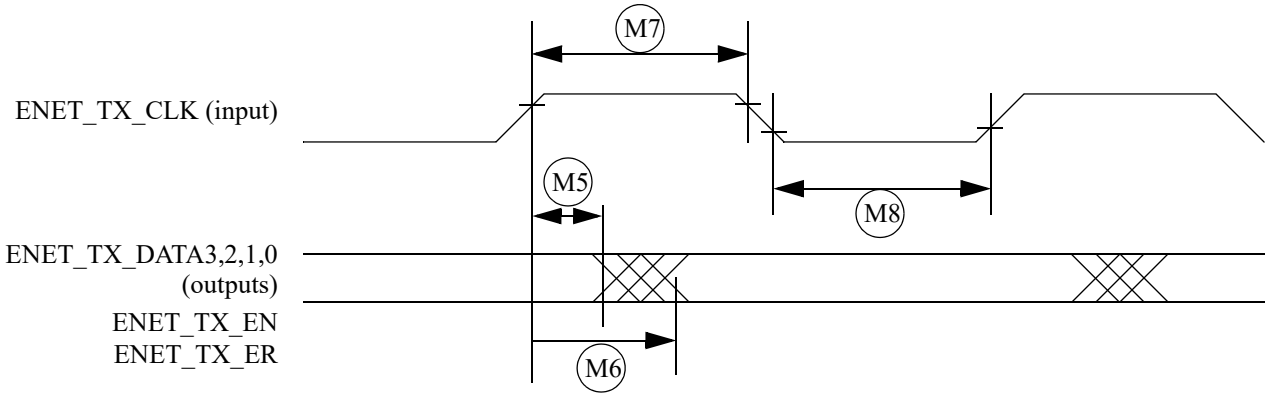


Figure 59. MII transmit signal timing diagram

Table 92. MII transmit signal timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.8.5.7.4 MII asynchronous inputs signal timing (ENET_CRS and ENET_COL)

Figure 60 shows MII asynchronous inputs timings. Table 93 describes the timing parameter (M9) shown in the figure.

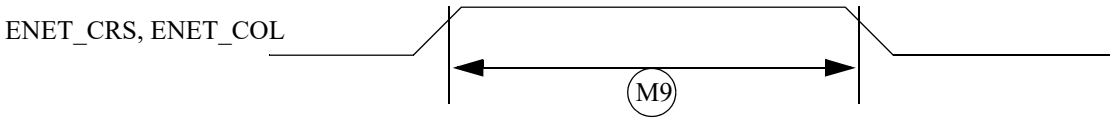


Figure 60. MII asynchronous inputs timing diagram

Table 93. MII asynchronous inputs signal timing

ID	Characteristic	Min.	Max.	Unit
M9	ENET_CRS and ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

4.8.5.7.5 MII serial management channel timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 61 shows MII serial management channel timings. Table 94 describes the timing parameters (M10–M15) shown in the figure.

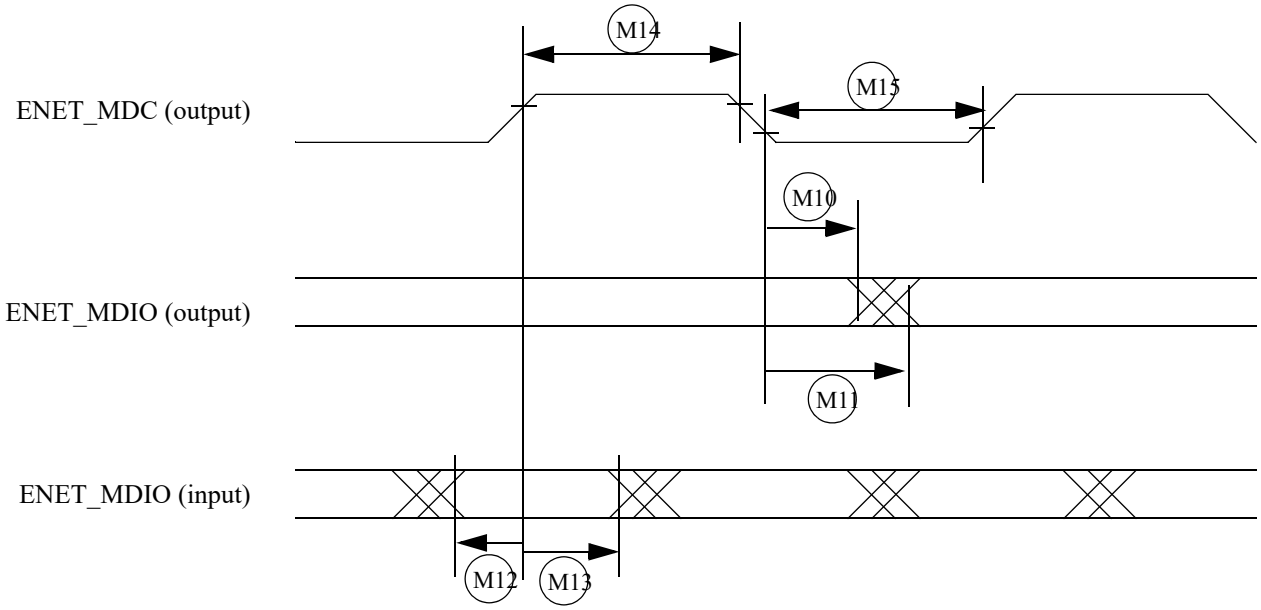


Figure 61. MII serial management channel timing diagram

Table 94. MII serial management channel timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.8.5.8 RMII mode timing

Please refer to Section 4.8.5.2, RMII mode timing.

4.8.6 Controller Area Network (CAN) AC electrical specifications

The Controller Area Network (CAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification. See the IOMUXC chapter of the device reference manual to see which pins expose Tx and Rx pins; these ports are named CAN_TX and CAN_RX, respectively.

Please refer to Section 4.3.2.1, General purpose I/O (GPIO) AC parameters.

4.8.7 LPUART electrical specifications

Please refer to Section 4.3.2.1, General purpose I/O (GPIO) AC parameters.

4.8.8 GPIO electrical specifications

Please refer to Section 4.3.2.1, General purpose I/O (GPIO) AC parameters.

4.8.9 Flexible IO controller (FlexIO) electrical specifications

Table 95 shows FlexIO timing specifications.

Table 95. FlexIO timing specifications

Symbol	Descriptions	Min	Typ	Max	Unit	Notes
t_{ODS}	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle	0	—	10	ns	1
t_{IDS}	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle	0	—	10	ns	1

1 Assume pins muxed on same VDD_IO domain with same load.

4.8.10 USB PHY parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG with the following amendments.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000

- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only

4.9 Timers

This section provide information on timers.

4.9.1 Pulse Width Modulator (PWM) characteristics

This section describes the electrical information of the PWM.

Table 96. PWM timing parameters

Parameter	Min	Typ	Max	Unit
PWM Clock Frequency	—	—	133	MHz
Output skew	—	—	2	ns

4.9.2 Quad Timer timing

Table 97 lists the Quad Timer parameters.

Table 97. Quad Timer timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Maximum frequency	f	—	133	MHz	—
Timer input period	T_{IN}	$2T^{1} + 6$	—	ns	—
Timer input high/low period	T_{INHL}	1T + 3	—	ns	—
Timer output period	T_{OUT}	30	—	ns	—
Timer output high/low period	T_{OUTHL}	15	—	ns	—

1 T = 1000/f

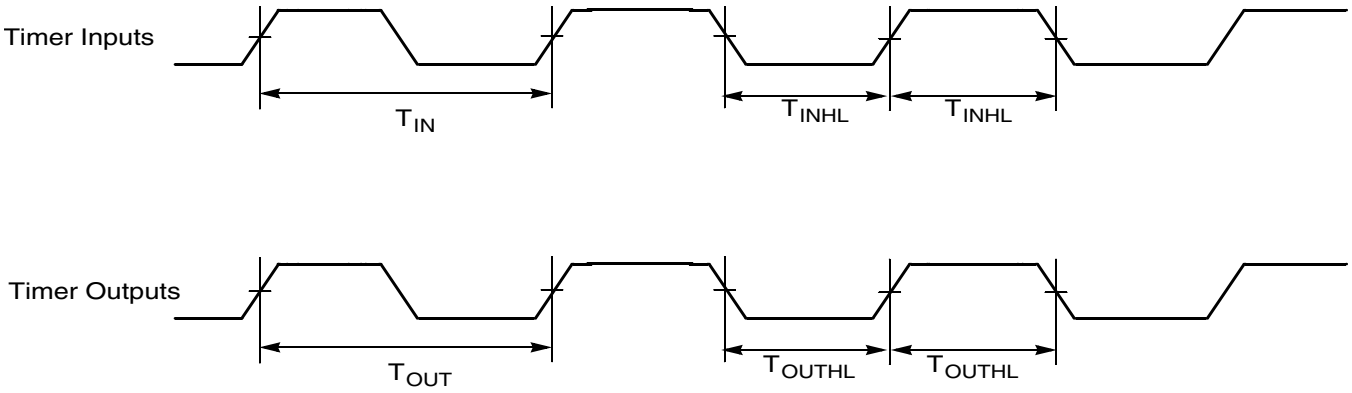


Figure 62. TMR timing

4.9.3 LPTMR characteristics

This section describes the characteristics of LPTMR.

Table 98. LPTMR timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Clock Frequency	f	—	—	80	MHz

4.10 BBSM

This section provides parameters of BBSM.

4.10.1 BBSM tamper

Table 99 lists the DC specification of BBSM tamper.

Table 99. DC specification of BBSM tamper

Parameter	Symbol	Min	Typ[1]	Max	Unit	Condition
High level input voltage	V_{IH}	0.7 x NVCC_BBSM	—	NVCC_BBSM + 0.1	V	—
Low level input voltage	V_{IL}	-0.3	—	0.3 x NVCC_BBSM	V	—
Output high current	I_{OH}	—	-45	—	μA	V_{OH} = NVCC_BBSM - 0.3
Output low current	I_{OL}	—	50	—	μA	V_{OL} = 0.3
Weak pull-up and pull-down						
Pull-up and pull-down resistance	R_{PU}/ R_{PD}	—	200	—	kΩ	—

1 Typical numbers are not guaranteed.

Table 100 lists the BBSM tamper specifications.

Table 100. BBSM tamper specifications

Parameters	Min	Typ	Max	Unit
High Temp Tamper	125	130	135	°C
Low Temp Tamper	-40	-30	-20	°C
Low Temp Tamper (Shelf mode)	-60	-50	-40	°C
Vbat LVD tamper	2.25	2.325	2.4	V
Vbat HVD tamper	4.25	4.375	4.5	V
Regulator LVD tamper	1.48	1.58	1.68	V
Regulator HVD tamper	1.86	1.96	2.06	V
Clock low freq tamper	15	20	25	kHz
Clock high freq tamper	40	52.5	80	kHz

5 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot mode configuration pins

Table 101 implements a compressed boot mode decode with 3 BOOT_MODE pins.

Table 101. Boot_MODE definition

BOOT_MODE[2:0]	Boot type
000	Boot from Internal Fuses
001	Serial Downloader
010	eMMC 8-bit via uSDHC2[1]
011	SD 4-bit via uSDHC[1]
100	Serial NOR Flash with JESD216 via FlexSPI1, Primary group, PortA[2]
101	Serial NAND Flash with 2K page via FlexSPI1, Primary group, PortA[2]
110	Infinite Loop Modes
111	Test mode[3]

1 Boot device, instance and bus width are fixed. The other options can be set by the values in the BOOT_CFG fuse words.

2 Boot device is fixed. The other options can be overwritten by the values in the BOOT_CFG fuse words, including instance, pin group, port, etc.

3 Test Mode is reserved for NXP usage only.

When booting from Internal Fuses, additional boot options are also supported:

- All boot modes supported for a range of speeds/timings/protocol formats
- eMMC and SD boot supported from any USDHC instance 1, 2 or 3 (if USDHC3 present in a given SoC)
- Serial NOR boot supported for 1-bit, 4-bit, and 8-bit mode
- Serial NAND boot supported for 1-bit, 4-bit, and 8-bit mode (8-bit Serial NAND)
- Assorted additional minor parameter options.

BOOT_MODE pins are multiplexed over other functional pins. The functional IO that are multiplexed with these pins must be selected subject to two criteria:

- Functional IO must not be used if they are inputs to the SoC which could potentially be constantly driven by external components. Such functional mode driving may interfere with the need for the board to pull these pins a certain way while POR is asserted.
- Functional IO must not be used if they are outputs of the SoC which will be connected to components on the board that may misinterpret the signals as valid signals if they toggle (such as when the board drives them while POR is asserted). Examples in this category include chip selects to memory devices that may be output of the SoC.

For detailed boot mode options configured by the boot mode pins, see the i.MX RT1180 Fuse Map and the System Boot chapter in *i.MX RT1180 Reference Manual (IMXRT1180RM)*.

5.2 Boot device interface allocation

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 102. Boot through NAND

PAD Name	IO Function	ALT	Comments
GPIO_EMC_B1_00	semc.DATA[0]	ALT 0	—
GPIO_EMC_B1_01	semc.DATA[1]	ALT 0	—
GPIO_EMC_B1_02	semc.DATA[2]	ALT 0	—
GPIO_EMC_B1_03	semc.DATA[3]	ALT 0	—
GPIO_EMC_B1_04	semc.DATA[4]	ALT 0	—
GPIO_EMC_B1_05	semc.DATA[5]	ALT 0	—
GPIO_EMC_B1_06	semc.DATA[6]	ALT 0	—
GPIO_EMC_B1_07	semc.DATA[7]	ALT 0	—
GPIO_EMC_B1_30	semc.DATA[8]	ALT 0	—
GPIO_EMC_B1_31	semc.DATA[9]	ALT 0	—
GPIO_EMC_B1_32	semc.DATA[10]	ALT 0	—
GPIO_EMC_B1_33	semc.DATA[11]	ALT 0	—
GPIO_EMC_B1_34	semc.DATA[12]	ALT 0	—
GPIO_EMC_B1_35	semc.DATA[13]	ALT 0	—
GPIO_EMC_B1_36	semc.DATA[14]	ALT 0	—
GPIO_EMC_B1_37	semc.DATA[15]	ALT 0	—
GPIO_EMC_B1_18	semc.ADDR[9]	ALT 0	—
GPIO_EMC_B1_19	semc.ADDR[11]	ALT 0	—
GPIO_EMC_B1_20	semc.ADDR[12]	ALT 0	—
GPIO_EMC_B1_22	semc.BA1	ALT 0	—
GPIO_EMC_B1_41	semc.CSX[0]	ALT 0	—
GPIO_B1_00	semc.CSX[1]	ALT 2	—
GPIO_B1_01	semc.CSX[2]	ALT 2	—
GPIO_B2_00	semc.CSX[3]	ALT 1	—

Table 103. Boot through FlexSPI1 (QSPI/HyperFLASH)

PAD Name	IO Function	ALT	Comments
GPIO_SD_B2_00	flexspi1_bus2bit.B_DATA[4]	ALT 1	Port B Group 0
GPIO_SD_B2_01	flexspi1_bus2bit.B_DATA[5]	ALT 1	
GPIO_SD_B2_02	flexspi1_bus2bit.B_DATA[6]	ALT 1	
GPIO_SD_B2_03	flexspi1_bus2bit.B_DATA[7]	ALT 1	
GPIO_SD_B2_04	flexspi1_bus2bit.B_SS1_B	ALT 1	
GPIO_SD_B2_05	flexspi1_bus2bit.B_DQS	ALT 1	
GPIO_SD_B2_06	flexspi1_bus2bit.B_SS0_B	ALT 1	
GPIO_SD_B2_07	flexspi1_bus2bit.B_SCLK	ALT 1	
GPIO_SD_B2_08	flexspi1_bus2bit.B_DATA[0]	ALT 1	
GPIO_SD_B2_09	flexspi1_bus2bit.B_DATA[1]	ALT 1	
GPIO_SD_B2_10	flexspi1_bus2bit.B_DATA[2]	ALT 1	
GPIO_SD_B2_11	flexspi1_bus2bit.B_DATA[3]	ALT 1	
GPIO_B2_03	flexspi1_bus2bit.A_DATA[4]	ALT 7	Port A
GPIO_B2_04	flexspi1_bus2bit.A_DATA[5]	ALT 7	
GPIO_B2_05	flexspi1_bus2bit.A_DATA[6]	ALT 7	
GPIO_B2_06	flexspi1_bus2bit.A_DATA[7]	ALT 7	
GPIO_B2_07	flexspi1_bus2bit.A_DQS	ALT 7	
GPIO_B2_02	flexspi1_bus2bit.A_SCLK_B	ALT 6	
GPIO_B2_08	flexspi1_bus2bit.A_SCLK	ALT 7	
GPIO_B2_01	flexspi1_bus2bit.A_SS1_B	ALT 6	
GPIO_B2_09	flexspi1_bus2bit.A_SS0_B	ALT 7	
GPIO_B2_10	flexspi1_bus2bit.A_DATA[0]	ALT 7	
GPIO_B2_11	flexspi1_bus2bit.A_DATA[1]	ALT 7	
GPIO_B2_12	flexspi1_bus2bit.A_DATA[2]	ALT 7	
GPIO_B2_13	flexspi1_bus2bit.A_DATA[3]	ALT 7	
GPIO_SD_B2_12_DUMMY	flexspi1_bus2bit.A_DQS	ALT 0	Secondary option
GPIO_SD_B2_12_DUMMY	flexspi1_bus2bit.B_DQS	ALT 1	Secondary option

Table 103. Boot through FlexSPI1 (QSPI/HyperFLASH) (continued)

PAD Name	IO Function	ALT	Comments
GPIO_B1_04	flexspi1_bus2bit.B_SS0_B	ALT 7	Port B Group 1
GPIO_B1_02	flexspi1_bus2bit.B_SS1_B	ALT 7	
GPIO_B1_05	flexspi1_bus2bit.B_SCLK	ALT 7	
GPIO_B1_03	flexspi1_bus2bit.B_DQS	ALT 7	
GPIO_B1_10	flexspi1_bus2bit.B_DATA[3]	ALT 7	
GPIO_B1_11	flexspi1_bus2bit.B_DATA[2]	ALT 7	
GPIO_B1_12	flexspi1_bus2bit.B_DATA[1]	ALT 7	
GPIO_B1_13	flexspi1_bus2bit.B_DATA[0]	ALT 7	
GPIO_B1_09	flexspi1_bus2bit.B_DATA[4]	ALT 7	
GPIO_B1_08	flexspi1_bus2bit.B_DATA[5]	ALT 7	
GPIO_B1_07	flexspi1_bus2bit.B_DATA[6]	ALT 7	
GPIO_B1_06	flexspi1_bus2bit.B_DATA[7]	ALT 7	

Table 104. Boot through FlexSPI2

PAD Name	IO Function	ALT	Comments
GPIO_EMC_B1_35	flexspi2_bus2bit.A_DATA[0]	ALT 3	Port A Group 1
GPIO_EMC_B1_36	flexspi2_bus2bit.A_DATA[1]	ALT 3	
GPIO_EMC_B1_37	flexspi2_bus2bit.A_DATA[2]	ALT 3	
GPIO_EMC_B1_38	flexspi2_bus2bit.A_DATA[3]	ALT 3	
GPIO_EMC_B1_39	flexspi2_bus2bit.A_SS0_B	ALT 3	
GPIO_EMC_B1_40	flexspi2_bus2bit.A_DQS	ALT 3	
GPIO_EMC_B1_41	flexspi2_bus2bit.A_SCLK	ALT 3	
GPIO_EMC_B1_26	flexspi2_bus2bit.A_SS1_B	ALT 3	
GPIO_AON_28_DUMMY	flexspi2_bus2bit.A_DQS	ALT 0	Secondary option
GPIO_AON_21	flexspi2_bus2bit.A_DQS	ALT 8	Port A Group 0
GPIO_AON_20	flexspi2_bus2bit.A_SS1_B	ALT 1	
GPIO_AON_22	flexspi2_bus2bit.A_SS0_B	ALT 0	
GPIO_AON_23	flexspi2_bus2bit.A_SCLK	ALT 0	
GPIO_AON_24	flexspi2_bus2bit.A_DATA[0]	ALT 0	
GPIO_AON_25	flexspi2_bus2bit.A_DATA[1]	ALT 0	
GPIO_AON_26	flexspi2_bus2bit.A_DATA[2]	ALT 0	
GPIO_AON_27	flexspi2_bus2bit.A_DATA[3]	ALT 0	

Table 104. Boot through FlexSPI2 (continued)

PAD Name	IO Function	ALT	Comments
GPIO_AON_18	flexspi2_bus2bit.B_DATA[0]	ALT 0	Port B Group 0
GPIO_AON_17	flexspi2_bus2bit.B_DATA[1]	ALT 0	
GPIO_AON_16	flexspi2_bus2bit.B_DATA[2]	ALT 0	
GPIO_AON_15	flexspi2_bus2bit.B_DATA[3]	ALT 0	
GPIO_AON_21	flexspi2_bus2bit.B_SS0_B	ALT0	
GPIO_AON_20	flexspi2_bus2bit.B_DQS	ALT0	
GPIO_AON_19	flexspi2_bus2bit.B_SCLK	ALT0	
GPIO_EMC_B1_33	flexspi2_bus2bit.B_DATA[0]	ALT 3	Port B Group 1
GPIO_EMC_B1_32	flexspi2_bus2bit.B_DATA[1]	ALT 3	
GPIO_EMC_B1_31	flexspi2_bus2bit.B_DATA[2]	ALT 3	
GPIO_EMC_B1_30	flexspi2_bus2bit.B_DATA[3]	ALT 3	
GPIO_EMC_B1_28	flexspi2_bus2bit.B_SS0_B	ALT 3	
GPIO_EMC_B1_29	flexspi2_bus2bit.B_DQS	ALT 3	
GPIO_EMC_B1_34	flexspi2_bus2bit.B_SCLK	ALT 3	
GPIO_EMC_B1_27	flexspi2_bus2bit.B_SS1_B	ALT 3	
GPIO_AON_28_DUMMY	flexspi2_bus2bit.B_DQS	ALT 1	Secondary option

Table 105. Boot through FlexSPI reset

PAD Name	IO Function	ALT	Comments
GPIO_SD_B1_00	gpio5.IO[4]	ALT 5	—
GPIO_EMC_B1_40	gpio3.IO[8]	ALT 5	—

Table 106. Boot through SPI-1

PAD Name	IO Function	ALT	Comments
GPIO_AON_04	lpspi1.SCK	ALT 0	—
GPIO_AON_05	lpspi1.PCS0	ALT 0	—
GPIO_AON_06	lpspi1.SDO	ALT 0	Recovery boot: SIO0
GPIO_AON_07	lpspi1.SDI	ALT 0	Recovery boot: SIO1
GPIO_AON_09	lpspi1.PCS2	ALT 8	Recovery boot: SIO2
GPIO_AON_03	lpspi1.PCS3	ALT 4	Recovery boot: SIO3, Serial: nIRQ

Table 107. Boot through SPI-2

PAD Name	IO Function	ALT	Comments
GPIO_AON_22	lpspi2.SCK	ALT 6	—
GPIO_AON_25	lpspi2.PCS0	ALT 6	—
GPIO_AON_23	lpspi2.SDO	ALT 6	—
GPIO_AON_24	lpspi2.SDI	ALT 6	—
GPIO_AON_26	lpspi2.PCS2	ALT 1	—
GPIO_AON_27	lpspi2.PCS3	ALT 1	—

Table 108. Boot through SPI-4

PAD Name	IO Function	ALT	Comments
GPIO_SD_B2_08	lpspi4.SCK	ALT 4	—
GPIO_SD_B2_09	lpspi4.PCS0	ALT 4	—
GPIO_SD_B2_10	lpspi4.SDO	ALT 4	—
GPIO_SD_B2_11	lpspi4.SDI	ALT 4	—
GPIO_SD_B2_06	lpspi4.PCS2	ALT 4	—
GPIO_SD_B2_05	lpspi4.PCS3	ALT 4	—

Table 109. Boot through SPI-5

PAD Name	IO Function	ALT	Comments
GPIO_AD_28	lpspi5.SCK	ALT 0	—
GPIO_AD_29	lpspi5.PCS0	ALT 0	—
GPIO_AD_30	lpspi5.SDO	ALT 0	—
GPIO_AD_31	lpspi5.SDI	ALT 0	—
GPIO_AD_26	lpspi5.PCS2	ALT 2	—
GPIO_AD_25	lpspi5.PCS3	ALT 2	—

Table 110. Boot through SD1

PAD Name	IO Function	ALT	Comments
GPIO_AD_32	usdhc1.CD_B	ALT 4	—
GPIO_AD_33	usdhc1.WP	ALT 4	—

Table 110. Boot through SD1 (continued)

GPIO_AD_34	usdhc1.VSELECT	ALT 4	—
GPIO_AD_35	usdhc1.RESET_B	ALT 4	—
GPIO_SD_B1_00	usdhc1.CMD	ALT 0	—
GPIO_SD_B1_01	usdhc1.CLK	ALT 0	—
GPIO_SD_B1_02	usdhc1.DATA0	ALT 0	—
GPIO_SD_B1_03	usdhc1.DATA1	ALT 0	—
GPIO_SD_B1_04	usdhc1.DATA2	ALT 0	—
GPIO_SD_B1_05	usdhc1.DATA3	ALT 0	—

Table 111. Boot through SD2

PAD Name	IO Function	ALT	Comments
GPIO_AD_26	usdhc2.CD_B	ALT 9	—
GPIO_AD_27	usdhc2.WP	ALT 9	—
GPIO_AD_29	usdhc2.VSELECT	ALT 9	—
GPIO_SD_B2_00	usdhc2.DATA3	ALT 0	—
GPIO_SD_B2_01	usdhc2.DATA2	ALT 0	—
GPIO_SD_B2_02	usdhc2.DATA1	ALT 0	—
GPIO_SD_B2_03	usdhc2.DATA0	ALT 0	—
GPIO_SD_B2_04	usdhc2.CLK	ALT 0	—
GPIO_SD_B2_05	usdhc2.CMD	ALT 0	—
GPIO_SD_B2_06	usdhc2.RESET_B	ALT 0	—
GPIO_SD_B2_08	usdhc2.DATA4	ALT 0	—
GPIO_SD_B2_09	usdhc2.DATA5	ALT 0	—
GPIO_SD_B2_10	usdhc2.DATA6	ALT 0	—
GPIO_SD_B2_11	usdhc2.DATA7	ALT 0	—

Table 112. Boot through UART1

PAD Name	IO Function	ALT	Comments
GPIO_AON_08	lpuart1.TX	ALT 0	—
GPIO_AON_09	lpuart1.RX	ALT 0	—

Table 113. Boot failure indicators

PAD Name	IO Function	ALT	Comments
GPIO_AD_00	gpio4.IO[0]	ALT 5	—
GPIO_AD_01	gpio4.IO[1]	ALT 5	—
GPIO_AD_02	gpio4.IO[2]	ALT 5	—
GPIO_AD_03	gpio4.IO[3]	ALT 5	—
GPIO_AD_04	gpio4.IO[4]	ALT 5	—
GPIO_AD_05	gpio4.IO[5]	ALT 5	—
GPIO_AD_06	gpio4.IO[6]	ALT 5	—
GPIO_AD_07	gpio4.IO[7]	ALT 5	—
GPIO_AD_08	gpio4.IO[8]	ALT 5	—
GPIO_AD_09	gpio4.IO[9]	ALT 5	—
GPIO_AD_10	gpio4.IO[10]	ALT 5	—
GPIO_AD_11	gpio4.IO[11]	ALT 5	—
GPIO_B1_00	gpio6.IO[0]	ALT 5	—
GPIO_B1_01	gpio6.IO[1]	ALT 5	—
GPIO_B2_00	gpio6.IO[14]	ALT 5	—
GPIO_AD_33	gpio5.IO[1]	ALT 5	—

6 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 14 x 14 mm package information

6.1.1 14 x 14 mm, 0.8 mm pitch, ball matrix

Figure 63 shows the top, bottom, and side views of the 14 x 14 mm MAPBGA package.

MAPBGA–289 I/O
14 X 14 X 1.37 PKG, 0.8 PITCH

SOT1534–4

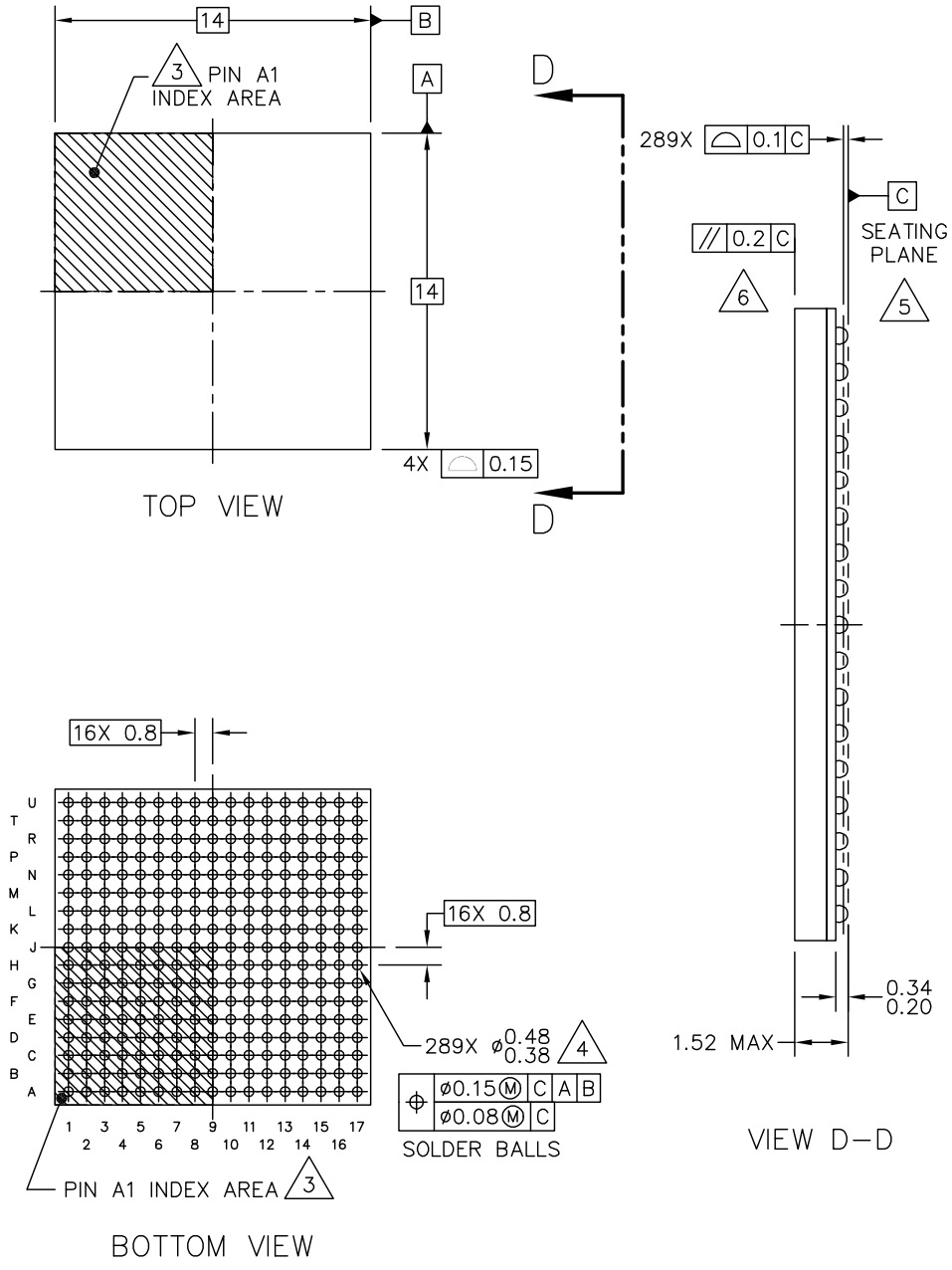


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Figure 63. 14 x 14 mm BGA, case x package top, bottom, and side Views

6.1.2 14 x 14 mm supplies contact assignments and functional contact assignments

Table 114 shows the device connection list for ground, sense, and reference contact signals.

Table 114. 14 x 14 mm supplies contact assignment

Supply Rail Name	Ball(s) Position(s)	Remark
ADC_VREFH	H16	—
DCDC_1P8	M4	—
DCDC_IN	M5, M6, M7, M8	—
DCDC_IN_Q	L7	—
DCDC_GND	K6, K7, K8, K9	—
DCDC_LP	T1. T2, T3, U2, U3	—
DCDC_MODE	L6	—
DCDC_PSWITCH	L5	—
DCDC_SENSE	L8	—
NVCC_AON	F7	—
NVCC_BBSM	U11	—
NVCC_EMC1	J5, J6, K5	—
NVCC_EMC2	N6, N7	—
NVCC_GPIO1	D11, E11	—
NVCC_GPIO2	F9, F10	—
NVCC_GPIO_AD	L12, M11	—
NVCC_SD1	C13	—
NVCC_SD2	H12, H13	—
VDD_AON_ANA	P12	—
VDD_AON_DIG	P11	—
VDD_AON_IN	U14	—
VDD_BBSM_ANA	R12	—
VDD_BBSM_IN	U12	—
VDD_SOC	H8, H9, H10, J8, J9, J10, K10	—
VDD_USB_1P8	B17	—
VDD_USB_3P3	G12	—
VDDA_1P0	N11	—
VDDA_1P8_IN	M12	—
VDDA_ADC_1P8	J13	—

Table 114. 14 x 14 mm supplies contact assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDDA_ADC_3P3	J14	—
VSS	A1, A17, C11, C14, D4, D7, D8, D12, F11, F12, F13, G4, G7, G8, G9, G10, G11, G14, H7, H11, J7, J11, K11, L4, L10, L11, L14, P3, P4, P7, P14, T12, U1, U17	—

Table 115 shows an alpha-sorted list of functional contact assignments of the 14 x 14 mm package.

Table 115. 14 x 14 mm functional contact assignment

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
CLK1_N	T15	—	—	—	—	—	—
CLK1_P	U15	—	—	—	—	—	—
DAC_OUT	J12	—	—	—	—	—	—
GPIO_AD_00	N12	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO00	Input	Pull Down
GPIO_AD_01	R14	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO01	Input	Pull Down
GPIO_AD_02	R13	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO02	Input	Pull Down
GPIO_AD_03	R15	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO03	Input	Pull Down
GPIO_AD_04	P15	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO04	Input	Pull Down
GPIO_AD_05	P13	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO05	Input	Pull Down
GPIO_AD_06	N13	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO06	Input	Pull Down
GPIO_AD_07	T17	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO07	Input	Pull Down
GPIO_AD_08	T14	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO08	Input	Pull Down
GPIO_AD_09	R16	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO09	Input	Pull Down
GPIO_AD_10	R17	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO10	Input	Pull Down
GPIO_AD_11	P16	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO11	Input	Pull Down
GPIO_AD_12	P17	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO12	Input	Pull Up

Table 115. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_AD_13	N15	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO13	Input	Pull Down
GPIO_AD_14	N14	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO14	Input	Pull Down
GPIO_AD_15	N16	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO15	Input	Pull Down
GPIO_AD_16	N17	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO16	Input	Pull Down
GPIO_AD_17	M17	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO17	Input	Pull Down
GPIO_AD_18	K16	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO18	Input	Pull Down
GPIO_AD_19	L13	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO19	Input	Pull Down
GPIO_AD_20	K13	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO20	Input	Pull Down
GPIO_AD_21	K15	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO21	Input	Pull Down
GPIO_AD_22	K12	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO22	Input	Pull Down
GPIO_AD_23	K14	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO23	Input	Pull Down
GPIO_AD_24	M13	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO24	Input	Pull Down
GPIO_AD_25	M15	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO25	Input	Pull Down
GPIO_AD_26	M14	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO26	Input	Pull Down
GPIO_AD_27	M16	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO27	Input	Pull Down
GPIO_AD_28	L16	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO28	Input	Pull Down
GPIO_AD_29	L15	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO29	Input	Pull Up
GPIO_AD_30	L17	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO30	Input	Pull Down
GPIO_AD_31	K17	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO31	Input	Pull Down

Table 115. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_AD_32	J17	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO5_IO00	Input	Pull Down
GPIO_AD_33	J16	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO5_IO01	Input	Pull Down
GPIO_AD_34	J15	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO5_IO02	Input	Pull Down
GPIO_AD_35	H17	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO5_IO03	Input	Pull Down
GPIO_AON_00	F8	NVCC_AON	Digital FSGPIO	ALT 0	SRC_BOOT_MODE0	Input	Pull Down
GPIO_AON_01	B7	NVCC_AON	Digital FSGPIO	ALT 0	SRC_BOOT_MODE1	Input	Pull Down
GPIO_AON_02	B6	NVCC_AON	Digital FSGPIO	ALT 0	SRC_BOOT_MODE2	Input	Pull Down
GPIO_AON_03	C8	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO03	Input	Pull Down
GPIO_AON_04	B4	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO04	Input	Pull Down
GPIO_AON_05	C7	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO05	Input	Pull Down
GPIO_AON_06	E7	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO06	Input	Pull Down
GPIO_AON_07	C6	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO07	Input	Pull Down
GPIO_AON_08	B1	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO08	Input	Pull Down
GPIO_AON_09	A5	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO09	Input	Pull Down
GPIO_AON_10	B5	NVCC_AON	Digital FSGPIO	ALT 0	JTAG_MUX_TRSTB	Input	Pull Up
GPIO_AON_11	A4	NVCC_AON	Digital FSGPIO	ALT 0	JTAG_MUX_TDO	Input	High Z
GPIO_AON_12	A3	NVCC_AON	Digital FSGPIO	ALT 0	JTAG_MUX_TDI	Input	Pull Up
GPIO_AON_13	A2	NVCC_AON	Digital FSGPIO	ALT 0	JTAG_MUX_TCK	Input	Pull Down
GPIO_AON_14	B2	NVCC_AON	Digital FSGPIO	ALT 0	JTAG_MUX_TMS	Input	Pull Up

Table 115. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_AON_15	B3	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO15	Input	Pull Down
GPIO_AON_16	C5	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO16	Input	Pull Down
GPIO_AON_17	D6	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO17	Input	Pull Down
GPIO_AON_18	E6	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO18	Input	Pull Down
GPIO_AON_19	D5	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO19	Input	Pull Up
GPIO_AON_20	E5	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO20	Input	Pull Up
GPIO_AON_21	F6	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO21	Input	Pull Up
GPIO_AON_22	C3	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO22	Input	Pull Up
GPIO_AON_23	C2	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO23	Input	Pull Down
GPIO_AON_24	C1	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO24	Input	Pull Down
GPIO_AON_25	D2	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO25	Input	Pull Down
GPIO_AON_26	C4	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO26	Input	Pull Down
GPIO_AON_27	D3	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO27	Input	Pull Up
GPIO_B1_00	E13	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO00	Input	Pull Up
GPIO_B1_01	C12	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO01	Input	Pull Up
GPIO_B1_02	E12	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO02	Input	Pull Up
GPIO_B1_03	A14	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO03	Input	Pull Down
GPIO_B1_04	B13	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO04	Input	Pull Up
GPIO_B1_05	B12	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO05	Input	Pull Down

Table 115. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_B1_06	B10	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO06	Input	Pull Down
GPIO_B1_07	D13	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO07	Input	Pull Down
GPIO_B1_08	B14	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO08	Input	Pull Down
GPIO_B1_09	A15	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO09	Input	Pull Down
GPIO_B1_10	A13	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO10	Input	Pull Down
GPIO_B1_11	A12	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO11	Input	Pull Down
GPIO_B1_12	A11	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO12	Input	Pull Down
GPIO_B1_13	B11	NVCC_GPIO1	Digital GPIO	ALT 5	GPIO6_IO13	Input	Pull Down
GPIO_B2_00	E9	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO14	Input	Pull Up
GPIO_B2_01	E10	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO15	Input	Pull Up
GPIO_B2_02	C10	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO16	Input	Pull Up
GPIO_B2_03	D9	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO17	Input	Pull Down
GPIO_B2_04	C9	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO18	Input	Pull Down
GPIO_B2_05	A9	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO19	Input	Pull Down
GPIO_B2_06	E8	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO20	Input	Pull Down
GPIO_B2_07	A6	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO21	Input	Pull Down
GPIO_B2_08	A7	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO22	Input	Pull Down
GPIO_B2_09	D10	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO23	Input	Pull Up
GPIO_B2_10	A10	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO24	Input	Pull Down

Table 115. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_B2_11	B9	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO25	Input	Pull Down
GPIO_B2_12	A8	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO26	Input	Pull Down
GPIO_B2_13	B8	NVCC_GPIO2	Digital GPIO	ALT 5	GPIO6_IO27	Input	Pull Down
GPIO_BBSM_00	R10	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER0	Input	Pull Down
GPIO_BBSM_01	P10	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER1	Input	Pull Down
GPIO_BBSM_02	L9	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER2	Input	Pull Down
GPIO_BBSM_03	M10	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER3	Input	Pull Down
GPIO_BBSM_04	N10	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER4	Input	Pull Down
GPIO_BBSM_05	P9	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER5	Input	Pull Down
GPIO_BBSM_06	M9	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER6	Input	Pull Down
GPIO_BBSM_07	R9	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER7	Input	Pull Down
GPIO_BBSM_08	N9	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER8	Input	Pull Down

Table 115. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_BBSM_09	R11	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER9	Input	Pull Down
GPIO_EMC_B1_00	H3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO00	Input	Pull Down
GPIO_EMC_B1_01	H4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO01	Input	Pull Down
GPIO_EMC_B1_02	K2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO02	Input	Pull Down
GPIO_EMC_B1_03	G3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO03	Input	Pull Down
GPIO_EMC_B1_04	J4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO04	Input	Pull Down
GPIO_EMC_B1_05	H6	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO05	Input	Pull Down
GPIO_EMC_B1_06	K3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO06	Input	Pull Down
GPIO_EMC_B1_07	M3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO07	Input	Pull Down
GPIO_EMC_B1_08	H5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO08	Input	Pull Down
GPIO_EMC_B1_09	E1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO09	Input	Pull Down
GPIO_EMC_B1_10	E3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO10	Input	Pull Down
GPIO_EMC_B1_11	F2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO11	Input	Pull Down
GPIO_EMC_B1_12	G6	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO12	Input	Pull Down
GPIO_EMC_B1_13	F3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO13	Input	Pull Down
GPIO_EMC_B1_14	G5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO14	Input	Pull Down
GPIO_EMC_B1_15	G2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO15	Input	Pull Down
GPIO_EMC_B1_16	H1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO16	Input	Pull Down

Table 115. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_EMC_B1_17	E2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO17	Input	Pull Down
GPIO_EMC_B1_18	D1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO18	Input	Pull Down
GPIO_EMC_B1_19	F4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO19	Input	Pull Down
GPIO_EMC_B1_20	G1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO20	Input	Pull Down
GPIO_EMC_B1_21	K4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO21	Input	Pull Down
GPIO_EMC_B1_22	L3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO22	Input	Pull Down
GPIO_EMC_B1_23	F1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO23	Input	Pull Down
GPIO_EMC_B1_24	P2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO24	Input	Pull Down
GPIO_EMC_B1_25	N3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO25	Input	Pull Down
GPIO_EMC_B1_26	N4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO26	Input	Pull Up
GPIO_EMC_B1_27	J3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO27	Input	Pull Down
GPIO_EMC_B1_28	F5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO28	Input	Pull Up
GPIO_EMC_B1_29	E4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO29	Input	Pull Down
GPIO_EMC_B1_30	H2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO30	Input	Pull Down
GPIO_EMC_B1_31	J2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO31	Input	Pull Down
GPIO_EMC_B1_32	J1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO00	Input	Pull Down
GPIO_EMC_B1_33	K1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO01	Input	Pull Down
GPIO_EMC_B1_34	L2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO02	Input	Pull Down
GPIO_EMC_B1_35	L1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO03	Input	Pull Down

Table 115. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_EMC_B1_36	M1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO04	Input	Pull Down
GPIO_EMC_B1_37	N1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO05	Input	Pull Down
GPIO_EMC_B1_38	M2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO06	Input	Pull Down
GPIO_EMC_B1_39	P1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO07	Input	Pull Up
GPIO_EMC_B1_40	N2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO08	Input	Pull Down
GPIO_EMC_B1_41	R1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO09	Input	Pull Down
GPIO_EMC_B2_00	N5	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO10	Input	Pull Down
GPIO_EMC_B2_01	R2	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO11	Input	Pull Down
GPIO_EMC_B2_02	P5	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO12	Input	Pull Down
GPIO_EMC_B2_03	T5	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO13	Input	Pull Down
GPIO_EMC_B2_04	R3	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO14	Input	Pull Down
GPIO_EMC_B2_05	T4	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO15	Input	Pull Down
GPIO_EMC_B2_06	T6	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO16	Input	Pull Down
GPIO_EMC_B2_07	T7	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO17	Input	Pull Down
GPIO_EMC_B2_08	U4	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO18	Input	Pull Down
GPIO_EMC_B2_09	U5	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO19	Input	Pull Down
GPIO_EMC_B2_10	U6	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO20	Input	Pull Down
GPIO_EMC_B2_11	P6	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO21	Input	Pull Down
GPIO_EMC_B2_12	R5	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO22	Input	Pull Down

Table 115. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_EMC_B2_13	R6	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO23	Input	Pull Down
GPIO_EMC_B2_14	N8	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO24	Input	Pull Down
GPIO_EMC_B2_15	R4	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO25	Input	Pull Down
GPIO_EMC_B2_16	R7	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO26	Input	Pull Down
GPIO_EMC_B2_17	U7	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO27	Input	Pull Down
GPIO_EMC_B2_18	P8	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO28	Input	Pull Up
GPIO_EMC_B2_19	U8	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO29	Input	Pull Down
GPIO_EMC_B2_20	R8	NVCC_EMC2	Digital GPIO	ALT 5	GPIO3_IO30	Input	Pull Down
GPIO_SD_B1_00	B16	NVCC_SD1	Digital GPIO	ALT 5	GPIO5_IO04	Input	Pull Down
GPIO_SD_B1_01	D15	NVCC_SD1	Digital GPIO	ALT 5	GPIO5_IO05	Input	Pull Down
GPIO_SD_B1_02	D14	NVCC_SD1	Digital GPIO	ALT 5	GPIO5_IO06	Input	Pull Up
GPIO_SD_B1_03	C15	NVCC_SD1	Digital GPIO	ALT 5	GPIO5_IO07	Input	Pull Up
GPIO_SD_B1_04	B15	NVCC_SD1	Digital GPIO	ALT 5	GPIO5_IO08	Input	Pull Up
GPIO_SD_B1_05	A16	NVCC_SD1	Digital GPIO	ALT 5	GPIO5_IO09	Input	Pull Up
GPIO_SD_B2_00	H15	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO10	Input	Pull Down
GPIO_SD_B2_01	H14	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO11	Input	Pull Down
GPIO_SD_B2_02	G17	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO12	Input	Pull Down
GPIO_SD_B2_03	G13	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO13	Input	Pull Down
GPIO_SD_B2_04	G15	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO14	Input	Pull Up

Table 115. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_SD_B2_05	E15	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO15	Input	Pull Down
GPIO_SD_B2_06	F15	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO16	Input	Pull Up
GPIO_SD_B2_07	E14	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO17	Input	Pull Down
GPIO_SD_B2_08	F14	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO18	Input	Pull Down
GPIO_SD_B2_09	F16	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO19	Input	Pull Down
GPIO_SD_B2_10	G16	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO20	Input	Pull Down
GPIO_SD_B2_11	F17	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO21	Input	Pull Down
ONOFF	U10	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	ONOFF	Input	Pull Up
PMIC_ON_REQ	U9	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	PMIC_ON_REQ	Output	No Pull
PMIC_STBY_REQ	T9	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	PMIC_STBY_REQ	Output	No Pull
POR_B	T10	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	POR_B	Input	Pull Up
RTC_XTALI	T13	—	—	—	—	—	—
RTC_XTALO	U13	—	—	—	—	—	—
TEST_MODE	T11	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TEST_MODE	Input	Pull Down
USB1_DN	E16	—	—	—	—	—	—
USB1_DP	E17	—	—	—	—	—	—
USB1_VBUS	D17	—	—	—	—	—	—

Table 115. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
USB2_DN	C16	—	—	—	—	—	—
USB2_DP	C17	—	—	—	—	—	—
USB2_VBUS	D16	—	—	—	—	—	—
WAKEUP	T8	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	WAKEUP	Input	Pull Down
XTALI	U16	—	—	—	—	—	—
XTALO	T16	—	—	—	—	—	—

6.1.3 14 x 14 mm, 0.8 mm pitch, ball map

Table 116 shows the 14 x 14 mm, 0.8 mm pitch ball map for the i.MX RT1180.

Table 116. 14 x 14 mm, 0.8 mm pitch, ball map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	GPIO_AON_13	GPIO_AON_12	GPIO_AON_11	GPIO_AON_09	GPIO_B2_07	GPIO_B2_08	GPIO_B2_12	GPIO_B2_05	GPIO_B2_10	GPIO_B1_12	GPIO_B1_11	GPIO_B1_10	GPIO_B1_03	GPIO_B1_09	GPIO_SD_B1_05	VSS
B	GPIO_AON_08	GPIO_AON_14	GPIO_AON_15	GPIO_AON_04	GPIO_AON_10	GPIO_AON_02	GPIO_AON_01	GPIO_B2_13	GPIO_B2_11	GPIO_B1_06	GPIO_B1_13	GPIO_B1_05	GPIO_B1_04	GPIO_B1_08	GPIO_SD_B1_04	GPIO_SD_B1_00	VDD_USB_1P8
C	GPIO_AON_24	GPIO_AON_23	GPIO_AON_22	GPIO_AON_26	GPIO_AON_16	GPIO_AON_07	GPIO_AON_05	GPIO_AON_03	GPIO_B2_04	GPIO_B2_02	VSS	GPIO_B1_01	NVCC_SD1	VSS	GPIO_SD_B1_03	USB2_DN	USB2_DP
D	GPIO_EMC_B1_18	GPIO_AON_25	GPIO_AON_27	VSS	GPIO_AON_19	GPIO_AON_17	VSS	VSS	GPIO_B2_03	GPIO_B2_09	NVCC_GPIO1	VSS	GPIO_B1_07	GPIO_SD_B1_02	GPIO_SD_B1_01	USB2_VBUS	USB1_VBUS
E	GPIO_EMC_B1_09	GPIO_EMC_B1_17	GPIO_EMC_B1_10	GPIO_EMC_B1_29	GPIO_AON_20	GPIO_AON_18	GPIO_AON_06	GPIO_B2_06	GPIO_B2_00	GPIO_B2_01	NVCC_GPIO1	GPIO_B1_02	GPIO_B1_00	GPIO_SD_B2_07	GPIO_SD_B2_05	USB1_DN	USB1_DP
F	GPIO_EMC_B1_23	GPIO_EMC_B1_11	GPIO_EMC_B1_13	GPIO_EMC_B1_19	GPIO_EMC_B1_28	GPIO_AON_21	NVCC_AON	GPIO_AON_00	NVCC_GPIO2	NVCC_GPIO2	VSS	VSS	VSS	GPIO_SD_B2_08	GPIO_SD_B2_06	GPIO_SD_B2_09	GPIO_SD_B2_11
G	GPIO_EMC_B1_20	GPIO_EMC_B1_15	GPIO_EMC_B1_03	VSS	GPIO_EMC_B1_14	GPIO_EMC_B1_12	VSS	VSS	VSS	VSS	VSS	VDD_USB_3P3	GPIO_SD_B2_03	VSS	GPIO_SD_B2_04	GPIO_SD_B2_10	GPIO_SD_B2_02
H	GPIO_EMC_B1_16	GPIO_EMC_B1_30	GPIO_EMC_B1_00	GPIO_EMC_B1_01	GPIO_EMC_B1_08	GPIO_EMC_B1_05	VSS	VDD_SOC	VDD_SOC	VDD_SOC	VSS	NVCC_SD2	NVCC_SD2	GPIO_SD_B2_01	GPIO_SD_B2_00	ADC_VREFH	GPIO_AD_35
J	GPIO_EMC_B1_32	GPIO_EMC_B1_31	GPIO_EMC_B1_27	GPIO_EMC_B1_04	NVCC_EMC1	NVCC_EMC1	VSS	VDD_SOC	VDD_SOC	VDD_SOC	VSS	DAC_OUT	VDDA_ADC_1P8	VDDA_ADC_3P3	GPIO_AD_34	GPIO_AD_33	GPIO_AD_32

Table 116. 14 x 14 mm, 0.8 mm pitch, ball map (continued)

K	GPIO_EMC_B1_33	GPIO_EMC_B1_02	GPIO_EMC_B1_06	GPIO_EMC_B1_21	NVCC_EMC1	DCDC_GND	DCDC_GND	DCDC_GND	DCDC_GND	VDD_SOC	VSS	GPIO_AD_22	GPIO_AD_20	GPIO_AD_23	GPIO_AD_21	GPIO_AD_18	GPIO_AD_31
L	GPIO_EMC_B1_35	GPIO_EMC_B1_34	GPIO_EMC_B1_22	VSS	DCDC_PSWITCH	DCDC_MODE	DCDC_IN_Q	DCDC_SENSE	GPIO_BBSM_02	VSS	VSS	NVCC_GPIO_AD	GPIO_AD_19	VSS	GPIO_AD_29	GPIO_AD_28	GPIO_AD_30
M	GPIO_EMC_B1_36	GPIO_EMC_B1_38	GPIO_EMC_B1_07	DCDC_1P8	DCDC_IN	DCDC_IN	DCDC_IN	DCDC_IN	GPIO_BBSM_06	GPIO_BBSM_03	NVCC_GPIO_AD	VDDA_1P8_IN	GPIO_AD_24	GPIO_AD_26	GPIO_AD_25	GPIO_AD_27	GPIO_AD_17
N	GPIO_EMC_B1_37	GPIO_EMC_B1_40	GPIO_EMC_B1_25	GPIO_EMC_B1_26	GPIO_EMC_B2_00	NVCC_EMC2	NVCC_EMC2	GPIO_EMC_B2_14	GPIO_BBSM_08	GPIO_BBSM_04	VDDA_1P0	GPIO_AD_00	GPIO_AD_06	GPIO_AD_14	GPIO_AD_13	GPIO_AD_15	GPIO_AD_16
P	GPIO_EMC_B1_39	GPIO_EMC_B1_24	VSS	VSS	GPIO_EMC_B2_02	GPIO_EMC_B2_11	VSS	GPIO_EMC_B2_18	GPIO_BBSM_05	GPIO_BBSM_01	VDD_AON_DIG	VDD_AON_ANA	GPIO_AD_05	VSS	GPIO_AD_04	GPIO_AD_11	GPIO_AD_12
R	GPIO_EMC_B1_41	GPIO_EMC_B2_01	GPIO_EMC_B2_04	GPIO_EMC_B2_15	GPIO_EMC_B2_12	GPIO_EMC_B2_13	GPIO_EMC_B2_16	GPIO_EMC_B2_20	GPIO_BBSM_07	GPIO_BBSM_00	GPIO_BBSM_09	VDD_BBSM_ANA	GPIO_AD_02	GPIO_AD_01	GPIO_AD_03	GPIO_AD_09	GPIO_AD_10
T	DCDC_LP	DCDC_LP	DCDC_LP	GPIO_EMC_B2_05	GPIO_EMC_B2_03	GPIO_EMC_B2_06	GPIO_EMC_B2_07	WAKEUP	PMIC_STBY_REQ	POR_B	TEST_MODE	VSS	RTC_XTALI	GPIO_AD_08	CLK1_N	XTALO	GPIO_AD_07
U	VSS	DCDC_LP	DCDC_LP	GPIO_EMC_B2_08	GPIO_EMC_B2_09	GPIO_EMC_B2_10	GPIO_EMC_B2_17	GPIO_EMC_B2_19	PMIC_ON_REQ	ONOFF	NVCC_BBSM	VDD_BBSM_IN	RTC_XTALO	VDD_AON_IN	CLK1_P	XTALI	VSS
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**

6.2 10 x 10 mm package information

6.2.1 10 x 10 mm, 0.8 mm pitch, ball matrix

Figure 63 shows the top, bottom, and side views of the 10 x 10 mm MAPBGA package.

PBGA–144 I/O
10 X 10 X 1.37 PKG, 0.8 PITCH

SOT2134–1

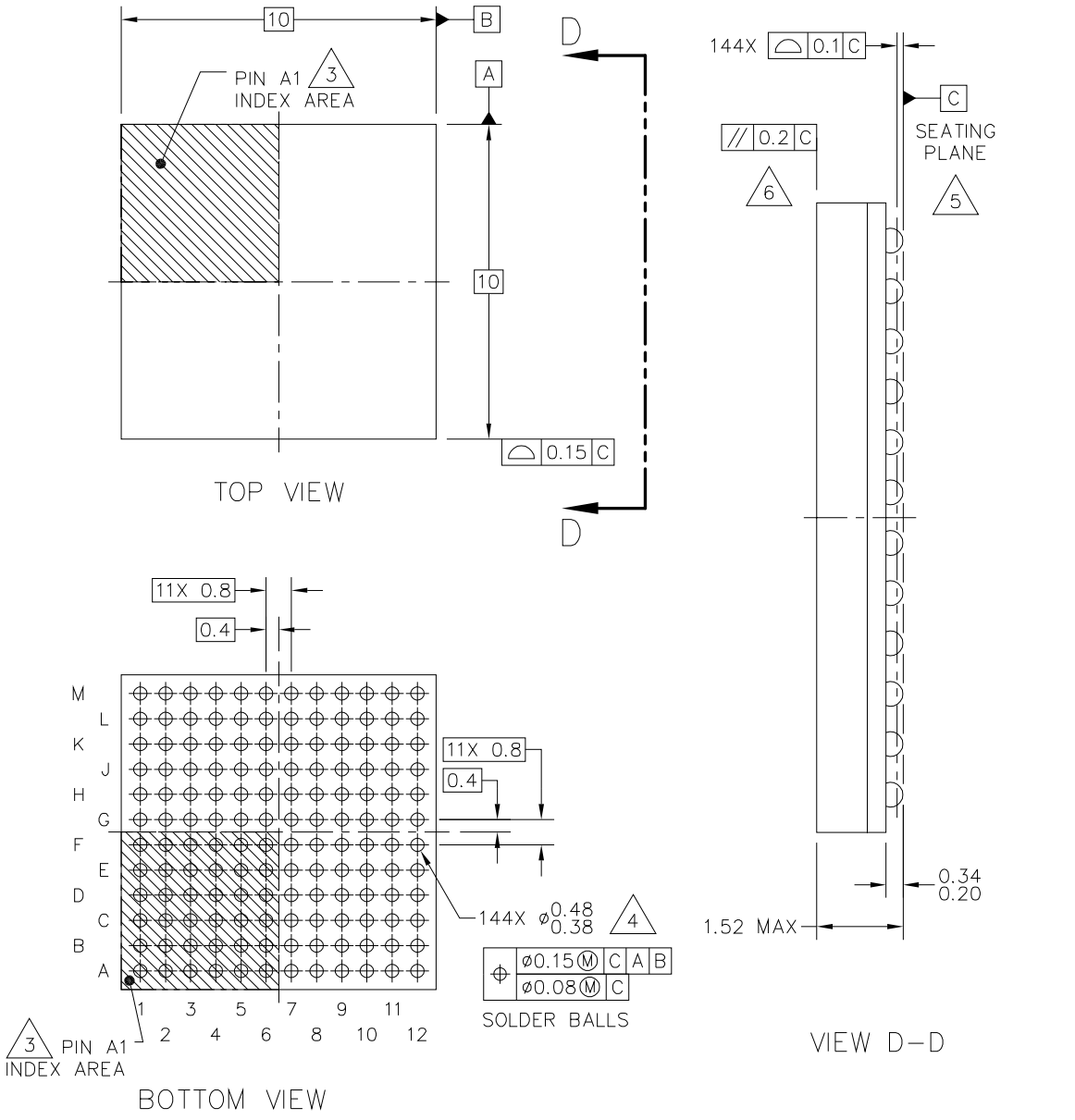

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Figure 64. 10 x 10 mm BGA, case x package top, bottom, and side Views

6.2.2 10 x 10 mm supplies contact assignments and functional contact assignments

Table 114 shows the device connection list for ground, sense, and reference contact signals.

Table 117. 10 x 10 mm supplies contact assignment

Supply Rail Name	Ball(s) Position(s)	Remark
ADC_VREFH	F12	—
DCDC_1P8	L1	—
DCDC_IN	L4, M4	—
DCDC_IN_Q	K4	—
DCDC_GND	K3, L3, M3	—
DCDC_LP	L2, M2	—
DCDC_PSWITCH	K2	—
DCDC_SENSE	K1	—
NVCC_AON	D5	—
NVCC_BBSM	K7	—
NVCC_EMC1	F6, G6, H6	—
NVCC_GPIO_AD	H9	—
NVCC_SD2	E9, F9	—
VDD_AON_ANA	K9	—
VDD_AON_DIG	M8	—
VDD_AON_IN	L8	—
VDD_BBSM_ANA	K8	—
VDD_BBSM_IN	M6	—
VDD_SOC	E8, F7, F8, G7	—
VDDA_1P0	M10	—
VDDA_1P8_IN	J10	—
VDDA_ADC_1P8	G9	—
VDDA_ADC_3P3	G8	—
VSS	A1, A12, C8, D4, D9, J4, J9, L10, M1, M12	—

Table 115 shows an alpha-sorted list of functional contact assignments of the 10 x 10 mm package.

Table 118. 10 x 10 mm functional contact assignment

Ball name	10 x 10 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
CLK1_N	L11	—	—	—	—	—	—
CLK1_P	M11	—	—	—	—	—	—
DAC_OUT	G10	—	—	—	—	—	—
GPIO_AD_12	K11	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO12	Input	Pull Up
GPIO_AD_13	K10	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO13	Input	Pull Down
GPIO_AD_14	J11	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO14	Input	Pull Down
GPIO_AD_15	J12	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO15	Input	Pull Down
GPIO_AD_16	L12	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO16	Input	Pull Down
GPIO_AD_17	K12	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO17	Input	Pull Down
GPIO_AD_18	H10	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO18	Input	Pull Down
GPIO_AD_19	H11	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO19	Input	Pull Down
GPIO_AD_29	H12	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO29	Input	Pull Up
GPIO_AD_30	G11	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO30	Input	Pull Down
GPIO_AD_31	G12	NVCC_GPIO_AD	Digital FSGPIO	ALT 5	GPIO4_IO31	Input	Pull Down
GPIO_AON_00	C9	NVCC_AON	Digital FSGPIO	ALT 0	SRC_BOOT_MODE0	Input	Pull Down
GPIO_AON_01	C7	NVCC_AON	Digital FSGPIO	ALT 0	SRC_BOOT_MODE1	Input	Pull Down
GPIO_AON_02	C6	NVCC_AON	Digital FSGPIO	ALT 0	SRC_BOOT_MODE2	Input	Pull Down
GPIO_AON_03	B7	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO03	Input	Pull Down
GPIO_AON_04	D6	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO04	Input	Pull Down

Table 118. 10 x 10 mm functional contact assignment (continued)

Ball name	10 x 10 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_AON_05	B6	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO05	Input	Pull Down
GPIO_AON_06	D7	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO06	Input	Pull Down
GPIO_AON_07	D8	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO07	Input	Pull Down
GPIO_AON_08	A11	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO08	Input	Pull Down
GPIO_AON_09	B8	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO09	Input	Pull Down
GPIO_AON_10	A8	NVCC_AON	Digital FSGPIO	ALT 0	JTAG_MUX_TRSTB	Input	Pull Up
GPIO_AON_11	B9	NVCC_AON	Digital FSGPIO	ALT 0	JTAG_MUX_TDO	Input	High Z
GPIO_AON_12	A9	NVCC_AON	Digital FSGPIO	ALT 0	JTAG_MUX_TDI	Input	Pull Up
GPIO_AON_13	B11	NVCC_AON	Digital FSGPIO	ALT 0	JTAG_MUX_TCK	Input	Pull Down
GPIO_AON_14	B10	NVCC_AON	Digital FSGPIO	ALT 0	JTAG_MUX_TMS	Input	Pull Up
GPIO_AON_15	A10	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO15	Input	Pull Down
GPIO_AON_16	C5	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO16	Input	Pull Down
GPIO_AON_17	C4	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO17	Input	Pull Down
GPIO_AON_18	E7	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO18	Input	Pull Down
GPIO_AON_19	E6	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO19	Input	Pull Up
GPIO_AON_20	E5	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO20	Input	Pull Up
GPIO_AON_21	E4	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO21	Input	Pull Up
GPIO_AON_22	A7	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO22	Input	Pull Up
GPIO_AON_23	A6	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO23	Input	Pull Down

Table 118. 10 x 10 mm functional contact assignment (continued)

Ball name	10 x 10 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_AON_24	B5	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO24	Input	Pull Down
GPIO_AON_25	A5	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO25	Input	Pull Down
GPIO_AON_26	A4	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO26	Input	Pull Down
GPIO_AON_27	B4	NVCC_AON	Digital FSGPIO	ALT 5	GPIO1_IO27	Input	Pull Up
GPIO_BBSM_00	J8	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER0	Input	Pull Down
GPIO_BBSM_01	K6	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER1	Input	Pull Down
GPIO_BBSM_05	H7	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER5	Input	Pull Down
GPIO_BBSM_06	H8	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TAMPER6	Input	Pull Down
GPIO_EMC_B1_00	G5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO00	Input	Pull Down
GPIO_EMC_B1_01	G4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO01	Input	Pull Down
GPIO_EMC_B1_02	H5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO02	Input	Pull Down
GPIO_EMC_B1_03	F4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO03	Input	Pull Down
GPIO_EMC_B1_04	H4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO04	Input	Pull Down
GPIO_EMC_B1_05	F5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO05	Input	Pull Down
GPIO_EMC_B1_06	J6	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO06	Input	Pull Down
GPIO_EMC_B1_07	J5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO07	Input	Pull Down

Table 118. 10 x 10 mm functional contact assignment (continued)

Ball name	10 x 10 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_EMC_B1_08	F3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO08	Input	Pull Down
GPIO_EMC_B1_09	A3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO09	Input	Pull Down
GPIO_EMC_B1_10	C1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO10	Input	Pull Down
GPIO_EMC_B1_11	B2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO11	Input	Pull Down
GPIO_EMC_B1_12	D3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO12	Input	Pull Down
GPIO_EMC_B1_13	E3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO13	Input	Pull Down
GPIO_EMC_B1_14	D2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO14	Input	Pull Down
GPIO_EMC_B1_15	B1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO15	Input	Pull Down
GPIO_EMC_B1_16	A2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO16	Input	Pull Down
GPIO_EMC_B1_17	B3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO17	Input	Pull Down
GPIO_EMC_B1_26	J1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO26	Input	Pull Up
GPIO_EMC_B1_27	G3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO27	Input	Pull Down
GPIO_EMC_B1_28	C2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO28	Input	Pull Up
GPIO_EMC_B1_29	C3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO29	Input	Pull Down
GPIO_EMC_B1_30	D1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO30	Input	Pull Down
GPIO_EMC_B1_31	E2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO2_IO31	Input	Pull Down
GPIO_EMC_B1_32	E1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO00	Input	Pull Down
GPIO_EMC_B1_33	F2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO01	Input	Pull Down
GPIO_EMC_B1_34	F1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO02	Input	Pull Down

Table 118. 10 x 10 mm functional contact assignment (continued)

Ball name	10 x 10 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
GPIO_EMC_B1_35	G1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO03	Input	Pull Down
GPIO_EMC_B1_36	G2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO04	Input	Pull Down
GPIO_EMC_B1_37	H1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO05	Input	Pull Down
GPIO_EMC_B1_38	H3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO06	Input	Pull Down
GPIO_EMC_B1_39	H2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO07	Input	Pull Up
GPIO_EMC_B1_40	J2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO08	Input	Pull Down
GPIO_EMC_B1_41	J3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO3_IO09	Input	Pull Down
GPIO_SD_B2_00	F10	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO10	Input	Pull Down
GPIO_SD_B2_01	E11	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO11	Input	Pull Down
GPIO_SD_B2_02	F11	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO12	Input	Pull Down
GPIO_SD_B2_03	E10	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO13	Input	Pull Down
GPIO_SD_B2_04	C12	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO14	Input	Pull Up
GPIO_SD_B2_05	D10	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO15	Input	Pull Down
GPIO_SD_B2_06	B12	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO16	Input	Pull Up
GPIO_SD_B2_07	C10	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO17	Input	Pull Down
GPIO_SD_B2_08	D11	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO18	Input	Pull Down
GPIO_SD_B2_09	D12	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO19	Input	Pull Down
GPIO_SD_B2_10	E12	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO20	Input	Pull Down
GPIO_SD_B2_11	C11	NVCC_SD2	Digital GPIO	ALT 5	GPIO5_IO21	Input	Pull Down

Table 118. 10 x 10 mm functional contact assignment (continued)

Ball name	10 x 10 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Value
ONOFF	K5	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	ONOFF	Input	Pull Up
PMIC_ON_REQ	L5	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	PMIC_ON_REQ	Output	No Pull
POR_B	L6	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	POR_B	Input	Pull Up
RTC_XTALI	M7	—	—	—	—	—	—
RTC_XTALO	L7	—	—	—	—	—	—
TEST_MODE	J7	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	TEST_MODE	Input	Pull Down
WAKEUP	M5	NVCC_BBSM	ANALOG GPIO (pad driver)	ALT 0	WAKEUP	Input	Pull Down
XTALI	M9	—	—	—	—	—	—
XTALO	L9	—	—	—	—	—	—

6.2.3 10 x 10 mm, 0.8 mm pitch, ball map

Table 119 shows the 10 x 10 mm, 0.8 mm pitch ball map for the i.MX RT1180i.MX RT1180_S.

Table 119. 10 x 10 mm, 0.8 mm pitch, ball map

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	GPIO_EMC_B1_16	GPIO_EMC_B1_09	GPIO_AON_26	GPIO_AON_25	GPIO_AON_23	GPIO_AON_22	GPIO_AON_10	GPIO_AON_12	GPIO_AON_15	GPIO_AON_08	VSS
B	GPIO_EMC_B1_15	GPIO_EMC_B1_11	GPIO_EMC_B1_17	GPIO_AON_27	GPIO_AON_24	GPIO_AON_05	GPIO_AON_03	GPIO_AON_09	GPIO_AON_11	GPIO_AON_14	GPIO_AON_13	GPIO_SD_B2_06
C	GPIO_EMC_B1_10	GPIO_EMC_B1_28	GPIO_EMC_B1_29	GPIO_AON_17	GPIO_AON_16	GPIO_AON_02	GPIO_AON_01	VSS	GPIO_AON_00	GPIO_SD_B2_07	GPIO_SD_B2_11	GPIO_SD_B2_04
D	GPIO_EMC_B1_30	GPIO_EMC_B1_14	GPIO_EMC_B1_12	VSS	NVCC_AON	GPIO_AON_04	GPIO_AON_06	GPIO_AON_07	VSS	GPIO_SD_B2_05	GPIO_SD_B2_08	GPIO_SD_B2_09
E	GPIO_EMC_B1_32	GPIO_EMC_B1_31	GPIO_EMC_B1_13	GPIO_AON_21	GPIO_AON_20	GPIO_AON_19	GPIO_AON_18	VDD_SOC	NVCC_SD2	GPIO_SD_B2_03	GPIO_SD_B2_01	GPIO_SD_B2_10
F	GPIO_EMC_B1_34	GPIO_EMC_B1_33	GPIO_EMC_B1_08	GPIO_EMC_B1_03	GPIO_EMC_B1_05	NVCC_EMC1	VDD_SOC	VDD_SOC	NVCC_SD2	GPIO_SD_B2_00	GPIO_SD_B2_02	ADC_VREFH
G	GPIO_EMC_B1_35	GPIO_EMC_B1_36	GPIO_EMC_B1_27	GPIO_EMC_B1_01	GPIO_EMC_B1_00	NVCC_EMC1	VDD_SOC	VDDA_ADC_3P3	VDDA_ADC_1P8	DAC_OUT	GPIO_AD30	GPIO_AD31
H	GPIO_EMC_B1_37	GPIO_EMC_B1_39	GPIO_EMC_B1_38	GPIO_EMC_B1_04	GPIO_EMC_B1_02	NVCC_EMC1	GPIO_BBSM_05	GPIO_BBSM_06	NVCC_GPIO_AD	GPIO_AD_18	GPIO_AD_19	GPIO_AD_29
J	GPIO_EMC_B1_26	GPIO_EMC_B1_40	GPIO_EMC_B1_41	VSS	GPIO_EMC_B1_07	GPIO_EMC_B1_06	TEST_MODE	GPIO_BBSM_00	VSS	VDDA_1P8_IN	GPIO_AD_14	GPIO_AD_15
K	DCDC_SENSE	DCDC_PSWITCH	DCDC_GND	DCDC_IN_Q	ONOFF	GPIO_BBSM_01	NVCC_BBSM	VDD_BBSM_ANA	VDD_AON_ANA	GPIO_AD_13	GPIO_AD_12	GPIO_AD_17
L	DCDC_1P8	DCDC_LP	DCDC_GND	DCDC_IN	PMIC_ON_REQ	POR_B	RTC_XTALO	VDD_AON_IN	XTALO	VSS	CLK1_N	GPIO_AD_16
M	VSS	DCDC_LP	DCDC_GND	DCDC_IN	WAKEUP	VDD_BBSM_IN	RTC_XTALI	VDD_AON_DIG	XTALI	VDDA_1P0	CLK1_P	VSS
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**

7 Revision history

Table 120 provides a revision history for this data sheet.

Table 120: i.MX RT1180 Data Sheet document revision history

Rev. 4	05/2024	• Updated part numbers information and added a footnote in Table 1. Ordering information • Updated ADC and FlexSPI descriptions in Section 1.1, Features • Updated Figure 1, "Part number nomenclature—i.MX RT1180" • Updated Figure 3, "i.MX RT1180 system block diagram" • Updated the description of DCDC_IN in Table 10. Thermal characteristics • Updated Table 11. Operating ranges • Updated Table 12. Maximum supply currents • Updated the notes in Section 4.2.1, Power supplies requirements and restrictions • Added table footnotes in Section 4.2.5, PLL's electrical characteristics and clock output range in Table 26. Arm PLL's electrical parameters • Updated Table 27. 24 MHz system oscillator specifications • Updated Table 33. DC specification for GPIO_EMC_B1/GPIO_EMC_B2/GPIO_B1/GPIO_B2/GPIO_SD1/GPIO_SD2 bank • Updated Table 35. Additional leakage parameters • Updated Figure 22, "FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0X3 (case A2)" and note descriptions • Add a footnote in Table 55. FlexSPI input timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x1 • Added Section 4.5.4, FlexSPI Follower parameters • Updated timing parameters in Section 4.8.1, LPSPI timing parameters • Updated the title of Section 4.8.4, Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing, added Section 4.8.5.2, RMII mode timing, and removed RGMII signal switching specifications • Added Section 4.9.3, LPTMR characteristics
Rev. 3	11/2023	• Updated Table 1. Ordering information
Rev. 2.1	09/2023	• Updated Figure 1, "Part number nomenclature—i.MX RT1180" • Added Table 35. Additional leakage parameters
Rev. 2	02/2023	• Updated Table 38. AC specifications for GPIO_AD/GPIO_AON bank • Added ADC temp sensor constants in Table 70. 16-bit ADC electrical characteristics • Removed tT1588OV from Table 89. NETC 1588 timing Parameters
Rev. 1	09/2022	• Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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