FS6600

Fail-safe system basis chip with multiple SMPS and LDO

Rev. 3 — 17 July 2024 Product data sheet

1 General description

The FS6600 is an automotive functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS domain controller, Radio and Infotainment applications. The FS6600 device family was developed in compliance with ASIL D process. It includes multiple switch mode and linear voltage regulators. All device options are pin to pin and software compatible.

The FS6600 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering ASIL D safety integrity level. It is developed in compliance with ISO 26262 standard and it is qualified in compliance with AEC-Q100 rev H (Grade1, MSL3).

Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power-up sequencing, to address multiple applications.

2 Features and benefits

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low-voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
- **Based on device options**: low-voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
- **Based on device options**: low-voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 3.6 A peak.
- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
- EMC optimization techniques including spread spectrum, slew rate control, manual frequency tuning
- 2x linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- OFF mode (power-down) with very low quiescent current (10 µA typ)
- 2x input pins for wake-up detection and battery voltage sensing
- Device control via 32 bits SPI with CRC
- Power synchronization pin to operate two FS6600 devices or FS6600 plus an external PMIC
- Scalable ASIL D portfolio with independent monitoring circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, power good, reset and interrupt, built-in self-test, fail-safe output
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.

3 Simplified application diagram

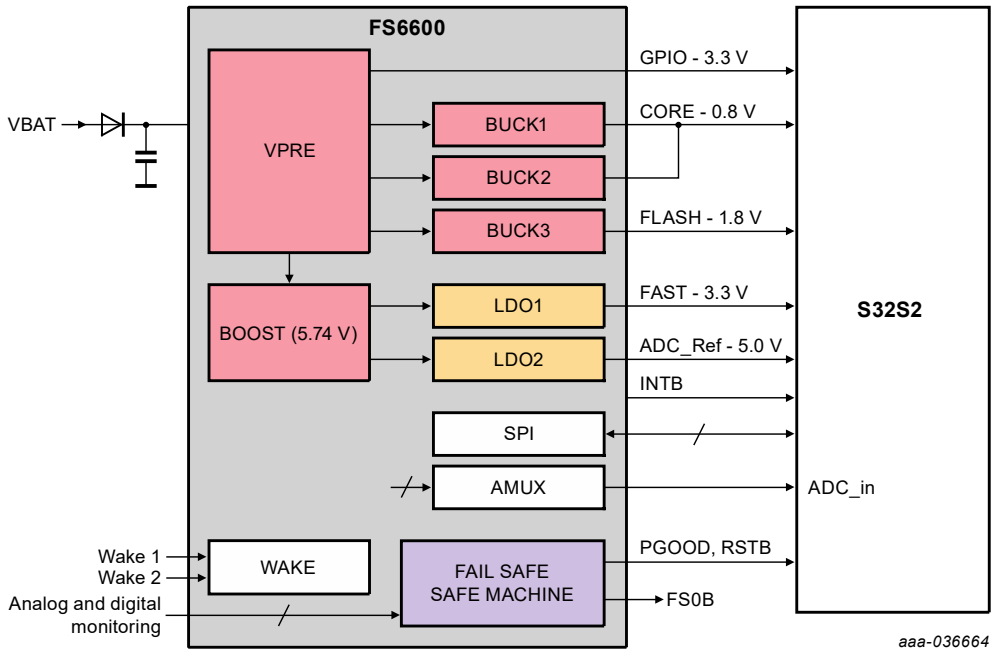


Figure 1. FS6600 superset device of the family

4 Ordering information

Table 1. Ordering information

Part number [1]	Application target	Package		
		Name	Description	Version
MC33FS6600**M0**ES	FS6600 superset covering FS6600 family of devices	HVQFN56	HVQFN56, plastic, thermally enhanced, very thin quad flat package, no leads, step-cut wettable flank, 56 terminals; 0.5 mm nominal pitch, 8 mm x 8 mm x 0.85 mm body	SOT684-23
MC33FS6600**M1**ES	Domain controller			
MC33FS6600**M2**ES	Domain controller			

[1] To order parts in tape and reel, add the R2 suffix to the part number.

M0 parts are non-programmed OTP configurations.

For a custom OTP configuration, contact your local NXP sales representative.

4.1 Main OTP flavors

	MC33FS6600M1ES	MC33FS6600M2ES
VPRE		
Output voltage	3.3 V	3.3 V
Slope compensation	70 mV/µs	70 mV/µs
Current limitation	120 mV	120 mV

	MC33FS6600M1ES	MC33FS6600M2ES
High-side slew rate	PU/PD/900 mA	PU/PD/900 mA
Low-side slew rate	PU/PD/900 mA	PU/PD/900 mA
Switching frequency	455 kHz (Force PWM)	455 kHz (Force PWM)
Phase shifting	delay 0	delay 0
Turn OFF delay	250 µs	250 µs
VBOOST		
Enabled	Yes	Yes
Output voltage	5.74 V	5.74 V
Slope compensation	160 mV/µs	160 mV/µs
Slew rate	500 V/µs	500 V/µs
Compensation resistor	750 kΩ	750 kΩ
Compensation capacitor	125 pF	125 pF
Switching frequency	2.22 MHz	2.22 MHz
Phase shifting	delay 0	delay 0
Behavior in case of TSD	BOOST shutdown	BOOST shutdown
VBUCK1		
Output voltage	0.825 V	0.825 V
Inductor	1 µH	1 µH
Current limitation	4.5 A	4.5 A
Compensation network	48.75 GM	48.75 GM
Switching frequency	2.22 MHz	2.22 MHz
Phase shifting	delay 0	delay 0
Behavior in case of TSD	BUCK1 shutdown	BUCK1 shutdown
Power sequencing slot	Regulator Start and Stop in Slot 4	Regulator Start and Stop in Slot 6
DVS (Soft start)	7.81 mV/µs	7.81 mV/µs
VBUCK2		
Enabled	Yes	Yes
Output voltage	0.825 V	0.825 V
Inductor	1 µH	1 µH
Current limitation	4.5 A	4.5 A
Compensation network	48.75 GM	48.75 GM
Switching frequency	2.22 MHz	2.22 MHz
Multiphase with Buck1	No	yes
Phase shifting	delay 4	delay 4
Behavior in case of TSD	BUCK2 shutdown	BUCK2 shutdown
Power sequencing slot	Regulator Start and Stop in Slot 4	Regulator Start and Stop in Slot 6
DVS (Soft start)	7.81 mV/µs	7.81 mV/µs

	MC33FS6600M1ES	MC33FS6600M2ES
VBUCK3		
Enabled	Yes	Yes
Output voltage	1.8 V	1.8 V
Inductor	1 µH	1 µH
Current limitation	4.5 A	4.5 A
Compensation resistor	Default	Default
Gain control	Default	Default
Switching frequency	2.22 MHz	2.22 MHz
Phase shifting	delay 0	delay 0
Behavior in case of TSD	BUCK3 shutdown	BUCK3 shutdown
Power sequencing slot	Regulator Start and Stop in Slot 0	Regulator Start and Stop in Slot 4
DVS (Soft start)	10.41 mV/µs	10.41 mV/µs
LDO1		
Output voltage	3.3 V	3.3 V
Current limitation	400 mA	400 mA
Behavior in case of TSD	LDO1 shutdown	LDO1 shutdown
Power sequencing slot	Regulator Start and Stop in Slot 2	Regulator Start and Stop in Slot2
LDO2		
Output voltage	5 V	5.0 V
Current limitation	400 mA	400 mA
Behavior in case of TSD	LDO2 shutdown	LDO2 shutdown
Power sequencing slot	Regulator Start and Stop in Slot 6	Regulator Start and Stop in Slot 0
Other		
PSYNC	Disabled	Disabled
TSlot	250 µs	250 µs
Deep Fail-safe (auto retry)	Infinite	Infinite
VSUP power-up threshold	4.9 V	4.9 V
Regulator assigned to VDDIO	External	External
Device ID	tbd	tbd

4.2 Fail-safe OTP flavors

	MC33FS6600M1ES	MC33FS6600M2ES
VCOREMON		
Monitoring voltage	0.825 V	0.825 V
OVTH	112 %	112 %
UVTH	88 %	88 %
OV_DGLT	25 µs	25 µs

	MC33FS6600M1ES	MC33FS6600M2ES
UV_DGLT	15 us	15 µs
SVS_CLAMP	8 steps available	8 steps available
VDDIOMON		
Monitoring voltage	3.3 V	3.3 V
OVTH	112 %	112 %
UVTH	88 %	88 %
OV_DGLT	25 µs	25 µs
UV_DGLT	15 µs	15 µs
VMON1		
OVTH	112 %	112 %
UVTH	88 %	88 %
OV_DGLT	25 µs	25 µs
UV_DGLT	15 µs	15 µs
VMON2		
OVTH	112 %	112 %
UVTH	88 %	88 %
OV_DGLT	25 µs	25 µs
UV_DGLT	15 µs	15 µs
VMON3		
OVTH	112 %	112 %
UVTH	88 %	88 %
OV_DGLT	45 µs	25 µs
UV_DGLT	40 µs	15 µs
VMON4		
OVTH	112 %	112 %
UVTH	88 %	88 %
OV_DGLT	25 µs	25 µs
UV_DGLT	15 µs	15 µs
PGOOD		
VCOREMON	Yes	Yes
VDDIOMON	Yes	Yes
VMON1	Yes	Yes
VMON2	Yes	Yes
VMON3	Yes	Yes
VMON4	Yes	Yes
RSTB	Yes	Yes
ABIST1		

	MC33FS6600M1ES	MC33FS6600M2ES
VCOREMON	Yes	Yes
VDDIOMON	Yes	Yes
VMON1	Yes	Yes
VMON2	Yes	Yes
VMON3	Yes	Yes
VMON4	Yes	Yes
Safety enable		
VMON1	Yes	Yes
VMON2	Yes	Yes
VMON3	Yes	Yes
VMON4	Yes	Yes
FCCU	Yes	Yes
ERRMON	No	Yes
WATCHDOG	Challenger WD	Challenger WD
FLT_RECOVERY	No	No

5 Applications

- Hybrid Vehicle Control Unit
- Electrical traction
- High-Voltage DC/DC Converter
- Battery Management System
- Internal Combustion Engine

6 Block diagram

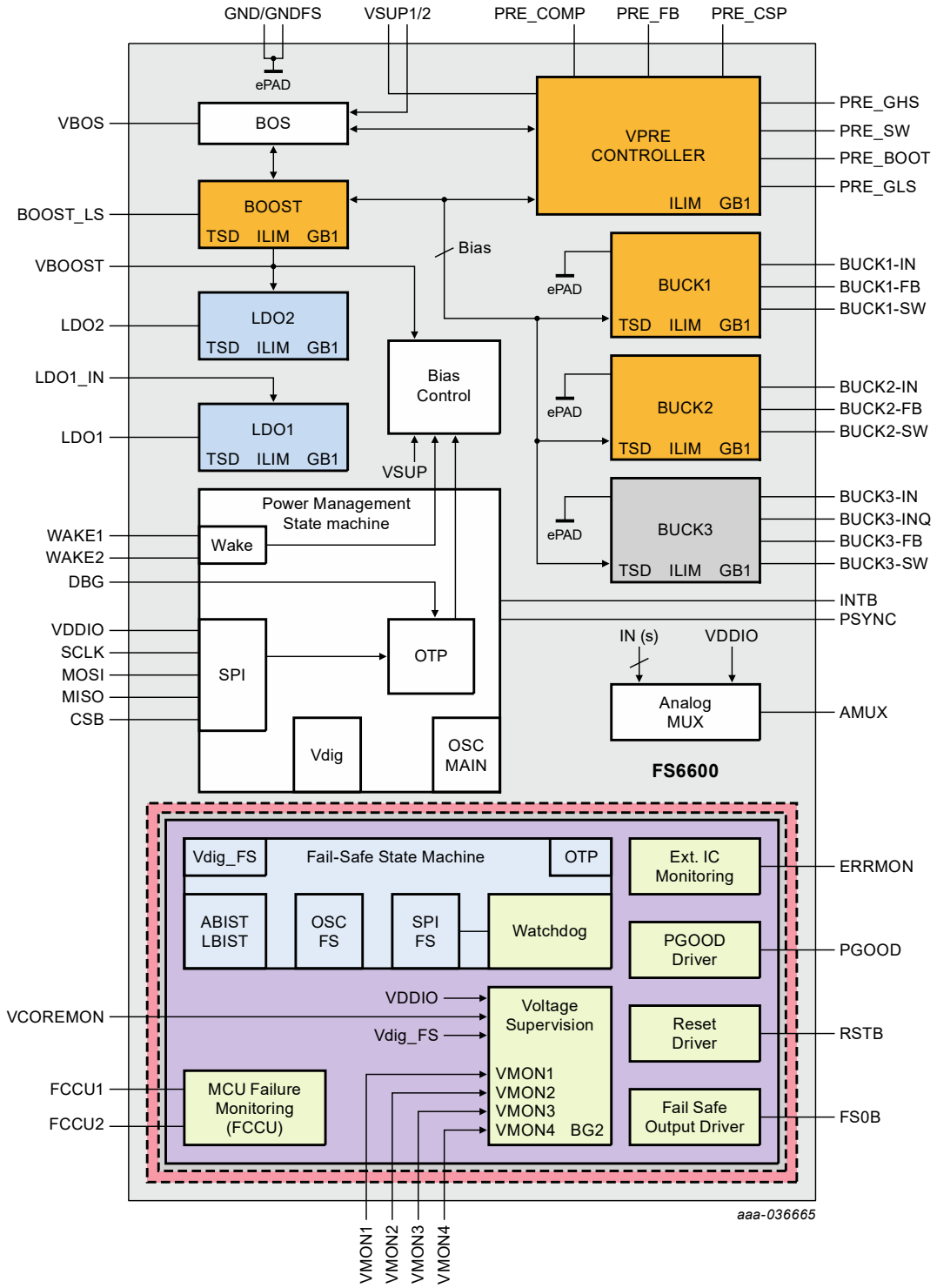


Figure 2. Block diagram

7 Pinning information

7.1 Pinning

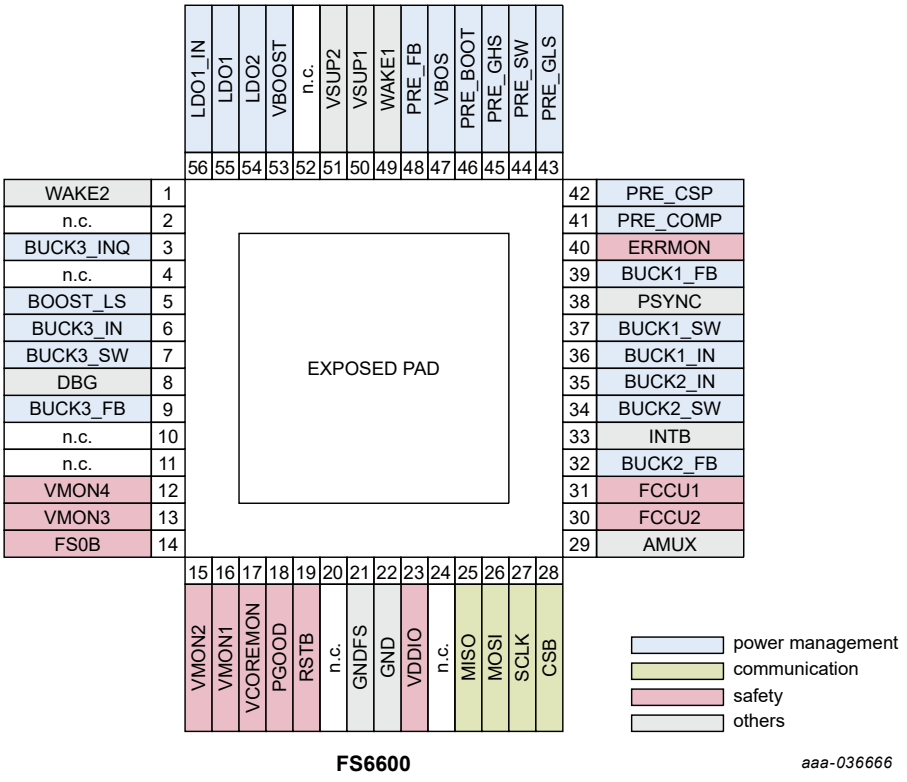


Figure 3. Pin configuration

7.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description [1]
WAKE2	1	A_IN / D_IN	Wake-up input 2 An external serial resistor is required if WAKE2 is a global pin
n.c.	2	n.c.	Not connected pin
BUCK3_INQ	3	A_IN	Low-voltage Buck3 quiet input voltage
n.c.	4	n.c.	Not connected pin
BOOST_LS	5	A_IN	Boost low-side drain of internal MOSFET
BUCK3_IN	6	A_IN	Low-voltage Buck3 input voltage
BUCK3_SW	7	A_OUT	Low-voltage Buck3 switching node
DBG	8	A_IN	Debug mode entry
BUCK3_FB	9	A_IN	Low-voltage Buck3 voltage feedback
n.c.	10	n.c.	Not connected pin
n.c.	11	n.c.	Not connected pin
VMON4	12	A_IN	Voltage monitoring input 4
VMON3	13	A_IN	Voltage monitoring input 3

Table 2. Pin description...*continued*

Symbol	Pin	Type	Description [1]
FS0B	14	D_OUT	Fail-safe output 0 Active low Open drain structure
VMON2	15	A_IN	Voltage monitoring input 2
VMON1	16	A_IN	Voltage monitoring input 1
VCOREMON	17	A_IN	VCORE monitoring input: Must be connected to Buck1 output voltage
PGOOD	18	D_OUT	Power good output Active low Pull up to VDDIO mandatory
RSTB	19	D_OUT	Reset output Active low The main function is to reset the MCU. Reset input voltage is monitored to detect external reset and fault condition. Pull up to VDDIO mandatory
n.c.	20	n.c.	Not connected pin
GNDFS	21	GND	Fail-safe ground
GND	22	GND	Main ground
VDDIO	23	A_IN	Input voltage for SPI, and AMUX buffers Allow voltage compatibility with MCU I/Os
n.c.	24	n.c.	Not connected pin
MISO	25	D_OUT	SPI Primary In Secondary Out
MOSI	26	D_IN	SPI Primary Out Secondary Input
SCLK	27	D_IN	Clock input
CSB	28	D_IN	Chip select (active low)
AMUX	29	A_OUT	Multiplexed output to connect to MCU ADC Selection of the analog parameter through SPI
FCCU2	30	D_IN	MCU error monitoring input 2
FCCU1	31	D_IN	MCU error monitoring input 1
BUCK2_FB	32	A_IN	Low-voltage Buck2 voltage feedback
INTB	33	D_OUT	Interrupt output
BUCK2_SW	34	A_OUT	Low-voltage Buck2 switching node
BUCK2_IN	35	A_IN	Low-voltage Buck2 input voltage
BUCK1_IN	36	A_IN	Low-voltage Buck1 input voltage
BUCK1_SW	37	A_OUT	Low-voltage Buck1 switching node
PSYNC	38	D_IN/OUT	Power synchronization input/output
BUCK1_FB	39	A_IN	Low-voltage Buck1 voltage feedback
ERRMON	40	D_IN	External IC error monitoring input
PRE_COMP	41	A_IN	VPRE compensation network
PRE_CSP	42	A_IN	VPRE positive current sense input
PRE_GLS	43	A_OUT	VPRE low-side gate driver for external MOSFET
PRE_SW	44	A_OUT	VPRE switching node
PRE_GHS	45	A_OUT	VPRE high-side gate driver for external MOSFET
PRE_BOOT	46	A_IN/OUT	VPRE bootstrap capacitor

Table 2. Pin description...*continued*

Symbol	Pin	Type	Description [1]
VBOS	47	A_OUT	Best of supply output voltage
PRE_FB	48	A_IN	VPRE voltage feedback and negative current sense input
WAKE1	49	A_IN / D_IN	Wake up input 1 An external serial resistor is required if WAKE1 is a global pin
VSUP1	50	A_IN	Power supply 1 of the device An external reverse battery protection diode in series is mandatory
VSUP2	51	A_IN	Power supply 2 of the device An external reverse battery protection diode in series is mandatory
n.c.	52	n.c.	Not connected pin
VBOOST	53	A_IN	VBOOST voltage feedback
LDO2	54	A_OUT	Linear regulator 2 output voltage
LDO1	55	A_OUT	Linear regulator 1 output voltage
LDO1_IN	56	A_IN	Linear regulator 1 input voltage
EP	57	GND	Expose pad (BUCK1, BUCK2 and BUCK3 Low Side GNDs are connected to the expose pad) Must be connected to GND

[1] See Section 8 "Connection of unused pins" for connection of unused pins.

8 Connection of unused pins

Table 3. Connection of unused pins

Pin	Name	Type	Connection if not used
1	WAKE2	A_IN / D_IN	External pulldown to GND
2	n.c.	n.c.	Open
3	BUCK3_INQ	A_IN	Open
4	n.c.	n.c.	Open
5	BOOST_LS	A_IN	See Section 21.5 "VBOOST not populated"
6	BUCK3_IN	A_IN	Open
7	BUCK3_SW	A_OUT	Open
8	DBG	A_IN	**Connection mandatory**
9	BUCK3_FB	A_IN	Open – 1.5 MΩ internal resistor bridge pulldown to GND
10	n.c.	n.c.	External pulldown to GND
11	n.c.	n.c.	External pulldown to GND
12	VMON4	A_IN	Open – 2 MΩ internal pulldown to GND, OTP_VMON4_EN = 0
13	VMON3	A_IN	Open – 2 MΩ internal pulldown to GND, OTP_VMON3_EN = 0
14	FS0B	D_OUT	Open – 2 MΩ internal pulldown to GND
15	VMON2	A_IN	Open – 2 MΩ internal pulldown to GND, OTP_VMON2_EN = 0
16	VMON1	A_IN	Open – 2 MΩ internal pulldown to GND, OTP_VMON1_EN = 0
17	VCOREMON	A_IN	**Connection mandatory**
18	PGOOD	D_OUT	**Connection mandatory**
19	RSTB	D_OUT	**Connection mandatory**
20	n.c.	n.c.	External pulldown to GND

Table 3. Connection of unused pins...*continued*

Pin	Name	Type	Connection if not used
21	GNDFS	GND	**Connection mandatory**
22	GND	GND	**Connection mandatory**
23	VDDIO	A_IN	**Connection mandatory**
24	n.c.	n.c.	Open
25	MISO	D_OUT	Open – push pull structure
26	MOSI	D_IN	Open – 450 kΩ internal pull up to VDDIO
27	SCLK	D_IN	External pulldown to GND
28	CSB	D_IN	Open – 450 kΩ internal pull up to VDDIO
29	AMUX	A_OUT	Open
30	FCCU2	D_IN	Open – 200 kΩ internal pull up to VDDIO
31	FCCU1	D_IN	Open – 800 kΩ internal pulldown to GND
32	BUCK2_FB	A_IN	Open – 1.5 MΩ Internal resistor bridge pulldown to GND
33	INTB	D_OUT	Open – 10 kΩ internal pull up to VDDIO
34	BUCK2_SW	A_OUT	Open
35	BUCK2_IN	A_IN	Open
36	BUCK1_IN	A_IN	**Connection mandatory**
37	BUCK1_SW	A_OUT	**Connection mandatory**
38	PSYNC	D_IN/OUT	External pull up to VBOS
39	BUCK1_FB	A_IN	**Connection mandatory**
40	ERRMON	D_IN	External pulldown to GND
41	PRE_COMP	A_IN	See Section 20.7 "VPRE not populated"
42	PRE_CSP	A_IN	See Section 20.7 "VPRE not populated"
43	PRE_GLS	A_OUT	See Section 20.7 "VPRE not populated"
44	PRE_SW	A_OUT	See Section 20.7 "VPRE not populated"
45	PRE_GHS	A_OUT	See Section 20.7 "VPRE not populated"
46	PRE_BOOT	A_IN/OUT	See Section 20.7 "VPRE not populated"
47	VBOS	A_OUT	**Connection mandatory**
48	PRE_FB	A_IN	See Section 20.7 "VPRE not populated"
49	WAKE1	A_IN / D_IN	External pulldown to GND
50	VSUP1	A_IN	**Connection mandatory**
51	VSUP2	A_IN	**Connection mandatory**
52	n.c.	n.c.	Open
53	VBOOST	A_OUT	See Section 21.5 "VBOOST not populated"
54	LDO2	A_OUT	Open – power sequence slot 7, OTP_LDO1S[2:0] = ‘111’
55	LDO1	A_OUT	Open – power sequence slot 7, OTP_LDO2S[2:0] = ‘111’
56	LDO1_IN	A_IN	Open
57	EP	GND	**Connection mandatory**

9 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanently damage the device.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltage ratings					
VSUP1/2	DC voltage	power supply VSUP1,2 pins	−0.3	60	V
WAKE1/2	DC voltage	WAKE1,2 pins; external serial resistor mandatory	−1.0	60	V
PRE_SW	DC voltage	PRE_SW pin	−2.0	60	V
	Transient voltage < 20 ns	PRE_SW pin	−3.0	60	V
VMONx, FS0B	DC voltage	VMON1,2,3,4, VCOREMON, FS0B pins	−0.3	60	V
PRE_GHS, PRE_BOOT	DC voltage	PRE_GHS, PRE_BOOT pins	−0.3	65.5	V
DBG	DC voltage	DBG pin	−0.3	10	V
BOOST_LS	DC voltage	BOOST_LS pin	−0.3	8.5	V
VBOOST, LDO1_IN	DC voltage	VBOOST, LDO1_IN pins	−0.3	6.5	V
BUCKx_IN	DC voltage	BUCK1_IN, BUCK2_IN, BUCK3_IN, BUCK3_INQ	−1.0	5.5	V
BUCKx_IN	Transient voltage < 3 µs	BUCK1_IN, BUCK2_IN, BUCK3_IN, BUCK3_INQ	−1.0	6.5	V
BUCKx_SW	Transient voltage < 20 ns	BUCK1_SW, BUCK2_SW, BUCK3_SW	−2.0	6.5	V
All other pins	DC voltage	at all other pins	−0.3	5.5	V
Current ratings					
I_WAKE	Maximum current capability	WAKE1,2	−5.0	5.0	mA
I_SUP	Maximum current capability	VSUP1,2	−5.0	—	mA

10 Electrostatic discharge

10.1 Human body model (JESD22/A114)

The device is protected up to ±2 kV, according to the human body model standard with 100 pF and 1.5 kΩ. This protection is ensured at all pins.

10.2 Charged device model

The device is protected up to ±500 V, according to the AEC Q100 - 011 charged device model standard. This protection is ensured at all pins.

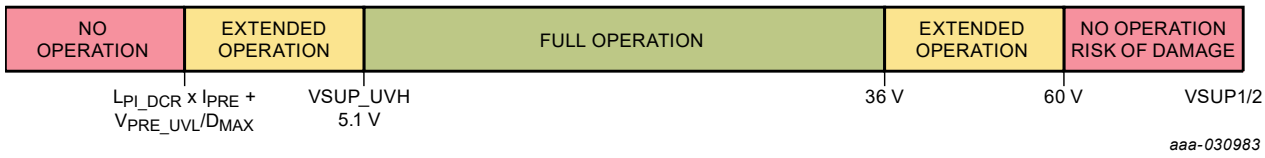
10.3 Discharged contact test

The device is protected up to ±8 kV, according to the following discharged contact tests.

Discharged contact test (IEC61000-4-2) at 150 pF and 330 Ω
Discharged contact test (ISO10605.2008) at 150 pF and 2 kΩ
Discharged contact test (ISO10605.2008) at 330 pF and 2 kΩ

This protection is ensured at VSUP1, VSUP2, WAKE1, WAKE2, FS0B pins.

11 Operating range



Assumptions

L_{PI_DCR} = 30 mΩ
D_{MAX} = 98.18 % with F_{PRE_SW} = 455 kHz and $T_{PRE\_OFF\_MIN}$ = 40 ns
I_{PRE} = 3.0 A
V_{RBD} = 0.56 V
VBAT_min = 3.4 V when VPRE = V_{PRE_UVL}

Figure 4. Operating range

- Below VSUP_UVH threshold, the extended operation range depends on VPRE output voltage configuration and external components.
  - When VPRE is configured at 5.0 V, VPRE may not remain in its regulation range
  - VSUP minimum voltage depends on external components (L_{PI_DCR}) and application conditions (I_{PRE}, F_{PRE_SW})
- When VPRE is switching at 455 kHz, the FS6600 maximum continuous operating voltage is 36 V. It has been validated at 48 V for limited duration of 15 minutes at room temperature to satisfy the jump-start requirement of 24 V applications. It can sustain 58 V load dump without external protection.
- When VPRE is switching at 2.2 MHz, the FS6600 maximum continuous operating voltage is 18 V. It is validated at 26 V for limited duration of 2 minutes at room temperature to satisfy the jump-start requirement of 12 V applications and 35 V load dump.

12 Thermal ratings

Table 5. Thermal ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$R_{\theta JA}$	Thermal resistance junction to ambient	2s2p circuit board [1]	—	31	°C/W
$R_{\theta JA}$	Thermal resistance junction to ambient	2s6p circuit board [1]	—	23	°C/W
$R_{\theta JB}$	Thermal resistance junction to board	2s2p circuit board [1]	—	15	°C/W
$R_{\theta JB}$	Thermal resistance junction to board	2s6p circuit board [1]	—	10	°C/W
$R_{\theta JC\_BOT}$	Thermal resistance junction to case bottom	between the die and the solder pad on the bottom of the package [1]	—	1	°C/W
$R_{\theta JP\_TOP}$	Thermal resistance junction to package top	between package top and the junction temperature [1]	—	3	°C/W
T_A	Ambient temperature (Grade 1)		−40	125	°C
T_J	Junction temperature (Grade 1)		−40	150	°C
T_{STG}	Storage temperature		−55	150	°C

[1] per JEDEC JESD51-2 and JESD51-8

13 Characteristics

Table 6. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Power supply					
I_{SUP_NORMAL}	Current in Normal mode, all regulators ON (I_{OUT} = 0)	—	15	25	mA
$I_{SUP\_STANDBY}$	Current in Standby mode, all regulators OFF except VBOS	—	5	10	mA
I_{SUP_OFF1}	Current in OFF mode (power-down), T_A < 85 °C	—	10	15	µA
I_{SUP_OFF2}	Current in OFF mode (power-down), T_A = 125 °C	—	—	25	µA
V_{SUP_UV7}	VSUP undervoltage threshold (7.0 V)	7.2	7.5	7.8	V
V_{SUP_UVH}	VSUP undervoltage threshold high (during power-up and Vsup rising) OTP_VSUP_CFG = 0	4.7	—	5.1	V
	VSUP undervoltage threshold high (during power-up and Vsup rising) OTP_VSUP_CFG = 1	6.0	—	6.4	V
V_{SUP_UVL}	VSUP undervoltage threshold low (during power-up and Vsup falling) OTP_VSUP_CFG = 0	4.0	—	4.4	V
	VSUP undervoltage threshold low (during power-up and Vsup falling) OTP_VSUP_CFG = 1	5.3	—	5.7	V
T_{SUP_UV}	V_{SUP_UV7}, V_{SUP_UVH} and V_{SUP_UVL} filtering time	6.0	10	15	µs

14 Functional description

The FS6600 device has two independent logic blocks. The main state machine manages the power management, the Standby mode and the wake-up sources. The fail-safe state machine manages the monitoring of the power management, the monitoring of the MCU and the monitoring of an external IC.

14.1 Simplified functional state diagram

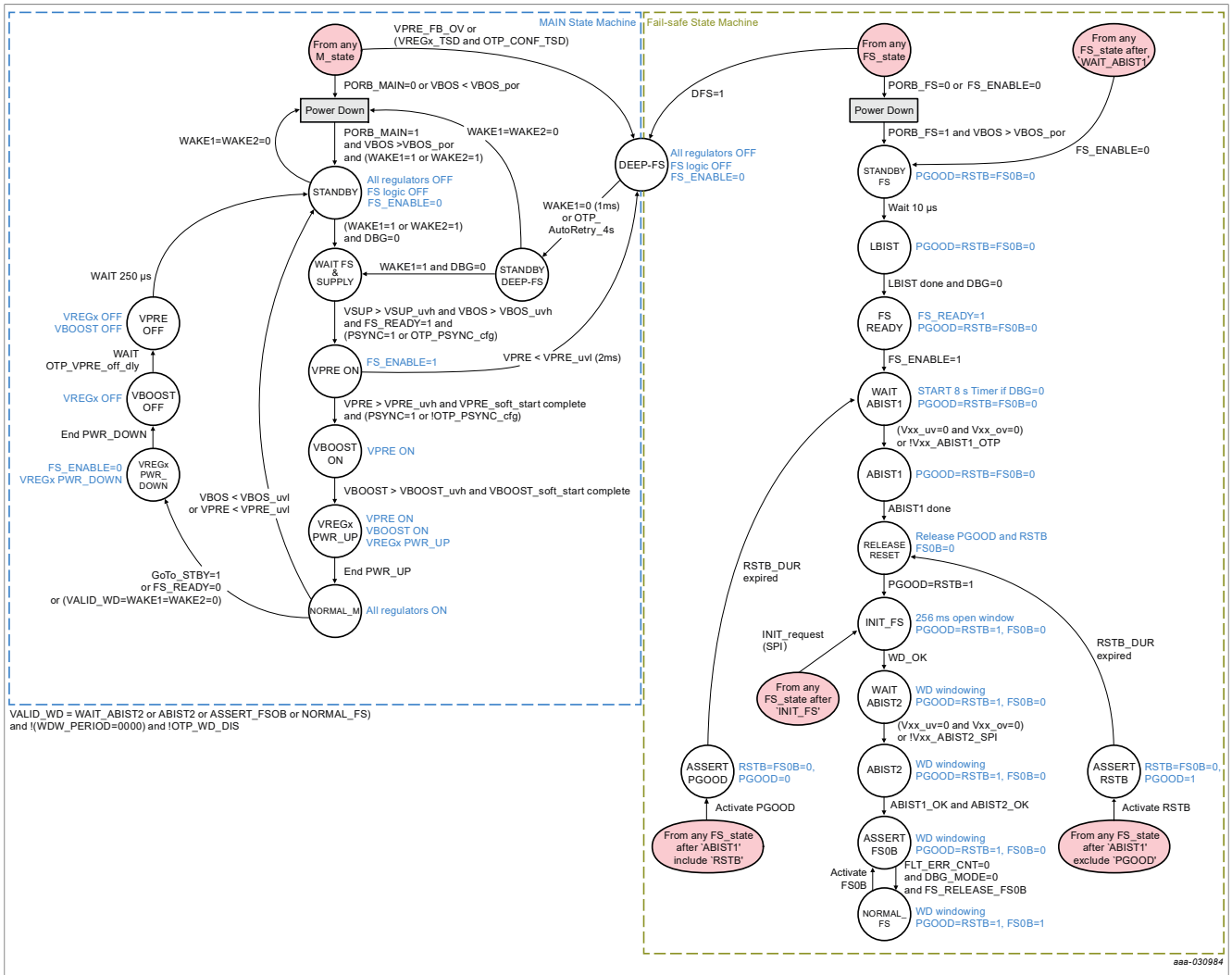


Figure 5. Simplified functional state diagram

VALID_WD = 0

- when the WD is disabled by OTP
  OR
- when the WD period = 0
  OR
- when the device is in INIT_FS sate

VALID_WD = 1

- when the WD period is different than 0
  AND
- when the device is in one of the following states: WAIT_ABIST2 or ABIST2 or ASSERT_FS0B or NORMAL_FS

14.2 Main state machine

The FS6600 starts when VSUP > V_{SUP_UVH} and WAKE1 or WAKE2 > $WAKE12_{VIH}$ with VBOS first, followed by VPRE, VBOOST and the power-up sequencing from the OTP programming for the remaining regulators if PSYNC pin is pulled up to VBOS. If during the power-up sequence VSUP < V_{SUP_UVL}, the device goes back to Standby mode. When the power up is finished, the main state machine is in Normal_M mode which is the application running mode with all the regulators ON and V_{SUP_UVL} has no effect even if VSUP < V_{SUP_UVL}. See Figure 4 for the minimum operating voltage.

The power-up sequence can be synchronized with another PMIC using the PSYNC pin. This synchronization is done in order to stop before or after VPRE is ON and then waiting for PMIC feedback on PSYNC pin before allowing FS6600 to continue its power-up sequence. See Section 27.3 "PSYNC for two FS6600" for more details on PSYNC pin. If the power-up sequence from VPRE ON to NORMAL_M is not completed within 1 second, the device goes back to Standby mode. VPRE restarts when VSUP > V_{SUP_UVH} and WAKE1 or WAKE2 > $WAKE12_{VIH}$.

The device goes to Standby mode by an SPI command from the MCU. If the WD is disabled by the OTP_WD_DIS bit, for an application without MCU, the device goes to Standby mode when both WAKE1 and WAKE 2 = 0. The device goes to Standby mode following the power-down sequence to stop all the regulators in the reverse order of the power-up sequence. VPRE shutdown can be delayed from 250 µs to 32 ms by OTP_VPRE_off_dly bit in case VPRE is supplying an external PMIC to wait its power-down sequence completion.

In case of loss of VPRE (VPRE < V_{PRE_UVL}) or loss of VBOS (VBOS < V_{BOS_UVL}), the device stops and goes directly to Standby mode without a power-down sequence. VPRE restarts when VSUP > V_{SUP_UVH} and WAKE1 or WAKE2 > $WAKE12_{VIH}$.

In case of VPRE_FB_OV detection, or TSD detection on a regulator depending on OTP_conf_tsd[5:0] bits configuration, or deep fail-safe request from the fail-safe state machine when DFS = 1, the device stops and goes directly to DEEP-FS mode without power-down sequence.

Exit of DEEP-FS mode is only possible by WAKE1 = 0 or after 4 s if the auto retry feature is activated by the OTP_Autorety_en bit. The number of auto retries can be limited to 15 or infinite depending on OTP_Autoretry_infinite bit. VPRE restarts when VSUP > V_{SUP_UVH} and WAKE1 or WAKE2 > $WAKE12_{VIH}$.

14.3 Fail-safe state machine

The fail-safe state machine starts with LBIST execution when VBOS > V_{BOS_POR}. When the LBIST is done, the 8 s timer monitoring the RSTB pin starts and the ABIST1 is automatically executed when all the regulators assigned to ABIST1 have passed their undervoltage threshold. When the ABIST1 is done, RSTB and PGOOD pins are released and the initialization of the device is opened for 256 ms. ABIST1 fail does not prevent RSTB and PGOOD release but maintains FS0B asserted.

The first good watchdog refresh closes the INIT_FS. Continuous watchdog refresh is now required. The device waits for SPI command to execute the ABIST2. When the ABIST2 is done and passes, the fault counter must be cleared with the appropriate number of good watchdog refreshes in order to release the FS0B pin per the procedure described in Section 31.8.4 "FS0B release".

When FS0B pin is released, the device is ready for application running mode with all the selected monitoring activated. From this point, the FS6600 reacts by asserting the safety pins (PGOOD, RSTB and FS0B) according to its configuration when a fault is detected. The safety pins hierarchical priority is 1-PGOOD, 2-RSTB, 3-FS0B.

14.4 Power sequencing

VPRE is the first regulator to start automatically, followed by the BOOST, before the SLOT_0. The other regulators are starting from the OTP power sequencing configuration. Seven slots are available to program the start-up sequence of BUCK1, BUCK 2, BUCK 3, LDO1 and LDO2 regulators. The delay between each slot is

configurable to 250 µs or 1 ms by OTP using the OTP_Tslot bit to accommodate the different ramp up speed of BUCK1, BUCK2 and BUCK3.

The power-up sequence starts at SLOT_0 and ends at SLOT_7 while the power-down sequence is executed in reverse order. This sequence means that all regulators set to SLOT_7 and powered up by SPI, will be stopped first during the power-down sequence. All the SLOTs are executed even if there is no regulator assigned to a SLOT. The regulators assigned to SLOT_7 are not started during the power-up sequence. They can be started (or not) later in NORMAL_M mode with a SPI command to write in M_REG_CTRL1 register if they were enabled by OTP.

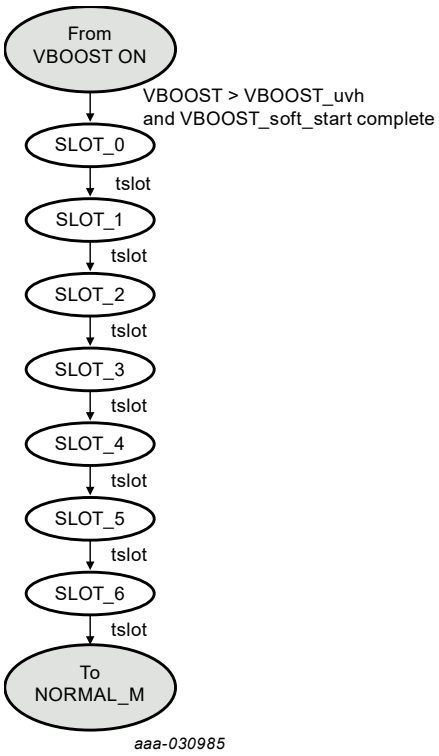


Figure 6. Power sequencing (VREGx PWR_UP)

Each regulator is assigned to a SLOT by OTP configuration using OTP_VB1S[2:0] for BUCK1, OTP_VB2S[2:0] for BUCK2, OTP_VB3S[2:0] for BUCK3, OTP_LDO1S[2:0] for LDO1 and OTP_LDO2S[2:0] for LDO2.

The different soft start duration of the BUCKs and the LDOs should be considered in the SLOT assignment to achieve the correct sequence.

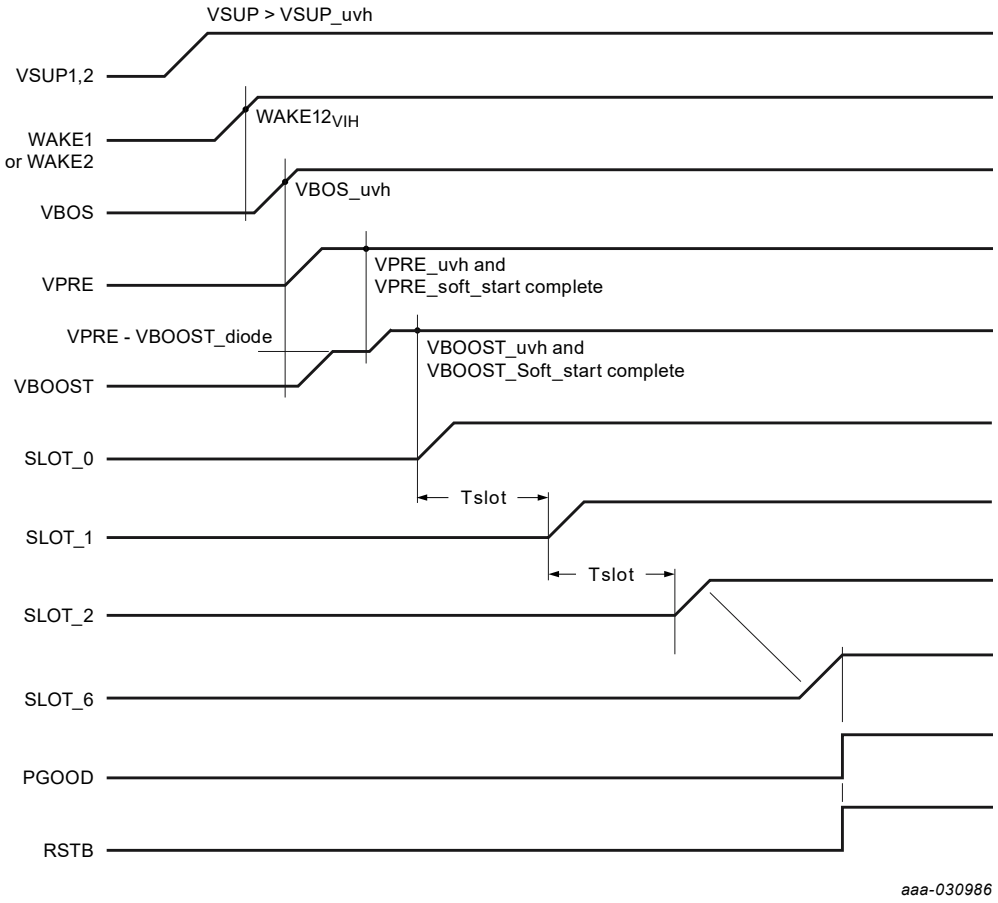


Figure 7. power-up sequence example

PGOOD and RSTB release depends on the combination of the power-up sequence and what regulator is assigned to PGOOD and ABIST1 through the voltage monitoring connection (VCOREMON, VDDIOMON and VMONx). The FS85_FS84_OTP_Config file used to generate the OTP configuration of the device draws the power-up sequence of an OTP configuration in the OTP_conf_summary sheet.

14.5 Debug mode

The FS6600 enters in Debug mode with the sequence described in Figure 8:

1. DBG pin = V_{DBG} and VSUP > V_{SUP_UVH}
2. WAKE1 or WAKE2 > $WAKE12_{VIH}$

V_{DBG} and VSUP can come up at the same time as long as WAKE1 or WAKE2 comes up last.

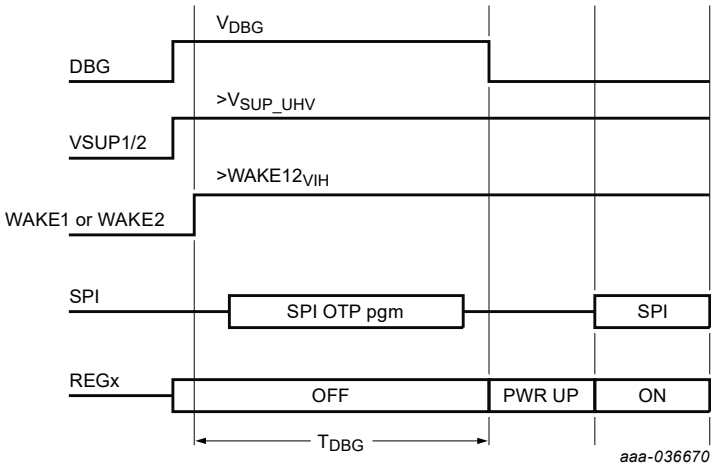


Figure 8. Debug mode entry

When the DBG pin is asserted low after T_{DBG} without SPI command access, the device starts with the internal OTP configuration.

If V_{DBG} voltage is maintained at DBG pin, a new OTP configuration can be emulated or programmed by SPI communication using NXP FlexGUI interface and NXP socket EVB. When the OTP process is completed, the device starts with the new OTP configuration when DBG pin is asserted low. The OTP emulation/programming is possible during engineering development only. The OTP programming in production is done by NXP only.

In Debug mode, the watchdog window is fully opened, the deep fail-safe request from the fail-safe state machine (DFS = 1) is masked, the 8 s timer monitoring of RSTB pin is disabled, the fail-safe output pin FS0B cannot be released, and the OTP emulation and programming of a raw device by SPI is possible.

In Debug mode, no watchdog refresh is required. It allows an easy debug of the hardware and software routines like SPI commands. However, the whole watchdog functionality is kept on (seed, LFSR, WD refresh counter, WD error counter...). WD errors are detected and counted with reaction on RSTB pin.

To release FS0B without taking care of the watchdog window, disable the watchdog window with WDW_PERIOD[3:0] = '0000' in FS_WD_WINDOW register before leaving the Debug mode. To leave Debug mode, write DBG_EXIT bit = '1' in FS_STATES register.

Refer to AN12333 for more details on Debug mode entry implementation.

Table 7. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
V_{DBG}	Debug mode entry threshold	4.5	—	5.5	V
T_{DBG}	Debug mode entry filtering time (minimum duration of DBG = V_{DBG} after VSUP > V_{SUP_UVH} and WAKE1 or WAKE2 > $WAKE12_{VIH}$	7	—	—	ms

14.6 Flowcharts

The flowcharts describe how the device starts and what to do when the RSTB pin is released.

14.6.1 Application flowchart

In application mode, the Debug pin is connected to GND and watchdog refresh is required as soon as INIT_FS is closed.

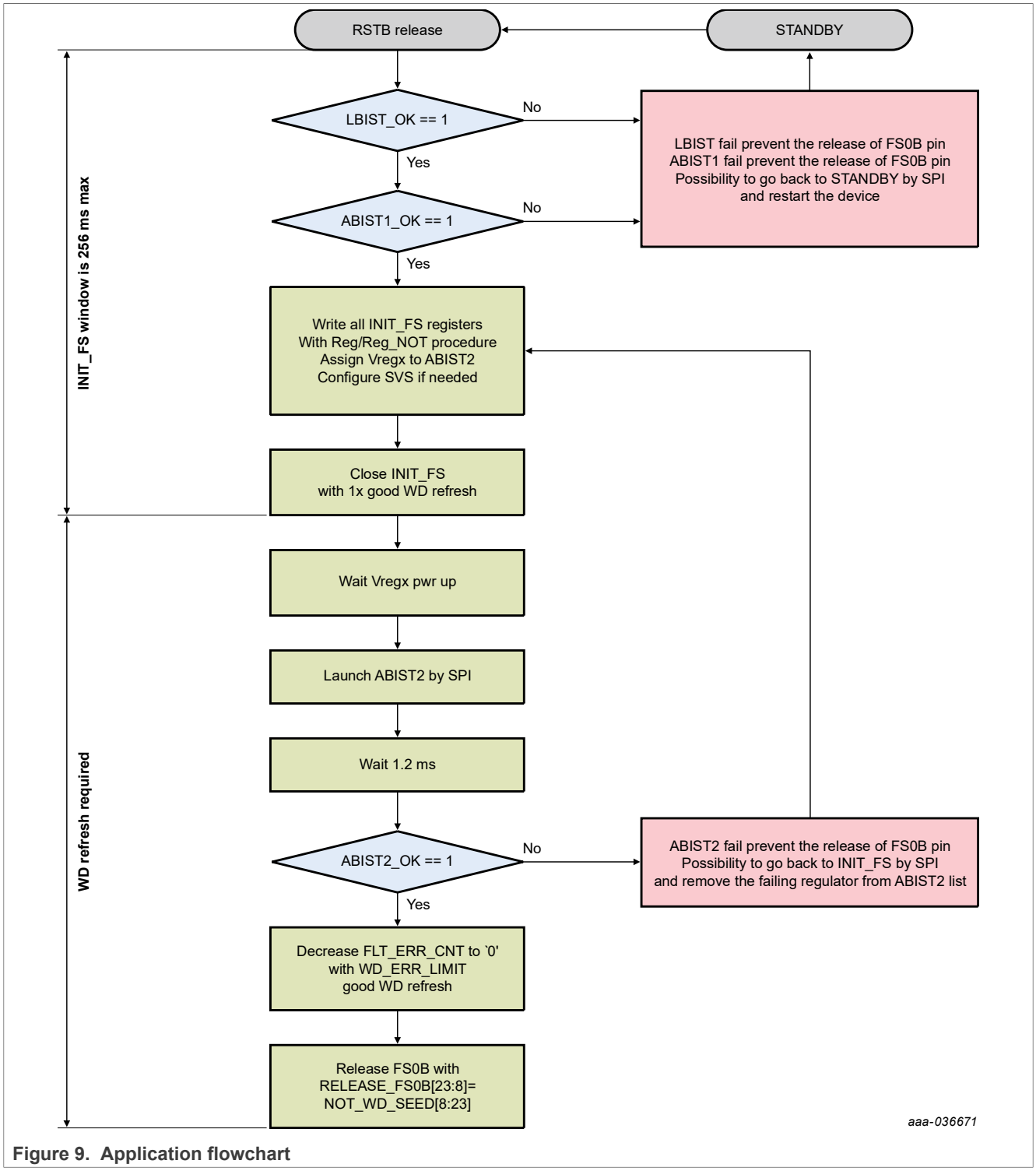


Figure 9. Application flowchart

14.6.2 Debug flowchart

In Debug mode, the Debug pin is managed according to Section 14.4 "Power sequencing" description. The watchdog window is fully opened, and the watchdog refresh is not required.

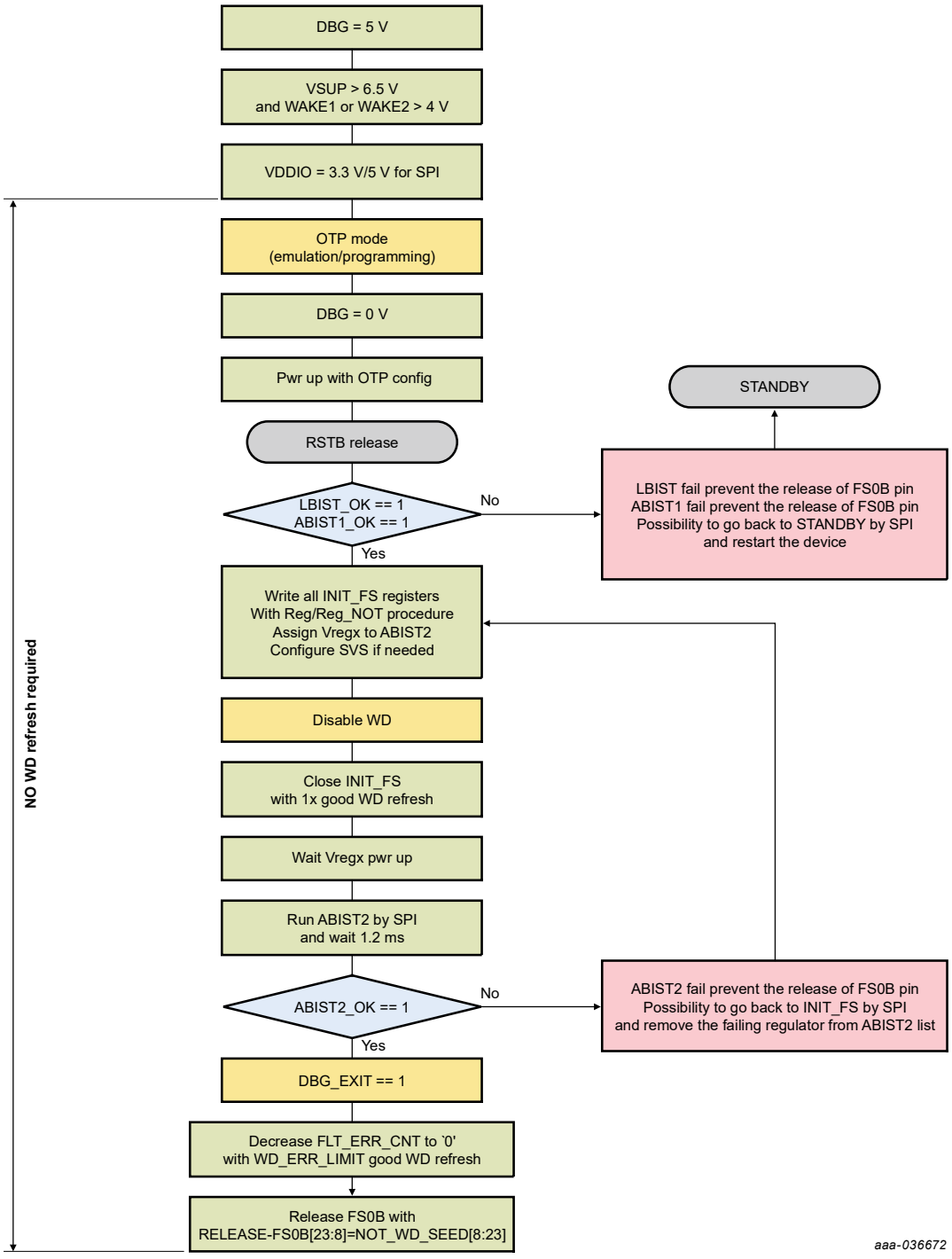


Figure 10. Debug flowchart

Note: *Disabling the watchdog before INIT_FS closure and Debug mode exit by SPI allows FS0B release. Otherwise, FS0B is stuck low in Debug mode.*

15 Register mapping

In the M/FS column, blue shaded cells represent main registers (M_...).
Lime shaded cells represent fail safe registers (FS_...).

Register	M/FS	Address						R/W SPI	Read / Write	Reference
		Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0			
M_FLAG	0	0	0	0	0	0	0	0/1	Read / Write	Section 16.3
M_MODE	0	0	0	0	0	0	1	0/1	Read / Write	Section 16.4
M_REG_CTRL1	0	0	0	0	0	1	0	0/1	Read / Write	Section 16.5
M_REG_CTRL2	0	0	0	0	0	1	1	0/1	Read / Write	Section 16.6
M_AMUX	0	0	0	0	1	0	0	0/1	Read / Write	Section 16.7
M_CLOCK	0	0	0	0	1	0	1	0/1	Read / Write	Section 16.8
M_INT_MASK1	0	0	0	0	1	1	0	0/1	Read / Write	Section 16.9
M_INT_MASK2	0	0	0	0	1	1	1	0/1	Read / Write	Section 16.10
M_FLAG1	0	0	0	1	0	0	0	0/1	Read / Write	Section 16.11
M_FLAG2	0	0	0	1	0	0	1	0/1	Read / Write	Section 16.12
M_VMON_REGX	0	0	0	1	0	1	0	0/1	Read / Write	Section 16.13
M_LVB1_SVS	0	0	0	1	0	1	1	0	Read only	Section 16.14
M_MEMORY0	0	1	0	0	0	1	1	0/1	Read / Write	Section 16.15
M_MEMORY1	0	1	0	0	1	0	0	0/1	Read / Write	Section 16.16
M_DEVICEID	0	1	0	0	1	0	1	0	Read only	Section 16.17
FS_GRL_FLAGS	1	0	0	0	0	0	0	0	Read only	Section 17.3
FS_I_OVUV_SAFE_REACTION1	1	0	0	0	0	0	1	0/1	Write during INIT then Read only	Section 17.4
FS_I_NOT_OVUV_SAFE_REACTION1	1	0	0	0	0	1	0	0/1	Write during INIT then Read only	
FS_I_OVUV_SAFE_REACTION2	1	0	0	0	0	1	1	0/1	Write during INIT then Read only	Section 17.5
FS_I_NOT_OVUV_SAFE_REACTION2	1	0	0	0	1	0	0	0/1	Write during INIT then Read only	
FS_I_WD_CFG	1	0	0	0	1	0	1	0/1	Write during INIT then Read only	Section 17.6
FS_I_NOT_WD_CFG	1	0	0	0	1	1	0	0/1	Write during INIT then Read only	
FS_I_SAFE_INPUTS	1	0	0	0	1	1	1	0/1	Write during INIT then Read only	Section 17.7
FS_I_NOT_SAFE_INPUTS	1	0	0	1	0	0	0	0/1	Write during INIT then Read only	
FS_I_FSSM	1	0	0	1	0	0	1	0/1	Write during INIT then Read only	Section 17.8
FS_I_NOT_FSSM	1	0	0	1	0	1	0	0/1	Write during INIT then Read only	
FS_I_SVS	1	0	0	1	0	1	1	0/1	Write during INIT then Read only	Section 17.9
FS_I_NOT_SVS	1	0	0	1	1	0	0	0/1	Write during INIT then Read only	
FS_WD_WINDOW	1	0	0	1	1	0	1	0/1	Read / Write	Section 17.10
FS_NOT_WD_WINDOW	1	0	0	1	1	1	0	0/1	Read / Write	
FS_WD_SEED	1	0	0	1	1	1	1	0/1	Read / Write	Section 17.11
FS_WD_ANSWER	1	0	1	0	0	0	0	0/1	Read / Write	Section 17.12
FS_OVUVREG_STATUS	1	0	1	0	0	0	1	0/1	Read / Write	Section 17.13
FS_RELEASE_FS0B	1	0	1	0	0	1	0	0/1	Read / Write	Section 17.14
FS_SAFE_IOS	1	0	1	0	0	1	1	0/1	Read / Write	Section 17.15
FS_DIAG_SAFETY	1	0	1	0	1	0	0	0/1	Read / Write	Section 17.16
FS_INTB_MASK	1	0	1	0	1	0	1	0/1	Read / Write	Section 17.17
FS_STATES	1	0	1	0	1	1	0	0/1	Read / Write	Section 17.18

16 Main register mapping

16.1 Main writing registers overview

Table 8. Main writing registers overview

Logic	Register name	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
Main	M_FLAG	0	0	0	0	0	0	0	0
		0	0	0	SPI_M_CLK	SPI_M_REQ	SPI_M_CRC	0	0
	M_MODE	0	0	0	0	0	0	0	0
		0	RESERVED	0	0	0	W2DIS	W1DIS	GoTo_STBY
	M_REG_CTRL1	VPRE_PD_DIS	VPDIS	BOOSTDIS	BUCK1DIS	BUCK2DIS	BUCK3DIS	LDO1DIS	LDO2DIS
		0	VPEN	BOOSTEN	BUCK1EN	BUCK2EN	BUCK3EN	LDO1EN	LDO2EN
	M_REG_CTRL2	VBSTSR[1:0]		BOOSTT SDCFG	BUCK1TSDCFG	BUCK2TSDCFG	BUCK3TSDCFG	LDO1TSDCFG	LDO2TSDCFG
		0	0	0	VPRESRLS		0	VPRESRHS	
	M_AMUX	0	0	0	0	0	0	0	0
		0	0	RATIO	AMUX[4:0)				
	M_CLOCK	MOD_CONF	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	MOD_EN	CLK_TUNE[3:0]			
	M_INT_MASK1	0	VPREOC_M	0	BUCK1OC_M	BUCK2OC_M	BUCK3OC_M	LDO1OC_M	LDO2OC_M
		0	0	BOOSTTSD_M	BUCK1TSD_M	BUCK2TSD_M	BUCK3TSD_M	LDO1TSD_M	LDO2TSD_M
	M_INT_MASK2	0	0	0	0	VBOOSTOV_M	VBOSUVH_M	COM_M	VPRE_ FB_OV_M
		VBOOST_ UVH_M	VSUPUV7	0	VPREUVH	VSUPUV	VSUPUVH	WAKE1_M	WAKE2_M
	M_FLAG1	VBOSUVH	VBOOSTUVH	VPREOC	BUCK1OC	BUCK2OC	BUCK3OC	LDO1OC	LDO2OC
		0	VBOOSTOV	VBOOSTOT	BUCK1OT	BUCK2OT	BUCK3OT	LDO1OT	LDO2OT
	M_FLAG2	VPRE_FB_OV	VSUPUV7	0	0	0	0	0	0
		VPREUVL	VPREUVH	VSUPUVL	VSUPUVH	0	0	WK2FLG	WK1FLG
	M_VMON_REGX	0	0	0	0	VMON4_REG[2:0]			VMON3_ REG[2:0]
		VMON3_REG[1:0]		VMON2_REG[2:0]			VMON1_REG[2]		
	M_MEMORY0	MEMORY0[15:0]							
	M_MEMORY1	MEMORY1[15:0]							

16.2 Main reading registers overview

Table 9. Main reading registers overview

Logic	Register name	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
Main	M_FLAG	COM_ERR	WU_G	VPRE_G	VBOOST_G	VBUCK1_G	VBUCK2_G	VBUCK3_G	VLDO1_G
		VLDO2_G	0	0	SPI_M_CLK	SPI_M_REQ	SPI_M_CRC	0	0
	M_MODE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PLL_LOCK_RT
		RESERVED	RESERVED	MAIN_NORMAL	RESERVED	RESERVED	W2DIS	W1DIS	RESERVED
	M_REG_CTRL1	VPRE_PD_DIS	VPDIS	BOOSTDIS	BUCK1DIS	BUCK2DIS	BUCK3DIS	LDO1DIS	LDO2DIS
		0	VPEN	BOOSTEN	BUCK1EN	BUCK2EN	BUCK3EN	LDO1EN	LDO2EN
	M_REG_CTRL2	VBSTSR[1:0]		BOOSTT SDCFG	BUCK1TSDCFG	BUCK2TSDCFG	BUCK3TSDCFG	LDO1TSDCFG	LDO2TSDCFG
		RESERVED	RESERVED	RESERVED	VPRESRLS		RESERVED	VPRESRHS	
	M_AMUX	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RATIO	AMUX[4:0]				
	M_CLOCK	MOD_CONF	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	MOD_EN	CLK_TUNE[3:0]			
	M_INT_MASK1	RESERVED	VPREOC_M	RESERVED	BUCK1OC_M	BUCK2OC_M	BUCK3OC_M	LDO1OC_M	LDO2OC_M
		RESERVED	RESERVED	BOOSTTSD_M	BUCK1TSD_M	BUCK2TSD_M	BUCK3TSD_M	LDO1TSD_M	LDO2TSD_M
	M_INT_MASK2	RESERVED	RESERVED	RESERVED	RESERVED	VBOOSTOV_M	VBOSUVH_M	COM_M	VPRE_ FB_OV_M
		VBOOST_ UVH_M	VSUPUV7	RESERVED	VPREUVH	VSUPUV	VSUPUVH	WAKE1_M	WAKE2_M
	M_FLAG1	VBOSUVH	VBOOSTUVH	VPREOC	BUCK1OC	BUCK2OC	BUCK3OC	LDO1OC	LDO2OC
		RESERVED	VBOOSTOV	VBOOSTOT	BUCK1OT	BUCK2OT	BUCK3OT	LDO1OT	LDO2OT
	M_FLAG2	VPRE_FB_OV	VSUPUV7	BOOST_ST	BUCK1_ST	BUCK2_ST	BUCK3_ST	LDO1_ST	LDO2_ST
		VPREUVL	VPREUVH	VSUPUVL	VSUPUVH	WK2RT	WK1RT	WK2FLG	WK1FLG
	M_VMON_REGX	RESERVED	RESERVED	RESERVED	RESERVED	VMON4_REG[2:0]			VMON3_ REG[2:0]
		VMON3_REG[1:0]		VMON2_REG[2:0]			VMON1_REG[2]		
	M_LVB1_SVS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	LVB1_SVS[4:0]				
	M_MEMORY0	MEMORY0[15:0]							
	M_MEMORY0	MEMORY1[15:0]							
	M_DEVICEID	FM_REV[3:0]				MM_REV[3:0]			
		DEVICEID[7:0]							

16.3 M_FLAG register

Table 10. M_FLAG register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	0	0	0	0	0
Read	COM_ERR	WU_G	VPRE_G	VBOOST_G	VBUCK1_G	VBUCK2_G	VBUCK3_G	VLDO1_G
Reset	0	1	1	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	SPI_M_CLK	SPI_M_REQ	SPI_M_CRC	Don't care	Don't care
Read	VLDO2_G	0	0	SPI_M_CLK	SPI_M_REQ	SPI_M_CRC	0	0
Reset	0	0	0	0	0	0	0	0

Table 11. M_FLAG register bit description

Bit	Symbol	Description
23	COM_ERR	Report an error in the Communication (SPI) **COM_ERR** = SPI_M_CRC or SPI_M_CLK or SPI_M_REQ or FS_COM_G
		0 No failure
		1 Failure
		Reset condition: Real-time information - cleared when all individual bits are cleared
22	WU_G	Report a wake-up event by WAKE1 or WAKE2 **WU_G** = WK1FLG or WK2FLG
		0 No wake event
		1 Wake event
		Reset condition: Real-time information - cleared when all individual bits are cleared
21	VPRE_G	Report an event on VPRE (status change or failure) **VPRE_G** = VPREOC or VPREUVH or VPREUVL or VPRE_FB_OV
		0 No event
		1 Event occurred
		Reset condition: Real-time information - cleared when all individual bits are cleared
20	VBOOST_G	Report an event on VBOOST (status change or failure) **VBOOST_G** = VBOOSTOT or BOOSTOV
		0 No event
		1 Event occurred
		Reset condition: Real-time information - cleared when all individual bits are cleared
19	VBUCK1_G	Report an event on BUCK1 (status change or failure) **VBUCK1_G** = BUCK1OC or BUCK1OT
		0 No event
		1 Event occurred
		Reset condition: Real-time information - cleared when all individual bits are cleared
18	VBUCK2_G	Report an event on BUCK2 (status change or failure) **VBUCK2_G** = BUCK2OC or BUCK2OT
		0 No event
		1 Event occurred
		Reset condition: Real-time information - cleared when all individual bits are cleared
17	VBUCK3_G	Report an event on BUCK3 (status change or failure) **VBUCK3_G** = BUCK3OC or BUCK3OT
		0 No event
		1 Event occurred
		Reset condition: Real-time information - cleared when all individual bits are cleared
16	VLDO1_G	Report an event on LDO1 (status change or failure) **VLDO1_G** = LDO1OC or LDO1OT
		0 No event
		1 Event occurred
		Reset condition: Real-time information

Table 11. M_FLAG register bit description*...continued*

Bit	Symbol	Description
15	VLDO2_G	Report an event on LDO2 (status change or failure) **VLDO2_G** = LDO2OC or LDO2OT
		0 No event
		1 Event occurred
		Reset condition: Real-time information
12	SPI_M_CLK	Main domain SPI SCLK error detection
		0 No error
		1 Wrong number of clock cycles (<32 or >32)
		Reset condition: POR / clear on Write (write '1')
11	SPI_M_REQ	Invalid main domain SPI access (wrong Write or Read, Write to INIT registers in normal mode, wrong address)
		0 No error
		1 SPI violation
		Reset condition: POR / clear on Write (write '1')
10	SPI_M_CRC	Main domain SPI communication CRC issue
		0 No error
		1 Error detected in the SPI CRC
		Reset condition: POR / clear on Write (write '1')

16.4 M_MODE register

Table 12. M_MODE register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PLL_ LOCK_RT
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	RESERVED	0	0	0	W2DIS	W1DIS	GoTo_STBY
Read	RESERVED	RESERVED	MAIN_ NORMAL	RESERVED	RESERVED	W2DIS	W1DIS	RESERVED
Reset	0	0	1	0	0	0	0	0

Table 13. M_MODE register bit description

Bit	Symbol	Description
16	PLL_LOCK_RT	Real-time status of the PPL
		0 PLL not locked
		1 PLL locked
		Reset condition: POR

Table 13. M_MODE register bit description*...continued*

Bit	Symbol	Description
13	MAIN NORMAL	Main state machine status
		0 Main state machine is not in Normal mode
		1 Main state machine is in Normal mode
		Reset condition: POR
10	W2DIS	WAKE2 wake-up disable
		0 Wake-up enable
		1 Wake-up disable
		Reset condition: POR
9	W1DIS	WAKE1 wake-up disable
		0 Wake-up enable
		1 Wake-up disable
		Reset condition: POR
8	GoTo_STBY	Standby mode request
		0 Device remains in current state
		1 Device enters in Standby mode
		Reset condition: POR

16.5 M_REG_CTRL1 register

Table 14. M_REG_CTRL1 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	VPRE_ PD_DIS	VPDIS	BOOSTDIS	BUCK1DIS	BUCK2DIS	BUCK3DIS	LDO1DIS	LDO2DIS
Read	VPRE_ PD_DIS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	VPEN	BOOSTEN	BUCK1EN	BUCK2EN	BUCK3EN	LDO1EN	LDO2EN
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Table 15. M_REG_CTRL1 register bit description

Bit	Symbol	Description
23	VPRE_PD_DIS	Force disable of VPRE pulldown
		0 No effect (VPRE pulldown is automatically controlled by the logic)
		1 VPRE pulldown disable request
		Reset condition: POR

Table 15. M_REG_CTRL1 register bit description*...continued*

Bit	Symbol	Description
22	VPDIS	Disable request of VPRE
		0 No effect (regulator remains in existing state)
		1 VPRE disable request
		Reset condition: POR
21	BOOSTDIS	Disable request of BOOST
		0 No effect (regulator remains in existing state)
		1 BOOST disable request
		Reset condition: POR
20	BUCK1DIS	Disable request of BUCK1
		0 No effect (regulator remains in existing state)
		1 BUCK1 disable request
		Reset condition: POR
19	BUCK2DIS	Disable request of BUCK2
		0 No effect (regulator remains in existing state)
		1 BUCK2 disable request
		Reset condition: POR
18	BUCK3DIS	Disable request of BUCK3
		0 No effect (regulator remains in existing state)
		1 BUCK3 disable request
		Reset condition: POR
17	LDO1DIS	Disable request of LDO1
		0 No effect (regulator remains in existing state)
		1 LDO1 disable request
		Reset condition: POR
16	LDO2DIS	Disable request of LDO2
		0 no effect (regulator remains in existing state)
		1 LDO2 disable request
		Reset condition: POR
14	VPEN	Enable request of VPRE
		0 No effect (regulator remains in existing state)
		1 VPRE enable request (after a VPDIS request)
		Reset condition: POR
13	BOOSTEN	Enable request of BOOST
		0 No effect (regulator remains in existing state)
		1 BOOST enable request
		Reset condition: POR
12	BUCK1EN	Enable request of BUCK1
		0 No effect (regulator remains in existing state)
		1 BUCK1 enable request
		Reset condition: POR

Table 15. M_REG_CTRL1 register bit description*...continued*

Bit	Symbol	Description
11	BUCK2EN	Enable request of BUCK2
		0 No effect (regulator remains in existing state)
		1 BUCK2 enable request
		Reset condition: POR
10	BUCK3EN	Enable request of BUCK3
		0 No effect (regulator remains in existing state)
		1 BUCK3 enable request
		Reset condition: POR
9	LDO1EN	Enable request of LDO1
		0 No effect (regulator remains in existing state)
		1 LDO1 enable request
		Reset condition: POR
8	LDO2EN	Enable request of LDO2
		0 no effect (regulator remains in existing state)
		1 LDO2 enable request
		Reset condition: POR

16.6 M_REG_CTRL2 register

Table 16. M_REG_CTRL2 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	VBSTSR[1:0]		BOOSTT SDCFG	BUCK1 TSDCFG	BUCK2 TSDCFG	BUCK3 TSDCFG	LDO1 TSDCFG	LDO2 TSDCFG
Read	VBSTSR[1:0]		BOOSTT SDCFG	BUCK1 TSDCFG	BUCK2 TSDCFG	BUCK3 TSDCFG	LDO1 TSDCFG	LDO2 TSDCFG
Reset	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	VPRESRLS[1:0]		0	VPRESRHS[1:0]	
Read	RESERVED	RESERVED	RESERVED	VPRESRLS[1:0]		RESERVED	VPRESRHS[1:0]	
Reset	0	0	0	1	1	0	OTP	OTP

Table 17. M_REG_CTRL2 register bit description

Bit	Symbol	Description
23 to 22	VBSTSR[1:0]	VBOOST low-side slew rate control
		00 50 V/µs - slow
		01 100 V/µs – medium
		10 300 V/µs – fast
		11 500 V/µs – ultra fast
		Reset condition: POR

Table 17. M_REG_CTRL2 register bit description*...continued*

Bit	Symbol	Description
21	BOOSTTSDCFG	BOOST behavior in case of TSD
		0 Regulator shutdown
		1 Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR
20	BUCK1TSDCFG	BUCK1 behavior in case of TSD
		0 Regulator shutdown
		1 Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR
19	BUCK2TSDCFG	BUCK2 behavior in case of TSD
		0 Regulator shutdown
		1 Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR
18	BUCK3TSDCFG	BUCK3 behavior in case of TSD
		0 Regulator shutdown
		1 Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR
17	LDO1TSDCFG	LDO1 behavior in case of TSD
		0 Regulator shutdown
		1 Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR
16	LDO2TSDCFG	LDO2 behavior in case of TSD
		0 Regulator shutdown
		1 Regulator shutdown and state machine transition to DEEP-FS
		Reset condition: POR
12 to 11	VPRESRLS[1:0]	VPRE low-side slew rate control
		00 130 mA typical drive capability - slow
		01 260 mA typical drive capability - medium
		10 520 mA typical drive capability - fast
		11 900 mA typical drive capability - ultra fast
		Reset condition: POR
9 to 8	VPRESRHS[1:0]	VPRE high-side slew rate control
		00 130 mA typical drive capability - slow
		01 260 mA typical drive capability - medium
		10 520 mA typical drive capability - fast
		11 900 mA typical drive capability - ultra fast
		Reset condition: POR

16.7 M_AMUX register

Table 18. M_AMUX register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	RATIO	AMUX[4:0]				
Read	RESERVED	RESERVED	RATIO	AMUX[4:0]				
Reset	0	0	0	0	0	0	0	0

Table 19. M_AMUX register bit description

Bit	Symbol	Description
13	RATIO	Selection of divider ratio for Vsup, Wake1 and Wake 2 inputs
		0 Ratio = 7.5 when Vsup is selected, 7.45 when WAKE1 or WAKE2 are selected
		1 Ratio = 14 when Vsup is selected,13.85 when WAKE1 or WAKE2 are selected
		Reset condition
12 to 8	AMUX[4:0]	See Table 87

16.8 M_CLOCK register

Table 20. M_CLOCK register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	MOD_CONF	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Read	MOD_CONF	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	RESERVED	RESERVED	RESERVED	MOD_EN	CLK_TUNE[3 :0]			
Read	RESERVED	RESERVED	RESERVED	MOD_EN	CLK_TUNE[3 :0]			
Reset	0	0	0	0	0	0	0	0

Table 21. M_CLOCK register bit description

Bit	Symbol	Description
23	MOD_CONF	Modulation configuration of main oscillator
		0 range ± 5 % 23 kHz
		1 range ± 5 % 94 kHz
		Reset condition: POR

Table 21. M_CLOCK register bit description*...continued*

Bit	Symbol	Description
12	MOD_EN	Modulation activation of main oscillator
		0 Modulation disabled
		1 Modulation enabled
		Reset condition: POR
11 to 8	CLK_TUNE[3:0]	See Table 85

16.9 M_INT_MASK1 register

Table 22. M_INT_MASK1 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	VPREOC_M	0	BUCK1 OC_M	BUCK2 OC_M	BUCK3 OC_M	LDO1OC_M	LDO2OC_M
Read	RESERVED	VPREOC_M	RESERVED	BUCK1 OC_M	BUCK2 OC_M	BUCK3 OC_M	LDO1OC_M	LDO2OC_M
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	BOOSTTSD_ M	BUCK1 TSD_M	BUCK2 TSD_M	BUCK3 TSD_M	LDO1TSD_M	LDO2TSD_M
Read	RESERVED	RESERVED	BOOSTTSD_ M	BUCK1 TSD_M	BUCK2 TSD_M	BUCK3 TSD_M	LDO1TSD_M	LDO2TSD_M
Reset	0	0	0	0	0	0	0	0

Table 23. M_INT_MASK1 register bit description

Bit	Symbol	Description
22	VPREOC_M	Inhibit INTERRUPT for VPRE overcurrent
		0 INT not masked
		1 INT masked
		Reset condition: POR
20	BUCK1OC_M	Inhibit INTERRUPT for BUCK1 overcurrent
		0 INT not masked
		1 INT masked
		Reset condition: POR
19	BUCK2OC_M	Inhibit INTERRUPT for BUCK3 overcurrent
		0 INT not masked
		1 INT masked
		Reset condition: POR
18	BUCK3OC_M	Inhibit INTERRUPT for BUCK3 overcurrent
		0 INT not masked
		1 INT masked
		Reset condition: POR

Table 23. M_INT_MASK1 register bit description*...continued*

Bit	Symbol	Description
17	LDO1OC_M	Inhibit INTERRUPT for LDO1 overcurrent
		0 INT not masked
		1 INT masked
		Reset condition: POR
16	LDO2OC_M	Inhibit INTERRUPT for LDO2 overcurrent
		0 INT not masked
		1 INT masked
		Reset condition: POR
13	BOOSTTSD_M	Inhibit INTERRUPT for BOOST overtemperature shutdown event
		0 INT not masked
		1 INT masked
		Reset condition: POR
12	BUCK1TSD_M	Inhibit INTERRUPT for BUCK1 overtemperature shutdown event
		0 INT not masked
		1 INT masked
		Reset condition: POR
11	BUCK2TSD_M	Inhibit INTERRUPT for BUCK2 overtemperature shutdown event
		0 INT not masked
		1 INT masked
		Reset condition: POR
10	BUCK3TSD_M	Inhibit INTERRUPT for BUCK3 overtemperature shutdown event
		0 INT not masked
		1 INT masked
		Reset condition: POR
9	LDO1TSD_M	Inhibit INTERRUPT for LDO1 overtemperature shutdown event
		0 INT not masked
		1 INT masked
		Reset condition: POR
8	LDO2TSD_M	Inhibit INTERRUPT for LDO2 overtemperature shutdown event
		0 INT not masked
		1 INT masked
		Reset condition: POR

16.10 M_INT_MASK2 register

Table 24. M_INT_MASK2 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	0	VBOOSTOV_M	VBOSUVH_M	COM_M	VPRE_FB_OV_M
Read	RESERVED	RESERVED	RESERVED	RESERVED	VBOOSTOV_M	VBOSUVH_M	COM_M	VPRE_FB_OV_M
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	VBOOST_UVH_M	VSUPUV7_M	0	VPREUVH_M	VSUPUVL_M	VSUPUVH_M	WAKE1_M	WAKE2_M
Read	VBOOST_UVH_M	VSUPUV7_M	RESERVED	VPREUVH_M	VSUPUVL_M	VSUPUVH_M	WAKE1_M	WAKE2_M
Reset	0	0	0	0	0	0	0	0

Table 25. M_INT_MASK2 register bit description

Bit	Symbol	Description
19	VBOOSTOV_M	Inhibit INTERRUPT for VBOOST_OV any transition
		0 INT not masked
		1 INT masked
		Reset condition: POR
18	VBOSUVH_M	Inhibit INTERRUPT for VBOS_UVH any transition
		0 INT not masked
		1 INT masked
		Reset condition: POR
17	COM_M	Inhibit INTERRUPT for COM any transition
		0 INT not masked
		1 INT masked
		Reset condition: POR
16	VPRE_FB_OV_M	Inhibit INTERRUPT for VPRE_FB_OV
		0 INT not masked
		1 INT masked
		Reset condition: POR
15	VBOOSTUVH_M	Inhibit INTERRUPT for VBOOST_UVH
		0 INT not masked
		1 INT masked
		Reset condition: POR
14	VSUPUV7_M	Inhibit INTERRUPT for VSUP_UV7
		0 INT not masked
		1 INT masked
		Reset condition: POR
12	VREUVH_M	Inhibit INTERRUPT for VSUP_UVH
		0 INT not masked
		1 INT masked
		Reset condition: POR
11	VSUPUVL_M	Inhibit INTERRUPT for VSUP_UVL
		0 INT not masked
		1 INT masked
		Reset condition: POR

Table 25. M_INT_MASK2 register bit description*...continued*

Bit	Symbol	Description
10	VSUPUVH_M	Inhibit INTERRUPT for VPRE_UVH
		0 INT not masked
		1 INT masked
		Reset condition: POR
9	WAKE1_M	Inhibit INTERRUPT for WAKE1 any transition
		0 INT not masked
		1 INT masked
		Reset condition: POR
8	WAKE2_M	Inhibit INTERRUPT for WAKE2 any transition
		0 INT not masked
		1 INT masked
		Reset condition: POR

16.11 M_FLAG1 register

When device starts, NXP recommends clearing all the flags by writing 1s on all bits.

Table 26. M_FLAG1 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	VBOSUVH	VBO OSTUVH	VPREOC	BUCK1OC	BUCK2OC	BUCK3OC	LDO1OC	LDO2OC
Read	VBOSUVH	VBO OSTUVH	VPREOC	BUCK1OC	BUCK2OC	BUCK3OC	LDO1OC	LDO2OC
Reset	1	1	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	VBOOSTOV	VBOOSTOT	BUCK1OT	BUCK2OT	BUCK3OT	LDO1OT	LDO2OT
Read	RESERVED	VBOOSTOV	VBOOSTOT	BUCK1OT	BUCK2OT	BUCK3OT	LDO1OT	LDO2OT
Reset	0	0	0	0	0	0	0	0

Table 27. M_FLAG1 register bit description

Bit	Symbol	Description
23	VBOSUVH	VBOS undervoltage high event (falling)
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
22	VBOOSTUVH	VBOOST undervoltage high event (falling)
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)

Table 27. M_FLAG1 register bit description*...continued*

Bit	Symbol	Description
21	VPREOC	VPRE overcurrent event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
20	BUCK1OC	BUCK1 overcurrent event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
19	BUCK2OC	BUCK3 overcurrent event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
18	BUCK3OC	BUCK3 overcurrent
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
17	LDO1OC	LDO2 overcurrent
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
16	LDO2OC	LDO1 overcurrent
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
14	VBOOSTOV	VBOOST overvoltage protection event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
13	VBOOSTOT	VBOOST overtemperature shutdown event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
12	BUCK1OT	BUCK1 overtemperature shutdown event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
11	BUCK2OT	BUCK2 overtemperature shutdown event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)

Table 27. M_FLAG1 register bit description*...continued*

Bit	Symbol	Description
10	BUCK3OT	BUCK3 overtemperature shutdown event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write '1')
9	LDO1OT	LDO1 overtemperature shutdown event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write '1')
8	LDO2OT	LDO2 overtemperature shutdown event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write '1')

16.12 M_FLAG2 register

When the device starts, NXP recommends clearing all the flags by writing 1s on all bits.

Table 28. M_FLAG2 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	VPRE_ FB_OV	VSUPUV7	0	0	0	0	0	0
Read	VPRE_ FB_OV	VSUPUV7	BOOST_ST	BUCK1_ST	BUCK2_ST	BUCK3_ST	LDO1_ST	LDO2_ST
Reset	0	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
Write	VPREUVL	VPREUVH	VSUPUVL	VSUPUVH	0	0	WK2FLG	WK1FLG
Read	VPREUVL	VPREUVH	VSUPUVL	VSUPUVH	WK2RT	WK1RT	WK2FLG	WK1FLG
Reset	1	1	1	1	0	1	0	1

Note: *Reset value for FS6600, wake-up by Wake1, all regulators started by default during power-up sequence.*

Table 29. M_FLAG2 register bit description

Bit	Symbol	Description
23	VPRE_FB_OV	VPRE_FB_OV event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write '1')
22	VSUPUV7	VSUP_UV7 event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write '1')

Table 29. M_FLAG2 register bit description*...continued*

Bit	Symbol	Description
21	BOOST_ST	BOOST state
		0 Regulator OFF
		1 Regulator ON
		Reset condition: Real-time information
20	BUCK1_ST	BUCK1 state
		0 Regulator OFF
		1 Regulator ON
		Reset condition: Real-time information
19	BUCK2_ST	BUCK2 state
		0 Regulator OFF
		1 Regulator ON
		Reset condition: Real-time information
18	BUCK3_ST	BUCK3 state
		0 Regulator OFF
		1 Regulator ON
		Reset condition: Real-time information
17	LDO1_ST	LDO1 state
		0 regulator OFF
		1 regulator ON
		Reset condition: Real-time information
16	LDO2_ST	LDO2 state
		0 regulator OFF
		1 regulator ON
		Reset condition: Real-time information
15	VPREUVL	VPRE_UVL event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
14	VPREUVH	VPRE_UVH event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
13	VSUPUVL	VSUP_UVL event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)
12	VSUPUVH	VSUP_UVH event
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write ‘1’)

Table 29. M_FLAG2 register bit description*...continued*

Bit	Symbol	Description
11	WK2RT	Report event: WAKE2 real-time state
		0 WAKE2 is low level
		1 WAKE2 is high
		Reset condition: Real-time information
10	WK1RT	Report event: WAKE1 real-time state
		0 WAKE1 is low level
		1 WAKE1 is high
		Reset condition: Real-time information
9	WK2FLG	WAKE2 wake-up source flag
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write '1')
8	WK1FLG	WAKE1 wake-up source flag
		0 No event
		1 Event occurred
		Reset condition: POR / Clear on Write (write '1')

16.13 M_VMON_REGx register

Table 30. M_VMON_REGx register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	0	VMON4_REG[2:0]			VMON3_ REG[2]
Read	RESERVED	RESERVED	RESERVED	RESERVED	VMON4_REG[2:0]			VMON3_ REG[2]
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	VMON3_REG[1:0]		VMON2_REG[1:0]			VMON1_REG[1:0]		
Read	VMON3_REG[1:0]		VMON2_REG[1:0]			VMON1_REG[1:0]		
Reset	0	0	0	0	0	0	0	0

Table 31. M_VMON_REGx register bit description

Bit	Symbol	Description
19 to 17	VMON4_REG[2:0]	Regulator assignment to VMON4
		000 External regulator
		001 VPRE
		010 LDO1
		011 LDO2
		100 BUCK2
		101 BUCK3
		11x External regulator
		Reset condition: POR
16 to 14	VMON3_REG[2:0]	Regulator assignment to VMON3
		000 External regulator
		001 VPRE
		010 LDO1
		011 LDO2
		100 BUCK2
		101 BUCK3
		11x External regulator
		Reset condition: POR
13 to 11	VMON2_REG[2:0]	Regulator assignment to VMON2
		000 External regulator
		001 VPRE
		010 LDO1
		011 LDO2
		100 BUCK2
		101 BUCK3
		11x External regulator
		Reset condition: POR
10 to 8	VMON1_REG[2:0]	Regulator assignment to VMON1
		000 External regulator
		001 VPRE
		010 LDO1
		011 LDO2
		100 BUCK2
		101 BUCK3
		11x External regulator
		Reset condition: POR

16.14 M_LVB1_SVS register

Table 32. M_LVB1_SVS register bit allocation

Bit	23	22	21	20	19	18	17	16
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Read	RESERVED	RESERVED	RESERVED	LVB1_SVS[4:0]				
Reset	0	0	0	0	0	0	0	0

Table 33. M_LVB1_SVS register bit description

Bit	Symbol	Description
12 to 8	LVB1_SVS[4:0]	Static voltage scaling negative offset
		00000 0 mV
		00001 −6.25 mV
		00010 −12.50 mV
		00011 −18.75 mV
		00100 −25 mV
		00101 −31.25 mV
		00110 −37.5 mV
		00111 −43.75 mV
		01000 −50 mV
		01001 −56.25 mV
		01010 −62.5 mV
		01011 −68.75 mV
		01100 −75 mV
		01101 −81.25 mV
		01110 −87.5 mV
		01111 −93.75 mV
		10000 −100 mV
		Reset condition: POR

16.15 M_MEMORY0 register

Table 34. M_MEMORY0 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	MEMORY0[15:8]							
Read	MEMORY0[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	MEMORY0[7:0]							
Read	MEMORY0[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 35. M_MEMORY0 register bit description

Bit	Symbol	Description
23 to 8	MEMORY0[15:0]	Free memory field for data storage
		0... 16 bits free memory
		...1
		Reset condition: POR

16.16 M_MEMORY1 register

Table 36. M_MEMORY1 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	MEMORY1[15:0]							
Read	MEMORY1[15:0]							
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	MEMORY1[15:0]							
Read	MEMORY1[15:0]							
Reset	0	0	0	0	0	0	0	0

Table 37. M_MEMORY1 register bit description

Bit	Symbol	Description
23 to 8	MEMORY1[15:0]	Free memory field for data storage
		0… 16 bits free memory
		…1
		Reset condition: POR

16.17 M_DEVICEID register

Table 38. M_DEVICEID register bit allocation

Bit	23	22	21	20	19	18	17	16
Read	FMREV[3:0]				MMREV[3:0]			
Reset	0	0	1	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Read	DEVICEID[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 39. M_DEVICEID register bit description

Bit	Symbol	Description
23 to 20	FMREV[3:0]	Full mask revision
		Full mask revision configured by metal connection
		Reset condition: POR
19 to 16	MMREV[3:0]	Metal Mask Revision
		Metal mask revision configured by metal connection
		Reset condition: POR
15 to 8	DEVICEID[7:0]	Device ID
		x…x Device ID from OTP_DEVICEID[7:0] bits
		Reset condition: POR

17 Fail-safe register mapping

17.1 Fail-safe writing registers overview

Table 40. Fail-safe writing registers overview

Logic	Register name	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
Fail-safe	FS_I_OVUV_SAFE_REACTION1	VCOREMON_OV_FS_IMPACT[1:0]		VCOREMON_UV_FS_IMPACT[1:0]		0	VCOREMON_ABIST2	VDDIO_ABIST2	VMON1_ABIST2
		VMON2_ABIST2	VMON3_ABIST2	VMON4_ABIST2	0	VDDIO_OV_FS_IMPACT[1:0]		VDDIO_UV_FS_IMPACT[1:0]	
	FS_I_OVUV_SAFE_REACTION2	VMON4_OV_FS_IMPACT[1:0]		VMON4_UV_FS_IMPACT[1:0]		VMON3_OV_FS_IMPACT[1:0]		VMON3_UV_FS_IMPACT[1:0]	
		VMON2_OV_FS_IMPACT[1:0]		VMON2_UV_FS_IMPACT[1:0]		VMON1_OV_FS_IMPACT[1:0]		VMON1_UV_FS_IMPACT[1:0]	
	FS_I_WD_CFG	WD_ERR_LIMIT[1:0]		0	WD_RFR_LIMIT[1:0]		0	WD_FS_IMPACT[1:0]	
		0	0	0	0	0	0	0	0
	FS_I_SAFE_INPUTS	FCCU_CFG[1:0]		0	FCCU12_FLT_POL	FCCU1_FLT_POL	FCCU2_FLT_POL	0	FCCU12_FS_IMPACT
		FCCU1_FS_IMPACT	FCCU2_FS_IMPACT	0	ERRMON_FLT_POL	ERRMON_ACK_TIME[1:0]		ERRMON_FS_IMPACT	0
	FS_I_FSSM	FLT_ERR_CNT_LIMIT[1:0]		0	FLT_ERR_IMPACT[1:0]		0	RSTB_DUR	0
		FS0B_SC_HIGH_CFG	0	CLK_MON_DIS	DIS_8s	0	0	0	0
	FS_I_SVS	SVS_OFFSET[4:0]					0	0	0
		0	0	0	0	0	0	0	0
	FS_WD_WINDOW	WDW_PERIOD [3:0]				0	WDW_DC[2:0]		
		0	0	0	0	WDW_RECOVERY[3:0]			
	FS_WD_SEED	WD_SEED[15:8]							
		WD_ SEED[7:0]							
	FS_WD_ANSWER	WD_ANSWER[15:8]							
		WD_ANSWER[7:0]							
	FS_OVUVREG_STATUS	VCOREMON_OV	VCOREMON_UV	VDDIO_OV	VDDIO_UV	VMON4_OV	VMON4_UV	VMON3_OV	VMON3_UV
		VMON2_OV	VMON2_UV	VMON1_OV	VMON1_UV	0	FS_DIG_REF_OV	FS_OSC_DRIFT	0
	FS_RELEASE_FS0B	RELEASE_FS0B[15:8]							
		RELEASE_FS0B[7:0]							
	FS_SAFE_IOS	PGOOD_DIAG	PGOOD_EVENT	0	EXT_RSTB	0	0	RSTB_EVENT	RSTB_DIAG
		RSTB_REQ	0	0	FS0B_DIAG	FS0B_REQ	GOTO_INITFS	0	0
	FS_DIAG_SAFETY	FCCU12	FCCU1	FCCU2	ERRMON_ACK	ERRMON	0	BAD_WD_DATA	BAD_WD_TIMING
		0	0	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_CRC	0	0	0
	FS_INTB_MASK	0	0	0	0	0	0	INT_INH_VMON4_OV_UV	INT_INH_VMON3_OV_UV
		INT_INH_VMON2_OV_UV	INT_INH_VMON1_OV_UV	INT_INH_VDDIO_OV_UV	INT_INH_VCOREMON_OV_UV	INT_INH_BAD_WD_REFRESH	INT_INH_ERRMON	INT_INH_FCCU2	INT_INH_FCCU1
	FS_STATES	0	DBG_EXIT	0	0	OTP_CORRUPT	0	REG_CORRUPT	0
		0	0	0	0	0	0	0	0

17.2 Fail-safe reading registers overview

Table 41. Fail-safe reading registers overview

Logic	Register name	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
Fail-safe	FS_GRL_FLAGS	FS_COM_G	FS_WD_G	FS_IO_G	FS_REG_OVUV_G	RESERVED	RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	FS_I_OVUV_SAFE_REACTION1	VCOREMON_OV_FS_IMPACT[1:0]		VCOREMON_UV_FS_IMPACT[1:0]		RESERVED	VCOREMON_ABIST2	VDDIO_ABIST2	VMON1_ABIST2
		VMON2_ABIST2	VMON3_ABIST2	VMON4_ABIST2	RESERVED	VDDIO_OV_FS_IMPACT[1:0]		VDDIO_UV_FS_IMPACT[1:0]	
	FS_I_OVUV_SAFE_REACTION2	VMON4_OV_FS_IMPACT[1:0]		VMON4_UV_FS_IMPACT[1:0]		VMON3_OV_FS_IMPACT[1:0]		VMON3_UV_FS_IMPACT[1:0]	
		VMON2_OV_FS_IMPACT[1:0]		VMON2_UV_FS_IMPACT[1:0]		VMON1_OV_FS_IMPACT[1:0]		VMON1_UV_FS_IMPACT[1:0]	
	FS_I_WD_CFG	WD_ERR_LIMIT[1:0]		RESERVED	WD_RFR_LIMIT[1:0]		RESERVED	WD_FS_IMPACT[1:0]	
		RESERVED	WD_RFR_CNT[2:0]			WD_ERR_CNT[3:0]			
	FS_I_SAFE_INPUTS	FCCU_CFG[1:0]		RESERVED	FCCU12_FLT_POL	FCCU1_FLT_POL	FCCU2_FLT_POL	RESERVED	FCCU12_FS_IMPACT
		FCCU1_FS_IMPACT	FCCU2_FS_IMPACT	RESERVED	ERRMON_FLT_POL	ERRMON_ACK_TIME[1:0]		ERRMON_FS_IMPACT	RESERVED
	FS_I_FSSM	FLT_ERR_CNT_LIMIT[1:0]		RESERVED	FLT_ERR_IMPACT[1:0]		RESERVED	RSTB_DUR	RESERVED
		FS0B_SC_HIGH_CFG	RESERVED	CLK_MON_DIS	DIS_8s	FLT_ERR_CNT[3:0]			
	FS_I_SVS	SVS_OFFSET[4:0]					RESERVED	RESERVED	RESERVED
		RESERVED	RESERVED	reserved	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	FS_WD_WINDOW	WDW_PERIOD[3:0]				RESERVED	WDW_DC[2:0]		
		RESERVED	RESERVED	RESERVED	RESERVED	WDW_RECOVERY[3:0]			
	FS_WD_SEED	WD_ SEED[15:8]							
		WD_ SEED[7:0]							
	FS_WD_ANSWER	WD_ANSWER[15:8]							
		WD_ANSWER[7:0]							
	FS_OVUVREG_STATUS	VCOREMON_OV	VCOREMON_UV	VDDIO_OV	VDDIO_UV	VMON4_OV	VMON4_UV	VMON3_OV	VMON3_UV
		VMON2_OV	VMON2_UV	VMON1_OV	VMON1_UV	RESERVED	FS_DIG_REF_OV	FS_OSC_DRIFT	RESERVED
	FS_RELEASE_FS0B	RELEASE_FS0B[15:8]							
		RELEASE_FS0B[7:0]							
	FS_SAFE_IOS	PGOOD_DIAG	PGOOD_EVENT	PGOOD_SNS	EXT_RSTB	RSTB_DRV	RSTB_SNS	RSTB_EVENT	RSTB_DIAG
		RESERVED	FS0B_DRV	FS0B_SNS	FS0B_DIAG	RESERVED	RESERVED	FCCU2_RT	FCCU1_RT
	FS_DIAG_SAFETY	FCCU12	FCCU1	FCCU2	RESERVED	ERRMON	ERRMON_STATUS	BAD_WD_DATA	BAD_WD_TIMING
		ABIST1_OK	ABIST2_OK	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_CRC	0	0	LBIST_OK
	FS_INTB_MASK	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	INT_INH_VMON4_OV_UV	INT_INH_VMON4_OV_UV
		INT_INH_VMON2_OV_UV	INT_INH_VMON1_OV_UV	INT_INH_VDDIO_OV_UV	INT_INH_VCOREMON_OV_UV	INT_INH_BAD_WD_REFRESH	INT_INH_ERRMON	INT_INH_FCCU2	INT_INH_FCCU1
	FS_STATES	RESERVED	RESERVED	DBG_MODE	RESERVED	OTP_CORRUPT	RESERVED	REG_CORRUPT	RESERVED
		RESERVED	RESERVED	RESERVED	FSM_STATE[4:0]				

17.3 FS_GRL_FLAGS register

Table 42. FS_GRL_FLAGS register bit allocation

Bit	23	22	21	20	19	18	17	16
Read	FS_COM_G	FS_WD_G	FS_IO_G	FS_REG_OVUV_G	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Table 43. FS_GRL_FLAGS register bit description

Bit	Symbol	Description
23	FS_COM_G	Report an issue in the communication (SPI) **FS_COM_G** = SPI_FS_CLK or SPI_FS_REQ or SPI_FS_CRC
		0 No failure
		1 Failure
		Reset condition: Real-time information - cleared when all individual bits are cleared
22	FS_WD_G	Report an issue on the watchdog refresh **FS_WD_G** = BAD_WD_DATA or BAD_WD_TIMING
		0 Good WD refresh
		1 Bad WD refresh
		Reset condition: Real-time information - cleared when all individual bits are cleared
21	FS_IO_G	Report an issue in one of the fail-safe IOs **FS_IO_G** = PGOOD_DIAG or RSTB_DIAG or FS0B_DIAG
		0 No failure
		1 Failure
		Reset condition: Real-time information - cleared when all individual bits are cleared
20	FS_REG_OVUV_G	Report an issue in one of the voltage monitoring (OV or UV) **FS_REG_OVUV_G** = VCOREMON_OV or VCOREMON_UV or VDDIO_OV or VDDIO_UV or VMON4_OV or VMON4_UV or VMON3_OV or VMON3_UV or VMON2_OV or VMON2_UV or VMON1_OV or VMON1_UV
		0 No failure
		1 Failure
		Reset condition: Real-time information - cleared when all individual bits are cleared

17.4 FS_I_OVUV_SAFE_REACTION1 register

Table 44. FS_I_OVUV_SAFE_REACTION1 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	VCOREMON_OV_FS_IMPACT[1:0]		VCOREMON_UV_FS_IMPACT[1:0]		0	VCOREMON_ABIST2	VDDIO_ABIST2	VMON1_ABIST2
Read	VCOREMON_OV_FS_IMPACT[1:0]		VCOREMON_UV_FS_IMPACT[1:0]		RESERVED	VCOREMON_ABIST2	VDDIO_ABIST2	VMON1_ABIST2
Reset	1	1	0	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	VMON2_ ABIST2	VMON3_ ABIST2	VMON4_ ABIST2	0	VDDIO_OV_ FS_IMPACT[1:0]		VDDIO_UV_ FS_IMPACT[1:0]	
Read	VMON2_ ABIST2	VMON3_ ABIST2	VMON4_ ABIST2	RESERVED	VDDIO_OV_ FS_IMPACT[1:0]		VDDIO_UV_ FS_IMPACT[1:0]	
Reset	0	0	0	0	1	1	0	1

Table 45. FS_I_OVUV_SAFE_REACTION1 register bit description

Bit	Symbol	Description
23 to 22	VCOREMON_OV_FS_IMPACT[1:0]	Table 110
21 to 20	VCOREMON_UV_FS_IMPACT[1:0]	Table 110
18	VCOREMON_ABIST2	VCOREMON ABIST2 configuration
		0 No ABIST
		1 VCOREMON BIST executed during ABIST2
		Reset condition: POR
17	VDDIO_ABIST2	VDDIO ABIST2 configuration
		0 No ABIST
		1 VDDIO BIST executed during ABIST2
		Reset condition: POR
16	VMON1_ABIST2	VMON1 ABIST2 configuration
		0 No ABIST
		1 VMON1 BIST executed during ABIST2
		Reset condition: POR
15	VMON2_ABIST2	VMON2 ABIST2 configuration
		0 No ABIST
		1 VMON2 BIST executed during ABIST2
		Reset condition: POR
14	VMON3_ABIST2	VMON3 ABIST2 configuration
		0 No ABIST
		1 VMON3 BIST executed during ABIST2
		Reset condition: POR
13	VMON4_ABIST2	VMON4 ABIST2 configuration
		0 No ABIST
		1 VMON4 BIST executed during ABIST2
		Reset condition: POR
11 to 10	VDDIO_OV_FS_IMPACT[1:0]	Table 113
9 to 8	VDDIO_UV_FS_IMPACT[1:0]	Table 113

17.5 FS_I_OVUV_SAFE_REACTION2 register

Table 46. FS_I_OVUV_SAFE_REACTION2 register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	VMON4_OV_FS_IMPACT[1:0]		VMON4_UV_FS_IMPACT[1:0]		VMON3_OV_FS_IMPACT[1:0]		VMON3_UV_FS_IMPACT[1:0]	
Read	VMON4_OV_FS_IMPACT[1:0]		VMON4_UV_FS_IMPACT[1:0]		VMON3_OV_FS_IMPACT[1:0]		VMON3_UV_FS_IMPACT[1:0]	
Reset	1	1	0	1	1	1	0	1

Bit	15	14	13	12	11	10	9	8
Write	VMON2_OV_FS_IMPACT[1:0]		VMON2_UV_FS_IMPACT[1:0]		VMON1_OV_FS_IMPACT[1:0]		VMON1_UV_FS_IMPACT[1:0]	
Read	VMON2_OV_FS_IMPACT[1:0]		VMON2_UV_FS_IMPACT[1:0]		VMON1_OV_FS_IMPACT[1:0]		VMON1_UV_FS_IMPACT[1:0]	
Reset	1	1	0	1	1	1	0	1

Table 47. FS_I_OVUV_SAFE_REACTION2 register bit description

Bit	Symbol	Description
23 to 22	VMON4_OV_FS_IMPACT[1:0]	See Table 115
21 to 20	VMON4_UV_FS_IMPACT[1:0]	
19 to 18	VMON3_OV_FS_IMPACT[1:0]	
17 to 16	VMON3_UV_FS_IMPACT[1:0]	
15 to 14	VMON2_OV_FS_IMPACT[1:0]	
13 to 12	VMON2_UV_FS_IMPACT[1:0]	
11 to 10	VMON1_OV_FS_IMPACT[1:0]	
9 to 8	VMON1_UV_FS_IMPACT[1:0]	

17.6 FS_I_WD_CFG register

Table 48. FS_I_WD_CFG register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	WD_ERR_LIMIT[1:0]		0	WD_RFR_LIMIT[1:0]		0	WD_FS_IMPACT[1:0]	
Read	WD_ERR_LIMIT[1:0]		RESERVED	WD_RFR_LIMIT[1:0]		RESERVED	WD_FS_IMPACT[1:0]	
Reset	0	1	0	0	0	0	1	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	WD_RFR_CNT[2:0]			WD_ERR_CNT[3:0]			
Reset	0	0	0	0	0	0	0	0

Table 49. FS_I_WD_CFG register bit description

Bit	Symbol	Description
23 to 22	WD_ERR_LIMIT[1:0]	See Table 100
20 to 19	WD_RFR_LIMIT[1:0]	See Table 101
17 to 16	WD_FS_IMPACT[1:0]	See Table 102
14 to 12	WD_RFR_CNT[2:0]	Reflect the value of the watchdog refresh counter
		000 0
		001 1
		010 2
		011 3
		100 4
		101 5
		110 6
		111 7
		Reset condition: POR
11 to 8	WD_ERR_CNT[3:0]	Reflect the value of the watchdog error counter
		0000 0
		0001 1
		0010 2
		0011 3
		0100 4
		0101 5
		0110 6
		0111 7
		1000 8
		Reset condition: POR

17.7 FS_I_SAFE_INPUTS register

Table 50. FS_I_SAFE_INPUTS register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	FCCU_CFG[1:0]		0	FCCU12_FLT_POL	FCCU1_FLT_POL	FCCU2_FLT_POL	0	FCCU12_FS_IMPACT
Read	FCCU_CFG[1:0]		RESERVED	FCCU12_FLT_POL	FCCU1_FLT_POL	FCCU2_FLT_POL	RESERVED	FCCU12_FS_IMPACT
Reset	0	1	0	0	0	0	0	1

Bit	15	14	13	12	11	10	9	8
Write	FCCU1_FS_IMPACT	FCCU2_FS_IMPACT	0	ERRMON_FLT_POL	ERRMON_ACK_TIME[1:0]		ERRMON_FS_IMPACT	0
Read	FCCU1_FS_IMPACT	FCCU2_FS_IMPACT	RESERVED	ERRMON_FLT_POL	ERRMON_ACK_TIME[1:0]		ERRMON_FS_IMPACT	RESERVED
Reset	1	1	0	0	0	1	1	0

Table 51. FS_I_SAFE_INPUTS register bit description

Bit	Symbol	Description
23 to 22	FCCU_CFG[1:0]	See Table 104
20	FCCU12_FLT_POL	See Table 105
19	FCCU1_FLT_POL	See Table 107
18	FCCU2_FLT_POL	See Table 107
16	FCCU12_FS_IMPACT	See Table 106
15	FCCU1_FS_IMPACT	See Table 108
14	FCCU2_FS_IMPACT	See Table 108
12	ERRMON_FLT_POL	See Table 117
11 to 10	ERRMON_ACK_TIME[1:0]	See Table 118
9	ERRMON_FS_IMPACT	See Table 119

17.8 FS_I_FSSM register

Table 52. FS_I_FSSM register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	FLT_ERR_CNT_LIMIT[1:0]		0	FLT_ERR_IMPACT[1:0]		0	RSTB_DUR	0
Read	FLT_ERR_CNT_LIMIT[1:0]		RESERVED	FLT_ERR_IMPACT[1:0]		RESERVED	RSTB_DUR	RESERVED
Reset	0	1	0	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	FS0B_SC_HIGH_CFG	0	CLK_MON_DIS	DIS_8s	0	0	0	0
Read	FS0B_SC_HIGH_CFG	RESERVED	CLK_MON_DIS	DIS_8s	FLT_ERR_CNT[3:0]			
Reset	1	0	0	0	0	0	0	1

Table 53. FS_I_FSSM register bit description

Bit	Symbol	Description
23 to 22	FLT_ERR_CNT_LIMIT[1:0]	See Table 121
20 to 19	FLT_ERR_IMPACT[1:0]	See Table 122
17	RSTB_DUR	RSTB pulse duration configuration
		0 10 ms
		1 1.0 ms
		Reset condition: POR
15	FS0B_SC_HIGH_CFG	Assert RSTB in case of a short to high detected on FS0B
		0 RSTB is not asserted
		1 RSTB is asserted
		Reset condition: POR

Table 53. FS_I_FSSM register bit description*...continued*

Bit	Symbol	Description
13	CLK_MON_DIS	Disable clock monitoring
		0 Clock monitoring enabled
		1 Clock monitoring disabled
		Reset condition: POR
12	DIS_8s	Disable 8 s timer
		0 RSTB low 8 s counter enabled
		1 RSTB low 8 s counter disabled
		Reset condition: POR
11 to 8	FLT_ERR_CNT[3:0]	Reflect the value of the fault error counter
		0000 0
		0001 1
		0010 2
		0011 3
		0100 4
		0101 5
		0110 6
		0111 7
		1000 8
		1001 9
		1010 10
		1011 11
		1100 12
		Reset condition: Real-time information

17.9 FS_I_SVS register

Table 54. FS_I_SVS register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	SVS_OFFSET[4:0]					0	0	0
Read	SVS_OFFSET[4:0]					RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Table 55. FS_I_SVS register bit description

Bit	Symbol	Description
23 to 19	SVS_OFFSET[4:0]	Static voltage scaling negative offset
		0 0000 0 mV
		0 0001 −6.25 mV
		0 0010 −12.50 mV
		0 0011 −18.75 mV
		0 0100 −25 mV
		0 0101 −31.25 mV
		0 0110 −37.5 mV
		0 0111 −43.75 mV
		0 1000 −50 mV
		0 1001 −56.25 mV
		0 1010 −62.5 mV
		0 1011 −68.75 mV
		0 1100 −75 mV
		0 1101 −81.25 mV
		0 1110 −87.5 mV
		0 1111 −93.75 mV
		1 0000 −100 mV
		Reset condition: POR

17.10 FS_WD_WINDOW register

Table 56. FS_WD_WINDOW register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	WDW_PERIOD [3:0]				0	WDW_DC[2:0]		
Read	WDW_PERIOD[3:0]				RESERVED	WDW_DC[2:0]		
Reset	0	0	1	1	0	0	1	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	WDW_RECOVERY[3:0]			
Read	RESERVED	RESERVED	RESERVED	RESERVED	WDW_RECOVERY[3:0]			
Reset	0	0	0	0	1	0	1	1

Table 57. FS_WD_WINDOW register bit description

Bit	Symbol	Description
23 to 20	WDW_PERIOD[3:0]	See Table 98
18 to 16	WDW_DC[2:0]	See Table 99
11 to 8	WDW_RECOVERY[3:0]	See Table 103

17.11 FS_WD_SEED register

Table 58. FS_WD_SEED register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	WD_SEED[15:8]							
Read	WD_ SEED[15:8]							
Reset	0	1	0	1	1	0	1	0

Bit	15	14	13	12	11	10	9	8
Write	WD_ SEED[7:0]							
Read	WD_ SEED[7:0]							
Reset	1	0	1	1	0	0	1	0

Table 59. FS_WD_SEED register bit description

Bit	Symbol	Description
23 to 8	WD_SEED [15:0]	Watchdog LFSR value
		0… 0x5AB2 default value at startup …1
		Reset condition: POR

17.12 FS_WD_ANSWER register

Table 60. FS_WD_ANSWER register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	WD_ANSWER[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	WD_ANSWER[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 61. FS_WD_ANSWER register bit description

Bit	Symbol	Description
23 to 8	WD_ANSWER[15:0]	Watchdog answer value from the MCU
		0… Challenger WD answer = (NOT(((LFSR x 4)+6)–4))/4 (see Section 31.3.1 "Challenger watchdog") …1 Simple WD answer = 0x5AB2 (see Section 31.3.2 "Simple watchdog")
		Reset condition: POR

17.13 FS_OVUVREG_STATUS register

Table 62. FS_OVUVREG_STATUS register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	VCOREMON_OV	VCOREMON_UV	VDDIO_OV	VDDIO_UV	VMON4_OV	VMON4_UV	VMON3_OV	VMON3_UV
Read	VCOREMON_OV	VCOREMON_UV	VDDIO_OV	VDDIO_UV	VMON4_OV	VMON4_UV	VMON3_OV	VMON3_UV
Reset	0	1	0	1	0	1	0	1

Bit	15	14	13	12	11	10	9	8
Write	VMON2_OV	VMON2_UV	VMON1_OV	VMON1_UV	0	FS_DIG_REF_OV	FS_OSC_DRIFT	0
Read	VMON2_OV	VMON2_UV	VMON1_OV	VMON1_UV	RESERVED	FS_DIG_REF_OV	FS_OSC_DRIFT	RESERVED
Reset	0	1	0	1	0	0	0	0

Table 63. FS_OVUVREG_STATUS register bit description

Bit	Symbol	Description
23	VCOREMON_OV	Overvoltage monitoring on VCOREMON
		0 No overvoltage
		1 Overvoltage reported on VCOREMON
		Reset condition: POR / clear on write (write ‘1’)
22	VCOREMON_UV	Undervoltage monitoring on VCOREMON
		0 No undervoltage
		1 Undervoltage reported on VCOREMON
		Reset condition: POR / clear on write (write ‘1’)
21	VDDIO_OV	Overvoltage monitoring on VDDIO
		0 No overvoltage
		1 Overvoltage reported on VDDIO
		Reset condition POR / clear on write (write ‘1’)
20	VDDIO_UV	Undervoltage monitoring on VDDIO
		0 No undervoltage
		1 Undervoltage reported on VDDIO
		Reset condition: POR / clear on write (write ‘1’)
19	VMON4_OV	Overvoltage monitoring on VMON4
		0 No overvoltage
		1 Overvoltage reported on VMON4
		Reset condition: POR / clear on write (write ‘1’)
18	VMON4_UV	Undervoltage monitoring on VMON4
		0 No undervoltage
		1 Undervoltage reported on VMON4
		Reset condition: POR / clear on write (write ‘1’)

Table 63. FS_OVUVREG_STATUS register bit description*...continued*

Bit	Symbol	Description
17	VMON3_OV	Overvoltage monitoring on VMON3
		0 No overvoltage
		1 Overvoltage reported on VMON3
		Reset condition: POR / clear on write (write '1')
16	VMON3_UV	Undervoltage monitoring on VMON3
		0 No Undervoltage
		1 Undervoltage reported on VMON3
		Reset condition: POR / clear on write (write '1')
15	VMON2_OV	Overvoltage monitoring on VMON2
		0 No overvoltage
		1 Overvoltage reported on VMON2
		Reset condition: POR / clear on write (write '1')
14	VMON2_UV	Undervoltage monitoring on VMON2
		0 No undervoltage
		1 Undervoltage reported on VMON2
		Reset condition: POR / clear on write (write '1')
13	VMON1_OV	Overvoltage monitoring on VMON1
		0 No overvoltage
		1 Overvoltage reported on VMON1
		Reset condition: POR / clear on write (write '1')
12	VMON1_UV	Undervoltage monitoring on VMON1
		0 No undervoltage
		1 Undervoltage reported on VMON1
		Reset condition: POR / clear on write (write '1')
9	FS_DIG_REF_OV	Overvoltage of the internal digital fail-safe reference voltage
		0 No overvoltage
		1 Overvoltage reported of the internal digital fail-safe reference voltage
		Reset condition: POR / clear on write (write '1')
8	FS_OSC_DRIFT	Drift of the fail-safe OSC
		0 No drift
		1 Oscillator drift
		Reset condition: POR / clear on write (write '1')

17.14 FS_RELEASE_FS0B register

Table 64. FS_RELEASE_FS0B register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	RELEASE_FS0B[15:8]							
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	RELEASE_FS0B[7:0]							
Reset	0	0	0	0	0	0	0	0

Table 65. FS_RELEASE_FS0B register bit description

Bit	Symbol	Description
23 to 8	RELEASE_FS0B [15:0]	Secure 16-bits word to release FS0B
		0... Depend on WD_SEED value and calculation. See Section 31.8.4 "FS0B release".
		...1
		Reset condition: POR

17.15 FS_SAFE_IOs register

Table 66. FS_SAFE_IOS register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	PGOOD_ DIAG	PGOOD_ EVENT	0	EXT_RSTB	0	0	RSTB_ EVENT	RSTB_DIAG
Read	PGOOD_ DIAG	PGOOD_ EVENT	PGOOD_ SNS	EXT_RSTB	RSTB_DRV	RSTB_SNS	RSTB_ EVENT	RSTB_DIAG
Reset	0	1	0	0	0	0	1	0

Bit	15	14	13	12	11	10	9	8
Write	RSTB_REQ	0	0	FS0B_DIAG	FS0B_REQ	GOTO_ INITFS	0	0
Read	RESERVED	FS0B_DRV	FS0B_SNS	FS0B_DIAG	RESERVED	RESERVED	FCCU2_RT	FCCU1_RT
Reset	0	0	0	0	0	0	0	0

Table 67. FS_SAFE_IOS register bit description

Bit	Symbol	Description
23	PGOOD_DIAG	Report a PGOOD Short to High
		0 No failure
		1 Short circuit HIGH
		Reset condition: POR / clear on write (write ‘1’)
22	PGOOD_EVENT	Report a Power GOOD event
		0 No Power GOOD
		1 Power GOOD event occurred
		Reset condition: POR / clear on write (write ‘1’)
21	PGOOD_SNS	Sense of PGOOD pad
		0 PGOOD pad sensed low
		1 PGOOD pad sensed high
		Reset condition: Real-time information

Table 67. FS_SAFE_IOS register bit description*...continued*

Bit	Symbol	Description
20	EXT_RSTB	Report an external RESET
		0 No external RESET
		1 External RESET
		Reset condition: POR / clear on write (write '1')
19	RSTB_DRV	RSTB driver – digital command
		0 RSTB driver command sensed low
		1 RSTB driver command sensed high
		Reset condition: Real-time information
18	RSTB_SNS	Sense of RSTB pad
		0 RSTB pad sensed low
		1 RSTB pad sensed high
		Reset condition: Real-time information
17	RSTB_EVENT	Report an RSTB event
		0 No RESET
		1 RESET occurred
		Reset condition: POR / clear on write (write '1')
16	RSTB_DIAG	Report an RSTB short to high
		0 No failure
		1 Short circuit high
		Reset condition: POR / clear on write (write '1')
15	RSTB_REQ	Request assertion of RSTB (Pulse)
		0 No assertion
		1 RSTB assertion (pulse)
		Reset condition: POR
14	FS0B_DRV	FS0B driver – digital command
		0 FS0B driver command sensed low
		1 FS0B driver command sensed high
		Reset condition: Real-time information
13	FS0B_SNS	Sense of FS0B pad
		0 FS0B pad sensed low
		1 FS0B pad sensed high
		Reset condition: Real-time information
12	FS0B_DIAG	Report a failure on FS0B
		0 No failure
		1 Short circuit high
		Reset condition: POR / clear on write (write '1')
11	FS0B_REQ	Request assertion of FS0B
		0 No assertion
		1 FS0B assertion
		Reset condition: POR

Table 67. FS_SAFE_IOS register bit description*...continued*

Bit	Symbol	Description
10	GOTO_INITFS	Go back to INIT fail-safe request
		0 No action
		1 Go back to INIT_FS
		Reset condition: POR
9	FCCU2_RT	Report FCCU2 pin level
		0 LOW level
		1 HIGH level
		Reset condition: Real-time information
8	FCCU1_RT	Report FCCU1 pin level
		0 LOW level
		1 HIGH level
		Reset condition: Real-time information

17.16 FS_DIAG_SAFETY register

Table 68. FS_DIAG_SAFETY register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	FCCU12	FCCU1	FCCU2	ERRMON_ ACK	ERRMON	0	BAD_ WD_DATA	BAD_WD_ TIMING
Read	FCCU12	FCCU1	FCCU2	RESERVED	ERRMON	ERRMON_ STATUS	BAD_ WD_DATA	BAD_WD_ TIMING
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_CRC	0	0	0
Read	ABIST1_OK	ABIST2_OK	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_CRC	0	0	LBIST_OK
Reset	1	0	0	0	0	0	0	1

Table 69. FS_DIAG_SAFETY register bit description

Bit	Symbol	Description
23	FCCU12	Report an error in the FCCU12 input
		0 No error
		1 Error detected
		Reset condition: POR / clear on write (write ‘1’)
22	FCCU1	Report an error in the FCCU1 input
		0 No error
		1 Error detected
		Reset condition: POR / clear on write (write ‘1’)

Table 69. FS_DIAG_SAFETY register bit description*...continued*

Bit	Symbol	Description
21	FCCU2	Report an error in the FCCU2 input
		0 No error
		1 Error detected
		Reset condition: POR / clear on write (write '1')
20	ERRMON_ACK	Acknowledge ERRMON failure detection from MCU
		0 No effect
		1 Acknowledge ERRMON failure detection
		Reset condition: POR
19	ERRMON	Report an error in the ERRMON input
		0 No error
		1 Error detected
		Reset condition: POR / clear on write (write '1')
18	ERRMON_STATUS	Report ERRMON pin level
		0 LOW level
		1 HIGH level
		Reset condition: Real-time information
17	BAD_WD_DATA	WD refresh status - Data
		0 Good WD refresh
		1 Bad WD refresh, error in the DATA
		Reset condition: POR / clear on write (write '1')
16	BAD_WD_TIMING	WD refresh status - Timing
		0 Good WD refresh
		1 Bad WD refresh, wrong window or in timeout
		Reset condition: POR / clear on write (write '1')
15	ABIST1_OK	Diagnostic of Analog BIST1
		0 ABIST1 FAIL
		1 ABIST1 PASS
		Reset condition: Real-time information
14	ABIST2_OK	Diagnostic of Analog BIST2
		0 ABIST2 FAIL or NOT EXECUTED
		1 ABIST2 PASS
		Reset condition: Real-time information
13	SPI_FS_CLK	Fail-safe SPI SCLK error detection
		0 No error
		1 Wrong number of clock cycles (<32 or >32)
		Reset condition: POR / clear on write (write '1')
12	SPI_FS_REQ	Invalid fail-safe SPI access (wrong write or read, write to INIT registers in Normal mode, wrong address)
		0 No error
		1 SPI violation
		Reset condition: POR / clear on write (write '1')

Table 69. FS_DIAG_SAFETY register bit description*...continued*

Bit	Symbol	Description
11	SPI_FS_CRC	Fail-safe SPI communication CRC issue
		0 No error
		1 Error detected in the CRC
		Reset condition: POR / clear on write (write '1')
8	LBIST_OK	Diagnostic of Logical BIST
		0 LBIST FAIL
		1 LBIST PASS
		Reset condition: Real-time information

17.17 FS_INTB_MASK register

Table 70. FS_INTB_MASK register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	0	0	0	0	0	INT_INH_VMON4_OV_UV	INT_INH_VMON3_OV_UV
Read	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	INT_INH_VMON4_OV_UV	INT_INH_VMON4_OV_UV
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	INT_INH_VMON2_OV_UV	INT_INH_VMON1_OV_UV	INT_INH_VDDIO_OV_UV	INT_INH_VCOREMON_OV_UV	INT_INH_BAD_WD_REFRESH	INT_INH_ERRMON	INT_INH_FCCU2	INT_INH_FCCU1
Read	INT_INH_VMON2_OV_UV	INT_INH_VMON1_OV_UV	INT_INH_VDDIO_OV_UV	INT_INH_VCOREMON_OV_UV	INT_INH_BAD_WD_REFRESH	INT_INH_ERRMON	INT_INH_FCCU2	INT_INH_FCCU1
Reset	0	0	0	0	0	0	0	0

Table 71. FS_INTB_MASK register bit description

Bit	Symbol	Description
17	INT_INH_VMON4_OV_UV	Inhibit INTERRUPT on VMON4 OV and UV event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR
16	INT_INH_VMON3_OV_UV	Inhibit INTERRUPT on VMON3 OV and UV event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR

Table 71. FS_INTB_MASK register bit description...*continued*

Bit	Symbol	Description
15	INT_INH_VMON2_OV_UV	Inhibit INTERRUPT on VMON2 OV and UV event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR
14	INT_INH_VMON1_OV_UV	Inhibit INTERRUPT on VMON1 OV and UV event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR
13	INT_INH_VDDIO_OV_UV	Inhibit INTERRUPT on VDDIO OV and UV event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR
12	INT_INH_VCOREMON_OV_UV	Inhibit INTERRUPT on VCOREMON OV and UV event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR
11	INT_INH_BAD_WD_REFRESH	Inhibit INTERRUPT on bad WD refresh event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR
10	INT_INH_ERRMON	Inhibit INTERRUPT on ERRMON event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR
9	INT_INH_FCCU2	Inhibit INTERRUPT on FCCU2 event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR
8	INT_INH_FCCU1	Inhibit INTERRUPT on FCCU1 event
		0 Interruption NOT MASKED
		1 Interruption MASKED
		Reset condition: POR

17.18 FS_STATES register

Table 72. FS_STATES register bit allocation

Bit	23	22	21	20	19	18	17	16
Write	0	DBG_EXIT	0	0	OTP_ CORRUPT	0	REG_ CORRUPT	0
Read	RESERVED	RESERVED	DBG_MODE	RESERVED	OTP_ CORRUPT	RESERVED	REG_ CORRUPT	RESERVED
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Write	0	0	0	0	0	0	0	0
Read	RESERVED	RESERVED	RESERVED	FSM_STATE |4:0]				
Reset	0	0	0	0	0	1	1	0

Table 73. FS_STATES register bit description

Bit	Symbol	Description
22	DBG_EXIT	Leave DEBUG mode
		0 No action
		1 Leave DEBUG mode
		Reset condition: POR
21	DBG_MODE	DEBUG mode status
		0 NOT in DEBUG mode
		1 In DEBUG mode
		Reset condition: Real-time information
19	OTP_CORRUPT	OTP bits corruption detection (5 ms cyclic check)
		0 No error
		1 OTP CRC error detected
		Reset condition: POR / clear on write (write ‘1’)
16 7	REG_CORRUPT	INIT register corruption detection (real-time comparison)
		0 No error
		1 INIT register content error detected (mismatch between FS_I_Register / FS_I_NOT_ Register)
		Reset condition: POR / clear on write (write ‘1’)
12 to 8	FSM_STATE[3:0]	Report fail-safe state machine current state
		0 0110 INIT_FS
		0 0111 WAIT_ABIST2
		0 1000 ABIST2
		0 1001 ASSERT_FS0B
		0 1010 NORMAL _FS
		Reset condition: Real-time information

18 OTP bits description

18.1 Main OTP Overview

Table 74. Main OTP_REGISTERS

Name [1]	Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OTP_CFG_VPRE_1	14	0	0	VPREV[5:0]					
OTP_CFG_VPRE_2	15	0	0	VPRESC[5:0]					
OTP_CFG_VPRE_3	16	VPREILIM[1:0]		1	0	**VPRESRLS[1:0]**		**VPRESRHS[1:0]**	
OTP_CFG_BOOST_1	17	0	0	VPRE_MODE	0	VBSTV[3:0]			
OTP_CFG_BOOST_2	18	BOOSTEN	VBSTTONTIME[1:0]		VBSTSC[4:0]				
OTP_CFG_BOOST_3	19	0	0	0	0	0	1	**VBSTSR[1:0]**	
OTP_CFG_BUCK1_1	1A	VB1V[7:0]							
OTP_CFG_BUCK1_2	1B	0	0	0	VB1INDOPT[1:0]		VB1SWILIM[1:0]		VB12 MULTIPH
OTP_CFG_BUCK2_1	1C	VB2V[7:0]							
OTP_CFG_BUCK2_2	1D	0	VB2INDOPT[1:0]		BUCK2EN	VB2SWILIM[1:0]		0	0
OTP_CFG_BUCK3_1	1E	BUCK3EN	VB3INDOPT[1:0]		VB3V[4:0]				
OTP_CFG_BUCK3_2	1F	VB2GMCOMP[2:0]			VB1GMCOMP[2:0]			VB3SWILIM[1:0]	
OTP_CFG_LDO	20	LDO2ILIM	LDO2V[2:0]			LDO1ILIM	LDO1V[2:0]		
OTP_CFG_SEQ_1	21	0	0	VB2S[2:0]			VB1S[2:0]		
OTP_CFG_SEQ_2	22	0	0	LDO2S[2:0]			LDO1S[2:0]		
OTP_CFG_SEQ_3	23	DVS_BUCK12[1:0]		DVS_BUCK3[1:0]		Tslot	VB3S[2:0]		
OTP_CFG_CLOCK_1	24	0	0	VPRE_ph[2:0]			1	0	0
OTP_CFG_CLOCK_2	25	0	0	BUCK1_ph[2:0]			VBST_ph[2:0]		
OTP_CFG_CLOCK_3	26	0	0	BUCK3_ph[2:0]			BUCK2_ph[2:0]		
OTP_CFG_CLOCK_4	27	BUCK3_ clk_sel	BUCK2_ clk_sel	BUCK1_ clk_sel	VBST_clk_sel	VPRE_clk_sel	PLL_sel	0	1
OTP_CFG_SM_1	28	0	0	**conf_TSD[5:0]**					
OTP_CFG_SM_2	29	0	0	0	VPRE_off_dly	Autoretry_ infinite	Autoretry_en	PSYNC_CFG	PSYNC_EN
OTP_CFG_VSUP_UV	2A	0	0	0	0	0	0	0	VSUPCFG
OTP_CFG_OV	2C	0	0	0	0	0	VDDIO_REG_ASSIGN[2:0]		
OTP_CFG_DEVID	2D	DeviceID[7:0]							

[1] Regulator behavior in case of TSD, VPRE and VBOOST slew rate parameters in bold can be changed later by SPI.

18.2 Main OTP bit description

Table 75. Main OTP bit description

Address	Register	Bit	Symbol	Value	Description
14	OTP_CFG_VPRE_1	5 to 0	VPREV[5:0]		VPRE output voltage
				0 01111	3.3 V
				010100	3.8 V
				0 10111	4.1 V
				1 00000	5.0 V

Table 75. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
15	OTP_CFG_VPRE_2	5 to 0	VPRESC[5:0]		VPRE slope compensation
				000100	40 mV/µs
				000101	50 mV/µs
				0 00110	60 mV/µs
				0 00111	70 mV/µs
				001000	80 mV/µs
				001001	90 mV/µs
				0 01010	100 mV/µs
				0 01110	140 mV/µs
				0 10001	170 mV/µs
				0 10100	200 mV/µs
				0 11000	240 mV/µs
16	OTP_CFG_VPRE_3	7 to 6	VPREILIM[1:0]		VPRE current limitation threshold
				00	50 mV
				01	80 mV
				10	120 mV
				11	150 mV
		3 to 2	VPRESRLS[1:0]		VPRE low-side slew rate control
				00	PU/PD/130 mA
				01	PU/PD/260 mA
				10	PU/PD/520 mA
				11	PU/PD/900 mA
		1 to 0	VPRESRHS[1:0]		VPRE high-side slew rate control
				00	PU/PD/130 mA
				01	PU/PD/260 mA
				10	PU/PD/520 mA
				11	PU/PD/900 mA
17	OTP_CFG_BOOST_1	5	VPRE_MODE		VPRE mode (PWM, APS)
				0	Force PWM for 455 kHz setting
				1	Automatic Pulse Skipping (APS) for 2.2 MHz setting
		3 to 0	VBSTV[3:0]		VBOOST output voltage
				0110	5.0 V
				1101	5.74 V
18	OTP_CFG_BOOST_2	7	BOOSTEN		BOOST enable
				0	Disabled
				1	Enabled
		6 to 5	VBSTTONTIME[1:0]		BOOST minimum ON time
				00	60 ns
				01	50 ns
		4 to 0	VBSTSC[4:0]		VBOOST slope compensation
				0 0110	160 mV/µs
				0 1100	125 mV/µs
				0 1110	79 mV/µs

Table 75. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
19	OTP_CFG_BOOST_3	1 to 0	VBSTSR[1:0]		VBOOST low-side slew rate control
				10	300 V/µs
				11	500 V/µs
1A	OTP_CFG_BUCK1_1	7 to 0	VB1V[7:0]		VBUCK1 output voltage
				0100 0000	0.8 V
				0100 0100	0.825 V
				0101 0000	0.9 V
				0101 1000	0.95 V
				0110 0000	1.0 V
				01100100	1.025 V
				0110 0101	1.03125 V
				0111 0000	1.1 V
				1000 0000	1.2 V
				1000 1000	1.25 V
				1001 0000	1.3 V
				1001 1000	1.35 V
				1010 0000	1.4 V
				1011 0000	1.5 V
				1011 0001	1.8 V
1B	OTP_CFG_BUCK1_2	4 to 3	VB1INDOPT[1:0]		BUCK1 inductor selection
				00	1 µH
				01	0.47 µH
				10	1.5 µH
		2 to 1	VB1SWILIM{1:0]		BUCK1 current limitation
				01	2.6 A
				11	4.5 A
		0	VB12MULTIPH		VBUCK1 and VBUCK2 multiphase operation enable
				0	Disabled
				1	Enabled

Table 75. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
1C	OTP_CFG_BUCK2_1	7 to 0	VB2V[7:0]		VBUCK2 output voltage
				0100 0000	0.8 V
				0100 0100	0.825 V
				0101 0000	0.9 V
				0101 1000	0.95 V
				0110 0000	1.0 V
				01100100	1.025 V
				0110 0101	1.03125 V
				0111 0000	1.1 V
				1000 0000	1.2 V
				1000 1000	1.25 V
				1001 0000	1.3 V
				1001 1000	1.35 V
				1010 0000	1.4 V
				1011 0000	1.5 V
				1011 0001	1.8 V
1D	OTP_CFG_BUCK2_2	6 to 5	VB2INDOPT[1:0]		BUCK2 inductor selection
				00	1 µH
				01	0.47 µH
				10	1.5 µH
		4	BUCK2EN		BUCK2 enable
				0	Disabled
				1	Enabled
		3 to 2	VB2SWILIM[1:0]		BUCK2 current limitation
				01	2.6 A
				11	4.5 A

Table 75. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
1E	OTP_CFG_BUCK3_1	7	BUCK3EN		BUCK3 enable
				0	Disabled
				1	Enabled
		6 to 5	VB3INDOPT[1:0]		BUCK3 inductor selection
				00	1 µH
				01	0.47 µH
				10	1.5 µH
		4 to 0	VB3V[4:0]		VBUCK3 output voltage
				0 0000	1.0 V
				0 0001	1.1 V
				0 0010	1.2 V
				0 0011	1.25 V
				0 0100	1.3 V
				0 0101	1.35 V
				0 0110	1.5 V
				0 0111	1.6 V
				0 1000	1.8 V
				0 1110	2.3 V
				1 0000	2.5 V
				1 0001	2.8 V
				1 0101	3.3 V
1F	OTP_CFG_BUCK3_2	7 to 5	VB2GMCOMP[2:0]		BUCK2 compensation network
				001	16.25 GM
				010	32.5 GM
				011	48.75 GM
				100	65 GM
				101	81.25 GM
				110	97.5 GM
		4 to 2	VB1GMCOMP[2:0]		BUCK1 compensation network
				001	16.25 GM
				010	32.5 GM
				011	48.75 GM
				100	65 GM
				101	81.25 GM
				110	97.5 GM
		1 to 0	VB3SWILIM[1:0]		BUCK3 current limitation
				01	2.6 A
				11	4.5 A

Table 75. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
20	OTP_CFG_LDO	7	LDO2ILIM		VLDO2 current limitation
				0	400 mA
				1	150 mA
		6 to 4	LDO2V[2:0]		VLDO2 output voltage
				000	1.1 V
				001	1.2 V
				010	1.6 V
				011	1.8 V
				100	2.5 V
				101	2.8 V
				110	3.3 V
				111	5.0 V
		3	LDO1ILIM		VLDO1 current limitation
				0	400 mA
				1	150 mA
		2 to 0	LDO1V[2:0]		VLDO1 output voltage
				000	1.1 V
				001	1.2 V
				010	1.6 V
				011	1.8 V
				100	2.5 V
				101	2.8 V
				110	3.3 V
				111	5.0 V
21	OTP_CFG_SEQ_1	5 to 3	VB2S[2:0]		BUCK2 sequencing slot
				000	Regulator start and stop in Slot 0
				001	Regulator start and stop in Slot 1
				010	Regulator start and stop in Slot 2
				011	Regulator start and stop in Slot 3
				100	Regulator start and stop in Slot 4
				101	Regulator start and stop in Slot 5
				110	Regulator start and stop in Slot 6
				111	Regulator does not start (enabled by SPI)
		2 to 0	VB1S[2:0]		BUCK1 sequencing slot
				000	Regulator start and stop in Slot 0
				001	Regulator start and stop in Slot 1
				010	Regulator start and stop in Slot 2
				011	Regulator start and stop in Slot 3
				100	Regulator start and stop in Slot 4
				101	Regulator start and stop in Slot 5
				110	Regulator start and stop in Slot 6
				111	Regulator does not start (enabled by SPI)

Table 75. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
22	OTP_CFG_SEQ_2	5 to 3	LDO2S[2:0]		LDO2 sequencing slot
				000	Regulator start and stop in Slot 0
				001	Regulator start and stop in Slot 1
				010	Regulator start and Stop in Slot 2
				011	Regulator start and stop in Slot 3
				100	Regulator start and stop in Slot 4
				101	Regulator start and stop in Slot 5
				110	Regulator start and stop in Slot 6
				111	Regulator does not start (enabled by SPI)
		2 to 0	LDO1S[2:0]		LDO1 sequencing slot
				000	Regulator start and stop in Slot 0
				001	Regulator start and stop in Slot 1
				010	Regulator start and stop in Slot 2
				011	Regulator start and stop in Slot 3
				100	Regulator start and stop in Slot 4
				101	Regulator start and stop in Slot 5
				110	Regulator start and stop in Slot 6
				111	Regulator does not start (enabled by SPI)
23	OTP_CFG_SEQ_3	7 to 6	DVS_BUCK12[1:0]		BUCK1 and BUCK2 soft start/stop configurability
				00	7.81 mV/µs
				01	3.13 mV/µs
				10	2.6 mV/µs
				11	2.23 mV/µs
		5 to 4	DVS_BUCK3[1:0]		BUCK3 soft start/stop configurability
				00	10.41 mV/µs
				01	3.47 mV/µs
				10	2.6 mV/µs
				11	2.08 mV/µs
		3	Tslot		Power up/down slot duration
				0	250 µs
				1	1 ms
		2 to 0	VB3S[2:0]		BUCK3 sequencing slot
				000	Regulator start and stop in Slot 0
				001	Regulator start and stop in Slot 1
				010	Regulator start and Stop in Slot 2
				011	Regulator start and stop in Slot 3
				100	Regulator start and stop in Slot 4
				101	Regulator start and stop in Slot 5
				110	Regulator start and stop in Slot 6
				111	Regulator does not start (enabled by SPI)

Table 75. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
24	OTP_CFG_CLOCK_1	5 to 3	VPRE_ph[2:0]		VPRE phase (delay) selection
				000	no delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5
				110	delay 6
				111	delay 7
25	OTP_CFG_CLOCK_2	5 to 3	BUCK1_ph[2:0]		VBUCK1 phase (delay) selection
				000	no delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5
				110	delay 6
				111	delay 7
		2 to 0	VBST_ph[2:0]		VBOOST phase (delay) selection
				000	no delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5
				110	delay 6
				111	delay 7
26	OTP_CFG_CLOCK_3	5 to 3	BUCK3_ph[2:0]		VBUCK3 phase (delay) selection
				000	no delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5
				110	delay 6
				111	delay 7
		2 to 0	BUCK2_ph[2:0]		VBUCK2 phase (delay) selection
				000	no delay
				001	delay 1
				010	delay 2
				011	delay 3
				100	delay 4
				101	delay 5
				110	delay 6
				111	delay 7

Table 75. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
27	OTP_CFG_CLOCK_4	7	BUCK3_clk_sel		BUCK3 clock selection
				0	CLK_DIV1 = 2.22 MHz
		6	BUCK2_clk_sel		BUCK2 clock selection
				0	CLK_DIV1 = 2.22 MHz
		5	BUCK1_clk_sel		BUCK1 clock selection
				0	CLK_DIV1 = 2.22 MHz
		4	VBST_clk_sel		VBOOST clock selection
				0	CLK_DIV1 = 2.22 MHz
		3	VPRE_clk_sel		VPRE clock selection
				0	CLK_DIV1 = 2.22 MHz
				1	CLK_DIV2 = 455 kHz
		2	PLL_sel		PLL enable
				0	Disabled
				1	Enabled
28	OTP_CFG_SM_1	5 to 0	conf_TSD[5]		BOOST behavior in case of TSD
				0	BOOST shutdown
				1	BOOST shutdown + DFS
			conf_TSD[4]		BUCK1 behavior in case of TSD
				0	BUCK1 shutdown
				1	BUCK1 shutdown + DFS
			conf_TSD[3]		BUCK2 behavior in case of TSD
				0	BUCK2 shutdown
				1	BUCK2 shutdown + DFS
			conf_TSD[2]		BUCK3 behavior in case of TSD
				0	BUCK3 shutdown
				1	BUCK3 Shutdown + DFS
			conf_TSD[1]		LDO1 behavior in case of TSD
				0	LDO1 shutdown
				1	LDO1 shutdown + DFS
			conf_TSD[0]		LDO2 behavior in case of TSD
				0	LDO2 shutdown
				1	LDO2 shutdown + DFS

Table 75. Main OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
29	OTP_CFG_SM_2	4	VPRE_off_dly		Delay to turn OFF VPRE at device power-down
				0	250 µs
				1	32 ms
		3	Auto retry_infinite		Deep fail-safe infinite auto retry enable
				0	Disabled
				1	Enabled
		2	Auto retry_en		Deep fail-safe auto retry enable
				0	Disabled
				1	Enabled
		1	PSYNC_CFG		Power-up synchronization
				0	2x FS6600
				1	1x FS6600 and 1x ext. PMIC
		0	PSYNC_EN		Synchronization with two devices
				0	Disabled
				1	Enabled
2A	OTP_CFG_VSUP_UV	0	VSUP_CFG		VSUP undervoltage threshold configuration
				0	4.9 V for Vpre < 4.5 V
				1	6.2 V for Vpre > 4.5 V
2C	OTP_CFG_OV	2 to 0	VDDIO_REG_ASSIGN[2:0]		Regulator assigned to VDDIO
				000	External regulator
				001	VPRE
				010	LDO1
				011	LDO2
				100	BUCK3
				101	External regulator
				110	External regulator
				111	External regulator
2D	OTP_CFG_DEVID	7 to 0	DeviceID[7:0]		Device ID

18.3 Fail-safe OTP Overview

Table 76. Fail-safe OTP_REGISTERS

Name	Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OTP_CFG_UVOV_1	0A	VCORE_V[7:0]							
OTP_CFG_UVOV_2	0B	VDDIOOVTH[3:0]				VCOREOVTH[3:0]			
OTP_CFG_UVOV_3	0C	0	0	VDDIO_V	VCORE_SVS_CLAMP[4:0]				
OTP_CFG_UVOV_4	0D	VMON2OVTH[3:0]				VMON1OVTH[3:0]			
OTP_CFG_UVOV_5	0E	VMON4OVTH[3:0]				VMON3OVTH[3:0]			
OTP_CFG_UVOV_6	0F	VDDIOUVTH[3:0]				VCOREUVTH[3:0]			
OTP_CFG_UVOV_7	10	VMON2UVTH[3:0]				VMON1UVTH[3:0]			
OTP_CFG_UVOV_8	11	VMON4UVTH[3:0]				VMON3UVTH[3:0]			
OTP_CFG_PGOOD	12	0	PGOOD_ RSTB	PGOOD_ VMON4	PGOOD_ VMON3	PGOOD_ VMON2	PGOOD_ VMON1	PGOOD_ VDDIO	PGOOD_ VCORE
OTP_CFG_ABIST1	13	0	0	ABIST1_ VMON4	ABIST1_ VMON3	ABIST1_ VMON2	ABIST1_ VMON1	ABIST1_ VDDIO	ABIST1_ VCORE
OTP_CFG_ASIL	14	WD_DIS	WD_Selection	ERRMON_EN	FCCU_EN	VMON4_EN	VMON3_EN	VMON2_EN	VMON1_EN
OTP_CFG_DGLT_DUR_1	16	0	0	VCORE_UV_DGLT[1:0]		VCORE_ OV_DGLT	VDDIO_UV_DGLT[1:0]		VDDIO_ OV_DGLT
OTP_CFG_DGLT_DUR_2	17	0	0	0	0	0	VMONx_UV_DGLT[1:0]		VMONx_ OV_DGLT

18.4 Fail-safe OTP bit description

Table 77. Fail-safe OTP bit description

Address	Register	Bit	Symbol	Value	Description
0A	OTP_CFG_UVOV_1	7 to 0	VCORE_V[7:0]		VCORE (VBUCK1) monitoring voltage
				0100 0000	0.8 V
				0100 0100	0.825 V
				0101 0000	0.9 V
				0101 1000	0.95 V
				0110 0000	1 V
				01100100	1.025 V
				0110 0101	1.03125 V
				0110 0000	1.1 V
				1000 0000	1.2 V
				1000 1000	1.25 V
				1001 0000	1.3 V
				1001 1000	1.35 V
				1010 0000	1.4 V
				1011 0000	1.5 V
				1011 0001	1.8 V

Table 77. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
0B	OTP_CFG_UVOV_2	7 to 4	VDDIOOVTH[3:0]		VDDIO overvoltage threshold configuration
				0000	104.5 %
				0001	105 %
				0010	105.5 %
				0011	106 %
				0100	106.5 %
				0101	107 %
				0110	107.5
				0111	108 %
				1000	108.5 %
				1001	109 %
				1010	109.5 %
				1011	110 %
				1100	110.5 %
				1101	111 %
				1110	111.5 %
				1111	112 %
		3 to 0	VCOREOVTH[3:0]		VCOREMON overvoltage threshold configuration
				0000	104.5 %
				0001	105 %
				0010	105.5 %
				0011	106 %
				0100	106.5 %
				0101	107 %
				0110	107.5
				0111	108 %
				1000	108.5 %
				1001	109 %
				1010	109.5 %
				1011	110 %
				1100	110.5 %
				1101	111 %
				1110	111.5 %
				1111	112 %
0C	OTP_CFG_UVOV_3	5	VDDIO_V		VDDIO voltage selection
				0	3.3 V
				1	5 V
0C	OTP_CFG_UVOV_3	4 to 0	VCORE_SVS_CLAMP[4:0]		SVS max value allowed (mask)
				00000	2 steps available (-12.5 mV)
				00001	4 steps available (-25 mV)
				00011	8 steps available (-50 mV)
				00100	16 steps available (-100 mV)

Table 77. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
0D	OTP_CFG_UVOV_4	7 to 4	VMON2OVTH[3:0]		VMON2 overvoltage threshold configuration
				0000	104.5 %
				0001	105 %
				0010	105.5 %
				0011	106 %
				0100	106.5 %
				0101	107 %
				0110	107.5
				0111	108 %
				1000	108.5 %
				1001	109 %
				1010	109.5 %
				1011	110 %
				1100	110.5 %
				1101	111 %
				1110	111.5 %
				1111	112 %
		3 to 0	VMON1OVTH[3:0]		VMON1 overvoltage threshold configuration
				0000	104.5 %
				0001	105 %
				0010	105.5 %
				0011	106 %
				0100	106.5 %
				0101	107 %
				0110	107.5
				0111	108 %
				1000	108.5 %
				1001	109 %
				1010	109.5 %
				1011	110 %
				1100	110.5 %
				1101	111 %
				1110	111.5 %
				1111	112 %

Table 77. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
0E	OTP_CFG_UVOV_5	7 to 4	VMON4OVTH[3:0]		VMON4 overvoltage threshold configuration
				0000	104.5 %
				0001	105 %
				0010	105.5 %
				0011	106 %
				0100	106.5 %
				0101	107 %
				0110	107.5
				0111	108 %
				1000	108.5 %
				1001	109 %
				1010	109.5 %
				1011	110 %
				1100	110.5 %
				1101	111 %
				1110	111.5 %
				1111	112 %
		3 to 0	VMON3OVTH[3:0]		VMON3 overvoltage threshold configuration
				0000	104.5 %
				0001	105 %
				0010	105.5 %
				0011	106 %
				0100	106.5 %
				0101	107 %
				0110	107.5
				0111	108 %
				1000	108.5 %
				1001	109 %
				1010	109.5 %
				1011	110 %
				1100	110.5 %
				1101	111 %
				1110	111.5 %
				1111	112 %

Table 77. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
0F	OTP_CFG_UVOV_6	7 to 4	VDDIOUVTH[3:0]		VDDIO undervoltage threshold configuration
				0000	95.5 %
				0001	95 %
				0010	94.5 %
				0011	94 %
				0100	93.5 %
				0101	93 %
				0110	92.5 %
				0111	92 %
				1000	91.5 %
				1001	91 %
				1010	90.5 %
				1011	90 %
				1100	89.5 %
				1101	89 %
				1110	88.5 %
				1111	88 %
		3 to 0	VCOREUVTH[3:0]		VCOREMON undervoltage threshold configuration
				0000	95.5 %
				0001	95 %
				0010	94.5 %
				0011	94 %
				0100	93.5 %
				0101	93 %
				0110	92.5 %
				0111	92 %
				1000	91.5 %
				1001	91 %
				1010	90.5 %
				1011	90 %
				1100	89.5 %
				1101	89 %
				1110	88.5 %
				1111	88 %

Table 77. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
10	OTP_CFG_UVOV_7	7 to 4	VMON2UVTH[3:0]		VMON2 undervoltage threshold configuration
				0000	95.5 %
				0001	95 %
				0010	94.5 %
				0011	94 %
				0100	93.5 %
				0101	93 %
				0110	92.5 %
				0111	92 %
				1000	91.5 %
				1001	91 %
				1010	90.5 %
				1011	90 %
				1100	89.5 %
				1101	89 %
				1110	88.5 %
				1111	88 %
		3 to 0	VMON1UVTH[3:0]		VMON1 undervoltage threshold configuration
				0000	95.5 %
				0001	95 %
				0010	94.5 %
				0011	94 %
				0100	93.5 %
				0101	93 %
				0110	92.5 %
				0111	92 %
				1000	91.5 %
				1001	91 %
				1010	90.5 %
				1011	90 %
				1100	89.5 %
				1101	89 %
				1110	88.5 %
				1111	88 %

Table 77. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
11	OTP_CFG_UVOV_8	7 to 4	VMON4UVTH[3:0]		VMON4 undervoltage threshold configuration
				0000	95.5 %
				0001	95 %
				0010	94.5 %
				0011	94 %
				0100	93.5 %
				0101	93 %
				0110	92.5 %
				0111	92 %
				1000	91.5 %
				1001	91 %
				1010	90.5 %
				1011	90 %
				1100	89.5 %
				1101	89 %
				1110	88.5 %
				1111	88 %
		3 to 0	VMON3UVTH[3:0]		VMON3 undervoltage threshold configuration
				0000	95.5 %
				0001	95 %
				0010	94.5 %
				0011	94 %
				0100	93.5 %
				0101	93 %
				0110	92.5 %
				0111	92 %
				1000	91.5 %
				1001	91 %
				1010	90.5 %
				1011	90 %
				1100	89.5 %
				1101	89 %
				1110	88.5 %
				1111	88 %

Table 77. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
12	OTP_CFG_PGOOD	6	PGOOD_RSTB		RSTB assignment to PGOOD
				0	Not assigned
				1	Assigned
		5	PGOOD_VMON4		VMON4 assignment to PGOOD
				0	Not assigned
				1	Assigned
		4	PGOOD_VMON3		VMON3 assignment to PGOOD
				0	Not assigned
				1	Assigned
		3	PGOOD_VMON2		VMON2 assignment to PGOOD
				0	Not assigned
				1	Assigned
		2	PGOOD_VMON1		VMON1 assignment to PGOOD
				0	Not assigned
				1	Assigned
		1	PGOOD_VDDIO		VDDIO assignment to PGOOD
				0	Not assigned
				1	Assigned
		0	PGOOD_VCORE		VCORE (BUCK1) assignment to PGOOD
				0	Not assigned
				1	Assigned
13	OTP_CFG_ABIST1	5	ABIST_VMON4		VMON4 assignment to ABIST1
				0	Not assigned
				1	Assigned
		4	ABIST_VMON3		VMON3 assignment to ABIST1
				0	Not assigned
				1	Assigned
		3	ABIST_VMON2		VMON2 assignment to ABIST1
				0	Not assigned
				1	Assigned
		2	ABIST_VMON1		VMON1 assignment to ABIST1
				0	Not assigned
				1	Assigned
		1	ABIST_VDDIO		VDDIO assignment to ABIST1
				0	Not assigned
				1	Assigned
		0	ABIST_VCORE		VCORE assignment to ABIST1
				0	Not assigned
				1	Assigned

Table 77. Fail-safe OTP bit description*...continued*

Address	Register	Bit	Symbol	Value	Description
14	OTP_CFG_ASIL	7	WD_DIS		Watchdog monitoring enable
				0	Enabled
				1	Disabled
		6	WD_SELECTION		Watchdog mode selection
				0	Simple WD
				1	Challenger WD
		5	ERRMON_EN		ERRMON monitoring enable
				0	Disabled
				1	Enabled
		4	FCCU_EN		FCCU monitoring enable
				0	Disabled
				1	Enabled
		3	VMON4_EN		VMON4 monitoring enable
				0	Disabled
				1	Enabled
		2	VMON3_EN		VMON3 monitoring enable
				0	Disabled
				1	Enabled
		1	VMON2_EN		VMON2 monitoring enable
				0	Disabled
				1	Enabled
		0	VMON1_EN		VMON1 monitoring enable
				0	Disabled
				1	Enabled
16	OTP_CFG_DGLT_DUR_1	5 to 4	VCORE_UV_DGLT[1:0]		VCORE undervoltage filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40 µs
		3	VCORE_OV_DGLT		VCORE overvoltage filtering time
				0	25 µs
				1	45 µs
		2 to 1	VDDIO_UV_DGLT[1:0]		VDDIO undervoltage filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40 µs
		0	VDDIO_OV_DGLT		VDDIO overvoltage filtering time
				0	25 µs
				1	45 µs

Table 77. Fail-safe OTP bit description...*continued*

Address	Register	Bit	Symbol	Value	Description
17	OTP_CFG_DGLT_DUR_2	2 to 1	VMONx_UV_DGLT[1:0]		VMONx undervoltage filtering time
				00	5 µs
				01	15 µs
				10	25 µs
				11	40 µs
		0	VMONx_OV_DGLT		VMONx overvoltage filtering time
				0	25 µs
				1	45 µs

19 Best of supply

19.1 Functional description

VBOS regulator manages the best of supply from VSUP, VPRE and VBOOST to efficiently generate 5.0 V output to supply the internal biasing of the device. VBOS is also the supply of VPRE high-side and low-side gate drivers and VBOOST low-side gate driver.

VBOS undervoltage may not guarantee the full functionality of the device. Consequently, VBOS_UVL detection powers down the device.

V_{SUP_UV7} undervoltage threshold is used to enable the path from VSUP to VBOS when VSUP < V_{SUP_UV7} to have a low drop path from VSUP, while VPRE is going low and to power up the device when VPRE is not started. When VSUP > V_{SUP_UV7}, VBOS is forced to use either VPRE or VBOOST to optimize the efficiency.

19.2 Electrical characteristics

Table 78. Best of supply electrical characteristics

T_A = –40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Best of supply					
V_{BOS}	Best of supply output voltage	3.3	5.0	5.25	V
V_{BOS_UVH}	VBOS undervoltage threshold high (VBOS rising)	4.1	—	4.5	V
V_{BOS_UVL}	VBOS undervoltage threshold low (VBOS falling)	3.2	—	3.4	V
T_{BOS_UV}	V_{BOS_UVH} and V_{BOS_UVL} filtering time	6.0	10	15	µs
V_{BOS_POR}	VBOS power-on reset threshold	—	—	2.5	V
T_{BOS_POR}	V_{BOS_POR} filtering time	0.5	—	1.5	µs
I_{BOS}	Best of supply current capability	—	—	60	mA
C_{OUT_BOS}	Effective output capacitor	4.7	—	10	µF
	Output decoupling capacitor	—	0.1	—	µF

20 High-voltage buck: VPRE

20.1 Functional description

VPRE block is a high-voltage, synchronous, peak current mode buck controller. VPRE is working with external logical level NMOS in force PWM mode at 455 kHz and in Automatic Pulse Skipping (APS) mode at 2.22 MHz. The APS mode helps to maintain the correct output voltage at high input voltage by skipping some turn ON cycles of the HS FET below the minimum duty cycle. VPRE input voltage is naturally limited to $V_{SUP} = L_{PI\_DCR} \times I_{PRE} + V_{PRE\_UVL} / D_{MAX}$ with $D_{MAX} = 1 - (F_{PRE\_SW} \times T_{PRE\_OFF\_MIN})$.

A bootstrap capacitor is required to supply the gate drive circuit of the high-side NMOS. The output voltage is configurable by OTP from 3.3 V to 5.0 V, and the switching frequency is configurable by OTP at 455 kHz for 12 V and 24 V transportation applications or 2.22 MHz for 12 V automotive applications. The stability is ensured by an external Type 2 compensation network with slope compensation.

The output current is sensed via an external shunt in series with the inductor and the maximum current capability is defined by the external components (NMOS gate charge, inductor, shunt resistor), the gate driver current capability and the switching frequency. An overcurrent detection is implemented to protect the external MOSFETs. If an overcurrent is detected after the HS minimum TON time, the HS is turned OFF and will be turned ON again at the next rising edge of the switching clock. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition on VPRE and/or one of the cascaded regulators.

The maximum input voltage is 60 V and allows operation in 24 V truck applications without external protection to sustain ISO 16750-2:2012 load dump pulse 5b. VPRE must be the input supply of the BOOST and BUCK1,2. VPRE can be the input supply of BUCK3 and LDO1. VPRE can be the supply of local loads remaining inside the ECU.

VPRE switching frequency is derived from the internal oscillator.

V_{PRE_UVH}, V_{PRE_UVL} and $V_{PRE\_FB\_OV}$ thresholds are monitored from PRE_FB pin and manage some transitions of the main state machine described in Section 14.1 "Simplified functional state diagram". These monitorings are not safety related.

20.2 Application schematic

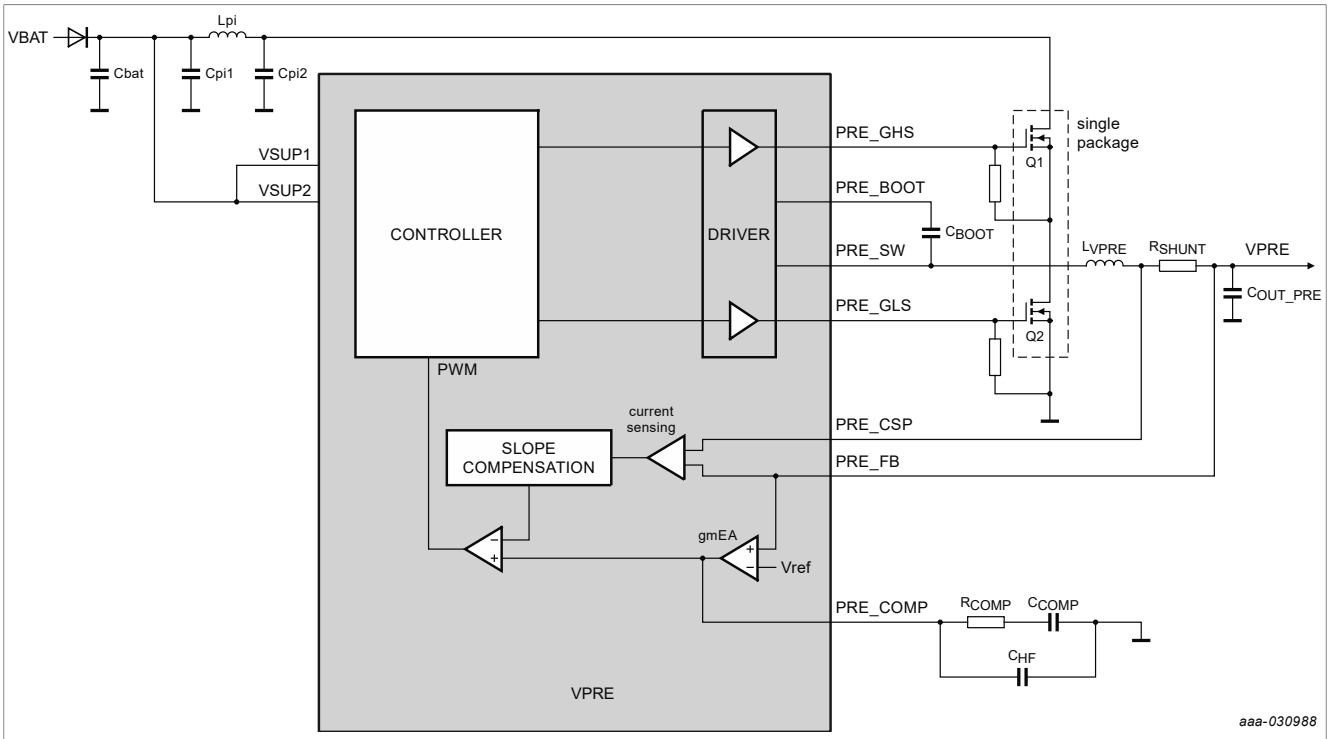


Figure 11. VPRE schematic

A PI filter, with F_{RES} = 1 / [2π x √(LCpi1)] and calculated for Fres < F_{PRE_SW} / 10, is required to filter VPRE switching frequency on the battery line. VSUP1, 2 pins must be connected before the PI filter for a clean biasing of the device. Cpi1 capacitor shall be implemented close to VSUP1,2 pins. Cpi2 capacitor shall be implemented close to Q1. The bootstrap capacitor value should be sized to be >10 times the gate source capacitor of Q1. Gate to source resistor on Q1 and Q2 is recommended in case of pin disconnection to guarantee a passive switch OFF of the transistors.

20.3 Compensation network and stability

The external compensation network, made with R_{COMP}, C_{COMP} and C_{HF} shall be calculated for best compromise between stability and transient response, based on below conceptual plot of Type 2 compensation network transfer function.

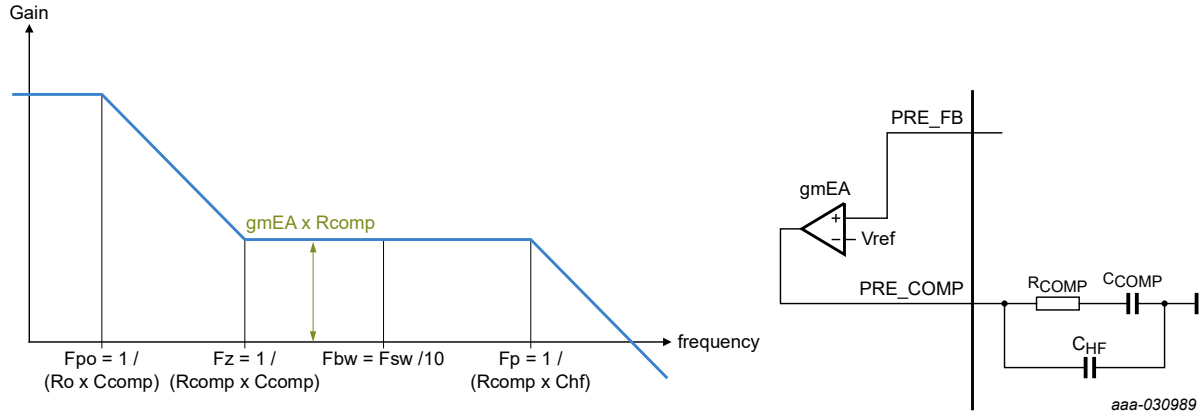


Figure 12. Type 2 compensation network concept

Calculation guideline:

- System bandwidth for VPRE = 455 kHz: $F_{bw} = F_{PRE\_SW} / 10$
- System bandwidth for VPRE = 2.22 MHz: $F_{bw} = F_{PRE\_SW} / 15$
- Compensation zero: $Fz = F_{bw} / 10$
- Compensation pole for VPRE = 455 kHz: $Fp = F_{PRE\_SW} / 2$
- Compensation pole for VPRE = 2.22 MHz: $Fp = F_{PRE\_SW} / 4$
- $F_{GBW} = 1 / (2\pi \times R_{SHUNT} \times V_{PRE\_LIM\_GAIN} \times C_{OUT\_PRE})$
- Error amplifier gain: $EA\_gain = (V_{REF} / V_{PRE}) \times gmEA_{PRE} \times R_{COMP} = 10 \text{ ^ } LOG (F_{BW} / F_{GBW})$
- $V_{REF} = 1.0$ V, $R_{COMP} = V_{PRE} \times (EA\_gain / gmEA_{PRE})$
- $C_{COMP} = 1 / (2\pi \times Fz \times R_{COMP})$
- $C_{HF} = 1 / (2\pi \times Fp \times R_{COMP})$
- Slope compensation: $Se > (V_{PRE} / L_{VPRE}) \times R_{SHUNT} \times V_{PRE\_LIM\_GAIN}$

The compensation network can be automatically calculated with the sheet FS85_VPRE_VBOOST_Components in the FS85_FS84_OTP_Config.xlsm file which is using the same formulas. A Simplis simulation is recommended to verify the Phase and Gain Margin with normalized components.

Use case calculation with $V_{PRE} = 4.1$ V, $L_{VPRE} = 6.8$ µH, $F_{PRE\_SW} = 455$ kHz, $C_{OUT\_PRE} = 66$ µF, $R_{SHUNT} = 10.0$ mΩ:

- System bandwidth: $F_{bw} = 45$ kHz
- Compensation zero: $Fz = 4.5$ kHz
- Compensation pole: $Fp = 227.5$ kHz
- $F_{GBW} = 53$ kHz
- Error amplifier gain: $EA\_gain = 10 \text{ ^ } LOG (F_{BW} / F_{GBW}) = 0.86$
- $R_{COMP} = 2.34$ kΩ = 2.2 kΩ
- $C_{COMP} = 15.9$ nF = 16 nF
- $C_{HF} = 318$ pF = 330 pF
- Slope compensation: Se > 30 mV/µs

Use case stability verification:

- Phase margin target PM > 45° and gain margin target GM > 6 dB.

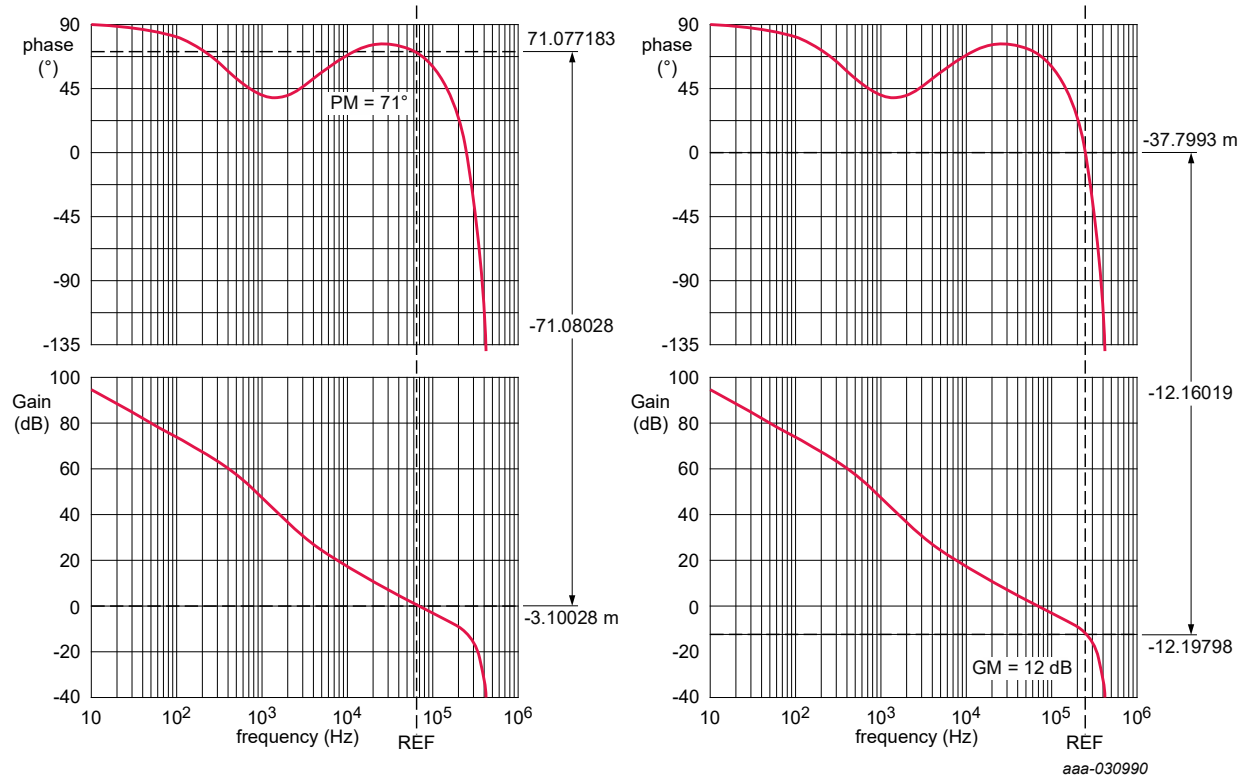


Figure 13. Phase and gain margin simulation

Use case transient response verification:

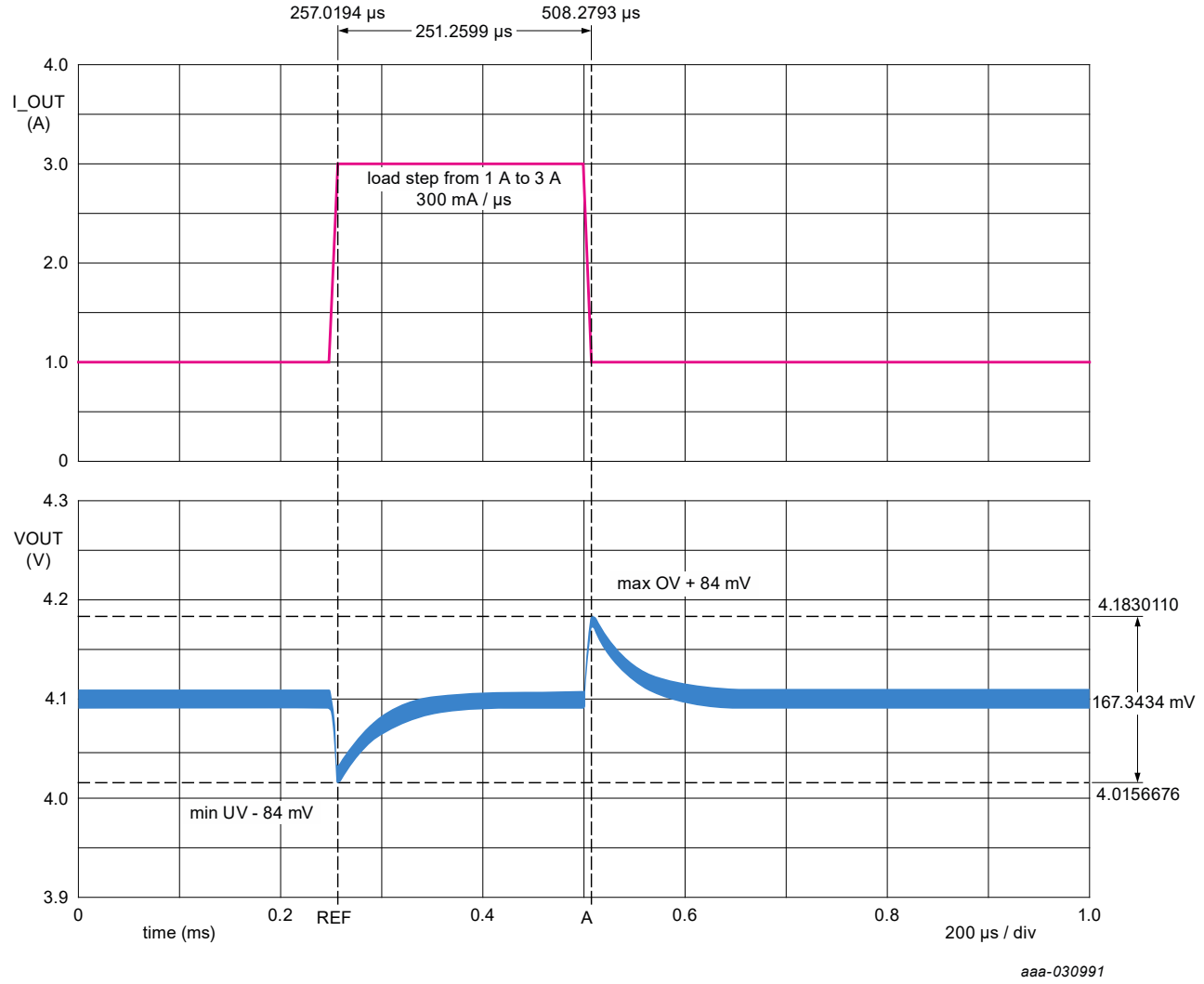


Figure 14. Transient response simulation

20.4 Electrical characteristics

Table 79. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VPRE					
V_{PRE}	Output voltage (OTP_VPREV[5:0] bits)	3.2	3.3	3.4	V
		3.68	3.8	3.92	V
		3.98	4.1	4.22	V
		4.85	5.0	5.15	V
$V_{PRE\_SOFT\_START}$	Output voltage from 10 % to 90 %	250	450	650	µs
	Digital DAC soft start completion	—	—	1.35	ms
$V_{PRE\_STARTUP}$	Overshoot at startup	—	—	3	%
$V_{PRE\_FB\_OV}$	Over voltage threshold protection	5.5	6.0	6.5	V

Table 79. Electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
$T_{PRE\_FB\_OV}$	$V_{PRE\_FB\_OV}$ filtering time	1	2	3	µs
V_{PRE_UVH}	Under voltage threshold high	2.9	—	3.1	V
V_{PRE_UVL}	Under voltage threshold low	2.5	—	2.7	V
T_{PRE_UV}	V_{PRE_UVH} and V_{PRE_UVL} filtering time	6.0	10	15	µs
F_{PRE_SW}	Switching frequency range (OTP_VPRE_clk_sel bit)	430	455	480	kHz
		2.1	2.22	2.35	MHz
L_{VPRE}	Typical inductor value for F_{PRE_SW} = 455 kHz	4.7	6.8	10	µH
	Typical inductor value for F_{PRE_SW} = 2.22 MHz	1.5	2.2	4.7	µH
$V_{PRE\_LINE\_REG\_455k}$	Transient line regulation at 455 kHz VSUP = 6.0 V to 18 V and VSUP = 12 V to 36 V (Cin = 47 µF + PI filter, L_{VPRE} = 6.8 µH, C_{OUT_PRE} = 66 µF, dv/dt = 100 mV/µs)	-3	—	3	%
$V_{PRE\_LINE\_REG\_2.2M}$	Transient line regulation at 2.22 MHz VSUP = 6.0 V to 18 V (Cin = 47 µF + PI filter, L_{VPRE} = 2.2 µH, C_{OUT_PRE} = 44 µF, dv/dt = 100 mV/µs)	-3	—	3	%
$V_{PRE\_LOAD\_REG\_455k}$	Transient load regulation at 455 kHz VSUP = 6.0 V to 36 V (L_{VPRE} = 6.8 µH, C_{OUT_PRE} = 66 µF, from 1.0 A to 3.0 A, di/dt = 300 mA/µs)	−3	—	3	%
$V_{PRE\_LOAD\_REG\_2.2M}$	Transient load regulation at 2.22 MHz VSUP = 6.0 V to 18 V (L_{VPRE} = 2.2 µH, C_{OUT_PRE} = 44 µF, from 1.0 A to 3.0 A, di/dt = 300 mA/µs)	-3	—	3	%
$V_{PRE\_RIPPLE\_455k}$	Ripple at 455 kHz VSUP = 12 V and VSUP = 24 V (L_{VPRE} = 6.8 µH, C_{OUT_PRE} = 66 µF, V_{PRE} = 3.3 V and 5.0 V, I_{PRE} = 4A)	-1	—	1	%
$V_{PRE\_RIPPLE\_2.2M}$	Ripple at 2.22 MHz VSUP = 12 V (L_{VPRE} = 2.2 µH, C_{OUT_PRE} = 44 µF, V_{PRE} = 3.3 V and 5.0 V, I_{PRE} = 2A)	-0.5	—	0.5	%
$T_{PRE\_ON\_MIN}$	HS minimum ON time	15	25	35	ns
$T_{PRE\_OFF\_MIN}$	HS minimum OFF time	20	40	60	ns
R_{SHUNT}	Current sense resistor (±1 %)	10	—	20	mΩ
$V_{PRE\_LIM\_GAIN}$	Current sense amplifier gain	4.5	5	5.5	
$V_{PRE\_LIM\_TH1}$	Current sense amplifier peak detection threshold (OTP_VPREILIM[1:0] bits) Note: 150 mV setting is not available for 2.22 MHz	37.5	50	62.5	mV
		64	80	96	mV
		96	120	144	mV
		120	150	180	mV
I_{LIM_PRE}	I_{LIM_PRE} = $V_{PRE\_LIM\_TH}$ / R_{SHUNT} Inductor peak current limitation range (R_{SHUNT} = 10 mΩ, $V_{PRE\_LIM\_TH1}$ = 50 mV)	3.75	5	6.25	A
	Inductor peak current limitation range (R_{SHUNT} = 10 mΩ, $V_{PRE\_LIM\_TH1}$ = 150 mV)	12	15	18	A

Table 79. Electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
	To be recalculated for different R_{SHUNT} and different $V_{PRE\_LIM\_TH}$				
V_{PRE_DRV}	HS and LS gate driver output voltage	—	VBOS	—	V
$I_{PRE\_GATE\_DRV}$	HS and LS gate driver pull up and pulldown current capability (OTP_VPRESRHS[1:0] and OTP_VPRESRLS[1:0] bits by default + VPRESRHS[1:0] and VPRESRLS[1:0] bits by SPI)	60	130	220	mA
		120	260	430	mA
		220	520	860	mA
		420	900	1490	mA
C_{OUT_PRE}	Effective output capacitor for F_{PRE_SW} = 455 kHz	40	66	220	µF
	Effective output capacitor for F_{PRE_SW} = 2.22 MHz	20	44	110	µF
	Output decoupling capacitor	—	0.1	—	µF
C_{IN_PRE}	Effective input capacitor (Cpi2)	20	—	—	µF
	Input decoupling capacitor	—	0.1	—	µF
I_{PRE_DRV}	Combined HS + LS gate driver average current capability $I_{PRE\_DRV} < F_{PRE\_SW} \times (QC_{HS} + QC_{LS})$ with QC_{HS} = gate charge of Q2 at VBOS with QC_{LS} = gate charge of Q1 at VBOS	—	—	30	mA
$gmEA_{PRE}$	Error amplifier transconductance	1.0	1.5	2.1	ms
V_{PRE_SLOPE}	Slope compensation (OTP_VPRESC[5:0] bits)	29	40	51	mV/µs
		36	50	64	mV/µs
		43	60	77	mV/µs
		51	70	89	mV/us
		58	80	102	mV/µs
		65	90	115	mV/µs
		73	100	127	mV/µs
		102	140	178	mV/µs
		124	170	216	mV/µs
		146	200	254	mV/µs
		175	240	305	mV/µs
$T_{PRE\_UV\_DFS}$	V_{PRE_UVL} filtering time to go to DEEP-FS during VPRE start up	1.8	2	2.2	ms
T_{PRE_DT}	Dead time to avoid cross conduction (this timing does not take into account the external FET turn ON/OFF times)	20	30	40	ns
VPRE_OFF_DLY	Wait time between VBOOST OFF and VPRE OFF (OTP_VPRE_off_dly bit)	—	250	—	µs
		—	32	—	ms
R_{PRE_DIS}	Discharge resistor (when VPRE is disabled)	250	500	1000	Ω
$I_{PRE\_SW\_LKG}$	PRE_SW leakage	—	—	10	µA
R_{DRV_OFF}	HS and LS gate driver pulldown resistor when VPRE is disabled	5	—	35	kΩ
R_{BOOT_OFF}	PRE_BOOT pulldown resistor when VPRE is disabled	1.2	—	2.6	kΩ

Table 79. Electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
I_{BOOT_LKG}	PRE_BOOT leakage	—	—	10	µA

20.5 VPRE external MOSFETs

MOSFETs selection:

- Logical level NMOS, gate drive comes from VBOS (5.0 V)
- VDS > 60 V for 24 V truck, bus applications
- VDS > 40 V for 12 V automotive applications
- Qg < 15 nC at Vgs = 5.0 V is recommended for 455 kHz
- Qg < 7 nC at Vgs = 5.0 V is recommended for 2.22 MHz
- Recommended components

Applications	Fpre	Ipre < 2.0 A	Ipre < 4.0 A	Ipre < 6.0 A	Ipre < 10 A
12 V	455 kHz	BUK9K25-40E, BUK9K18-40E	BUK9K25-40E, BUK9K18-40E	BUK9K18-40E	BUK9K18-40E, NVTFS5C471NLWFTAG, HS = BUK9M9R5-40H, LS = BUK9M3R3-40H
	2.22 MHz	BUK9K25-40E, BUK9Y29-40E	BUK9K25-40E, BUK9Y29-40E	BUK9K25-40E, BUK9Y29-40E	N/A
24 V	455 kHz	BUK9K35-60E, BUK9K52-60E	BUK9K35-60E, BUK9K52-60E	BUK9K35-60E	BUK9K12-60E

Other MOSFETs are possible but should have similar performances than the recommended references. The maximum current at 2.22 MHz is limited to 6 A for which the efficiency is equivalent to 10 A at 455 kHz. Above, the power dissipation in the external MOSFETs becomes important and the junction temperature may rise above 175 °C.

VPRE switching slew rate can be configured by SPI to align with external MOSFET selection, VPRE switching frequency, and to optimize power dissipation and EMC performance. NXP recommends configuring the maximum slew rate by OTP and reducing it later by SPI if needed. FS6600 is using current source to drive the external MOSFET so adding an external serial resistor with the gate will not affect the slew rate. NXP recommends changing the current source selection by SPI to change the slew rate.

VPRE MOSFET switching time can be estimated to $T_{SW} = (Q_{GD} + Q_{GS} / 2) / I_{PRE\_GATE\_DRV}$ using the gate charge definition from Figure 15. Q_{GD} and Q_{GS} can be extracted from the MOSFET data sheet.

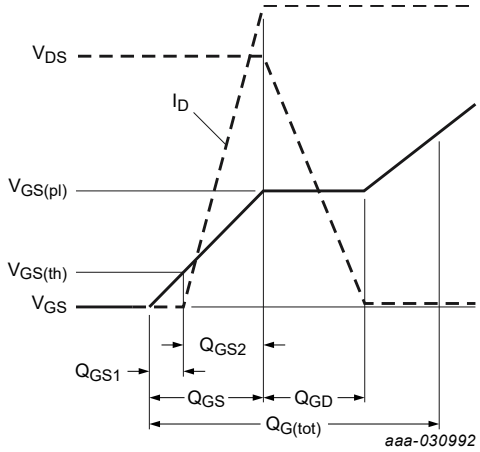


Figure 15. MOSFET gate charge definition

20.6 VPRE efficiency

VPRE efficiency versus current load is given for information based on external component criteria provided and VSUP voltage 14 V. If the conditions change, it has to be recalculated with the FS85_PDTCAL tool. The real efficiency has to be verified by measurement at the application level.

VPRE at 455 kHz: BUK9K18-40E
VPRE at 2.22 MHz: BUK9K25-40E

Ext. C and L			
Fpre	455	2220	kHz
Cin	47	47	µF
ESR Cin	30	30	mΩ
Cout	66	44	µF
ESR Cout	10	10	mΩ
L coil	6.8	2.2	µH
DCR coil	25	25	mΩ
Rshunt	10	10	mΩ
Ext. MOSFET's			
GHS_drive	5	5	V
HS_Rdson	17	24	mΩ
HS_QGtot	7	5	nC
HS_QGD	3	2.4	nC
HS_QGS	2	1.4	nC
HS_Igate	900	900	mA
THS_sw	5	4	ns
GLS_drive	5	5	V
LS_Rdson	17	24	mΩ
LS_QGtot	7	5	nC
LS_QGD	3	2.4	nC
LS_QGS	2	1.4	nC
LS_QRR	16	7.6	nC
LS_Igate	900	900	mA
TLS_sw	5	4	ns

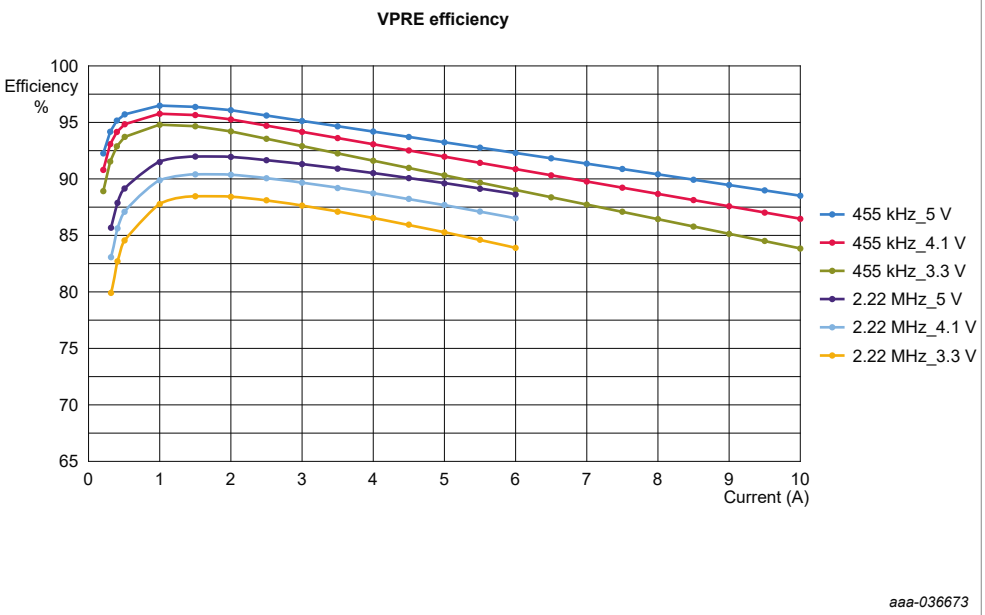


Figure 16. VPRE theoretical efficiency

20.7 VPRE not populated

When two FS6600 are used, only one VPRE may be required. It is possible to not populate the external components of the second VPRE to optimize the bill of material.

In that case, specific connection of the VPRE2 pins is required:

- PRE_FB2 must be connected to PRE_FB1
- PRE_CSP2 must be connected to PRE_FB1
- PRE_COMP2 must be left open
- PRE_SW2 must be connected to GND
- PRE_BOOT2 must be connected to VBOS2
- PRE_GHS2 and PRE_GLS2 must be left open

After the startup phase, VPRE2 shall be disabled by SPI with VPDIS bit.

21 Low-voltage boost: VBOOST

21.1 Functional description

VBOOST block is a low-voltage, asynchronous, peak current mode boost converter. VBOOST works in PWM and uses an external diode and an internal low-side FET. VBOOST enters Skip mode to maintain the correct output voltage in light load condition. The output voltage is configurable by OTP at 5.0 V or 5.74 V, the switching frequency is 2.22 MHz and the output current is limited to 1.5 A peak input current. The input of the boost is connected to the output of VPRE. This block is intended to supply LDO1, LDO2, BUCK3 or an external regulator. The stability is ensured by an internal Type 2 compensation network with slope compensation.

VBOOST switching frequency is derived from the internal oscillator.

An overcurrent detection and a thermal shutdown are implemented to protect the internal MOSFET. If an overcurrent is detected after the LS minimum TON time, the LS is turned OFF and will be turned ON again at the next rising edge of the switching clock. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition on one of the cascaded regulators.

Since the current limitation is on the input current, Table 80 summarizes the expected output current capability depending on VPRE and VBOOST voltage configurations and L = 4.7 µH.

Table 80. Output current capability

VPRE	VBOOST	IBOOST_OUT
3.3 V	5.0 V	800 mA
	5.74 V	700 mA
4.1 V	5.0 V	1 A
	5.74 V	900 mA
5.0 V	5.74 V	1.1 A

An overvoltage protection is implemented on BOOST_LS pin. When V_{BOOST_OV} is detected during two consecutive turn ON cycles, VBOOST is disabled. A SPI command is required to enable it again. This monitoring is not safety related.

21.2 Application schematic

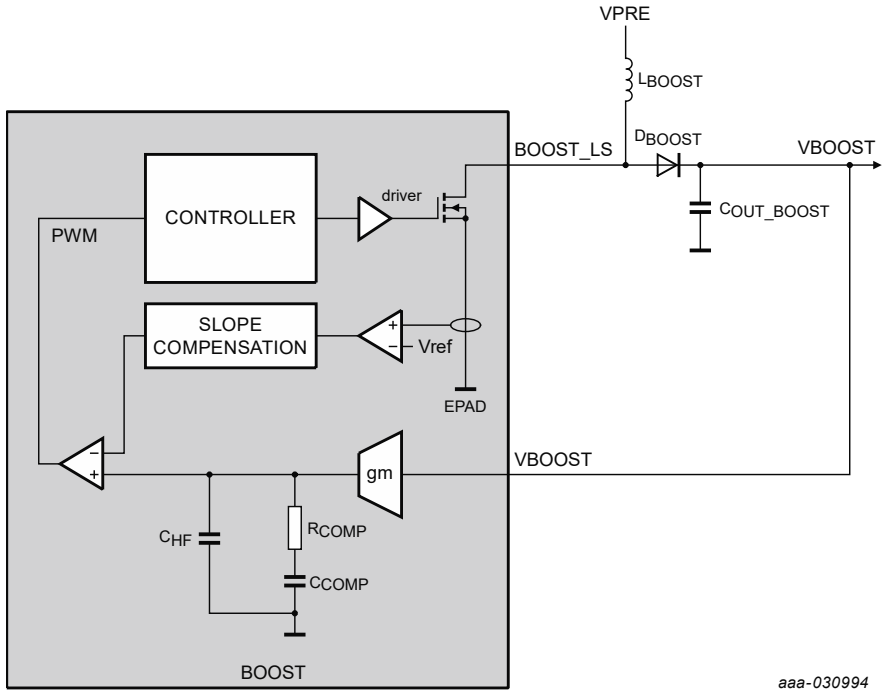


Figure 17. BOOST schematic

NXP recommends selecting a Schottky diode for D_{BOOST} to limit the impact on the SMPS efficiency.

21.3 Compensation network and stability

The internal compensation network, made with R_{COMP}, C_{COMP} and C_{HF} is optimized for best compromise between stability and transient response with R_{COMP} = 750 kΩ, C_{COMP} = 125 pF and C_{HF} = 2.0 pF.

Use case with V_{BOOST} = 5.74 V, L_{VBOOST} = 4.7 µH, F_{BOOST_SW} = 2.22 MHz, C_{OUT_BOOST} = 22 µF

Use case stability verification:

- Phase margin target PM > 45° and gain margin target GM > 6 dB.

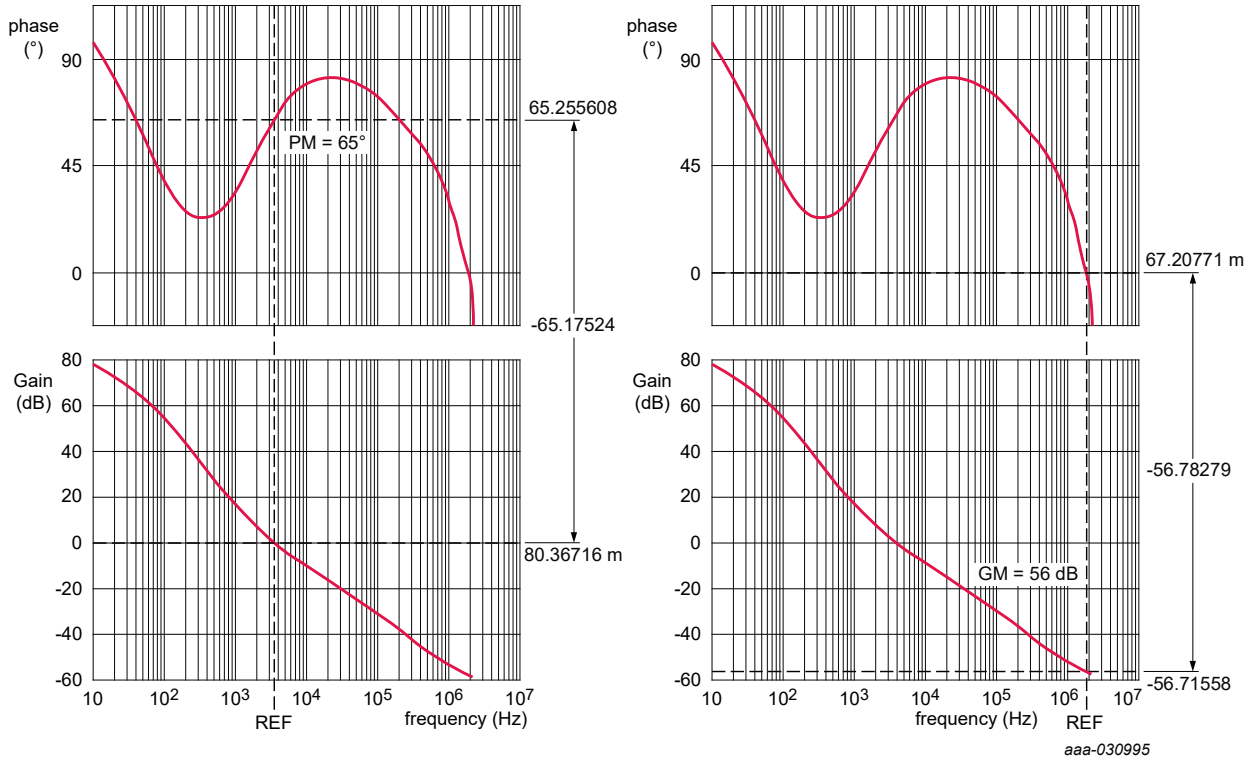


Figure 18. Phase and gain margin simulation

Use case transient response verification:

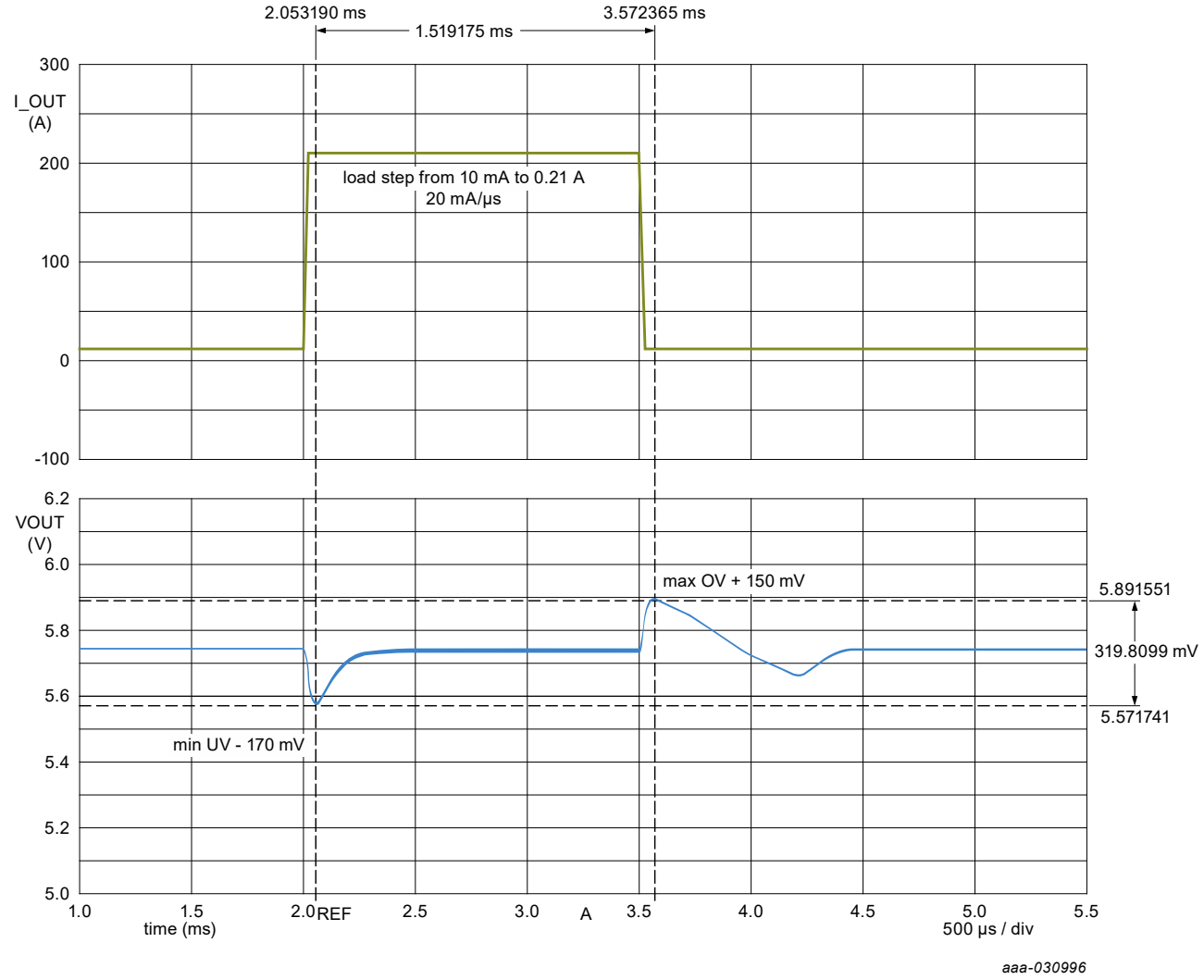


Figure 19. Transient response simulation

21.4 Electrical characteristics

Table 81. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VBOOST					
V_{BOOST}	Output voltage (OTP_VBSTV[3:0] bits)	5.57	5.74	5.91	V
		4.85	5.0	5.15	V
$V_{BOOST\_SOFT\_START}$	Output voltage from 10 % to 90 %	—	500	—	µs
	Digital DAC soft start completion	—	—	825	µs
$V_{BOOST\_STARTUP}$	Overshoot at startup	—	—	3	%
V_{BOOST_UVH}	Undervoltage threshold high	3.3	—	3.7	V
T_{BOOST_UVH}	V_{BOOST_UVH} filtering time	6	10	15	µs
V_{BOOST_OV}	Overvoltage protection threshold	7.4	—	7.9	V
F_{BOOST_SW}	Switching frequency range	2.1	2.22	2.35	MHz
L_{BOOST}	Typical inductor value	2.2	4.7	6.8	µH
C_{OUT_BOOST}	Effective output capacitor	20	—	60	µF
$V_{BOOST\_LOAD\_REG}$	Transient load regulation (C_{OUT_BOOST} = 22 µF, from 10 mA to 400 mA, di/dt = 200 mA/µs)	—	—	750	mV
$V_{BOOST\_LOAD\_REG}$	Transient load regulation (C_{OUT_BOOST} = 22 µF, from 1.0 mA to 20 mA, di/dt = 200 mA/µs)	—	—	500	mV
I_{LIM_BOOST}	Inductor peak current limitation range (OTP_VBSTILIM[1:0] bits)	1.5	2	2.75	A
$T_{BOOST\_ON\_MIN}$	LS minimum ON time (OTP_VBSTTONTIME[1:0] bits)	40	60	90	ns
		30	50	80	ns
R_{BOOST_RON}	LS NMOS RDSon	—	150	280	mΩ
T_{BOOST_SR}	Switching output slew rate (OTP_VBSTSR[1:0] bits by default + VBSTSR[1:0] bits by SPI)	—	500	1500	V/µs
		—	300	750	V/µs
$gmEA_{BOOST}$	Error amplifier transconductance	3.5	7	9	µs
V_{BOOST_SLOPE}	Slope compensation (OTP_VBSTSC[3:0] bits)	40	79	110	mV/µs
		70	125	190	mV/µs
		90	160	230	mV/µs
R_{COMP}	Compensation network resistor	500	750	1200	kΩ
		250	500	1000	kΩ
C_{COMP}	Compensation network capacitor	90	125	175	pF
TSD_{BOOST}	Thermal shutdown threshold	160	—	—	°C
TSD_{BOOST_HYST}	Thermal shutdown threshold hysteresis	—	9	—	°C
T_{BOOST_TSD}	Thermal shutdown filtering time	3	5	8	µs

21.5 VBOOST not populated

It is possible to not use the VBOOST when VPRE is configured at 4.1 V or 5.0 V. In this case, the external VBOOST components can be unpopulated to optimize the bill of material. The OTP_BOOSTEN bit shall be programmed to 0 and VBOOST pin must be connected to VPRE. BOOST_LS pin must be left open.

VBOOST must be used when VPRE is configured at 3.3 V or 3.8 V to supply VBOS.

22 Low-voltage buck: BUCK1 and BUCK2

22.1 Functional description

BUCK1 and BUCK2 blocks are low-voltage, synchronous, valley current mode buck converters with integrated HS PMOS and LS NMOS. BUCK1 and BUCK2 work in force PWM and the output voltage is configurable by OTP from 0.8 V to 1.8 V, the switching frequency is 2.22 MHz and the output current is limited to 3.6 A peak. The input of these blocks must be connected to the output of VPRE. The stability is ensured by an internal Type 2 compensation network with slope compensation.

BUCK1 and BUCK2 switching frequency is derived from the internal oscillator.

BUCK2 is part number dependent according to OTP_BUCK2EN bit. BUCK1 and BUCK2 can work independently or in dual phase mode to double the output current capability. When BUCK1 and BUCK2 are used in dual phase, they must have the same output voltage configuration. Any action like TSD, OV, disable by SPI, on BUCK1 affects BUCK2 and vice versa.

An overcurrent detection and a thermal shutdown are implemented on BUCK1 and BUCK2 to protect the internal MOSFETs. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition.

.The ramp up and ramp down of BUCK1 and BUCK2 when they are enabled and disabled is configurable with OTP_DVS_BUCK12[1:0] bits to accommodate multiple MCU soft start requirements. Static Voltage Scaling (SVS) feature is available to decrease the output voltage after power up during INIT_FS.Programmable phase shift control is implemented, see Section 25 "Clock management".

22.2 Application schematic: single phase mode

In this configuration, BUCK1 and BUCK2 are configured as independent outputs, working independently. Each output is configured and controlled independently by SPI.

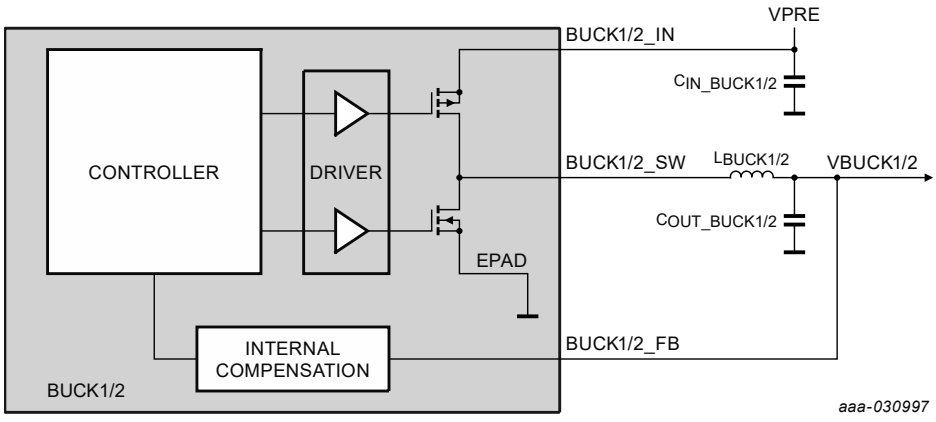


Figure 20. BUCK1/2 standalone schematic

22.3 Application schematic: dual phase mode

In this configuration, BUCK1 and BUCK2 are configured in dual phase mode to double the output current capability. The dual phase mode is enabled with OTP_VB12MULTIPH bit. The PCB layout of BUCK1 phase and BUCK2 must be symmetric for optimum EMC performance.

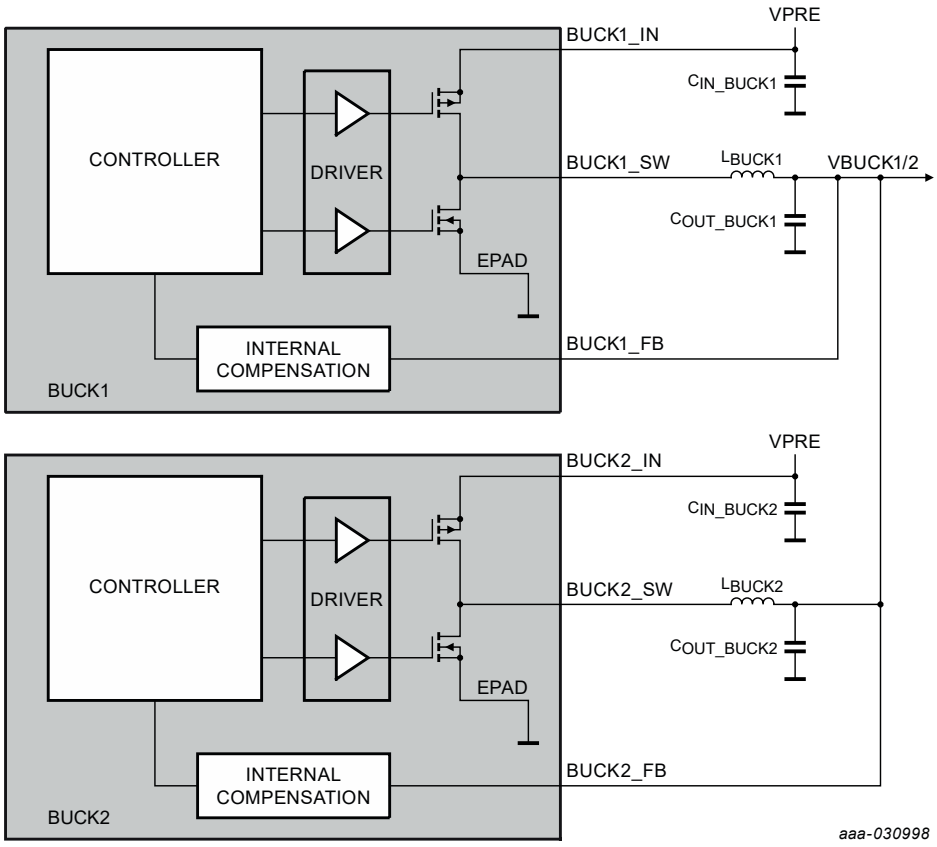


Figure 21. BUCK1/2 multiphase schematic

22.4 Compensation network and stability

The internal compensation network ensures the stability and the transient response performance of the buck converter. The error amplifier gain is configurable with OTP_VBxGMCOMP[2:0] bits for each BUCK 1 and BUCK2 regulators. NXP recommends using the default value that covers most of the use cases.

Decreasing the gain reduces the regulation bandwidth and increase the phase and gain margin but transient performance is degraded. Increasing the gain enlarges the regulation bandwidth and improves the transient performance but the phase and gain margin is degraded.

OTP_VBxINDOPT[1:0] scales the slope compensation and the zero cross detection according to the inductor value. 1.0 µH is the recommended inductor value for BUCK1 and BUCK2.

Use case with V_{PRE} = 3.3 V, V_{BUCK1} = 1.0 V, L_{VBUCK1} = 1.0 µH, V_{BUCK1_SW} = 2.22 MHz, C_{OUT_BUCK1} = 44 µF, default Err Amp gain

Use case stability verification:

- Phase margin target PM > 45° and gain margin target GM > 6 dB.

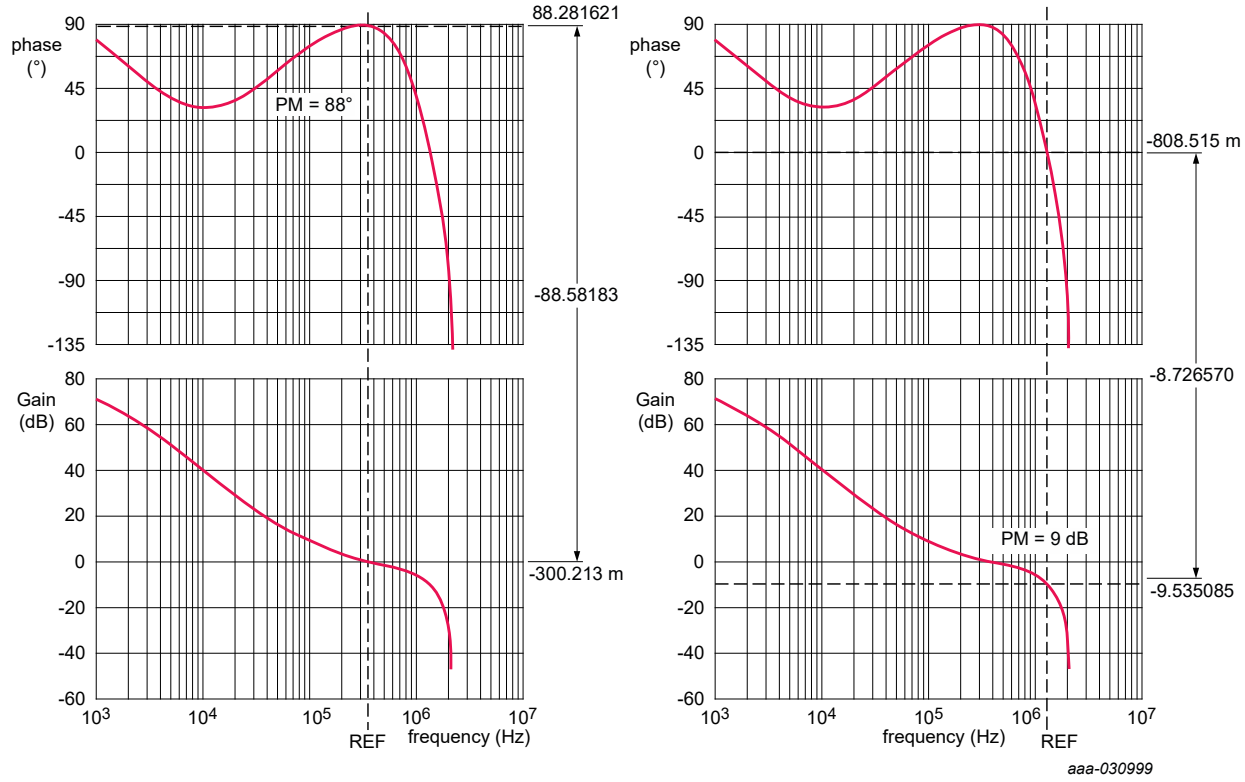


Figure 22. Phase and gain margin simulation

Use case transient response verification:

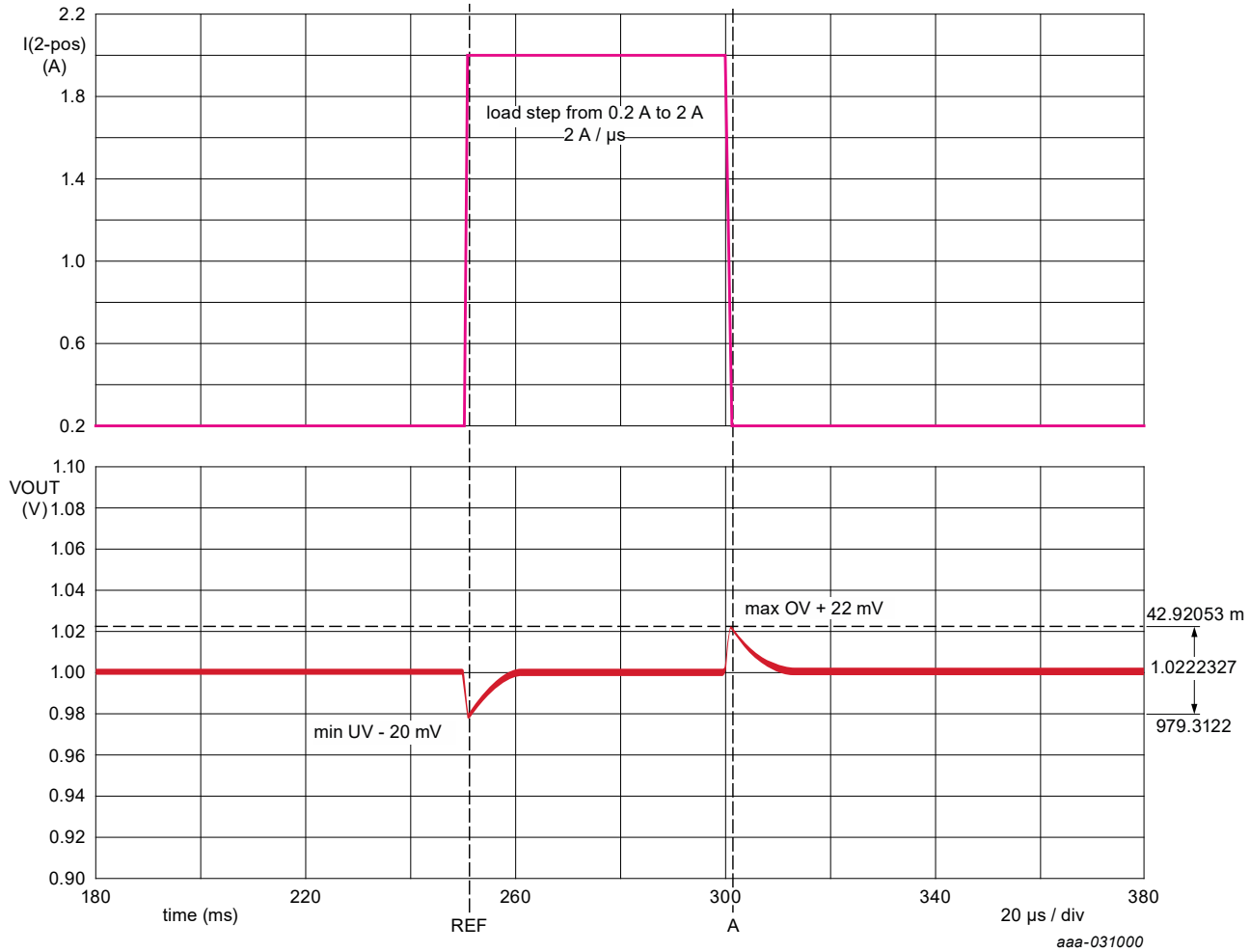


Figure 23. Transient response simulation

22.5 Electrical characteristics

Table 82. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
BUCK1 and BUCK2					
V_{BUCK12_IN}	Input voltage range	2.5	—	5.5	V
V_{BUCK12}	Output voltage (OTP_VB1V[7:0] and OTP_VB2V[7:0] bits) 0.8 V, 0.825 V, 0.9 V, 0.95 V, 1.0 V, 1.025 V, 1.03125 V, 1.075 V, 1.1 V, 1.1375 V, 1.2 V, 1.25 V, 1.3 V, 1.35 V, 1.4 V, 1.5 V, 1.8 V	0.8	—	1.8	V
I_{BUCK12}	DC output current capability (one phase)	—	—	2.5	A
V_{BUCK12_ACC}	Output voltage accuracy (I_{OUT} < 2.5 A)	−2	—	+2	%
F_{BUCK12_SW}	Switching frequency range	2.1	2.22	2.35	MHz
L_{BUCK12}	Typical inductor value (OTP_VB1INDOPT[1:0] and OTP_VB2INDOPT[1:0] bits)	0.47	1.0	1.5	µH

Table 82. Electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
C_{OUT_BUCK12}	Effective output capacitor	40	—	160	µF
	Output decoupling capacitor	—	0.1	—	µF
C_{IN_BUCK12}	Effective input capacitor (close to BUCK1_IN and BUCK2_IN pins)	4.7	—	—	µF
	Input decoupling capacitor (close to BUCK1_IN and BUCK2_IN pins)	—	0.1	—	µF
V_{BUCK12_TLR}	Transient load regulation for V_{BUCK12} < 1.2 V (Cout = 40 µF, from 200 mA to 1.0 A, di/dt = 2.0 A/µs for mono phase configuration) (Cout = 40 µF, from 400 mA to 2.0 A, di/dt = 4.0 A/µs for dual phase configuration)	−25	—	+25	mV
V_{BUCK12_TLR}	Transient load regulation for V_{BUCK12} >1.2 V (Cout = 40 µF, from 200 mA to 1.0 A, di/dt = 2.0 A/µs for mono phase configuration) (Cout = 40 µF, from 400 mA to 2.0 A, di/dt = 4.0 A/µs for dual phase configuration)	−3	—	+3	%
I_{LIM_BUCK12}	Inductor peak current limitation range for one phase (OTP_VB1SWILIM[1:0] and OTP_VB2 SWILIM[1:0] bits)	2.0	2.6	3.1	A
		3.6	4.5	5.45	A
$V_{BUCK12\_DVS\_UP}$ (for V_{BUCK12} up to 1.5 V)	Ramp up speed, OTP_DVS_BUCK12[1:0] = 00	5.86	7.81	9.77	mV/µs
	Ramp up speed, OTP_DVS_BUCK12[1:0] = 01	2.34	3.13	3.91	mV/µs
	Ramp up speed, OTP_DVS_BUCK12[1:0] = 10	1.95	2.60	3.26	mV/µs
	Ramp up speed, OTP_DVS_BUCK12[1:0] = 11	1.67	2.23	2.79	mV/µs
$V_{BUCK12\_DVS\_UP\_1p8}$ (for V_{BUCK12} = 1.8 V)	Ramp up speed, OTP_DVS_BUCK12[1:0] = 00	7.33	9.763	12.21	mV/µs
	Ramp up speed, OTP_DVS_BUCK12[1:0] = 01	2.93	3.91	4.89	mV/µs
	Ramp up speed, OTP_DVS_BUCK12[1:0] = 10	2.44	3.25	4.08	mV/µs
	Ramp up speed, OTP_DVS_BUCK12[1:0] = 11	2.09	2.79	3.49	mV/µs
$V_{BUCK12\_DVS\_DOWN}$(for V_{BUCK12} up to 1.5 V)	Ramp down speed, OTP_DVS_BUCK12[1:0] = 00	3.91	5.21	6.51	mV/µs
	Ramp down speed, OTP_DVS_BUCK12[1:0] = 01	2.34	3.13	3.91	mV/µs
	Ramp down speed, OTP_DVS_BUCK12[1:0] = 10	1.95	2.6	3.26	mV/µs
	Ramp down speed, OTP_DVS_BUCK12[1:0] = 11	1.67	2.23	2.79	mV/µs
$V_{BUCK12\_DVS\_DOWN\_1p8}$ (for V_{BUCK12} = 1.8 V)	Ramp down speed, OTP_DVS_BUCK12[1:0] = 00	4.89	6.51	8.14	mV/µs
	Ramp down speed, OTP_DVS_BUCK12[1:0] = 01	2.93	3.91	3.89	mV/µs
	Ramp down speed, OTP_DVS_BUCK12[1:0] = 10	2.44	3.25	4.08	mV/µs
	Ramp down speed, OTP_DVS_BUCK12[1:0] = 11	2.09	2.79	3.49	mV/µs
$V_{BUCK12\_SOFT\_START}$	$V_{BUCK12\_SOFT\_START}$ = V_{BUCK12} / $V_{BUCK12\_DVS\_UP}$ Soft start for V_{BUCK12} = 1.2 V and OTP_DVS_BUCK12[1:0] = 00	122.9	153.6	204.8	µs
	Soft start for V_{BUCK12} = 1.2 V and OTP_DVS_BUCK12[1:0] = 11 To be recalculated for different V_{BUCK12} and different $V_{BUCK12\_DVS\_UP}$	430.1	537.6	716.8	µs
$V_{BUCK12\_STARTUP}$	Overshoot at startup	—	—	50	mV
$T_{BUCK12\_OFF\_MIN}$	HS minimum OFF time	9	30	54	ns

Table 82. Electrical characteristics...*continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
T_{BUCK12_DT}	Dead time to avoid cross conduction	0.01	3	20	ns
$R_{BUCK12\_HS\_RON}$	HS PMOS RDSon	—	—	135	mΩ
$R_{BUCK12\_LS\_RON}$	LS NMOS RDSon	—	—	80	mΩ
R_{BUCK12_DISch}	Discharge resistance (when BUCK1,2 is disabled)	250	500	1000	Ω
TSD_{BUCK12}	Thermal shutdown threshold	160	—	—	°C
TSD_{BUCK12_HYST}	Thermal shutdown threshold hysteresis	—	9	—	°C
T_{BUCK12_TSD}	Thermal shutdown filtering time	3	5	8	µs

22.6 BUCK1 and BUCK2 efficiency

BUCK1 and BUCK2 efficiency versus current load is given for information based on external component criteria provided and VPRE voltage 4.1 V. If the conditions change, it has to be recalculated with the FS85_PDTCAL tool. The real efficiency has to be verified by measurement at the application level.

Ext. C and L		
Cin	60	µF
ESR Cin	10	mΩ
Cout	44	µF
ESR Cout	10	mΩ
L coil	1	µH
DCR coil	20	mΩ
Int. MOSFET's		
HS_Rdson	135	MΩ
QHS	0.5	nC
THS_sw	3	ns
GHS_drive	5	V
LS_Rdson	80	MΩ
QLS	0.5	nC
TLS_sw	3	ns
GLS_drive	5	V

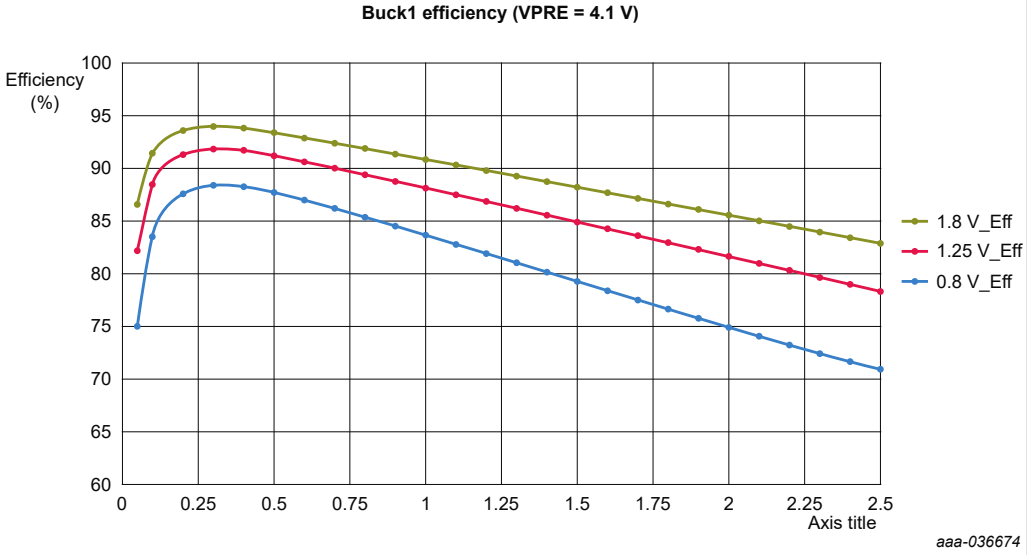


Figure 24. BUCK1 and BUCK2 theoretical efficiency

23 Low-voltage buck: BUCK3

23.1 Functional description

BUCK3 block is a low-voltage, synchronous, peak current mode buck converter with integrated HS PMOS and LS NMOS. BUCK3 works in force PWM and the output voltage is configurable by OTP from 1.0 V to 3.3 V, the switching frequency is 2.22 MHz and the output current is limited to 3.6 A peak. The input of this block can be connected to the output of VPRE or VBOOST when VBOOST = 5.0 V only. The stability is ensured by an internal Type 2 compensation network with slope compensation.

BUCK3 switching frequency is derived from the internal oscillator.

An overcurrent detection and a thermal shutdown are implemented on BUCK3 to protect the internal MOSFETs. The overcurrent induces a duty cycle reduction that could lead to the output voltage gradually dropping, causing an undervoltage condition.

BUCK3 is part number dependent according to OTP_BUCK3EN bit. BUCK3_INQ pin, used to bias internal BUCK3 driver, must be connected to BUCK3_IN pin close to the device pins. The ramp up and ramp down of BUCK3 when it is enabled and disabled is configurable with OTP_DVS_BUCK3[1:0] bits to accommodate multiple MCU soft start requirements.

Programmable phase shift control is implemented, see Section 25 "Clock management".

23.2 Application schematic

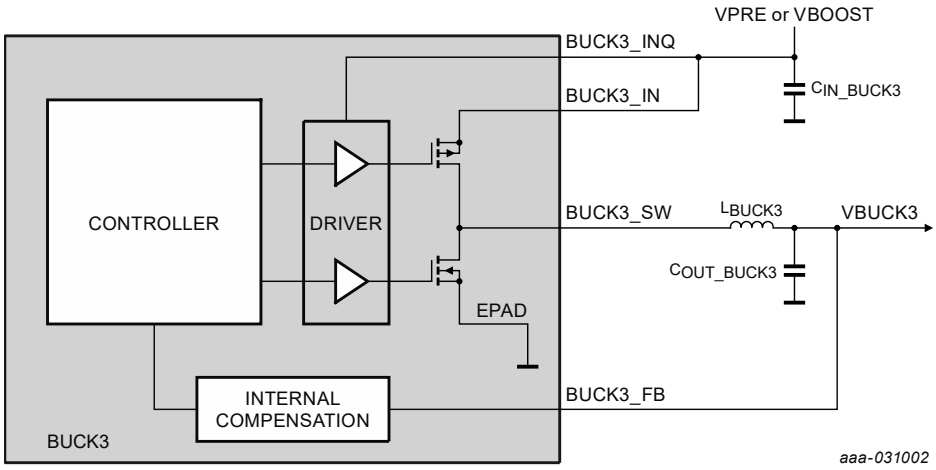


Figure 25. BUCK3 schematic

23.3 Compensation network and stability

The internal compensation network ensures the stability and the transient response performance of the buck converter. OTP_VB3INDOPT[1:0] scales the slope compensation and the zero cross detection according to inductor value. 1.0 µH is the recommended inductor value for BUCK3.

Use case with V_{PRE} = 3.3 V, V_{BUCK3} = 2.3 V, L_{VBUCK3} = 1.0 µH, F_{BUCK3_SW} = 2.22 MHz, C_{OUT_BUCK3} = 44 µF

Use case stability verification:

- Phase margin target PM > 45° and gain margin target GM > 6 dB.

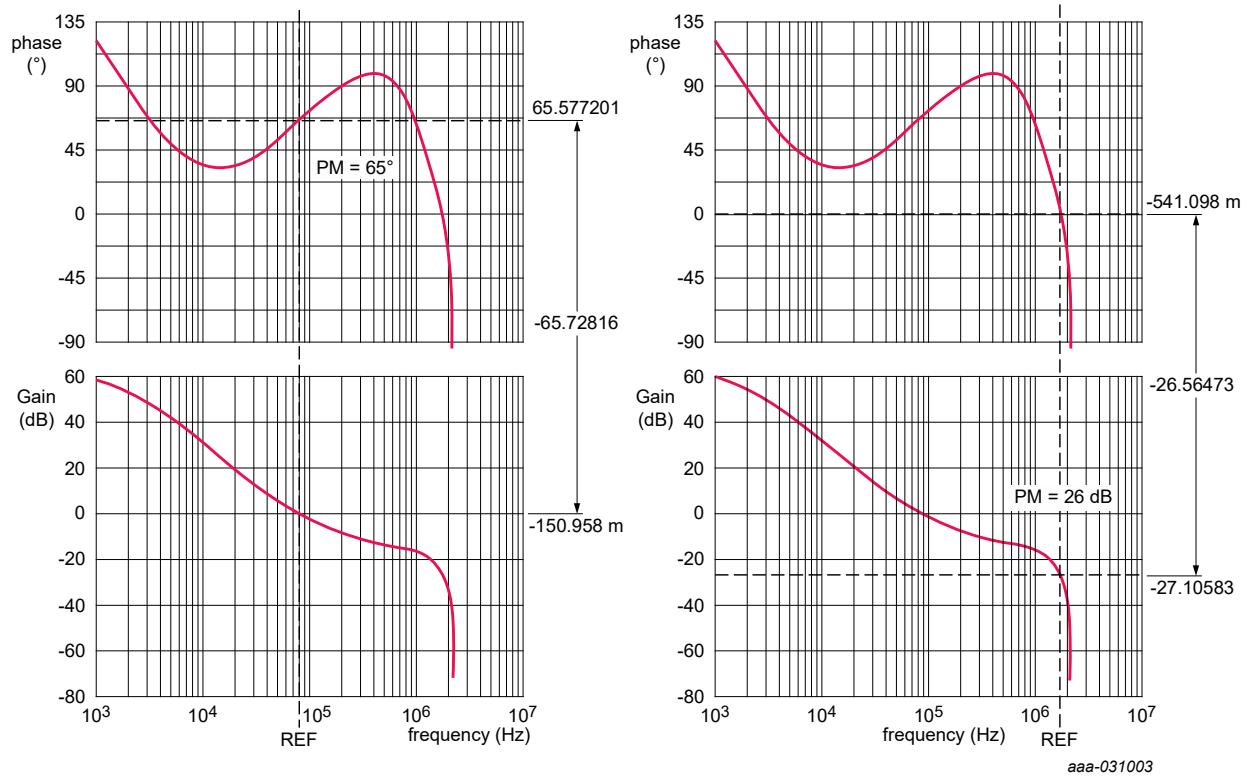


Figure 26. Phase and gain margin simulation

Use case transient response verification:

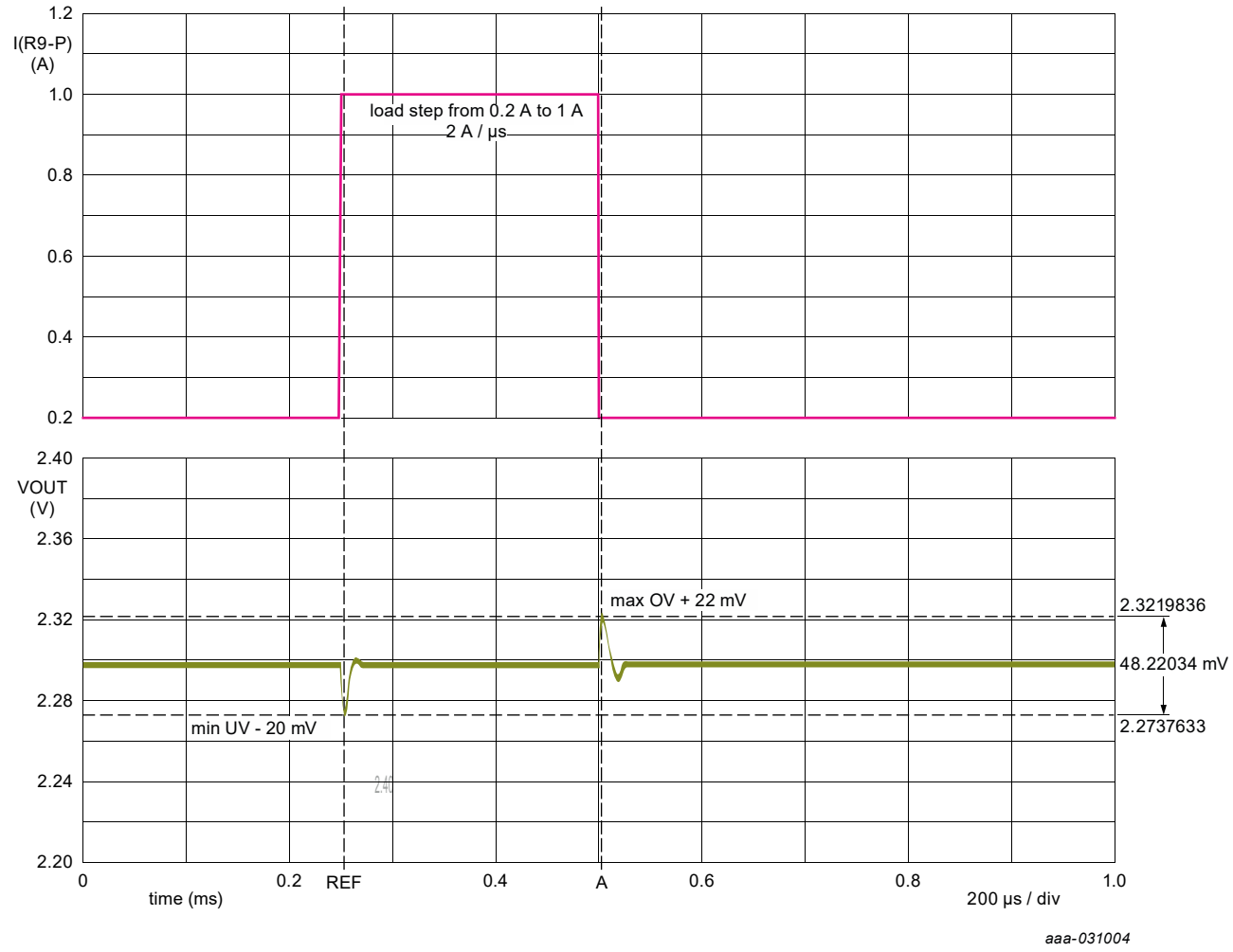


Figure 27. Transient response simulation

23.4 Electrical characteristics

Table 83. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
BUCK3					
V_{BUCK3_IN}	Input voltage range	2.5	—	5.5	V
V_{BUCK3}	Output voltage (OTP_VB3V[4:0] bits) 1.0 V, 1.1 V, 1.2 V, 1.25 V, 1.3 V, 1.35 V, 1.5 V, 1.6 V, 1.8 V, 2.3 V, 2.5 V, 2.8 V, 3.3 V	1.0	—	3.3	V
I_{BUCK12}	DC output current capability	—	2.5	—	A
V_{BUCK3_ACC}	Output voltage accuracy (Iout < 2.5 A)	−2	—	+2	%
F_{BUCK3_SW}	Switching frequency range	2.1	2.22	2.35	MHz
L_{BUCK3}	Typical inductor value (OTP_VB3INDOPT[1:0] bits)	0.47	1.0	1.5	µH
C_{OUT_BUCK3}	Effective output capacitor	40	—	120	µF

Table 83. Electrical characteristics*...continued*

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
	Output decoupling capacitor	—	0.1	—	µF
C_{IN_BUCK3}	Effective input capacitor (close to BUCK3_IN pin)	4.7	—	—	µF
	Input decoupling capacitor (close to BUCK3_IN pin)	—	0.1	—	µF
V_{BUCK3_TLR}	Transient load regulation (Cout = 40 µF, from 200 mA to 1.0 A, di/dt = 2.0 A/µs)	−50	—	+50	mV
I_{LIM_BUCK3}	Inductor peak current limitation range (OTP_VB3 SWILIM[1:0] bits)	2.0	2.6	3.1	A
		3.6	4.5	5.45	A
$T_{BUCK3\_ON\_MIN}$	HS minimum ON time	5	50	80	ns
$V_{BUCK3\_DVS\_UP\_DOWN}$	Ramp up and ramp down speed, OTP_DVS_ BUCK3[1:0] = 00	7.81	10.42	13.02	mV/µs
	Ramp up and ramp down speed, OTP_DVS_ BUCK3[1:0] = 01	2.6	3.47	4.34	mV/µs
	Ramp up and ramp down speed, OTP_DVS_ BUCK3[1:0] = 10	1.95	2.6	3.26	mV/µs
	Ramp up and ramp down speed, OTP_DVS_ BUCK3[1:0] = 11	1.56	2.08	2.60	mV/µs
BUCK3_SOFT_START	$V_{BUCK12\_SOFT\_START}$ = V_{BUCK12} / $V_{BUCK12\_DVS\_UP}$ Soft start for V_{BUCK3} = 1.8 V and OTP_DVS_ BUCK3[1:0] = 00	84.8	105.6	140.8	µs
	Soft start for V_{BUCK3} = 1.8 V and OTP_DVS_ BUCK3[1:0] = 11 To be recalculated for different V_{BUCK3} and different $V_{BUCK3\_DVS\_UP\_DOWN}$	422.4	528	704	µs
$V_{BUCK3\_STARTUP}$	Overshoot at startup	—	—	50	mV
T_{BUCK3_DT}	Dead time to avoid cross conduction	0.01	3	20	ns
$R_{BUCK3\_HS\_RON}$	HS PMOS RDSon	—	—	135	mΩ
$R_{BUCK3\_LS\_RON}$	LS NMOS RDSon	—	—	80	mΩ
R_{BUCK3_DISCH}	Discharge resistance (when BUCK3 is disabled)	250	500	1000	Ω
TSD_{BUCK3}	Thermal shutdown threshold	160	—	—	°C
TSD_{BUCK3_HYST}	Thermal shutdown threshold hysteresis	—	9	—	°C
T_{BUCK3_TSD}	Thermal shutdown filtering time	3	5	8	µs

23.5 BUCK3 efficiency

BUCK3 efficiency versus current load is given for information based on external component criteria provided and VPRE voltage 4.1 V. If the conditions change, it has to be recalculated with the FS85_PDTCAL tool. The real efficiency has to be verified by measurement at the application level.

Ext. C and L		
Cin	60	µF
ESR Cin	10	mΩ
Cout	44	µF
ESR Cout	10	mΩ
L coil	1	µH
DCR coil	20	mΩ
Int. MOSFETs		
HS_Rdson	135	mΩ
QHS	0.5	nC
THS_sw	3	ns
GHS_drive	5	V
LS_Rdson	80	mΩ
QLS	0.5	nC
TLS_sw	3	ns
GLS_drive	5	V

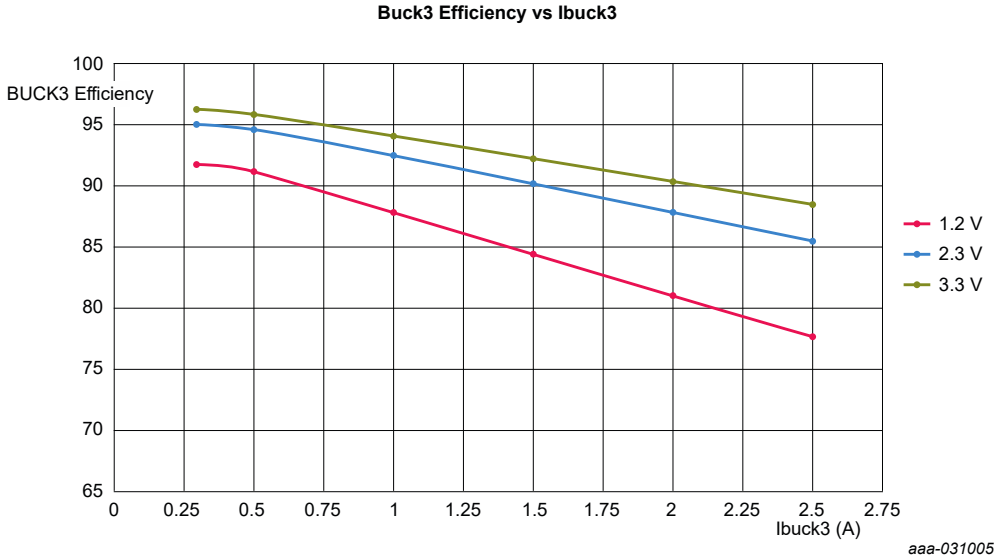


Figure 28. BUCK3 theoretical efficiency

24 Linear voltage regulator: LDO1, LDO2

24.1 Functional description

LDO1 and LDO2 blocks are two linear voltage regulators. The output voltage is configurable by OTP from 1.1 V to 5.0 V. A minimum voltage drop is required depending on the output current capability (0.5 V for 150 mA and 1.0 V for 400 mA). The LDO current capability is linear with the voltage drop and can be estimated to I(mA) = 500 x V_{LDO12_DROP} -100 for intermediate voltage drop between 0.5 V and 1.0 V.

LDO1 input supply is externally connected to VPRE, VBOOST, or another supply. LDO2 input supply is internally connected to the output of VBOOST. An overcurrent detection and a thermal shutdown are implemented on LDO1 and LDO2 to protect the internal pass device.

24.2 Application schematics

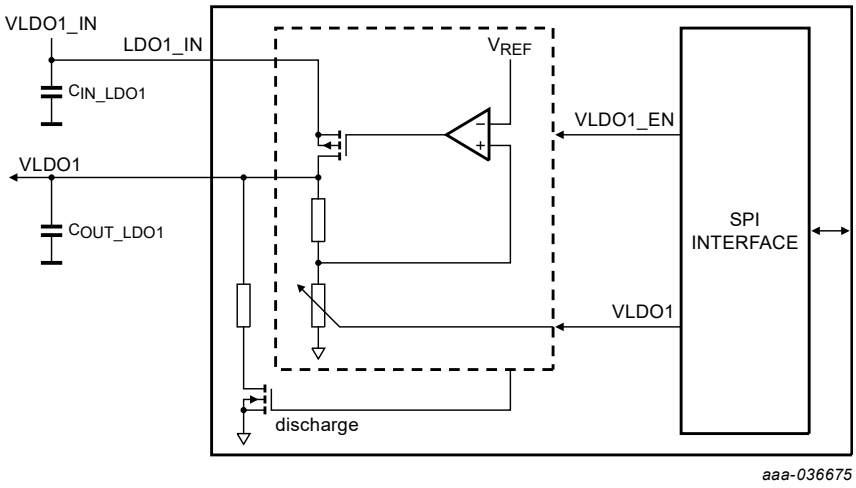


Figure 29. LDO1 block diagram

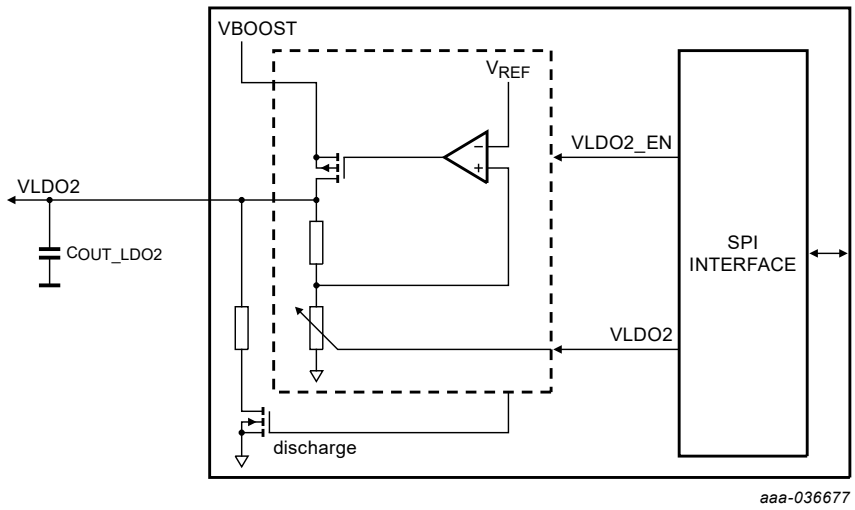


Figure 30. LDO2 block diagram

24.3 Electrical characteristics

Table 84. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
LDO1 and LDO2					
V_{LDO12_IN}	Input voltage range	2.5	—	6.5	V
V_{LDO12}	Output voltage (OTP_VLDO1V[2:0] and OTP_LDO2V[2:0] bits) 1.1 V, 1.2 V, 1.6 V, 1.8 V, 2.5 V, 2.8 V, 3.3 V, 5.0 V	1.1	—	5.0	V
$V_{LDO12\_ACC\_150}$	Output voltage accuracy, 150 mA current capability	−2	—	+2	%
$V_{LDO12\_ACC\_400}$	Output voltage accuracy, 400 mA current capability	−3	—	+3	%
$V_{LDO12\_DROP\_150}$	Minimum voltage drop for 150 mA current capability	0.5	—	—	V
$V_{LDO12\_DROP\_400}$	Minimum voltage drop for 400 mA current capability	1.0	—	—	V
C_{IN_LDO1}	Input capacitor (close to LDO1_IN pin)	1.0	—	—	µF
$C_{OUT\_LDO12\_150}$	Output capacitor, 150 mA current capability	4.7	—	10	µF
$C_{OUT\_LDO12\_400}$	Output capacitor, 400 mA current capability	6.8	—	10	µF
C_{OUT_LDO12}	Output decoupling capacitor	0.1	—	—	µF
$V_{LDO12\_LTR\_150}$	Transient load regulation (from 10 mA to 150 mA in 2.0 µs)	−4	—	+4	%
$V_{LDO12\_LTR\_400}$	Transient load regulation (from 10 mA to 400 mA in 4.0 µs)	−5	—	+5	%
V_{LDO12_LR}	Line regulation	—	—	0.5	%
$V_{LDO12\_ILIM\_150}$	Current limitation, 150 mA current capability (OTP_LDO1ILIM and OTP_LDO2ILIM bits)	200	280	500	mA
$V_{LDO12\_ILIM\_400}$	Current limitation, 400 mA current capability (OTP_LDO1ILIM and OTP_LDO2ILIM bits)	430	560	800	mA
$V_{LDO12\_SOFT\_START}$	Soft start (enable to 90 %)	—	1.0	1.3	ms
$V_{LDO12\_STARTUP}$	Overshoot at startup	—	—	2	%
R_{LDO12_DISCH}	Discharge resistance (when LDO1,2 is disabled)	10	20	60	Ω
TSD_{LDO12}	Thermal shutdown threshold	160	—	—	°C
TSD_{LDO12_HYST}	Thermal shutdown threshold hysteresis	—	9	—	°C
T_{LDO12_TSD}	Thermal shutdown filtering time	3	5	8	µs

25 Clock management

25.1 Clock description

The clock management block is made of the Internal oscillator, the Phase Locked Loop (PLL) and multiple dividers. This block manages the clock generation for the internal digital state machines, the switching regulators and the external clock synchronization.

The internal oscillator is running at 20 MHz by default after start-up. The frequency is programmable by SPI and a spread spectrum feature can be activated by SPI to reduce the emission of the oscillator fundamental frequency.

VPRE switching frequency is coming from CLK2 (455 kHz) or CLK1 (2.22 MHz). BUCK1,2,3 and BOOST switching frequency is coming from CLK1 (2.22 MHz).

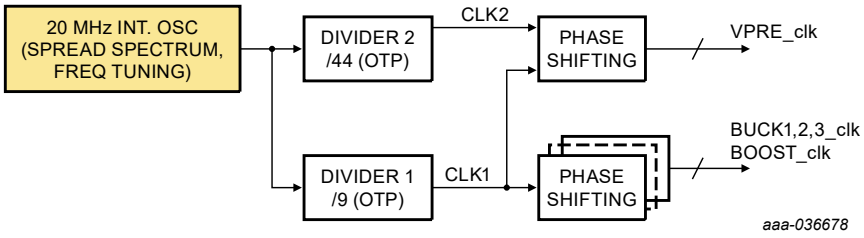


Figure 31. Clock management block diagram

25.2 Phase shifting

The clocks of the switching regulators (VPRE_clk, BOOST_clk, BUCK1_clk, BUCK2_clk and BUCK3_clk) can be delayed in order to avoid all the regulators to turn ON at the same time to reduce peak current and improve EMC performance.

Each clock of each regulator can be shifted from 1 to 7 clock cycles of CLK running at 20 MHz what corresponds to 50 ns. The phase shift configuration is done by OTP configuration using OTP_VPRE_ph[2:0], OTP_VBST_ph[2:0], OTP_BUCK1_ph[2:0], OTP_BUCK2_ph[2:0] and OTP_BUCK3_ph[2:0].

VPRE and BUCK3 have a peak current detection architecture. The PWM synchronizes the turn ON of the high-side switch. BUCK1 and BUCK2 have a valley current detection architecture. The PWM synchronizes the turn ON of the low-side switch.

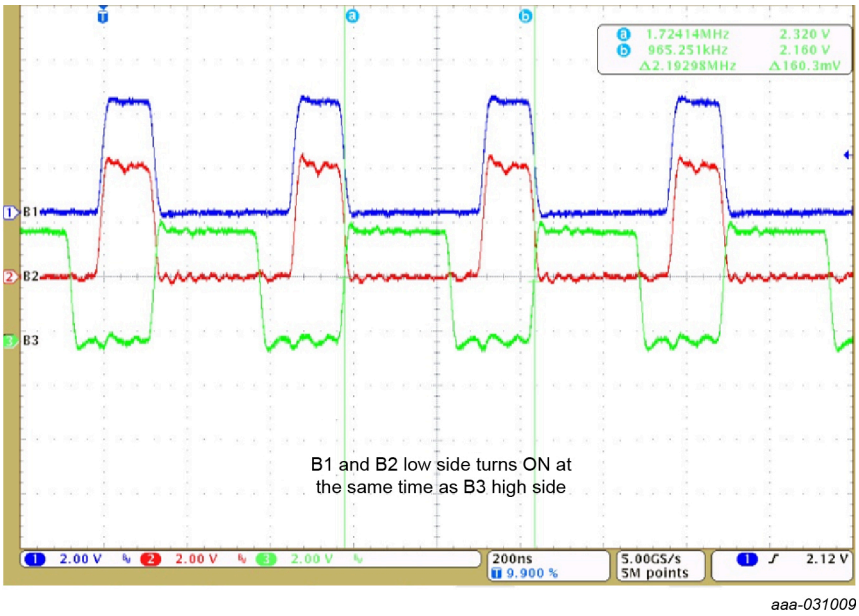


Figure 32. BUCK1,2,3_clk = 2.22 MHz without clock phase shifting

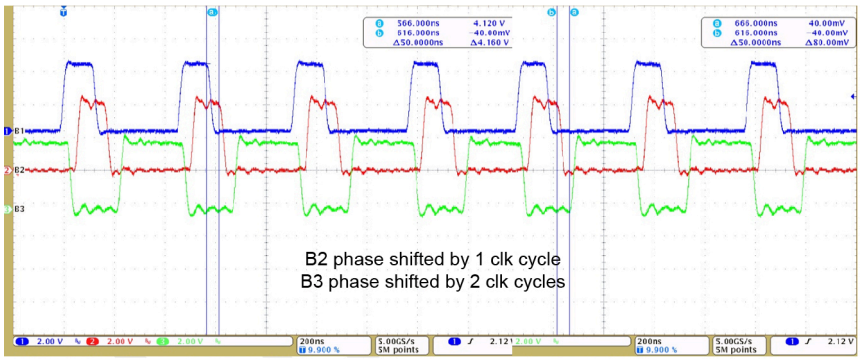


Figure 33. BUCK1,2,3_clk = 2.22 MHz with clock phase shifting

25.3 Manual frequency tuning

The internal oscillator frequency, 20 MHz by default, can be programmed from 16 MHz to 24 MHz with 1.0 MHz frequency step by SPI. The oscillator functionality is guaranteed for frequency increment of one step at a time in either direction, with a minimum of 10 µs between two steps. For any unused code of the CLK_TUNE [3:0] bits, the internal oscillator is set at the default 20 MHz frequency.

To change the internal oscillator frequency from 20 MHz to 24 MHz, four SPI commands are required with 10 µs wait time between each command (21 MHz – wait 10 µs – 22 MHz – wait 10 µs – 23 MHz – wait 10 µs – 24 MHz). To change the internal oscillator frequency from 24 MHz to 16 MHz, eight SPI commands are required with 10 µs wait time between each command (23 MHz – wait 10 µs – 22 MHz – wait 10 µs – 21 MHz – wait 10 µs – 20 MHz – wait 10 µs – 19 MHz – wait 10 µs – 18 MHz – wait 10 µs – 17 MHz – wait 10 µs – 16 MHz).

Table 85. Manual frequency tuning configuration

CLK_TUNE [3:0]	Oscillator frequency [MHz]
0000 (default)	20
0001	21
0010	22
0011	23
0100	24
1001	16
1010	17
1011	18
1100	19
Reset condition	POR

25.4 Spread spectrum

The internal oscillator can be modulated with a triangular carrier frequency of 23 kHz or 94 kHz with ±5 % deviation range around the oscillator frequency. The spread spectrum feature can be activated by SPI with the MOD_EN bit and the carrier frequency can be selected by SPI with the MOD_CONF bit. By default, the spread spectrum is disabled. The spread spectrum and the manual frequency tuning functions cannot be used at the same time.

The main purpose of the spread spectrum is to improve the EMC performance by spreading the energy of the internal oscillator and VPRE frequency on VBAT frequency spectrum. NXP recommends selecting a 23 kHz carrier frequency when VPRE is configured at 455 kHz and 94 kHz when VPRE is configured at 2.2 MHz for the best performance.

25.5 Electrical characteristics

Table 86. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
20 MHz internal oscillator					
$F_{20\ MHz}$	Oscillator nominal frequency (programmable)	—	20	—	MHz
$F_{20\ MHz\_ACC}$	Oscillator accuracy	−6	—	+6	%
$T_{20\ MHz\_step}$	Oscillator frequency tuning step transition time	—	10	—	µs
Spread spectrum					
FSS_{MOD}	Spread spectrum frequency modulation (MOD_CONF SPI configuration)	—	23	—	kHz
		—	94	—	kHz
FSS_{RANGE}	Spread spectrum range (around the nominal frequency)	−5	—	+5	%

26 Analog multiplexer: AMUX

26.1 Functional description

The AMUX pin delivers 32 analog voltage channels to the MCU ADC input. The voltage channels delivered to AMUX pin can be selected by SPI. The maximum AMUX output voltage range is VDDIO. External Rs/Cout components are required for the buffer stability.

26.2 Block diagram

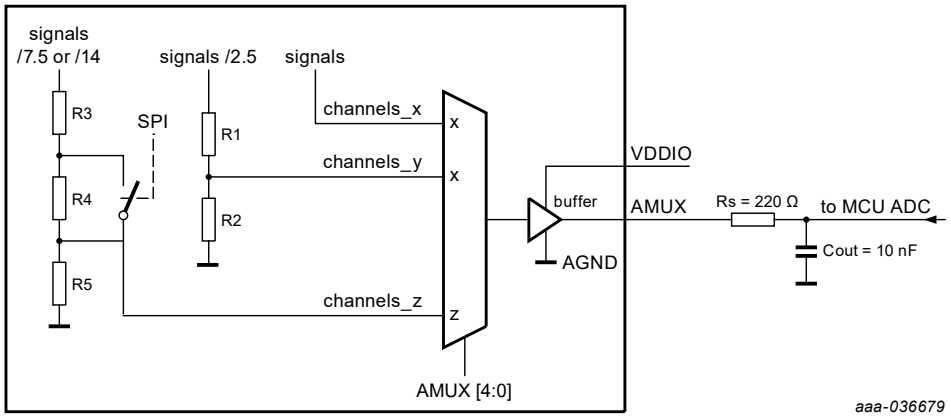


Figure 34. AMUX block diagram

26.3 AMUX channel selection

Table 87. AMUX output selection

AMUX[4:0]	Signal selection for AMUX output
00000 (default)	GND
00001	VDDIO voltage
00010	Temperature sensor: T(°C) = [(V_{AMUX} – V_{TEMP25}) / V_{TEMP_COEFF}] + 25
00011	Band gap main: 1.0 V ±1 %
00100	Band gap fail-safe: 1.0 V ±1 %
00101	VBUCK1 voltage
00110	VBUCK2 voltage
00111	VBUCK3 voltage divided by 2.5
01000	VPRE voltage divided by 2.5
01001	VBOOST voltage divided by 2.5
01010	VLDO1 voltage divided by 2.5
01011	VLDO2 voltage divided by 2.5
01100	VBOS voltage divided by 2.5
01101	Reserved
01110	VSUP1 voltage divided by 7.5 or 14 (SPI configuration with bit RATIO)
01111	WAKE1 voltage divided by 7.45 or 13.85 (SPI configuration with bit RATIO)
10000	WAKE2 voltage divided by 7.45 or 13.85 (SPI configuration with bit RATIO)
10001	Vana: internal main analog voltage supply: 1.6 V ±2 %
10010	Vdig: internal main digital voltage supply: 1.6 V ±2 %
10011	Vdig_fs: internal fail-safe digital voltage supply: 1.6 V ±2 %
10100	PSYNC voltage
Others	Same as default value (00000): GND

26.4 Electrical characteristics

Table 88. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
AMUX					
V_{AMUX_VDDIO}	Minimum VDDIO operating voltage for AMUX	3.2	—	—	V
V_{AMUX_IN}	Input voltage range for VSUP, WAKE1, WAKE2 • Ratio 7.45 and 7.5 • Ratio 13.85 and 14	 2.25 4.2	 — —	 22.5 42	V
I_{AMUX}	Output buffer current capability	—	—	2.0	mA
V_{AMUX_OFF}	Offset voltage (Iout = 1.0 mA)	−7	—	+7	mV
V_{AMUX_RATIO}	Ratio accuracy • Ratio 1 • Ratio 2.5 • Ratio 7.5 for VSUP1 • Ratio 7.45 for WAKE12 • Ratio 14 for VSUP1 • Ratio 13.85 for WAKE12	 −0.5 −1.5 −2.0 −2.0 −2.0 −2.0	 — — — — — —	 0.5 1.5 2.0 2.0 2.0 2.0	%
V_{AMUX_BRIDGE}	VSUP1, WAKE1, WAKE2 resistor bridge	0.75	1.5	3	MΩ
V_{TEMP25}	Temperature sensor voltage at 25 °C	2.01	2.07	2.12	V
V_{TEMP_COEFF}	Temperature sensor coefficient	−6.25	−6	−5.75	mV/°C
T_{AMUX_SET}	Settling time (from 10 % to 90 % of V_{DDIO}, Rs = 220 Ω, Cout = 10 nF)	—	—	10	µs
Rs	Output resistor	—	220	—	Ω
Cout	Output capacitor	—	10	—	nF

26.5 1.8 V MCU ADC input use case

FS6600 AMUX buffer is referenced to VDDIO, 3.3 V or 5.0 V. In case the MCU requires a 1.8 V ADC input voltage, an external resistor bridge R1/R2 can be added in between AMUX output and ADC input as shown in Figure 35. NXP recommends using a 0.1 % resistor accuracy to limit the conversion error impact.

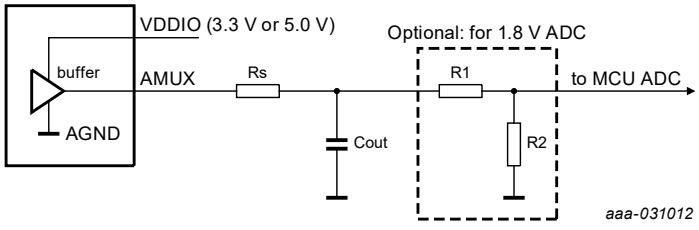


Figure 35. Optional 1.8 V ADC use case

The total resistor bridge value (R1 + R2) shall consume between min 10x ADC input current and max 1 mA at AMUX output to neither disturb the AMUX output buffer nor the ADC input. A good estimate is to calculate the resistor bridge value for 200 µA current consumption at VDDIO = 3.3 V.

Target R1 + R2 = 20 kΩ

For VDDIO = 3.3 V, R2 / (R1 + R2) = 1.8 / 3.3 = 0.545

After calculation, R2 = 11 kΩ and R1 = 9.3 kΩ

27 I/O interface pins

27.1 WAKE1, WAKE2

WAKE pins are used to manage the internal biasing of the device and the main state machine transitions.

- When WAKE1 or WAKE2 is > $WAKE12_{VIH}$, the internal biasing is started and the equivalent digital state is '1'
- When WAKE1 or WAKE2 is < $WAKE12_{VIL}$, the equivalent digital state is '0'
- When WAKE1 and WAKE2 are < $WAKE12_{AVIL}$, the internal biasing is stopped if the device was in Standby mode

WAKE1 and WAKE2 are level based wake-up input signals with analog measurement capability thru AMUX. WAKE1 can be for example connected to to a switched VBAT (KL15 line) and WAKE2 to the wake-up output of a CAN or FlexRay transceiver. When a WAKE pin is used as a global pin, a C - R - C protection is required (see Section 30 "Application information").

Table 89. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
WAKE1, WAKE2					
$WAKE12_{AVIL}$	Analog low input voltage threshold	1	—	—	V
$WAKE12_{VIL}$	Digital low input voltage threshold	2	—	—	V
$WAKE12_{VIH}$	Digital high input voltage threshold	—	—	4	V
I_{WAKE12}	Input current leakage at WAKE12 = 36 V	—	—	100	µA
	Input current leakage at WAKE12 = 60 V	—	—	300	µA
T_{WAKE12}	Filtering time	50	70	100	µs

27.2 INTB

INTB is an open-drain output pin with internal pull up to VDDIO. This pin generates a pulse when an internal interrupt occurs to inform the MCU. Each interrupt can be masked by setting the corresponding inhibit interrupt bit in M_INT_MASK registers.

Table 90. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
Interrupt pin					
$INTB_{PULL-up}$	Internal pull-up resistor to VDDIO	5.5	10	15	kΩ
$INTB_{VOL}$	Low output level threshold (I = 2.0 mA)	—	—	0.5	V
$INTB_{PULSE}$	Pulse duration (without manual frequency tuning)	90	100	110	µs

Table 91. List of interrupts from main logic

Interrupt main	Description
VSUP_UV7	VSUP undervoltage 7.0 V
VSUP_UVH	VSUP undervoltage high

Table 91. List of interrupts from main logic*...continued*

Interrupt main	Description
VSUP_UVL	VSUP undervoltage low
VBOS_UVH	VBOS undervoltage high
VPRE_OC	VPRE overcurrent
VPRE_FB_OV	VPRE overvoltage protection
VPRE_UVH	VPRE undervoltage high
BUCK1_TSD	BUCK1 overtemperature shutdown event
BUCK1_OC	BUCK1 overcurrent
BUCK2_TSD	BUCK2 over temperature shutdown event
BUCK2_OC	BUCK2 overcurrent
BUCK3_TSD	BUCK3 overtemperature shutdown event
BUCK3_OC	BUCK3 overcurrent
BOOST_TSD	BOOST overtemperature shutdown event
VBOOST_OV	BOOST overvoltage
VBOOST_UVH	BOOST undervoltage high
LDO1_TSD	LDO1 overtemperature shutdown event
LDO1_OC	LDO1 overcurrent
LDO2_TSD	LDO2 overtemperature shutdown event
LDO2_OC	LDO2 overcurrent
WAKE1	WAKE1 transition
WAKE2	WAKE2 transition
COM	SPI communication error

Table 92. List of interrupts from fail-safe logic

Interrupt fail-safe	Description
FCCU12	FCCU12 bi-stable error detected
FCCU1	FCCU1 single error detected
FCCU2	FCCU2 single error detected
ERRMON	External IC error detected
VCOREMON_OV	VCOREMON overvoltage detected
VCOREMON_UV	VCOREMON undervoltage detected
VDDIO_OV	VDDIO overvoltage detected
VDDIO_UV	VDDIO undervoltage detected
VMONx_OV	VMONx overvoltage detected
VMONx_UV	VMONx undervoltage detected
WD_BAD_DATA	Wrong watchdog refresh – wrong data
WD_BAD_TIMING	Wrong watchdog refresh – CLOSED window or timeout

27.3 PSYNC for two FS6600

PSYNC function allows the management of a complex start-up sequence with multiple power management ICs like two FS6600 (OTP_PSYNC_CFG = 0) or one FS6600 plus one PF82 (OTP_PSYNC_CFG = 1). This function is enabled with the OTP_PSYNC_EN bit.

When PSYNC is used to synchronize two FS6600, the PSYNC pin of each device shall be connected together and pulled up to VBOS pin of the FS6600 controller device as shown in Figure 36. In this configuration, FS6600#1 state machine stops before FS6600#1_VPRE starts and waits for FS6600#2 to synchronize FS6600#2_VPRE start.

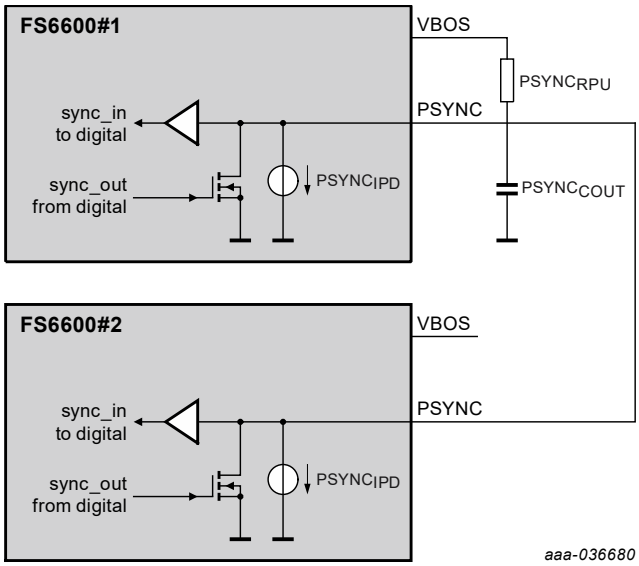


Figure 36. Synchronization of two FS6600

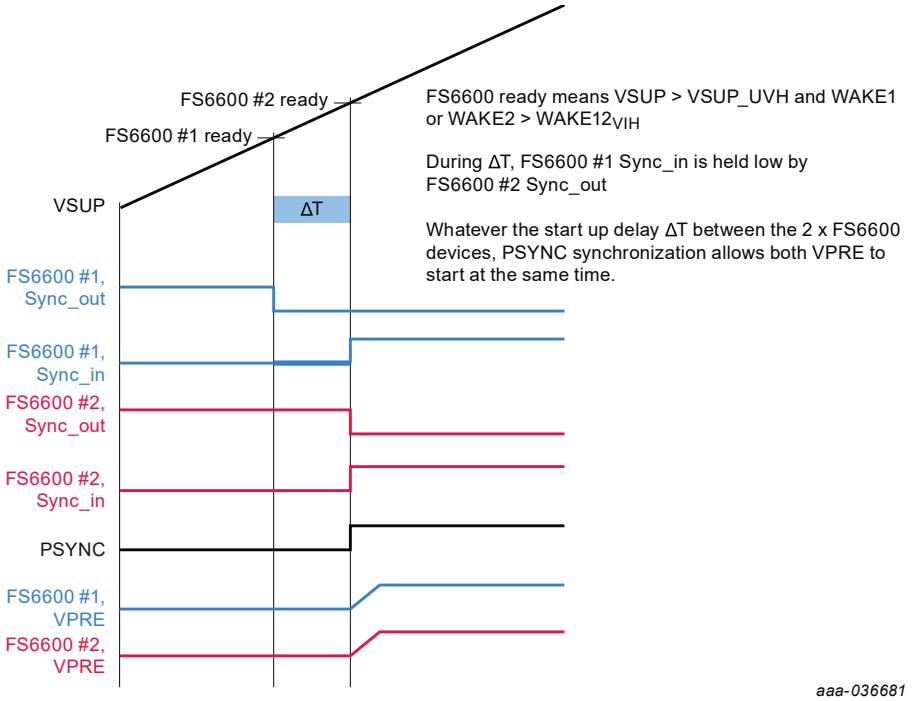


Figure 37. Two FS6600 synchronization timing diagram

27.4 PSYNC for FS6600 and external PMIC

When PSYNC is used to synchronize one FS6600 and one external PMIC, PSYNC pin of FS6600 shall be connected to PGOOD pin of the external PMIC. When the external PMIC is PF82 from NXP, it can be pulled up to VSNVS pin of PF82. In this configuration, FS6600 state machine stops after VPRE starts and waits for the PGOOD pin of the external PMIC to be released to continue its own power sequencing. It allows the power-up sequence of both devices to be synchronized.

During power-down sequence, FS6600 should wait the external PMIC power-down sequence completion before turning OFF VPRE (VPRE is powering the external PMIC). OTP_VPRE_off_dly bit shall be configured to extend VPRE turn OFF delay from 250 µs default value to 32 ms.

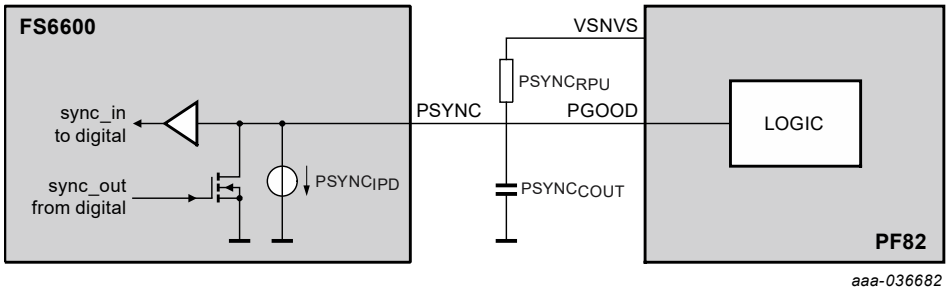


Figure 38. Synchronization of one FS6600 and one external PMIC (PF82)

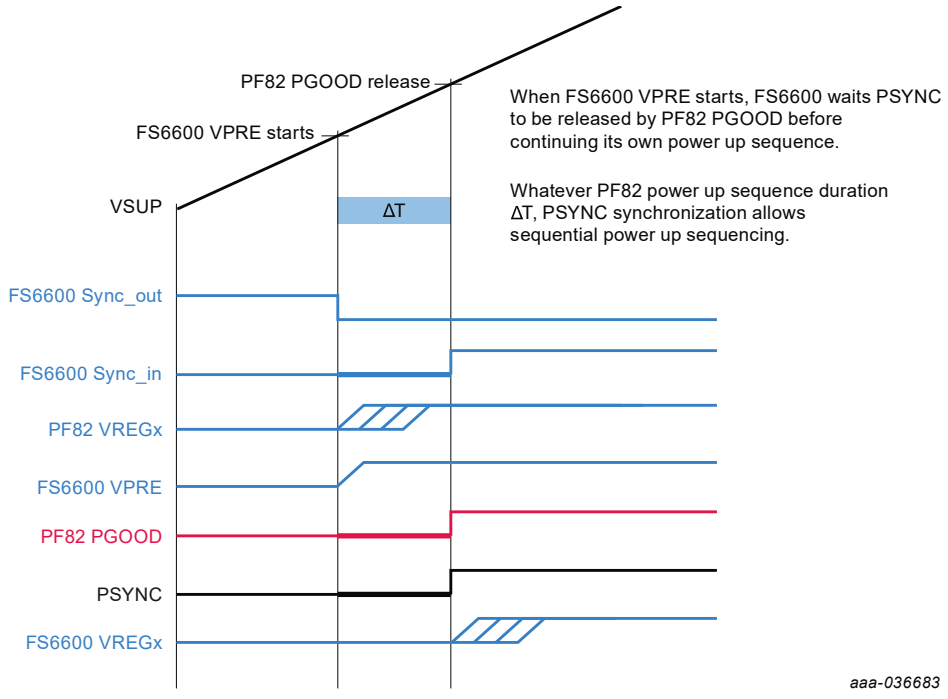


Figure 39. FS6600 and one external PMIC (PF82) synchronization timing diagram

Table 93. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
PSYNC					
$PSYNC_{VIL}$	Low-level input voltage threshold	1	—	—	V
$PSYNC_{VIH}$	High-level input voltage threshold	—	—	2	V
$PSYNC_{HYST}$	Hysteresis	0.1	—	—	V
$PSYNC_{VOL}$	Low-level output threshold (I = 2.0 mA)	—	—	0.5	V
$PSYNC_{IPD}$	Internal pulldown current source	7	10	13	µA
$PSYNC_{RPU}$	External pull-up resistor to VBOS	—	10	—	kΩ
$PSYNC_{COUT}$	External decoupling capacitor	—	0.1	—	µF
$PSYNC_{TFB}$	Feedback filtering time	6	10	15	µs

28 Cyclic Redundant Check generation

An 8-bit CRC is required for each Write and Read SPI command. Computation of a cyclic redundancy check is derived from the mathematics of polynomial division, modulo two.

The CRC polynomial used is x^8+x^4+x^3+x^2+1 (identified by 0x1D) with a SEED value of hexadecimal '0xFF'.

Figure 40 is an example of CRC encoding HW implementation.

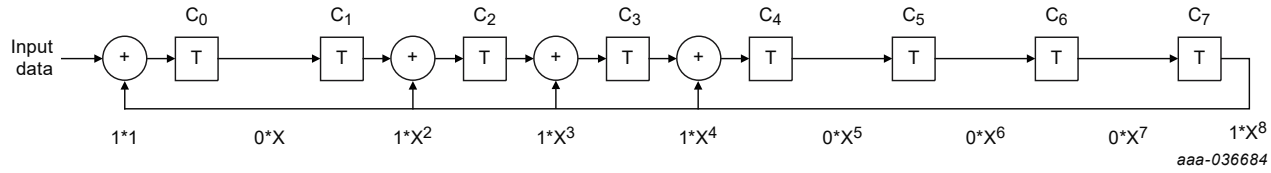


Figure 40. CRC encoder example

The effect of CRC encoding procedure is shown in the following table. The seed value is appended into the most significant bits of the shift register.

Table 94. Data preparation for CRC encoding (SPI format)

Seed	M/FS	Reg_ Address	Read/Write	Data_MSB	Data_LSB
0xFF	Bits[31]	Bit[30:25]	BIT[24]	Bit[23:16]	Bits[15:8]

Seed…	…padded with the message to encode…	…padded with 8 zeros

1. Using a serial CRC calculation method, the transmitter rotates the seed and data into the least significant bits of the shift register.
2. During the serial CRC calculation, the seed and the data bits are XOR compared with the polynomial data bits. When the MSB is logic 1, the comparison result is loaded in the register, otherwise the data bits are shifted. It must be noted the 32-bit message to be processed must have the bits corresponding to the CRC byte all equal to zero (00000000).
3. Once the CRC is calculated, it replaces the CRC byte initially set to all zeros and is transmitted.

Following is the procedure for the CRC decoding:

1. The seed value is loaded into the most significant bits of the receive register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
   - If the shift register contains all zeros, the CRC is correct.
   - If the shift register contains a value other than zero, the CRC is incorrect.

29 SPI interface

29.1 SPI interface overview

The FS6600 uses a 32-bit SPI, with the following arrangement:

- MOSI, SPI Primary Out Secondary Input bits:
  - Bit 31: main or fail-safe registers selection
  - Bit 30 to 25: register address
  - Bit 24: read/write
  - Bit 23 to 8: control bits
  - Bit7 to 0: cyclic redundant check (CRC)
- MISO, SPI Primary Input Secondary Output bits:
  - Bit 31-24: general device status
  - bits 23 to 8: extended device status, or device internal control register content or device flags
  - Bit7 to 0: cyclic redundant check (CRC)

The digital SPI pins (CSB, SCLK, MOSI, MISO) are referenced to VDDIO.

Table 95. SPI message arrangement

	B31	B30	B29	B28	B27	B26	B25	B24								
MOSI	M/FS	Adr_5	Adr_4	Adr_3	Adr_2	Adr_1	Adr_0	R/W								
MISO	COM_ERR	WU_G	VPRE_G	VBOOST_G	VBUCK1_G	VBUCK2_G	VBUCK3_G	VLDO_G								
	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8
MOSI	Data_15	Data_14	Data_13	Data_12	Data_11	Data_10	Data_9	Data_8	Data_7	Data_6	Data_5	Data_4	Data_3	Data_2	Data_1	Data_0
MISO	Data MSB								Data LSB							
									B7	B6	B5	B4	B3	B2	B1	B0
MOSI									CRC_7	CRC_6	CRC_5	CRC_4	CRC_3	CRC_2	CRC_1	CRC_0
MISO									CRC_7	CRC_6	CRC_5	CRC_4	CRC_3	CRC_2	CRC_1	CRC_0

The MCU is the controller driving MOSI and FS6600 is the slave driving MISO. The MISO data is latched at the SCLK rising edge and MOSI data is latched at the SCLK falling edge. In write command, MISO [23:8] bits are the previous register bits and MISO [7:0] is the CRC of the message sent by the FS6600. In read command, MOSI [23:8] bits are all 0 and MOSI [7:0] is the CRC of the message sent by the MCU. Refer to AN12333[11] for more details.

29.2 SPI CRC calculation and results

CRC calculation using XOR:

CRC_7 = XOR (B31, B24, B23, B22, B20, B17, B13, B12, B11, 1, 1)

CRC_6 = XOR (B31, B30, B23, B22, B21, B19, B16, B12, B11, B10, 1, 1)

CRC_5 = XOR (B30, B29, B22, B21, B20, B18, B15, B11, B10, B9, 1, 1)

CRC_4 = XOR (B29, B28, B21, B20, B19, B17, B14, B10, B9, B8, 1, 1)

CRC_3 = XOR (B28, B27, B24, B23, B22, B19, B18, B17, B16, B12, B11, B9, B8, 1, 1, 1)

CRC_2 = XOR (B27, B26, B24, B21, B20, B18, B16, B15, B13, B12, B10, B8, 1, 1, 1)

CRC_1 = XOR (B26, B25, B24, B22, B19, B15, B14, B13, B9, 1, 1, 1)

CRC_0 = XOR (B25, B24, B23, B21, B18, B14, B13, B12, B8, 1, 1)

CRC results examples:

Table 96. CRC result examples

M/FS, Register address, R/W, 8-bit (Hex)	Data MSB, 8-bit (Hex)	Data LSB, 8-bit (Hex)	CRC, 8-bit (Hex)
0x05	0x00	0x00	0x87
0x83	0xD0	0x0D	0x54

29.3 Electrical characteristics

Table 97. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
SPI					
F_{SPI}	SPI operation frequency (50 % DC)	0.5	—	10	MHz
t_{CLH}	Minimum time SCLK = HIGH	50	—	—	ns
t_{CLL}	Minimum time SCLK = LOW	50	—	—	ns
t_{PCLD}	Propagation delay (SCLK to data at 10 % of MISO rising edge)	—	—	30	ns
t_{CSDV}	CSB = low to data at MISO active	—	—	70	ns
t_{SCLCH}	SCLK low before CSB low (setup time SCLK to CSB change H/L)	70	—	—	ns
t_{HCLCL}	SCLK change L/H after CSB = low	70	—	—	ns
t_{SCLD}	SDI input setup time (SCLK change H/L after MOSI data valid)	35	—	—	ns
t_{HCLD}	SDI input hold time (MOSI data hold after SCLK change H/L)	35	—	—	ns
t_{SCLCL}	SCLK low before CSB high	90	—	—	ns
t_{HCLCH}	SCLK high after CSB high	90	—	—	ns
t_{PCHD}	CSB L/H to MISO at high-impedance	—	—	75	ns
t_{ONCSB}	CSB min. high time	500	—	—	ns
SPI_{VIL}	CSB, SCLK, MOSI low-level input voltage threshold	0.3 x V_{DDIO}	—	—	V
SPI_{VIH}	CSB, SCLK, MOSI high-level input voltage threshold	—	—	0.7 x V_{DDIO}	V
I_{CSB_MOSI}	CSB, MOSI Input leakage current	—	—	1.0	µA
$SCLK_{IPD}$	SCLK internal pulldown current source	7	10	13	µA
$MISO_{VOH}$	MISO high output voltage (I = 2.0 mA)	V_{DDIO}-0.4	—	—	V
$MISO_{VOL}$	MISO low output voltage (I = 2.0 mA)	—	—	0.4	V
I_{MISO}	Tri-state leakage current (VDDIO = 5.0 V)	−1.0	—	1.0	µA
$SPI_{PULL\text{-}up}$	CSB, MOSI internal pull-up (pull-up to VDDIO)	200	450	800	kΩ

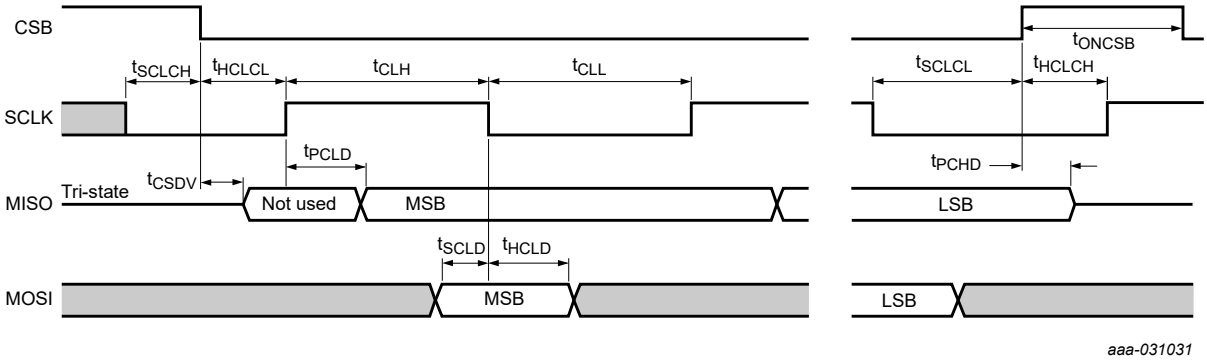


Figure 41. SPI timings

30 Application information

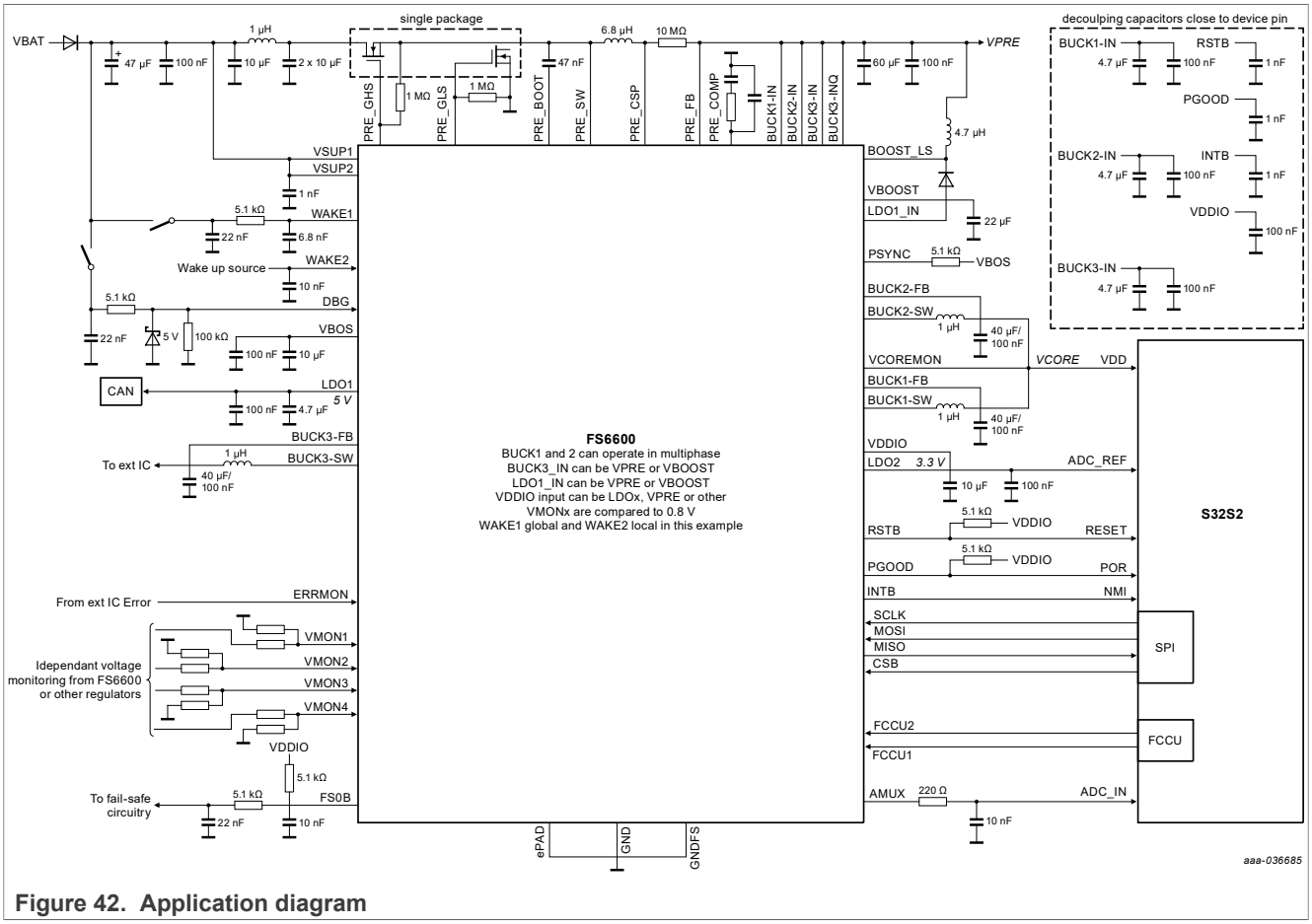


Figure 42. Application diagram

31 Functional safety

31.1 Functional description

The fail-safe domain is electrically independent and physically isolated. The fail-safe domain is supplied by its own reference voltages and current, has its own oscillator, has duplicated analog path to minimize the

common cause failures and has LBIST/ABIST to cover latent faults. The fail-safe domain offers ASIL B or ASIL D compliance depending on device part number. The fail-safe timings are derived from the fail-safe oscillator with ±10 % accuracy unless otherwise specified.

All fail-safe OTP bits are described in detail in the safety manual.

The fail-safe domain and the dedicated pins are represented in Figure 43:

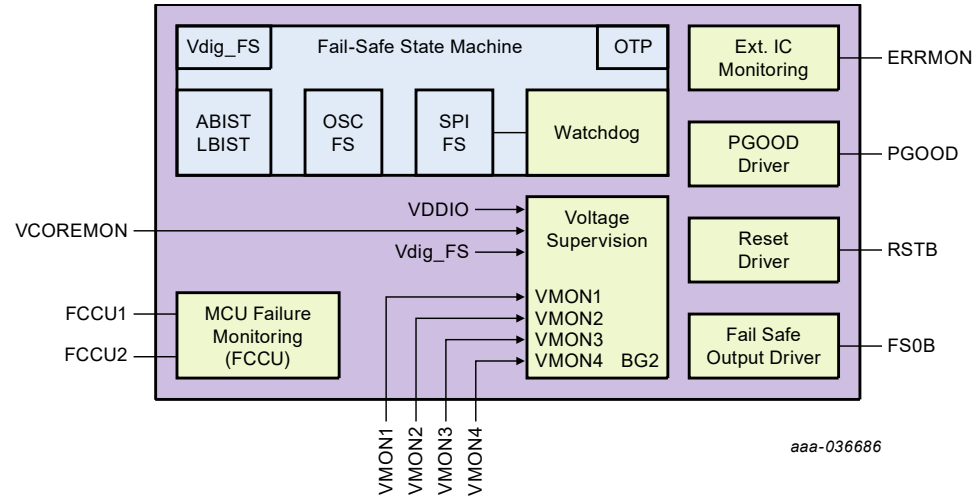


Figure 43. Fail-safe block diagram

31.2 Fail-safe initialization

After POR or wake-up from Standby, when the RSTB pin is released, the fail-safe state machine enters in INIT_FS phase for initialization. To secure the writing process during INIT_FS phase, in addition to CRC computation during SPI transfer, it is requested for the MCU to perform the following sequence for all INIT_FS registers:

1 - Write the desired data in the FS_I_Register_A (DATA)

2 - Write the opposite in the FS_I_NOT_Register_A (DATA_NOT)

As an example, if the data of FS_I_Register_A = 0xABCD, the data not of FS_I_NOT_Register_A = 0x5432. A real-time comparison process (XOR) is performed by the FS6600 to ensure DATA FS_I_Register_A = DATA_NOT FS_I_NOT_Register_A. Only the utility bits must be inverted in the DATA_NOT content. The RESERVED bits are not considered and can be written at ‘0’. If the comparison result is correct, then the REG_CORRUPT is set to ‘0’. If the comparison result is wrong, then the REG_CORRUPT bit is set to ‘1’. The REG_CORRUPT monitoring is active as soon as the INIT_FS is closed by the first good watchdog refresh.

INIT_FS must be closed by the first good watchdog refresh before 256 ms timeout.

After INIT_FS closure, it is possible to come back to INIT_FS with the GoTo_INITFS bit in FS_SAFE_IOS register, from any FS_state after INIT_FS. NXP recommends sending the GoTo_INITFS command just after a good watchdog refresh.

31.3 Watchdog

The watchdog is a windowed watchdog for the Simple and the Challenger watchdog. The first half of the window is said CLOSED and the second half is said OPEN. A good watchdog refresh is a good watchdog answer during the OPEN window. A bad watchdog refresh is a bad watchdog answer during the OPEN window, no watchdog refresh during the OPEN window or a good watchdog answer during the CLOSED window.

After a good or a bad watchdog refresh, a new window period starts immediately for the MCU to keep the synchronization with the windowed watchdog.

The first good watchdog refresh closes the INIT_FS. Then the watchdog window is running and the MCU must refresh the watchdog in the OPEN window of the watchdog window period. The duration of the watchdog window is configurable from 1.0 ms to 1024 ms with the WDW_PERIOD [3:0] bits. The new watchdog window is effective after the next watchdog refresh. The watchdog window can be disabled during INIT_FS only. The watchdog disable is effective when the INIT_FS is closed.

The watchdog configuration requires to write in FS_WD_WINDOW and FS_NOT_WD_WINDOW registers like INIT registers.

Table 98. Watchdog window period configuration

WDW_PERIOD [3:0]	Watchdog window period
0000	DISABLE (during INIT_FS only)
0001	1.0 ms
0010	2.0 ms
0011 (default)	**3.0 ms**
0100	4.0 ms
0101	6.0 ms
0110	8.0 ms
0111	12 ms
1000	16 ms
1001	24 ms
1010	32 ms
1011	64 ms
1100	128 ms
1101	256 ms
1110	512 ms
1111	1024 ms
Reset condition	POR

The duty cycle of the watchdog window is configurable from 31.25 % to 68.75 % with the WDW_DC [2:0] bits. The new duty cycle is effective after the next watchdog refresh.

Table 99. Watchdog window duty cycle configuration

WDW_DC [2:0]	CLOSED window	OPEN window
000	31.25 %	68.75 %
001	37.5 %	62.5 %
010 (default)	**50 %**	**50 %**
011	62.5 %	37.5 %
100	68.75 %	31.25 %
Others	50 %	50 %
Reset condition	POR	

31.3.1 Challenger watchdog

The Challenger watchdog monitoring feature is enabled by OTP_WD_SELECTION bit. The Challenger watchdog is based on a question/answer process with the MCU. A 16-bits pseudo-random word is generated by implementing a Linear Feedback Shift Register (LFSR) in the FS6600. The MCU can send the seed of the LFSR or use the LFSR generated by the FS6600 during the INIT_FS phase and performs a pre-defined calculation. The result is sent through the SPI during the OPEN watchdog window and verified by the FS6600. When the result is right, the watchdog window is restarted and a new LFSR is generated. When the result is wrong, the WD error counter is incremented, the watchdog window is restarted and the LFSR value is not changed.

During the initialization phase (INIT_FS), the MCU sends the seed for the LFSR, or uses the default LFSR value generated by the FS6600 (0x5AB2), available in the WD_SEED register. Using this LFSR, the MCU performs a simple calculation based on below formula and sends the results in the WD_ANSWER register.

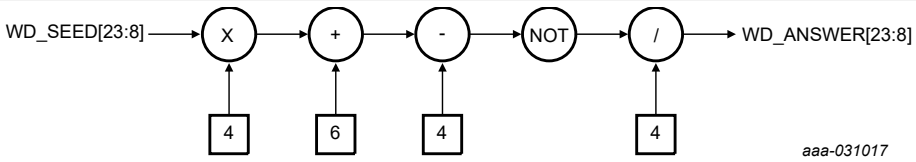


Figure 44. Challenger watchdog formula

In Challenger watchdog configuration, it is impossible to write 0x0000 in WD_SEED register. A communication error is reported in case of 0x0000 write tentative and the configuration is ignored.

31.3.2 Simple watchdog

The Simple watchdog monitoring feature is enabled by OTP_WD_SELECTION bit. The Simple watchdog uses a unique seed. The MCU can send its own seed in WD_SEED register or uses the default value 0x5AB2. This seed must be written in the WD_ANSWER register during the OPEN watchdog window. When the result is right, the watchdog window is restarted. When the result is wrong, the WD error counter is incremented and the watchdog window is restarted. In Simple watchdog configuration, it is impossible to write 0xFFFF and 0x0000 in WD_SEED register. A communication error is reported in case of 0x0000 and 0xFFFF write tentative and the configuration is ignored.

31.3.3 Watchdog error counter

The watchdog error strategy is available for the Challenger watchdog and the Simple watchdog. The watchdog error counter is implemented in the device to filter the incorrect watchdog refresh. Each time a watchdog failure occurs, the device increments this counter by 2. The watchdog error counter is decremented by 1 each time the watchdog is properly refreshed. This principle ensures a cyclic 'OK/NOK' behavior converges to a failure detection.

To allow flexibility in the application, the maximum value of this counter is configurable with the WD_ERR_LIMIT[1:0] bits during the INIT_FS phase.

Table 100. Watchdog error counter configuration

WD_ERR_LIMIT[1:0]	Watchdog error counter value
00	8
01 (default)	**6**
10	4
11	2
Reset condition	POR

The watchdog error counter value can be read by the MCU for diagnostic with the WD_ERR_CNT[3:0] bits.

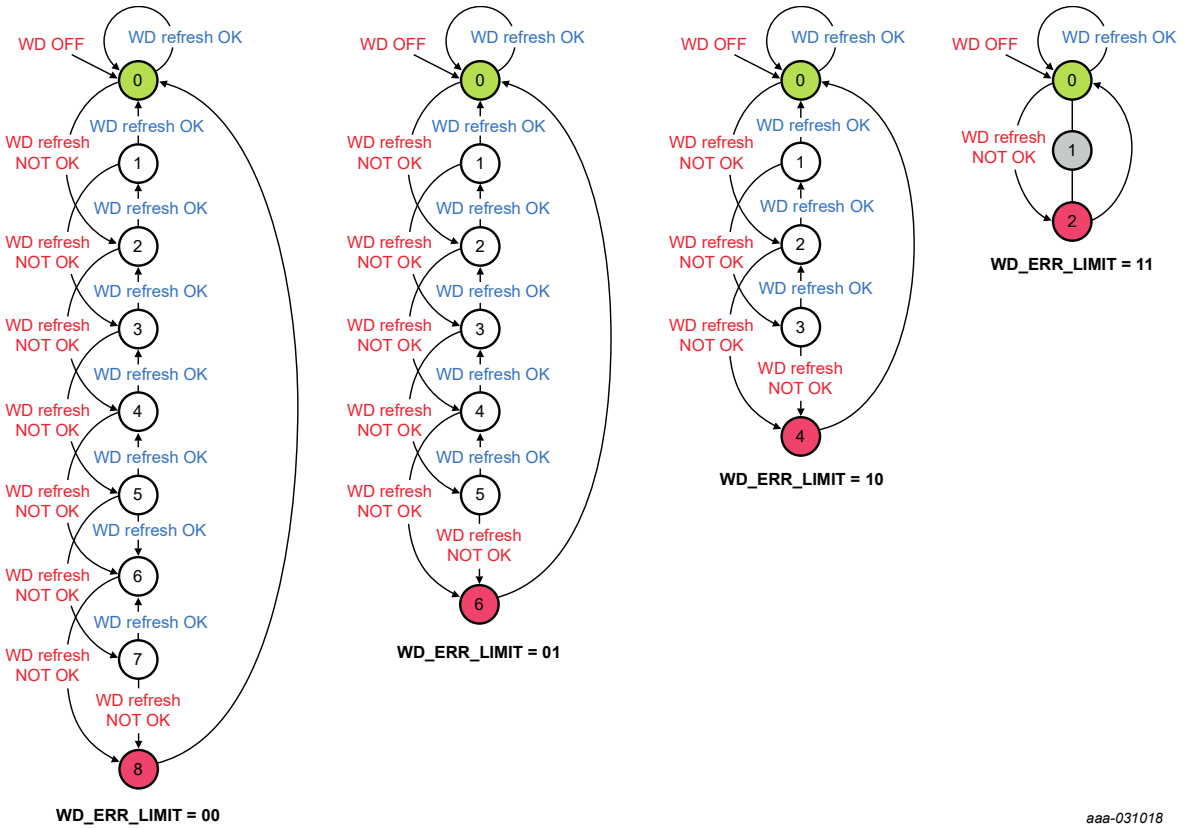


Figure 45. Watchdog error counter configurations

31.3.4 Watchdog refresh counter

The watchdog refresh strategy is available for the Challenger watchdog and the Simple watchdog. The watchdog refresh counter is used to decrement the fault error counter. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by '1'. Each time the watchdog refresh counter reaches its maximum value ('6' by default) and if next WD refresh is also good, the fault error counter is decremented by '1'. Whatever the position the watchdog refresh counter is in, each time there is a wrong refresh watchdog, the watchdog refresh counter is reset to '0'.

To allow flexibility in the application, the maximum value of this watchdog refresh counter is configurable with the WD_RFR_LIMIT[1:0] bits during the INIT_FS phase.

Table 101. Watchdog refresh counter configuration

WD_RFR_LIMIT[1:0]	Watchdog refresh counter value
00 (default)	**6**
01	4
10	2
11	1
Reset condition	POR

The watchdog refresh counter value can be read by the MCU for diagnostic with the WD_RFR_CNT[2:0] bits.

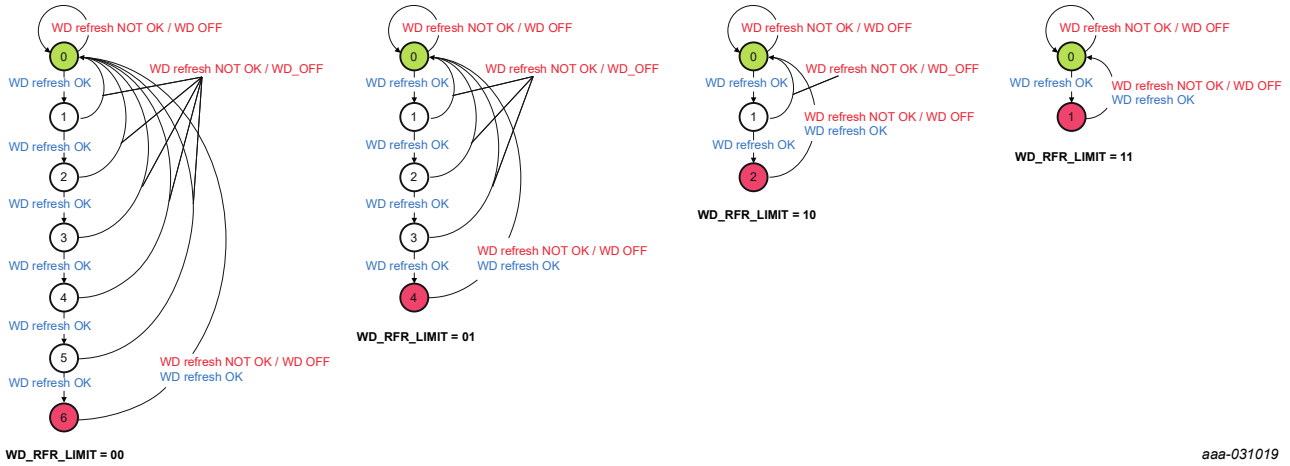


Figure 46. Watchdog refresh counter configurations

31.3.5 Watchdog error impact

When the watchdog error counter reaches its maximum value, the fail-safe reaction on RSTB and/or FS0B is configurable with the WD_FS_IMPACT[1:0] bits during the INIT_FS phase.

Table 102. Watchdog error impact configuration

WD_FS_IMPACT[1:0]	Watchdog error impact on RSTB/FS0B
00	No action on RSTB and FS0B
01	FS0B only is asserted if WD error counter = WD_ERR_ LIMIT[1:0]
1x	**FS0B and RSTB are asserted if WD error counter = WD_ ERR_LIMIT[1:0]**
Reset condition	POR

31.3.6 MCU fault recovery strategy

The fault recovery strategy feature is enabled by OTP_FLT_RECOVERY_EN bit. This function extends the watchdog window to allow the MCU to perform a fault recovery strategy. The goal is to not reset the MCU while it is trying to recover the application after a failure event. When a fault is triggered by the MCU via its FCCU pins, the FS0B pin is asserted by the device and the watchdog window duration becomes automatically an open window (no more duty cycle). This open window duration is configurable with the WDW_RECOVERY [3:0] bits during the INIT_FS phase.

Table 103. Watchdog window in fault recovery configuration

WDW_RECOVERY [3:0]	Watchdog window duration when the device is in fault recovery strategy
0000	DISABLE
0001	1.0 ms
0010	2.0 ms
0011	3.0 ms
0100	4.0 ms
0101	6.0 ms
0110	8.0 ms
0111	12 ms
1000	16 ms
1001	24 ms
1010	32 ms
1011(default)	**64 ms**
1100	128 ms
1101	256 ms
1110	512 ms
1111	1024 ms
Reset condition	POR

The transition from WDW_PERIOD to WDW_RECOVERY happens when the FCCU pin indicates an error and FS0B is asserted. If the MCU sends a good watchdog refresh before the end of the WDW_RECOVERY duration, the device switches back to the WDW_PERIOD duration and associated duty cycle if the FCCU pins do not indicate an error anymore. Otherwise, a new WDW_RECOVERY period is started. If the MCU does not send a good watchdog refresh before the end of the WDW_RECOVERY duration, then a reset pulse is generated, and the fail-safe state machine moves back to INIT_FS.

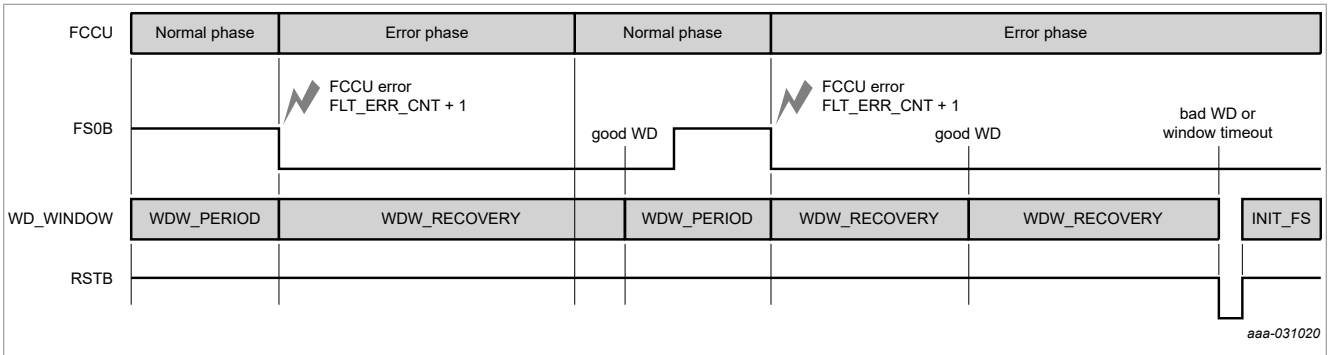


Figure 47. Fault recovery strategy principle

31.4 FCCU monitoring

The FCCU monitoring feature is enabled by OTP_FCCU_EN bit. The FCCU input pins are in charge of monitoring HW failure from the MCU. The FCCU input pins can be configured by pair, or single independent

inputs. The FCCU monitoring is active as soon as the INIT_FS is closed by the first good watchdog refresh. The FCCU input pins are configured by pair, or single independent inputs with the FCCU_CFG[1:0] bits.

Table 104. FCCU pins configuration

FCCU_CFG[1:0]	FCCU pins configuration
00	No monitoring
01 (default)	**FCCU1 and FCCU2 monitoring by pair (bi-stable protocol)**
10	FCCU1 or FCCU2 input monitoring
11	FCCU1 input monitoring only
Reset condition	POR

31.4.1 FCCU12 monitoring by pair

When FCCU12 are used by pair, the bi-stable protocol is supported according to Figure 48:

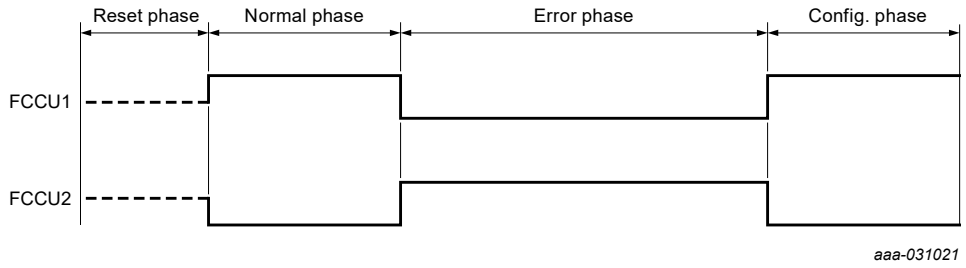


Figure 48. FCCU bi-stable protocol

The polarity of the FCCU fault signals is configurable with FCCU12_FLT_POL bit during the INIT_FS phase.

Table 105. FCCU12 polarity configuration

FCCU12_FLT_POL	FCCU12 polarity
0 (default)	**FCCU1=0 or FCCU2=1 level is a fault**
1	FCCU1=1 or FCCU2=0 level is a fault
Reset condition	POR

When FCCU fault is detected, the fail-safe reaction on RSTB and/or FS0B is configurable with the FCCU12_FS_IMPACT bit during the INIT_FS phase

Table 106. FCCU12 error impact configuration

FCCU12_FS_IMPACT	FCCU12 impact on RSTB/FS0B
0	FS0B only is asserted
1 (default)	**FS0B and RSTB are asserted**
Reset condition	POR

31.4.2 FCCU12 independent monitoring

When FCCU1 and/or FCCU2 are used independently, the FCCU inputs can monitor two different and independent error signals. For each input the polarity of the FCCU fault signal is configurable with FCCUx_FLT_POL bits during the INIT_FS phase.

Table 107. FCCUx polarity configuration

FCCU1_FLT_POL	FCCU1 polarity
0 (default)	**FCCU1 low-level is a fault**
1	FCCU1 high-level is a fault
Reset condition	POR

FCCU2_FLT_POL	FCCU2 polarity
0 (default)	**FCCU2 low-level is a fault**
1	FCCU2 high-level is a fault
Reset condition	POR

When FCCU fault is detected, the fail-safe reaction on RSTB and/or FS0B is configurable with the FCCUx_FS_IMPACT bits during the INIT_FS phase.

Table 108. FCCUx error impact configuration

FCCU1_FS_IMPACT	FCCU1 impact on RSTB/FS0B
0	FS0B only is asserted
1 (default)	**FS0B and RSTB are asserted**
Reset condition	POR

FCCU2_FS_IMPACT	FCCU2 impact on RSTB/FS0B
0	FS0B only is asserted
1 (default)	**FS0B and RSTB are asserted**
Reset condition	POR

31.4.3 FCCU12 electrical characteristics

Table 109. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
FCCU1,2					
$FCCU12_{TERR}$	FCCU1,2 filtering time	4.0	—	8.0	µs
$FCCU12_{VIH}$	FCCU1,2 high-level input voltage threshold	—	—	0.7 x V_{DDIO}	V
$FCCU12_{VIL}$	FCCU1,2 low level input voltage threshold	0.3 x V_{DDIO}	—	—	V
$FCCU12_{HYST}$	FCCU1,2 input voltage hysteresis	0.1 x V_{DDIO}	—	1.85	V
$FCCU12_{ILKG}$	Input leakage current	—	—	1.0	µA
$FCCU1_{RPD}$	FCCU1 internal pulldown resistor	400	800	1300	kΩ
$FCCU2_{RPU}$	FCCU2 internal pull-up resistor to VDDIO	100	200	400	kΩ
$FCCU12_{RATIO}$	FCCU1/2 internal resistor ratio ($FCCU1_{RPD}$ / $FCCU2_{RPD}$)	3.5	4	4.5	—

31.5 Voltage supervisor

The voltage supervisor is in charge of overvoltage and undervoltage monitoring of VCOREMON, VDDIO and VMONx input pins. When an overvoltage occurs on an FS6600 regulator monitored by one of these pins, the associated FS6600 regulator is switched off until the fault is removed. The voltage monitoring is active as soon as FS_ENABLE=1 and UV/OV flags are then reported accordingly.

31.5.1 VCOREMON monitoring

VCOREMON input pin is dedicated to BUCK1 or BUCK1 and BUCK2 in case of multiphase operation. When overvoltage or undervoltage fault is detected, the fail-safe reaction on RSTB and/or FS0B is configurable with the VCOREMON_OV/UV_FS_IMPACT[1:0] bits during the INIT_FS phase.

Table 110. VCOREMON error impact configuration

VCOREMON_OV_FS_IMPACT[1:0]	VCOREMON OV impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01	FS0B only is asserted
1x (default)	**FS0B and RSTB are asserted**
Reset condition	POR
VCOREMON_UV_FS_IMPACT[1:0]	**VCOREMON UV impact on RSTB/FS0B**
00	No effect on RSTB and FS0B
01 (default)	**FS0B only is asserted**
1x	FS0B and RSTB are asserted
Reset condition	POR

Table 111. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VCOREMON					
VCOREMON_OV_min	Overvoltage threshold minimum	—	+4.5	—	%
VCOREMON_OV_max	Overvoltage threshold maximum	—	+12	—	%
VCOREMON_OV_step	Overvoltage threshold step (OTP_VCOREOVTH[7:0] bits)	—	+0.5	—	%
VCOREMON_OV_acc	Overvoltage threshold accuracy	−2	—	2	%
TCOREMON_OV	Overvoltage filtering time (OTP_VCORE_OV_DGLT bit)	20	25	30	µs
		40	45	50	µs
VCOREMON_UV_min	Undervoltage threshold minimum	—	−4.5	—	%
VCOREMON_UV_max	Undervoltage threshold maximum	—	−12	—	%
VCOREMON_UV_step	Undervoltage threshold step (OTP_VCOREUVTH[7:0] bits)	—	−0.5	—	%
VCOREMON_UV_acc	Undervoltage threshold accuracy	−2	—	2	%
TCOREMON_UV	Undervoltage filtering time (OTP_VCORE_UV_DGLT[1:0] bits)	2.5	5	7.5	µs
		10	15	20	µs
		20	25	30	µs
		35	40	45	µs

31.5.2 Static voltage scaling (SVS)

A static voltage scaling function is implemented to allow the MCU to reduce the output voltage initially configured at start-up of BUCK1 (and BUCK2 if used in multiphase). The SVS configuration must be done in INIT_FS phase. The offset value is configurable by SPI with the SVS_OFFSET[4:0] bits and the exact complemented value shall be written in the NOT_SVS_OFFSET[4:0] bits.

Table 112. SVS offset configuration

SVS_OFFSET[4:0]	NOT_SVS_OFFSET[4:0]	Offset applied to BUCK1 (and BUCK2 if used in multiphase)
00000 (default)	**11111**	**0 mV**
00001	11110	−6.25 mV
- - - - -	- - - - -	−6.25 mV step per bit
10000	01111	−100 mV
Reset condition	POR	

The BUCK1/2 output voltage transition starts when the NOT_SVS_OFFSET[4:0] SPI command is received and confirmed good. If the NOT_SVS_OFFSET[4:0] SPI command is not the exact opposite to the SVS_OFFSET[4:0] SPI command, the SVS procedure is not executed and the BUCK1 output voltage remains at its original value. The OV/UV threshold changes immediately when the NOT_SVS_OFFSET[4:0] SPI command is received and confirmed good. The BUCK1 output voltage transition last less than TCOREMON_OV, preventing a false OV detection.

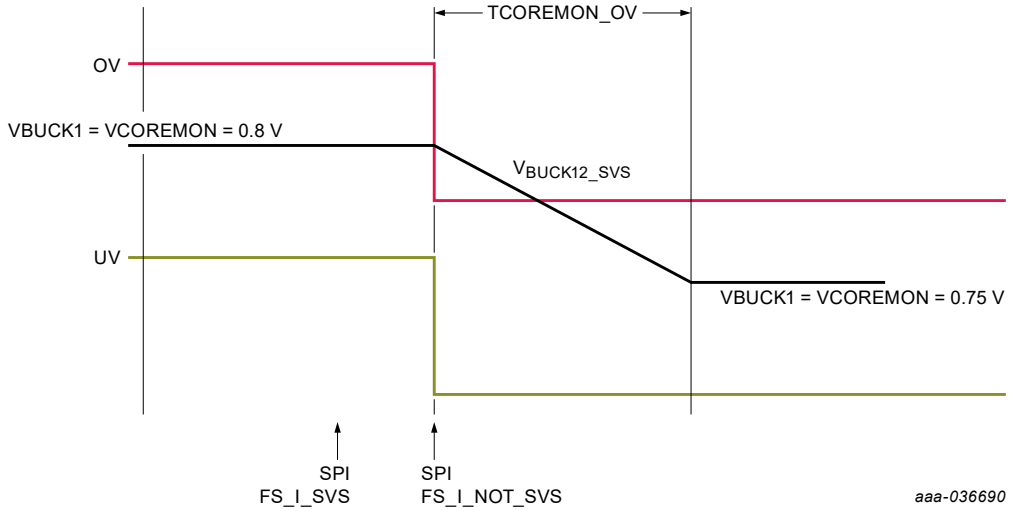


Figure 49. SVS principle

31.5.3 VDDIO monitoring

VDDIO input pin can be connected to VPRE, LDO1, LDO2, BUCK3 or an external regulator. The regulator connected to VDDIO must be at 3.3 V or 5.0 V to be compatible with overvoltage and undervoltage monitoring thresholds. In order to turn OFF the regulator in case of overvoltage detection, the configuration of which regulator is connected to VDDIO is done with OTP_VDDIO_REG_ASSIGN[2:0] bits. If an external regulator (not delivered by the FS6600) is connected to VDDIO, this regulator cannot be turned OFF, but the overvoltage flag is reported to the MCU which can take appropriate action. In all cases, the fail-safe reaction on RSTB and/or FS0B configured with VDDIO_OV/UV_FS_IMPACT[1:0] bits is guaranteed.

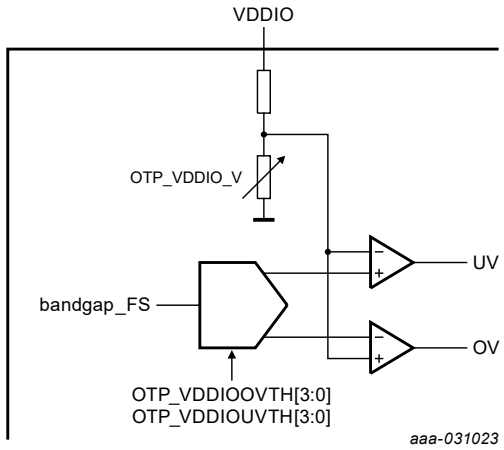


Figure 50. VDDIO monitoring principle

When overvoltage or undervoltage fault is detected, the fail-safe reaction on RSTB and/or FS0B is configurable with the VDDIO_OV/UV_IMPACT[1:0] bits during the INIT_FS phase.

Table 113. VDDIO error impact configuration

VDDIO_OV_FS_IMPACT[1:0]	VDDIO OV impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01	FS0B only is asserted
1x (default)	**FS0B and RSTB are asserted**
Reset condition	POR

VDDIO_UV_FS_IMPACT[1:0]	VDDIO UV impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01 (default)	**FS0B only is asserted**
1x	FS0B and RSTB are asserted
Reset condition	POR

Table 114. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VDDIO					
VDDIO_OV_min	Overvoltage threshold minimum	—	+4.5	—	%
VDDIO_OV_max	Overvoltage threshold maximum	—	+12	—	%
VDDIO_OV_step	Overvoltage threshold step (OTP_VDDIOOVTH[7:0] bits)	—	+0.5	—	%
VDDIO_OV_acc	Overvoltage threshold accuracy	−2	—	2	%
TVDDIO_OV	Overvoltage filtering time (OTP_VDDIO_OV_DGLT bit)	20	25	30	µs
		40	45	50	µs
VDDIO_UV_min	Undervoltage threshold minimum	—	−4.5	—	%
VDDIO_UV_max	Undervoltage threshold maximum	—	−12	—	%
VDDIO_UV_step	Undervoltage threshold step (OTP_VDDIOUVTH[7:0] bits)	—	−0.5	—	%
VDDIO_UV_acc	Undervoltage threshold accuracy	−2	—	2	%
TVDDIO_UV	Undervoltage filtering time (OTP_VDDIO_UV_DGLT[1:0] bits)	2.5	5	7.5	µs
		10	15	20	µs
		20	25	30	µs
		35	40	45	µs

31.5.4 VMONx monitoring

Each VMONx monitoring feature is enabled by OTP. VMONx input pin can be connected to VPRE, LDO1, LDO2, BUCK3, BUCK2 (in case BUCK2 is not used in multiphase) or even an external regulator. In order to turn OFF the regulator in case of Overvoltage detection, the configuration of which regulator is connected to VMONx is done by SPI in the register M_VMON_REGx. If an external regulator (not delivered by the FS6600) is connected to VMONx, this regulator cannot be turned OFF, but the Overvoltage flag is reported to the MCU which can take appropriate action. In all cases, the fail-safe reaction on RSTB and/or FS0B configured with VMONx_OV/UV_FS_IMPACT[1:0] bits is guaranteed.

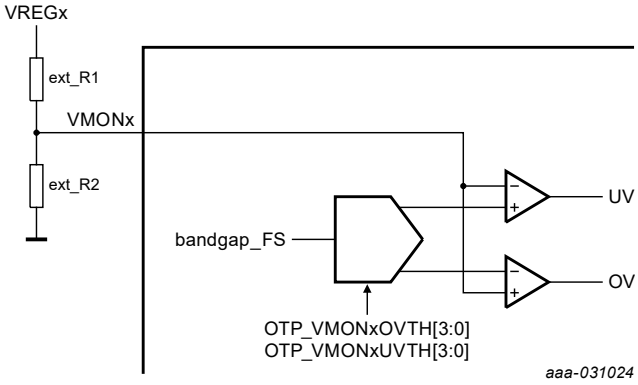


Figure 51. VMONx monitoring principle

The external resistor bridge connected to VMONx shall be calculated to deliver a middle point of 0.8 V. NXP recommends using a ±1 % or less resistor accuracy. When overvoltage or undervoltage fault is detected, the fail-safe reaction on RSTB and/or FS0B is configurable with the VMONx_OV/UV_FS_IMPACT[1:0] bits during the INIT_FS phase.

Table 115. VMONx error impact configuration

VMONx_OV_FS_IMPACT[1:0]	VMONx OV impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01	FS0B only is asserted
1x (default)	**FS0B and RSTB are asserted**
Reset condition	POR

VMONx_UV_FS_IMPACT[1:0]	VMONx UV impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01 (default)	**FS0B only is asserted**
1x	FS0B and RSTB are asserted
Reset condition	POR

Table 116. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
VMONx (without ext resistor accuracy)					
VMONx_OV_min	Overvoltage threshold minimum	—	+4.5	—	%
VMONx_OV_max	Overvoltage threshold maximum	—	+12	—	%
VMONx_OV_step	Overvoltage threshold step (OTP_VMONxOVTH[7:0] bits)	—	+0.5	—	%
VMONx_OV_acc	Overvoltage threshold accuracy	−2	—	2	%
TMONx_OV	Overvoltage filtering time (OTP_VMONx_OV_DGLT bit)	20	25	30	µs
		40	45	50	µs
VMONx_UV_min	Undervoltage threshold minimum	—	−4.5	—	%
VMONx_UV_max	Undervoltage threshold maximum	—	−12	—	%
VMONx_UV_step	Undervoltage threshold step (OTP_VMONxUVTH[7:0] bits)	—	−0.5	—	%
VMONx_UV_acc	Undervoltage threshold accuracy	−2	—	2	%
TMONx_UV	Undervoltage filtering time (OTP_VMONx_UV_DGLT[1:0] bits)	2.5	5	7.5	µs
		10	15	20	µs
		20	25	30	µs
		35	40	45	µs
VMONx_PD	Internal passive pulldown	1	2	4	MΩ

31.6 External IC monitoring (ERRMON)

The external IC monitoring feature is enabled by OTP_ERRMON_EN bit. The ERRMON input pin is in charge to monitor an external IC on the application, neither the FS6600, nor the MCU. The ERRMON monitoring is active as soon as the INIT_FS is closed by the first good watchdog refresh.

A transition detected at ERRMON pin indicates an error from the external IC. The polarity of the ERRMON fault signal is configurable with ERRMON_FLT_POL bit during the INIT_FS phase.

Table 117. ERRMON polarity configuration

ERRMON_FLT_POL	ERRMON polarity
0 (default)	**Negative edge at ERRMON pin is a fault**
1	Positive edge at ERRMON pin is a fault
Reset condition	POR

The acknowledge timing from the MCU is configurable with the ERRMON_ACK_TIME[1:0] bits.

Table 118. ERRMON timing configuration

ERRMON_ACK_TIME[1:0]	ERRMON acknowledgment timing
00	1 ms
01 (default)	**8 ms**
10	16 ms
11	32 ms
Reset condition	POR

The acknowledgment by the MCU is done through SPI communication according to Figure 52.

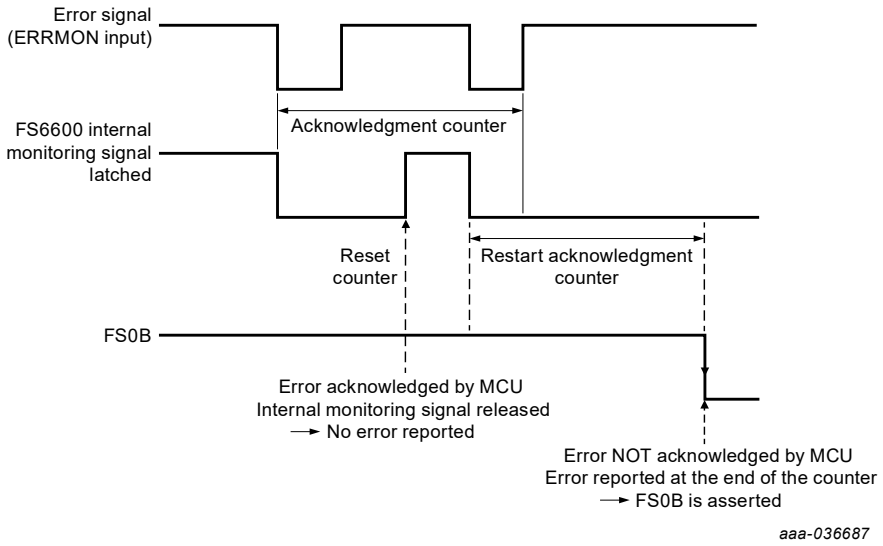


Figure 52. ERRMON principle

When ERRMON fault is detected, the fail-safe reaction on RSTB and/or FS0B is configurable with the ERRMON_FS_IMPACT bit during the INIT_FS phase.

Table 119. ERRMON error impact configuration

ERRMON_FS_IMPACT	ERRMON impact on RSTB/FS0B
0	FS0B only is asserted when ERRMON fault is detected
1 (default)	**FS0B and RSTB are asserted when ERRMON fault is detected**
Reset condition	POR

Table 120. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
ERRMON					
$ERRMON_{TACK\_ACC}$	Acknowledgment counter accuracy	−10	—	10	%
$ERRMON_{TERR}$	Filtering time	4.0	—	8.0	µs
$ERRMON_{VIH}$	High-level input voltage threshold	—	—	2.0	V
$ERRMON_{VIL}$	Low-level input voltage threshold	1.0	—	—	V
$ERRMON_{HYST}$	Input voltage hysteresis	100	—	500	mV
$ERRMON_{IPD}$	Internal pulldown current source	7	10	13	µA

31.7 Fault management

31.7.1 Fault error counter

The FS6600 integrates a configurable fault error counter which is counting the number of faults related to the device itself and also caused by external events. The fault error counter starts at level "1" after a POR or resuming from Standby. The final value of the fault error counter is used to transition in DEEP-FS mode. The maximum value of this counter is configurable with the FLT_ERR_CNT_LIMIT[1:0] bits during the INIT_FS phase.

Table 121. Fault error counter configuration

FLT_ERR_CNT_LIMIT[1:0]	Fault error counter max value configuration	Fault error counter intermediate value
00	2	1
01 (default)	**6**	**3**
10	8	4
11	12	6
Reset condition	POR	

The fault error counter has two output values: intermediate and final. The intermediate value can be used to force the FS0B activation or generate a RSTB pulse according to the FLT_ERR_IMPACT[1:0] bits configuration.

Table 122. Fault error counter impact configuration

FLT_ERR_IMPACT[1:0]	Fault error counter intermediate value impact on RSTB/FS0B
00	No effect on RSTB and FS0B
01	FS0B only is asserted if FLT_ERR_CNT=intermediate value
1x (default)	**FS0B is asserted if FLT_ERR_CNT=intermediate value** **RSTB is asserted for each value of FLT_ERR_CNT>=intermediate value**
Reset condition	POR

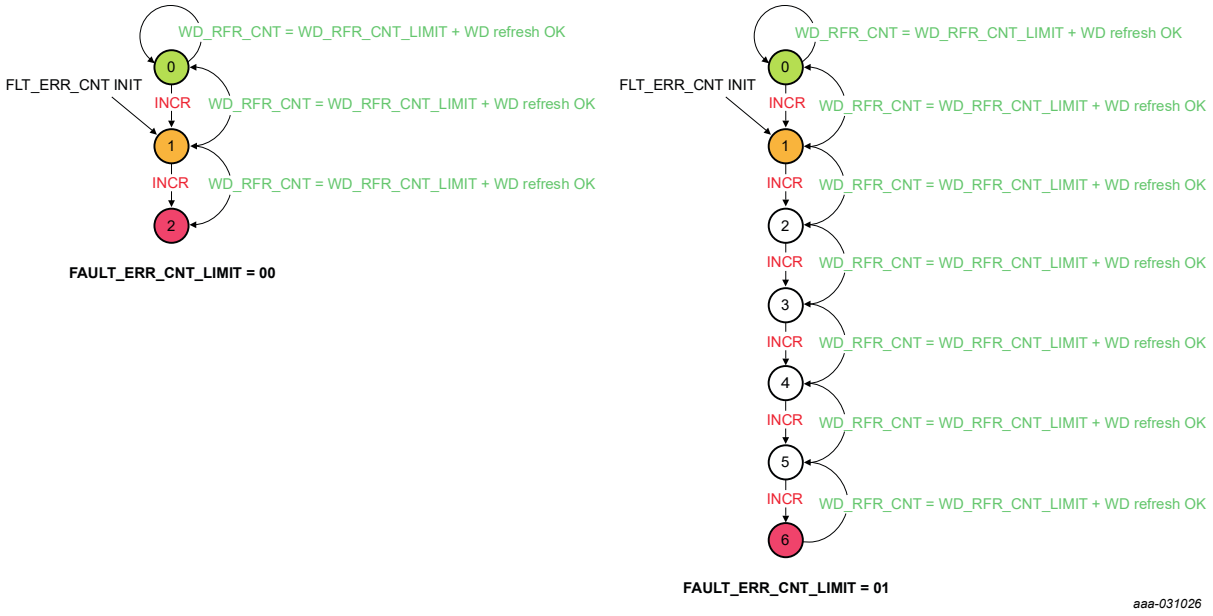


Figure 53. Fault error counter max value = 2 or 6

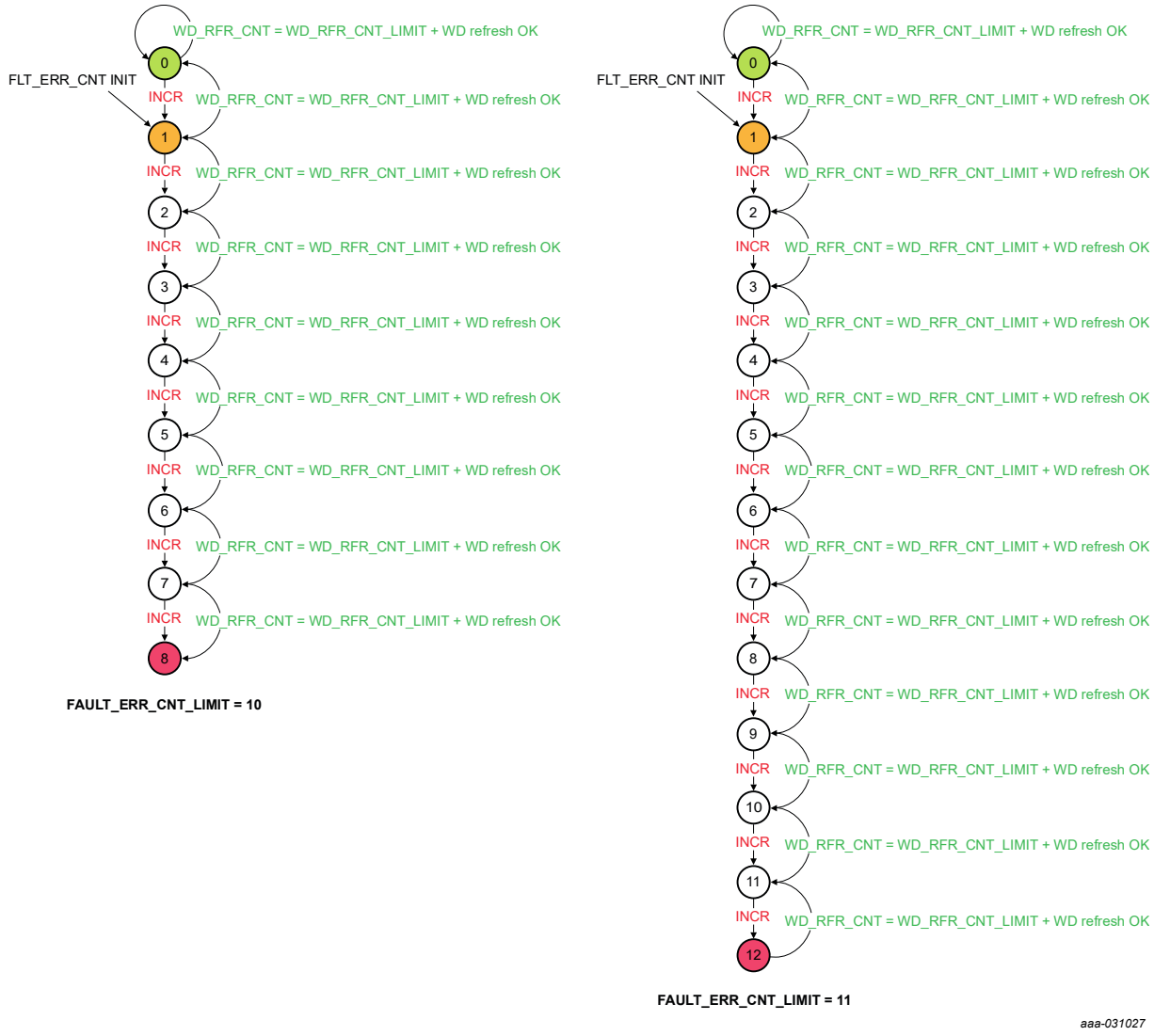


Figure 54. Fault error counter max value = 8 or 12

31.7.2 Fault source and reaction

In normal operation when FS0B and RSTB are released, the fault error counter is incremented when a fault is detected by the FS6600 fail-safe sate machine. Table 123 lists the faults and their impact on PGOOD, RSTB and FS0B pins according to the device configuration. The faults that are configured to not assert RSTB and FS0B will not increment the fault error counter. In that case, only the flags are available for MCU diagnostic. When FS0B is asserted, the fault error counter continues to be incremented by +1 each time the WD error counter reach its maximum value. The fault error counter is incremented by 1, each time the RSTB and/or FS0B pin is asserted.

Table 123. Application-related fail-safe fault list and reaction

With orange shading, the reaction in not configurable.

With green shading, the reaction is configurable by OTP for PGOOD and by SPI for RSTB/FS0B during INIT_FS.

Application-related fail-safe faults	FLT_ERR_CNT increment	FS0B assertion	RSTB assertion	PGOOD assertion
VCOREMON_OV	+1	VCOREMON_OV_FS_IMPACT[0]	VCOREMON_OV_FS_IMPACT[1]	OTP_PGOOD_VCORE
VDDIO_OV	+1	VDDIO_OV_FS_IMPACT[0]	VDDIO_OV_FS_IMPACT[1]	OTP_PGOOD_VDDIO
VMONx_OV	+1	VMONx_OV_FS_IMPACT[0]	VMONx_OV_FS_IMPACT[1]	OTP_PGOOD_VMONx
VCOREMON_UV	+1	VCOREMON_UV_FS_IMPACT[0]	VCOREMON_UV_FS_IMPACT[1]	OTP_PGOOD_VCORE
VDDIO_UV	+1	VDDIO_UV_FS_IMPACT[0]	VDDIO_UV_FS_IMPACT[1]	OTP_PGOOD_VDDIO
VMONx_UV	+1	VMONx_UV_FS_IMPACT[0]	VMONx_UV_FS_IMPACT[1]	OTP_PGOOD_VMONx
FCCU12 (pair)	+1	FCCU12_FS_IMPACT	FCCU12_FS_IMPACT	No
FCCU1 (single)	+1	FCCU1_FS_IMPACT	FCCU1_FS_IMPACT	No
FCCU2 (single)	+1	FCCU2_FS_IMPACT	FCCU2_FS_IMPACT	No
ERRMON	+1	ERRMON_FS_IMPACT	ERRMON_FS_IMPACT	No
WD error counter = max value	+1	WD_FS_IMPACT[0]	WD_FS_IMPACT[1]	No
Fault error counter impact at intermediate Value	No	FLT_ERR_IMPACT[0]	FLT_ERR_IMPACT[1]	No
Wrong WD refresh in INIT_FS	+1	Yes	Yes	No
No WD refresh in INIT_FS	+1	Yes	Yes	No
External RESET (out of extended RSTB)	+1	No[1]	Yes (low externally)	OTP_PGOOD_RSTB
RSTB pulse request by MCU	No	No[1]	Yes	No
RSTB short to high	+1	Yes	No (high externally)	No
FS0B short to high	+1	No (high externally)	FS0B_SC_HIGH_CFG	No
FS0B request by the MCU	No	Yes	No	No
REG_CORRUPT = 1	+1	Yes	No	No
OTP_CORRUPT = 1	+1	Yes	No	No
GOTO_INITFS request by MCU	No	Yes	No	No

[1] By cascaded effect, FSOB asserted low because of INIT_FS state.

If OTP_PGOOD_RSTB = ‘0’ (default configuration), RSTB and PGOOD pins work independently according to Table 123.

If OTP_PGOOD_RSTB = ‘1’, RSTB and PGOOD pins work concurrently and all the faults asserting RSTB will also assert PGOOD except in case of External RESET detection.

31.8 PGOOD, RSTB, FS0B

These three safety output pins have a hierarchical implementation in order to guarantee the safe state.

- PGOOD has the priority one. If PGOOD is asserted, RSTB and FS0B are asserted.
- RSTB has the priority two. If RSTB is asserted, FS0B is asserted but PGOOD may not be asserted.

- FS0B has the priority three. If FS0B is asserted, RSTB and PGOOD may not be asserted.

RSTB release is managed by the fail-safe state machine and depends on PGOOD release and ABIST1 execution.

Voltage monitoring assigned to PGOOD and to ABIST1 determines when RSTB is released. This configuration is done by OTP.

31.8.1 PGOOD

PGOOD is an open-drain output that can be connected in the application to the PORB of the MCU. PGOOD requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity. An internal pulldown RPD ensures PGOOD low-level in Standby and Power-down mode. BUCK1, VDDIO, VMONx can be assigned to PGOOD by OTP.

PGOOD is asserted low by the FS_LOGIC when any of the assigned regulators are in undervoltage or overvoltage. When PGOOD is asserted low, RSTB and FS0B are also asserted low. An internal pull up on the gate of the low-side MOS ensure PGOOD low-level in case of FS_LOGIC failure.

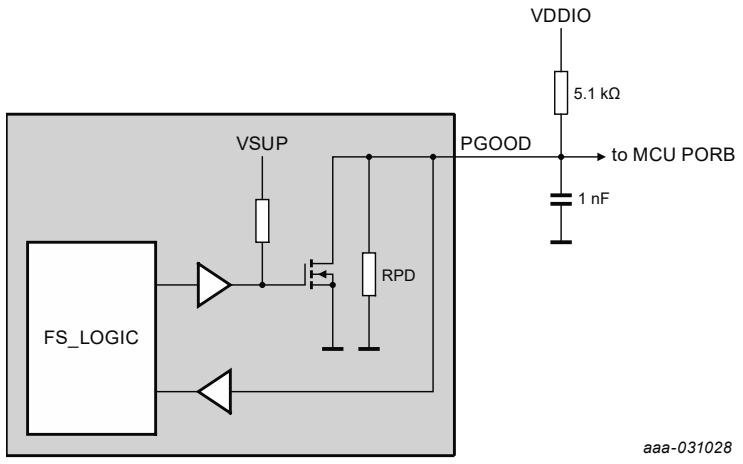


Figure 55. PGOOD pin implementation

Table 124. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
PGOOD					
$PGOOD_{VIL}$	Low-level input voltage threshold	1.0	—	—	V
$PGOOD_{VIH}$	High-level input voltage threshold	—	—	2.0	V
$PGOOD_{HYST}$	Input voltage hysteresis	100	—	—	mV
$PGOOD_{VOL}$	Low-level output voltage (I = 2.0 mA)	—	—	0.5	V
$PGOOD_{RPD}$	Internal pulldown resistor	200	400	800	kΩ
$PGOOD_{ILIM}$	Current limitation	4.0	—	20	mA
$PGOOD_{TFB}$	Feedback filtering time	8.0	—	15	µs

31.8.2 RSTB

RSTB is an open-drain output that can be connected in the application to the RESET of the MCU. RSTB requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity. An internal

pulldown RPD ensures RSTB low-level in Standby and Power-down mode. RSTB assertion depends on the device configuration during INIT_FS phase. When RSTB is asserted low, FS0B is also asserted low. An internal pull up on the gate of the low-side MOS ensures RSTB low-level in case of FS_LOGIC failure. When RSTB is stuck low for more than $RSTB_{T8S}$, the device transitions in DEEP-FS mode.

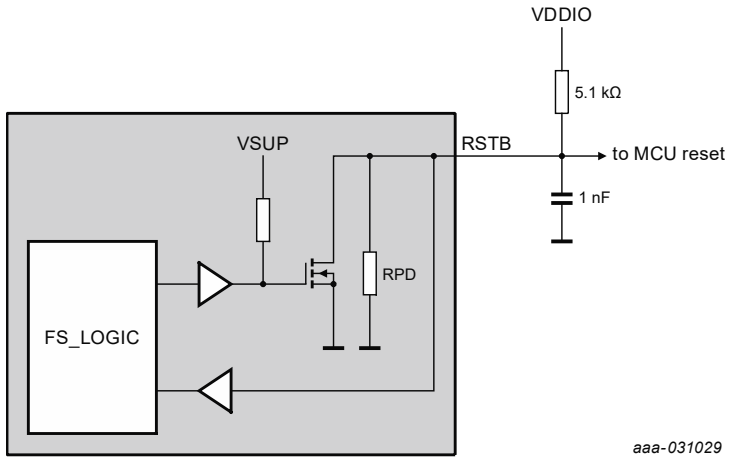


Figure 56. RSTB pin implementation

Table 125. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
RSTB					
$RSTB_{VIL}$	Low-level input voltage threshold	1.0	—	—	V
$RSTB_{VIH}$	High-level input voltage threshold	—	—	2.0	V
$RSTB_{HYST}$	Input voltage hysteresis	100	—	—	mV
$RSTB_{VOL}$	Low-level output voltage (I = 2.0 mA)	—	—	0.5	V
$RSTB_{RPB}$	Internal pull-down resistor	200	400	800	kΩ
$RSTB_{ILIM}$	Current limitation	4.0	—	20	mA
$RSTB_{TFB}$	Feedback filtering time	8.0	—	15	µs
$RSTB_{TSC}$	Short to high filtering time	500	—	800	us
$RSTB_{TLG}$	Long pulse (configurable with RSTB_DUR bit)	9.0	—	11	ms
$RSTB_{TST}$	Short pulse (configurable with RSTB_DUR bit)	0.9	—	1.1	ms
$RSTB_{T8S}$	8 second timer	7.0	8.0	9.0	s
$RSTB_{TRELEASE}$	Time to release RSTB from wake-up or POR with all regulators started in Slot 0	—	8	—	ms

31.8.3 FS0B

FS0B is an open-drain output that can be used to transition the system in safe sate. FS0B requires an external pull-up resistor to VDDIO or VSUP, a 10 nF filtering capacitor to GND for immunity when FS0B is a local pin, and an additional RC network when FS0B is a global pin to be robust against ESD GUN and ISO 7637 transient pulses. An internal pulldown RPD ensures FS0B low-level in Standby and Power-down mode. FS0B assertion depends on the device configuration during INIT_FS phase. An internal pull up on the gate of the low-side MOS ensures FS0B low-level in case of FS_LOGIC failure.

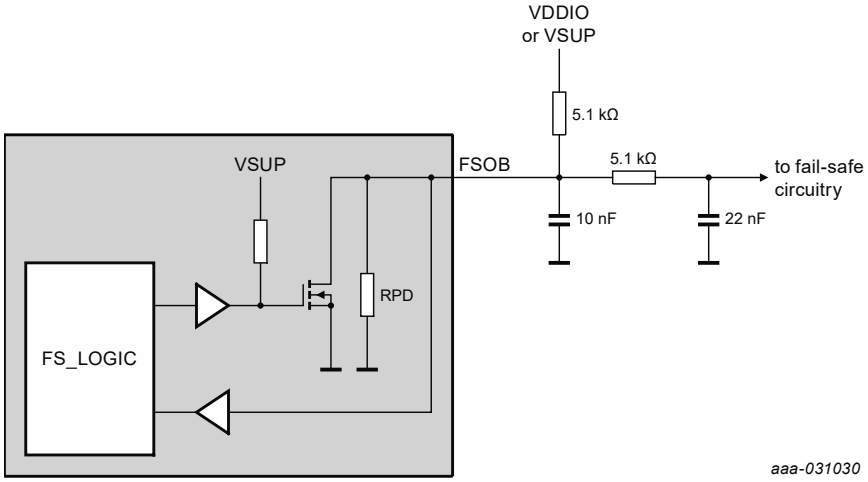


Figure 57. FS0B pin implementation

Table 126. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
FS0B					
$FS0B_{VIL}$	Low-level input voltage threshold	1.0	—	—	V
$FS0B_{VIH}$	High-level input voltage threshold	—	—	2.0	V
$FS0B_{HYST}$	Input voltage hysteresis	100	—	—	mV
$FS0B_{VOL}$	Low-level output voltage (I = 2.0 mA)	—	—	0.5	V
$FS0B_{RPD}$	Internal pulldown resistor	1	2	4	MΩ
$FS0B_{ILIM}$	Current limitation	4.0	—	20	mA
$FS0B_{TFB}$	Feedback filtering time	8.0	—	15	µs
$FS0B_{TSC}$	Short to high filtering time	500	—	800	µs

31.8.4 FS0B release

When the fail-safe output FS0B is asserted low by the device due to a fault, some conditions must be validated before allowing these pins to be released by the device. These conditions are:

- LBIST_OK = ABIST1_OK = ABIST2_OK = 1
- Fault Error Counter = 0
- RELEASE_FS0B register filled with ongoing WD_SEED reversed and complemented

Table 127. RELEASE_FS0B register based on WD_SEED value

WD_SEED[23:16]	B23	B22	B21	B20	B19	B18	B17	B16
RELEASE_FS0B[23:16]	**Not(B8)**	**Not(B9)**	**Not(B10)**	**Not(B11)**	**Not(B12)**	**Not(B13)**	**Not(B14)**	**Not(B15)**
WD_SEED[15:8]	B15	B14	B13	B12	B11	B10	B9	B8
RELEASE_FS0B[15:8]	**Not(B16)**	**Not(B17)**	**Not(B18)**	**Not(B19)**	**Not(B20)**	**Not(B21)**	**Not(B22)**	**Not(B23)**

31.9 Built-in self-test (BIST)

31.9.1 Logical BIST

The fail-safe state machine includes a logical built-in self-test (LBIST) to verify the correct functionality of the safety logic monitoring. The LBIST is performed after each POR, or after each wake-up from Standby. In case of LBIST fail, RSTB and PGOOD are released but FS0B remains stuck low and cannot be released. The flag LBIST_OK is available through SPI for MCU diagnostic. The typical LBIST duration is 4.2 ms and the maximum LBIST duration is 6.0 ms.

31.9.2 Analog BIST

The fail-safe state machine includes two analog built-in self-test (ABIST) to verify the correct functionality of the safety analog monitoring. ABIST1 is executed automatically after each POR, or after each wake-up from Standby. The assignment of which regulator is checked during ABIST1 is done by OTP.

ABIST2 is executed by SPI with Vxxx_ABIST2 bit after INIT_FS phase. In case of ABIST fail, RSTB and PGOOD are released but FS0B remains stuck low and cannot be released. The flags ABIST1_OK and ABIST2_OK are available through SPI for MCU diagnostic.

Table 128. ABIST coverage

Parameter	Overvoltage	Undervoltage	Short to high	Low speed	High speed	ABIST1	ABIST2
VCOREMON	X	X				OTP	SPI
VDDIO	X	X				OTP	SPI
VMONx	X	X				OTP	SPI
OSC				X	X	X	
V1p6D_FS	X					X	
PGOOD			X			X	
RSTB			X			X	
FS0B			X			X	

Table 129. ABIST2 execution bit

VCOREMON_ABIST2	VCOREMON BIST executed during ABIST2
0 (default)	**No ABIST2**
1	VCOREMON BIST executed during ABIST2
Reset condition	POR

VDDIO_ABIST2	VDDIO BIST executed during ABIST2
0 (default)	**No ABIST2**
1	VDDIO BIST executed during ABIST2
Reset condition	POR

VMONx_ABIST2	VMONx BIST executed during ABIST2
0 (default)	**No ABIST2**
1	VMONx BIST executed during ABIST2
Reset condition	POR

Table 130. Electrical characteristics

T_A = −40 °C to 125 °C, unless otherwise specified. VSUP = VSUP_UVH to 36 V, unless otherwise specified. All voltages referenced to ground.

Symbol	Parameter	Min	Typ	Max	Unit
ABIST					
$ABIST1_{TDUR}$	ABIST1 duration • MIN with **no** voltage monitoring assigned by OTP • MAX with **all** voltage monitoring assigned by OTP	0.2	—	1.2	ms
$ABIST2_{TDUR}$	ABIST2 duration • MIN with **no** voltage monitoring selected by SPI • MAX with **all** voltage monitoring selected by SPI	0.2	—	1.2	ms

32 Package information

The FS6600 package is a HVQFN56, plastic, thermally enhanced, very thin quad flat package, with no leads, a step-cut wettable flank, 56 terminals, and a 0.5 mm nominal pitch with an 8 mm x 8 mm x 0.85 mm body.

33 Package outline

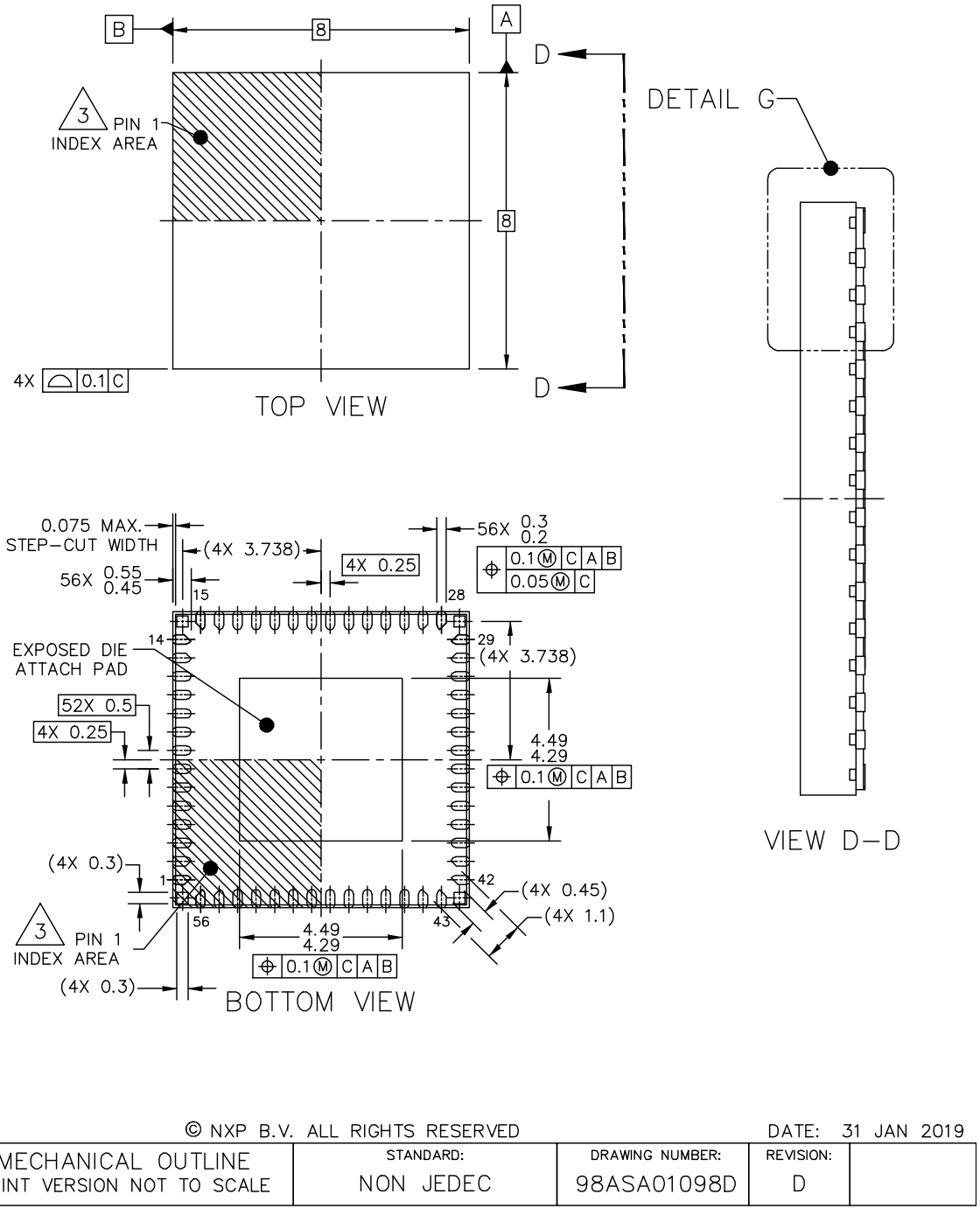
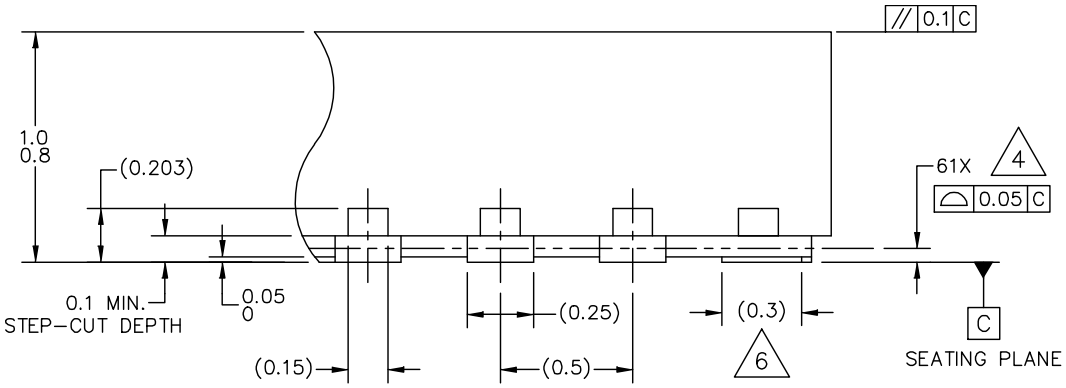


Figure 58. Package outline for HVQFN56 (SOT684-23, Step cut)

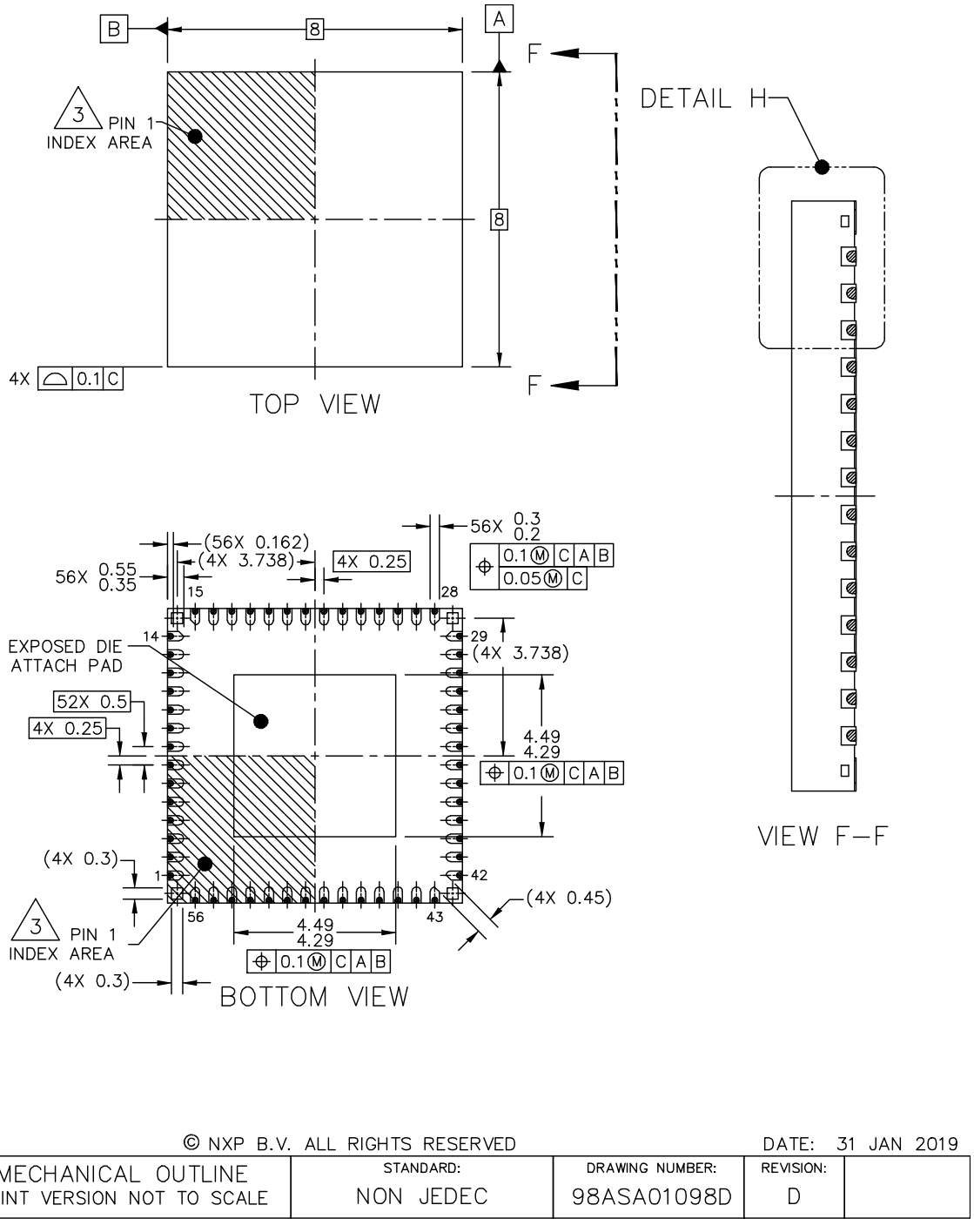


DETAIL G
VIEW ROTATED 90° CW

DATE: 31 JAN 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01098D	REVISION: D	

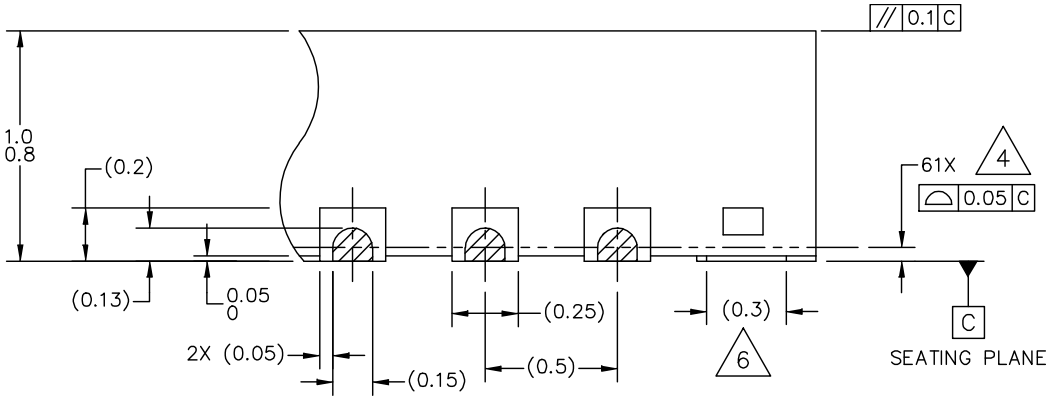
Figure 59. Package outline detail for HVQFN56 (SOT684-23, Step cut)



DATE: 31 JAN 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01098D	REVISION: D	

Figure 60. Package outline HVQFN56 (SOT684-23, Dimple)



DETAIL H
VIEW ROTATED 90° CW

DATE: 31 JAN 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01098D	REVISION: D	

Figure 61. Package outline detail for HVQFN56 (SOT684-23, Dimple)

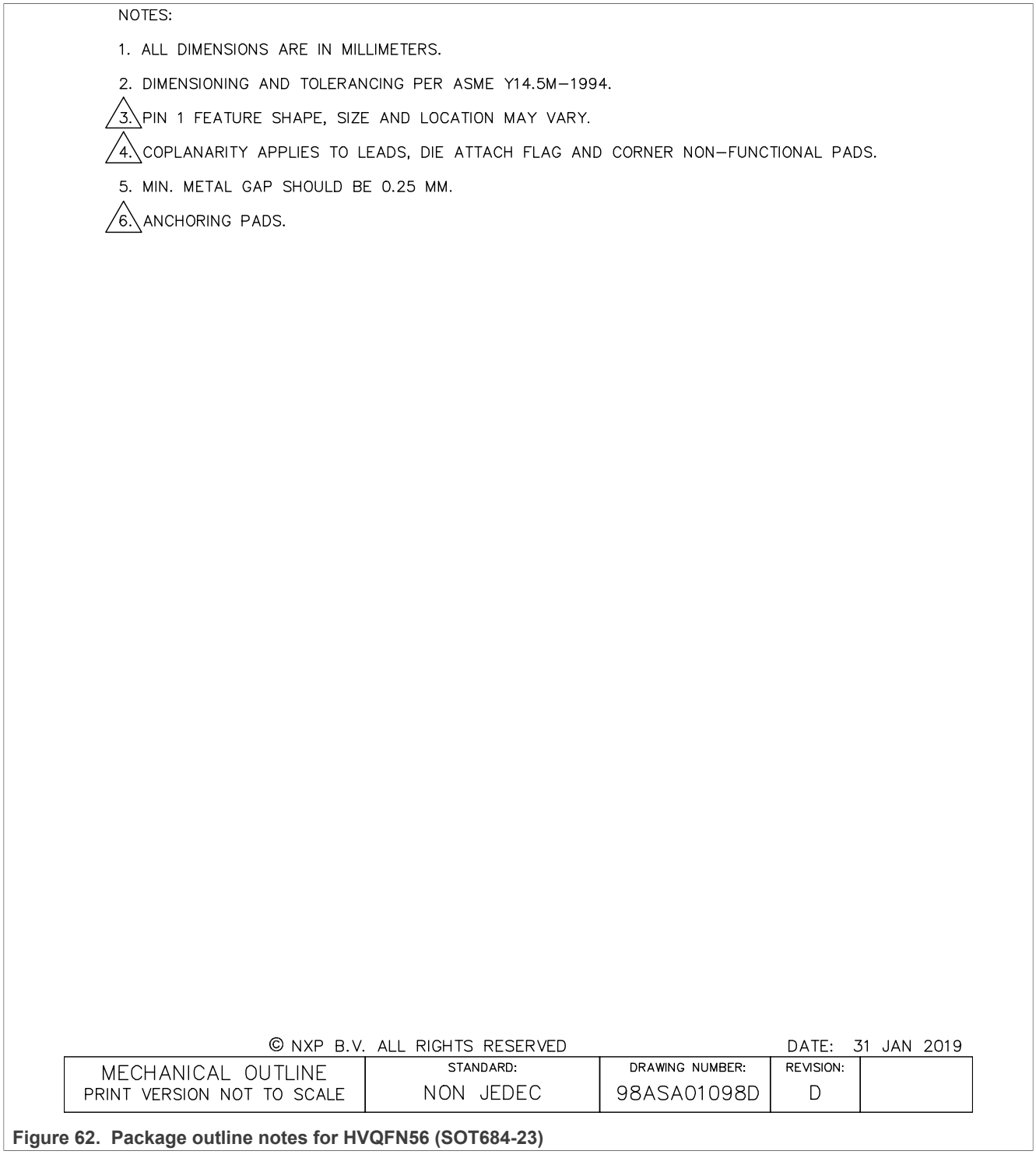
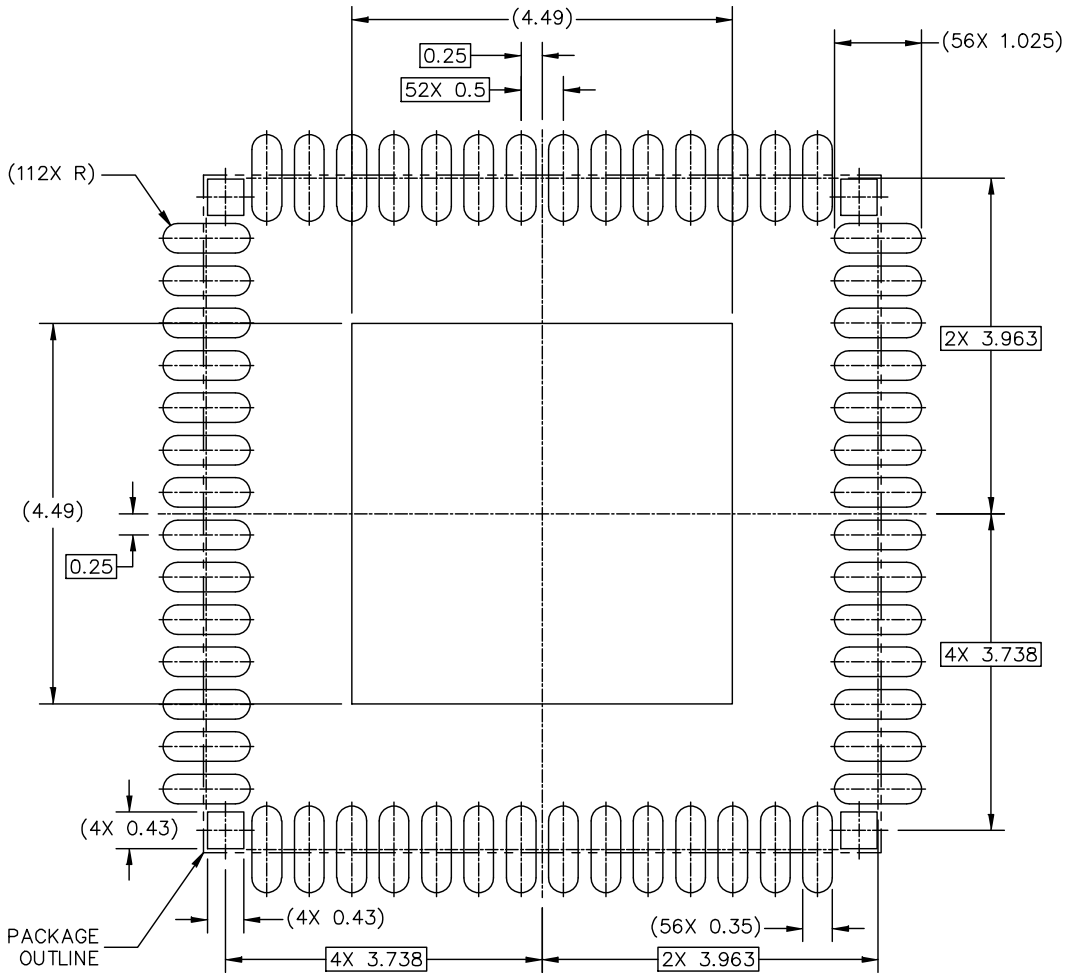


Figure 62. Package outline notes for HVQFN56 (SOT684-23)

34 Layout and PCB guidelines

34.1 Landing pad information



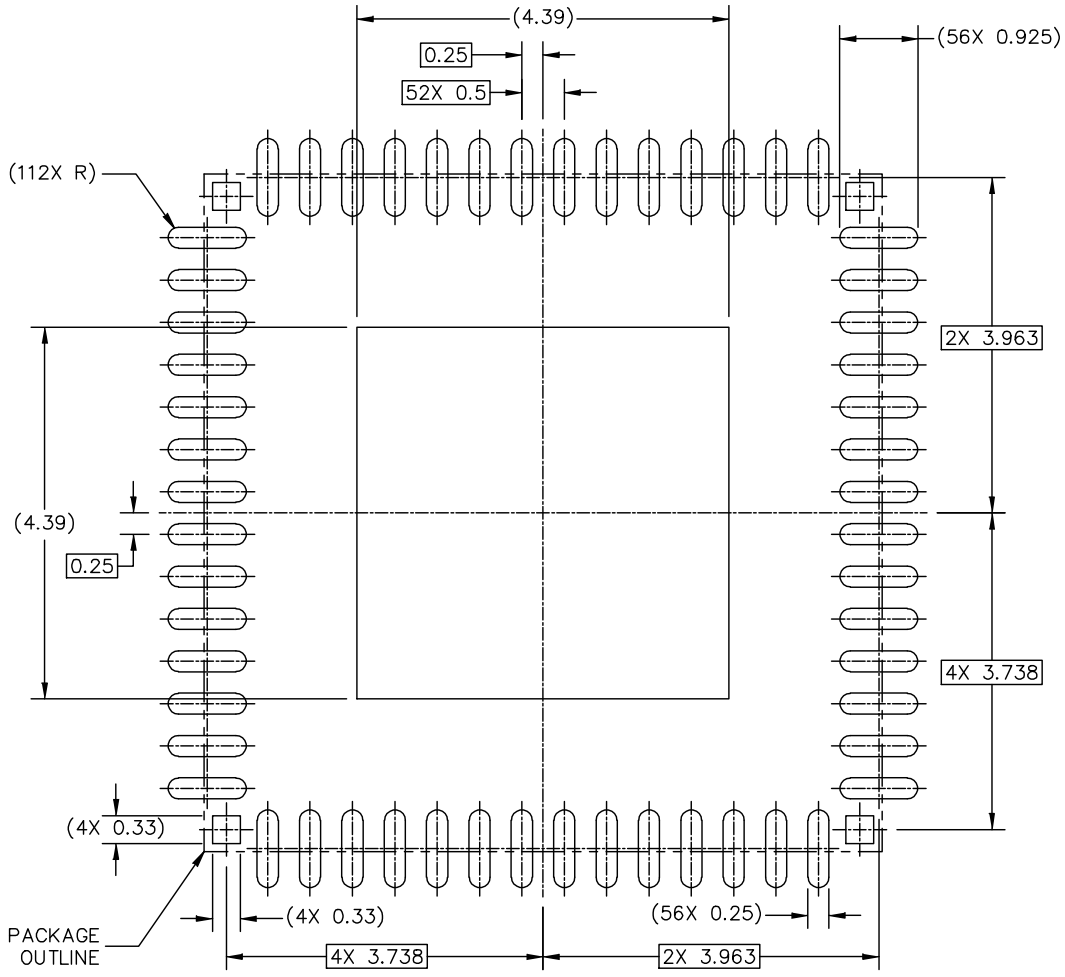
PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 31 JAN 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01098D	REVISION: D	

Figure 63. Solder mask opening pattern



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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DATE: 31 JAN 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01098D	REVISION: D	

Figure 64. I/O pads and solderable area

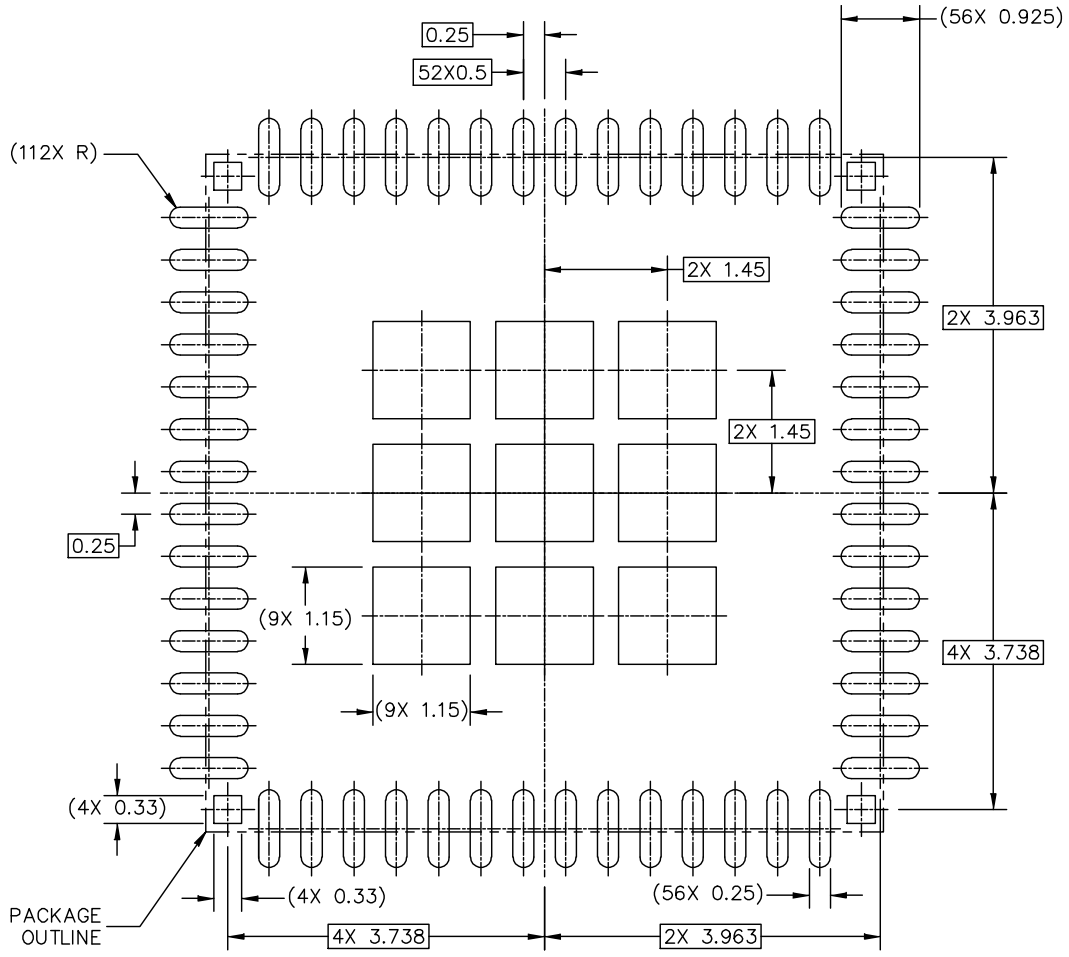


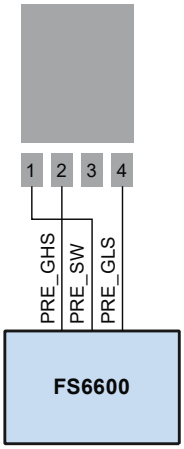
Figure 65. Solder paste stencil

34.2 Component selection

- SMPS input and output capacitors shall be chosen with low ESR (ceramic or MLCC type of capacitors). X7R ceramic type is preferred. Input decoupling capacitors shall be placed as close as possible to the device pin. Output capacitor voltage rating shall be selected to be 3x the voltage output value to minimize the DC bias degradation.
- SMPS inductors shall be shielded with ISAT higher than maximum inductor peak current.

34.3 VPRE

- Inductor charging and discharging current loop shall be designed as small as possible.
- Input decoupling capacitors shall be placed close to the high-side drain transistor pin.
- The boot strap capacitor shall be placed close to the device pin using wide and short track to connect to the external low-side drain transistor.
- PRE_GLS, PRE_GHS and PRE_SW tracks shall be wide and short and should not cross any sensitive signal (current sensing, for example).



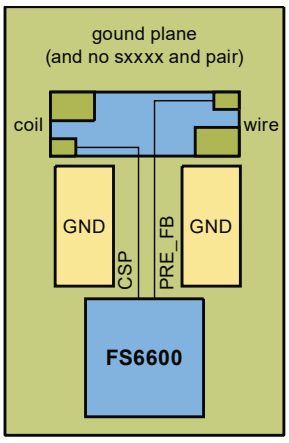
Implementation
Note : L2 is system ground.

L1 connection

L3 connection

aaa-036688

- PRE_FB used as voltage feedback AND current sense shall be connected to R_{SHUNT} and routed as a pair with CSP.



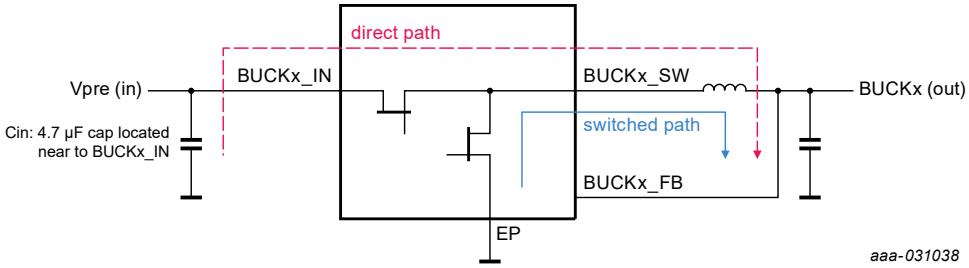
layout as a pair
do not cross any noisy signal

aaa-036689

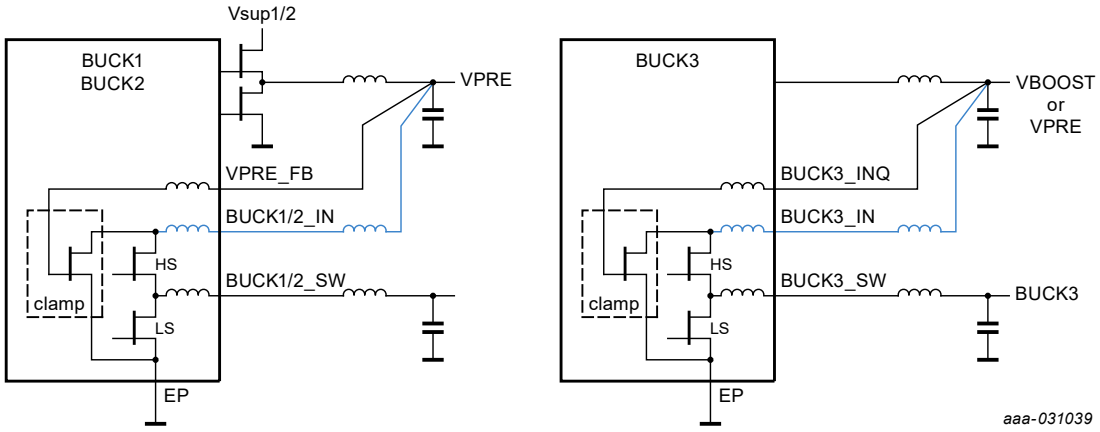
- The external transistor thermal shape should be in the range of 25 x 25 mm for optimum Rth.
- See LFPAK56 application note for more details: http://assets.nexperia.com/documents/application-note/AN10874.pdf

34.4 VBUCKx

- Inductor charging and discharging current loop shall be designed as small as possible.



- Input decoupling capacitors shall be placed close to BUCKx_IN pins.
- BUCK3_FB and BUCK3_INQ pins shall be tied to the same capacitor, VPRE or VBOOST output capacitor depending on BUCK3_IN supply selected (in the blue path below). On the PCB, the coil is parasitic from tracks. In the package, the coil is parasitic from the bonding.



35 EMC compliance

The FS6600 EMC performance is verified against BISS generic IC EMC test specification version 2.0 from 07.2012 and FMC1278 electromagnetic compatibility specification for electrical/electronic components and subsystems from 2016 with the following specific conditions:

- Conducted emission: IEC 61967-4
  - Global pins: VBAT (Vsup1 and Vsup2), WAKE1/2, FS0B, 150 ohm method, 12-M level
  - Local pins: VPRE, BUCK1/2/3, LDO1/2, VBOOST, 150 ohm method, 10-K level
- Conducted immunity: IEC 62132-4
  - Global pins: VBAT (Vsup1 and Vsup2), 36 dBm, Class A (no state change on FS0B, RSTB, PGOOD and all regulators in spec)
  - Global pins: WAKE1, WAKE2, FS0B, 30 dBm, Class A (no state change on FS0B, RSTB, PGOOD and all regulators in spec)
  - Local pins: RSTB, PGOOD, VDDIO, VBOS, 12 dBm, Class A (no state change on FS0B, RSTB, PGOOD and all regulators in spec)

  - Supply pins: VPRE, BUCK1/2/3, LDO1/2, 12 dBm, Class A (no state change on FS0B, RSTB, PGOOD and all regulators in spec)
- Radiated emission: FMC1278 from July 2015
  - Compliance with FMC1278 RE310 Level 2 requirement in Normal mode
- Radiated immunity: FMC1278 from July 2015
  - Injection level per FMC1278 RI112 Level 2 requirement in Normal mode, FS0B released and no assertion
  - Injection level per FMC1278 RI112 Level 2 requirement in Normal mode, FS0B asserted and no release
  - No wake-up when injecting FMC1278 RI112 Level 2 requirement in Standby mode

Table 131. Regulators setup for the EMC tests

VPRE	Output voltage	3.3 V
	Switching frequency	455 kHz
	Output current	3 A
BUCK1	Output voltage	1.25 V
	Switching frequency	2.22 MHz
	Output current	1.2 A
BUCK2	Output voltage	0.8 V
	Switching frequency	2.22 MHz
	Output current	1.2 A
BUCK3	Output voltage	2.3 V
	Switching frequency	2.22 MHz
	Output current	1.2 A
BOOST	Output voltage	5 V
	Switching frequency	2.22 MHz
	Output current	275 mA
LDO1	Output voltage	2.5 V
	Output current	75 mA
LDO2	Output voltage	1.1 V
	Output current	200 mA

36 References

[1] **FS85_PDTCALC**[1] — VPRE compensation network calculation and power dissipation tool (Excel file)

[2] **FS85_OTP_Mapping**[1] — OTP programming configuration (Excel file)

[3] **FS85_FMEDA**[1] — FMEDA analysis

[4] **UM11369**[1] — FS6600 functional safety manual

[5] **FS85_PCB_Apps_Note**[1] — PCB layout guidelines

[6] **FS85_VPRE_Simplis_Model**[1] — Simplis model for stability and transient simulations

[7] **Schematic**[1] — Reference schematic in Cadence and PDF formats

[8] **Layout**[1] — Reference layout in Cadence format

[9] **EVB**[1] — Evaluation board (EVB)

[10] **FlexGUI**[1] — Graphical user interface to be used with the EVB

[11] **AN12333**[1] — FS84, FS85 product guidelines application note

[1] Available upon request

37 Revision history

Table 132. Revision history

Document ID	Release date	Description
FS6600 v.3	17 July 2024	• FS6600 v.3 supersedes FS6600 v.2. • FS6600 v.3 is a product data sheet. • The formatting of FS6600 v.3 was updated to conform to new NXP document and branding guidelines including a revised revision history format and updated legal information. Also minor grammer and typographic corrections were performed globally. Prior revisions of this document required an NDA. With version 3, the FS6600 data sheet is now a public document. • Section 1, merged and revised the first two paragraphs. • Section 7.2, Table 2: MISO and MOSI descripions, removed and revised references to "Master" and "Slave" in accordance with NXP's inclusive language intitiative. • Section 27.3, revised "master" to "controller" in the second paragraph in accordance with NXP's inclusive language intitiative.. • Section 29.1, revised "master" and "slave" to "primary" and "secondary" in the first 2 bullets and revised "master" to controller in the paragraph below the table.
FS6600 v.2	9 April 2021	• FS6600 v.2 supersedes FS6600 v.1. • FS6600 v.2 is a product data sheet. • Updated disclaimer (Suitability for use – Automotive qualified functional safety products)
FS6600 v.1.1	11 March 2020	• FS6600 v.1.1 supersedes FS6600 v.1. • FS6600 v.1.1 is a product data sheet. • Section 27.3, Figure 37, replaced incorrect image of a black diagram with correct image of timing diagram.
FS6600 v.1	28 February 2020	• FS6600 v.1: Initial release. • FS6600 v.1 is a product data sheet.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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Tables

Figures

Contents