BMI7014

14 cells battery cell controller IC

Rev. 3 — 8 August 2024 Product data sheet

1 General description

The BMI7014 is a SMARTMOS lithium-ion battery cell controller IC family designed for industrial applications, such as energy storage systems (ESS) and uninterruptible power supply (UPS) systems.

The device performs ADC conversions of the differential cell voltages and battery temperature measurements. The information is transmitted to MCU using one of the microcontroller interfaces (serial peripheral interface (SPI) or transformer physical layer (TPL)) of the IC.

2 Features

- 9.6 V ≤ V_{PWR} ≤ 63 V operation, 75 V transient
- 7 to 14 cells management
- Isolated 2.0 Mbps differential communication or 4.0 Mbps SPI
- Addressable on initialization
- Bidirectional transceiver to support up to 63 nodes in daisy chain
- 0.8 mV maximum total voltage measurement error
- Averaging of cell voltage measurements
- Total stack voltage measurement
- Seven GPIO/temperature sensor inputs
- 5.0 V at 5.0 mA reference supply output
- Automatic over/undervoltage and temperature detection routable to fault pin
- Integrated sleep mode over/undervoltage and temperature monitoring
- Onboard 300 mA passive cell balancing with diagnostics
- Hot plug capable
- Detection of internal and external faults, as open lines, shorts, and leakages

3 Simplified application diagram

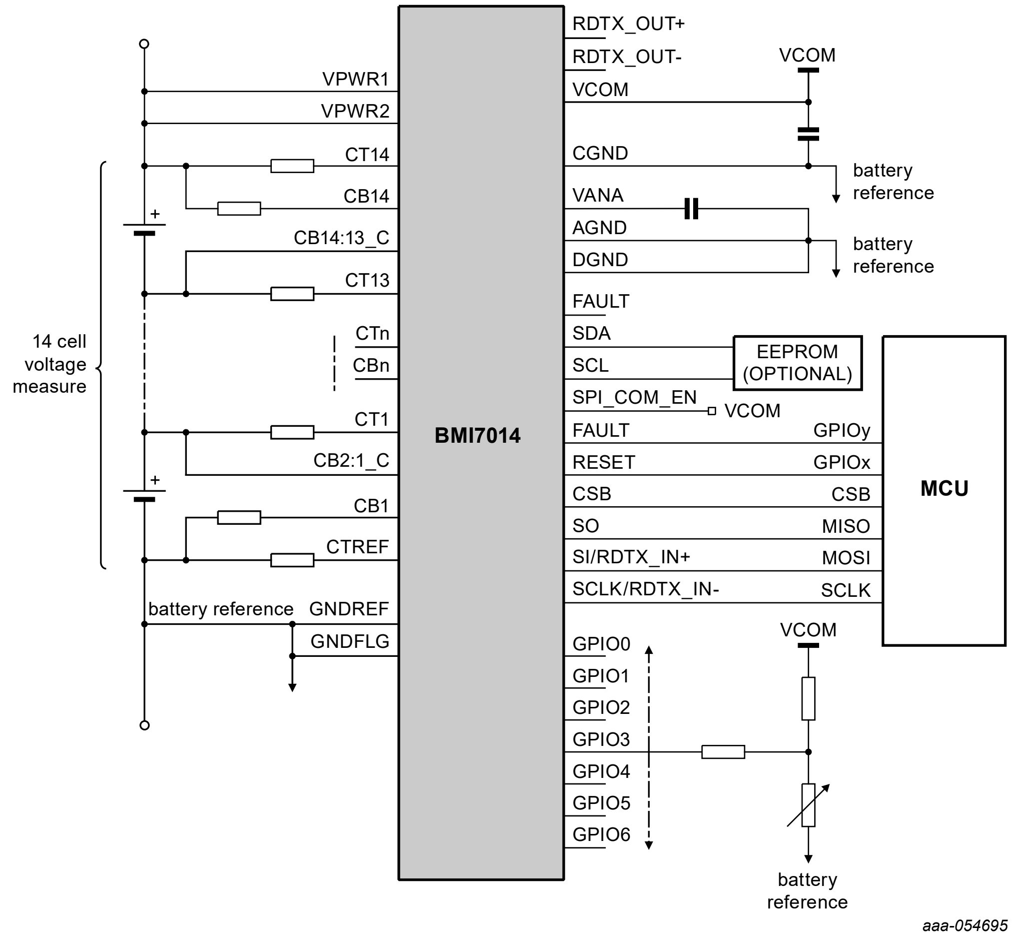


Figure 1. Simplified application diagram, SPI use case

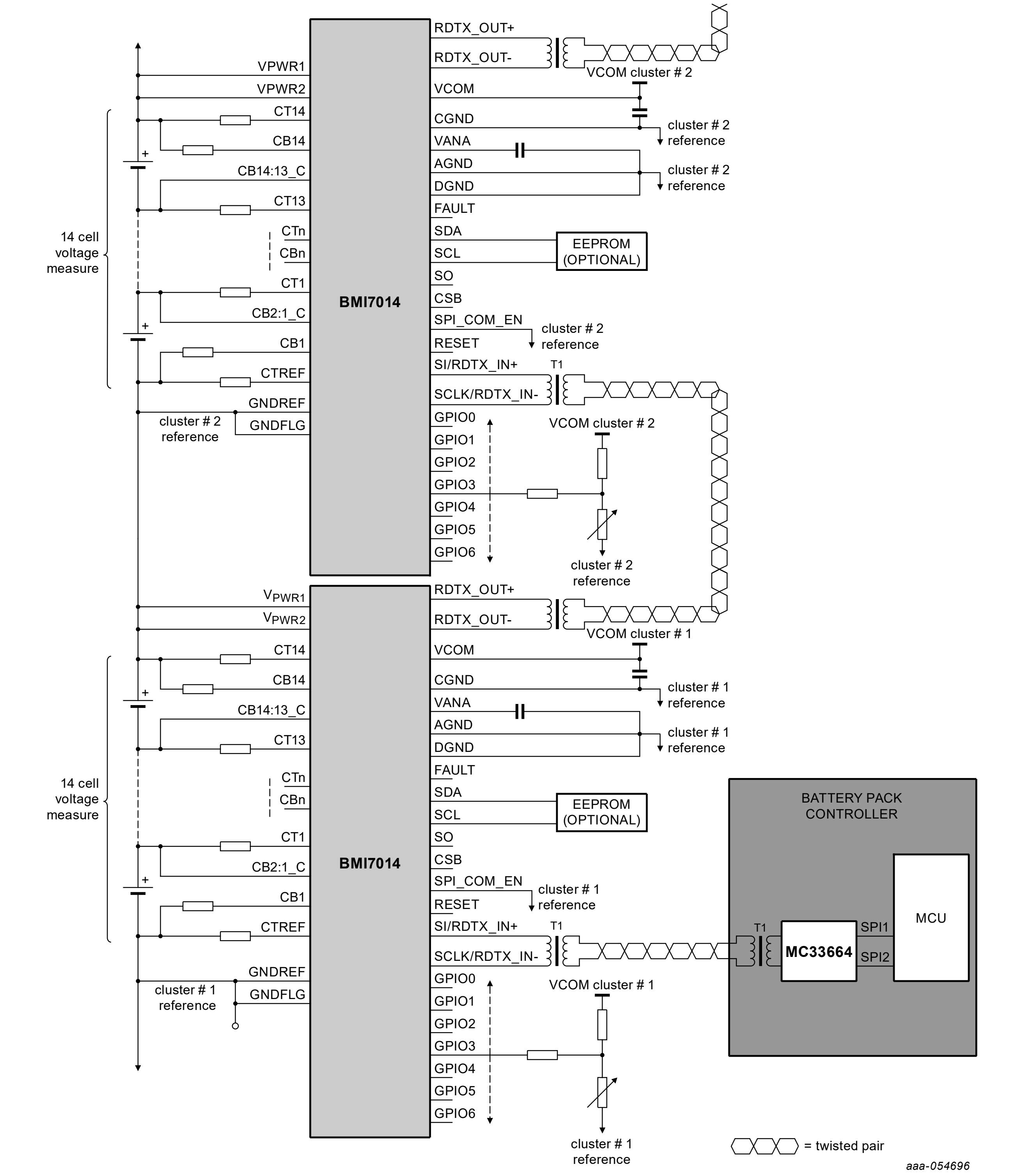


Figure 2. Simplified application diagram, TPL use case

4 Applications

- Energy storage systems
- Uninterruptible power supply (UPS)

5 Ordering information

5.1 Part numbers definition

MBMI7014 T A y AE/R2

Table 1. Part number breakdown

Code	Option	Description
	T	TPL communication type
	A	A (silicon revision)
y	1	y = 1 (Premium accuracy performance)
		y = 2 (Standard accuracy performance)
	AE	Package suffix
	R2	Tape and reel indicator

5.2 Part numbers list

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com.

Table 2. Advanced orderable part table

Temperature range is –20 °C to 85 °C

Package type is 64-pin LQFP-EP

Orderable part	Description
BMI7014TA1AE	Premium cell voltage accuracy performances
BMI7014TA2AE	Standard cell voltage accuracy performances

6 Internal block diagram

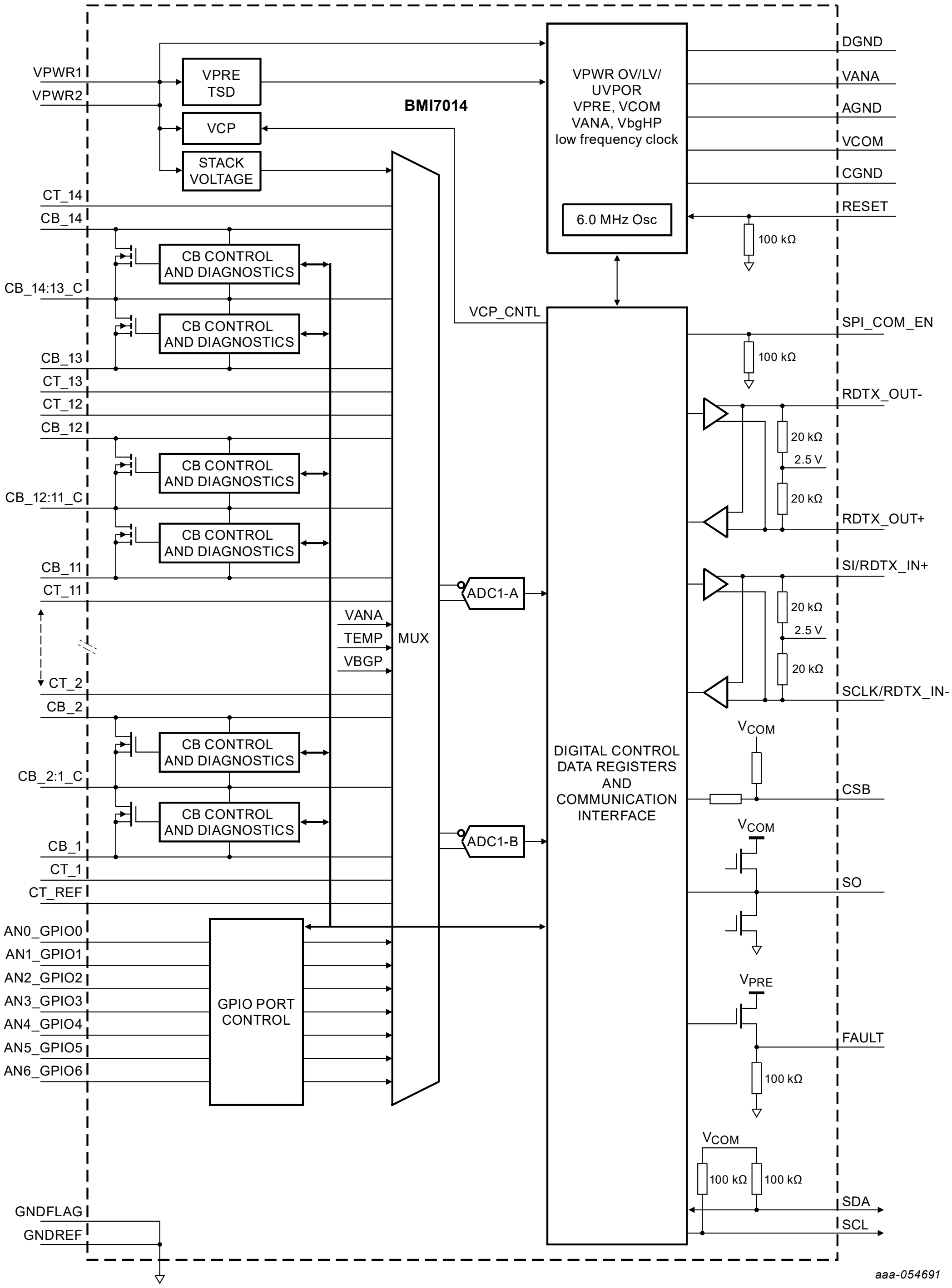


Figure 3. Simplified internal block diagram

7 Pinning information

7.1 Pinout diagram

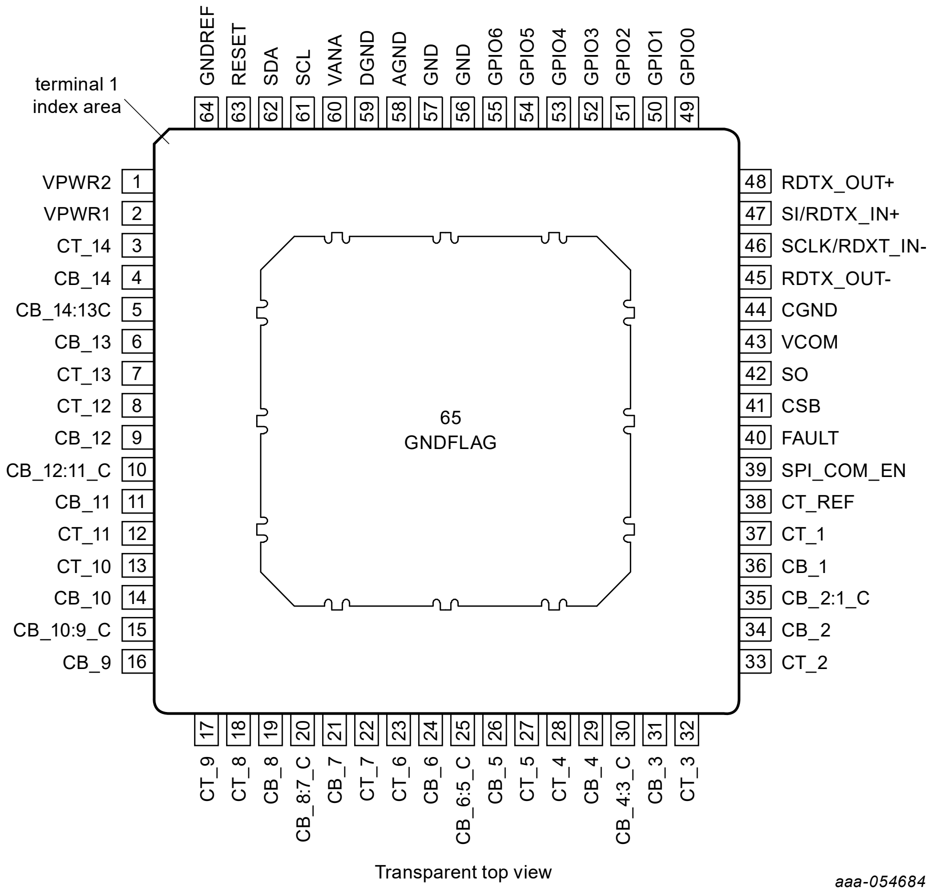


Figure 4. Pinout diagram

7.2 Pin definitions

Table 3. Pin definitions

Number	Name	Function	Definition
1	VPWR2	Input	Power input to the BMI7014
2	VPWR1	Input	Power input to the BMI7014
3	CT_14	Input	Cell pin 14 input. Terminate to LPF resistor.
4	CB_14	Output	Cell balance driver. Terminate to cell 14 cell balance load resistor.
5	CB_14:13_C	Output	Cell balance 14:13 common. Terminate to CB_14:13_C balance load resistor.
6	CB_13	Output	Cell balance driver. Terminate to cell 13 cell balance load resistor.
7	CT_13	Input	Cell pin 13 input. Terminate to LPF resistor.
8	CT_12	Input	Cell pin 12 input. Terminate to LPF resistor.
9	CB_12	Output	Cell balance driver. Terminate to cell 12 cell balance load resistor.

Table 3. Pin definitions*...continued*

Number	Name	Function	Definition
10	CB_12:11_C	Output	Cell balance 12:11 common. Terminate to CB_12:11_C balance load resistor.
11	CB_11	Output	Cell balance driver. Terminate to cell 11 cell balance load resistor.
12	CT_11	Input	Cell pin 11 input. Terminate to LPF resistor.
13	CT_10	Input	Cell pin 10 input. Terminate to LPF resistor.
14	CB_10	Output	Cell balance driver. Terminate to cell 10 cell balance load resistor.
15	CB_10:9_C	Output	Cell balance 10:9 common. Terminate to CB_10:9_C balance load resistor.
16	CB_9	Output	Cell balance driver. Terminate to cell 9 cell balance load resistor.
17	CT_9	Input	Cell pin 9 input. Terminate to LPF resistor.
18	CT_8	Input	Cell pin 8 input. Terminate to LPF resistor.
19	CB_8	Output	Cell balance driver. Terminate to cell 8 cell balance load resistor.
20	CB_8:7_C	Output	Cell balance 8:7 common. Terminate to CB_8:7_C balance load resistor.
21	CB_7	Output	Cell balance driver. Terminate to cell 7 cell balance load resistor.
22	CT_7	Input	Cell pin 7 input. Terminate to LPF resistor.
23	CT_6	Input	Cell pin 6 input. Terminate to LPF resistor.
24	CB_6	Output	Cell balance driver. Terminate to cell 6 cell balance load resistor.
25	CB_6:5_C	Output	Cell balance 6:5 common. Terminate to CB_6:5_C balance load resistor.
26	CB_5	Output	Cell balance driver. Terminate to cell 5 cell balance load resistor.
27	CT_5	Input	Cell pin 5 input. Terminate to LPF resistor.
28	CT_4	Input	Cell pin 4 input. Terminate to LPF resistor.
29	CB_4	Output	Cell balance driver. Terminate to cell 4 cell balance load resistor.
30	CB_4:3_C	Output	Cell balance 4:3 common. Terminate to CB_4:3_C balance load resistor.
31	CB_3	Output	Cell balance driver. Terminate to cell 3 cell balance load resistor.
32	CT_3	Input	Cell pin 3 input. Terminate to LPF resistor.
33	CT_2	Input	Cell pin 2 input. Terminate to LPF resistor.
34	CB_2	Output	Cell balance driver. Terminate to cell 2 cell balance load resistor.
35	CB_2:1_C	Output	Cell Balance 2:1 common. Terminate to CB_2:1_C balance load resistor.
36	CB_1	Output	Cell balance driver. Terminate to cell 1 cell balance load resistor.
37	CT_1	Input	Cell pin 1 input. Terminate to LPF resistor.
38	CT_REF	Input	Cell pin REF input. Terminate to LPF resistor.
39	SPI_COM_EN	Input	SPI communication enable. Pin must be high for the SPI to be active.
40	FAULT	Output	Fault output dependent on user defined internal or external faults. If not used, it must be left open.
41	CSB	Input	SPI chip select
42	SO	Output	SPI serial output
43	VCOM	Output	Communication regulator output

Table 3. Pin definitions*...continued*

Number	Name	Function	Definition
44	CGND	Ground	Communication decoupling ground. Terminate to GNDREF.
45	RDTX_OUT-	I/O	Receive/transmit output negative
46	SCLK/RDTX_IN-	I/O	SPI clock or receive/transmit input negative
47	SI/RDTX_IN+	I/O	SPI serial input or receive/transmit input positive
48	RDTX_OUT+	I/O	Receive/transmit output positive
49	GPIO0	I/O	General purpose analog input or GPIO or wake-up or fault daisy chain
50	GPIO1	I/O	General purpose analog input or GPIO
51	GPIO2	I/O	General purpose analog input or GPIO or conversion trigger
52	GPIO3	I/O	General purpose analog input or GPIO
53	GPIO4	I/O	General purpose analog input or GPIO
54	GPIO5	I/O	General purpose analog input or GPIO
55	GPIO6	I/O	General purpose analog input or GPIO
56	GND	Ground	Ground
57	GND	Ground	Ground
58	AGND	Ground	Analog ground, terminate to GNDREF
59	DGND	Ground	Digital ground, terminate to GNDREF
60	VANA	Output	Precision ADC analog supply
61	SCL	I/O	I^2C clock
62	SDA	I/O	I^2C data
63	RESET	Input	RESET is an active high input. RESET has an internal pull down. If not used, it can be tied to GND.
64	GNDREF	Ground	Ground reference for device. Terminate to reference of battery cluster.
65	GNDFLAG	Ground	Device flag. Terminate to lowest potential of battery cluster.

8 General product characteristics

8.1 Ratings and operating requirements relationship

The operating voltage range pertains to the VPWR pins referenced to the AGND pins.

Table 4. Ratings vs. operating requirements

Fatal range • Permanent failure might occur	Handling range – no permanent failure			Fatal range • Permanent failure might occur
	Lower limited operating range • No permanent failure, but IC functionality is not guaranteed	Normal operating range • 100 % functional	Upper limited operating range • IC parameters might be out of specification • Detection of V_{PWR} overvoltage is functional	
V_{PWR} < −0.3 V	7.6 V ≤ V_{PWR} < 9.6 V **Reset range:** –0.3 V ≤ V_{PWR} < 7.6 V	9.6 V ≤ V_{PWR} ≤ 63 V	63 V < V_{PWR} ≤ 75 V	75 V < V_{PWR}

In both upper and lower limited operating range, no information can be provided about IC performance. Only the detection of V_{PWR} overvoltage is guaranteed in the upper limited operating range.

Performance in normal operating range is guaranteed only if there is a minimum of seven battery cells in the stack.

8.2 Maximum ratings

Table 5. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit
Electrical ratings				
VPWR1, VPWR2	Supply input voltage	−0.3	75	V
CT14	Cell terminal voltage	−0.3	75	V
VPWR to CT14	Voltage across VPWR1,2 pins pair and CT14 pin	−10	10.5	V
CT_N to CT_{N-1}	Cell terminal differential voltage [1]	−0.3	6.0	V
CT_{REF} to GND	Cell terminal reference to ground	—	5	V
CT_N to GND	Cell terminal voltage to ground (N = 1 to 4 or N = 6 to 14)	—	(N+1) * 5	V
	Cell terminal voltage to ground (N = 5)	—	27.5	V
$CT_{N(CURRENT)}$	Cell terminal input current	—	±500	μA
CB_N to $CB_{N:N-1\_C}$ $CB_{N:N-1\_C}$ to CB_{N-1}	Cell balance differential voltage	—	10	V
CB_{2n} to GND	Cell balance voltage to GND (n = 1 to 7)	—	(2n+1) . 5	V
CB_{2n+1} to GND	Cell balance voltage to GND (n = 0 to 6)	—	(2n+1) . 5	V
$CB_{2n:2n-1\_C}$ to GND	Cell balance voltage to GND (n = 1 to 6)	—	2n . 5	V
$CB_{N:N-1\_C}$ to CTn-1	Cell balance input to cell terminal input	−10	10	V
VCOM	Maximum voltage may be applied to VCOM pin from external source	—	5.8	V
VANA	Maximum voltage may be applied to VANA pin	—	3.1	V
V_{GPIO0}	GPIO0 pin voltage	–0.3	6.5	V
V_{GPIOx}	GPIOx pins (x = 1 to 6) voltage	–0.3	VCOM + 0.5	V
V_{DIG}	Voltage I^2C pins (SDA, SCL)	–0.3	VCOM + 0.5	V
V_{RESET}	RESET pin	–0.3	6.5	V
V_{CSB}	CSB pin	–0.3	6.5	V
$V_{SPI\_COMM\_EN}$	SPI_COMM_EN	–0.3	6.5	V
V_{SO}	SO pin	–0.3	VCOM + 0.5	V
FAULT	Maximum applied voltage to pin	−0.3	7.0	V
$I_{pin\_unpowered}$	Input current in a pin when the device is unpowered	–2	2	mA

Table 5. Maximum ratings*...continued*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit
V_{COMM}	Maximum voltage to pins RDTX_OUT+, RDTX_OUT–, SI/RDTX_IN+, SCLK/RDTX_IN-	−10.0	10.0	V
V_{ESD1}	ESD voltage Human body model (HBM) Charge device model (CDM) Charge device model corner pins (CDM)	 — — —	 ±2000 ±500 [2] ±750	V
V_{ESD2}	ESD voltage (VPWR1, VPWR2, CTx, CBx, GPIOx, RDTX_OUT+, RDTX_OUT−, SI/RDTX_IN+, SCLK/RDTX_IN−) versus all ground pins [3] Human body model (HBM)	—	±4000	V
V_{ESD3}	ESD voltage (CTREF, CTx, CBx, GPIOx, RDTX_OUT+, RDTX_OUT−, SI/RDTX_IN+, SCLK/ RDTX_IN−) [4] IEC 61000-4-2, Unpowered (Gun configuration: 330Ω / 150pF) HMM, Unpowered (Gun configuration: 330Ω / 150pF) ISO 10605:2009, Unpowered (Gun configuration: 2 kΩ / 150pF) ISO 10605:2009, Powered (Gun configuration: 2 kΩ / 150pF)	 — — — —	 ±8000 ±8000 ±8000 ±8000	V

[1] Adjacent CT pins may experience an overvoltage that exceeds their maximum rating during OV/UV functional verification test or during open line diagnostic test. Nevertheless, the IC is completely tolerant to this special situation.
[2] For CT_REF pin applicable limit is ±450 V.
[3] ESD testing is performed in accordance with the human body model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the charge device model (CDM) (C_{ZAP} = 4.0 pF).
[4] These voltage values can be sustained only if ESD caps are used as described in Section 12.2

8.3 Thermal characteristics

Table 6. Thermal ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit
Thermal ratings				
T_J	Operating temperature Junction[1]	−40	+150	°C
T_{STG}	Storage temperature	−55	+150	°C
T_{PPRT}	Peak package reflow temperature [2][3]	—	260	°C
Thermal resistance and package dissipation ratings				
$R_{\Theta JB}$	Junction-to-board (bottom exposed pad soldered to board) 64 LQFP EP [4]	—	10	°C/W
$R_{\Theta JA}$	Junction-to-ambient, natural convection, single-layer board (1s) 64 LQFP EP [5][6]	—	59	°C/W
$R_{\Theta JA}$	Junction-to-ambient, natural convection, four-layer board (2s2p) 64 LQFP EP [5][6]	—	27	°C/W
$R_{\Theta JCTOP}$	Junction-to-case top (exposed pad) 64 LQFP EP [7]	—	14	°C/W
$R_{\Theta JCBOTTOM}$	Junction-to-case bottom (exposed pad) 64 LQFP EP [8]	—	0.97	°C/W
Ψ_{JT}	Junction to package top, natural convection [9]	—	3	°C/W

[1] The user must ensure that the average maximum operating junction temperature (TJ) is not exceeded.

[2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
[3] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts and review parametrics.
[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[5] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[6] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
[7] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1), with the cold plate temperature used for the case temperature.
[8] Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
[9] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

8.4 Electrical characteristics

Table 7. Static and dynamic electrical characteristics

Characteristics noted under conditions 9.6 V ≤ V_{PWR} ≤ 63 V, −20 °C ≤ T_J ≤ 85 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 56 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
Power management					
$V_{PWR(FO)}$	Supply voltage Full parameter specification	9.6	—	63	V
I_{VPWR}	Supply current (base value) Normal mode, cell balance OFF, ADC inactive, SPI communication inactive, IVCOM = 0 mA Normal mode, cell balance OFF, ADC inactive, TPL communication inactive, IVCOM = 0 mA	— —	5.4 8.0	8.5 10.0	mA
$I_{VPWR(TPL\_TX)}$	Supply current adder when TPL communication active	—	—	16	mA
$I_{VPWR(CBON)}$	Supply current adder to set all 14 cell balance switches ON	—	0.97	—	mA
$I_{VPWR(ADC)}$	Delta supply current to perform ADC conversions (addend) [1] ADC1-A,B continuously converting	—	3.0	5.0	mA
$I_{VPWR(SS)}$	Supply current in sleep mode and in idle mode, communication inactive, cell balance off, cyclic measurement off, oscillator monitor on [2] SPI mode (T_A = 25 °C) SPI mode (T_A = −20 °C to 60 °C) BMI7014TA1 SPI mode (T_A = −20 °C to 60 °C) BMI7014TA2 TPL mode (T_A = 25 °C) TPL mode (T_A = −20 °C to 60 °C)	— — — 64 54	40 — — — —	— 75 110 108 115	µA
$I_{VPWR(CKMON)}$	Clock monitor current consumption	—	5	8	µA
V_{VPWR_CT}	Voltage drop across CT14 and VPWR without accuracy degradation [3] 3.0 V ≤ V_{CELL} 2.5 V ≤ V_{CELL} < 3.0 V V_{CELL} < 2.5 V	−3.0 −2.0 −1.5	— — —	3.0 2.0 1.5	V
$V_{PWR(OV\_FLAG)}$	V_{PWR} overvoltage fault threshold (flag)	63	65	68	V
$V_{PWR(LV\_FLAG)}$	V_{PWR} low-voltage warning threshold (flag)	11.7	12	12.3	V
$V_{PWR(UV\_POR)}$	V_{PWR} undervoltage shutdown threshold (POR)	7.6	8.5	9.6	V
$V_{PWR(HYS)}$	V_{PWR} UV hysteresis voltage	100	200	—	mV
$t_{VPWR(FILTER)}$	V_{PWR} OV, LV filter	—	50	—	µs

Table 7. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions 9.6 V ≤ V_{PWR} ≤ 63 V, −20 °C ≤ T_J ≤ 85 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 56 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
VCOM power supply					
V_{COM}	VCOM output voltage	4.9	5.0	5.2	V
I_{VCOM}	VCOM output current allocated for external use	—	—	5.0	mA
$V_{COM(UV)}$	VCOM undervoltage fault threshold	4.2	4.4	4.6	V
V_{COM_HYS}	VCOM undervoltage hysteresis	—	100	—	mV
$t_{VCOM(FLT\_TIMER)}$	VCOM undervoltage fault timer	—	10	—	μs
$t_{VCOM(RETRY)}$	VCOM fault retry timer	—	10	—	ms
$V_{COM(OV)}$	VCOM overvoltage fault threshold	5.4	—	5.9	V
$I_{LIM\_VCOM(OC)}$	VCOM current limit	65	—	140	mA
$R_{VCOM(SS)}$	VCOM sleep mode pulldown resistor	1.0	2.0	5.0	kΩ
t_{VCOM}	VCOM rise time (for V_{PWR} > 10V and CL = 2.2 μF (ceramic X7R only) in parallel with 220 pF) [4]	—	—	440	μs
VANA power supply					
V_{ANA}	VANA output voltage (not used by external circuits) Decouple with 47 nF X7R 0603 or 0402	2.6	2.65	2.7	V
$V_{ANA(UV)}$	VANA undervoltage fault threshold	2.28	2.4	2.5	V
V_{ANA_HYS}	VANA undervoltage hysteresis	—	50	—	mV
$V_{ANA(FLT\_TIMER)}$	VANA undervoltage fault timer	—	11	—	μs
$V_{ANA(OV)}$	VANA overvoltage fault threshold	2.77	2.8	2.85	V
$t_{VANA(RETRY)}$	VANA fault retry timer	—	10	—	ms
$I_{LIM\_VANA(OC)}$	VANA current limit	5.0	—	10	mA
R_{VANA_RPD}	VANA sleep mode pulldown resistor	—	1.0	—	kΩ
t_{VANA}	VANA rise time (CL = 47 nF ceramic X7R only) [4]	—	—	400	μs
ADC1-A, ADC1-B					
$CTn_{(LEAKAGE)}$	Cell terminal input leakage current (except in Sleep mode when cell balancing is ON)	—	10	100 —	nA
$CTn_{(FV)}$	Cell terminal input current - functional verification	—	0.365	0.5	mA
CT_N	Cell terminal input current during conversion	—	50	—	nA
R_{PD}	Cell terminal open load detection pulldown resistor	850	950	1250	Ω
V_{VPWR_RES}	VPWR terminal measurement resolution	—	2.44141	—	mV/LSB
V_{VPWR_RNG}	VPWR terminal measurement range	9.6	—	75	V
$VPWR_{TERM\_ERR}$	VPWR terminal measurement accuracy	−0.5	—	0.5	%
V_{CT_RNG}	ADC differential input voltage range for CTn to CTn-1 [5]	0.0	—	4.85	V
$V_{CT\_ANx\_RES}$	Cell voltage and ANx resolution in 15-bit MEAS_xxxx registers	—	152.58789	—	μV/LSB
$V_{ANx\_RATIO\_RES}$	ANx resolution in 15-bit MEAS_xxxx registers in ratiometric mode	—	VCOM. (30.51758)	—	μV/LSB
$V_{ERR33RT\_BMI7014TA1}$	Cell voltage measurement error [6][7] V_{CELL} = 3.3 V, T_A = 25 °C	−0.8	±0.4	0.8	mV
$V_{ERR33rt\_1\_BMI7014TA2}$	Cell voltage measurement error [6][7] V_{CELL}= 3.3 V , T_A = 25 °C	−1.0	—	1.0	mV

Table 7. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions 9.6 V ≤ V_{PWR} ≤ 63 V, −20 °C ≤ T_J ≤ 85 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 56 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
$V_{ERR\_1\_BMI7014TA1}$	Cell voltage measurement error [6][7][8] 0.1 V ≤ V_{CELL} ≤ 4.3 V, −20 °C ≤ T_J ≤ 85 °C	−3.0	±1.0	3.0	mV
$V_{ERR\_1\_BMI7014TA2}$	Cell voltage measurement error [6][7][8] 0.1 V ≤ V_{CELL} ≤ 4.3 V , -20 °C ≤ Tj ≤ 85 °C	–9.0	–	9.0	mV
$V_{ERR\_2\_BMI7014TA2}$	Cell voltage measurement error [6][7][8] 0.1 V ≤ V_{CELL} ≤ 3.7 V , 0 °C ≤ Tj ≤ 65 °C	–5.0	–	5.0	mV
$V_{ERR\_A\_BMI7014TA1}$	Cell voltage measurement error [6][8][9] after aging, 0.1 V ≤ V_{CELL} ≤ 4.3 V, −20 °C ≤ T_J ≤ 85 °C	–5.0	±1.0	5.0	mV
V_{ANx_ERR}	Magnitude of ANx error in the entire measurement range: [6][9] Ratiometric measurement Absolute measurement after soldering and aging, input in the range [1.0, 4.5] V Absolute measurement after soldering and aging, input in the range [0, 4.85] V, for –40 °C < T_A < 60 °C	 — — –8.0	 — — —	 16 10 8.0	mV
t_{VCONV}	Single channel net conversion time 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	 — — — —	 6.77 9.43 14.75 25.36	 — — — —	µs
V_{V_NOISE}	Conversion noise 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	 — — — —	 1800 1000 600 400	 — — — —	µVrms
ADC_{CLK}	ADC1-A,B clocking frequency	5.7	6.0	6.3	MHz
Diagnostic thresholds					
V_{OL_DETECT}	Cell terminal open load V detection threshold [10] 1.5 V ≤ V_{CELL} ≤ 2.7 V 2.5 V ≤ V_{CELL} ≤ 3.7 V 2.5 V ≤ V_{CELL} ≤ 4.3 V	 — — —	 50 100 150	 — — —	mV
V_{LEAK}	Cell terminal leakage detection level [6]	−27	—	27	mV
V_{REF_ZD}	Precision diagnostic Zener reference for cell voltage channel functional verification [6]	4.45	4.6	4.85	V
V_{CVFV}	Cell voltage channel functional verification allowable error in CT verification measurement [6]	−22	—	6.0	mV
V_{BGP}	Voltage reference used in ADC1-A,B functional verification	—	1.18	—	V
$ADC1a_{FV}$, $ADC1b_{FV}$	ADC1-A and ADC1-B functional verification Maximum tolerance between ADC1-A, B and diagnostic reference (1.5 V ≤ V_{CELL} ≤ 4.3 V)	−5.25	—	5.25	mV
CTx_UV_TH	Undervoltage functional verification threshold in Diagnostic mode [10] 1.5 V ≤ V_{CELL} ≤ 2.7 V 2.5 V ≤ V_{CELL} ≤ 3.7 V 2.5 V ≤ V_{CELL} ≤ 4.3 V	 390 650 1200	 — — —	 — — —	mV
CTx_OV_TH	Overvoltage functional verification threshold in Diagnostic mode [10] 1.5 V ≤ V_{CELL} ≤ 2.7 V 2.5 V ≤ V_{CELL} ≤ 3.7 V 2.5 V ≤ V_{CELL} ≤ 4.3 V	 — — —	 — — —	 1800 4000 4000	mV

Table 7. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions 9.6 V ≤ V_{PWR} ≤ 63 V, −20 °C ≤ T_J ≤ 85 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 56 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
Cell balance drivers					
$V_{DS(CLAMP)}$	Cell balance driver VDS active clamp voltage	10	11	12	V
$V_{OUT(FLT\_TH)}$	Output fault detection voltage threshold Balance off (open load) Balance on (shorted load)	0.3	0.55	0.75	V
R_{PD_CB}	Output OFF open load detection pulldown resistor Balance off, open load detect disabled	1.7	2.0	2.9	kΩ
$I_{OUT(LKG)}$	Output leakage current Balance off, open load detect disabled at V_{DS} = 4.0 V	—	—	1.0	μA
$R_{DS(on)}$	Drain-to-source on resistance I_{OUT} = 300 mA, T_J = 85 °C I_{OUT} = 300 mA, T_J = 25 °C I_{OUT} = 300 mA, T_J = −20 °C	 — — —	 — 0.5 0.4	 0.80 — —	Ω
I_{LIM_CB}	Driver current limitation	310	—	950	mA
t_{ON}	Cell balance driver turn on R_L = 15 Ω	—	350	450	μs
t_{OFF}	Cell balance driver turn off R_L = 15 Ω	—	200	—	μs
$t_{BAL\_DEGLICTH}$	Short/open detect filter time	19	20	42.1	μs
Internal temperature measurement					
IC_TEMP1_ERR	IC temperature measurement error	−3.0	—	3.0	K
IC_TEMP1_RES	IC temperature resolution	—	0.032	—	K/LSB
TSD_TH	Thermal shutdown	155	170	185	°C
TSD_HYS	Thermal shutdown hysteresis	5.0	10	12.2	°C
Default operational parameters					
$V_{CTOV(TH)}$	Cell overvoltage threshold (8 bits), typical value is default value after RESET	0.0	4.2	5.0	V
$V_{CTOV(RES)}$	Cell overvoltage threshold resolution	—	19.53125	—	mV/LSB
$V_{CTUV(TH)}$	Cell undervoltage threshold (8 bits), typical value is default value after RESET	0.0	2.5	5.0	V
$V_{CTUV(RES)}$	Cell undervoltage threshold resolution	—	19.53125	—	mV/LSB
$V_{GPIO\_OT(TH)}$	GPIOx configured as ANx input overtemperature threshold after RESET	—	1.16	—	V
$V_{GPIO\_OT(RES)}$	Temperature voltage threshold resolution	—	4.8828125	—	mV/LSB
$V_{GPIO\_UT(TH)}$	GPIOx configured as ANx input undertemperature threshold after RESET	—	3.82	—	V
$V_{GPIO\_UT(RES)}$	Temperature voltage threshold resolution	—	4.8828125	—	mV/LSB
General purpose input/output GPIOx					
V_{IH}	Input high-voltage (3.3 V compatible) [11]	2.0	—	—	V
V_{IL}	Input low-voltage (3.3 V compatible) [11]	—	—	1.0	V
V_{HYS}	Input hysteresis [11]	—	100	—	mV
I_{IL}	Input leakage current Pins tristate, V_{IN} = V_{COM} or AGND	−100	—	100	nA

Table 7. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions 9.6 V ≤ V_{PWR} ≤ 63 V, −20 °C ≤ T_J ≤ 85 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 56 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output high-voltage I_{OH} = −0.5 mA	V_{COM} − 0.8	—	—	V
V_{OL}	Output low-voltage I_{OL} = +0.5 mA	—	—	0.8	V
V_{ADC}	Analog ADC input voltage range for ratiometric measurements	AGND	—	V_{COM}	V
$V_{OL(TH)}$	Analog input open pin detect threshold	0.1	0.15	0.23	V
R_{OPENPD}	Internal open detection pulldown resistor [12]	3.8	5.0	6.2	kΩ
t_{GPIO0_WU}	GPIO0 WU de-glitch filter	47	50	85	μs
t_{GPIO0_FLT}	GPIO0 daisy chain de-glitch filter both edges	19	20	48	μs
t_{GPIO2_SOC}	GPIO2 convert trigger de-glitch filter	1.9	2.0	2.1	μs
t_{GPIOx_DIN}	GPIOx configured as digital input de-glitch filter	2.5	—	5.6	μs
Reset input					
V_{IH_RST}	Input high-voltage (3.3 V compatible)	2.0	—	—	V
V_{IL_RST}	Input low-voltage (3.3 V compatible)	—	—	1.0	V
V_{HYS}	Input hysteresis	—	0.6	—	V
$t_{RESETFLT}$	RESET de-glitch filter	—	100	—	μs
R_{RESET_PD}	Input logic pull down (RESET)	—	100	—	kΩ
SPI_COM_EN input					
V_{IH}	Input high-voltage (3.3 V compatible)	2.0	—	—	V
V_{IL}	Input low-voltage (3.3 V compatible)	—	—	1.0	V
V_{HYS}	Input hysteresis	—	450	—	mV
$R_{SPI\_COM\_EN\_PD}$	Input pulldown resistor (SPI_COM_EN)	—	100	—	kΩ
Digital interface					
V_{FAULT_HA}	FAULT output (high active, IOH = 1.0 mA)	4.0	4.9	6.0	V
I_{FAULT_CL}	FAULT output current limit	3.0	—	40	mA
R_{FAULT_PD}	FAULT output pulldown resistance	—	100	—	kΩ
V_{IH_COMM}	Voltage threshold to detect the input as high SI/RDTX_IN+, SCLK/RDTX_IN–, CSB, SDA, SCL (NOTE: needs to be 3.3 V compatible)	—	—	2.0	V
V_{IL_COMM}	Voltage threshold to detect the input as low SI/RDTX_IN+, SCLK/RDTX_IN–, CSB, SDA, SCL	0.8	—	—	V
V_{HYS}	Input hysteresis SI/RDTX_IN+, SCLK/RDTX_IN–, CSB, SDA, SCL	30	80	130	mV
I_{LOGIC_SS}	Sleep state input logic current CSB	−100	—	100	nA
R_{SCLK_PD}	Input logic pulldown resistance (SCLK/RDTX_IN–, SI/RDTX_IN+)	—	20	—	kΩ
R_{I_PU}	Input logic pullup resistance to V_{COM} (CSB, SDA, SCL)	—	100	—	kΩ
I_{SO_TRI}	Tristate SO input current 0 V to V_{COM}	−2.0	—	2.0	μA
V_{SO_HIGH}	SO high-state output voltage with $I_{SO(HIGH)}$ = −2.0 mA	V_{COM} − 0.4	—	—	V
V_{SO_LOW}	SO, SDA, SLK low-state output voltage with $I_{SO(HIGH)}$ = −2.0 mA	—	—	0.4	V
CSB_{WU_FLT}	CSB wake-up de-glitch filter, low to high transition	—	—	80	μs

Table 7. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions 9.6 V ≤ V_{PWR} ≤ 63 V, −20 °C ≤ T_J ≤ 85 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 56 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
System timing					
t_{CELL_CONV}	Time needed to acquire all 14 cell voltages after an on-demand conversion [13] 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	56 76 117 197	59 80 123 208	62 84 129 218	µs
$t_{VPWR(READY)}$	Time after VPWR connection for the IC to be ready for initialization	—	—	5.0	ms
$t_{WAKE-UP}$	Power up duration	—	—	440	µs
t_{WAKE_DELAY}	Time between wake pulses	500	600	700	µs
t_{NOWUP}	Time, starting from the first SOM received, to go back to Sleep/Idle mode time after receiving incomplete TPL bus wake-up sequence	—	—	1.3	ms
t_{IDLE}	Idle timeout after POR	57	60	64	s
$t_{BALANCE}$	Cell balance timer range	0.5	—	511	min
t_{CYCLE}	Cyclic acquisition timer range	0.0	—	8.5	s
t_{FAULT}	Fault detection to activation of fault pin Normal mode	—	—	56	µs
t_{DIAG}	Diagnostic mode timeout	0.047	1.0	8.5	s
t_{EOC}	SOC to data ready (includes post processing of data, ADC_CFG[AVG] = 0) [13] 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	140 190 291 494	148 201 307 520	156 211 323 546	µs
t_{SETTLE}	Time after SOC to begin converting with ADC1-A,B [13]	11.67	12.28	12.90	µs
t_{SYS_MEAS1}	Time needed to send an SOC command and read back 96 cell voltages, 48 temperatures, and ADC1-A,B configured as follows (with ADC_CFG[AVG] = 0): 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	— — — —	4.67 4.73 4.83 5.05	— — — —	ms
t_{SYS_MEAS2}	Time needed to send an SOC command and read back 96 cell voltages, and ADC1-A,B configured as follows (with ADC_CFG[AVG] = 0): 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	— — — —	3.24 3.39 3.40 3.61	— — — —	ms

Table 7. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions 9.6 V ≤ V_{PWR} ≤ 63 V, −20 °C ≤ T_J ≤ 85 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 56 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLST_TPL}	Time needed to send an SOC command and read back 14 cell voltages, 7 temperatures, with TPL communication working at 2.0 Mbps and ADC1-A,B configured as follows (with ADC_CFG[AVG] = 0): 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	— — — —	0.85 0.90 1.101 1.22	— — — —	ms
t_{CLST_SPI}	Time needed to send an SOC command and read back 14 cell voltages, 7 temperatures, with SPI communication working at 4.0 Mbps and ADC1-A,B configured as follows (with ADC_CFG[AVG] = 0): 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	— — — —	0.57 0.64 0.76 1.03	— — — —	ms
$t_{I2C\_DOWNLOAD}$	Time to download EEPROM calibration after POR	—	—	1.0	ms
t_{I2C_ACCESS}	EEPROM access time, EEPROM write (depends on device selection)	—	5.0	—	ms
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx = 00}$	450	500	550	μs
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx = 01}$	0.9	1.0	1.1	ms
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx = 10}$	9	10	11	ms
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx = 11}$	90	100	110	ms
$t_{WAVE\_DC\_ON}$	Daisy chain duty cycle on time	450	500	550	μs
t_{COM_LOSS}	Time out to reset the IC in the absence of communication	—	1024	—	ms
SPI interface					
t_{SPI_TD}	Sequential data transfer delay in SPI mode (N) [14]	1.0	—	—	μs
F_{SCK}	SCLK/RDTX_IN– frequency [14]	—	—	4.0	MHz
t_{SCK_H}	SCLK/RDTX_IN– high time (A) [14]	125	—	—	ns
t_{SCK_L}	SCLK/RDTX_IN– high time (B) [14]	125	—	—	ns
t_{SCK}	SCLK/RDTX_IN− period (A+B) [14]	250	—	—	ns
t_{FALL}	SCLK/RDTX_IN− falling time [14]	—	—	15	ns
t_{RISE}	SCLK/RDTX_IN− rising time [14]	—	—	15	ns
t_{SET}	SCLK/RDTX_IN− setup time (O) [14]	20	—	—	ns
t_{HOLD}	SCLK/RDTX_IN– hold time (P) [14]	20	—	—	ns
t_{SI_SETUP}	SI/RDTX_IN+ setup time (F) [14]	40	—	—	ns
t_{SI_HOLD}	SI/RDTX_IN+ hold time (G) [14]	40	—	—	ns
t_{SO_VALID}	SO data valid, rising edge of SCLK/RDTX_IN− to SO data valid (I) [14]	—	—	40	ns
t_{SO_EN}	SO enable time (H) [14]	—	—	40	ns
$t_{SO\_DISABLE}$	SO disable time (K) [14]	—	—	40	ns

Table 7. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions 9.6 V ≤ V_{PWR} ≤ 63 V, −20 °C ≤ T_J ≤ 85 °C, GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 56 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSB_LEAD}	CSB lead time (L) [14]	100	—	—	ns
t_{CSB_LAG}	CSB lag time (M) [14]	100	—	—	ns
TPL interface (MCU)					
t_{MCU_RES}	Time between two consecutive message request transmitted by MCU [15]	4.0	—	—	µs
t_{WU_Wait}	Time the MCU shall wait after sending first wake-up message per BMI7014 IC [16]	0.75	—	—	ms
TPL interface (BMI7014)					
t_{TPL_TD}	Sequential data transfer delay in TPL mode [17][18]	3.8	4.0	4.25	µs
t_{TPL}	Transmit pulse duration	—	210	—	ns
t_{port_delay}	Port delay introduced by each repeater in BMI7014 [19]	—	—	0.95	µs
t_{RES}	Slave response after read command [20]	4.0	5.0	9	µs
$V_{RDTX\ INTH_}$TA1	Differential receiver threshold	480	580	680	mV
$V_{RDTX\ INTH_}$TA2	Differential receiver threshold	480	580	720	mV
t_{EOM}	Message timeout duration [21]	238	250	—	µs

[1] Use of ADC1-A,B can be performed with a duty cycle of t_{EOC}/period (µs). For example, SYS_CFG1[CYCLIC_TIMER] = 010, corresponding to 100000 µs period, and ADC_CFG[ADC1_A_DEF] = ADC_CFG[ADC1_B_DEF] = 11, corresponding to 16 bits and therefore t_{EOC} = 520 µs, given a duty cycle of 0.0052 (or ROM). When an ADC is configured in continuous mode, the duty cycle is equal to 1, resulting in high-current consumption.

[2] To calculate the current consumption in sleep mode, the following formula has to be used: $I_{SLEEP\_MODE} = (1 - \tau_{NORMAL}) \cdot I_{VPWR(SS)} + \tau_{NORMAL} \cdot [I_{VPWR} + I_{VPWR(ADC)}] + I_{VPWR(CBON)}$ (not zero only if SYS_CFG1[CB_DRVEN] = 1), where $\tau_{NORMAL} = (t_{VCOM} + t_{EOC})$/period (µs), where t_{EOC} depends on the selected number of bits for the ADCs (see ADC_CFG[ADC1_A_DEF, ADC1_B_DEF] fields) and period (µs) depends on SYS_CFG1[CYCLIC_TIMER], as explained in note [1] . Evidently $I_{SLEEP\_MODE} = I_{VPWR(SS)}$ only if no conversion is requested in sleep mode (for example, SYS_CFG1[CYCLIC_TIMER] = 000) and if the cell balancing is OFF.

[3] If the battery stack has at least eight cells and if –1.5 V < $V_{PWR} – V_{CT\_14}$ < –0. 7 V, each cell voltage has to be greater than 2.0 V to meet the accuracy spec. If the battery stack has seven cells and if –1.5 V < $V_{PWR} – V_{CT\_14}$ < –0. 7 V, each cell voltage has to be greater than 2.3 V to meet the accuracy spec.

[4] 5 % to 95 % rise time

[5] ADC1-A/B may clamp when the voltage of the Cellx or ANx is over 4.85 V.

[6] The cell voltage error includes all internal errors, for example; ADC offset, gain error, INL and DNL. Single shot measurements are affected by noise, which has zero mean and standard deviation given by VV_NOISE and is not included in the cell voltage error. In order to reduce it, SW implemented IIR or FIR low-pass filters may be used; example, a moving average, whose length is N samples, has output standard deviation VOUTPUT_NOISE = VV_NOISE /sqrt(N). Performance can be granted only if ADC1-A,B are configured at 16-bits resolution (ADC_CFG[ADC1_A_DEF] =ADC_CFG[ADC1_B_DEF] = 11) and if -100 mV ≤ CTREF - GND ≤ 100 mV.

[7] Inaccuracies from soldering or aging are not included.

[8] If the battery stack has at least eight cells, for all accuracy ranges, the accuracy for a given cell can be guaranteed if all other cells are at least at 1.2 V. If the battery stack has seven cells, for all accuracy ranges, the achievement of the accuracy spec for a given cell can be guaranteed if all other cells are at least 1.8 V.

[9] Inaccuracies from soldering (MSL3 preconditioning) and aging (after 3000 h HTOL at T_A = 125 °C) are included.

[10] Only one of the three threshold values shall be selected, dependent on the voltage range in which the cell is typically working, provided a 5 KΩ resistor is used for the input cell low pass filter. Using a dynamic selection of the threshold, depending on the measured voltage is not allowed.

[11] For GPIO0 configured as wake-up, transition time must be shorter than 100 µs

[12] During internal open detection, an internal pullup current of 10 µA typical is generated in the pin.

[13] See the ADC conversion sequence in Figure 10

[14] See the timing diagram in Figure 5

[15] It is the time which MCU shall wait for sending new message request to BMI7014.

[16] The waiting time for MCU after transmitting the first wake-up message is dependent on the number of BMI7014 in daisy chain. If the number of nodes in daisy chain is N, then the total waiting time for MCU after sending first wake-up message is N*t_{WU_Wait}

[17] See the waveforms diagram in Figure 26

[18] t_{TPL_TD} is the time between two consecutive response messages at the node which is initiating transmission. This time could vary when measured at other forwarding nodes in daisy chain.

[19] The expected waiting time for MCU, to get the response from BMI7014 is dependant on number of BMI7014 used in daisy chain. The repeater of each node imposes a delay of t_{port_delay} for both request and respose. Example: if 24, BMI7014 ICs are used in a daisy chain, the last node (24th BMI7014) receives the request in (24*0.95)µs = 22.8 µs.

[20] t_{RES} is the time between request received and response transmitted by the slave device, which is addressed in the read command. This time could vary when measured at other forwarding nodes in daisy chain.

[21] The EOM timeout counter starts/restarts after reception of SOM. This means that the maximum length of allowed message frame is t_{EOM}. If a valid EOM is not received in this time frame, the message frame is discarded and the device is ready for new reception.

8.5 Timing diagrams

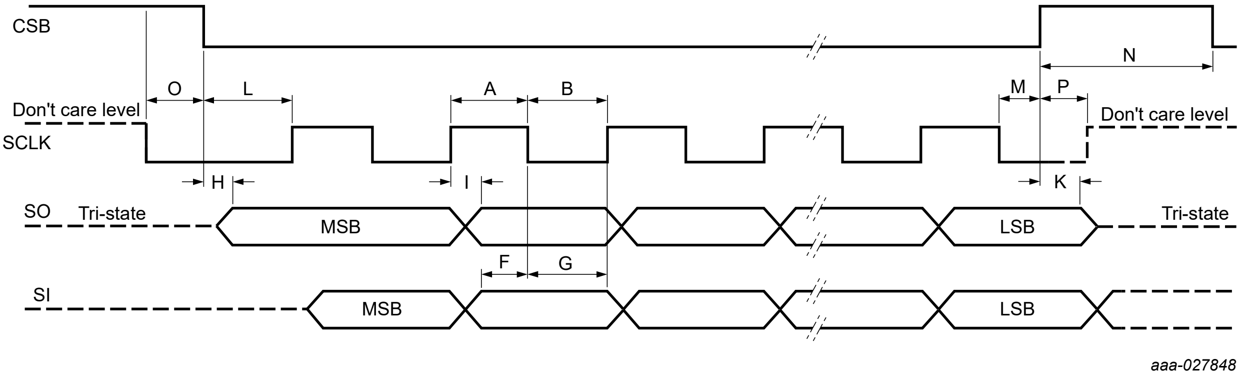


Figure 5. Low-voltage SPI interface timing

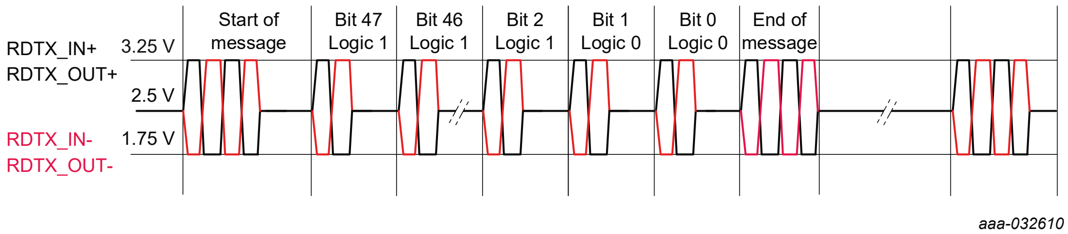


Figure 6. Transformer communication signaling

9 Functional description

9.1 Introduction

The BMI7014 contains all circuit blocks necessary to perform battery voltage measurements, cell temperature measurement and integrated cell balancing. These features along with high speed communication make the BMI7014 ideal for industrial Lithium-ion battery monitoring. In addition to the battery management functions, the BMI7014 is designed to monitor many internal and external functions to validate the integrity of the measurements and the measurement system. The following section describes in detail the features, functions and modes of operation of the device. Table 8 summarizes the IC measurement capability depending on the operating mode. Following terms, phrasings and conventions are used in this document:

- User: this word denotes the battery pack controller, including at least one MCU, where the intelligence of the system is located. The pack controller uses one or more BMI7014 to sense the physical quantities of a battery.
- User parameter (or simply parameter): it is a datum memorized in the IC registers that is readable or writable by the user and is denoted by an identifier within square brackets preceded by a prefix, for example, REGISTER_NAME[FIELD_NAME], where REGISTER_NAME is the symbol for the intended register and FIELD_NAME is the symbol for the parameter itself, which is, in general, a portion of the 16-bit register data.
- Channel: it is a signal, which can be measured. There are external channels, for example, cell voltages and temperatures, and internal channels, for example, die temperature, and voltage diagnostic references.
- Conversion: this word denotes an analog to digital conversion performed by an ADC and is often meant as measurement of a given channel.
- Sequence: this term denotes a scan of channels that enter some multiplexers to be routed to the ADCs according to a certain sequence. During the scan, each ADC performs subsequent data conversions,

where each conversion affects a predetermined channel. Sequences are necessary because the number of channels is much greater than the number of ADCs.

- Cyclic measurement: this means the bank of ADCs perform sequences autonomously, for example, with no intervention requested to the user. The user has to do a single programming of an internal timer by providing it with the period value. Then the timer provides the periodic trigger starting each measurement sequence. For example, the period may be 100 ms, while the sequence duration is order of magnitudes shorter. The main purpose of performing cyclic measurements is to carry out automatic comparisons of some measured channels against predefined tunable thresholds, so some fault bits can be set accordingly. Fault bits are readable by the user by accessing the proper fault registers through the ordinary communication channel; or the fault bits may be used to assert the FAULT pin, for the information be propagated to the user through the fault line of daisy chained devices.
- On-demand measurement: this means the bank of ADCs perform a sequence when triggered by a SOC command, where SOC means start of conversion. Typically, the user periodically sends a SOC command followed by the reading of the measured values of the most important channels, namely all cell voltages and temperatures.

Table 8. Working mode versus measurements

Operating mode	On-demand measurements	Voltage/temperature cyclic measurements	Reference
Normal mode	Available	Available, if SYS_CFG1[CYCLIC_TIMER] ≠ 0	Section 9.3.4
Diagnostic mode	Available	Not available	Section 9.3.6
Sleep mode	Not available	Available, if SYS_CFG1[CYCLIC_TIMER] ≠ 0	Section 9.3.5
Other modes	Not available	Not available	

9.2 Power supplies and reset

9.2.1 Decoupling of power supplies

The recommended decoupling of power supplies is shown in Figure 7 The capacitors should be placed close to the IC pins.

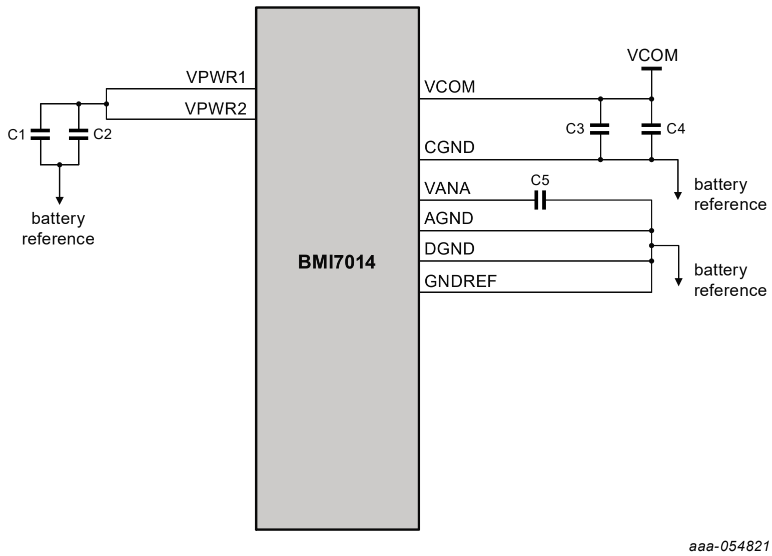


Figure 7. Recommended decoupling of power supplies

Table 9. Recommended capacitor values for power supply decoupling

ID	Value	Units	Comments
C1	220	nF	—
C2	1	nF	—
C3	2.2	μF	Ceramic capacitor
C4	220	pF	—
C5	47	nF	Ceramic capacitor

9.2.2 VPWR overvoltage, low-voltage

The BMI7014 incorporates comparators to monitor VPWR pins for overvoltage and low-voltage conditions. In the event the voltage on VPWR pin is above the overvoltage threshold $V_{PWR(OV\_Flag)}$ for greater than the $t_{VPWR(Filter)}$ period, the overvoltage fault flag is set in FAULT1_STATUS[VPWR_OV_FLT].

When unmasked by FAULT_MASK1[MASK_12_F], the FAULT1_STATUS[VPWR_OV_FLT] bit sets the FAULT output pin high. An overvoltage condition on the VPWR pin does not cause the BMI7014 to perform a shutdown. The pack controller may clear the FAULT1_STATUS[VPWR_OV_FLT] bit when V_{PWR} returns to the normal operating range by writing logic 0 to the FAULT1_STATUS[VPWR_OV_FLT] bit.

A low-voltage condition on VPWR pin causes the FAULT1_STATUS[VPWR_LV_FLT] bit to be set. The FAULT1_STATUS[VPWR_LV_FLT] bit may be cleared when the normal operating range voltage resumes on the VPWR pin and by writing 0 to the FAULT1_STATUS[VPWR_LV_FLT].

9.2.3 VCOM supply

The VCOM supply is a linear regulator used to supply power for communication, GPIOx, SPI interface, external temperature sensor reference, and optional external EEPROM.

The VCOM supply is monitored by the BMI7014 for undervoltage. Excessive load on the VCOM pin activates VCOM current limit causing an undervoltage fault condition to occur. During the event, the FAULT2_STATUS[VCOM_UV_FLT] fault bit is set and the regulator enters $t_{VCOM(RETRY)}$ shutdown/retry strategy.

Undervoltage shutdown of the VCOM supply directly affects communication, GPIO outputs and external temperature measurements. In addition to setting the individual fault bits for each ANx/GPIO, multiple faults may be set in the FAULTx_STATUS register.

Faults may be cleared by the pack controller when communication resumes. VCOM also has a comparator that monitors for overvoltage. In the event the voltage on VCOM becomes greater than $V_{COM(OV)}$, the FAULT2_STATUS[VCOM_OV_FLT] fault flag is set.

9.2.4 VANA supply

The VANA supply is an internal 2.5 V supply used by the BMI7014 for analog control. No circuits other than the decoupling capacitor should be terminated to the VANA pin. The VANA supply is monitored by the BMI7014 for undervoltage. External load on the VANA pin activates the VANA current limit causing an undervoltage fault condition to occur. During the event, the FAULT2_STATUS[VANA_UV_FLT] fault bit is set and the regulator enters $t_{VANA(retry)}$ shutdown/retry strategy.

Undervoltage shutdown of the VANA supply directly affects the performance of the analog to digital converters generating fault condition. Additionally, VANA is monitored by the ADC converter for an overvoltage condition each time a conversion sequence is performed. In the event VANA exceeds the $V_{ANA(OV)}$ threshold, the FAULT2_STATUS[VANA_OV_FLT] is set.

9.2.5 Power-on reset (POR)

The BMI7014 has two sources of POR in the IC system. An undervoltage condition on the VPWR pin causes the BMI7014 to reset. Upon returning from undervoltage, the BMI7014 performs a POR.

The second source of potential POR occurs during transient conditions when the internal digital logic supply voltage drops below the critical threshold where logic states cannot be guaranteed. In this case, the BMI7014 performs a POR.

POR is indicated by the FAULT1_STATUS[POR] bit. In the event of a POR, all registers in the BMI7014 are set to their POR state and the FAULT pin becomes active.

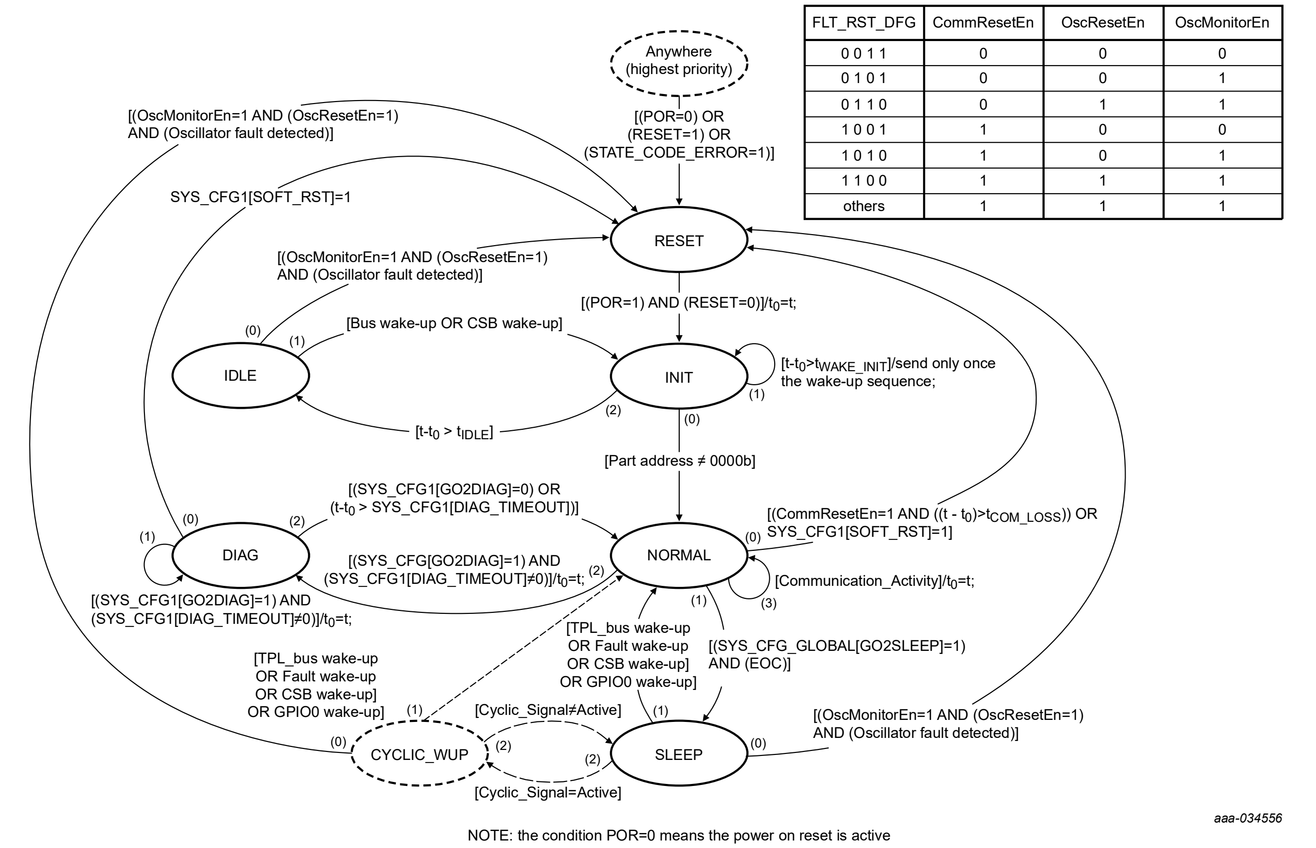
9.2.6 Hardware and software reset

An active high on the RESET pin for greater than the $t_{RESETFLT}$ filter time causes the BMI7014 to reset. Software resets are performed when the BMI7014 receives a message written to the SYS_CFG1[SOFT_RST] bit. Hardware and software resets are indicated by the status of the FAULT1_STATUS[RESET_FLT] bit, and the FAULT pin becomes active. After a HW or SW reset, it is necessary to wait for the time interval $t_{VPWR(READY)}$ before being possible to reprogram the part.

9.3 Modes of operation

From RESET mode, the BMI7014 must be initialized with a cluster ID before the device is allowed to enter Normal mode. After initialization, the BMI7014 enters Normal mode. In Normal mode the device is in full operation performing on-demand conversions. When commanded to Sleep mode, the device will have reduced current consumption. Diagnostic mode provides a method for diagnosing the integrity of many functions as well as internal or external faults that may have occurred. If properly configured, if there is no traffic during Normal mode on the bus during t_{COM_LOSS}, the BMI7014 will reset.

In the event the device is powered up and not initialized, the BMI7014 enters the low-power IDLE mode after a t_{IDLE} timeout period. Detecting a wake-up pattern transfers the BMI7014 to the initialization state INIT where the CID can be programmed. In Figure 8, an integer number enclosed in round brackets close to a transition arc indicates the priority of such a state transition in case the conditions are verified at the same time. The lower the number is, the higher is the priority, so if several conditions are true at the same time, the one with lowest priority number determines the state transition; a boolean condition is enclosed between square brackets. A list of actions after the state transition condition is preceded by the slash symbol. Symbol "t" represents the absolute time, symbol t_0 stays for a variable having the dimension of time.



FLT_RST_DFG	CommResetEn	OscResetEn	OscMonitorEn
0 0 1 1	0	0	0
0 1 0 1	0	0	1
0 1 1 0	0	1	1
1 0 0 1	1	0	0
1 0 1 0	1	0	1
1 1 0 0	1	1	1
others	1	1	1

Figure 8. Operating mode state diagram

Table 10. Power supply mode operation

	Normal/Init mode	Diagnostic mode	Cyclic WUP	Sleep/Idle mode
Supplies active	VCOM = ON, VANA = ON	VCOM = ON, VANA = ON	VCOM = ON (during cycle) VANA = ON (during cycle)	VCOM = 0, VANA = 0
Communication	Communication enabled	Communication enabled	Communication enabled (during cycle)	Wake-up function only

9.3.1 Reset mode

The table in Figure 8 provides information about the mapping between all possible values of the SYS_CFG2[FLT_RST_CFG] field, which may be written and read by the user, and the corresponding values of the following internal bits, which are not user readable:

- CommResetEN: If it is equal to 1, the IC reset due to a communication timeout in Normal mode is enabled, else it is disabled
- OscResetEN: If it is equal to 1, the IC reset due to the detection of a defective oscillator in Sleep mode is enabled, else it is disabled
- OscMonitorEN: If it is equal to 1, the oscillator monitoring is enabled, else it is disabled

The value "others" readable in the column labeled as SYS_CFG2[FLT_RST_CFG] refers to values that are different from those listed above.

The registers are reset to their default values, except some bits of the FAULT1_STATUS register.

9.3.2 Idle mode

The BMI7014 enters IDLE mode from INIT mode when the communication bus is not active for the t_{IDLE} time period. While the BMI7014 is in IDLE mode, no messages are recognized, only a valid wake-up sequence lets the device transition from IDLE mode to INIT mode. When the BMI7014 is configured as a SPI interface and enters IDLE mode, the device transitions from IDLE mode to INIT mode if CSB duration is larger than CSB_{WU_FLT} maximum value, otherwise the pulse will be considered as a glitch and then filtered.

9.3.3 Init mode

After a POR or reset (Soft RST or pin RESET), the BMI7014 enters INIT mode. The BMI7014's cluster ID is 0 (unassigned CID). All registers, except the INIT register, are read-only. In INIT mode, any unassigned BMI7014 does not forward any message and responds (if needed) only on the side that received a request. The user has to assign a cluster ID between 1 and 63, to enter Normal mode. This assignment is mandatory for both SPI and TPL communication. If the assignment of a cluster ID is not performed within the t_{IDLE} timeout, IDLE mode will be entered to reduce current consumption.

9.3.4 Normal mode

In Normal mode, on reception of a valid message, the BMI7014 executes the commanded operation. Device configuration registers control the operating characteristics of the BMI7014 and are all programmed while the device is in Normal mode. Once programmed, the BMI7014 performs control operations like overvoltage and undervoltage in the background without further instruction from the pack controller.[1]

To accomplish the control operations in Normal mode, the BMI7014 performs a cyclic conversion sequence at the programmed timed interval. In the event the BMI7014 receives an on-demand conversion request from the pack controller during a cyclic conversion, the device stops the cyclic conversion and immediately starts the on-demand conversion cycle. Halting the cyclic conversion and performing the on-demand conversion allows all BMI7014 devices in the system to achieve measurements. From Normal mode, the BMI7014 may be commanded to Sleep mode or DIAG mode. If instructed by a proper value of the SYS_CFG2[FLT_RST_CFG] field, the part automatically resets whenever the communication is absent for longer than t_{COM_LOSS}.

9.3.5 Sleep mode

Sleep mode provides a method to significantly reduce battery current and the overall quiescent current of the battery management system. In Sleep mode, the overvoltage, undervoltage, overtemperature, and undertemperature circuitry can remain cyclically active[1], as well as the monitoring of V_{PWR}.

Based on the CYCLIC_TIMER setting, the BMI7014 may continue performing cyclic conversions in Sleep mode. This is the meaning of the dotted bubble labeled as CYCLIC_WUP in the state diagram shown in Figure 8. The permanence time in the CYCLIC_WUP transient state is really short; it is basically the time needed to turn on the VCOM power supply and to acquire 20 channels.

In the event a conversion value is greater than or less than the threshold value and the particular wake-up/fault is unmasked, the BMI7014 performs a bus wake-up and can activate the FAULT pin.

To instruct the BMI7014 to enter the Sleep mode, the user sets the SYS_CFG_GLOBAL[GO2SLEEP] bit to logic 1. If the communication type is TPL, only a global write command can be used, while in case of pure SPI communication, a local write command is necessary. In case the ADCs are performing acquisition (for a single sample or an average of N samples), the transition is delayed until the ongoing sequence is completed. It means that a single sample will be correctly acquired while an average will be potentially interrupted; in this latter case MEAS_CELL registers cannot be updated (DATA_RDY bit stays at 0 until the completion of the next average).

1 The cyclic measurement is disabled by default. Cyclic measurement can be activated by writing to SYS_CFG1[CYCLIC_TIMER].

Exit from Sleep mode is possible if one of the following occurs:

- Upon detection of a bus wake-up sequence, in TPL mode only
- By transitioning the CSB pin from low state to high state (shortly referred to as CSB wake-up)
- Upon detection of at least one out of a certain number of fault conditions (see FAULT1_STATUS, FAULT2_STATUS and FAULT3_STATUS along with their associated wake-up mask registers WAKEUP_MASK1, WAKEUP_MASK2 and WAKEUP_MASK3)[2]
- Depending on the content of SYS_CFG2[FLT_RST_CFG] field, it is possible to set the OscResetEn variable to 1.
- Wake-up by GPIO0.

The CSB wake-up capability imply some system considerations when SPI communication is used. Assumed the CSB line is pulled up to the same power supply used by the MCU. When the MCU commands the BMI7014 to go sleep and then the MCU itself goes to sleep, both devices sleep until the time the MCU wakes up. However, when this happens, the BMI7014 wakes up, because the CSB line transitions from low state to high state. To avoid this behavior, the MCU has to take care to force the CSB line to the high state during the entire sleep time.

9.3.6 Diagnostic mode

In Diagnostic mode, the system controller has extended control of the BMI7014 in order to execute performance integrity checks of the device. It is critical to note that when the BMI7014 is in Diagnostic mode, cyclic conversions are halted and OV/UV/OT/UT detection is not performed automatically. To perform OV/UV/OT/UT or any other protection feature that requires a conversion, an on-demand conversion message must be sent by the pack controller.

To prevent the BMI7014 from remaining in Diagnostic mode without automatic OV/UV/OT/UT detection, a protection DIAG_TIMEOUT timer has been implemented. In the event of the timeout, the BMI7014 reverts to Normal mode and sets the bit FAULT3_STATUS[DIAG_TO_FLT] to logic 1.

To enter Diagnostic mode, the user must set the SYS_CFG1[GO2DIAG] bit to logic 1. To exit Diagnostic mode, the user must clear the GO2DIAG bit.

Note: *If cyclic acquisition is enabled, before transitioning to Diagnostic mode, the cyclic acquisition needs to be disabled. Disabling of cyclic acquisition and GO2DIAG should be two separate commands sent by MCU.*

9.4 Analog to digital converters ADC1-A, ADC1-B

At the heart of the BMI7014 are two hybrid ADCs using a 6.0 MHz clock and having two modes of operation, called *phases*:

- Incremental phase: it is necessary to compute the most significant bits. During this first phase, the ADC operates as shown in Figure 9 (left part). It appears equal to a 1st order ΣΔ, but it has no memory, as the initial state is always 0.
- The second phase, referred to as cyclic phase, is needed to extract the least significant bits. During this phase, the converter is blind to the input (but not to the reference) and performs the conversion of the residual error.

This ADC, which is built around a switched capacitor integrator, is much faster than a ΣΔ, an essential feature when the input comes from a multiplexer and the channel switching has to be very fast. There is no decimation downstream the ADC.

2 The wake-up performed by BMI7014 under the detection of internal fault is disabled by default. It can be activated by writing to registers WAKEUP_MASK1, WAKEUP_MASK2 and WAKEUP_MASK3.

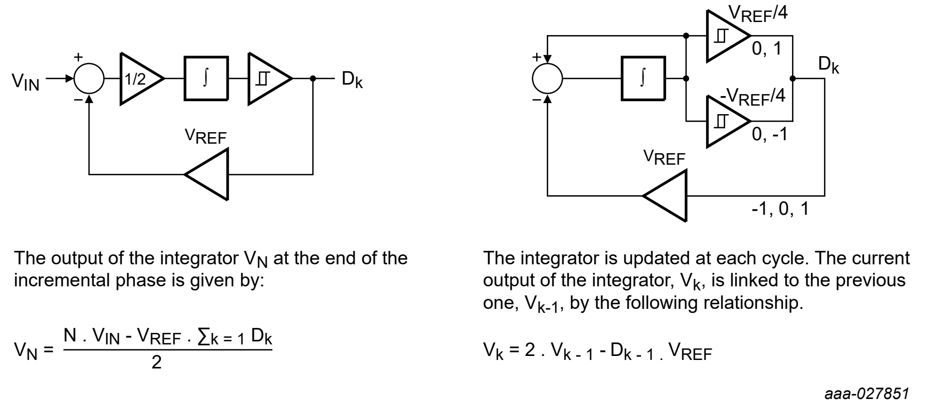


Figure 9. ADC converter: incremental phase (left) and cyclic phase (right)

The ADC architecture affords the user the flexibility to select the speed vs. accuracy. Conversion resolution setting for ADC1-A and ADC1-B are programmable from 13 to 16 bits (see Section 11.7 "ADC configuration register – ADC_CFG"). ADC1-A and ADC1-B settings must be equal to each other.

9.4.1 High precision voltage reference

To guarantee the accuracy of all ADC conversion data, the BMI7014 integrates a high precision fully compensated voltage reference.

9.4.2 Measurement sequence

The BMI7014 performs on-demand differential measurements of external inputs and internal measurements using two ADC converters for measurement, calibration, and diagnostics. Once the device is initialized, on-demand conversions are initiated by writing to the ADC_CFG [SOC] convert register or a GPIO2 input trigger.

The ADC_CFG register contains the conversion parameters for ADC1-A and ADC1-B converters and the start conversion bit for synchronization. Writing a logic 1 to the SOC bit initiates the conversion sequence. Conversions in progress may be interrupted by reinitiating a new conversion. Measurements for each ADC converters in the BMI7014 have a predefined measuring sequence. Voltage conversions coming from ADC1-A and ADC1-B are synchronized.

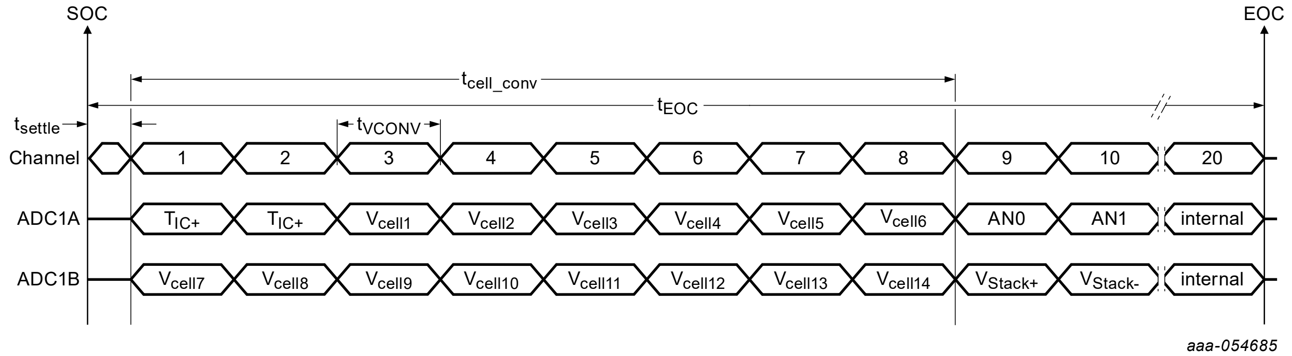


Figure 10. ADC conversion sequence in normal mode

Immediately after receipt of a conversion request, there is a dead time t_{SETTLE}, after which ADC1-A and ADC1-B converters start their conversion sequence as shown in Figure 10.

At time t_{CELL_CONV}, all voltage samples are frozen and then post-elaborated. Offset is measured and canceled, a multiplicative correction with a gain depending on the IC die temperature is performed. The completion of the entire sequence, whose length is equal to 20 time slots, occurs at time t_{EOC}. All results are stored into user registers and their associated data ready bits are set to Logic 1. Channels identified as "internal" are used for calibration purposes and are performed at each conversion sequence. Information on how the data is tagged and stored is provided in Section 10. On-demand conversions are not only used for storing measurement results in user registers, but also for OV/UV/OT/UT comparisons.

In addition to on-demand conversion requests, the BMI7014 provides timing control for cyclic measurements, that is, conversions occurring with no need for the pack controller to repeatedly send SOC commands. Cyclic measurements are useful for automatic OV/UV/OT/UT check. The user may select the cycle period by programming register SYS_CFG1[CYCLIC_TIMER]. The effective duration of a cyclic sequence is given by the t_{EOC} parameter. A cyclic sequence does not affect the content of the measurement registers (namely, of registers MEAS_ xxxx), while it has effect on the content of CELL_OV_FLT, CELL_UV_FLT, AN_OT_UT_FLT and FAULTx_STATUS registers.

9.4.2.1 Voltage averaging

The BMI7014 provides a feature of on-demand, on-chip voltage averaging. Using this feature, cell terminal voltage, Vstack voltage, and VrefA and VrefB voltages can be averaged for a configured number of samples. Averaging makes the measurement data more robust to noise, the averaging feature acts as a digital low pass filter. The on-chip averaging feature of BMI7014 reduces the MCU load by performing the averaging on-chip and also reducing the number of communication frames to be exchanged between master and slave.

After initialization of BMI7014, averaging can be triggered by configuring the ADC_CFG register as described in Section 11.7 "ADC configuration register – ADC_CFG". The number of samples to be averaged is chosen by writing to bit-field ADC_CFG[AVG] and accumulation of samples to be averaged is initiated by setting bit-field ADC_CFG[SOC] to logic 1 or by triggering GPIO2 input. Once the averaging is started the BMI7014 accumulates the configured number of samples and divides the accumulated value by the number of configured samples. The final value is updated in MEAS_CELLXX registers.

Ongoing accumulation of samples can only be interrupted by the GO2SLEEP and GO2DIAG commands. However, the averaging can be restarted with a new SOC command. On reception of a new SOC command, the BMI7014 discards the ongoing measurement (accumulation) and starts the new measurement. It is to be noted that the feature of voltage averaging is not available for cyclic measurement.

In Normal mode, during ongoing averaging the device can interrupt the voltage averaging and change its mode of operation. However, the GO2SLEEP and GO2DIAG commands have certain priority over averaging. The BMI7014 performing averaging is able to transition to Sleep or Diagnostic mode on reception of a valid GO2SLEEP or GO2DIAG command but only after completion of the ongoing sequence of measurement.

9.5 Cell terminal voltage measurement

Cell terminal voltages are monitored differentially, level shifted and multiplexed to the ADC1-A and ADC1-B converters. Conversion results of the cells are available in MEAS_CELLx registers.

Unused cell terminal (CTx) inputs may be terminated as shown in Figure 1 or as described in Section 12.2.2 "Unused cells". Overvoltage and undervoltage of unused inputs should be disabled through the OV_UV_EN[CTx_OVUV_EN] bits to prevent the input from triggering fault events. Conversions performed on unused inputs result in nearly zero ADC values.

The differential measurement of each cell terminal input is designed to function in conjunction with external anti-aliasing filter (see Section 12.2 "BMI7014 external components").

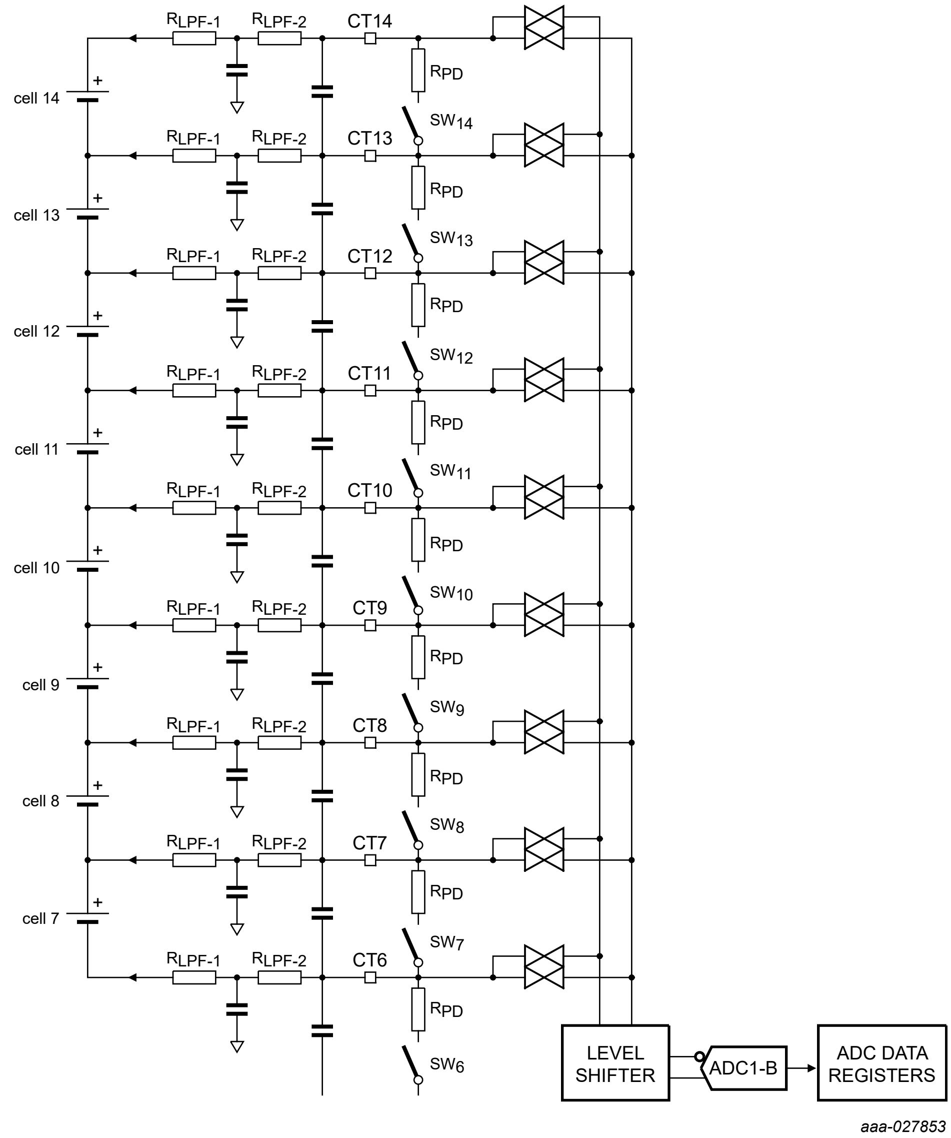


Figure 11. ADC1-B voltage measurement chain

Cell terminal CT7 through CT14 have the same type input structure as CTref through CT6 and are multiplexed to ADC1-B.

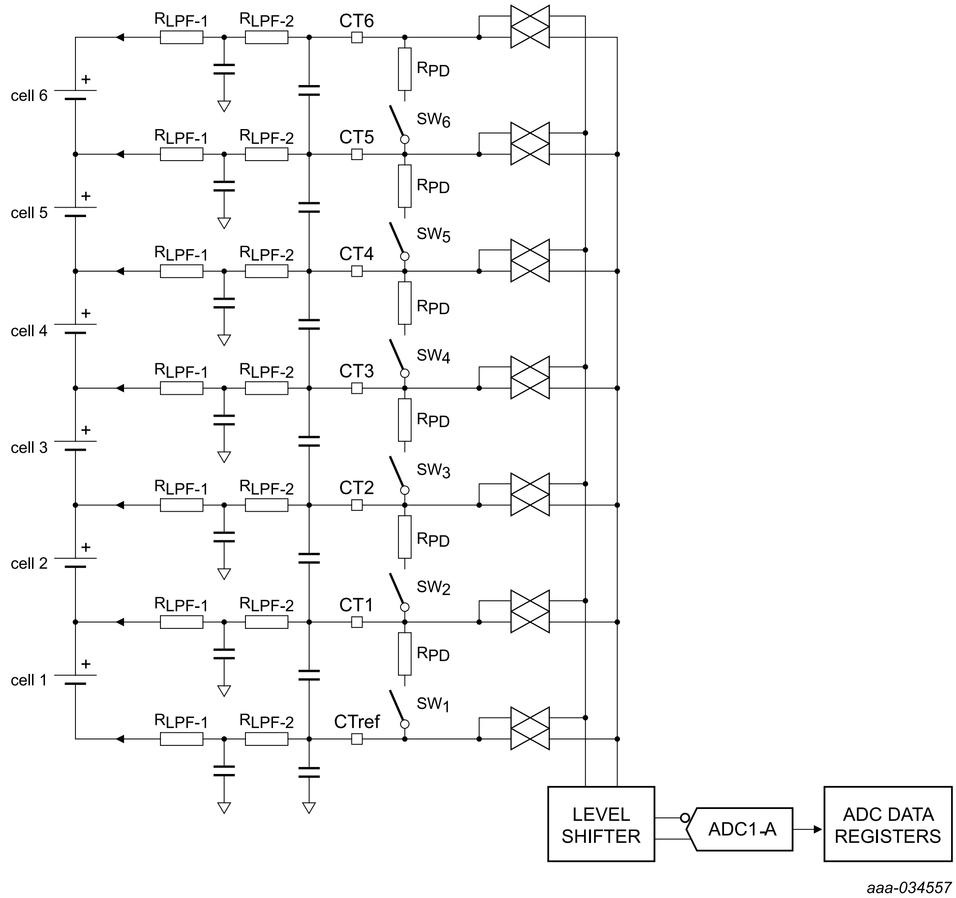


Figure 12. ADC1-A voltage measurement chain

9.6 GPIOx port control and diagnostics

For user flexibility, the BMI7014 has seven GPIO to support voltage measurements referenced to GND - typically coming from NTC based circuits used to extract temperature information, for example, that of cells - or to drive external circuits. All GPIOs may be individually configured as digital inputs or output ports, wake-up inputs, convert trigger inputs, ratiometric analog inputs with reference to VCOM, or analog inputs with absolute measurements. With the exception of the GPIO0, no external voltage must be applied on GPIOx pins when the device is off or in Sleep mode.

Table 11. GPIO port configurations

GPIO port	GPIO			Anx	
	Standard GPIO	Wup and daisy chain	Convert trigger	Absolute	Ratiometric
0	x	x		x	x
1	x			x	x
2	x		x	x	x
3	x			x	x
4	x			x	x
5	x			x	x
6	x			x	x

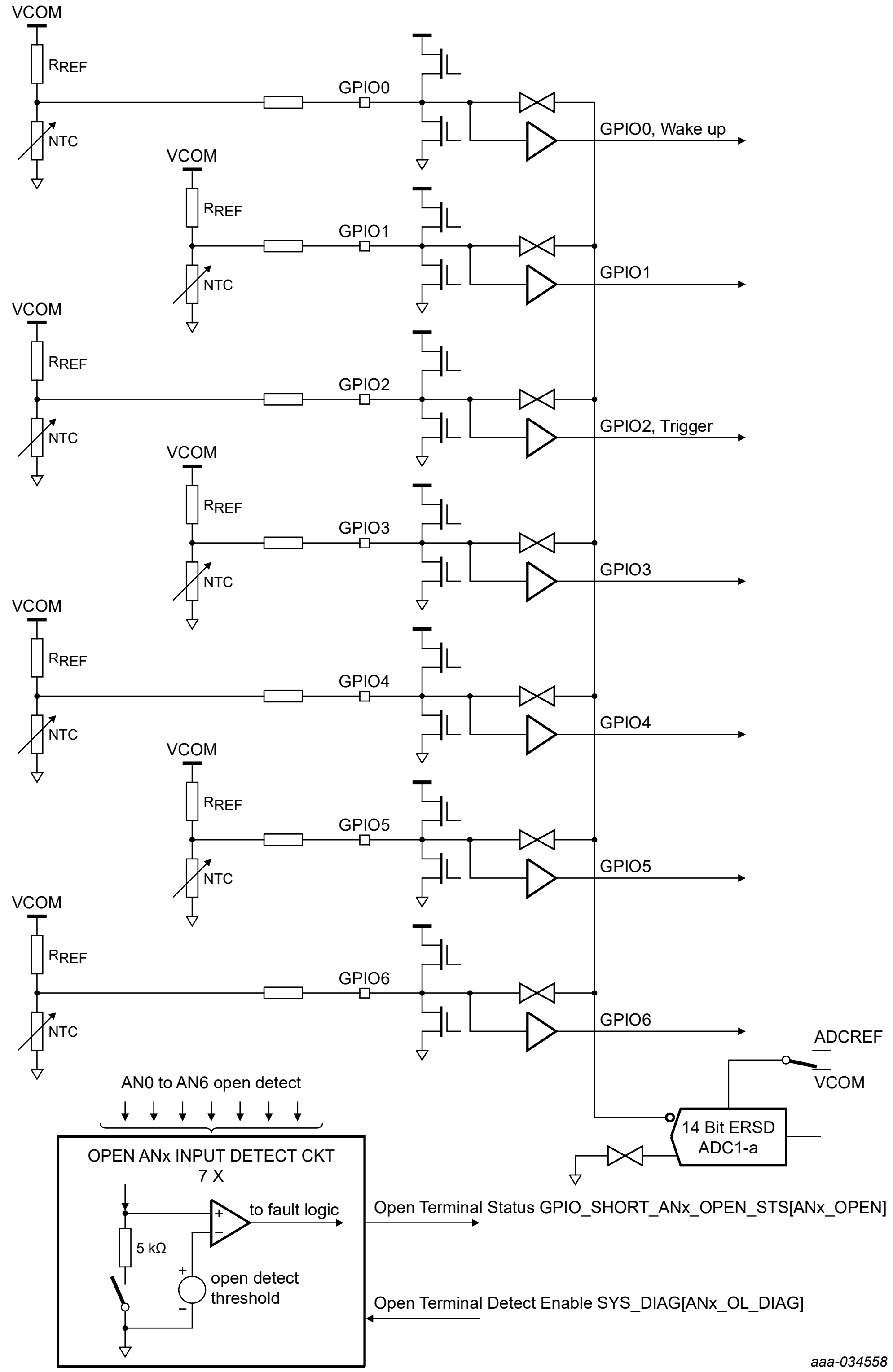


Figure 13. GPIO internal input structure

9.6.1 GPIOx used as digital I/O

Setting the GPIO_CFG1[GPIOx_CFG] bits to 10 or 11 configures the specific port as an input or output. Pins configured as outputs are driven high or low by writing to the GPIO_CFG2 register. Status of the ports, regardless of the digital configuration, is provided in the GPIO_STS register, which is a feedback of the actually commanded output.

Ports configured as GPIO outputs are diagnosed by the BMI7014. An output state GPIO_STS[GPIOx_ST], which is opposite of the commanded state GPIO_CFG2[GPIOx_DR], is considered to be shorted. Each short fault bit GPIO_SHORT_ANx_OPEN_STS[GPIOx_SH] associated with each GPIOx is OR wired to the FAULT2_STATUS[GPIO_SHORT_FLT] bit. Each GPIO_SHORT_ANx_OPEN_STS[GPIOx_SH] bit when unmasked activates the FAULT pin.

9.6.2 GPIO0 used as wake-up input or fault pin activation input

Setting the GPIO_CFG1[GPIO0_CFG] bits to 10 is used to configure a GPIO0 port as an input. To program GPIO0 as wake-up input, the user must set the GPIO_CFG2[GPIO0_WU] bit to logic 1. In this case, the device performs a wake-up on the rising or falling edge.

By setting the GPIO_CFG2[GPIO0_FLT_ACT] to logic 1, the GPIO0 port may be used to activate the FAULT pin in normal, sleep, and diagnostic modes of operation. This feature allows the user to daisy chain the FAULT pin in high-voltage battery pack applications.

9.6.3 FAULT pin daisy chain operation

The FAULT pin may be programmed to provide the battery management system with a diagnostic feedback. Two behaviors are possible. One is based on logic levels: low level indicates normal condition, high level reveals a faulty condition. The other possibility is based on the heartbeat signal, a periodic signal generated by the IC to indicate normal operation, which provides a higher integrity level.

Both modes can be activated in Normal mode, Sleep mode, and Diagnostic mode. The fault pin, carrying the diagnostic signal, is daisy chained to the next lower BMI7014 GPIO0 port. Each BMI7014 device is programmed to pass the heartbeat through to the neighboring device in the system. In this configuration, any fault that the BMI7014 can automatically detect may activate the FAULT line.

To configure the BMI7014 for daisy chain fault output:

1. Set GPIO0 as an input GPIO0_CFG = 10.
2. Disable wake-up on GPIO0 with GPIO0_WU = 0.
3. Set GPIO0 to propagate signal to FAULT pin with GPIO_CFG2[GPIO0_FLT_ACT] = 1.

To use the BMI7014 heartbeat feature, the user must write a 1 in the SYS_CFG1[FAULT_WAVE] bit. The signaling square wave has constant on time, whereas the desired off time may be selected by writing a proper value in the SYS_CFG1[WAVE_DC_BITx] configuration field.

The usage of the fault pin is essential if the IC uses SPI communication and must provide some monitoring functionality in Sleep mode. In such use case the fault line is the only means to alert the system controller about an occurred fault, while in TPL mode, even if the IC is sleeping, it has the chance to send a wake-up signal through the bus. The fault line usage is optional in Normal and diagnostic modes, as well as in Sleep mode and TPL configuration.

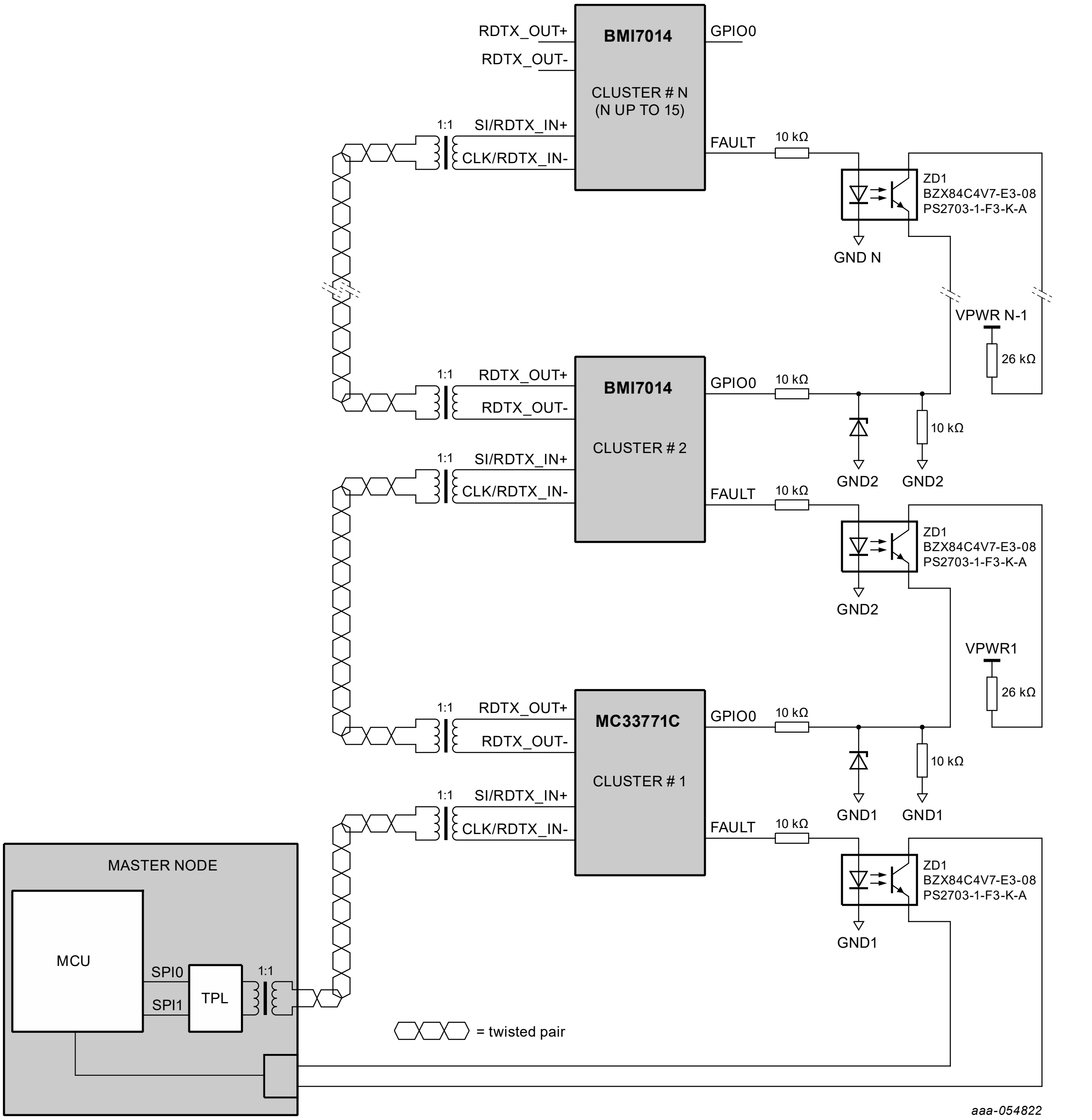


Figure 14. Heartbeat daisy chain

9.6.4 GPIO2 used as ADC trigger

The BMI7014 provides a convenient method to trigger an ADC conversion from an external digital source. To use GPIO2 as an ADC trigger, configure the port as a digital input through the setting GPIO_CFG1[GPIO2_CFG] = 10 and enable the trigger through the setting GPIO_CFG2[GPIO2_SOC] = 1. With the port configured, positive edge events on GPIO_CFG2[GPIO2_SOC] triggers a start of conversion sequence.

With a GPIO2 trigger, the converter operates as programmed in the ADC_CFG[SOC] bit. The GPIO2 convert trigger feature is not available in sleep mode.

9.6.5 GPIOx used as analog

Setting the GPIO_CFG1[GPIOx_CFG] bits to 00 or 01 configures the specific port as an analog ratiometric input or single ended. GPIOs configured as analog inputs are usually used for temperature measurement. The BMI7014 may be programmed to detect overtemperature and undertemperature.

To detect overtemperature and undertemperature, the generated digital value is compared to an individually programmed threshold in the TH_ANx_OT and TH_ANx_UT registers. Any ADC1-A result that exceeds the threshold, on any temperature measurement input, activates the FAULT1_STATUS[AN_OT_FLT,AN_UT_FLT] bit. The conversion results for the analog inputs are available in MEAS_ANx register for the pack controller to read.

9.7 Cell balance control

The BMI7014 features fully protected integrated cell balancing drivers with fault diagnostics. The cell balancing feature is active in normal, sleep and diagnostic modes. The BMI7014 contains registers to control and monitor cell balance drivers and cell balance fault status.

The SYS_CFG1 register contains the CB_DRVEN bit. The CB_DRVEN bit must be enabled for any of the drivers to be activated. All drivers are disabled when CB_DRVEN bit is logic 0. For cell balance drivers to be active, both the SYS_CFG1[CB_DRVEN] and the CBx_CFG[CB_EN] bits must be set to logic 1.

The individual cell balance timer is set through the CBx_CFG[CB_TIMER]. Timing parameters can be found in the register map of this specification. Each time the cell balance CBx_CFG[CB_TIMER] bit is written by the MCU controller, the BMI7014 initiates the cell balance timer. It is important to explicitly mention, each time the CB_DRVEN bit is set to logic 0, then cell balancing timers get reset to 0 (the CBx_CFG[CB_TIMER] bits are unchanged) and all cell balancing MOSFETs are turned off. Before the CB_DRVEN bit is set again to logic 1, all CBx_CFG registers need to be configured again. Otherwise, a cell balancing sequence will be started with the previous settings.

The SYS_CFG1 register contains the CB_MANUAL_PAUSE bit, which, if set to logic 1, instructs the BMI7014 to disable the cell balance switches. When the CB_MANUAL_PAUSE bit is set again to logic 0, the cell balance switches are restored according to the programming. However, the cell balance timers are not frozen during a manual pause. The contents of CBx_CFG[CB_TIMER] and ADC2_OFFSET_COMP[ALLCBOFF ON SHORT] bits must not be changed while balancing.

It is not recommended to perform any cell measurement when cell balancing switches are activated, for two main reasons:

1) During Sleep mode, when cell balancing switches are ON, additional leakage current can be generated by the cell balancing activation which may cause a cell voltage measurement error.

2) The parasitic resistance on the cell terminal connections may also lead to a cell voltage measurement error which depends on the value of the CT parasitic resistance and on the cell balancing current.

In addition, due to the input cell low pass filter, it is required to wait a certain amount of time after opening the cell balancing switches before performing an accurate cell measurement sequence. This time depends on the input cell filter used. For the cell input filter described in Table 78, the waiting time recommended is 3ms. For similar reasons, it is also recommended to disable cyclic acquisitions when cell balancing is active to avoid false cell OV/UV fault detections. These recommendations are valid when the IC is in Normal mode or Sleep mode.

9.8 Internal IC temperature

Internal temperature measurement is completed automatically during each ADC conversion sequence. The MEAS_IC_TEMP register containing the IC temperature measurement may be read at any time by the pack controller. Resolution of MEAS_IC_TEMP is 32 mK/LSB.

9.9 Internal temperature fault

In addition to the digital temperature measurement register, the BMI7014 is equipped with a silicon overtemperature thermal shutdown (TSD). In the event the silicon thermal shutdown is activated in normal mode, the BMI7014 halts all monitoring operations and enters a low-power state with the FAULT pin activated. When the die temperature returns to normal, the BMI7014 resumes operation in normal mode.

In the event of an internal TSD:

1. Conversion sequence is aborted and the BMI7014 stops converting.
2. The FAULT2_STATUS[IC_TSD_FLT] bit is set to logic 1, implying a FAULT pin activation.
3. VCOM and VANA are in shut down, communication gets blocked.
4. All cell balance switches are disabled and CB_DRVEN cleared.

When the die temperature returns to normal level, the BMI7014 resumes to Init mode. Therefore, the user shall provide the device with an address and proper parameters again.

Overtemperature TSD events are also detected while the BMI7014 is in sleep mode during cyclic measurements. TSD events detected during the sleep mode cyclic measurement force the BMI7014 to set the IC_TSD_FLT bit and activate the FAULT pin while remaining in sleep mode. When the BMI7014 returns to normal operating temperature it transfers to normal mode and initiates a wake-up sequence on the bus.

9.10 Storage of parameters in an optional EEPROM

NXP provides parts with optimal calibration values. Standard parameters are stored in a read only memory called *fuses cell array*. It is typically neither necessary nor advised to change the standard values. Nevertheless, sometimes this might be required.

If the BMI7014 is linked to an EEPROM, the latter device is automatically recognized, provided the address $00 of the EEPROM contains the proper one byte key value, namely $CB hex. To program the EEPROM with calibration parameters, the user's final test and assembly must write to the EEPROM_CTRL register, providing address and data in EEPROM_CTRL[EEPROM_ADD] and EEPROM_CTRL[DATA_TO_WRITE] fields, with the EEPROM_CTRL[RW] bit set to logic 0. The user must simply send the write command with the EEPROM address and data to be written, and set the write bit to logic 0. The BMI7014 automatically writes the data to the given EEPROM address. To read data from the EEPROM, the user has to first write to the EEPROM_CTRL register, providing the address in EEPROM_CTRL[EEPROM_ADD] field, with the EEPROM_CTRL[RW] bit set to logic 1, then read in the same register to get the data in EEPROM_CTRL[READ_DATA] field.

Each time the part experiences a power up or reset event, an internal R/W memory, which is referred to as *mirror memory*, is first of all uploaded with the value of the fuses cell array. The content of such memory is propagated to the applicative part of the chip. All calibration values, before being used in the IC, are protected by an ECC (Error correction code). But if an EEPROM is recognized, the mirror registers bank, in which the content of the fuses memory was stored at the very beginning of the initialization process (transparent to the user), gets automatically reloaded with the content of the EEPROM.

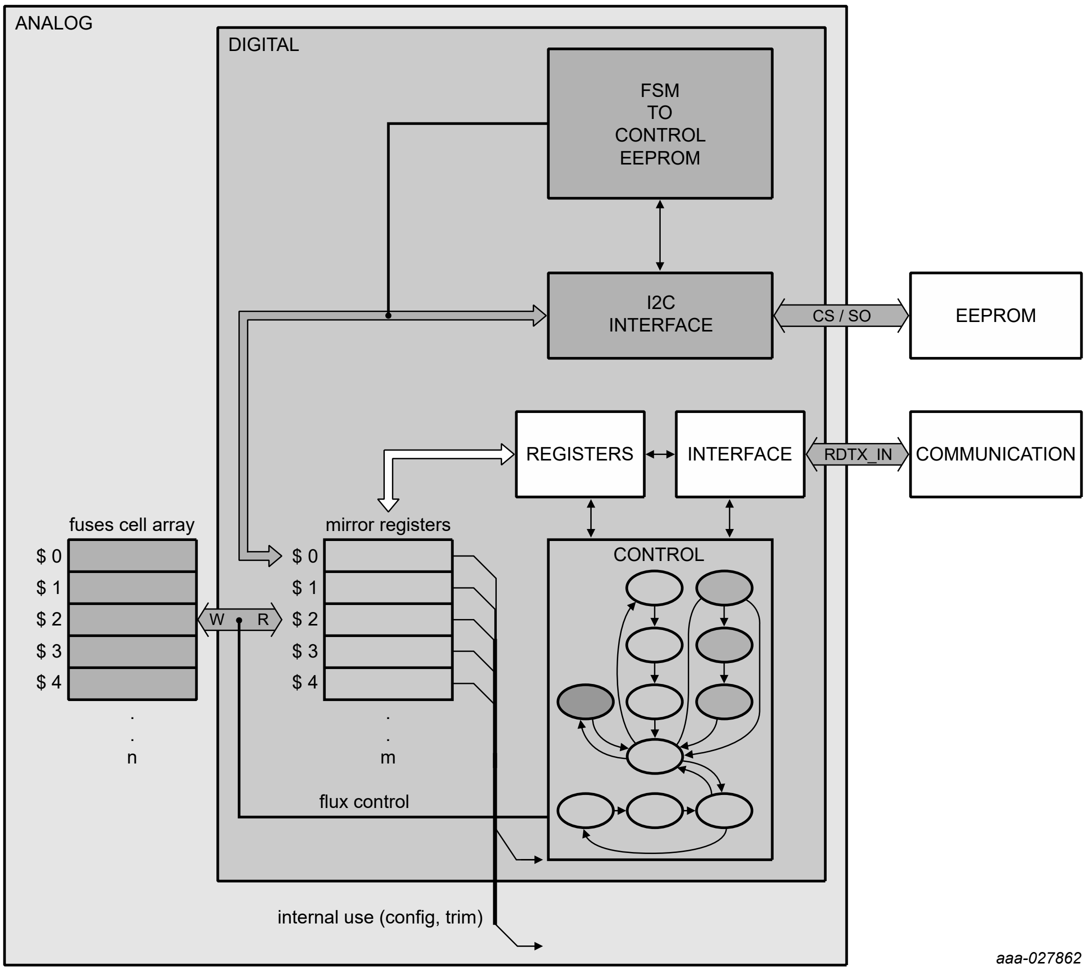


Figure 15. Memories

The space of EEPROM-addresses and the space of mirror-addresses correlate to each other. Mirror data are organized in 16-bit words, while the data of the EEPROM have been thought as bytes. As at EEPROM-address $00 there is the key value, the first calibration byte of the EEPROM must have EEPROM-address $01 and corresponds to the most significant byte of the mirror word having mirror-address $00. The second calibration byte of the EEPROM must have EEPROM-address $02 and corresponds to the least significant byte of the mirror word still having mirror-address $00, and so on.

This can be seen in Table 13. The columns labeled as "Gain comp.?" and "by …" show if the input signals are gain compensated (yes/no) and by which gain. For instance, GCF_c1 stays for a gain, which may be calculated by using GCF_room_c1, GCF_hot_c1 and GCF_cold_c1 variables specified in Table 77. In this table, attributes "cold" and "hot" refer to –40 °C and 89 °C respectively, and attribute room refers to 25 °C. A gain may or may not depend on the temperature (column "Temp. comp.?" may attain the value yes or no). If a gain depends on the IC temperature, there are three scalar gains. For instance: gain_cold_a, acq_gain_a, gain_hot_a represent respectively the delta gain compensation values at cold (−40 °C) vs room, room (+25 °C) and the delta gain compensation values at hot (+89 °C) vs. room temperature of the die. They are used to calculate, by delta gain compensation, the actual value of gain at any temperature.

Even if the most typical usage of the EEPROM is as storage of gains, nothing prevents the user to use it as a generic information storage. If this is the case, the first portion of the EEPROM has to be reserved to the copy of all gains, even if this is identical to the content of the fuse memory.

Table 12. Gain format

Gain = 1 + DG (DG)	Representation: 2's complement (number of bits)	Min (%)	Max (%)	Resolution (%)
GCF_room_cx (odd cell)	10	−6.2500	6.2378	0.01221
GCF_room_c(x+1)vs(x) (even cell vs odd cell)	4 for x = 1 2 for x ≠ 1	–0.098 for x = 1 –0.024 for x ≠ 1	0.085 for x = 1 0.012 for x ≠ 1	0.01221
GCF_cold_cx (odd cell) (cold temp vs room)	7 for x = 1 6 for x ≠ 1	–0.781 for x = 1 –0.391 for x ≠ 1	0.769 for x = 1 0.378 for x ≠ 1	0.01221
GCF_cold_c(x+1)vs(x) (even cell vs odd cell)	6 for x = 1 2 for x ≠ 1	–0.391 for x = 1 –0.024 for x ≠ 1	0.378 for x = 1 0.012 for x ≠ 1	0.01221
GCF_hot_cx (odd cell) (hot temp vs room)	7 for x = 1 6 for x ≠ 1	–0.781 for x = 1 –0.391 for x ≠ 1	–0.769 for x = 1 –0.378 for x ≠ 1	0.01221
GCF_hot_c(x+1)vs(x) (even cell vs odd cell)	5 for x = 1 3 for x ≠ 1	–0.195 for x = 1 –0.049 for x ≠ 1	0.183 for x = 1 0.037 for x ≠ 1	0.01221
GCF_Vbgtj1-2 (diagnostic voltage reference)[1]	8	−3.1250	3.1006	0.02441
GCF_stack (Stack voltage)	7	−3.1250	3.0762	0.04883
GCF_ANx_ratio (ANx ratio)	5	−1.5625	1.4648	0.09766
GCF_IcTemp (IC temperature)	4	−3.1250	2.7344	0.39063

[1] This gain compensation factor is relative to GCF_c1.

Table 13. Gain compensation

Measured channel	No.	Offset comp.?	Gain comp.?	By...	Temp. comp. ?	Result stored in…	…checked by…	… in the range of	
By ADC1-A									
ICTEMP1	1	Chopper	Yes	GCF_IcTemp	No	MEAS_IC_TEMP	N/A	N/A	N/A
ICTEMP1	2	Chopper	Yes	GCF_IcTemp	No	MEAS_IC_TEMP	N/A	N/A	N/A
CT1	3	Yes	Yes	GCF_c1	Yes	MEAS_CELL1	IC	CT1_UV_TH	CT1_OV_TH
CT2	4	Yes	Yes	GCF_c2	Yes	MEAS_CELL2	IC	CT2_UV_TH	CT2_OV_TH
CT3	5	Yes	Yes	GCF_c3	Yes	MEAS_CELL3	IC	CT3_UV_TH	CT3_OV_TH
CT4	6	Yes	Yes	GCF_c4	Yes	MEAS_CELL4	IC	CT4_UV_TH	CT4_OV_TH
CT5	7	Yes	Yes	GCF_c5	Yes	MEAS_CELL5	IC	CT5_UV_TH	CT5_OV_TH
CT6	8	Yes	Yes	GCF_c6	Yes	MEAS_CELL6	IC	CT6_UV_TH	CT6_OV_TH
AN0	9	Yes	Yes	GCF_ANx_ratio [1]	No [2]	MEAS_AN0	IC	AN0_UT_TH	AN0_OT_TH
AN1	10	Yes	Yes	GCF_ANx_ratio [2]	No [2]	MEAS_AN1	IC	AN1_UT_TH	AN1_OT_TH
AN2	11	Yes	Yes	GCF_ANx_ratio [2]	No [2]	MEAS_AN2	IC	AN2_UT_TH	AN2_OT_TH
AN3	12	Yes	Yes	GCF_ANx_ratio [2]	No [2]	MEAS_AN3	IC	AN3_UT_TH	AN3_OT_TH
AN4	13	Yes	Yes	GCF_ANx_ratio [2]	No [2]	MEAS_AN4	IC	AN4_UT_TH	AN4_OT_TH
AN5	14	Yes	Yes	GCF_ANx_ratio [2]	No [2]	MEAS_AN5	IC	AN5_UT_TH	AN5_OT_TH
AN6	15	Yes	Yes	GCF_ANx_ratio [2]	No [2]	MEAS_AN6	IC	AN6_UT_TH	AN6_OT_TH
V_{BG_TJ}	16	Yes	Yes	GCF_Vbgp1	Yes	MEAS_VBG_ DIAG_ADC1A	IC	thresholds vs. fuse_bg_ti	

Table 13. Gain compensation*...continued*

Measured channel	No.	Offset comp.?	Gain comp.?	By...	Temp. comp. ?	Result stored in…	…checked by…	… in the range of	
Reserved	17								
Reserved	18								
Reserved	19								
Reserved	20								
By ADC1-B									
CT7	1	Yes	Yes	GCF_c7	Yes	MEAS_CELL7	IC	CT7_UV_TH	CT7_OV_TH
CT8	2	Yes	Yes	GCF_c8	Yes	MEAS_CELL8	IC	CT8_UV_TH	CT8_OV_TH
CT9	3	Yes	Yes	GCF_c9	Yes	MEAS_CELL9	IC	CT9_UV_TH	CT9_OV_TH
CT10	4	Yes	Yes	GCF_c10	Yes	MEAS_CELL10	IC	CT10_UV_TH	CT10_OV_TH
CT11	5	Yes	Yes	GCF_c11	Yes	MEAS_CELL11	IC	CT11_UV_TH	CT11_OV_TH
CT12	6	Yes	Yes	GCF_c12	Yes	MEAS_CELL12	IC	CT12_UV_TH	CT12_OV_TH
CT13	7	Yes	Yes	GCF_c13	Yes	MEAS_CELL13	IC	CT13_UV_TH	CT13_OV_TH
CT14	8	Yes	Yes	GCF_c14	Yes	MEAS_CELL14	IC	CT14_UV_TH	CT14_OV_TH
Stack	9	Chopper	Yes	GCF_stack	No	MEAS_STACK	N/A	N/A	N/A
Stack	10	Chopper	Yes	GCF_stack	No	MEAS_STACK	N/A	N/A	N/A
Reserved	11	No	Yes	N/A	Yes	ADC1_B_RESULT	N/A	N/A	N/A
VANA	12	Yes	Yes	GCF_c1	Yes	ADC1_B_RESULT	IC	N/A	VANA_OV_ TH
V_{BG_TJ}	13	Yes	Yes	GCF_Vbgp2	Yes	MEAS_VBG_ DIAG_ADC1B	IC	thresholds vs. fuse_bg_ti	
Reserved	14								
Reserved	15								
Reserved	16								
Reserved	17								

[1] It is assumed that all ANx have been programmed as ratiometric; in case a certain ANx is programmed as an absolute input, the gain GCF_ANx_ratio gets replaced by GCF_c1 and the 'No' value contained in the column labeled 'Temp. comp. ?' is replaced by a 'Yes'.
[2] This gain compensation factor is relative to GCF_c1.

9.10.1 EEPROM content protection

If there is an EEPROM containing the equivalent of the fuse memory, some ECC bits are needed to protect them, as in the standard case of the fuse memory. The customized values and their own ECC values are completely independent on the NXP basic calibrations and their specific ECC stored in the fuses. Therefore, the user has to evaluate new ECC bits starting from its own calibration data and, finally, save both in the EEPROM.

There is a special calculation sheet the customer has to request from NXP. This sheet contains the correct values for DED_ENCODE_2 and DED_ENCODE_1 information, that is, ECC words used in the BMI7014 to detect a single error in the data and to correct it. In case of a double error, the problem can only be detected. However, in the normal usage, the SYS_CFG2[HAMM_ENCOD] bit has to be set at logic 0. It is recommended the value of such bit is periodically checked to be at logic 0. If the bit is not at logic 0, then it must be written at logic 0 again.

9.11 Mirror memory access

The mirror memory can be changed by using the FUSE_MIRROR_DATA and FUSE_MIRROR_CNTL general registers. The former contains the value of the data to be written into the mirror or to be read from it, while the latter contains the data address FMR_ADDR (whose value is in the range 0 to 31 decimal), some control fields (FSTM and FST) and a read only information about a possibly occurred detection and correction of data values (SEC_ERR_FLT).

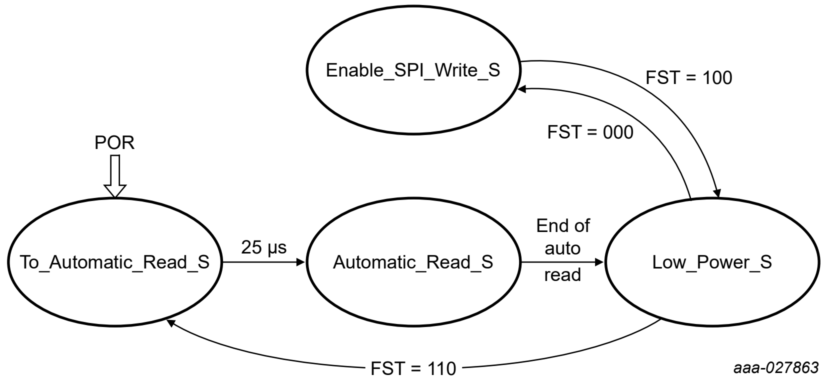


Figure 16. Mirror memory control

To manage the mirror memory the FSM of Figure 16 must be used.

Meaning of the states:

- To_Automatic_Read_S: transient state for slightly delaying the automatic read, after POR.
- Automatic_Read_S: in this state the entire bank of fuses is automatically transferred from analog matrix to the digital mirror.
- Low_Power_S: low power state; it must be the initial and final state of a sequence of write operations. This is the state where the mechanism idles after an automatic read.
- Enable_SPI_Write_S: state allows writing into the mirror.

Table 14. Sequence of read operations

Type of command	FSTM	FST	FMR_ADDR	FUSE_MIRROR_DATA
FUSE_MIRROR_CNTL[FMR_ADDR] set	0	000	00000	X
FUSE_MIRROR_DATA	X	X	X	data read at addr $0
FUSE_MIRROR_CNTL[FMR_ADDR] set	0	000	00001	X
FUSE_MIRROR_DATA	X	X	X	data read at addr $1
FUSE_MIRROR_CNTL[FMR_ADDR] set	0	000	00010	X
FUSE_MIRROR_DATA read	X	X	X	data read at addr $2

The read sequence may be useful, for example when the user wants to read the traceability information (serial number) contained in some specific words of the mirror memory. See Table 34 and Table 77.

Table 15. Sequence of write operations

Type of command	FSTM	FST	FMR_ADDR	FUSE_MIRROR_DATA
FUSE_MIRROR_CNTL to enable writing	1	000	00000	X
FUSE_MIRROR_CNTL[FMR_ADDR] at $0	1	000	00000	X
FUSE_MIRROR_DATA	X	X	X	Data to be written at addr $0
FUSE_MIRROR_CNTL[FMR_ADDR] at $1	1	000	00001	X

Table 15. Sequence of write operations*...continued*

Type of command	FSTM	FST	FMR_ADDR	FUSE_MIRROR_DATA
FUSE_MIRROR_DATA	X	X	X	Data to be written at addr $1
FUSE_MIRROR_CNTL[FMR_ADDR] at $2	1	000	00010	X
FUSE_MIRROR_DATA	X	X	X	Data to be written at addr $2
FUSE_MIRROR_CNTL to low power	1	100	X	X

10 Communication

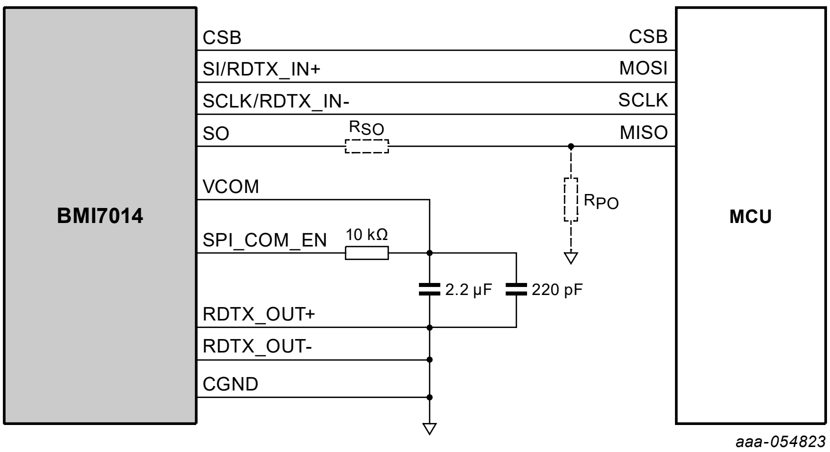
The BMI7014 is designed to support serial peripheral interface (SPI) or transformer physical layer (TPL) communication.

SPI communication uses the standard CSB to select the BMI7014 and clocks data in and out using SCLK, SI, and SO. Using SPI to communicate to the BMI7014 provides system isolation when used in conjunction with galvanic isolators. Serial communication is enabled using the SPI_COM_EN pin. To select SPI communication, the SPI_COM_EN pin must be terminated to the VCOM supply. Terminating the SPI_COM_EN pin to CGND pin selects TPL communication. Systems using only SPI communication to the BMI7014 may leave RDTX_OUT+ and RDTX_OUT– unterminated or may short them to ground.

During initialization, each BMI7014 device is assigned a specific address by the MCU by writing a non-zero value to INIT[CID] bit field. Only the BMI7014 with the correct address acts upon and responds to the request from MCU. After initialization, the MCU may communicate globally to all slave devices by using a global command. No response is generated when a global command is received by each slave device in the chain.

Note: *The BMI7014 supports only one communication method at a time and is determined by the state of SPI_COM_EN pin. Changing the state of the SPI_COM_EN pin after POR and VCOM is in regulation is considered a communication fault, and sets the COM_LOSS_FLT bit. The BMI7014 remains in same configuration determined at POR.*

10.1 SPI communication



In the presence of 3.3 V SPI interface, resistors represented by a dotted line could have R_{SO} = 5.23 kΩ and R_{PO} = 10 kΩ. For a 5.0 V SPI interface, it must be R_{SO} = 0 Ω (short) and R_{PO} = ∞ (open).

Figure 17. SPI interface termination

SPI input signal levels to the BMI7014 operate at 5.0 V logic levels but are 3.3 V compatible.

The SO output driver provides 5.0 V levels only and therefore must be attenuated to be compatible with a 3.3 V MCU.

The BMI7014 SPI interface is a standard SPI interface with a chip select (CSB), clock (SCLK), master in slave out (MISO), and master out slave in (MOSI). The SI/SO shifting of the data follows a first-in-first-out method, with both input and output words transferring the most significant bit (MSB) first. All SPI communication to the BMI7014 is controlled by the microcontroller.

One 48-bit message frame for previously requested data is retrieved through serial out for each current serial in message sent by the MCU. For message integrity and communication robustness, each SPI transmit message consists of nine bit fields with a total of 48 bits message frame. The nine transmit fields are defined as following:

1. Register data (16 bits).
2. Master/slave (1 bit), always at 1 in the response.
3. Register address (7 bits).
4. Reserved (2 bits).
5. Cluster ID (6 bits).
6. Message counter (4 bits).
7. Reserved (2 bits).
8. Command (2 bits).
9. Cyclic redundancy check (8 bits)

Messages having less or more than 48 bits, incorrect CRC, or incorrect SCLK phase are disregarded. Communication faults set the COM_ERR_FLT fault bit in the FAULT1_STATUS register and increments the COM_STATUS[COM_ERR_COUNT] register.

Note: *It is required that the SCLK input is low before the falling edge of CSB (SCLK phase).*

Table 16. SPI command format

Register data	Master/ slave	Register address	Reserved	Device address (cluster ID)	Message counter	Reserved	Command	CRC
Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]

Information is transferred to and from the BMI7014 through the read and write commands. After a power-up (POR) or RESET (pin) or SYS_CFG1[SOFT_RST], the BMI7014 device only responds to the cluster ID of 00 0000b. The user must change the cluster ID of the device by writing a new cluster ID into register INIT[CID]. Subsequent read/write command must use the new cluster ID to communicate to the device. Whatever the type of transmitted message, the master has to write a logic 0 in the master/slave bit. Any message transmitted by the user with master/slave bit set to 1 or with wrong CID is treated as Invalid request by BMI7014.

Notes:

- *In SPI communication, global write commands are not allowed and the BMI7014 responds with all bit field set to zero except message counter and correct CRC, in the subsequent message frame.*
- *In SPI communication, the BMI7014 responds with all bit filed set to zero except message counter and correct CRC to an invalid request from MCU.*
- *In SPI communication, the BMI7014 responds with all bit filed set to zero except message counter and the correct CRC to the very first BMI7014/ MCU message frame.*

The response message sent by BMI7014 to MCU is similar to the receive message and includes the 4-bit message counter. The Message counter is a local counter to BMI7014. It is increased by one for each new response transmitted by BMI7014, this applies also to auto read generated by BMI7014 for write and NOP commands. It is recommended that the MCU compares the message counter value of two consecutive responses transmitted by BMI7014, if the values are same then MCU shall treat the messages as error.

1. Register data (16 bits)
2. Master/slave (1 bit)
3. Register address (7 bits)

4. Reserved (2 bits)
5. Cluster ID (6 bits)
6. Message counter (4 bits)
7. Reserved (2 bits)
8. Command (2 bits)
9. Cyclic redundancy check (8 bit)

Table 17. SPI response format

Register data	Master/ slave	Register address	Reserved	Device address (cluster ID)	Message counter	Reserved	Command	CRC
Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]

To initiate communication, the MCU transitions CSB from high to low. The data from the MCU is sent with the most significant bit first. The SI data is latched by the device on the falling edge of SCLK. Data on SO is changed on the rising edge of SCLK and read by MCU on the falling edge of SCLK. The SO response message is dependent on the previous command.

Falling edge of CSB initiates the following:

1. Enables the SI Input
2. Enables the SO output driver

Rising edge of CSB initiates the following operation:

1. Disables the SO driver (high-impedance)
2. Activates the received 48-bit command word allowing the BMI7014 to act upon the new command

Notes:

- *The BMI7014 responds to a NO_OPERATION command with a NO_OPERATION response (with increased message counter value) in the subsequent response.*
- *After initialization, when writing to a register, the BMI7014 responds with an auto read of the register which was written in the subsequent write request.*
- *The BMI7014 does not execute any command if the master/slave bit is equal to logic 1.*

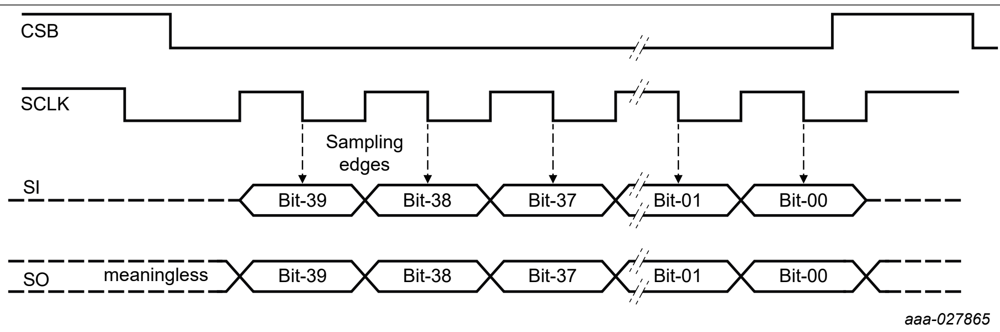


Figure 18. SPI transmission

10.2 TPL communication

High speed differential isolated communication is achieved through the use of transformer or capacitive isolation. Terminating the SPI_COM_EN pin to the CGND pin selects transformer communication. For transformer communication (TPL), an MC33664 IC is required between the BMI7014 IC and the MCU, as shown in Figure 46

For TPL communication, it is recommended that the device is terminated as shown in Figure 46. Component values are given in Section 12.2 "BMI7014 external components".

The BMI7014 IC is equipped with a bidirectional transceivers for upstream and downstream communication. The bidirectional transceiver is implemented to support up to 63 nodes in one daisy chain (CID = 00 0000b is reserved for network initialization). The message received by the receiver on one port of BMI7014 is retransmitted by the transmitter of the opposite port of BMI7014. This ensures that the message is not attenuated as it propagates through the daisy chain. Each node in the daisy chain adds a delay of t_{port_delay} for forwarding messages in the daisy chain.

In TPL communication, the CSB pin may be used as a wake-up input. During Sleep mode, an edge transition of the CSB initiates the wake-up function. Alternatively, the CSB pin may be shorted to ground or software masked to prevent undesired wake-up events.

Communication between the pack controller and the BMI7014 is half duplex communication with transformer isolation. Transformer physical layer in the pack controller creates a pulse phase modulated signal transmitted to the bus through the transformer. The BMI7014 physical layer is equipped with a segment-based transmitter, which is used as a terminating resistor (internally) during the receive mode. The default value of terminating resistance is set to 120 Ω for impedance matching and network stability. In TPL communication, the BMI7014 IC is always electrically connected to its neighbouring BMI7014 ICs in a daisy chain.

10.2.1 TPL Encoding

The transformer physical layer (TPL) uses pulse encoded symbols for communication. The three signal pulses used for encoding positive (P,black), negative (N, red) and zero (M, black) are shown in Figure 19 .

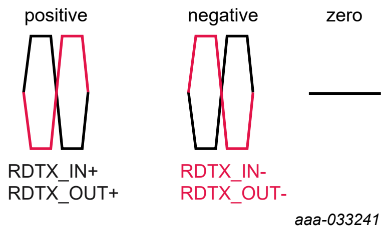


Figure 19. TPL Pulses

Start-of-message and end-of-message symbols are generated by the transformer driver and always occur at the start and end of the communication message. The start-of-message symbol and end-of-message symbol each contain two complete signal pulses. The start-of-message symbol produces a double pulse with a logic 1 phase. End-of-message produces a double pulse with logic 0 phase. Data pulses are single period pulse waves that indicate logic 1 or 0, based on the phase. The four symbols shown in Table 18 are used.

Table 18. TPL encoding

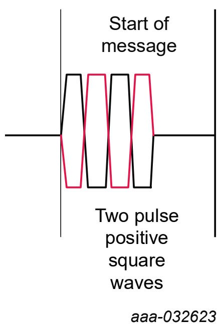
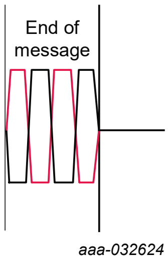
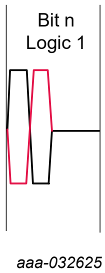
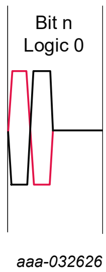
Symbols	Pulse modulation	Description
Start-of-message (SOM)	 **Figure 20. SOM**	positive phase, double pulse (and plus pause)

Table 18. TPL encoding *...continued*

Symbols	Pulse modulation	Description
End-of-message (EOM)	 **Figure 21. EOM**	negative phase, double pulse
Logic 1	 **Figure 22. Logic 1**	positive phase, single pulse (and plus pause)
Logic 0	 **Figure 23. Logic 0**	negative phase, single pulse (and plus pause)

10.2.2 Command message bit order

Same as in Section 10.1 "SPI communication"

10.2.3 Response message bit order

Same as in Section 10.1 "SPI communication"

10.2.4 Transformer communication format

Command and response frames are exchanged primarily between a single master and any single slave. One exception is the use of a global command, which can be transmitted from one master to multiple slaves, but includes no slave response. The purpose of the command and response transactions are to read and write to registers within the slave register map.

The command and response communication structure provides all context information required for unambiguous single-exchange transactions for extended memory applications requiring efficient memory access.

The message structures have predefined fixed bit length frames and defined timing between transfers. To transfer data efficiently from the slave, multiple response packets may be requested by the read command. The BMI7014 defines a set of fields that constitute the command and response message structure.

Transformer message format is identical to the SPI format. Command message frames consist of nine fields containing exactly 48 bits. The response structure is similar to the SPI format.

After initialization, information is transferred to and from the BMI7014 through the read and write commands. On Power Up or POR, the first BMI7014 device in the chain responds to address 00 0000b[3] [4]. The user must program the first device with a new address by writing to the INIT[CID] register. Programming the device with a new address allows the pack controller to communicate and initialize the next device in the daisy chain. Subsequent read/write commands to the next device must use the new address to communicate.

All write commands sent by the master must consist of a single frame. The slave device does not generate any response to a write command from master but only acts on it. Similarly, the slave device does not generate any response nor performs any operation after receiving a valid NOP message from the master.

Read commands sent by the master may generate a single response or multiple responses depending on the parameters set in the read request. The packet size and memory start location are identified in the read command sent by the master.

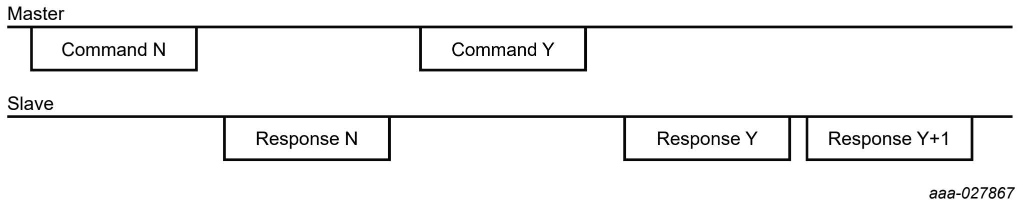


Figure 24. Bus traffic example

No response is generated by a slave BMI7014 when a corrupted message is received. Confirmation that a global write command is received by the slave must be done by reading the register in which it was written.

In cases where a bus error occurs, due to induced noise or a bus fault, the slave detects bad data transfers. The BMI7014 slave reacts to communication faults by setting the FAULT1_STATUS[COM_ERR_FLT] and incrementing the COM_STATUS[COM_ERR_COUNT] register.

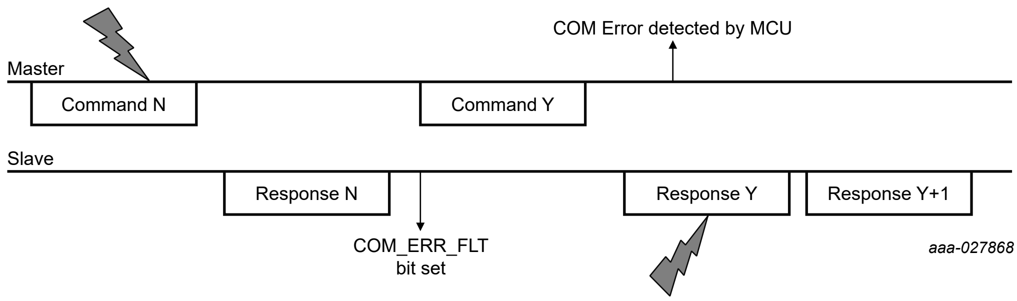


Figure 25. Bus traffic with receive error and recovery

All valid read commands sent to an individual slave provide a response. In the event a slave does not respond to a read request message, the master must assume the message was corrupted or lost. To recover from the event, the master must retransmit the message. Corrupted messages received by the master are detected through an incorrect CRC code. To recover, the master must request the data again.

3 A slave device at POR with INIT[CID] = 00 0000b responds only at the port it received the request.
4 A slave device with CID = 00 0000b does not forward messages.

10.2.5 Transformer communication timing

Command and response message frames are to be sent and received at 2.0 Mbps bit rate. The response to a first read request command is provided within t_{RES} of the end of the frame. However, two consecutive message responses transmitted by BMI7014 IC for burst read request are separated by t_{TPL_TD} time as shown in Figure 26.

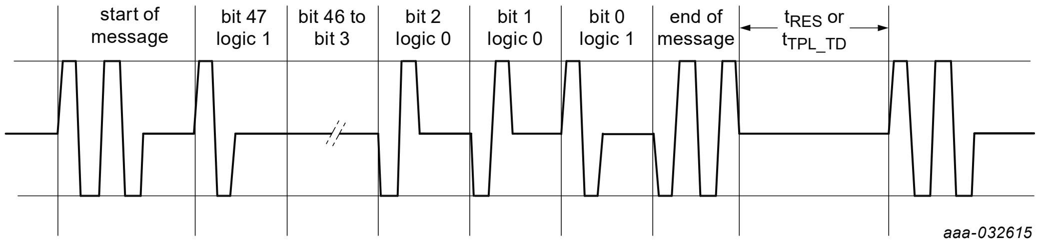


Figure 26. Transformer communication waveforms

Each sent and received message starts with Start of Message (SOM) bit followed by a 48-bit message and ends with an End of Message (EOM) bit.

10.2.6 Transformer communication wake-up

In TPL communication, the system wake-up can be triggered by either the BMI7014 IC (wake-up due to internal event) or the pack controller (MCU). In both cases, a dedicated wake-up pulse sequence is used. The wake-up pulse sequence consists of two transmit messages with or without no data transmitted. The messages are separated by a delay time (t_{WAKE_DELAY}). Each message contains a SOM and EOM symbol.

10.2.6.1 BMI7014 System wake-up

By default, the internal event wake-up capability of the BMI7014 is disabled. When enabled and in the event the BMI7014 detects a wake-up condition, the device initiates a wake-up pulse sequence on the bus to alert the pack controller. The BMI7014 IC initiating the wake-up, due to an internal event, sends the wake-up sequence upstream and downstream in the daisy chain to ensure the wake-up message propagates along the entire chain to the pack controller. Each neighbouring BMI7014 IC in daisy chain forwards the received wake-up sequence opposite to the direction where it received the wake-up sequence. In this process, all BMI7014 devices in the daisy chain, along with the pack controller, are awoken. After the pack controller gets awoken; it is recommended the pack controller interrogate each BMI7014 in the system to determine the source of the wake-up.

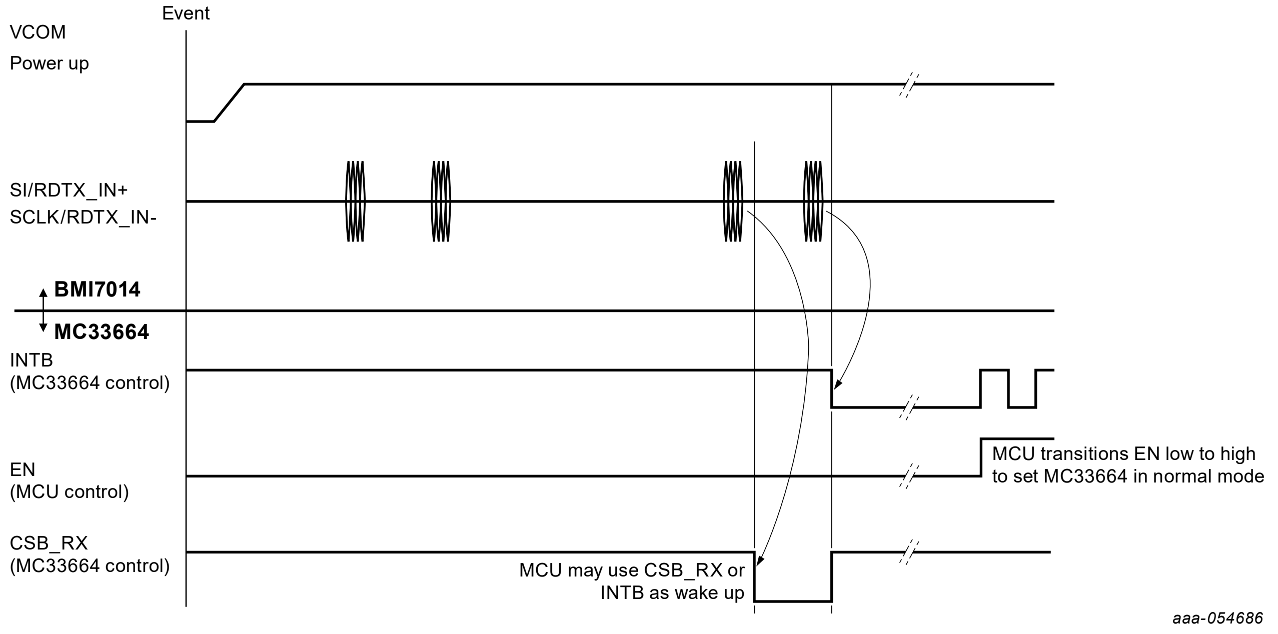


Figure 27. BMI7014 system wake-up

Note: *The system wake-up performed by BMI7014 IC in case of any internal event is disabled by default. This wake-up can be activated by writing to register WAKEUP_MASK1, WAKEUP_MASK2 and WAKEUP_MASK3.*

10.2.6.2 Pack controller system wake-up

The pack controller can also perform system wake-up by sending a wake-up sequence to the first BMI7014 IC. The pack controller can use the CSB_TX pin of the MC33664 to generate SOM and EOM with correct timing.

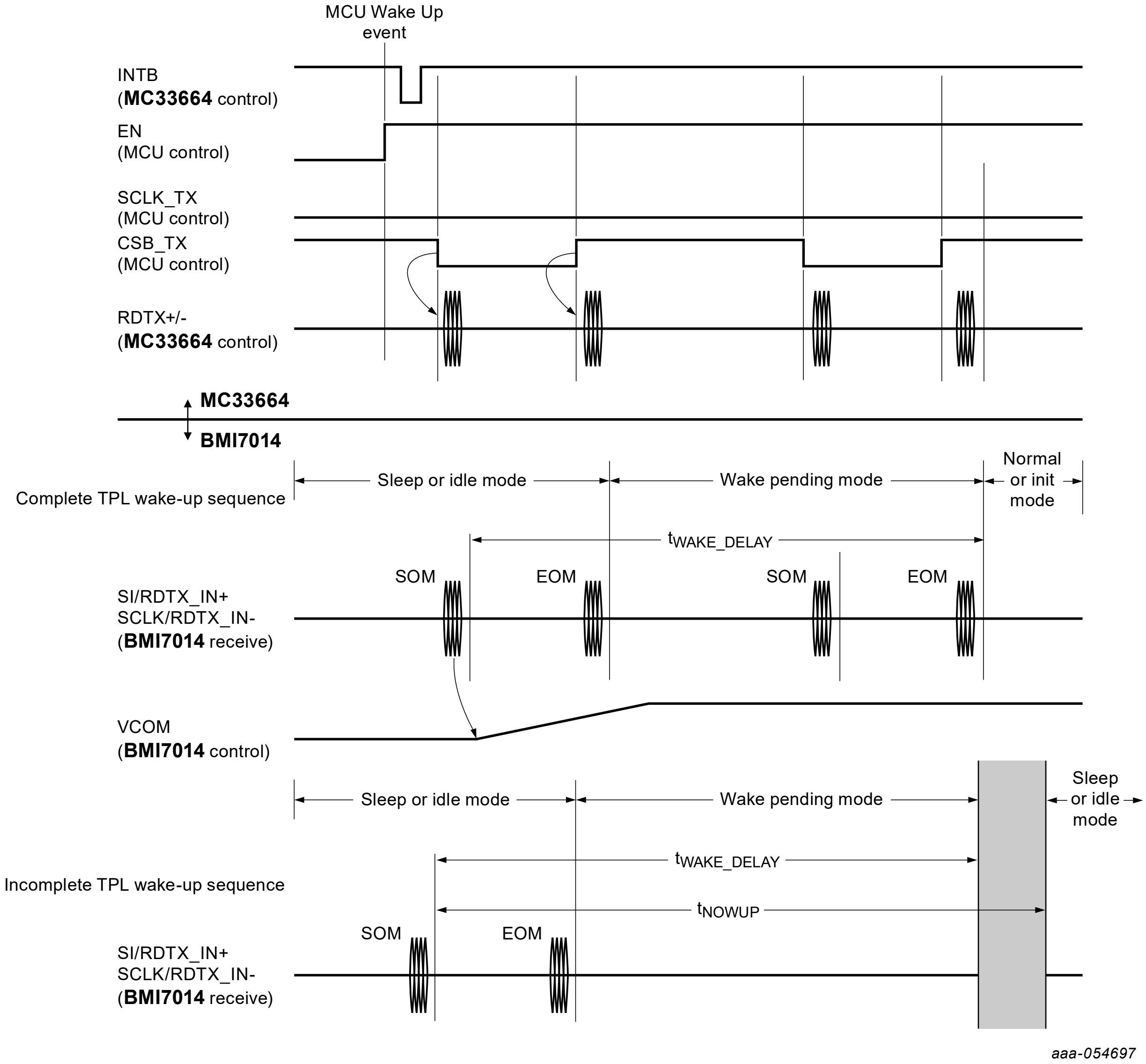


Figure 28. Pack controller system wake-up

If the device is in Sleep mode, each successive slave device awoken by the wake-up message on the bus, generates a new wake-up message for its neighbor. The message is to be transmitted in one direction only on the bus. The direction of transmission of the wake-up message on the bus is always at the opposite port of the received wake-up message. In the unlikely event of a collision, the message at the lower port (RDTX_IN) is given a higher priority than the message at the higher port (RDTX_OUT).

Note:

- *Any write message of any length can be used to generate both wake-up pulses and obtain a valid device wake-up.*
- *The second wake-up message should be sent after a minimum time of t_{WAKE_DELAY} (min) from the first SOM reception.*
- *The device falls back to Sleep or Idle mode when an SOM followed by EOM is not received in t_{WAKE_DELAY} (max).*
- *If the wake-up sequence is incomplete, then a new wake-up attempt can only be done after a t_{NOWUP} delay. See Figure 28.*

- *The pack controller must wait for t_{WU_Wait} ms per node to communicate with the BMI7014 ICs after sending the first wake-up message. For example, given that the BMI7014 IC is enumerated, with 10 nodes in a daisy chain the pack controller must wait 7.5 ms before communicating to BMI7014 IC. The waiting time allows all the BMI7014 ICs in the system to transition to normal mode.*
- *The pack controller must use only one master node to perform wake-up of devices.*

10.3 CRC generation

The master and slaves calculate a CRC on the entire message using the processes detailed in this section.

The command and response CRC is fixed at 8 bits in length. The CRC is calculated using the polynomial $x^8 + x^5 + x^3 + x^2 + x + 1$ (identified by 0x2F) with a seed value of binary 11111111.

An example CRC encoding HW implementation is shown in Figure 29.

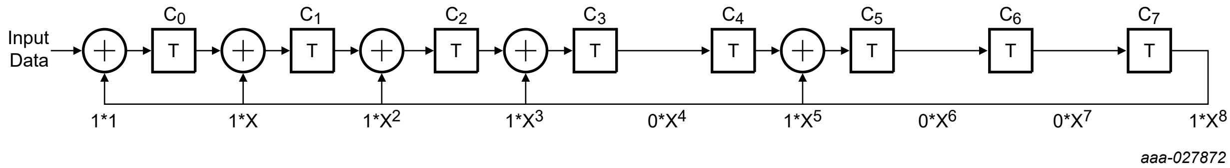


Figure 29. Command and response mode – example CRC encoder

The effect of the CRC encoding procedure is shown in the following table. The seed value is appended into the most significant bits of the shift register.

Table 19. Data preparation for CRC encoding

Seed	Register data	Master / Slave	Register address	Reserved	Cluster ID	Message counter	Reserved	Cmd
1111_1111	Bits [47:32]	Bit [31]	Bits [30:24]	Bits[23:22]	Bits[21:16]	Bits[15:12]	Bits[11:10]	Bits[9:8]

Seed…	…padded with the message to encode…	…padded with 8 zeros

1. Using a serial CRC calculation method, the transmitter rotates the seed and data into the least significant bits of the shift register.
2. During the serial CRC calculation, the seed and the data bits are XOR compared with the polynomial data bits. When the MSB is logic 1, the comparison result is loaded in the register, otherwise the data bits are simply shifted. It must be noted the 48-bit message to be processed must have the bits corresponding to the CRC byte all equal to zero (00000000).
3. Once the CRC is calculated, it replaces the CRC byte initially set to all zeros and is transmitted.

Following is the procedure for the CRC decoding:

1. The seed value is loaded into the most significant bits of the receive register.
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first).
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result.
   - If the shift register contains all zeros, the CRC is correct.
   - If the shift register contains a value other than zero, the CRC is incorrect.

CRC calculation examples:

Table 20. Command CRC calculation examples

Data 16 bit (Hex)	Master/slave bit and memory address, 8 bit (Hex)	Reserved (2 bits) and Cluster Id (6 bit), 8 bit (Hex)	Message counter, 4 bit (Hex)	Reserved (2 bits) and Command (2 bits), 4 bit (Hex)	CRC 8 bit (Hex)	Frame 48 bit (Hex)
0x0101	0x08	0x01	0x3	0x0	0x3C	0x0101080130 3C
0x0A0A	0x01	0x0A	0x9	0x1	0x84	0x0A0A010A9 184
0x01C4	0x0F	0x02	0x1	0x2	0x26	0x01C40F0212 26
0x7257	0x01	0x05	0x7	0x3	0xC7	0x7257010573 C7

Table 21. Response CRC calculation examples

Data 16 bit (Hex)	Master/slave bit and memory address, 8 bit (Hex)	Reserved (2 bits) and Cluster Id (6 bit), 8 bit (Hex)	Message counter 4 bit (Hex)	Reserved (2 bits) and Command (2 bits), 4 bit (Hex)	CRC 8 bit (Hex)	Frame 48 bit (Hex)
0x1101	0x89	0x01	0x3	0x0	0x26	0x1101890130 26
0x2002	0x89	0x05	0x9	0x0	0x7A	0x2002890590 7A
0x5103	0x89	0x0A	0x1	0x5	0x07	0x5103890A1 507
0xFF04	0x89	0x06	0x7	0x2	0xA6	0xFF04890672 A6

10.4 Commands

10.4.1 Read command and response

Read command is intended to be used for SPI and transformer interface. The read command is a local command used for retrieving data from the BMI7014 device. The data field contains the number of data registers to be returned. Requesting data from registers greater than address $7F forces the device to loop the register counter back to register $00.

Table 22. Read command table

Command name	Register data		Response/ Command	Register address	Reserved	Device address (cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]		Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Read command	XXXX XXXX X	NRT-01 to 7F	0b	Register address	xxb	CID	xxxxb	xxb	01b	CRC

Table 23. Read response table

Command name	Register data	Response/ Command	Register address	Reserved	Device address (cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Read MsgCntr Response	Register Data	1b	Register address	00b	CID	MsgCntr	00b	01b	CRC

Table 24. Legend for read command, read response tables

Read command		Read response	
Bit[7:0]	= 8-bit CRC	Bit[7:0]	= 8-bit CRC
Bit[9:8]	= Command (01b)	Bit[9:8]	= Command field (01b)
Bit[11:10]	= Reserved (xxb)	Bit[11:10]	= Reserved (00b)
Bit[15:12]	= Message counter	Bit[15:12]	= Message counter
Bit[21:16]	= Device address (Cluster ID)	Bit[21:16]	= Device address (Cluster ID)
Bit[23:22]	= Reserved = X, don't care	Bit[23:22]	= Reserved (00b)
Bit[30:24]	= Register address	Bit[30:24]	= Register address
Bit[31]	= Master/slave = 0b (master)	Bit[31]	= Response/Command = 1b(slave)
Bit[39:32]	= NRT, number of registers to transfer back. Max is $7F, loop back on address $00	Bit[47:32]	= Data at memory address
Bit[47:40]	= X, don't care		

Notes:

- *The read command is a local command*
- *Requesting a read of a reserved register provides a $0000 data response*
- *Registers are read-only on devices that have not been initialized*
- *Requesting a number of NRT equal to 00 is the same as requesting 01*
- *The MsgCntr is a local counter of BMI7014 IC. It is only increased by the node responding to MCU request. The node increases the value of MsgCntr by 1 with each new response transmitted by BMI7014. On saturation of this counter it restarts from 0000b.*
- *The initial value of message counter is 0000b and first response transmitted by BMI7014 has the message counter value set to 0000b.*

10.4.2 Local write command

Unlike the read command, for which BMI7014 responds with data, the write command does not generate any response. When the slave receives a valid local write command, the message is acted upon but no response is generated. Writing to read only registers does not allow the register content to be updated.

Table 25. Write command table

Command name	Register data	Response/ Command	Register address	Reserved	Device address (cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Write command	Register Data	0b	Register address	xxb	CID	xxxxb	xxb	10b	CRC

Table 26. Legend for write command and write response tables

Write command	
Bit[7:0]	= 8-bit CRC
Bit[9:8]	= Command (10b)
Bit[11:10]	= Reserved (xxb)
Bit[15:12]	= Message counter (xxxxb)
Bit[21:16]	= Device address (cluster ID)
Bit[23:22]	= Reserved (xxb)
Bit[30:24]	= Register address
Bit[31]	= Response/Command = 0b
Bit[47:32]	= Register Data

Note: *Writing to reserved registers performs no operation and loads no data in the reserved register.*

10.4.3 Global write command

The global write command allows the transformer user to communicate to all devices on the bus at the same time. The global write command is useful to program all devices at the same time with values for fault threshold or to synchronize conversions for all devices on the bus. When a slave receives a valid global write command, the message is acted upon, but no response is generated.

Table 27. Global write command table

Command name	Register data	Response/ Command	Register address	Reserved	Device address (cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Global Write command	Register Data	0b	Register address	xxb	XX XXXXb (global)	MsgCntr	xxb	11b	CRC

Table 28. Legend for global write command table

Write command	
Bit[7:0]	= 8-bit CRC
Bit[9:8]	= Command field (11b)
Bit[11:10]	= Reserved (xxb)
Bit[15:12]	= Message counter = xxxxb (global)
Bit[21:16]	= Device address (Cluster ID) = xx xxxxb (global)
Bit[23:22]	= Reserved = xxb, Don't care
Bit[30:24]	= Register address
Bit[31]	= Response/Command = 0b
Bit[47:32]	= Register Data

10.4.4 No operation command

The No Operation (NOP) command allows the user to reset the communication time-out timer of the BMI7014. If the pack controller has no new request for BMI7014 IC but does not want the BMI7014 to reset (and lose its CID address), it can send a NOP command to the BMI7014 IC. The NOP command does not trigger any response or operation from the BMI7014. Thus, the NOP command can be used by the pack controller like a ping to prevent the IC from resetting itself.

Table 29. No operation command table

Command name	Register data	Response/ Command	Register address	Reserved	Device address (cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
No operation (NOP) command	Register Data	0b	Register address	xxb	CID	xxxxb	xxb	00b	CRC

Table 30. Legend for no operation command and no operation response tables

Write command	
Bit[7:0]	= 8-bit CRC
Bit[9:8]	= Command field (00b)
Bit[11:10]	= Reserved (xxb)
Bit[15:12]	= Message counter
Bit[21:16]	= Device address (Cluster ID) = CID
Bit[23:22]	= Reserved = xxb, Don't care
Bit[30:24]	= Register address
Bit[31]	= Response/Command = 0b
Bit[47:32]	= Register Data

10.4.5 Command and response summary

Table 31. Command summary table

Command name	Register data	Response/ Command	Register address	Reserved	Device address (Cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
NOP command	xxxx xxxxb	0b	xxx xxxxb	xxb	CID	XXXXb	XXb	00b	CRC
Read command	Number of registers	0b	Register address	xxb	CID	XXXXb	XXb	01b	CRC
Write command	Register Data	0b	Register address	xxb	CID	XXXXb	XXb	10b	CRC
Global write command	Register Data	0b	Register address	xxb	XX XXXXb	XXXXb	XXb	11b	CRC

If a device has its cluster ID (CID) equal to 00 0000b, then only its INIT register can be written by the pack controller. All the BMI7014 devices have their First message from MCU controller writing to cluster ID 00 0000b. To perform a read/write operation of any register (other than INIT) of BMI7014 IC, the MCU must first assign a unique address to each BMI7014 device by writing to its INIT register with a suitable CID value. The process of assigning a unique CID address to each slave device by the pack controller is called *initialization*.

After initialization, each time the device receives a frame having the master/slave bit equal to logic 1, this frame is not recognized, even though the address contained in the CID field is equal to the programmed one. In this condition, the device neither acts upon nor answers the command. This is a normal behavior, whose purpose is to avoid the device acting upon or responding to a frame generated by another slave device of the network.

Table 32. Response summary table

Command name	Register data	Response/ Command	Register address	Reserved	Device address (Cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Read response	Register Data	1b	Register address	00b	CID	MsgCntr	XXb	01b	CRC

10.5 I^{2}C communication interface

As an optional feature, the BMI7014 has an integrated I^{2}C communication link to an external local EEPROM, which may be used to store calibration parameters defined by the user. If the EEPROM is not used, then the SCL and SDA pins must be left open. When this occurs, the FAULT1_STATUS[I2C_ERR_FLT] bit is automatically updated to logic 1. The automatic update happens even if an error bit is masked. If no EEPROM is mounted, the pack controller has to ignore the content of FAULT1_STATUS[I2C_ERR_FLT].

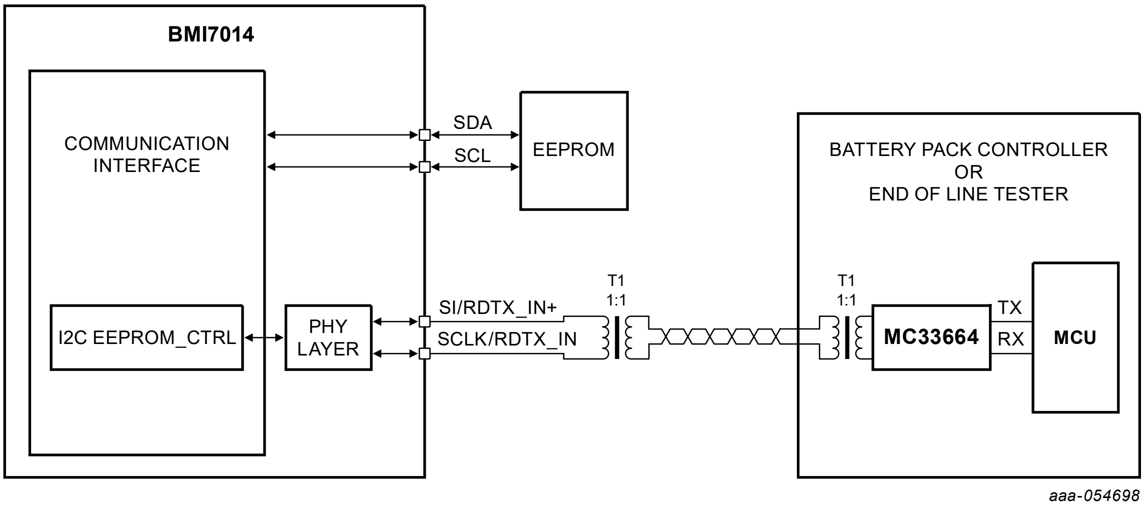


Figure 30. BMI7014 calibration registers

11 Registers

11.1 Register map

Important: *Trying to access registers marked as reserved produces responses having all zeros in the data field.*

Unless otherwise stated, in all register descriptions, POR means one of the following:

- Power-on reset
- Hardware reset
- Software reset
- Reset event based on SYS_CFG2[FLT_RST_CFG] register configuration

Table 33. Register table

Register		Response	Reference	Description	Notes
A[6:0]	Symbol				
$00	Reserved	Table 23		Reserved	Not readable or writeable
$01	INIT	Table 23	Section 11.2	Device initialization	Global write is forbidden for CID
$02	SYS_CFG_ GLOBAL	Table 23	Section 11.3	Global system configuration	Only accessible through a global access in transformer mode. In SPI mode it can be written by a standard write command.
$03	SYS_CFG1	Table 23	Section 11.4	System configuration	
$04	SYS_CFG2	Table 23	Section 11.5	System configuration	

Table 33. Register table*...continued*

Register		Response	Reference	Description	Notes
A[6:0]	Symbol				
$05	SYS_DIAG	Table 23	Section 11.6	System diagnostic	Writable in DIAG mode only, automatically cleared when exiting DIAG mode
$06	ADC_CFG	Table 23	Section 11.7	ADC configuration	
$07	CB_SHORT_CFG	Table 23	Section 11.8	CB short event configuration	
$08	OV_UV_EN	Table 23	Section 11.9	CT measurement selection	
$09	CELL_OV_FLT	Table 23	Section 11.10	CT overvoltage fault	
$0A	CELL_UV_FLT	Table 23	Section 11.11	CT undervoltage fault	
$0B	TPL_CFG	Table 23	Section 11.12	TPL configuration for up and down Transmitter	
$0C	CB1_CFG	Table 23	Section 11.13	CB configuration for cell 1	
$0D	CB2_CFG	Table 23	Section 11.13	CB configuration for cell 2	
$0E	CB3_CFG	Table 23	Section 11.13	CB configuration for cell 3	
$0F	CB4_CFG	Table 23	Section 11.13	CB configuration for cell 4	
$10	CB5_CFG	Table 23	Section 11.13	CB configuration for cell 5	
$11	CB6_CFG	Table 23	Section 11.13	CB configuration for cell 6	
$12	CB7_CFG	Table 23	Section 11.13	CB configuration for cell 7	
$13	CB8_CFG	Table 23	Section 11.13	CB configuration for cell 8	
$14	CB9_CFG	Table 23	Section 11.13	CB configuration for cell 9	
$15	CB10_CFG	Table 23	Section 11.13	CB configuration for cell 10	
$16	CB11_CFG	Table 23	Section 11.13	CB configuration for cell 11	
$17	CB12_CFG	Table 23	Section 11.13	CB configuration for cell 12	
$18	CB13_CFG	Table 23	Section 11.13	CB configuration for cell 13	
$19	CB14_CFG	Table 23	Section 11.13	CB configuration for cell 14	
$1A	CB_OPEN_FLT	Table 23	Section 11.14	Open CB fault	
$1B	CB_SHORT_FLT	Table 23	Section 11.15	Short CB fault	
$1C	CB_DRV_STS	Table 23	Section 11.16	CB driver status	
$1D	GPIO_CFG1	Table 23	Section 11.17	GPIO configuration	
$1E	GPIO_CFG2	Table 23	Section 11.18	GPIO configuration	
$1F	GPIO_STS	Table 23	Section 11.19	GPIO diagnostic	
$20	AN_OT_UT_FLT	Table 23	Section 11.20	AN over and undertemperature	
$21	GPIO_SHORT_ ANx_OPEN_STS	Table 23	Section 11.21	Short GPIO/open AN diagnostic	
$23	COM_STATUS	Table 23	Section 11.22	Number of COM error counted	
$24	FAULT1_STATUS	Table 23	Section 11.23	Fault status	
$25	FAULT2_STATUS	Table 23	Section 11.24	Fault status	

Table 33. Register table*...continued*

Register		Response	Reference	Description	Notes
A[6:0]	Symbol				
$26	FAULT3_STATUS	Table 23	Section 11.25	Fault status	
$27	FAULT_MASK1	Table 23	Section 11.26	FAULT pin mask	
$28	FAULT_MASK2	Table 23	Section 11.27	FAULT pin mask	
$29	FAULT_MASK3	Table 23	Section 11.28	FAULT pin mask	
$2A	WAKEUP_MASK1	Table 23	Section 11.29	Wake-up events mask	
$2B	WAKEUP_MASK2	Table 23	Section 11.30	Wake-up events mask	
$2C	WAKEUP_MASK3	Table 23	Section 11.31	Wake-up events mask	
$32	MEAS_STACK	Table 23	Section 11.32	Stack voltage measurement	
$33	MEAS_CELL14	Table 23	Section 11.32	Cell 14 voltage measurement	
$34	MEAS_CELL13	Table 23	Section 11.32	Cell 13 voltage measurement	
$35	MEAS_CELL12	Table 23	Section 11.32	Cell 12 voltage measurement	
$36	MEAS_CELL11	Table 23	Section 11.32	Cell 11 voltage measurement	
$37	MEAS_CELL10	Table 23	Section 11.32	Cell 10 voltage measurement	
$38	MEAS_CELL9	Table 23	Section 11.32	Cell 9 voltage measurement	
$39	MEAS_CELL8	Table 23	Section 11.32	Cell 8 voltage measurement	
$3A	MEAS_CELL7	Table 23	Section 11.32	Cell 7 voltage measurement	
$3B	MEAS_CELL6	Table 23	Section 11.32	Cell 6 voltage measurement	
$3C	MEAS_CELL5	Table 23	Section 11.32	Cell 5 voltage measurement	
$3D	MEAS_CELL4	Table 23	Section 11.32	Cell 4 voltage measurement	
$3E	MEAS_CELL3	Table 23	Section 11.32	Cell 3 voltage measurement	
$3F	MEAS_CELL2	Table 23	Section 11.32	Cell 2 voltage measurement	
$40	MEAS_CELL1	Table 23	Section 11.32	Cell 1 voltage measurement	
$41	MEAS_AN6	Table 23	Section 11.32	AN6 voltage measurement	
$42	MEAS_AN5	Table 23	Section 11.32	AN5 voltage measurement	
$43	MEAS_AN4	Table 23	Section 11.32	AN4 voltage measurement	
$44	MEAS_AN3	Table 23	Section 11.32	AN3 voltage measurement	
$45	MEAS_AN2	Table 23	Section 11.32	AN2 voltage measurement	
$46	MEAS_AN1	Table 23	Section 11.32	AN1 voltage measurement	
$47	MEAS_AN0	Table 23	Section 11.32	AN0 voltage measurement	
$48	MEAS_IC_TEMP	Table 23	Section 11.32	IC temperature measurement	
$49	MEAS_ VBG_ DIAG_ADC1A	Table 23	Section 11.32	ADCIA voltage reference measurement	
$4A	MEAS_ VBG_ DIAG_ADC1B	Table 23	Section 11.32	ADCIB voltage reference measurement	
$4B	TH_ALL_CT	Table 23	Section 11.33	CTx over and undervoltage threshold	

Table 33. Register table...*continued*

Register		Response	Reference	Description	Notes
A[6:0]	Symbol				
$4C	TH_CT14	Table 23	Section 11.34	CT14 over and undervoltage threshold	
$4D	TH_CT13	Table 23	Section 11.34	CT13 over and undervoltage threshold	
$4E	TH_CT12	Table 23	Section 11.34	CT12 over and undervoltage threshold	
$4F	TH_CT11	Table 23	Section 11.34	CT11 over and undervoltage threshold	
$50	TH_CT10	Table 23	Section 11.34	CT10 over and undervoltage threshold	
$51	TH_CT9	Table 23	Section 11.34	CT9 over and undervoltage threshold	
$52	TH_CT8	Table 23	Section 11.34	CT8 over and undervoltage threshold	
$53	TH_CT7	Table 23	Section 11.34	CT7 over and undervoltage threshold	
$54	TH_CT6	Table 23	Section 11.34	CT6 over and undervoltage threshold	
$55	TH_CT5	Table 23	Section 11.34	CT5 over and undervoltage threshold	
$56	TH_CT4	Table 23	Section 11.34	CT4 over and undervoltage threshold	
$57	TH_CT3	Table 23	Section 11.34	CT3 over and undervoltage threshold	
$58	TH_CT2	Table 23	Section 11.34	CT2 over and undervoltage threshold	
$59	TH_CT1	Table 23	Section 11.34	CT1 over and undervoltage threshold	
$5A	TH_AN6_OT	Table 23	Section 11.35	AN6 overtemperature threshold	
$5B	TH_AN5_OT	Table 23	Section 11.35	AN5 overtemperature threshold	
$5C	TH_AN4_OT	Table 23	Section 11.35	AN4 overtemperature threshold	
$5D	TH_AN3_OT	Table 23	Section 11.35	AN3 overtemperature threshold	
$5E	TH_AN2_OT	Table 23	Section 11.35	AN2 overtemperature threshold	
$5F	TH_AN1_OT	Table 23	Section 11.35	AN1 overtemperature threshold	
$60	TH_AN0_OT	Table 23	Section 11.35	AN0 overtemperature threshold	
$61	TH_AN6_UT	Table 23	Section 11.35	AN6 undertemperature threshold	
$62	TH_AN5_UT	Table 23	Section 11.35	AN5 undertemperature threshold	
$63	TH_AN4_UT	Table 23	Section 11.35	AN4 undertemperature threshold	
$64	TH_AN3_UT	Table 23	Section 11.35	AN3 undertemperature threshold	
$65	TH_AN2_UT	Table 23	Section 11.35	AN2 undertemperature threshold	

Table 33. Register table...*continued*

Register		Response	Reference	Description	Notes
A[6:0]	Symbol				
$66	TH_AN1_UT	Table 23	Section 11.35	AN1 undertemperature threshold	
$67	TH_AN0_UT	Table 23	Section 11.35	AN0 undertemperature threshold	
$6B	SILICON_REV	Table 23	Section 11.36	Silicon revision	
$6C	EEPROM_CNTL	Table 23	Section 11.37	EEPROM transfer control	
$6D	DED_ENCODE1	Table 23	Section 11.38	ECC signature 1	
$6E	DED_ENCODE2	Table 23	Section 11.39	ECC signature 2	
$6F	FUSE_MIRROR_ DATA	Table 23	Section 11.40	Fuse mirror data	
$70	FUSE_MIRROR_ CNTL	Table 23	Section 11.40	Fuse mirror address	
$71	Reserved	Table 23	Section 11.41	NXP reserved	
...	Reserved	Table 23	Section 11.41	NXP reserved	
$7F	Reserved	Table 23	Section 11.41	NXP reserved	

Table 34. Mirror memory

Register		Description	Notes
A[4:0]			
$00	FUSE_MIRROR_BANK	Fuse bank 0	
$01	FUSE_MIRROR_BANK	Fuse bank 1	
$02	FUSE_MIRROR_BANK	Fuse bank 2	
$03	FUSE_MIRROR_BANK	Fuse bank 3	
$04	FUSE_MIRROR_BANK	Fuse bank 4	
$05	FUSE_MIRROR_BANK	Fuse bank 5	
$06	FUSE_MIRROR_BANK	Fuse bank 6	
$07	FUSE_MIRROR_BANK	Fuse bank 7	
$08	FUSE_MIRROR_BANK	Fuse bank 8	
$09	FUSE_MIRROR_BANK	Fuse bank 9	
$0A	FUSE_MIRROR_BANK	Fuse bank 10	
$0B	FUSE_MIRROR_BANK	Fuse bank 11	
$0C	FUSE_MIRROR_BANK	Fuse bank 12	
$0D	FUSE_MIRROR_BANK	Fuse bank 13	
$0E	FUSE_MIRROR_BANK	Fuse bank 14	
$0F	FUSE_MIRROR_BANK	Fuse bank 15	
$10	FUSE_MIRROR_BANK	Fuse bank 16	
$11	FUSE_MIRROR_BANK	Fuse bank 17	

Table 34. Mirror memory...*continued*

Register		Description	Notes
$12	FUSE_MIRROR_BANK	Fuse bank 18	
$13	FUSE_MIRROR_BANK	Fuse bank 19	
$14	FUSE_MIRROR_BANK	Fuse bank 20	
$15	FUSE_MIRROR_BANK	Fuse bank 21	
$16	FUSE_MIRROR_BANK	Fuse bank 22	DED_ENCODE 2
$17	FUSE_MIRROR_BANK	Fuse bank 23	DED_ENCODE 1
$18	FUSE_MIRROR_BANK	Fuse bank 24	
$19	FUSE_MIRROR_BANK	Fuse bank 25	
$1A	FUSE_MIRROR_BANK	Fuse bank 26	
$1B	FUSE_MIRROR_BANK	Fuse bank 27	
$1C	FUSE_MIRROR_BANK	Fuse bank 28	
$1D	FUSE_MIRROR_BANK	Fuse bank 29	
$1E	FUSE_MIRROR_BANK	Fuse bank 30	
$1F	FUSE_MIRROR_BANK	Fuse bank 31	

11.2 Initialization register – INIT

Following power-up or soft POR, the BMI7014 is in a reset state. In the INIT mode, the user may read the registers of the BMI7014 using the cluster id 00 0000b. The BMI7014 must be enumerated before it acts upon to write commands.

To initialize the device, a write command has to be sent with the value of 00 0000b in the cluster Identifier field of the frame, Section 10.4.2, with the new cluster ID, that is the new address to be assigned to the node, must be written to the CID field of the INIT register. Only a device with current cluster ID of 00 0000b may be programmed to a new address. By programming the device with a new CID the device is considered enumerated. After a device has been initialized, it only acts on subsequent global write (transformer mode) or local write and responds to read commands matching the device cluster ID. Once a device has been enumerated, the CID bits in the register INIT cannot be reprogrammed unless the device receives a hard or soft reset.

The bit field INIT[TPLx_TX_TERM] is used for preventing pins (RDTX_IN/OUT±) from floating when the BMI7014s are connected in single ended daisy chain (without loop-back). It is to be noted that this applies only to last node in the daisy chain. Depending on which pin (RDTX_IN± or RDTX_OUT±) of last node is floating, INIT[TPLx_TX_TERM] should be set to 1.The BMI7014 IC used in daisy chain communication with loop-back shall have the bit fields INIT[TPLx_TX_TERM] set to zero while for single ended daisy chain communication (without loop-back) the floating TPL port shall be set to 1.

Table 35. INIT

INIT																
$01	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write									TPL1_TX_TERM	TPL2_TX_TERM	CID					
Read	0	0	0	0	0	0	0	0								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 35. INIT...*continued*

TPL1_TX_TERM (RDTX_IN)	Description	Enable for TPL port termination for RDTX_IN pin
	0	Disabled
	1	Enabled
	Reset condition	POR
TPL_TX2_TERM (RDTX_OUT)	Description	Enable for TPL port termination for RDTX_OUT pin
	0	Disabled
	1	Enabled
	Reset condition	POR
CID	Description	Cluster Identifier, can be overridden by any combination different from all zeros. Not accessible with global write.
	0 0 0 0 0 0	Default
	x x x x x x	CID
	Reset condition	POR

11.3 System configuration global register SYS_CFG_GLOBAL

In TPL mode, only a global command can be used to write to register $02, while a local write is disregarded. In contrast, if using the SPI mode, only a local write to register $02 can be executed.

Table 36. SYS_CFG_GLOBAL

SYS_CFG_GLOBAL																
$02	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																GO2 SLEEP
Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GO2SLEEP	Description	Go to sleep command
	0	Disabled
	1 (active pulse)	Device goes to sleep mode after all conversions in progress are completed
	Reset condition	POR

11.4 System configuration register 1 – SYS_CFG1

The SYS_CFG1 register contains control bits and register settings that allow the user to adapt the BMI7014 to specific applications and system requirements. Of these control bits, it is important to note the SYS_CFG1[SOFT_RST] bit is used to reset register contents of the device.

Table 37. SYS_CFG1

SYS_CFG1																
$03	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	CYCLIC_TIMER			DIAG_TIMEOUT			Do not change	Do not change	CB_ DRVEN	GO2DIAG	CB_ MANUAL_ PAUSE	SOFT_ RST	FAULT_ WAVE	WAVE_ DC_BITx		x
Read										DIAG_ST		0				x
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1

CYCLIC_TIMER	Description	Timer to trigger cyclic measurements in normal mode or sleep mode
	0 0 0	Cyclic measure is disabled, whatever the mode
	0 0 1	Continuous measurements
	0 1 0	0.1 s
	0 1 1	0.2 s
	1 0 0	1.0 s
	1 0 1	2.0 s
	1 1 0	4.0 s
	1 1 1	8.0 s
	Reset condition	POR

Table 37. SYS_CFG1*...continued*

DIAG_TIMEOUT	Description	DIAG mode timeout. Length of time the device is allowed to be in diag mode before being forced to normal mode.
	0 0 0	No timer, not allowed to enter diag mode
	0 0 1	0.05 s
	0 1 0	0.1 s
	0 1 1	0.2 s
	1 0 0	1.0 s
	1 0 1	2.0 s
	1 1 0	4.0 s
	1 1 1	8.0 s
	Reset condition	POR
CB_DRVEN	Description	General enable or disable for all cell balance drivers.
	0	Disabled
	1	Enabled, each cell balance driver can be individually switched on and off by CB_xx_CFG register.
	Reset condition	POR
GO2DIAG	Description	Commands the device to diag mode. Rewriting the GO2DIAG bit restarts the DIAG_TIMEOUT.
	0	Exit diag mode
	1	Enter diag mode (starts timer)
	Reset condition	POR
CB_MANUAL_ PAUSE	Description	Cell balancing manual pause
	0	Disabled CB switches can be normally commanded on/off by the dedicated logic functions
	1	CB switches are forced off, CB counters are not frozen
	Reset condition	POR
DIAG_ST	Description	Identifies when the device is in diag mode
	0	System is not in diag mode
	1	System is in diag mode
	Reset condition	POR
SOFT_RST	Description	Software reset
	0	Disabled
	1 (active pulse)	Active software reset
	Reset condition	POR (bit is not reset if reset was due to software reset)
FAULT_WAVE	Description	FAULT pin wave form control bit.
	0	FAULT pin has high or low level behavior. FAULT pin high, fault is present. FAULT pin low indicates no fault present.
	1	FAULT pin has heartbeat wave when no fault is present. Pulse high time is fixed at 500 μs.
	Reset condition	POR
WAVE_DC_BITx	Description	Controls the off time of the heartbeat pulse.
	0 0	500 μs
	0 1	1.0 ms
	1 0	10 ms
	1 1	100 ms
	Reset condition	POR

11.5 System configuration register 2 – SYS_CFG2

Table 38. SYS_CFG2

SYS_CFG2																
$04	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	x	x	x				FLT_RST_CFG [1]				TIMEOUT_COMM		x	x	NUMB _ODD	HAMM _ENCOD
Read	x	x	x	PREVIOUS_STATE									x	x		
Reset	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0

Table 38. SYS_CFG2...continued

PREVIOUS_ STATE	Description	Information about the previous state of the device
	0 0 0	The device is coming from INIT state
	0 0 1	The device is coming from Idle state
	0 1 0	The device is coming from Normal state
	0 1 1	The device is coming from DIAG state
	1 1 1	The device is coming from Sleep state
	1 1 0	The device is coming from CYCLIC_WUP state
	Reset condition	POR
TIMEOUT_COMM	Description	No communication timeout - flag in FAULT1_STATUS[COM_LOSS] if no communication during…
	0 0	32 ms
	0 1	64 ms
	1 0	128 ms
	1 1	256 ms
	Reset condition	POR
FLT_RST_CFG	Description	Fault reset configuration[2]
	0 0 1 1	Disabled COM timeout (1024 ms) reset and OSC fault monitoring and reset
	0 1 0 1	Enabled OSC fault monitoring
	0 1 1 0	Enabled OSC fault monitoring and reset
	1 0 0 1	Enabled COM timeout (1024 ms) reset
	1 0 1 0	Enabled COM timeout (1024 ms) reset and OSC fault monitoring
	1 1 0 0	Enabled COM timeout (1024 ms) reset and OSC fault monitoring and reset
	others	Invalid, leads to enabled COM timeout (1024 ms) reset and OSC fault monitoring and reset (1100)
	Reset condition	POR (except after a reset caused by a communication timeout or caused by an oscillator fault)
NUMB_ODD	Description	Odd number of cells in the cluster (useful for open load diagnosis)
	0	Even configuration
	1	Odd configuration
	Reset condition	POR
HAMM_ENCOD	Description	Hamming encoders
	0	Decode - the DED Hamming decoders fulfill their job
	1	Encode - the DED hamming decoders generate the redundancy bits
	Reset condition	POR

[1] The Go2Reset option should not be disabled after a communication time out
[2] For more information, refer to Figure 8

11.6 System diagnostics register – SYS_DIAG

Table 39. SYS_DIAG

SYS_DIAG																
$05	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	FAULT_ DIAG			Do not change			ANx_ OL_ DIAG	ANx_ TEMP_ DIAG	DA_DIAG	POL ARITY	CT_ LEAK_ DIAG	CT_OV_ UV	CT_OL_ ODD	CT_OL_ EVEN	CB_OL_ ODD	CB_OL_ EVEN
Read		0	0													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FAULT_DIAG	Description	FAULT pin driver command
	0	No FAULT pin drive, FAULT pin is under command of the pack controller
	1	FAULT pin is forced to high level
	Reset condition	POR
ANx_OL_DIAG	Description	ANx open load diagnostic control bit. Used to activate the pull down on GPIO input pins.
	0	Diagnostic disabled
	1	Diagnostic enabled
	Reset condition	POR
ANx_TEMP_DIAG	Description	Control bit to activate the OT/UT diagnostic on GPIOx configured as ANx ratiometric or single ended ADC input
	0	Diagnostic inactive
	1	Diagnostic active
	Reset condition	POR
DA_DIAG	Description	Cell voltage channel functional verification. Diagnostic mode function only
	0	No check
	1	Check is enabled (floating Zener conversion, ground Zener measurement added, comparison)
	Reset condition	POR
POLARITY	Description	Control bit used in terminal leakage detection. Controls the polarity between the level shifter and the ADC1-A and ADC1-B converters
	0	Noninverted
	1	Inverted
	Reset condition	POR
CT_LEAK_DIAG	Description	Control bit used in terminal leakage detection. Commands the MUX to route the CTx/CBx pin to ADC1-A,B converters. This bit must be exclusive vs. DA_DIAG.
	0	Normal operation, CTx are MUXed to converter
	1	Δ between CT and CB pins are routed to the analog front end, to be converted
	Reset condition	POR
CT_OV_UV	Description	OV and UV diagnostic is enabled. This bit must be set to logic 0 when performing CT open load diagnostic.
	0	OV and UV diagnostic disabled
	1	OV and UV diagnostic enabled
	Reset condition	POR
CT_OL_ODD	Description	Control bit used to control the odd numbered cell terminal open detect switches
	0	Odd switches are open
	1	Odd switches are closed (may be set only when CT_OL_EVEN is logic 0)
	Reset condition	POR
CT_OL_EVEN	Description	Control bit used to control the even numbered cell terminal open detect switches
	0	Even switches are open
	1	Even switches are closed (may be set only when CT_OL_ODD is logic 0)
	Reset condition	POR
CB_OL_ODD	Description	Control bit used to control the cell balance open load ODD detection switches.
	0	ODD cell balance open load detection switches are open
	1	ODD cell balance open load detection switches are closed
	Reset Condition	POR
CB_OL_EVEN	Description	Control bit used to control the cell balance open load EVEN detection switches
	0	EVEN cell balance open load detection switches are open
	1	EVEN cell balance open load detection switches are closed
	Reset condition	POR

11.7 ADC configuration register – ADC_CFG

The ADC_CFG is used to set the conversion parameters of the three ADC converters and command the BMI7014 to perform on-demand conversions in both normal and diagnostic modes.

Table 40. ADC_CFG

ADC_CFG																
$06	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	AVG				SOC	x					ADC1_A_DEF		ADC1_B_DEF		x	
Read					EOC_N											
Reset	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	1

AVG	Description	With each conversion request, the number of samples to be averaged can be configured
	0 0 0 0	No averaging, the result is taken as is (compatibility mode)
	0 0 0 1	Averaging of 2 consecutive samples
	0 0 1 0	Averaging of 4 consecutive samples
	0 0 1 1	Averaging of 8 consecutive samples
	0 1 0 0	Averaging of 16 consecutive samples
	0 1 0 1	Averaging of 32 consecutive samples
	0 1 1 0	Averaging of 64 consecutive samples
	0 1 1 1	Averaging of 128 consecutive samples
	1 0 0 0	Averaging of 256 consecutive samples
	All other Configurations	No averaging, the result is taken as is (compatibility mode)
	Reset condition	POR
SOC	Description	Control bit to command the BMI7014 to initiate a conversion sequence
	0	Disabled. Writing SOC to 0 has no effect on an ongoing conversion sequence.
	1 (active pulse)	Enabled. Initiate a conversion sequence.
	Reset condition	POR
EOC_N	Description	End of conversion flag
	0	Device has completed the commanded conversion
	1	Device is performing the commanded conversion
	Reset condition	POR
ADC1_A_DEF	Description	ADC1_A measurement resolution
	0 0	13 bit
	0 1	14 bit
	1 0	15 bit
	1 1	16 bit
	Reset condition	POR
ADC1_B_DEF	Description	ADC1_B measurement resolution
	0 0	13 bit
	0 1	14 bit
	1 0	15 bit
	1 1	16 bit
	Reset condition	POR

11.8 CB_SHORT_CFG

Table 41. CB_SHORT_CFG

CB_SHORT_CFG																
$07	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	x	x	x	x	x	x	x	ALLCBOFF_ON_SHORT	x	x	x	x	x	x	x	x
Read	x	x	x	x	x	x	x		x	x	x	x	x	x	x	x
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ALLCBOFF_ON_SHORT	Description	All CB's turn off in case of at least one short
	0	Only shorted CB's are turned off
	1	If at least one CB is shorted, all CB's are then turned off (CB_DRVEN is reset)
	Reset condition	POR

11.9 Cell select register – OV_UV_EN

The user has the option to select a common overvoltage and undervoltage threshold, or individual thresholds for each cell. To use a common threshold for all cell terminal inputs, the user must program register TH_ALL_CT and enable the common threshold bit. An individual threshold may be programmed for each cell terminal through register TH_CTx. Either threshold selection requires the CTx_OVUV_EN bit be set for the BMI7014 to monitor the cell terminal input for over and undervoltage.

Table 42. OV_UV_EN

OV_UV_EN																
$08	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write / Read	COMMON_OV_TH	COMMON_UV_TH	CT14_OVUV_EN	CT13_OVUV_EN	CT12_OVUV_EN	CT11_OVUV_EN	CT10_OVUV_EN	CT9_OVUV_EN	CT8_OVUV_EN	CT7_OVUV_EN	CT6_OVUV_EN	CT5_OVUV_EN	CT4_OVUV_EN	CT3_OVUV_EN	CT2_OVUV_EN	CT1_OVUV_EN
Reset	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

COMMON_OV_TH	Description	All CTx measurement use the common overvoltage threshold register for comparison
	0	Use individual threshold register
	1	Use common threshold register
	Reset condition	POR
COMMON_UV_TH	Description	All CTx measurement use the common undervoltage threshold register for comparison
	0	Use individual threshold register
	1	Use common threshold register
	Reset condition	POR
CTx_OVUV_EN	Description	Enable or disable ADC data to be compared with thresholds for OV/UV. If disabled no OVUV fault is set.
	0	OVUV disabled
	1	OVUV is enabled
	Reset condition	POR

11.10 Cell terminal overvoltage fault register – CELL_OV_FLT

The CELL_OV_FLT register contains the overvoltage fault status of each cell. The CELL_OV_FLT register is updated with each cyclic conversion and each on-demand conversion from the system controller. In normal mode, the CTx_OV_FLT bit may be cleared by writing logic 0 when overvoltage is no longer present at the cell terminal inputs.

Table 43. CELL_OV_FLT

CELL_OV_FLT																
$09	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	0	CT14_ OV_FLT	CT13_ OV_FLT	CT12_ OV_FLT	CT11_ OV_FLT	CT10_ OV_FLT	CT9_ OV_FLT	CT8_ OV_FLT	CT7_ OV_FLT	CT6_ OV_FLT	CT5_ OV_FLT	CT4_ OV_FLT	CT3_ OV_FLT	CT2_ OV_FLT	CT1_ OV_FLT
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CTx_OV_FLT	Description	CTx_OV_FLT register contains the status of the overvoltage fault for each cell terminal. Register is updated with each internal and system controller on-demand conversion cycle.
	0	No Cell Terminal overvoltage
	1	Cell Terminal overvoltage detected on terminal x
	Reset condition	POR/clear on write 0

[1] w0c: write 0 to clear

11.11 Cell terminal undervoltage fault register – CELL_UV_FLT

The CELL_UV_FLT register contains the undervoltage fault status of each cell. The CELL_UV_FLT register is updated with each cyclic conversion and each on-demand conversion from the system controller. In normal mode, the CTx_UV_FLT bit may be cleared by writing logic 0 when undervoltage is no longer present at the cell terminal inputs.

Table 44. CELL_UV_FLT

CELL_UV_FLT																
$0A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	0	CT14_ UV_FLT	CT13_ UV_FLT	CT12_ UV_FLT	CT11_ UV_FLT	CT10_ UV_FLT	CT9_ UV_FLT	CT8_ UV_FLT	CT7_ UV_FLT	CT6_UV _FLT	CT5_ UV_FLT	CT4_ UV_FLT	CT3_ UV_FLT	CT2_ UV_FLT	CT1_ UV_FLT
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CTx_UV_FLT	Description	CTx_UV_FLT register contains the status of the overvoltage fault for each cell terminal. Register is updated with each internal and system controller requested conversion cycle.
	0	No cell terminal undervoltage
	1	Cell terminal undervoltage detected on terminal x
	Reset condition	POR/clear on write 0

[1] w0c: write 0 to clear

11.12 TPL_CFG

TPL_CFG register configures up and down transmitter. It allows the pack controller to configure transmitter drive strength based on capacitive or transformer isolation and selection of differential load termination.

Table 45. TPL_CFG

TPL_CFG																
$0B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	Do not change															
Read																
Reset	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0

Note: *The default value TPL_CFG register is set considering a transmission line of 120 Ω .*

11.13 Cell balance configuration register – CBx_CFG

The cell balance configuration register holds the operating parameters of the cell balance output drivers.

Table 46. CBX_CFG

CBx_CFG																
$0C to $19	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							CBx_EN	CBx_TIMER								
Read	0	0	0	0	0	0	CBx_STS									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CBx_EN	Description	Cell balance enable
	0	Cell balance driver disabled
	1	Cell balance is enabled or re-launched if overwritten (restarts the timer count from zero and enables the driver)
	Reset condition	POR
CBx_STS	Description	Cell balance driver status
	0	Cell balance driver is off
	1	Cell balance driver is on
	Reset condition	POR
CBx_TIMER	Description	Cell balance timer in minutes
	000000000	0.5 minutes
	000000001	1 minute
	000000010	2 minutes
	...	
	111111111	511 minutes
	Reset condition	POR

11.14 Cell balance open load fault detection register – CB_OPEN_FLT

Table 47. CB_OPEN_FLT

CB_OPEN_FLT																
$1A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	0	CB14_OPEN_FLT	CB13_OPEN_FLT	CB12_OPEN_FLT	CB11_OPEN_FLT	CB10_OPEN_FLT	CB9_OPEN_FLT	CB8_OPEN_FLT	CB7_OPEN_FLT	CB6_OPEN_FLT	CB5_OPEN_FLT	CB4_OPEN_FLT	CB3_OPEN_FLT	CB2_OPEN_FLT	CB1_OPEN_FLT
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CBx_OPEN_FLT	Description	Cell balancing open load detection – (info) Logic OR of CBx_OPEN_FLT is provided in the FAULT2_STATUS[CB_OPEN_FLT]
	0	No open load cell balance fault detected
	1	Off state open load detected
	Reset condition	POR/Clear on write 0

[1] w0c: write 0 to clear

11.15 Cell balance shorted load fault detection register – CB_SHORT_FLT

The cell balance short detection register holds the cell balance shorted load status.

Table 48. CB_SHORT_FLT

CB_SHORT_FLT																
$1B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	0	CB14_ SHORT_ FLT	CB13_ SHORT_ FLT	CB12_ SHORT_ FLT	CB11_ SHORT_ FLT	CB10_ SHORT_ FLT	CB9_ SHORT_ FLT	CB8_ SHORT_ FLT	CB7_ SHORT_ FLT	CB6_ SHORT_ FLT	CB5_ SHORT_ FLT	CB4_ SHORT_ FLT	CB3_ SHORT_ FLT	CB2_ SHORT_ FLT	CB1_ SHORT_ FLT
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CBx_SHORT_FLT	Description	Cell balancing shorted load fault detection – (info) CBx_SHORT_FLT Ored is provided in the FAULT2[CB_SHORT_FLT]
	0	No shorted load fault detected
	1	Shorted load fault detected
	Reset condition	POR/clear on write 0

[1] w0c: write 0 to clear

11.16 Cell balance driver on/off status register – CB_DRV_STS

Table 49. CB_DRV_STS

CB_DRV_STS																
$1C	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	0	0	CB14_ STS	CB13_ STS	CB12_ STS	CB11_ STS	CB10_ STS	CB9_STS	CB8_STS	CB7_STS	CB6_STS	CB5_STS	CB4_STS	CB3_STS	CB2_STS	CB1_STS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CBx_STS	Description	Contains the state of the cell balance driver
	0	Driver CBx is off
	1	Driver CBx is on
	Reset condition	POR

11.17 GPIO configuration register 1 – GPIO_CFG1

The GPIO_CFG1 register programs the individual GPIO port as a ratiometric, single ended, input or output port.

Table 50. GPIO_CFG1

GPIO_CFG1																
$1D	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			GPIO6_CFG		GPIO5_CFG		GPIO4_CFG		GPIO3_CFG		GPIO2_CFG		GPIO1_CFG		GPIO0_CFG	
Read	0	0														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_CFG	Description	Register controls the configuration of the GPIO port
	0 0	GPIOx configured as analog input for ratiometric measurement
	0 1	GPIOx configured as analog input for absolute measurement
	1 0	GPIOx configured as digital input
	1 1	GPIOx configured as digital output
	Reset condition	POR

11.18 GPIO configuration register 2 – GPIO_CFG2

Table 51. GPIO_CFG2

GPIO_CFG2																
$1E	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							GPIO2_ SOC	GPIO0_ WU	GPIO0_ FLT_ ACT	GPIO6_ DR	GPIO5_ DR	GPIO4_ DR	GPIO3_ DR	GPIO2_ DR	GPIO1_ DR	GPIO0_ DR
Read	0	0	0	0	0	0										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 51. GPIO_CFG2 *...continued*

GPIO2_SOC	Description	GPIO2 used as ADC1_A/ADC1_B start-of-conversion. Requires GPIO2_CFG = 10.
	0	GPIO2 port ADC trigger is disabled
	1	GPIO2 port ADC trigger is enabled. A rising edge on GPIO2 triggers an ADC1-A and ADC1-B conversion – only when in normal mode
	Reset condition	POR
GPIO0_WU	Description	GPIO0 wake-up capability. Valid only when GPIO0_CFG = 10.
	0	No wake-up capability
	1	Wake-up on any edge, transitioning the system from sleep to normal
	Reset condition	POR
GPIO0_FLT_ACT	Description	GPIO0 activate fault output pin. Valid only when GPIO0_CFG = 10.
	0	Does not activate FAULT pin when GPIO0 is configured as an input and is logic 1
	1	Activates the FAULT pin when GPIO is configured as an input and is logic 1
	Reset condition	POR
GPIOx_DR	Description	GPIOx pin drive. Ignored except when GPIOx_CFG = 11
	0	Drive GPIOx to low level
	1	Drive GPIOx to high level
	Reset condition	POR

11.19 GPIO status register – GPIO_STS

Table 52. GPIO_STS

GPIO_STS																
$1F	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write		w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]								
Read	0	GPIO6_H	GPIO5_H	GPIO4_H	GPIO3_H	GPIO2_H	GPIO1_H	GPIO0_H	0	GPIO6_ST	GPIO5_ST	GPIO4_ST	GPIO3_ST	GPIO2_ST	GPIO1_ST	GPIO0_ST
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_H	Description	The GPIOx_H bits detects and latches the low to high transition occurring on the GPIOx input
	0	No high state detected
	1	A high state has been detected
	Reset condition	POR/clear on write 0
GPIOx_ST	Description	Real time GPIOx status
	0	Report GPIOx at low level
	1	Report GPIOx at high level
	Reset condition	POR

[1] w0c: write 0 to clear

11.20 Overtemperature/undertemperature fault register – AN_OT_UT_FLT

Table 53. AN_OT_UT_FLT

AN_OT_UT_FLT																
$20	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write		w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]		w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	AN6_OT	AN5_OT	AN4_OT	AN3_OT	AN2_OT	AN1_OT	AN0_OT	0	AN6_UT	AN5_UT	AN4_UT	AN3_UT	AN2_UT	AN1_UT	AN0_UT
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Anx_OT	Description	Overtemperature detection for AN n°x – Anx_OT ored is provided in FAULT1_STATUS[AN_OT_FLT]
	0	No overtemperature fault detected
	1	Overtemperature fault detected on Anx
	Reset condition	POR/clear on write 0 (Anx_OT is set again on next cyclic conversion or on-demand conversion if overtemperature persists)
Anx_UT	Description	Undertemperature detection for AN n°x – Anx_UT ored is provided in FAULT1_STATUS[AN_UT_FLT]
	0	No undertemperature fault detected
	1	Undertemperature fault detected on Anx
	Reset condition	POR/clear on write 0 (Anx_UT is set again on next cyclic conversion or on-demand conversion if undertemperature persists)

[1] w0c: write 0 to clear

11.21 GPIO open short register – GPIO_SHORT_ANx_OPEN_STS

Table 54. GPIO_SHORT_ANx_OPEN_STS

GPIO_SHORT_ANx_OPEN_STS																
$21	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write		w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]		w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	GPIO6_ SH	GPIO5_ SH	GPIO4_ SH	GPIO3_ SH	GPIO2_ SH	GPIO1_ SH	GPIO0_ SH	0	AN6_ OPEN	AN5_ OPEN	AN4_ OPEN	AN3_ OPEN	AN2_ OPEN	AN1_ OPEN	AN0_ OPEN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIOx_SH		Description		GPIOx short detection GPIOx_SH ored is provided in FAULT2_STATUS[GPIO_SHORT_FLT]												
		0		No short detected												
		1		Short detected, pad sense is different from pad command												
		Reset condition		POR/clear on write 0												
ANx_OPEN		Description		Analog inputs open load detection. ANx_OPEN ored is provided in FAULT2_STATUS[AN_OPEN_FLT]												
		0		No open load detected												
		1		Open load detected on Anx												
		Reset condition		POR/Clear On Write 0 (ANx_OPEN is set again with open load detect switch closed and open load persists)												

[1] w0c: write 0 to clear

11.22 Communication status register – COM_STATUS

Table 55. COM_STATUS

COM_STATUS																
$23	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	w0c[1]															
Read	COM_ERR _COUNT								0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
COM_ERR_ COUNT		Description		Number of communication errors detected												
		0 0 0 0 0 0 0 0		0 communication errors have been detected												
		...														
		1 1 1 1 1 1 1 1		255 communication errors have been detected. Overflow of counter sets FAULT1_STATUS[COMM_ERR_OVR_FLT]. Count remains at 255 until cleared by controller.												
		Reset condition		POR/clear on write 0												

[1] w0c: write 0 to clear

11.23 Fault status register 1 – FAULT1_STATUS

Table 56. FAULT1_STATUS

FAULT1_STATUS																
$24	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	x	x				
Read	POR	RESET_ FLT	COM_ ERR_ OVR_ FLT	VPWR_ OV_FLT	VPWR_ LV_FLT	COM_ LOSS_ FLT	COM_ ERR_ FLT	CSB_ WUP_ FLT	GPIO0_ WUP_ FLT	I2C_ ERR_ FLT	x	x	AN_OT_ FLT	AN_UT_ FLT	CT_OV_ FLT	CT_UV_ FLT
Reset	1	0**	0*	0*	0*	0**	0*	0	0	0	0	0	0	0	0	0

Notes:

1. *Depending on the voltage conditions occurring on some pins at the IC initialization, the initial value of bits marked by an * may be flipped.*
2. *Values marked ** may be flipped at reset, depending on its cause (see bit descriptions).*

Table 56. FAULT1_STATUS*...continued*

POR	Description	Power-on reset indication (POR)
	0	No POR
	1	Device has PORed
	Reset condition	POR/clear on write 0
RESET_FLT	Description	RESET Indication (nonmaskable)
	0	No reset
	1	Device has been reset through the RESET pin or by a write command setting the SYS_CFG1[SOFT_RST] or by a communication loss or an oscillator monitoring fault
	Reset condition	POR/clear on write 0
COM_ERR_OVR_FLT	Description	Overflow indicator on the COM_STATUS[COM_ERR_COUNT]
	0	No error
	1	COM_STATUS[COM_ERR_COUNT] went in overflow
	Reset condition	POR/clear on write 0
VPWR_OV_FLT	Description	VPWR overvoltage notification
	0	No overvoltage (VPWR < VPWR(OV_FLAG)) detected
	1	Overvoltage detected (VPWR > VPWR(OV_FLAG), timing filtered)
	Reset condition	POR/clear on write 0
VPWR_LV_FLT	Description	VPWR low-voltage notification
	0	No low-voltage (VPWR > VPWR(LV_FLAG)) detected
	1	Low-voltage detected (VPWR < VPWR(LV_FLAG), timing filtered)
	Reset condition	POR/clear on write 0
COM_LOSS_FLT	Description	In normal mode, each slave device must receive a local message within the programmed period or COM_LOSS_FLT flag is set
	0	No error
	1	Communication loss detected after a reset due to a communication loss
	Reset condition	POR/clear on write 0 (bit is not cleared if reset was caused by a communication loss)
COM_ERR_FLT	Description	Communication error detected
	0	No error
	1	An error has been detected during a communication
	Reset condition	POR/clear on write 0
CSB_WUP_FLT	Description	CSB wake-up notification
	0	No wake-up
	1	CSB wake-up detected
	Reset condition	POR/clear on write 0
GPIO0_WUP_FLT	Description	GPIO0_ wake-up notification
	0	No wake-up
	1	GPIO0 wake-up detected
	Reset condition	POR/clear on write 0
I2C_ERR_FLT	Description	I^2C communication error during the transfer from EEPROM to the IC
	0	No Error
	1	Error detected
	Reset condition	POR/clear on write 0
AN_OT_FLT	Description	Analog input overtemperature detection
	0	No overtemperature detected
	1	Overtemperature detected in one or more of the Anx analog inputs
	Reset condition	POR/Clear On Write 0 all AN_OT_UT[Anx_OT] bits
AN_UT_FLT	Description	Analog inputs undertemperature detection
	0	No undertemperature detected
	1	Undertemperature detected in at least one of the seven analog inputs
	Reset condition	POR/Clear On Write 0 all AN_OT_UT[ANx_UT] bits
CT_OV_FLT	Description	Cell terminal overvoltage detection
	0	No overvoltage detected
	1	Overvoltage detected in one or more of the 14 cell terminals
	Reset condition	POR/clear on write 0 all CELL_OV[CTx_OV] bits

Table 56. FAULT1_STATUS...*continued*

CT_UV_FLT	Description	Cell terminal undervoltage detection
	0	No undervoltage detected
	1	Undervoltage detection in at least one of the 14 cell terminals
	Reset condition	POR/clear on write 0 all CELL_UV[CTx_UV] bits

[1] w0c: write 0 to clear

11.24 Fault status register 2 – FAULT2_STATUS

Table 57. FAULT2_STATUS

FAULT2_STATUS																
$25	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]					w0c[1]	w0c[1]	w0c[1]
Read	VCOM_ OV_FLT	VCOM_ UV_FLT	VANA_ OV_FLT	VANA_ UV_FLT	ADC1_ B_FLT	ADC1_ A_FLT	GND_ LOSS_ FLT	IC_ TSD_ FLT	IDLE_ MODE_ FLT	AN_ OPEN_ FLT	GPIO_ SHORT_ FLT	CB_ SHORT_ FLT	CB_ OPEN_ FLT	OSC_ ERR_ FLT	DED_ ERR_ FLT	FUSE_ ERR_ FLT
Reset	0*	0*	0*	0*	0	0	0*	0	0	0	0	0	0	0*	0*	0**

Notes:

1. *Depending on the voltage conditions occurring on some pins at the IC initialization, the initial value of bits marked by an * may be flipped.*
2. *Values marked ** may be flipped at reset, depending on its cause (see bit descriptions).*

VCOM_OV_FLT	Description	VCOM overvoltage notification
	0	No overvoltage detected
	1	Overvoltage has been detected on VCOM supply
	Reset condition	POR/clear on write 0
VCOM_UV_FLT	Description	VCOM undervoltage notification
	0	No undervoltage detected
	1	Undervoltage has been detected on VCOM supply
	Reset condition	POR/clear on write 0
VANA_OV_FLT	Description	VANA overvoltage notification
	0	No overvoltage detected
	1	Overvoltage has been detected on the VANA supply
	Reset condition	POR/clear on write 0
VANA_UV_FLT	Description	VANA undervoltage notification
	0	No undervoltage detected
	1	Undervoltage has been detected on the VANA supply
	Reset condition	POR/clear on write 0
ADC1_B_FLT	Description	ADC1_B fault notification
	0	No fault detected
	1	ADC1_B fault (over or undervoltage has been detected on MEAS_VBG_DIAG_ADC1B)
	Reset condition	POR/clear on write 0
ADC1_A_FLT	Description	ADC1_A fault notification
	0	No fault detected
	1	ADC1_A fault (over or undervoltage has been detected on MEAS_VBG_DIAG_ADC1A)
	Reset condition	POR/clear on write 0
GND_LOSS_FLT	Description	Loss of ground has been detected on DGND or AGND
	0	No error
	1	Loss of ground detected
	Reset condition	POR/clear on write 0
IC_TSD_FLT	Description	IC thermal limitation notification
	0	No thermal limitation detected
	1	Thermal limitation detected
	Reset condition	POR/clear on write 0

Table 57. FAULT2_STATUS*...continued*

IDLE_MODE_FLT	Description	IDLE mode notification
	0	No notification
	1	The system has transitioned through idle mode
	Reset condition	POR/clear on write 0
AN_OPEN_FLT	Description	Analog inputs open load detection
	0	No open load detected
	1	Open load detected in one of the seven analog inputs
	Reset condition	POR/clear on write 0 all GPIO_SHORT_ANx_OPEN_STS[ANx_OPEN] bits
GPIO_SHORT_FLT	Description	GPIO short detection
	0	No short detected
	1	Short detected in one or more of the seven GPIOs, pad sense is different from pad command
	Reset condition	POR/clear on write 0 all GPIO_SHORT_ANx_OPEN_STS (GPIOx_SH) bits
CB_SHORT_FLT	Description	Cell balance short-circuit detection
	0	No short-circuit detected
	1	On state short-circuit detected in one or more of the 14 cell balancing switches
	Reset condition	POR/clear on write 0 all CB_SHORT_FLT[CBx_SHORT] bits
CB_OPEN_FLT	Description	Cell balancing open load detection
	0	No cell balance open load detected
	1	Off state open load detected in one or more of the 14 cell balancing switches
	Reset condition	POR/clear on write 0 all CB_OPEN_FLT[CBx_OPEN] bits
OSC_ERR_FLT	Description	Low-power oscillator error
	0	No error
	1	The low-power oscillator frequency is out of range after a reset due to an oscillator monitoring fault
	Reset condition	POR/clear on write 0 (bit is not cleared if reset was caused by an oscillator monitoring fault)
DED_ERR_FLT	Description	ECC error, double error detection
	0	No error
	1	A double error has been detected (and only one corrected) in the fuses
	Reset condition	POR/clear on write 0
FUSE_ERR_FLT	Description	Error in the loading of fuses
	0	No error
	1	The lock bit was not set after loading, meaning transfer of the fuse values is aborted
	Reset condition	POR/clear on write 0

[1] w0c: write 0 to clear

11.25 Fault status register 3 – FAULT3_STATUS

Table 58. FAULT3_STATUS

FAULT3_STATUS																
$26	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	x	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	x	DIAG_ TO_FLT	EOT_ CB14	EOT_ CB13	EOT_ CB12	EOT_ CB11	EOT_ CB10	EOT_ CB9	EOT_ CB8	EOT_ CB7	EOT_ CB6	EOT_ CB5	EOT_ CB4	EOT_ CB3	EOT_ CB2	EOT_ CB1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DIAG_TO_FLT	Description	Timeout of Diagnostic state
	0	No timeout
	1	The system has exited itself from Diagnostic state after timeout
	Reset condition	POR/clear on write 0
EOT_CBx	Description	End of time cell balancing notification – indicates when a cell balance timer has expired and driver has been shutoff
	0	Cell balance timer has not timed out
	1	Cell balance timer has timed out
	Reset condition	POR/clear on write 0

[1] w0c: write 0 to clear

11.26 Fault mask register 1 – FAULT_MASK1

The FAULT_MASK1 register allows the user to selectively mask fault bits associated to the FAULT1_STATUS register. Masking a certain fault bit has the effect of preventing this bit from activating the FAULT output pin.

Table 59. FAULT_MASK1

FAULT_MASK1																
$27	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write				MASK_12_F	MASK_11_F	MASK_10_F	MASK_9_F	MASK_8_F	MASK_7_F	MASK_6_F	x	x	MASK_3_F	MASK_2_F	MASK_1_F	MASK_0_F
Read	0	0	0													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MASK_x_F	Description	Prevent the corresponding flags in FAULT1_STATUS to activate the FAULT pin
	0	The flag in position (x) activates the FAULT pin
	1	No activation
	Reset condition	POR

11.27 Fault mask register 2 – FAULT_MASK2

The FAULT_MASK2 register allows the user to selectively mask fault bits associated to the FAULT2_STATUS register. Masking a certain fault bit has the effect of preventing this bit from activating the FAULT output pin.

Table 60. FAULT_MASK2

FAULT_MASK2																
$28	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	MASK_15_F	MASK_14_F	MASK_13_F	MASK_12_F	MASK_11_F	MASK_10_F	MASK_9_F			MASK_6_F	MASK_5_F	MASK_4_F	MASK_3_F	MASK_2_F	MASK_1_F	MASK_0_F
Read								0	0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MASK_x_F	Description	Prevent the corresponding flags in FAULT2_STATUS to activate the FAULT pin
	0	The flag in position (x) activates the FAULT pin
	1	No activation
	Reset condition	POR

11.28 Fault mask register 3 – FAULT_MASK3

The FAULT_MASK3 register allows the user to selectively mask fault bits associated to the FAULT3_STATUS register. Masking a certain fault bit has the effect of preventing this bit from activating the FAULT output pin.

Table 61. FAULT_MASK3

FAULT_MASK3																
$29	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	x	MASK_14_F	MASK_13_F	MASK_12_F	MASK_11_F	MASK_10_F	MASK_9_F	MASK_8_F	MASK_7_F	MASK_6_F	MASK_5_F	MASK_4_F	MASK_3_F	MASK_2_F	MASK_1_F	MASK_0_F
Read																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MASK_x_F	Description	Prevent the corresponding flags in FAULT3_STATUS to activate the FAULT pin
	0	The flag in position (x) activates the FAULT pin
	1	No activation
	Reset condition	POR

11.29 Wake-up mask register 1 – WAKEUP_MASK1

The WAKEUP_MASK1 register enables wake-up events related to several FAULT1_STATUS fault bits. If a certain bit contained in the latter register is not masked by the corresponding bit of the former register, the IC transitions from sleep mode to normal mode.

Table 62. WAKEUP_MASK1

WAKEUP_MASK1																
$2A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write				MASK_ 12_F	MASK_ 11_F				MASK_ 7_F			Do not change	MASK_ 3_F	MASK_ 2_F	MASK_ 1_F	MASK_ 0_F
Read	0	0	0			0	0	0		0	0					
Reset	0	0	0	1	1	0	0	0	1	0	0	1	1	1	1	1
MASK_x_F		Description		Prevent the corresponding flags in FAULT1_STATUS to wake-up the device												
		0		The flag in position (x) wakes the device up, when active												
		1		No wake-up is possible by this source												
		Reset condition		POR												

11.30 Wake-up mask register 2 – WAKEUP_MASK2

The WAKEUP_MASK2 register enables wake-up events related to several FAULT2_STATUS fault bits. If a certain bit contained in the latter register is not masked by the corresponding bit of the former register, the IC transitions from sleep mode to normal mode.

Table 63. WAKEUP_MASK2

WAKEUP_MASK2																
$2B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	MASK_ 15_F	MASK_ 14_F	MASK_ 13_F	MASK_ 12_F	MASK_ 11_F	MASK_ 10_F	MASK_ 9_F	MASK_ 8_F			MASK_ 5_F	MASK_ 4_F		Mask_ 2_F	MASK_ 1_F	
Read									0	0			0			0
Reset	1	1	1	1	1	1	1	1	0	0	1	1	0	1	1	0
MASK_x_F		Description		Prevent the corresponding flags in FAULT2_STATUS to wake-up the device												
		0		The flag in position (x) wakes the device, when active												
		1		No wake-up is possible by this source												
		Reset condition		POR												

11.31 Wake-up mask register 3 – WAKEUP_MASK3

The WAKEUP_MASK3 register enables wake-up events related to several FAULT3_STATUS fault bits. If a certain bit contained in the latter register is not masked by the corresponding bit of the former register, the IC transitions from sleep mode to normal mode.

Table 64. WAKEUP_MASK3

WAKEUP_MASK3																
$2C	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	do not change		MASK_ 13_F	MASK_ 12_F	MASK_ 11_FK	MASK_ 10_F	MASK_ 9_F	MASK_ 8_F	MASK_ 7_F	MASK_ 6_F	MASK_ 5_F	MASK_ 4_F	MASK_ 3_F	MASK_ 2_F	MASK_ 1_F	MASK_ 0_F
Read		0														
Reset	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
MASK_x_F		Description		Prevent the corresponding flags in FAULT3_STATUS to wake-up the device												
		0		The flag in position (x) wakes the device, when active												
		1		No wake-up is possible by this source												
		Reset condition		POR												

11.32 Measurement registers – MEAS_xxxx

The MEAS_xxxx registers contain the measured values as a result of on-demand conversions. Note that the cyclic conversions leave no trace in these registers, as they are only used to update the OV/UV/OT/UT flags and other status information.

Table 65. MEAS_xxxx

MEAS_xxxx																
$32 to $4A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	DATA_ RDY	MEAS_xxxx														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DATA_RDY	Description	This bit is set when the conversion is complete and the register is updated. The Data_Rdy bit is cleared when a request to convert is received either through the SOC or GPIO2 convert trigger.
	0	A new sequence of conversions is currently running
	1	A data is available in MEAS_xxxx
	Reset condition	POR
MEAS_xxxx	Description	Value is unsigned, resolution is $V_{CT\_ANx\_RES}$ independently on the selected resolution of ADC_CFG
	Reset condition	POR

11.33 Overvoltage undervoltage threshold register – TH_ALL_CT

Resolution for OV threshold and UV threshold are, respectively, $V_{CTOV(TH)}$ and $V_{CTUV(TH)}$.

Table 66. TH_ALL_CT

TH_ALL_CT																
$4B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write Read	ALL_CT_OV_TH								ALL_CT_UV_TH							
Reset	1	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0

ALL_CT_OV_TH	Description	Overvoltage threshold setting for all cell terminals. Enabled through register OV_UV_EN
	11010111	Default overvoltage threshold set to 4.2 V
	Reset condition	POR
ALL_CT_UV_TH	Description	Undervoltage threshold setting for all cell terminals. Enabled through register OV_UV_EN
	10000000	Default undervoltage threshold set to 2.5 V
	Reset condition	POR

11.34 Overvoltage undervoltage threshold register – TH_CTx

Table 67. TH_CTX

TH_CTx																
$4C to $59	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write Read	CTx_OV_TH								CTx_UV_TH							
Reset	1	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0

CTx_OV_TH	Description	Overvoltage threshold setting for individual cell terminals. OV_UV_EN[COMMON_OV_TH] bit must be logic 0 and OV_UV_EN[CTx_OVUV_EN] bit must be logic 1 to use TH_CTx register as threshold.
	11010111	Default overvoltage threshold set to 4.2 V
	Reset condition	POR
CTx_UV_TH	Description	Undervoltage threshold setting for individual cell terminals. OV_UV_EN[COMMON_UV_TH] bit must be logic 0 and OV_UV_EN[CTx_OVUV_EN] bit must be logic 1 to use TH_CTx register as threshold.
	10000000	Default undervoltage threshold set to 2.5 V
	Reset condition	POR

11.35 Overtemperature, undertemperature threshold registers – TH_Anx_OT, TH_Anx_UT

Registers TH_Anx_OT and TH_Anx_UT contain the individually programmed overtemperature and undertemperature value for each analog input.

Table 68. TH_ANX_OT

TH_Anx_OT																
$5A to $60	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							ANx_OT_TH									
Read	0	0	0	0	0	0										
Reset	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	1
Anx_OT_TH		Description		Overtemperature threshold setting for analog input x												
		0011101101		Overtemperature default set to 1.16 V												
		Reset condition		POR												

Table 69. TH_ANX_UT

TH_Anx_UT																
$61 to $67	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							ANx_UT_TH									
Read	0	0	0	0	0	0										
Reset	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	0
Anx_UT_TH		Description		Undertemperature threshold setting for analog input x												
		1100001110		Undertemperature default set to 3.82 V												
		Reset condition		POR												

11.36 Silicon revision register – SILICON_REV

Table 70. SILICON_REV

SILICON_REV																
$6B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	0	0	0	0	0	0	0	0	0	0	FREV			MREV		
Reset	0	0	0	0	0	0	0	0	0	0	F	F	F	M	M	M
FREV		Description		Full mask revision												
		001		Pass 1.x												
		010		Pass 2.x												
		…														
		Reset condition		POR												
MREV		Description		Metal mask revision												
		000		Pass y.0												
		001		Pass y.1												
		…														
		Reset condition		POR												

11.37 EEPROM communication register EEPROM_CTRL

Table 71. EEPROM_CTRL

EEPROM_CTRL																
$6C	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	R/W	EEPROM_ADD							DATA_TO_WRITE							
Read	BUSY	ERROR	EE_ PRESENT	0	0	0	0	0	READ_DATA							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R/W	Description	Read/write bit, directs the BMI7014 to read or write from EEPROM
	0	Write
	1	Read
	Reset condition	POR
EEPROM_ADD	Description	EEPROM address to read or write
	Reset condition	POR
DATA_TO_WRITE	Description	Data to be written into the EEPROM
	Reset condition	POR
BUSY	Description	Busy bit
	0	Indicates the IC has completed the EEPROM read or write operation
	1	Indicates the IC is in the process of performing the EEPROM read or write operation.
	Reset condition	POR
ERROR	Description	EEPROM communication error bit.
	0	No error occurred during the communication to EEPROM
	1	An error occurred during the communication to EEPROM
	Reset condition	POR
EE_PRESENT	Description	EEPROM detection
	0	No EEPROM detected
	1	EEPROM has been detected and present
	Reset condition	POR
READ_DATA	Description	Data read in the EEPROM at address given by EEPROM_ADD
	Reset condition	POR

11.38 ECC signature 1 register

Table 72. DED_ENCODE1

DED_ENCODE1																
$6D	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	DED_HAMMING_COUT1_31_16															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DED_HAMMING_ COUT1_31_16	Description	Reports the 16 MSBits to encode in the fuse matrix (ECC)
	Reset condition	POR

11.39 ECC signature 2 register

Table 73. DED_ENCODE2

DED_ENCODE2																
$6E	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	DED_HAMMING_COUT_1_15_0															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DED_HAMMING_ COUT_1_15_0	Description	Report the 16 LSBits to encode in the fuse matrix (ECC)
	Reset condition	POR

11.40 FUSE mirror and data control

Table 74. FUSE_MIRROR_DATA

FUSE_MIRROR_DATA																
$6F	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	FMR_DATA															
Read																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMR_DATA	Description	Fuse mirror data to read or write
	Reset condition	POR

Table 75. FUSE_MIRROR_CNTL

FUSE_MIRROR_CNTL																
$70	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	w0c[1]			FMR_ADDR									FSTM	FST		
Read	SEC_ ERR_ FLT	0	0						0	0	0	0	0	FST_ST		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SEC_ERR_FLT	Description	ECC error, single error correction
	0	No error
	1	A single error has been detected and corrected. The IC is usable, must not be considered defective.
	Reset condition	POR/clear on write 0
FMR_ADDR	Description	Fuse mirror register address
	Reset condition	POR
FSTM	Description	Fuse state write mask. This bit controls the write access to the FST[2:0] bits.
	0	Writing in FST bits has no effect
	1	FST bits are unlocked for writing
	Reset condition	POR
FST	Description	Fuse state control. write to this register controls the switching of the fuse state machine. Read in this register enables tracing the current state.
	0 0 0	Refer to Section 9.11 for bit description.
	Reset condition	POR
FST_ST	Description	Fuse state control. Read in this register enables to trace the current state
	0 0 0	Refer to Section 9.11 for bit description.
	Reset condition	POR

[1] w0c: write 0 to clear

11.41 Reserved

Table 76. RESERVED

Reserved																
$71 to $FF	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	Do not change															
Read																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.42 Fuse bank

Table 77. FUSE_BANK

<table>
<tr><th rowspan="2">Bank address</th><th colspan="16">Data</th></tr>
<tr><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>$00</td><td colspan="6">GCF_cold_c13</td><td colspan="10">GCF_room_c13</td></tr>
<tr><td>$01</td><td colspan="6">GCF_cold_c11</td><td colspan="10">GCF_room_c11</td></tr>
<tr><td>$02</td><td colspan="6">GCF_cold_c9</td><td colspan="10">GCF_room_c9</td></tr>
<tr><td>$03</td><td colspan="6">GCF_cold_c7</td><td colspan="10">GCF_room_c7</td></tr>
<tr><td>$04</td><td colspan="6">GCF_cold_c5</td><td colspan="10">GCF_room_c5</td></tr>
<tr><td>$05</td><td colspan="6">GCF_cold_c3</td><td colspan="10">GCF_room_c3</td></tr>
<tr><td>$06</td><td colspan="6">cold_c2vs1</td><td colspan="10">GCF_room_c1</td></tr>
<tr><td>$0B</td><td colspan="6">GCF_hot_c5</td><td colspan="5">GCF_ANx_ratio</td><td colspan="2">room_c14vs13</td><td colspan="3">hot_c14vs13</td></tr>
<tr><td>$0C</td><td colspan="6">GCF_hot_c3</td><td colspan="5">hot_c2vs1</td><td colspan="2">room_c12vs11</td><td colspan="3">hot_c12vs11</td></tr>
<tr><td>$0D</td><td>Single Side</td><td colspan="2">c2_offset</td><td colspan="2">cold_c14vs13</td><td colspan="2">cold_c12vs11</td><td colspan="2">cold_c10vs9</td><td colspan="2">cold_c6vs5</td><td colspan="2">room_c10vs9</td><td colspan="3">hot_c10vs9</td></tr>
<tr><td>$0E</td><td colspan="7">GCF_hot_c1</td><td colspan="2">cold_c8vs7</td><td colspan="2">cold_c4vs3</td><td colspan="2">room_c8vs7</td><td colspan="3">hot_c8vs7</td></tr>
<tr><td>$0F</td><td colspan="7">GCF_stack</td><td colspan="4">room_c2vs1</td><td colspan="2">room_c6vs5</td><td colspan="3">hot_c6vs5</td></tr>
<tr><td>$10</td><td colspan="7">GCF_cold_c1</td><td colspan="4">GCF_IcTemp</td><td colspan="2">room_c4vs3</td><td colspan="3">hot_c4vs3</td></tr>
<tr><td>$11</td><td colspan="7">cold_Vbgp2vs1</td><td colspan="9">x</td></tr>
<tr><td>$12</td><td colspan="7">cold_Vbgp1vs1</td><td colspan="9">x</td></tr>
<tr><td>$13</td><td colspan="7">hot_Vbgp2vs1</td><td colspan="9">x</td></tr>
<tr><td>$14</td><td colspan="7">hot_Vbgp1vs1</td><td colspan="9">x</td></tr>
<tr><td>$15</td><td colspan="8">room_Vbgp2vs1</td><td colspan="8">room_Vbgp1vs1</td></tr>
<tr><td>$16</td><td colspan="16">DED_ENCODE 2</td></tr>
<tr><td>$17</td><td colspan="16">DED_ENCODE 1</td></tr>
<tr><td>$18</td><td colspan="16">Traceability</td></tr>
<tr><td>$19</td><td colspan="16">Traceability</td></tr>
<tr><td>$1A</td><td colspan="11">Reserved</td><td colspan="5">Traceability</td></tr>
</table>

12 Typical applications

12.1 Introduction

NXP Semiconductors has developed a battery cell controller IC supporting both centralized and distributed battery management architectures. Centralized battery monitoring systems contain a controller module sensing individual differential cell voltages through a wiring harness. Distributed systems locate monitoring devices close to the lithium-ion batteries and use a communication interface to transfer data to the main controller MCU.

There are significant advantages to using transformers for isolation and communication. The most obvious benefit of the pulse transformers is the high degree of voltage isolation. Transformers specified in this document are automotive qualified and rated at 3750 Vrms. Using pulse transformers allow the NXP battery management system to achieve communication rates of 2.0 Mbps with very low radiated emissions.

An added benefit to the transformer daisy chain network is the ability to loop the network back to the pack controller. This feature allows the user to verify communication to each node in the daisy chain.

12.1.1 Centralized battery management system

A centralized system is comprised of a single transformer driver with a transformer or capacitive isolation between each battery cell controller IC.

The centralized battery monitoring system using capacitive isolation is shown in Figure 31.

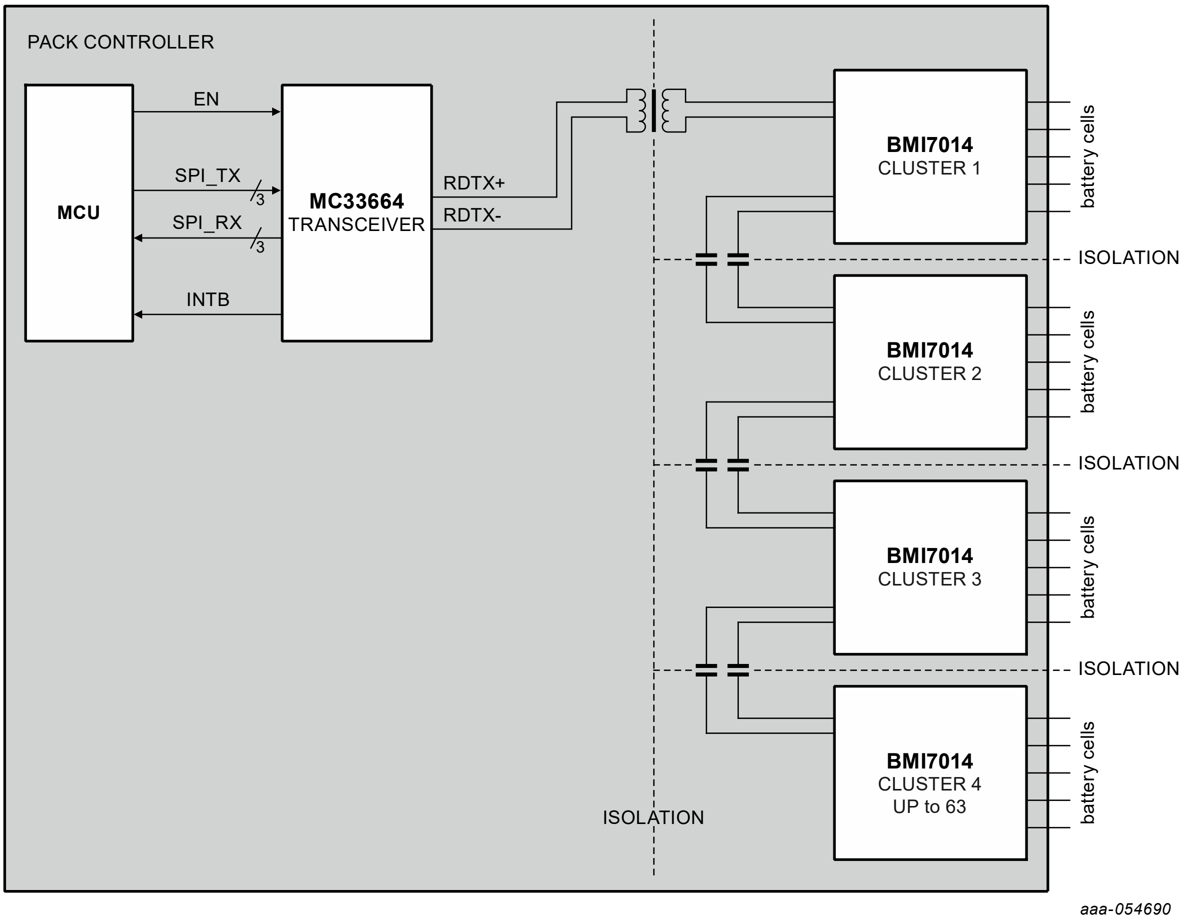


Figure 31. Centralized battery monitoring system with capacitive isolation

The centralized battery monitoring system using transformer isolation is shown in Figure 32

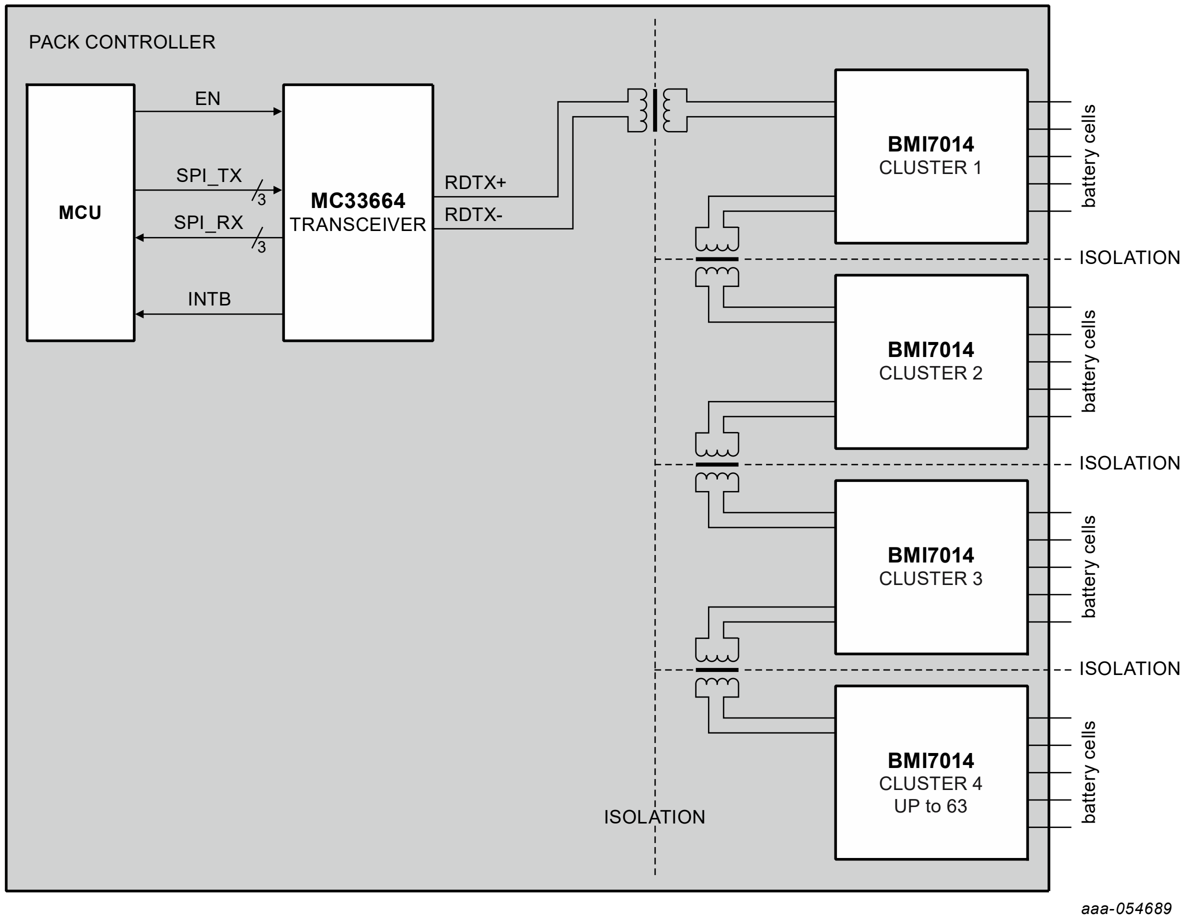


Figure 32. Centralized battery monitoring system with transformer isolation

12.1.2 Distributed battery management system

The distributed battery management solution is identical to the centralized system with an additional transformer and daisy chain cable in the pack controller and between each node.

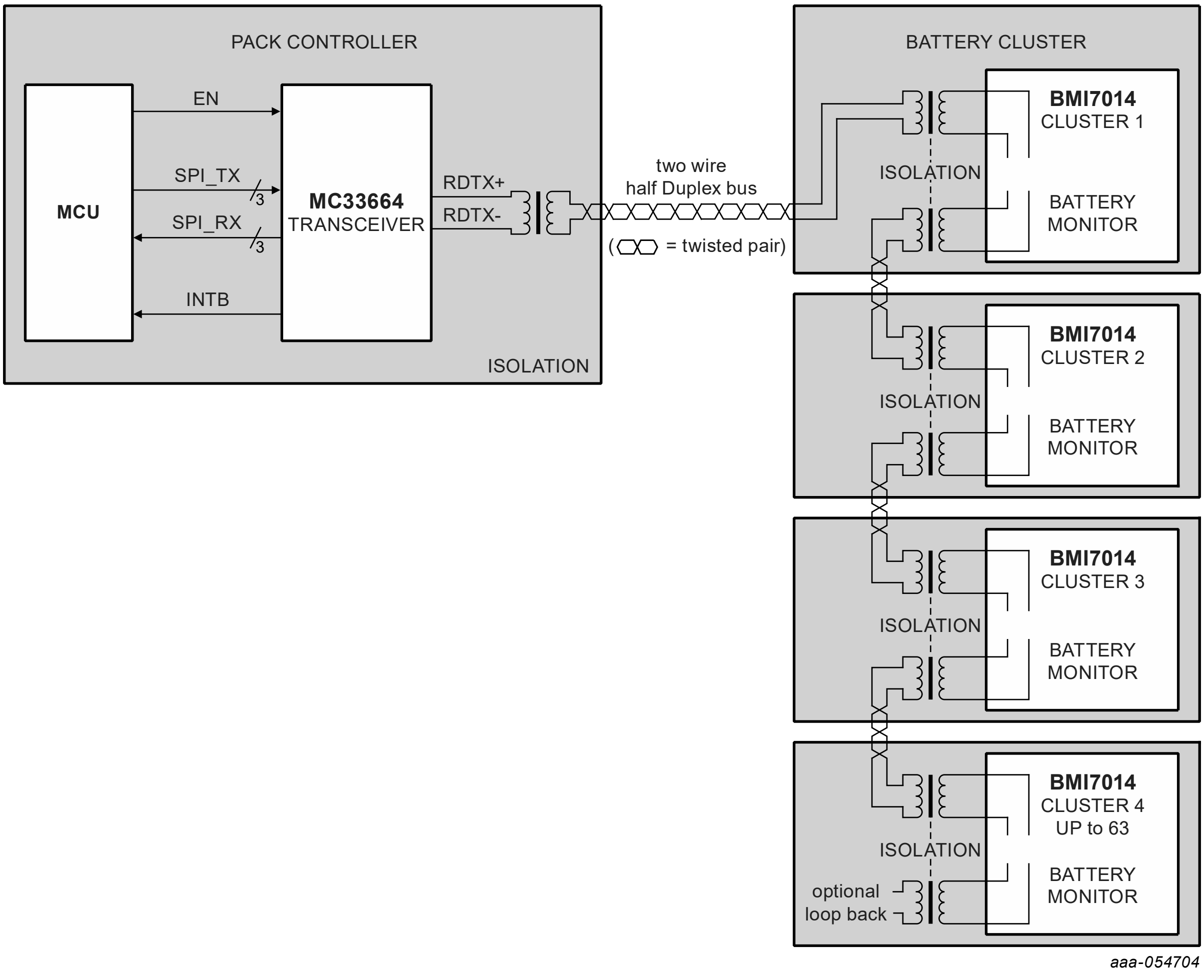


Figure 33. Distributed battery monitoring system

12.1.3 Multiple daisy chain

In a distributed system, the BMI7014 ICs can be connected in multiple daisy chains. The number of daisy chains supported by the BMI7014 IC is configurable with the MSB of the INIT[CID] register. Using one bit MSB of CID supports two daisy chains with up to 31 slave devices in each daisy chain. Similarly, using two bit MSB of CID supports 4 daisy chains with up to 15 slave devices in each daisy chain.

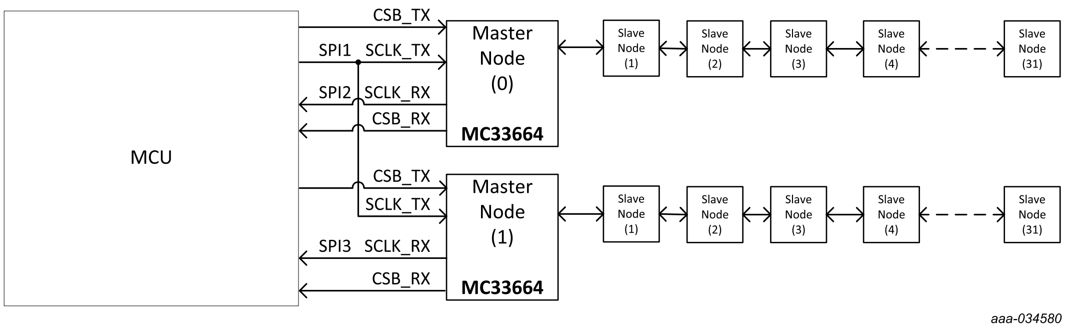


Figure 34. Example of multiple daisy chain.

12.1.4 Loop-back daisy chain

In a distributed system, the BMI7014 IC can also support a loop-back daisy chain with two master nodes connected at two SPI ports of the MCU. The slave devices are connected at each end of the master nodes as shown in the figure.

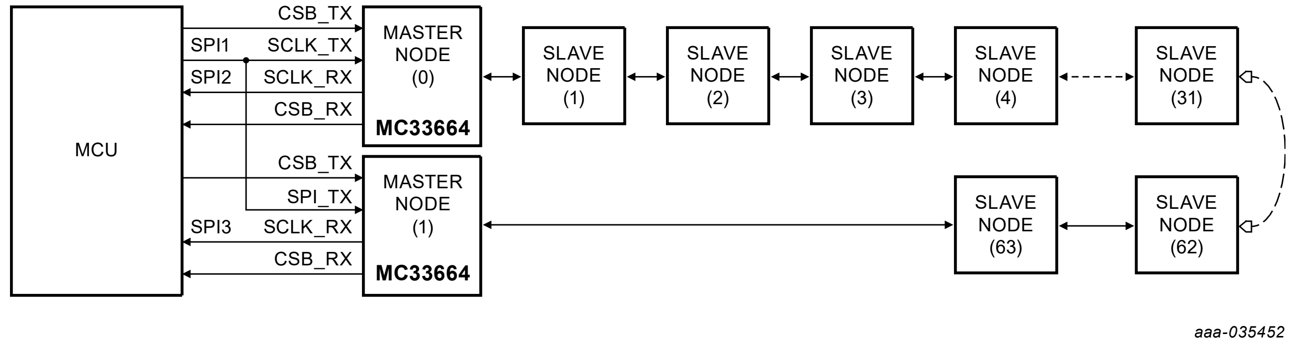


Figure 35. Example of loop-back daisy chain

Note: *In the case of a loop-back daisy chain configuration, the MCU shall use only one master node at a time for communicating with the BMI7014 IC.*

Note: *If multiple daisy chains are used in case of loop-back daisy chain communication, then two master nodes forming one complete loop are to be assigned with one daisy chain address.*

12.2 BMI7014 external components

This section provides information about recommended external components and how to select them.

12.2.1 Cell terminal filters

Figure 36 shows the recommended second order low-pass filters for cell voltages.

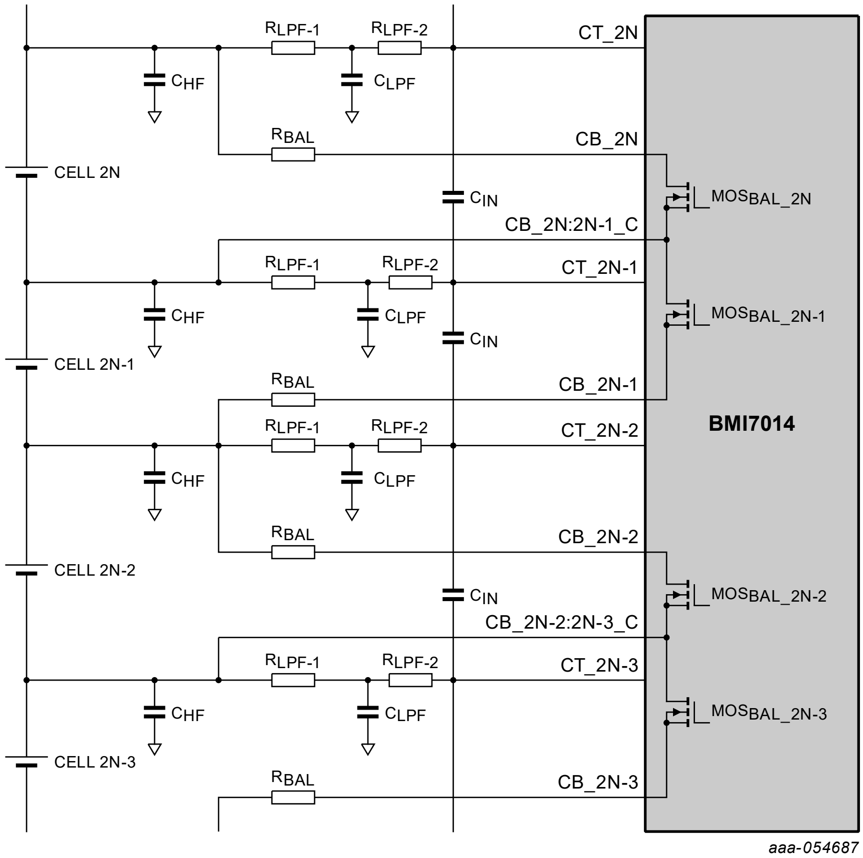


Figure 36. Second order cell terminal filters and cell balancing resistors (internal cell balancing MOSFETs are shown for clarity)

Table 78. CT filter components

ID	Value	Units	Comments
C_{HF}	0.047	µF	Value used and tested at NXP Semiconductors to withstand ESD gun and hot plug
R_{LPF-1}	3	kΩ	Value used and tested to withstand hot plug at NXP. Low-pass filter resistor R_{LPF-1} together with C_{LPF} determine the filter cut-off frequency. This value must not be changed. Component tolerance depends on the wanted accuracy for the bandwidth. See Equation (1) and Equation (2) .
C_{LPF}	0.1	µF	This capacitance value together with R_{LPF-1} provides 530 Hz cut-off frequency. Value used and tested to withstand hot plug at NXP. Component tolerance depends on the wanted accuracy for the bandwidth. See Equation (1) and Equation (2).
R_{LPF-2}	2	kΩ	Value used and tested to withstand hot plug at NXP. This value must not be changed. No special requirement for the tolerance of this component.
C_{IN}	0.01	µF	Value used and tested to withstand hot plug at NXP. This value must not be changed. No special requirement for the tolerance of this component.
R_{BAL}	X	Ω	Any value is possible, as long as the cell balance current does not exceed 300 mA
R_{BAL_C}	$R_{BAL}/5$	Ω	Maximum value

Using the arrangement shown in Figure 36, the filter cut-off frequency in Hz, depending on the measurement time constant τ, is given by the following formula:

$$f_{cut} = 1 / (2\pi\tau) \quad (1)$$

$$\tau = R_{LPF-1} C_{LPF} \quad (2)$$

For noisy applications if the customer cannot guarantee to keep CTREF voltage within the limits described in Table 7 footnote [6], a setup of dual anti-parallel Schottky diodes can be added between CTREF battery connector pin and module ground to limit the voltage drop amplitude in transient. These diodes should be placed close to the corresponding Rlpf-1 resistor (CT_REF pin low pass filter).

12.2.2 Unused cells

If the cluster has less than the maximum number of cells, the usage of cell terminal pins CTx and cell balancing pins CBx has to satisfy some constraints. Each external LPF block is masked, as shown in Figure 37, to simplify the diagrams. As a convention, cell numbering is exactly the same as the associated CTx. For example, cell 12 is the one whose positive terminal is connected to CT12, even though it is the 5th cell in a seven cell system, see Figure 38. A minimum of seven cells must be used. At least cell 1 through cell 4 and cell 12 through cell 14 must be used. Unused cells must start with CT5. Stacked cells arrangements from 7 to 14 cells are described in Table 79.

Table 79. Stacked cells arrangements

	stacked cells							
Cell	14	13	12	11	10	9	8	7
1	CT_REF/CT1	CT_REF/CT1	CT_REF/CT1	CT_REF/CT1	CT_REF/CT1	CT_REF/CT1	CT_REF/CT1	CT_REF/CT1
2	CT1/CT2	CT1/CT2	CT1/CT2	CT1/CT2	CT1/CT2	CT1/CT2	CT1/CT2	CT1/CT2
3	CT2/CT3	CT2/CT3	CT2/CT3	CT2/CT3	CT2/CT3	CT2/CT3	CT2/CT3	CT2/CT3
4	CT3/CT4	CT3/CT4	CT3/CT4	CT3/CT4	CT3/CT4	CT3/CT4	CT3/CT4	CT3/CT4
5	CT4/CT5	CT5/CT6	CT6/CT7	CT7/CT8	CT8/CT9	CT9/CT10	CT10/CT11	CT11/CT12
6	CT5/CT6	CT6/CT7	CT7/CT8	CT8/CT9	CT9/CT10	CT10/CT11	CT11/CT12	CT12/CT13
7	CT6/CT7	CT7/CT8	CT8/CT9	CT9/CT10	CT10/CT11	CT11/CT12	CT12/CT13	CT13/CT14
8	CT7/CT8	CT8/CT9	CT9/CT10	CT10/CT11	CT11/CT12	CT12/CT13	CT13/CT14	
9	CT8/CT9	CT9/CT10	CT10/CT11	CT11/CT12	CT12/CT13	CT13/CT14		
10	CT9/CT10	CT10/CT11	CT11/CT12	CT12/CT13	CT13/CT14			
11	CT10/CT11	CT11/CT12	CT12/CT13	CT13/CT14				
12	CT11/CT12	CT12/CT13	CT13/CT14					
13	CT12/CT13	CT13/CT14						
14	CT13/CT14							

Notes:

- *CT5 is always populated with the full low-pass filter.*
- *Other not used pins are shorted directly to CT5.*

As a general rule, unused CTx have to be terminated to the positive terminal of cell 4. As shown, several external components may be removed. Cell balancing resistors (R_{BAL}) of unused cells are to be mounted and terminated at the positive terminal of cell 4. Resistors for hot plug protection R_{LPF-2} must also be mounted.

A different number of missing cells leads to an application diagram analogous to Figure 38 . In general, if the cluster has N missing cells, it is possible to save N−2 times C_{HF}, N-2 times R_{LPF}-1, N-2 times C_{LPF} and N times C_{IN} mentioned in Table 78.

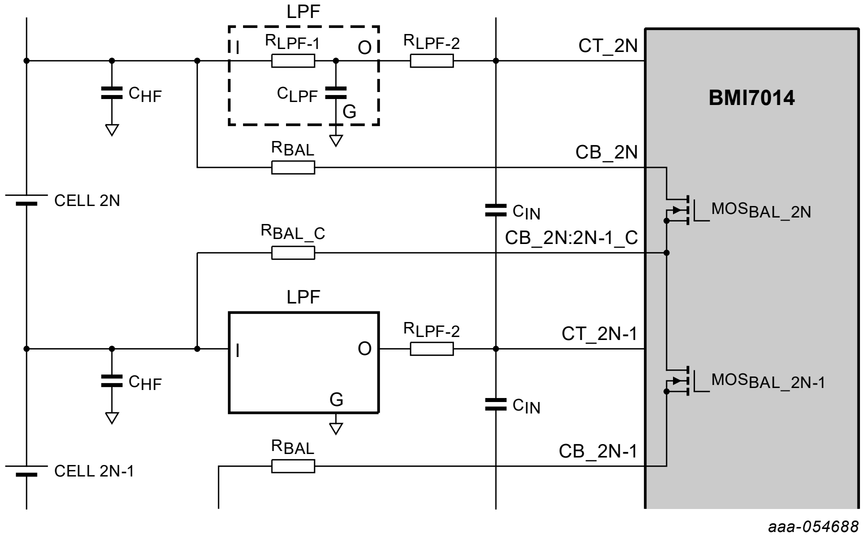


Figure 37. LPF block masking

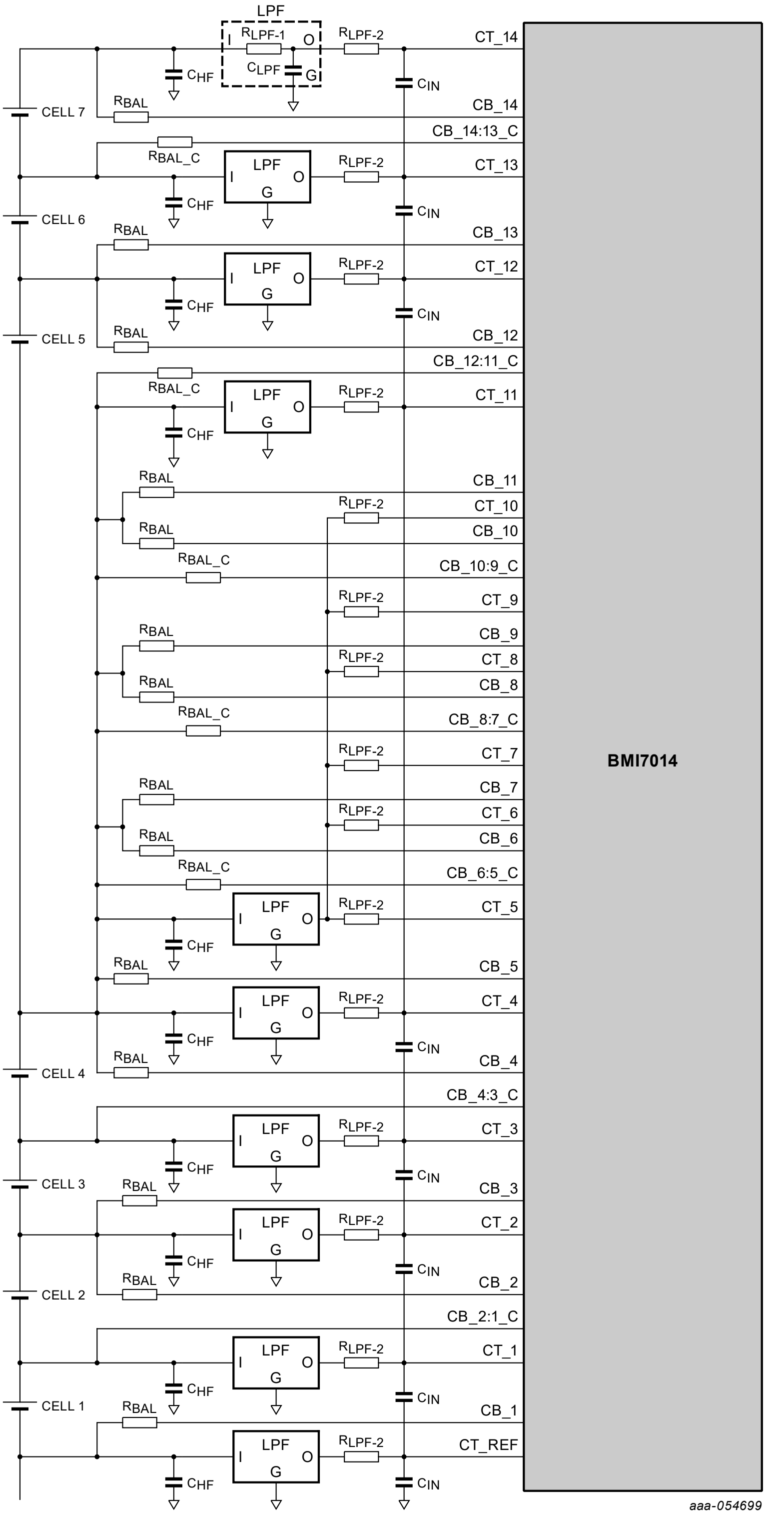


Figure 38. The seven-cell configuration

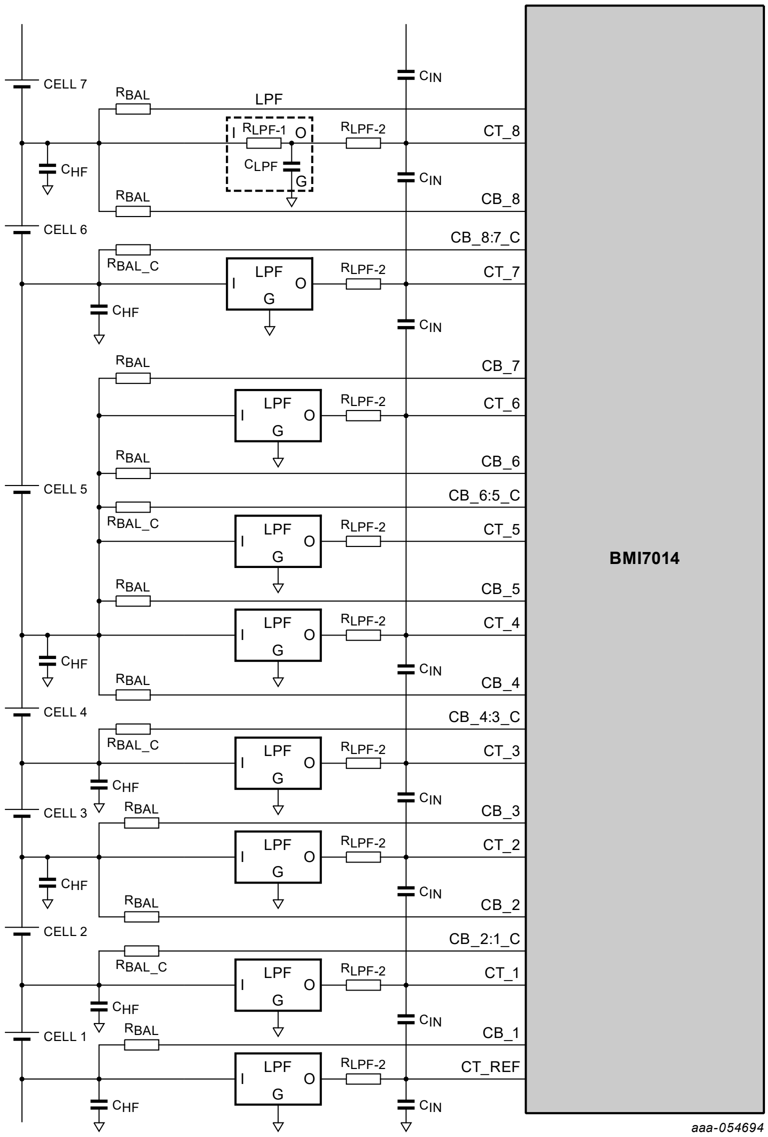


Figure 39. The 12-cell configuration

12.2.3 Hot plug protection

The VPWR line, shown in Figure 40, must be protected by a serial resistor in order to limit the inrush current and a parallel capacitor to filter fast voltage variation. A higher value of R_{VPWR} provides better protection. The drawback of higher R_{VPWR} is higher voltage drop. The minimum battery voltage (V_{BAT}) supplying the device through the R_{vpwr}resistor is then equal to Equation (12) . As the stack voltage is measured across VPWR1, 2 pins and ground, stack measurement is affected by such voltage drop. Furthermore, voltage drops higher than V_{VPWR_CT} have a negative impact on cell measurement accuracy.

$$\min(V_{\mathrm{BAT}}) = \max\left(V_{\mathrm{PWR(UV\_POR)}} + R_{\mathrm{vpwr}} * \left[\max(I_{\mathrm{VPWR(TPL\_TX)}}) + \max(I_{\mathrm{LIM\_VCOM(OC)}}) + \max(I_{\mathrm{LIM\_VANA(OC)}})\right]\right) \quad (12)$$

In order to withstand hot plug, it is mandatory to use Zener diodes as shown in Figure 40 close to the VPWR line. In general, all components, whose values are given in Table 80, are mandatory to protect the IC when a connection is made to the battery pack. Changing the value of any external components listed in Table 80 may result in serious IC damage during the connection to the battery pack. Capability of the device to sustain random connection to live voltage for pins VPWRx, CT_x, CB_x, CTREF, GND has been extensively evaluated. Nevertheless, the total number of random combinations related to those pins cannot be entirely tested. Therefore, despite all engineering efforts performed by NXP, it is the responsibility of the system provider to ensure safe connection to the battery pack.

Furthermore, it is the responsibility of the system provider to manage the risk of short circuits on any external components connected to the IC, including external low-pass filters. A short-circuit on the pins connected to the battery can lead to high current flowing through the IC, causing a thermal event on the PCB. The system provider must employ common practices, such as fuse protection on the VPWR line, series of capacitors on the CT pins, appropriate power rating for external resistors, or any other appropriate measure capable to mitigate hazards.

Zener diodes D1 to D4 are required to protect internal ESD structures between VPWR and CB_x pins, when VPWR is connected before cells. The energy to charge the C_{HF} capacitors on CB_x pins exceeds the capability of the internal ESD devices for VPWR max operating range. Zener diodes D1 to D4 are placed on CB_14, CB_12, CB_10:9_C and CB_8:7_C pins according to the internal ESD protection network. The joint presence of these Zener diodes and the set of internal cell balancing transistors, which are highly robust due to their large size, guarantee hot plug protection of the following pins: CB_14:13_C, CB_13, CB_12:11_C, CB_11, CB_10, CB_9, CB_8, and CB_7. All other CB_x pins do not need external Zener diodes, because the internal ESD clamping voltage is higher than the VPWR max operating value. Clamping voltages of Zener diodes D1 to D4 are defined to be higher than the maximum rating between VPWR and CB_x, and lower than the clamping voltage of the internal ESD devices between these pins.

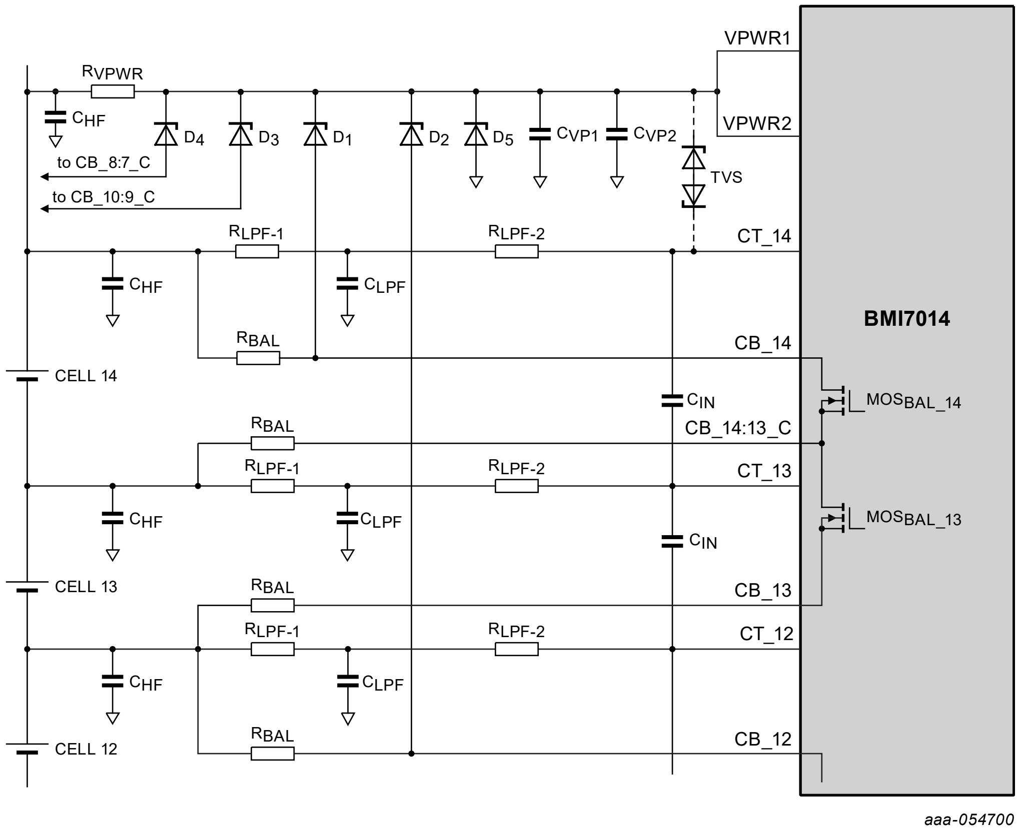


Figure 40. Top cell terminal filters and balancing resistors, VPWR1, 2 components to withstand hot plug

Table 80. Components to avoid hot plug issues

ID	Value	Units	Comments
D_5	75	V	To protect the IC against transient overvoltage, use the specified Zener voltage. For example, use MMSZ5267BT1G (75V) or BZX384-B75
D_4	43	V	D4 is rated 43 V because max operating voltage between VPWR and CB_8:7_C is 35 V and typical internal ESD clamping voltage between VPWR and CB_8:7_C is 60 V. For example, use MMSZ5260BT1G (43v) or BZX384-B43.
D_3	27	V	D3 is rated in the range 26.5 V to 29.5 V, because max operating voltage between VPWR and CB_10:9_C is 25 V and typical internal ESD clamping voltage between VPWR and CB_10:9 is 50 V. The diode voltage rating is limited because the typical internal ESD clamping voltage between VPWR and CT9 is 33v. For example, use MMSZ5255BT1G (28v) or BZX384-B27.
D_2	20	V	D2 is rated 20 V, because max operating voltage between VPWR and CB_12 is 10 V and typical internal ESD clamping voltage between VPWR and CB_12 is 50 V. For example, use MMSZ5250BT1G (20v) or BZX384-B20.
D_1	2 x 8.2	V	D1 is rated 16.4 V, because max operating voltage between VPWR and CB_14 is 10 V and typical internal ESD clamping voltage between VPWR and CB_14 is 50 V. Implementation may be done by using two diodes in series, each of which having half Zener voltage. For example, use two MMSZ5237BT1G (8.2v) or two BZX384-B8V2.
R_{VPWR}	10	Ω	Reducing resistance value may jeopardize hot plug capability. Power rating is 0.1 W.
C_{VP1}	220	nF	To withstand hot plug, this value must not be changed
C_{VP2}	1	nF	Ceramic capacitor

Table 80. Components to avoid hot plug issues...*continued*

ID	Value	Units	Comments
TVS (optional)	8	V	If V_{PWR} > 55 V during hot plug then a TVS (PESD5V0V1BB or equivalent) should be added between CT14 and VPWR. The indicated voltage is the nominal breakdown voltage.

12.2.4 Temperature channels

Figure 41 shows usage of GPIOx as analog inputs (ANx) for temperature measurements. If not used, each GPIOx may be shorted to GND.

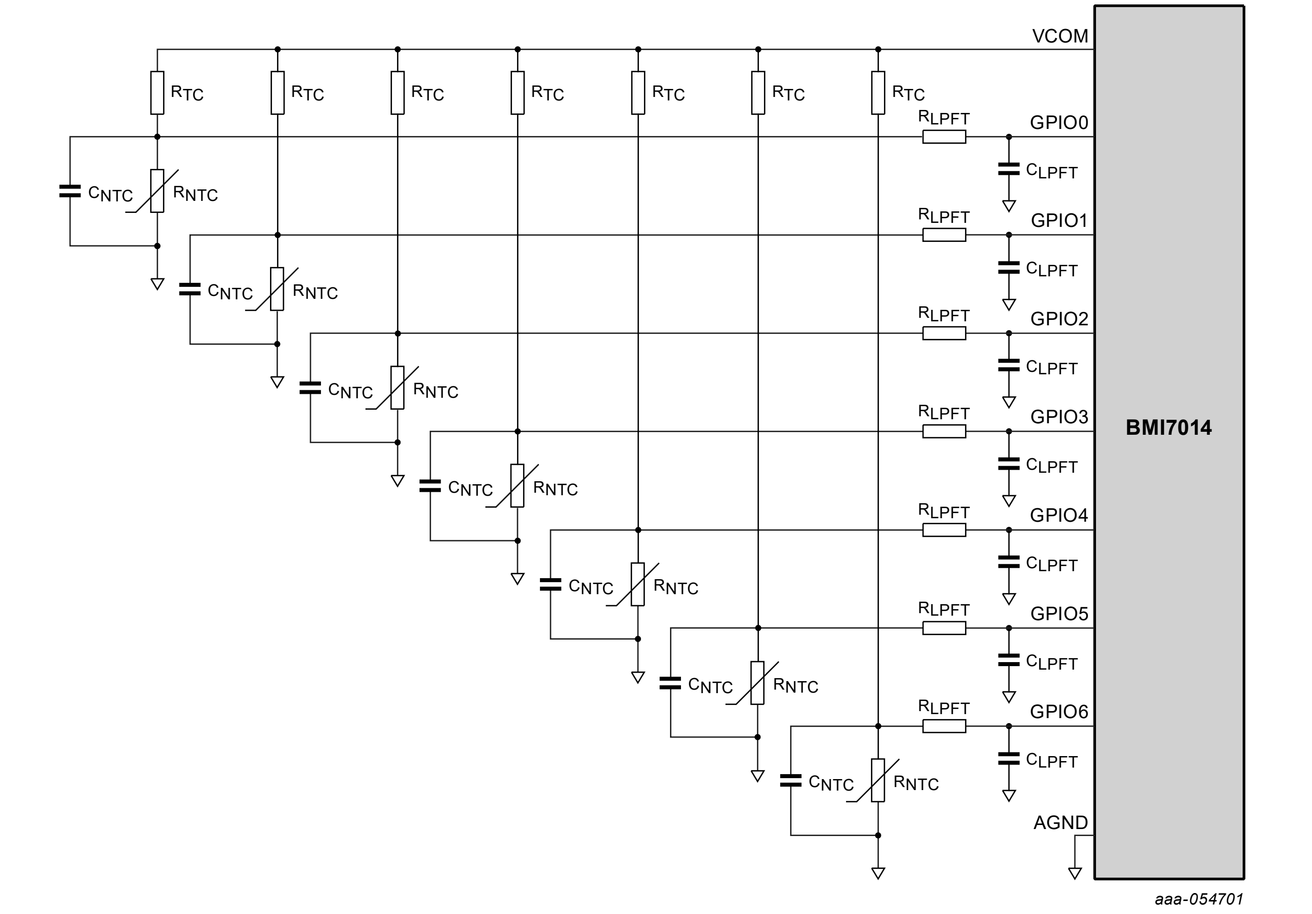


Figure 41. GPIOx used as ANx

Table 81. ANx filter components

ID	Value	Units	Comments
R_{TC}	6.8	kΩ	Component with 1 % tolerance, for accurate temperature measurement. Proposed value, together with all other proposed values, gives approximately f_{CUTT} = 10 kHz. See Equation (18), Equation (19), Equation (20), and Equation (21).
R_{NTC}	10	kΩ	Nominal resistance value is given at 25 °C, tolerance must be 5 % or better
C_{NTC}	1.2	nF	This component is for ESD protection
R_{LPFT}	3.3	kΩ	Influences the channel bandwidth. See Equation (18), Equation (19), Equation (20), and Equation (21).

Table 81. ANx filter components*...continued*

ID	Value	Units	Comments
C_{LPFT}	1.2	nF	5 % tolerance or better. Influences the channel bandwidth. See Equation (18), Equation (19), Equation (20), and Equation (21).

The signal cutoff frequency (in Hz) for the arrangement shown in Figure 41 of GPIOx used as radiometric analog inputs, depends on the measurement time constant τ_T, given by the following formula.

$$f_{cutT} = 1 / (2\pi\tau_T) \tag{18}$$

where,

$$\tau_T = \max(\tau_1, \tau_2) \tag{19}$$

$$\tau_1 = (R_{LPFT} + (R_{TC}R_{NTC})/(R_{TC} + R_{NTC}))C_{LPFT} \tag{20}$$

$$\tau_2 = C_{NTC}(R_{TC}R_{NTC}) / (R_{TC} + R_{NTC}) \tag{21}$$

In case the NTC resistor is located outside of the board and can be submitted to large EMC and ESD Gun constraints, the recommended filter for temperature is 2nd order as shown in Figure 42.

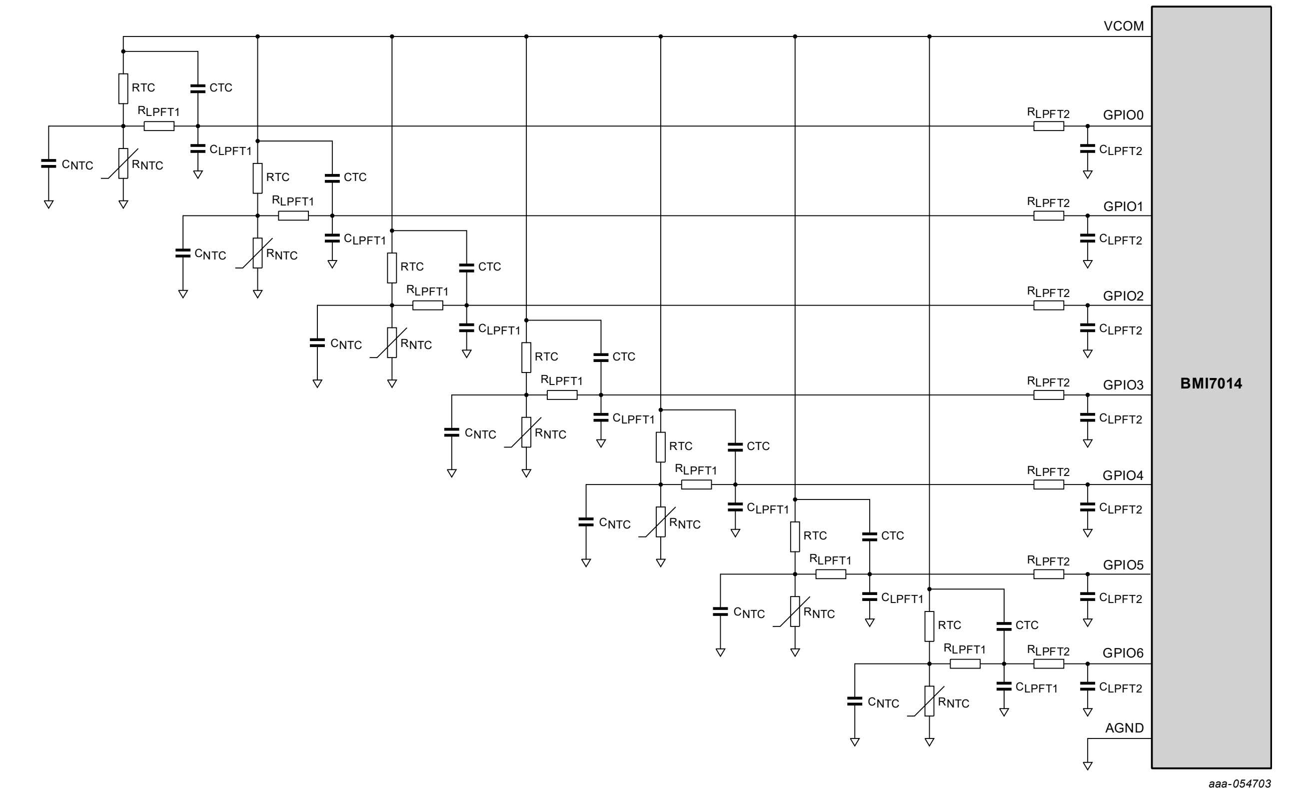


Figure 42. GPIOx used as ANX (with 2nd order filter)

Table 82. ANx second order filter components

ID	Value	Units	Comments
R_{TC}	6.8	kΩ	Component with 1 % tolerance, for accurate temperature measurement
C_{TC}	1.2	nF	
R_{NTC}	10	kΩ	Nominal resistance value is given at 25 °C, tolerance must be 5 % or better
C_{NTC}	1.2	nF	This component is for ESD protection
C_{LPFT1}	1.2	nF	5 % tolerance or better
R_{LPFT1}	3.3	kΩ	
C_{LPFT2}	1.2	nF	5 % tolerance or better
R_{LPFT2}	3.3	kΩ	

12.2.5 Centralized applications

12.2.5.1 Centralized applications - Transformer or capacitive isolation - Master node

For capacitive isolation in a centralized system the schematic is split into two segments. The first segment displays the external component of master node as shown in Figure 43. The second segment displays the external components between two BMI7014 ICs as shown in Figure 44. In high voltage system applications, a high voltage isolation transformer is recommended between master node and first slave node.

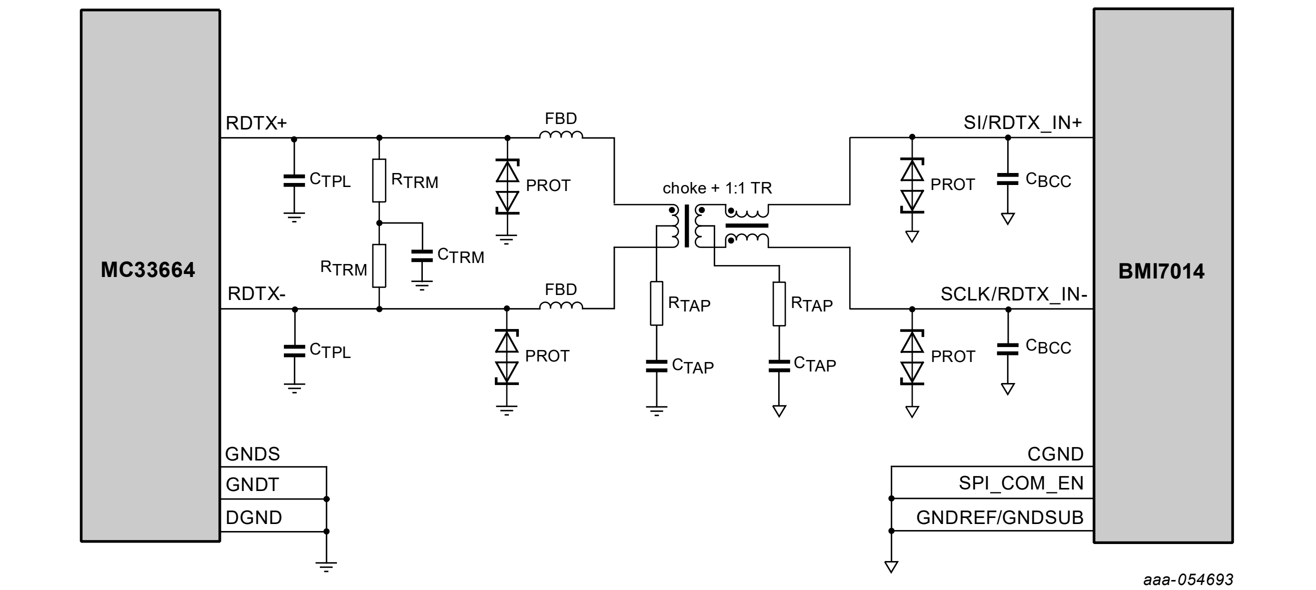


Figure 43. Master node in a centralized application with transformer isolation

Table 83. Master node components for a centralized application with transformer or capacitive isolation

ID	Value	Units	Comments
C_{TPL}	68	pF	Ceramic capacitor
C_{TRM}	4.7	nF	Ceramic capacitor for split termination of MC33664
R_{TRM}	75	Ω	Split termination resistor for MC33664
PROT	8	V	ESD protection. Use PESD5VOV1BB or equivalent. The indicated voltage is the nominal breakdown voltage.
R_{TAP}	150	Ω	Center tap resistor
C_{TAP}	10	nF	Center tap capacitor
C_{BCC}	220	pF	Ceramic capacitor
Choke +1:1 TR	Pulse Electronic HM2103	NA	Single-channel transformer with common mode choke
FBD	120	Ω	Ferrite Bead (optional). Use MMZ1608Y121BTD25 or equivalent.

12.2.5.2 Centralized applications - Capacitive isolation - Slave node

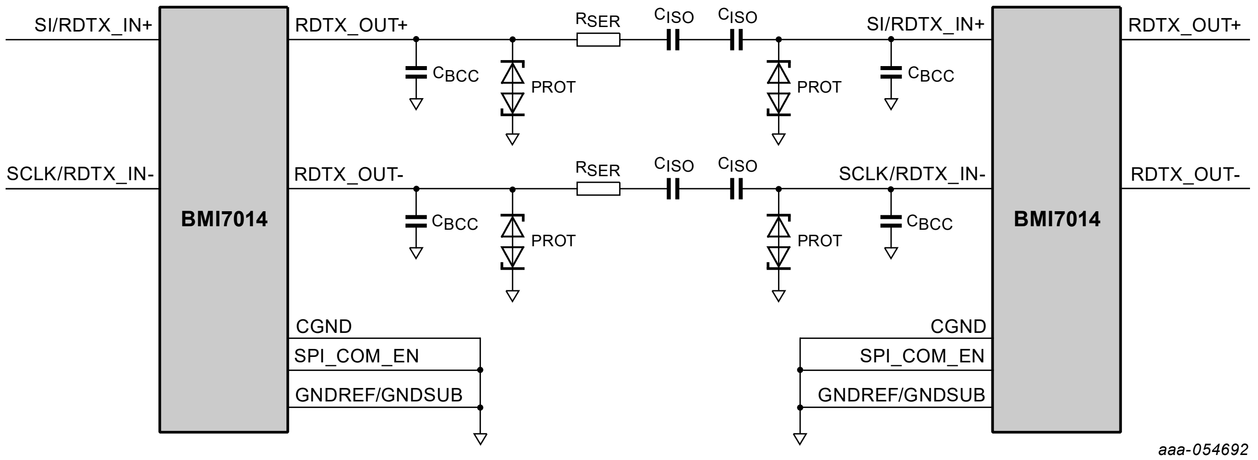


Figure 44. Slave node for a centralized application with capacitive isolation

Table 84. Slave node components for a centralized application with capacitive isolation

ID	Value	Units	Comments
C_{BCC}	22	pF	Ceramic capacitor
R_{SER}	62	Ω	Series resistance
C_{ISO}	10	nF	Isolation capacitor
PROT	8	V	ESD protection. Use PESD5V0V1BB or equivalent. The indicated voltage is the nominal breakdown voltage.

12.2.5.3 Centralized applications - Transformer isolation - Slave node

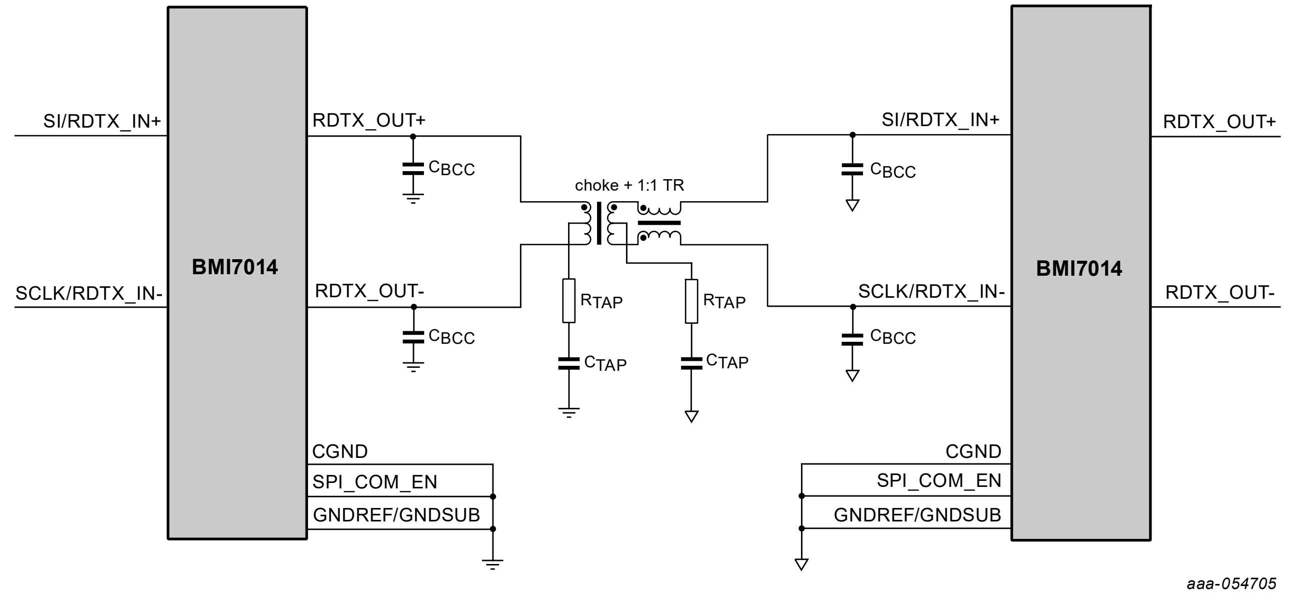


Figure 45. Slave node for a centralized application with transformer isolation

Table 85. Slave node components for a centralized application with transformer isolation

ID	Value	Units	Comments
C_{BCC}	220	pF	Ceramic capacitor
C_{TAP}	10	nF	Center tap capacitor
R_{TAP}	150	Ω	Center tap resistor

12.2.6 Distributed applications

12.2.6.1 Distributed systems - Master node

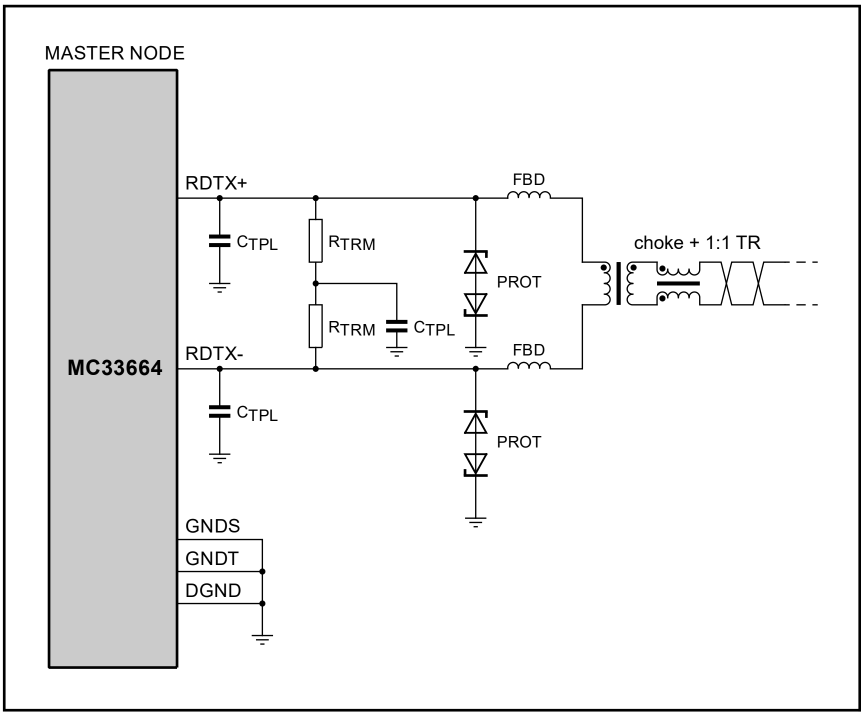


Figure 46. Master node in a distributed system (transformer isolation only)

Table 86. Master node components in a distributed system

ID	Value	Units	Comments
C_{TPL}	68	pF	Ceramic capacitor
C_{TRM}	4.7	nF	Ceramic capacitor for split termination of MC33664
R_{TRM}	75	Ω	Split termination resistor for MC33664
PROT	8	V	ESD protection. Use PESD5V0V1BB or equivalent. The indicated voltage is the nominal breakdown voltage.
Choke + 1:1 TR	Pulse Electronic HM2103	NA	Single-channel transformer with common mode choke
FBD	470	Ω	Ferrite Bead (optional).Use MMZ1608Q471BTD25 or equivalent

12.2.6.2 Distributed applications - Slave node

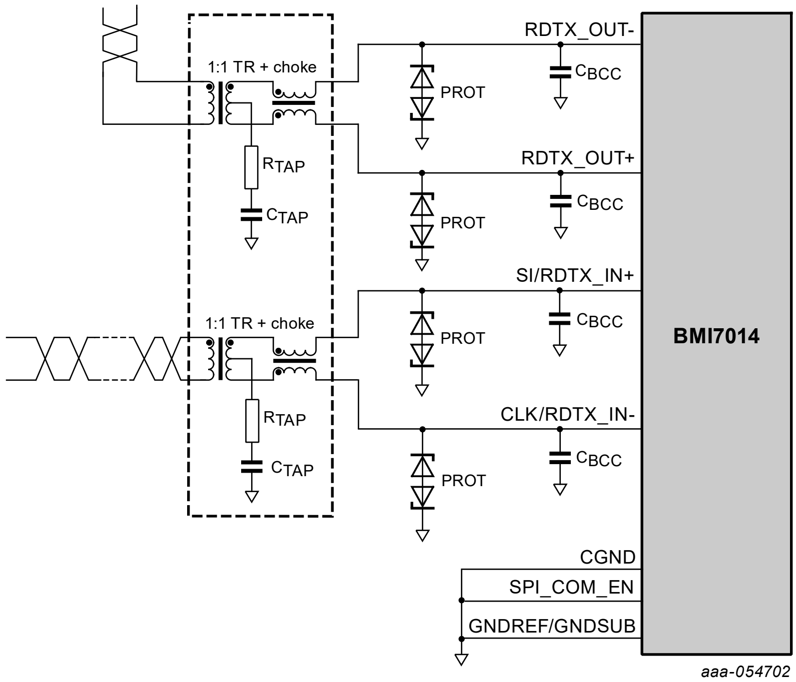


Figure 47. Slave node of a distributed application (transformer isolation only)

Table 87. Slave node components in a distributed application

ID	Value	Units	Comments
C_{BCC}	220	pF	Ceramic capacitor
PROT	8	V	ESD protection. Use PESD5V0V1BB or equivalent. The indicated voltage is the nominal breakdown voltage.
C_{TAP}	10	nF	Center tap capacitor
R_{TAP}	150	Ω	Center tap resistor
1:1 TR + choke	PULSE Electronic HM2102		Dual-channel transformer with common mode choke

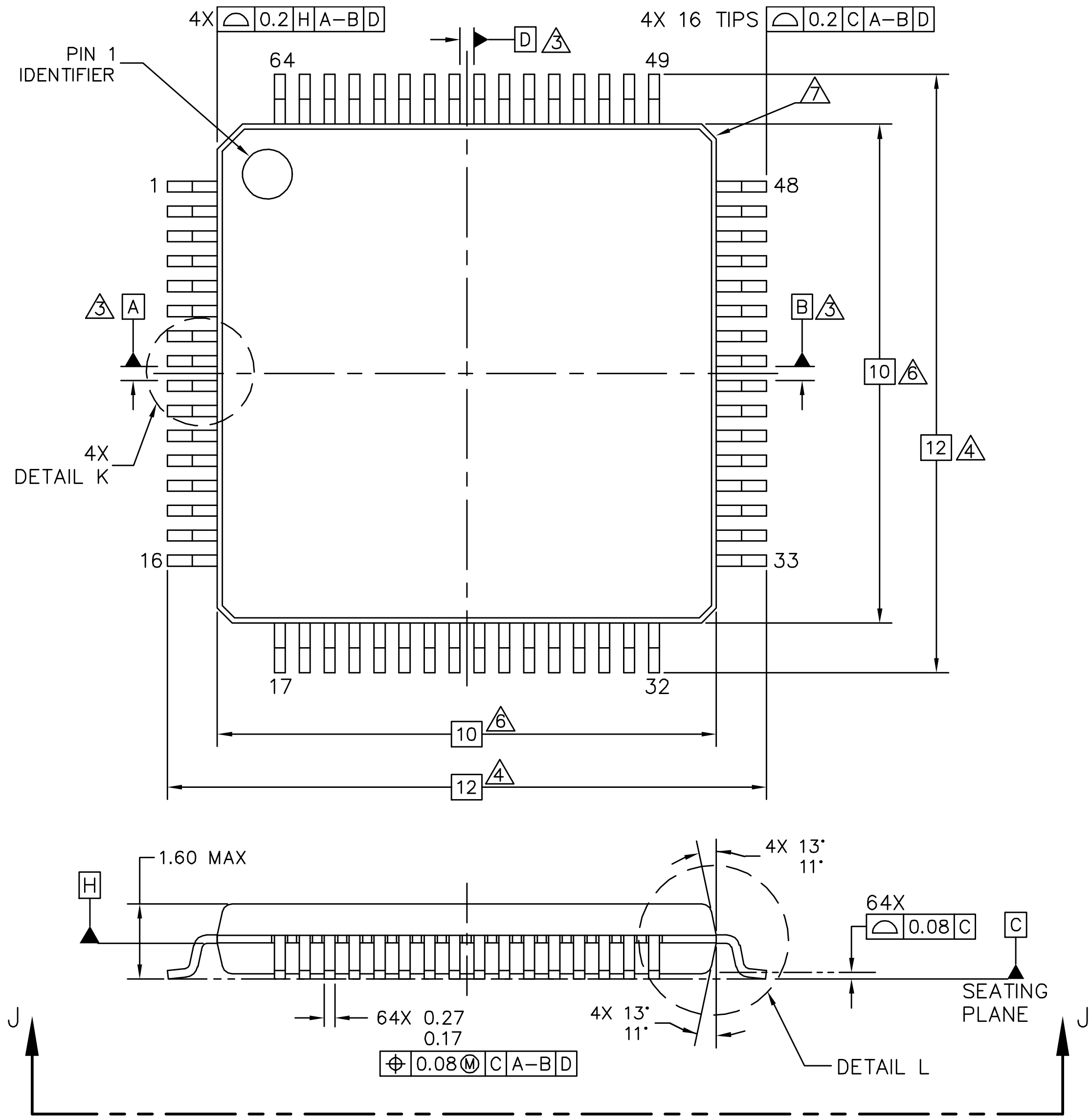
13 Packaging

13.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

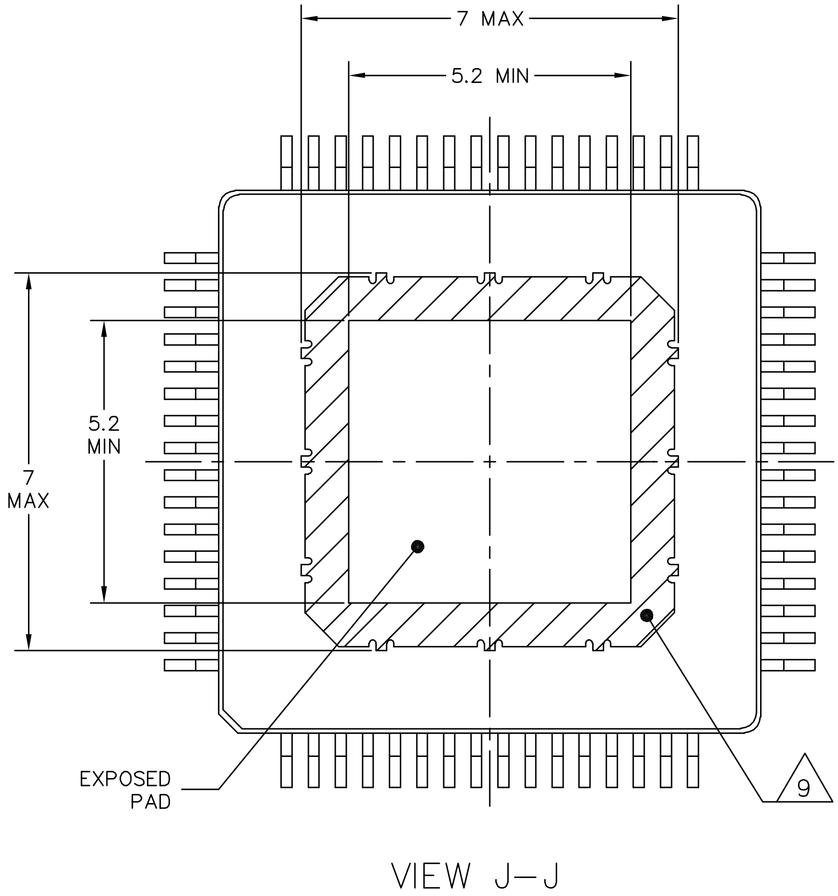
Table 88. Package outline

Package	Suffix	Package outline drawing number
64-pin LQFP-EP	AE	98ASA10763D



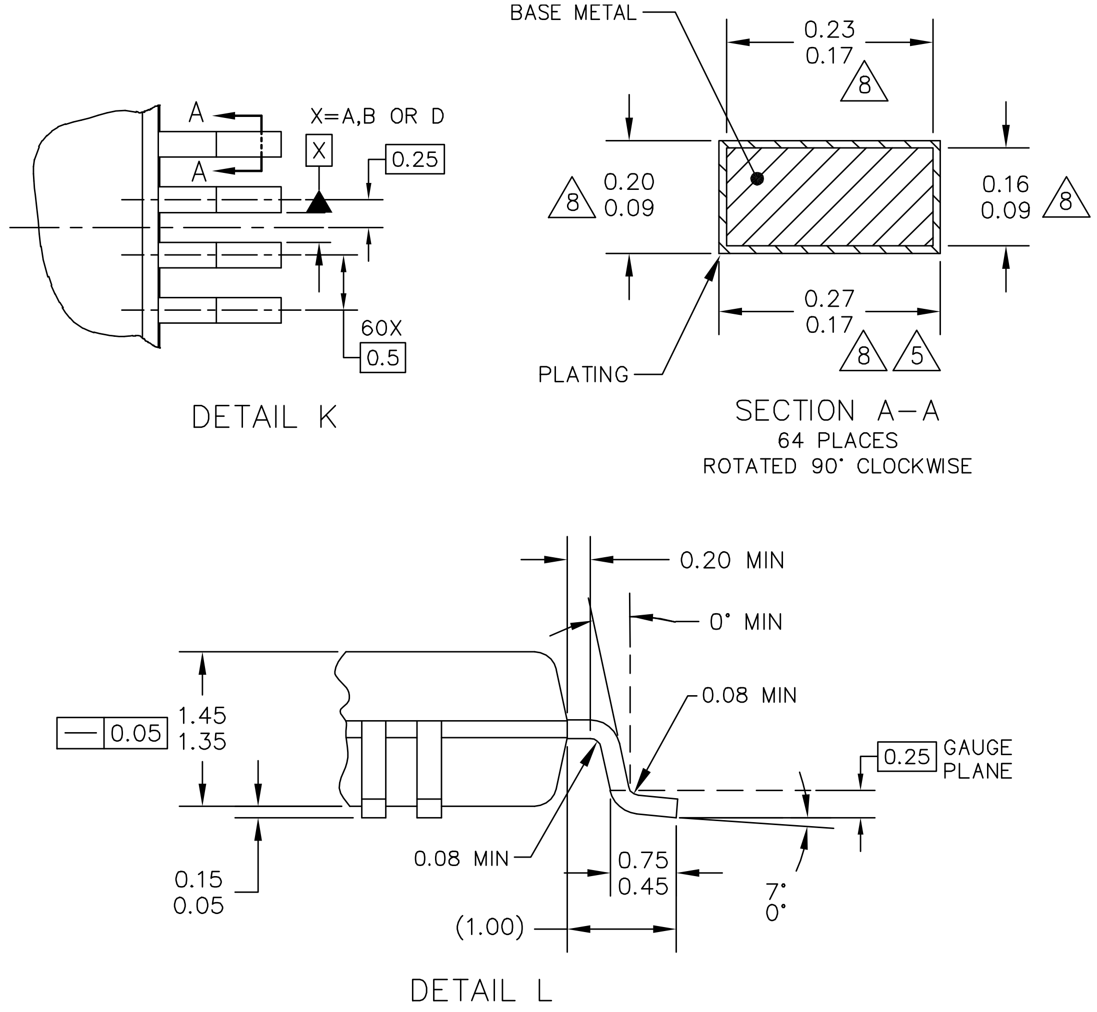
© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED		MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE:	LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D	REV: E
		STANDARD: JEDEC MS-026 BCD	
		SOT1510-2	29 JUN 2018

Figure 48. Package outline



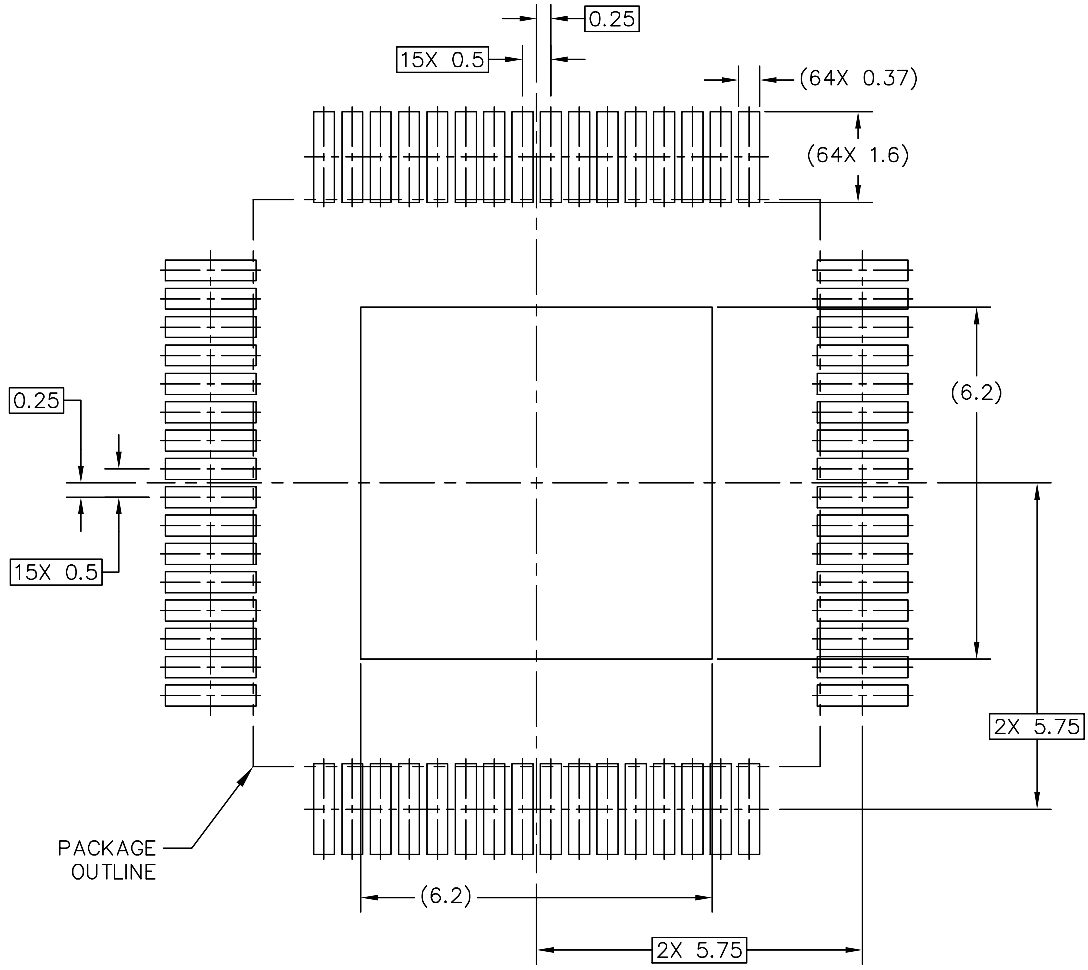
© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D	REV: E
	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2	29 JUN 2018

Figure 49. Package outline



© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D REV: E	
	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2 29 JUN 2018	

Figure 50. Package outline

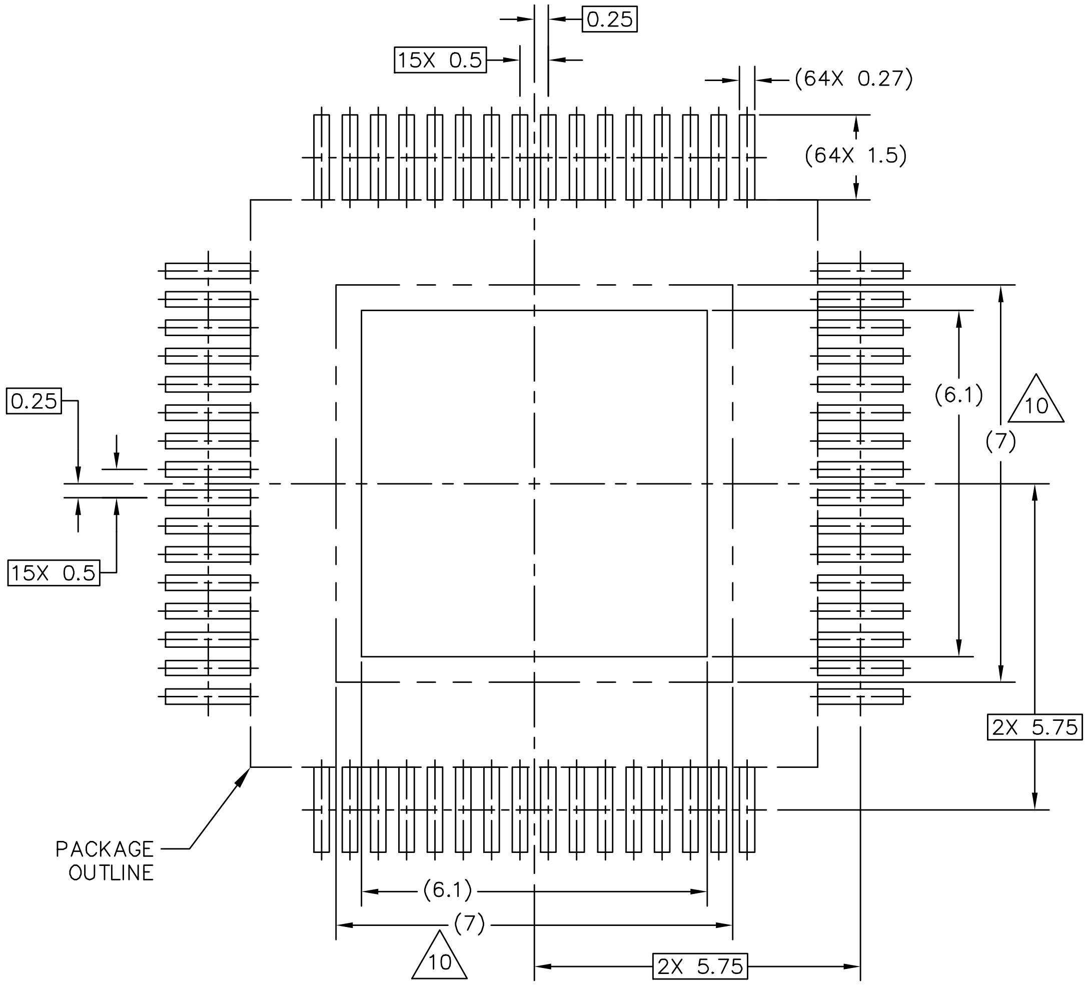


PCB DESIGN GUIDELINES — SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D	REV: E
	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2	29 JUN 2018

Figure 51. Package outline

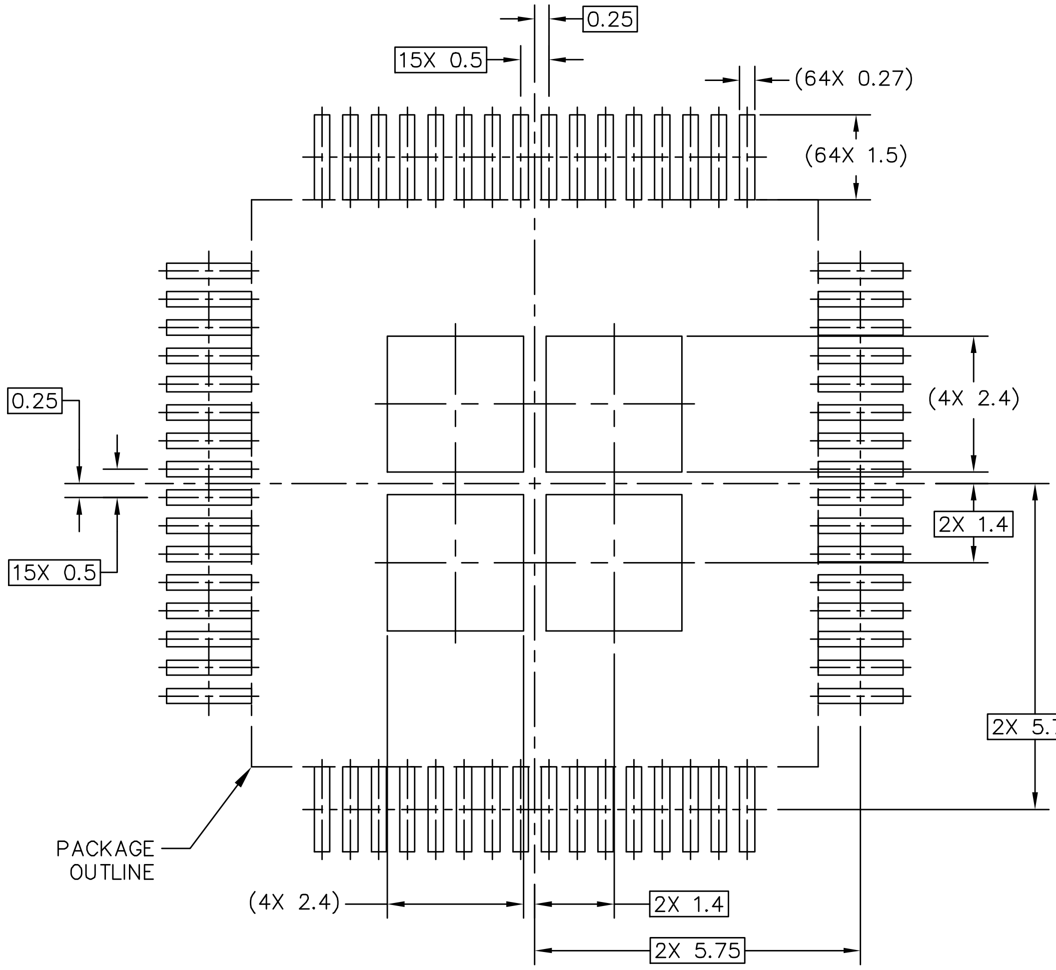


PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D	REV: E
	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2	29 JUN 2018

Figure 52. Package outline



STENCIL THICKNESS 0.125 OR 0.150

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D	REV: E
	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2	29 JUN 2018

Figure 53. Package outline

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.
9. HATCHED AREA REPRESENTS POSSIBLE MOLD FLASH ON EXPOSED PAD.
10. KEEP OUT ZONE REPRESENTS AREA ON PCB THAT MUST NOT HAVE ANY EXPOSED METAL (EG. TRACE/VIA) FOR PCB ROUTING DUE TO THE POSSIBILITY OF SHORTING TO TIE BAR/EXPOSED PAD.

© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D	REV: E
	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2	29 JUN 2018

Figure 54. Package outline

14 Revision history

Table 89. Revision history

Document ID	Release date	Description
BMI7014 v.3	08 August 2024	• Product data sheet. • Supersedes BMI7014 v.2. • Updated status from confidential to public. • Updated Legal information
BMI7014 v.2	20 May 2024	• Product data sheet. • Supersedes BMI7014 v.1. • Global editing for grammar and style. • Section 14 updated to conform with NXP's document appearance standards and content hierarchy. • Table 1: Add row to Code "y". • Table 2: Added row "BMI7014TA2AE". • Table 7 – Added "BMI7014TA1", and second SPI mode line, "BMI7014 TA2", for "$I_{VPWR(SS)}$" – Added rows for "$V_{ERR33rt\_1\_BMI7014TA1}$", "$V_{ERR\_1\_BMI7014TA2}$", "$V_{ERR\_2\_BMI7014TA2}$" – Changed "$V_{RDTX\ INTH}$" to "$V_{RDTX\ INTH\_TA1}$" – Added row for "$V_{RDTX\ INTH\_TA2}$" • Removed section titled "Contact information".
BMI7014 v.1	20 February 2024	Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents