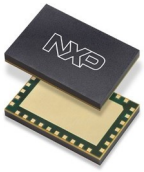
A5M26SG240

Airfast Power Amplifier Module with Autobias Control

Rev. 1 — 8 November 2024 Product data sheet



1 General description

The A5M26SG240 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field-proven LDMOS and GaN power amplifiers are designed for TDD LTE and 5G systems. The module includes an autobias feature that automatically sets the transistor bias upon power up and an integrated sensor that monitors the temperature. Communications to the module can be accomplished via either I^2C or SPI.

2 Features and benefits

- 2-stage module solution that includes an LDMOS integrated circuit as a driver and a GaN final stage amplifier
- Advanced high performance in-package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity digital linearization systems
- Reduced memory effects for improved linearized error vector magnitude
- Autobias on power up
- Temperature sensing
- Digital interface (I^2C or SPI)
- Embedded registers and DACs for setting bias conditions
- Tx enable control pin for TDD operation

3 Typical LTE performance

Table 1. 2496–2690 MHz — Typical LTE performance

P_{out} = 8.9 W Avg., V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc, 1 × 20 MHz LTE, input signal PAR = 8 dB @ 0.01 % probability on CCDF.[1]

Carrier center frequency	Gain (dB)	ACPR (dBc)	PAE (%)
2506 MHz	34.6	-32.2	46.5
2600 MHz	35.2	-32.6	47.7
2680 MHz	35.5	-29.7	47.0

[1] All data measured with device soldered to NXP reference circuit.

4 Functional block diagram

4.1 Functional block diagram

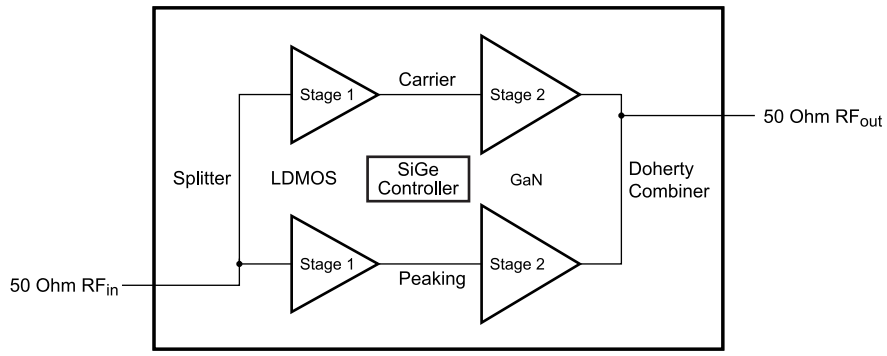


Figure 1. Functional block diagram

5 Pinning information

5.1 Pinning

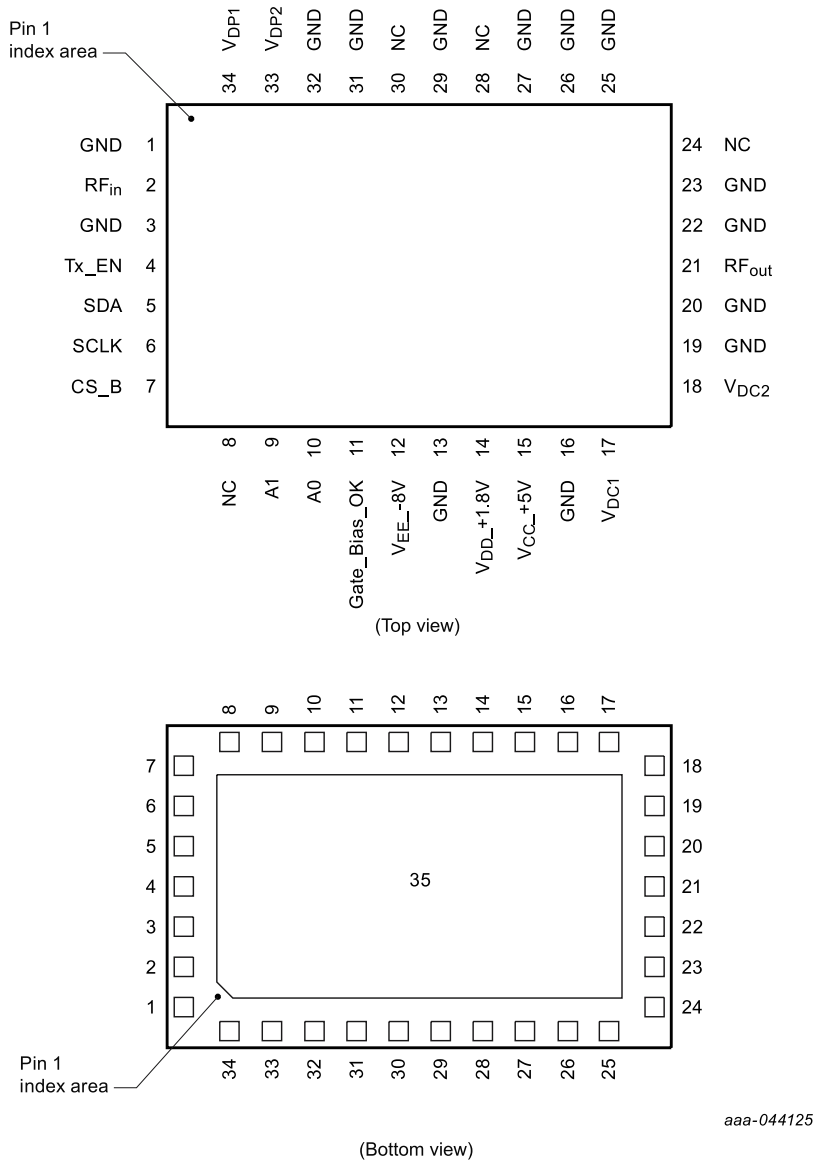


Figure 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Pin number	Pin function	Pin description
1, 3, 13, 16, 19, 20, 22, 23, 25, 26, 27, 29, 31, 32, 35	GND	Ground
2	RF_{in}	RF input signal @ 50 ohms
4	Tx_EN	PA enable signal (1.8 V JEDEC compatible)
5	SDA	SPI/I^2C serial data signal (1.8 V JEDEC compatible)
6	SCLK	SPI/I^2C serial clock signal (1.8 V JEDEC compatible)
7	CS_B	Chip selection bar. Can be tied to GND when strictly following I^2C protocol.
8, 24, 28, 30	NC	No connection
9	A1	I^2C address A1 (tri-state, tie to 1.8 V, tie to ground or leave floating)
10	A0	I^2C address A0 (tri-state, tie to 1.8 V, tie to ground or leave floating)
11	Gate_Bias_OK	Gate bias OK (1.8 V JEDEC compatible) (Indicates gate voltage is present and drain voltage can now be applied.)
12	V_{EE}_-8V	Maximum -8 V power source for autobias controller
14	V_{DD}_+1.8V	1.8 V power source for autobias controller (No connection needed externally. The module generates 1.8 V internally for autobias controller.)
15	V_{CC}_+5V	5 V V_{CC} power source for autobias controller
17	V_{DC1}	Carrier LDMOS driver drain supply, stage 1
18	V_{DC2}	Carrier GaN drain supply, stage 2 (No connection needed externally. V_{DC2} is internally connected to V_{DP2}.)
21	RF_{out}	RF output signal @ 50 ohms
33	V_{DP2}	Peaking GaN drain supply, stage 2
34	V_{DP1}	Peaking LDMOS driver drain supply, stage 1

6 Ordering information

Table 3. Ordering information

Device	Tape and reel information	Package
A5M26SG240T2	T2 suffix = 2,000 units, 24 mm tape width, 13-inch reel	12 mm × 8 mm Module

7 Product marking

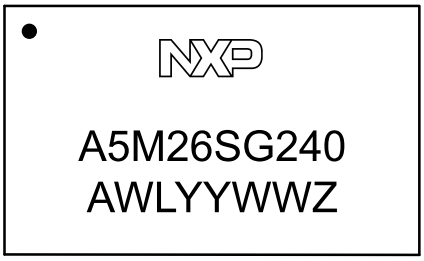


Figure 3. Product marking

Table 4. Product marking trace code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

8 Electrical characteristics

8.1 Ratings

8.1.1 Limiting values

Table 5. Limiting values

Symbol	Parameter	Conditions	Value	Unit
$V_{CC\_}$ +5V $V_{EE\_}$ -8V	Gate-bias voltage range		4.75 to 5.25 -8.4, -7.6	Vdc
$V_{CC\_}$+5V_SLEW	5 V_{CC} slew rate	T_C = 25 °C	< 9.5	ms
V_{DC1}, V_{DP1} V_{DC2}, V_{DP2}	Operating voltage range		4.75 to 5.25 38 to 55	Vdc
CS_B, SDA, SCLK, Tx_EN, A1, A0	Operating voltage range		1.65 to 1.95	Vdc
T_{stg}	Storage temperature range		-65 to +150	°C
T_{CH}	Maximum channel temperature		225	°C
P_{in}	Peak input power	2600 MHz, pulsed CW, 10 µsec(on), 10 % duty cycle	24	dBm

8.1.2 Lifetime

Table 6. Lifetime

Symbol	Parameter	Conditions	Value	Unit
MTTF	Mean time to failure	Case temperature 125 °C, internal sense temperature 109 °C, 8.9 W Avg., V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc[1]	> 10	Years

[1] All data measured with device soldered to NXP reference circuit.

8.1.3 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta SC}$ (IR)	Thermal resistance by infrared measurement, active die surface-to-case	Case temperature 116 °C, $P_{D\text{-}Global}$ = 10.5 W	4.9[1]	°C/W
$R_{\theta CHC}$ (FEA)	Thermal resistance by finite element analysis, channel-to-case	Case temperature 123 °C, P_D = 10.0 W	10.0[2]	°C/W

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to https://www.nxp.com/RF and search for AN1955.
[2] $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, A = -12.5 and B = 9729.

8.1.4 ESD protection characteristics

Table 8. ESD protection characteristics

Test methodology	Class
Human Body Model (per JS-001-2023)	2
Charge Device Model (per JS-002-2022)	C3

8.1.5 Moisture sensitivity level

Table 9. Moisture sensitivity level

Test methodology	Rating	Package peak temperature	Unit
Per JESD22-A113, EIA/IPC/JEDEC J-STD-020/JEDEC J-STD-075A	3/R6	250	°C

8.2 Operating characteristics

8.2.1 Typical I_{DQ} currents

Table 10. Typical I_{DQ} currents

(T_A = 25 °C unless otherwise noted)[1]

Symbol	Parameter	Conditions	Typ	Unit
I_{DQC1}	LDMOS_VGC1_DAC Gate Quiescent	V_{DC1} = 5 Vdc, LDMOS_SENSE_DAC = 32	100	mA
I_{DQP1}	LDMOS_VGP1_DAC Gate Quiescent	V_{DP1} = 5 Vdc, LDMOS_SENSE_DAC = 32	42	mA
I_{DQC2}	GaN_VGC2_DAC Gate Quiescent	V_{DC2} = 48 Vdc, GaN_SENSE_DAC = 18	60	mA
I_{DQP2}	GaN_VGP2_DAC Gate Quiescent[2]	V_{DP2} = 48 Vdc, GaN_SENSE_DAC = 18	0	mA

[1] One-time programmable registers are set at final test to meet typical I_{DQ} values for each stage on power up. DACs are programmable in Engineering Mode. Each stage of device is measured separately.
[2] Set GaN_VGP2_DAC until I_{DQP2} = 30 mA current is attained, and then subtract 101 DAC steps.

8.2.2 Functional tests

Table 11. Functional tests — 2506 MHz

(In NXP Doherty production ATE[1] test fixture, T_A = 25 °C unless otherwise noted, 50 ohm system)[2] V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc, nominal DAC settings[3], Tx_EN = High, P_{out} = 8.9 W Avg., LTE-FDD 20 MHz, 7.5 dB PAR, f = 2506 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G	Gain		33.0	34.6	-	dB
η_D	Drain efficiency		41.0	45.7	-	%
P_{sat}	Saturated power[4]	Pulsed CW, 5 % duty cycle	47.2	48.2	-	dBm
ACPR	Adjacent channel power ratio		-	-32.7	-27.0	dBc

[1] ATE is a socketed test environment.
[2] Part input and output matched to 50 ohms.
[3] Nominal DAC setting is burnt during the OTP process to match the I_{DQ} values in Table 10, Typical I_{DQ} currents.
[4] P_{sat} is defined at P6dB compression point.

Table 12. Functional tests — 2680 MHz

(In NXP Doherty production ATE[1] test fixture, T_A = 25 °C unless otherwise noted, 50 ohm system)[2] V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc, nominal DAC settings[3], Tx_EN = High, P_{out} = 8.9 W Avg., LTE-FDD 20 MHz, 7.5 dB PAR, f = 2680 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G	Gain		34.0	35.4	-	dB
η_D	Drain efficiency		40.0	45.6	-	%
P_{sat}	Saturated power[4]	Pulsed CW, 5 % duty cycle	47.8	48.8	-	dBm
ACPR	Adjacent channel power ratio		-	-29.8	-24.0	dBc

[1] ATE is a socketed test environment.
[2] Part input and output matched to 50 ohms.
[3] Nominal DAC setting is burnt during the OTP process to match the I_{DQ} values in Table 10, Typical I_{DQ} currents.
[4] P_{sat} is defined at P6dB compression point.

8.2.3 Wideband ruggedness

Table 13. Wideband ruggedness

(In NXP Doherty power amplifier module reference circuit, T_A = 25 °C unless otherwise noted, 50 ohm system)[1] nominal DAC settings, Tx_EN = High, f = 2600 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR.

Characteristic	Test results
ISBW of 400 MHz at 55 Vdc, 3 dB input overdrive from 8.9 W Avg. modulated output power	No device degradation

[1] All data measured with device soldered to NXP reference circuit.

8.2.4 Typical performance

Table 14. Typical performance

(In NXP Doherty power amplifier module reference circuit, T_A = 25 °C unless otherwise noted, 50 ohm system)[1]
V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc, nominal DAC settings, Tx_EN = High, f = 2600 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBW_{res}	VBW resonance[2]	2-tone, 1 MHz tone spacing	-	> 300	-	MHz
1-carrier 20 MHz LTE, 8 dB input signal PAR						
G	Gain		-	35.2	-	dB
PAE	Power added efficiency		-	47.7	-	%
ACPR	Adjacent channel power ratio		-	-32.6	-	dBc
ALT1	Adjacent channel power ratio		-	-44.2	-	dBc
ALT2	Adjacent channel power ratio		-	-49.4	-	dBc
G_F	Gain flatness[3]		-	0.9	-	dB
Pulsed CW, 10 % duty cycle						
P_{sat}	Saturated power[4]		-	48.7	-	dBm
Φ	AM/PM @ saturated power[4]		-	-19	-	°
ΔG	Gain variation @ Avg. power over temperature	-40 °C to +105 °C	-	0.039	-	dB/°C
ΔP_{sat}	Output power variation @ saturated power over temperature[4]	-40 °C to +105 °C	-	0.003	-	dB/°C

[1] All data measured with device soldered to NXP reference circuit.
[2] IMD third order inflection point.
[3] Gain flatness = Max(G(f_{Low} to f_{High})) - Min(G(f_{Low} to f_{High})).
[4] P_{sat} is defined at P6dB compression point.

9 Register map and OTP memory

9.1 One-time programmable memory

The A5M26SG240 contains a one-time programmable (OTP) memory array that is used to store and recall register values for the integrated autobias controller at power up or reset. The data sheet I_{DQ} target values from Table 10 are programmed into the OTP memory during NXP's production testing. These values can be overwritten using the Engineering Mode (EM) sequence; however, the overwritten values do not persist after a power cycle or a reset.

The OTP memory can be programmed only by NXP during the manufacturing process and cannot be changed by the user. The values in OTP memory have been selected to allow the device to operate in a wide variety of applications.

9.2 Register map

There are nine 8-bit user accessible registers available in the A5M26SG240. The register mapping is listed in Table 15. Address 0 RW register is designed to control soft reset, refresh OTP and read the chip version. Address 1−6 registers are RW and/or OTP controlled and provide settings for the two RF transistor group DACs. Address 15 is read only for temperature sense functionality. Address 17 is a virtual write only register for enabling Engineering Mode.

Table 15. Register map

Address (in decimal)	Register attribute	Register name	Register definition								Default value
			bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
0	RW	System_Reg	N/A	Soft reset	Refresh OTP	N/A	Chip version [3:0] (Read only)				8'b0000_0001
1	OTP COPY (RW)	LDMOS_Sense_DAC	Reserved		LDMOS sense DAC						OTP value
2	OTP COPY (RW)	LDMOS_VGC1_DAC	LDMOS V_{GC1} DAC								OTP value
3	OTP COPY (RW)	LDMOS_VGP1_DAC	LDMOS V_{GP1} DAC								OTP value
4	OTP COPY (RW)	GaN_Sense_DAC	Reserved		GaN sense DAC						OTP value
5	OTP COPY (RW)	GaN_VGC2_DAC	GaN V_{GC2} DAC								OTP value
6	OTP COPY (RW)	GaN_VGP2_DAC	GaN V_{GP2} DAC								OTP value
7	RO	Device_ID	Final GaN stage nominal drain voltage = 48 V [7:2]						Device version [1:0]		8'b11000000
8–14	-	-	Reserved								-
15	RO	Temp_ADC	Temperature sensor [7:0]								-
16	-	-	Reserved								-
17	Virtual W only	EM_Passcode	Engineering Mode (EM) passcode 8'hE3								-

Read Only register (RO)
Read Write register (RW)
Read Write register with OTP overwrite at Startup (RW)
Reserved non-accessible register
Write Only register

Table 16. Register overview and bit description

Address	Register name	Bit	Bit descriptions	Power on/reset value[1]	Overwritten by OTP	Attribute	EM mode
0	System_Reg	7	Not available	N/A	N/A	N/A	N/A
		6	Soft Reset. A 1 written to this register will perform a reset of all registers to their default values. A 0 should be written after the reset operation is completed.	0	No	RW	
		5	Refresh OTP. A 1 written to this register will overwrite current DAC values with those stored in OTP into registers identified in the "Overwritten by OTP" column. A 0 should be written after the reset operation is completed.	0	No		
		4	Not available	N/A	N/A	N/A	
		0–3	Chip version bits. Inserted by NXP to provide revision information. Cannot be changed.	N/A	No	R	
1	LDMOS_Sense_DAC	6–7	Not available	N/A	N/A	N/A	
		0–5	LDMOS_Sense_DAC 6-bit logic value for LDMOS driver stage amplifiers. LDMOS_Sense_DAC sets the reference voltage to compare to the V_{DS} across the reference device. Optimal value set by NXP. Adjustment by end user to the optimal setting is not recommended.	8'h20	Yes	RW[2]	Yes
2	LDMOS_VGC1_DAC	0–7	Sets 8-bit DAC logic value for carrier amplifier driver stage. 8'h00 sets gate to equal ceiling voltage. 8'hFF reduces gate voltage by a max value.	8'h80			
3	LDMOS_VGP1_DAC	0–7	Sets 8-bit DAC logic value for peaking amplifier driver stage. 8'h00 sets gate to equal ceiling voltage. 8'hFF reduces gate voltage by a max value.	8'h80			

[1] At power on or reset, OTP values set by NXP are automatically loaded into registers indicated with a “Yes” in the “Overwritten by OTP” column. For these registers, values shown in the “Power On/Reset Value” column will be loaded only if OTP has not been programmed to prevent damage to the device.
[2] Register can be read at any time. Can write to register only when in Engineering Mode (EM).

(continued)

Table 16. Register overview and bit description...*continued*

Address	Register name	Bit	Bit descriptions	Power on/reset value[1]	Overwritten by OTP	Attribute	EM mode
4	GaN_Sense_DAC	6–7	Not available	N/A	N/A	N/A	No
		0–5	GaN_Sense_DAC 6-bit logic value for GaN final stage amplifiers. GaN_Sense_DAC sets the reference voltage to compare to the V_{DS} across the reference device. Optimal value set by NXP. Adjustment by end user to the optimal setting is not recommended.	8'h20	Yes	RW[2]	Yes
5	GaN_VGC2_DAC	0–7	Sets 8-bit DAC logic value for carrier final stage. 8'hFF sets gate to equal ceiling voltage. 8'h00 reduces gate voltage by a max value.	8'h80			
6	GaN_VGP2_DAC	0–7	Sets 8-bit DAC logic value for peaking final stage. 8'hFF sets gate to equal ceiling voltage. 8'h00 reduces gate voltage by a max value.	8'h80			
7	Device ID	7–2	Final stage GaN nominal drain voltage for both carrier and peaking sides = 48 V.		N/A	R	No
		0–1	Device version ID		N/A	R	No
8–14	Reserved	N/A	Not available	N/A	N/A	N/A	No
15	Temp_ADC	0–7	Temperature sensor 8-bit DAC value. 8'h00 is lowest temperature, 8'hFF is highest temperature.	8'h00	No	R	No
16	Reserved	N/A	Not available	N/A	N/A	N/A	No
17	EM_Passcode	0–7	Engineering Mode (EM). By writing 8'hE3 to this register the user can enter Engineering Mode. EM can be cleared by writing any other code to this register. When in Engineering Mode, the registers identified in “EM mode” column can be changed.	N/A	No	W	Yes

[1] At power on or reset, OTP values set by NXP are automatically loaded into registers indicated with a “Yes” in the “Overwritten by OTP” column. For these registers, values shown in the “Power On/Reset Value” column will be loaded only if OTP has not been programmed to prevent damage to the device.

[2] Register can be read at any time. Can write to register only when in Engineering Mode (EM).

10 Power supply sequence

Power up sequence

1. V_{EE}_-8V: -8 V power up
2. V_{CC}_+5V: 5 V, V_{DP1}, V_{DC1}: 5 V power up. Note: V_{CC}_+5V needs to reach steady state within 9.5 ms.
3. Gate_Bias_OK should return 1.8 V as this indicates SPI/I^2C interface is active.
4. V_{DP2}, V_{DC2}: 48 V power up
5. Tx_EN: 1.8 V power up
6. DUT is now biased and ready for RF measurements.

Power down sequence

1. Tx_EN: 1.8 V power down
2. V_{DP2}, V_{DC2}: 48 V power down
3. SPI/I^2C interface deactivated
4. V_{DP1}, V_{DC1}: 5 V, V_{CC}_+5V: 5 V power down
5. V_{EE}_-8V: -8 V power down

Note: All digital interfaces (SDA, SCLK, CS_B, Tx_EN, A0, A1) are 1.8 V logic.

11 Autobias functionality

11.1 General overview

After power up, the integrated bias controller develops and applies a quiescent bias voltage to the gate of each of the RF transistors contained within the power amplifier module (PAM) based on the preset OTP values. The standard SPI or I^2C interface can be used to read the temperature sensor and overwrite preset DAC values. The device can be used without the programming interface at initial power up; however, additional compensation for the GaN FETs over temperature is recommended to achieve optimal performance. The thermal compensation circuit is analog and not programmable; however, the preset DAC values for the four V_{GS} DACs can be overwritten to provide an additional thermal compensation scheme via the SPI or I^2C interface. This section describes the operation and programming of the bias controller.

11.2 Operational overview

11.2.1 LDMOS driver stage autobias operation

Figure 4 shows a detailed view of the driver stage autobias controller. The driver stage on both the carrier side and peaking side is an RF LDMOS field-effect transistor (FET). Each die for the carrier and peaking driver stage also contains a small periphery reference FET that is designed to match the properties of the larger RF transistors with regard to part-to-part process and temperature-dependent variations. The bias controller interfaces with each of the RF FETs and provides flexibility to control the biasing of the driver stage transistor groups independently.

The bias controller operates by establishing a known current through each reference FET. This in turn establishes a gate-source operating voltage by sensing the voltage drop across an integrated, high tolerance resistor placed between V_{CC} (5 V) and the reference device drain terminal. The bias controller V_{CC}_+5V pin should be operated from a 5 V supply with a tolerance of ±5 %. The reference voltage across the precision resistor R1 is compared to a voltage programmed in the bias controller (LDMOS_Sense_DAC), thereby providing fine incremental adjustment to the default bias current of the reference FET. Because the reference FET and RF FET are manufactured on the same die in close proximity, they exhibit similar process and temperature dependencies.

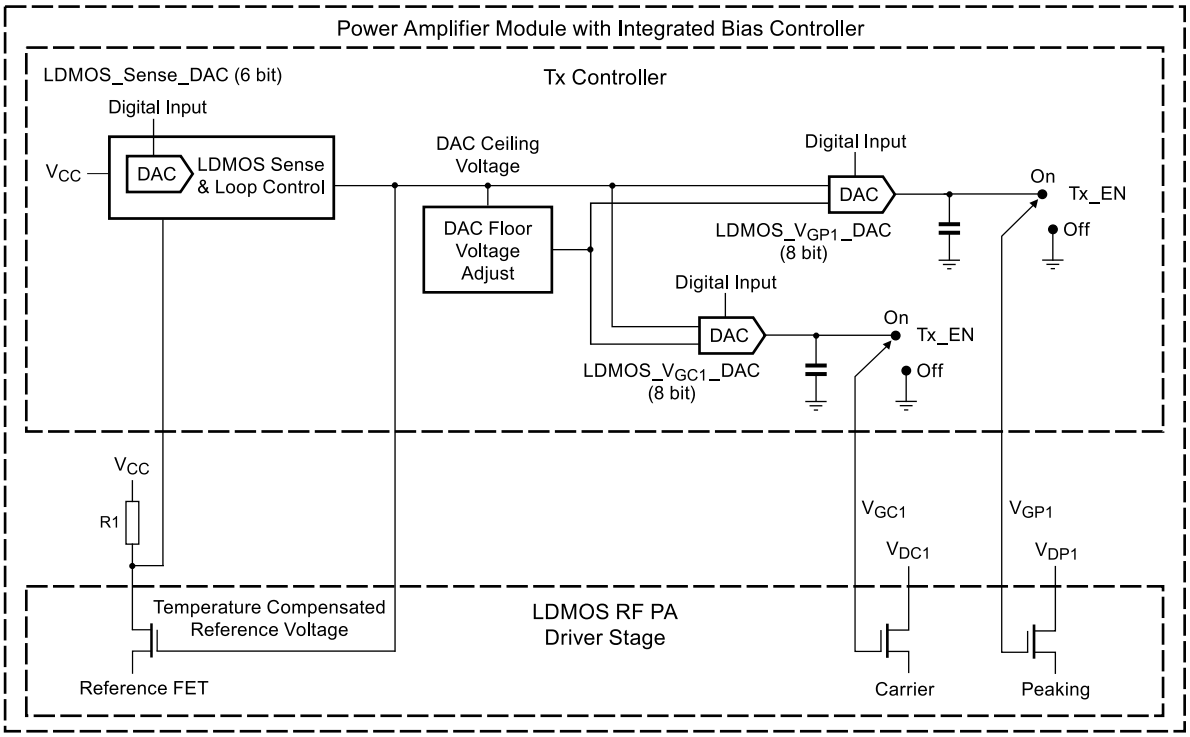


Figure 4. Block diagram of LDMOS driver autobias functionality

The initial bias condition is set via the LDMOS_Sense_DAC register. The bias condition is then sensed and adjusted as temperature changes via the closed-loop feedback. The feedback mechanism adjusts the DAC ceiling voltage to maintain a constant I_{DS} current through the reference FET. The temperature compensated DAC ceiling voltage can either be passed to the carrier PA driver and peaking PA driver directly, or reduced by values set in the LDMOS_VGC1_DAC and LDMOS_VGP1_DAC to the DAC floor voltage.

11.2.2 GaN final stage autobias operation

Figure 5 shows a detailed view of the final stage autobias controller. The final stage on both the carrier side and the peaking side are RF GaN FETs. Each die for the carrier and peaking final stage also contains a small periphery reference FET that is designed to match the properties of the larger RF transistors with regard to part-to-part process and temperature-dependent variations. The bias controller interfaces with each of the RF FETs and provides flexibility to control the biasing of the final stage transistors independently.

The bias controller operates by establishing a known current through the reference FET. This in turn establishes a gate-source operating voltage by sensing the voltage drop across an integrated, high tolerance resistor on the reference device drain terminal. The bias controller V_{CC}_+5V pin should be operated from a 5 V supply with tolerance of ±5 %. The bias controller V_{EE}_-8V pin should be operated from a -8 V supply with tolerance of ±5 %. The reference voltage across the precision resistor R1 is compared to a voltage programmed in the bias controller (GaN_Sense_DAC), thereby providing fine incremental adjustment to the default bias current of the reference FET. Because the reference FET and RF FET are manufactured on the same die in close proximity, they exhibit similar process and temperature dependencies. Additional compensation is recommended for the GaN FETs over temperature to achieve optimal performance.

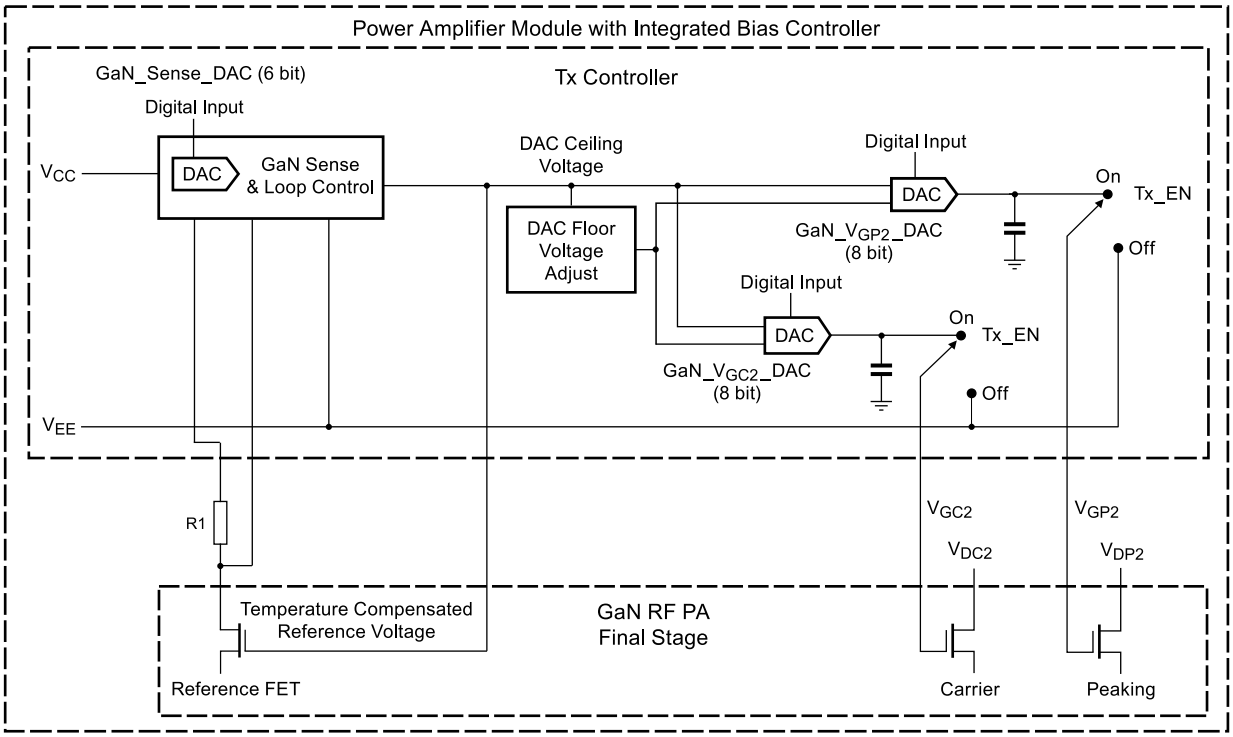


Figure 5. Block diagram of GaN final stage autobias functionality

11.3 Tx enable control

A 1.8 V JEDEC compliant enable signal (Tx_EN) is included for bias control to support TDD operation. The controller provides capability to quickly switch the RF FETs between ON and OFF modes in less than 100 ns. With Tx_EN in an ON state, the RF FET gate terminals are internally decoupled with sufficient capacitance providing a low impedance for wide baseband signals. The large capacitance also serves as a charge holding cap for reducing switching transient time in TDD operation. In Tx OFF mode, LDMOS RF FET device gates are grounded and GaN RF FETs are tied to -8 V, effectively shutting them OFF.

Table 17. TX_EN off-state typical currents

Characteristic	Typical value	Unit
$V_{CC\_}$+5V supply current	35–38	mA
$V_{EE\_}$-8V supply current (with $V_{CC\_}$+5V supply ON)	9–11	mA

11.4 Sense_DAC

The current in the reference FET is controlled and programmed with 6 bits (two MSBs of the 8-bit register are not used) via the sense DAC (LDMOS_Sense_DAC and GaN_Sense_DAC). By programming the sense DAC, the RF stage DAC ceiling voltage reference operating point can be optimally set. The DAC ceiling voltage reference point impacts both RF PA stages simultaneously for each group. After OTP has been programmed, the Sense_DAC is loaded with the programmed values and should not be adjusted in Engineering Mode.

The factory programmed values for LDMOS_Sense_DAC and GaN_Sense_DAC are decimal 32 and 18 respectively. These values have been optimized for best power, linearity and efficiency tradeoffs.

11.5 VGS_DAC

The VGS_DAC voltage is determined via the Sense_DAC setting, creating the top end or ceiling of the VGS_DAC voltage range and a fixed offset voltage creating the bottom end or floor of the VGS_DAC voltage range. With a decimal VGS_DAC setting of 0, the gate voltage developed on the reference FET is buffered with minimum offset to the gates of the RF transistors in the carrier amplifier. As the LDMOS VGS_DAC value increases, the voltage applied to the gates of the driver stage RF transistors decreases, which reduces I_{DQ}. As the GaN VGS_DAC value increases, the voltage applied to the gates of the final stage RF transistors increases, which increases I_{DQ}. This allows the operating point of the four RF devices to be set to any desired value, from Class AB to Class C.

The reference FETs and RF FETs exhibit approximately the same current density (that is, I_{DQ}/mm gate width). It is important to note that, because the reference device and RF transistors are manufactured on the same die in close proximity, they exhibit similar process and temperature dependencies. Both the driver amplifiers and the final amplifiers operate in the same way with regard to the reference device and the RF transistors.

11.6 Engineering Mode (EM)

Flexibility exists to overwrite the OTP memory values. A special Engineering Mode (EM) is available to allow the user to overwrite data that has been placed into the OTP memory space. To enter EM, issue the write address d’17 command with the predefined EM passcode (see Table 15). After entering EM, all DAC OTP registers (address 1–6) can be overwritten with the normal I^2C/SPI write instruction. This interface programmed value will be valid so long as the V_{CC} supply power is maintained. The V_{CC} power cycle will load OTP programmed DAC settings again. If the user writes the address d’17 register with any value other than the passcode, EM will automatically exit.

12 Component layout and parts list

12.1 Component layout

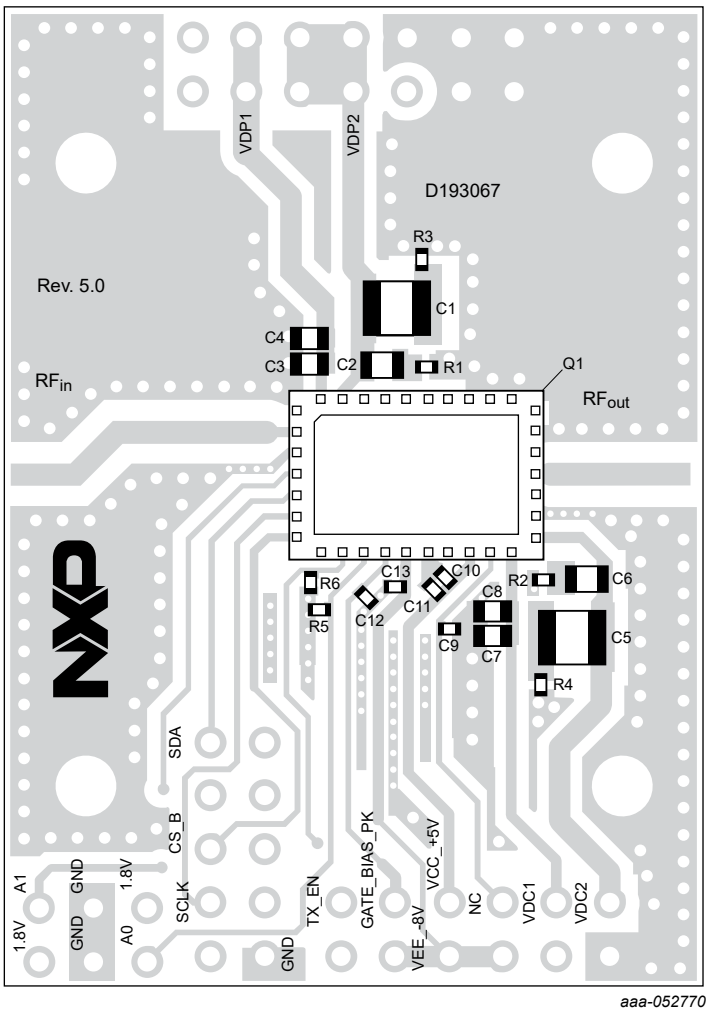


Figure 6. A5M26SG240 reference circuit component layout

12.2 Component designations and values

Table 18. A5M26SG240 reference circuit component designations and values

Part	Description	Part number	Manufacturer
C1, C5	10 µF chip capacitor	GRM32EC72A106KE05L	Murata
C2, C6	1 µF chip capacitor	GRM21BC72A105KE01	Murata
C3, C7, C9, C12	Do not place	-	-
C4, C8	10 µF chip capacitor	GRM188D71A106MA73	Murata
C10	0.01 µF chip capacitor	CGA2B3X7R1H103K050BB	TDK
C11, C13	1 µF chip capacitor	GRM155R61H105KE5D	Murata
Q1	Power amplifier module	A5M26SG240	NXP
R1, R2, R3, R4, R5, R6	0 Ω, 1/10 W chip resistor	ERJ2GE0R00X	Panasonic
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D193067	MTL

13 Temperature sensor

The temperature value is converted from the 8-bit temperature sense ADC value (stored in the Temp_ADC register) via the following preliminary equation. Further measurement and validation of this equation may result in future changes.

T_J in °C = (0.67481 × Temp_ADC) - 45.14529

A plot of this equation is shown in Figure 7.

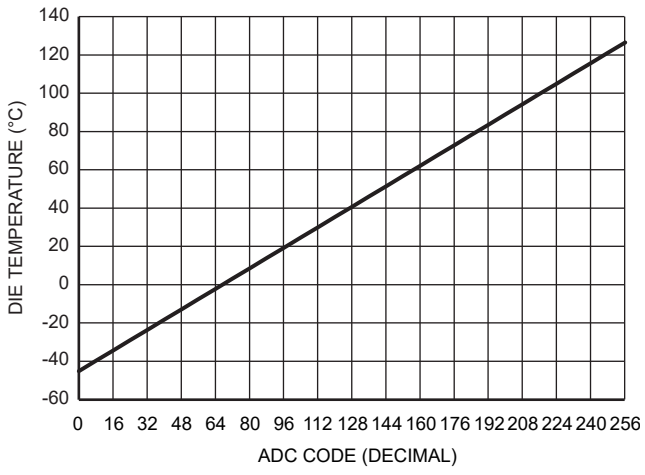


Figure 7. Die temperature versus ADC code

Table 19. Temperature sensor accuracy

Parameter	Conditions	Value	Unit
Operating die temperature	T_J = 25 °C to 85 °C	±3	°C
Operating die temperature	T_J = -35 °C to +125 °C	±5	°C

14 Communication interfaces

The A5M26SG240 device contains a digital interface that supports either a 3-pin SPI or 2-pin I^2C interface. The digital interface is used to both read and write data to and from the device. The preferred interface type can be selected externally by adjusting the A0 and A1 pins.

14.1 SPI

The A5M26SG240 can be programmed and the Tx bias settings and temperature read through the 3-pin SPI interface. To enable SPI mode, pins A0 and A1 must be connected to ground (see Table 21).

14.1.1 SPI timing diagram

The SPI interface timing of A5M26SG240 complies with SPI mode3 as shown in Figure 8.

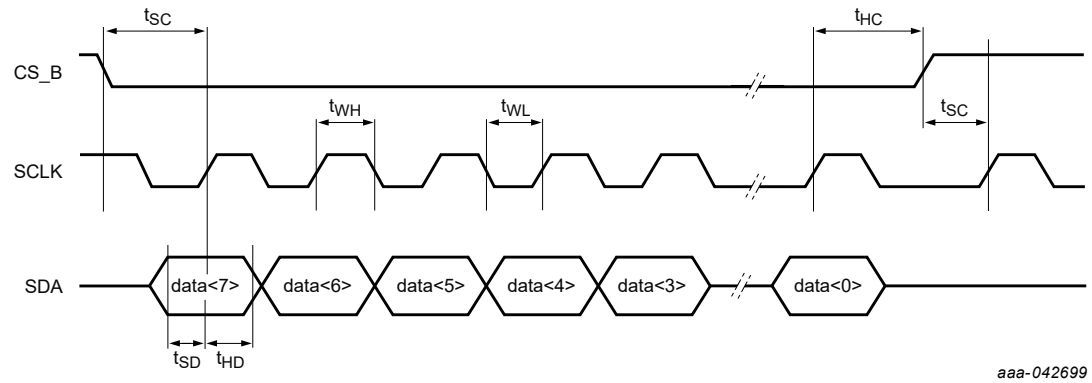


Figure 8. Serial interface timing diagram

Table 20. Serial interface timing specification

Symbol	Parameter	Min (ns)
t_{SC}	Setup timing requirement of CS_B (both rising and falling) in relation to the rising edge of SCLK	50
t_{WH}	clk high duration	160
t_{WL}	clk low duration	160
t_{SD}	Date to clock rising edge setup	20
t_{HD}	clk rising edge to data hold time	20
t_{HC}	clk to CS_B hold time	50
$t_{WH} + t_{WL}$	Minimum clock period	400

14.1.2 SPI instruction set definition

The SPI instruction set is determined by the first byte after releasing the CS_B signal. The order of SPI instruction is MSB sent first, LSB sent last. Bit 7 of the SPI instruction set is defined as read (1) or write (0) command. Bits 6−5 define the burst width in the range of 1−4 bytes: 00 is for 1 byte data, 01 for 2 bytes data, 10 for 3 bytes data and 11 is for 4 bytes data. Bits 4−0 are defined as the register address that is to be accessed.

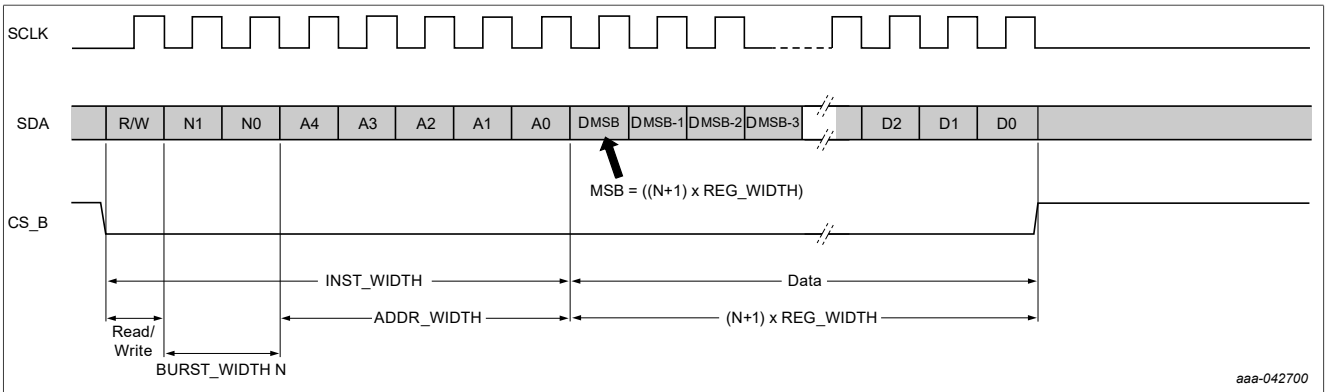


Figure 9. SPI instruction sets diagram

SPI instruction set information:

- R/W read = 1, write = 0
- N1, N0
  - 2'b00 1 byte
  - 2'b01 2 bytes
  - 2'b10 3 bytes
  - 2'b11 4 bytes
- A4, A3, A2, A1, A0 decode for address 0–15
- MSB sent first, LSB last

14.2 I^2C

The A5M26SG240 follows the I^2C protocol standard. It supports I^2C fast mode with a bit rate up to 400 Kbit/s. It also supports I^2C standard mode with bit rate up to 100 Kbit/s.

14.2.1 I^2C addressing

The two external tri-state address pins A0 and A1 use 1.8 V logic levels and are decoded into 7-bit I^2C addresses as shown in Table 21. The three LSBs of the 7-bit address are set via the A0 and A1 pins. The four MSBs are the base address, which is fixed at 1000.

Table 21. I^2C 7-bit address assignment

A1	A0	I^2C 7-bit address
0	0	Disable I^2C (SPI mode)
0	Z	1000 000
0	1	1000 001
Z	0	1000 010
Z	Z	1000 011
Z	1	1000 100
1	0	1000 101
1	Z	1000 110
1	1	1000 111

14.2.2 I²C instruction set

14.2.2.1 I²C Write instruction

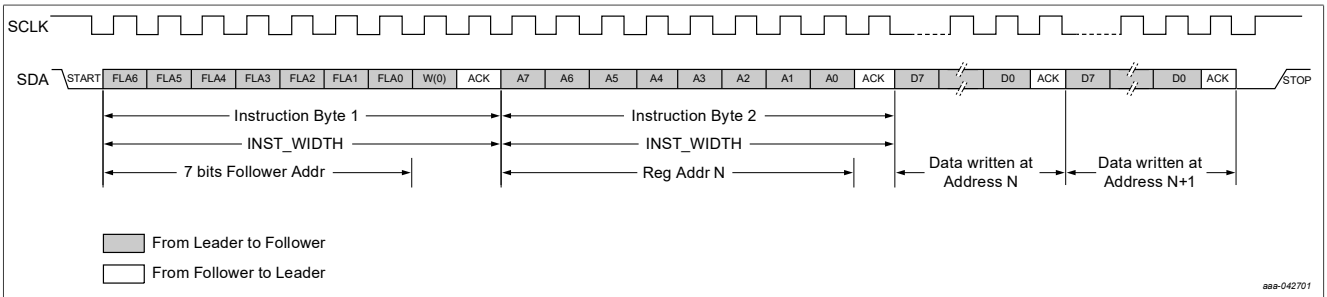


Figure 10. I²C Write instruction

14.2.2.2 I²C Read instruction

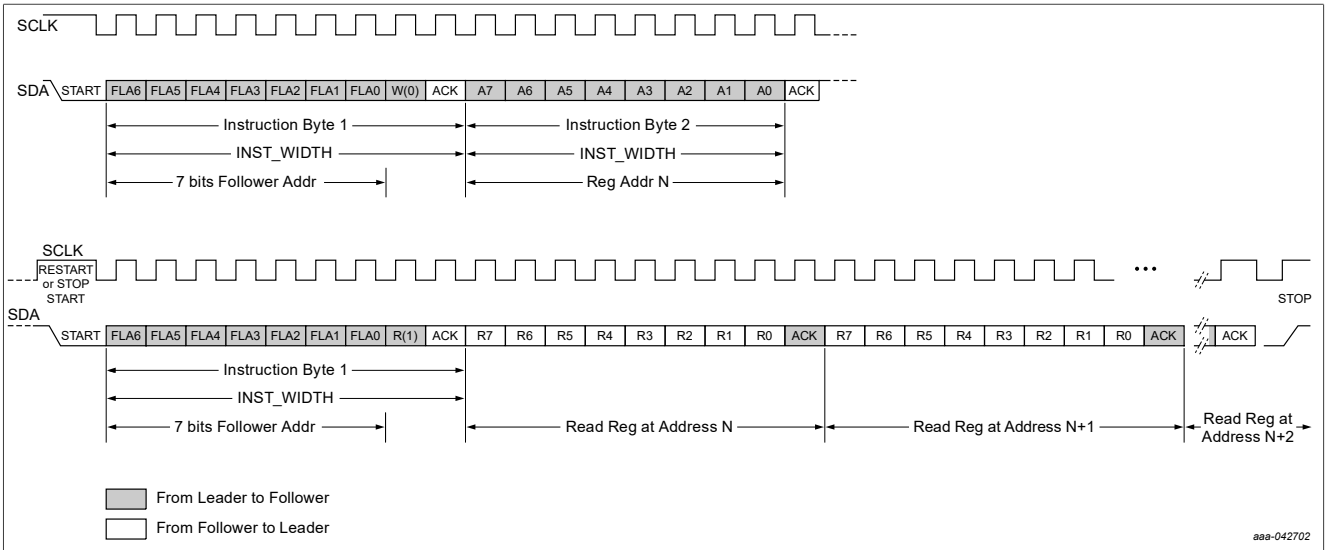


Figure 11. I²C Read instruction

14.2.2.3 I²C Write and Read combination sequence

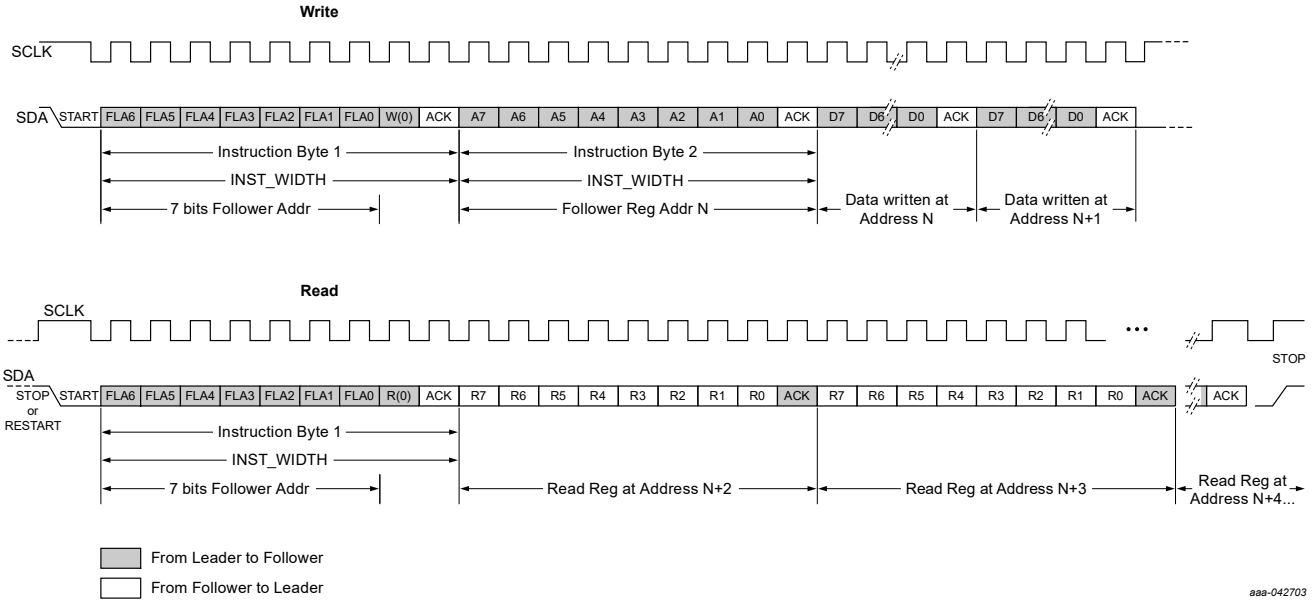


Figure 12. I²C Write and Read combination sequence

14.2.3 I²C Device ID Read instruction

The Device ID is read only, hardwired in the device and can be accessed as follows:

1. START condition
2. The leader sends the Reserved Device ID I²C bus address followed by the R/W bit set to '0' (write): '1111 1000'.
3. The leader sends the I²C bus follower address of the follower device it must identify. The LSB is a "don't care" value. Only one device must acknowledge this byte (the device that has the I²C bus follower address).
4. The leader sends a RESTART condition.

Remark: A STOP condition followed by a START condition resets the follower state machine and the Device ID read cannot be performed. Also, a STOP condition or a RESTART condition followed by an access to another follower device resets the follower state machine and the Device ID read cannot be performed.

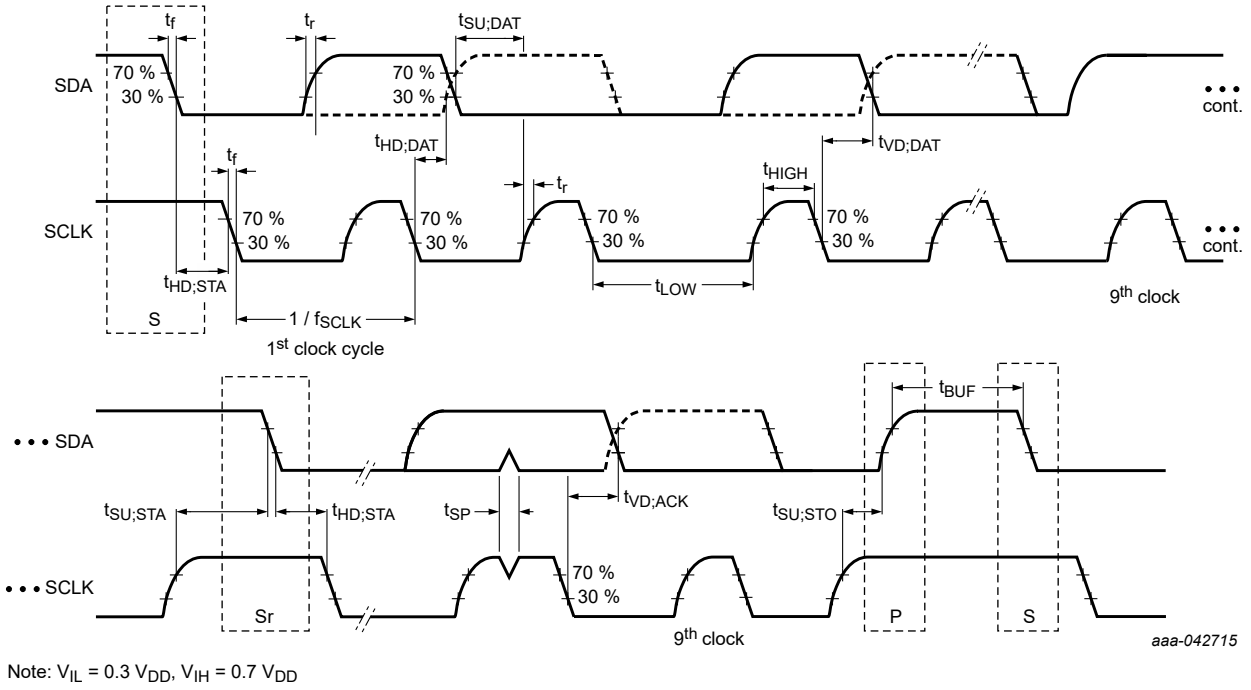
1. The leader sends the Reserved Device ID I²C bus address followed by the R/W bit set to '1' (read): '1111 1001'.
2. The Device ID read can be completed, starting with the 12 manufacturer bits (first byte + four MSBs of the second byte), followed by the nine part identification bits (four LSBs of the second byte + five MSBs of the third byte), and then the three die revision bits (three LSBs of the third byte).
3. The leader ends the reading sequence by NACKing the last byte, thus resetting the follower device state machine and allowing the leader to send the STOP condition.

Remark: The reading of the Device ID can be stopped anytime by sending a NACK.

Table 22. I²C Device Read instructions

Leader to Follower	Leader to Follower	Leader to Follower	Leader to Follower	Leader to Follower	Follower to Leader	Leader to Follower	Leader to Follower
START	1111 1000	XXXXXXX+'0/1'	RESTART	1111 1001	3 bytes ID	NACK	STOP

14.3 I²C electrical specification and timing for I/O stages and bus lines



Note: V_{IL} = 0.3 V_{DD}, V_{IH} = 0.7 V_{DD}

Figure 13. I²C electrical specification and timing for I/O stages and bus lines

14.3.1 I^2C SCLK and SDA characteristics

Table 23. I^2C SCLK and SDA

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCLK}	SCLK clock frequency		0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	After this period, the first clock pulse is generated.	0.6	-	µs
t_{LOW}	Low period of the SCLK clock[1]		1.3	-	µs
t_{HIGH}	High period of the SCLK clock		0.6	-	µs
$t_{SU;STA}$	Setup time for a repeated START condition		0.6	-	µs
$t_{HD;STA}$	Data hold time[2]	BBUS-compatible masters	-	-	µs
		I^2C bus devices	0	-	µs
$t_{SU;STA}$	Data setup time		100[3]	-	µs
t_r	Rise time of both SDA and SCLK signals		20	300	ns
t_f	Fall time of both SDA and SCLK signals[4][5][6]		6.5	300	ns
$t_{SU;STA}$	Setup time for STOP condition		0.6	-	µs
t_{BUF}	Bus free time between a STOP and START condition		1.3	-	µs
$t_{VD;DAT}$	Data valid time[7]		-	0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time[6]		-	0.9	µs

[1] Note: All values referred to $V_{IH(min)}$ (0.3 V_{DD}) and $V_{IL(max)}$ (0.7 V_{DD}) level.
[2] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCLK and applies to data in transmission and the Acknowledge.
[3] A fast mode I^2C bus device can be used in a standard mode I^2C bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCLK signal. If such a device does not stretch the LOW period of the SCLK signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DATA}$ = 1000 + 250 = 1250 ns (according to the Standard Mode I^2C Bus Specification) before the SCLK line is released. Also the Acknowledge timing must meet this setup time.
[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.
[5] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for standard mode and fast mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (i_{LOW}) of the SCLK signal. If the clock stretches the SCLK, the data must be valid by the setup mode before it releases the clock.
[6] $t_{VD;ACK}$ = time for Acknowledgement signal from SCLK LOW to SDA output (HIGH or LOW, depending on which one is longer).
[7] $t_{VD;DAT}$ = time for data signal from SCLK LOW to SDA output (HIGH or LOW, depending on which one is longer).

14.3.2 I²C bus electrical characteristics

Table 24. I²C SCLK and SDA

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IL}	LOW-level input voltage		-	0.3*V_{DD}[1]	V
V_{IH}	HIGH-level input voltage		0.7*V_{DD}[1]	-	V
V_{hys}	Hysteresis of Schmitt trigger inputs		0.05*V_{DD}[1]	-	V
V_{OL}	LOW-level output voltage	(Open-drain/open-collector) at 2 mA sink current V_{DD}[1] = < 2 V	0	0.2*V_{DD}[1]	V
V_{OH}	HIGH-level output voltage	(Open-drain/open-collector)	0.7*V_{DD}[1]	V_{DD}[1]	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	mA
		V_{OL} = 0.6 V	6	-	mA
I_{iL}	Input leakage current at the pin	V_{DD} = 1.8, Pin voltage = 1.8 V, 0.1 V_{DD} < VI < 0.9 V_{DD}[1]	-10	10	µA
C_i	Capacitance for each I/O pin		-	10	pF
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	ns
t_{of}	Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$	Pullup res = 250 ohm and max allowed load capacitance C_b	-	250	ns
C_b	Capacitive load for each bus line[2]		-	400	pF

[1] V_{DD} in this table refers to 1.8 V provided by the leader.
[2] The maximum t_f for the SDA and SCLK bus lines is specified at 300 ns. This allows series protection resistors to be connected in between the SDA and the SCLK pins and the SCLK bus lines without exceeding the maximum specified t_f.

15 Design considerations

15.1 Power on sequence

The initial power on sequence will take approximately 200 µs to complete the OTP memory fetching process. Therefore, it is suggested to wait at least 200 µs before issuing the SPI or I²C read and write processes. The normal SPI or I²C read and write processes should follow the sequence illustrated in Figure 14.

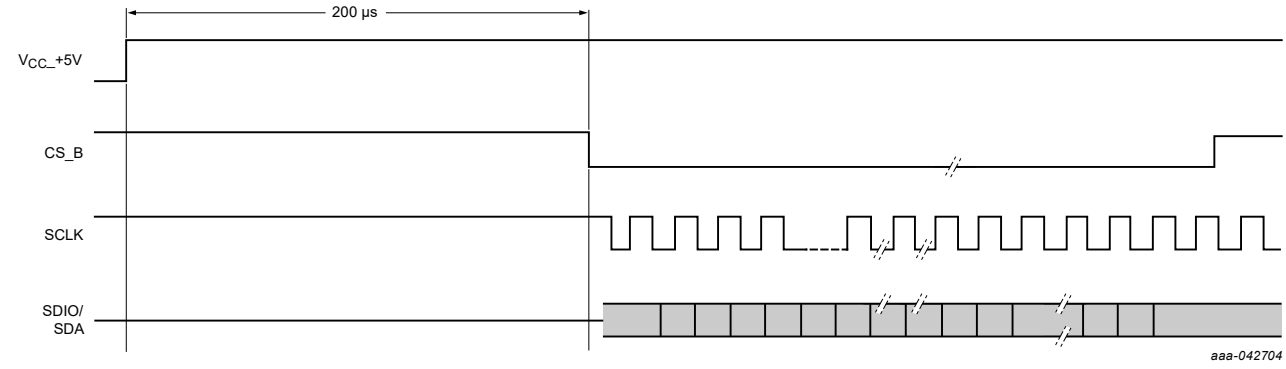


Figure 14. Power on sequence timing diagram

15.2 Programming guidelines to avoid hardware failure or damage

Users must be aware of the following guidelines to avoid potential hardware failure or damage.

- Do not program the Refresh OTP and Soft Reset bits to a 1 state at the same time.
- Soft Reset bit will reset Engineering Mode (EM).
- The Soft Reset bit is easily accessible; therefore, be cautious of the accidental reset.
- Tx_EN must not be active during an OTP refresh or during Engineering Mode.

15.3 Group programming

A common way of grouping A5M26SG240 modules is with parallel data inputs and unique chip CS_B connectivity. In this case, each module can be independently controlled and programmed by its individual CS_B, which has more flexibility to program each module separately as Figure 15 illustrates.

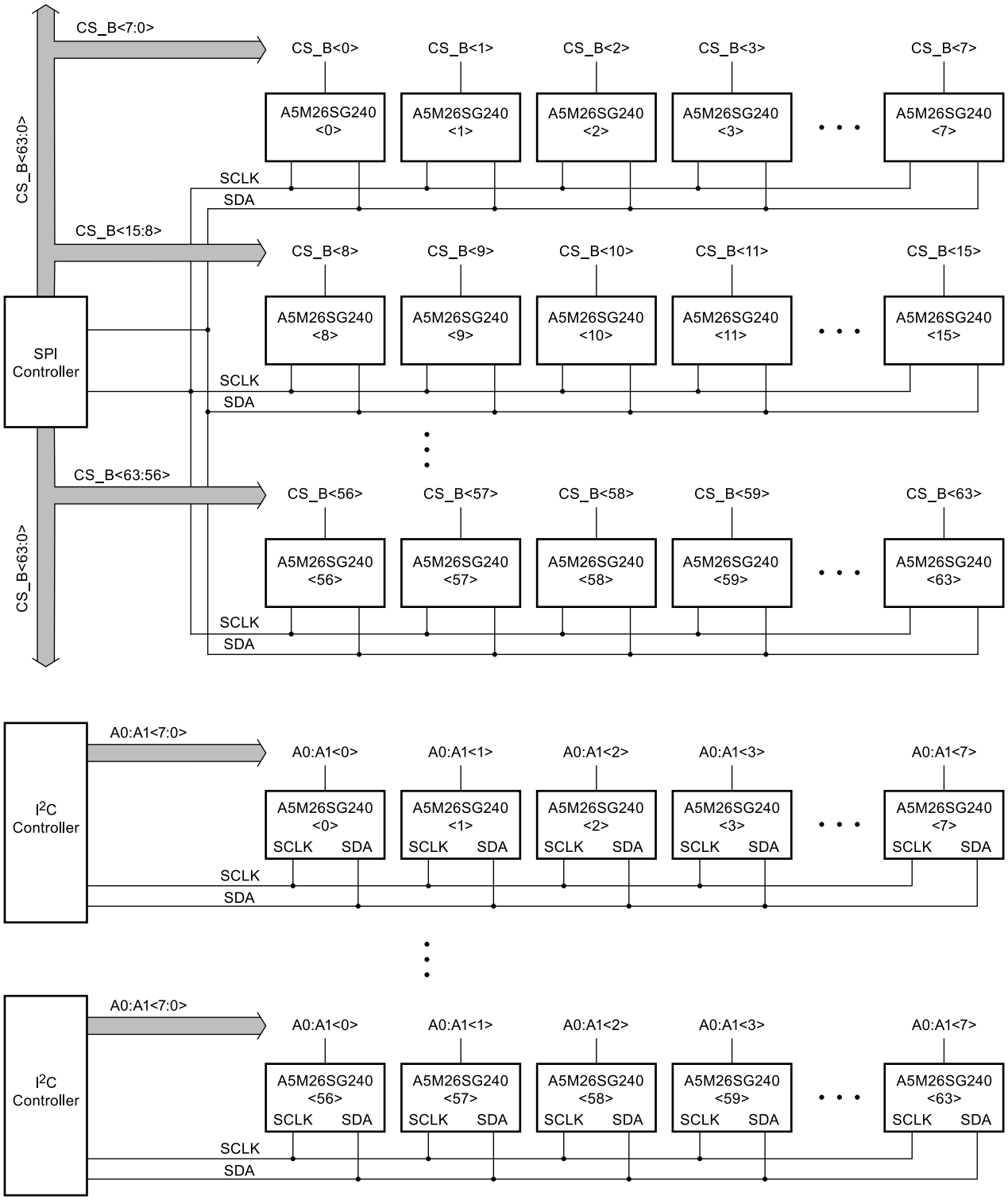


Figure 15. Parallel connectivity of grouping

16 Package information

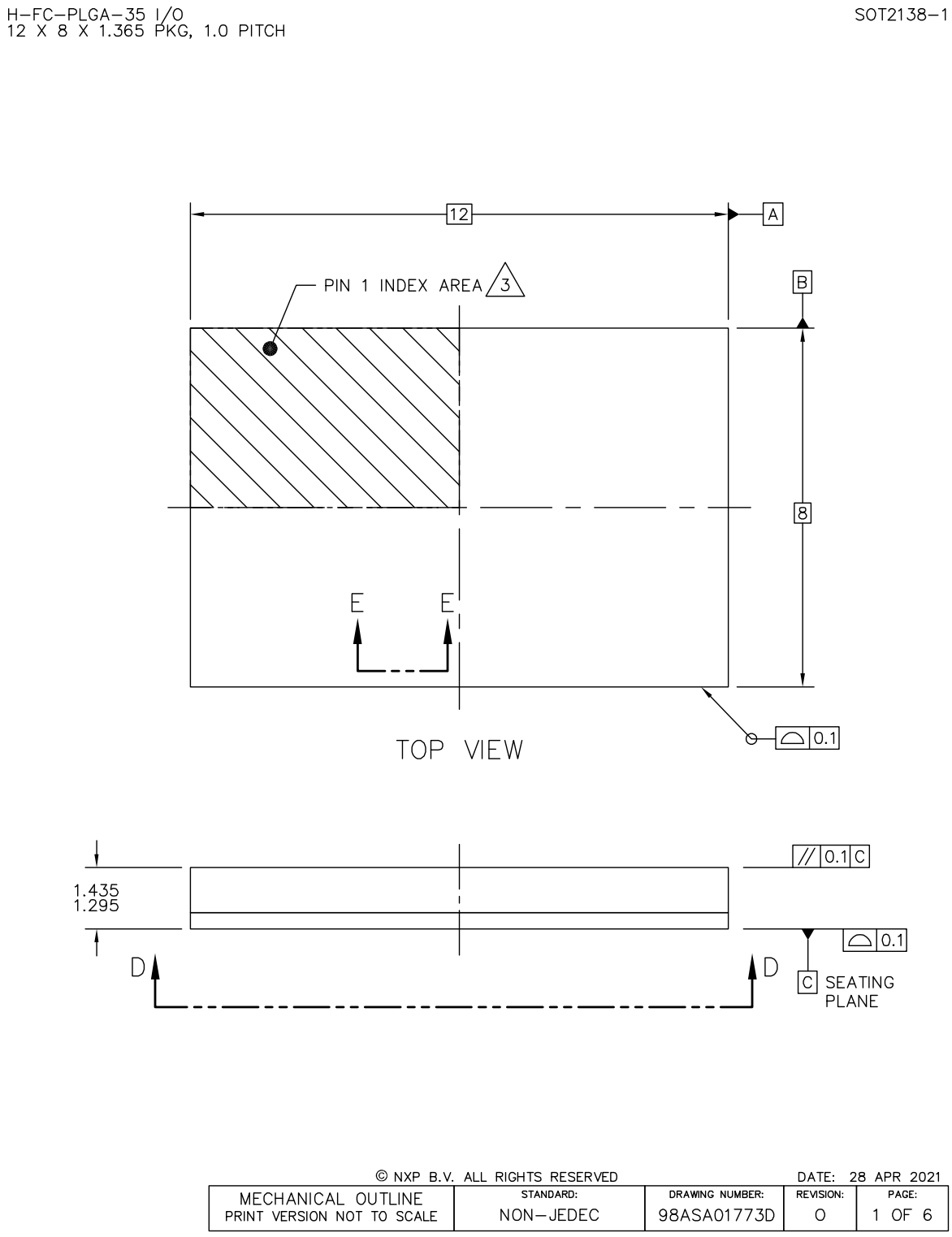


Figure 16. Package outline (12 mm × 8 mm Module) — top view

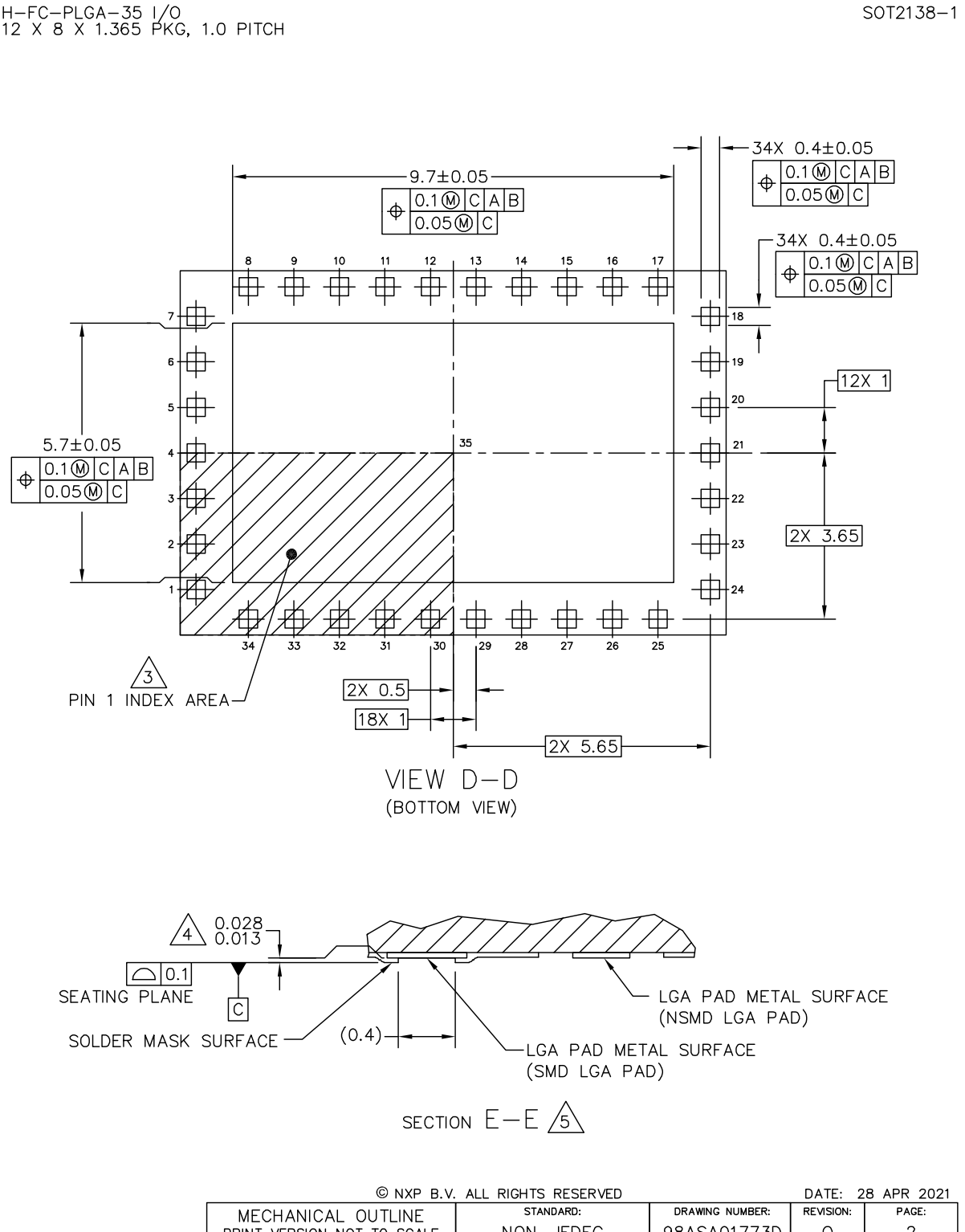
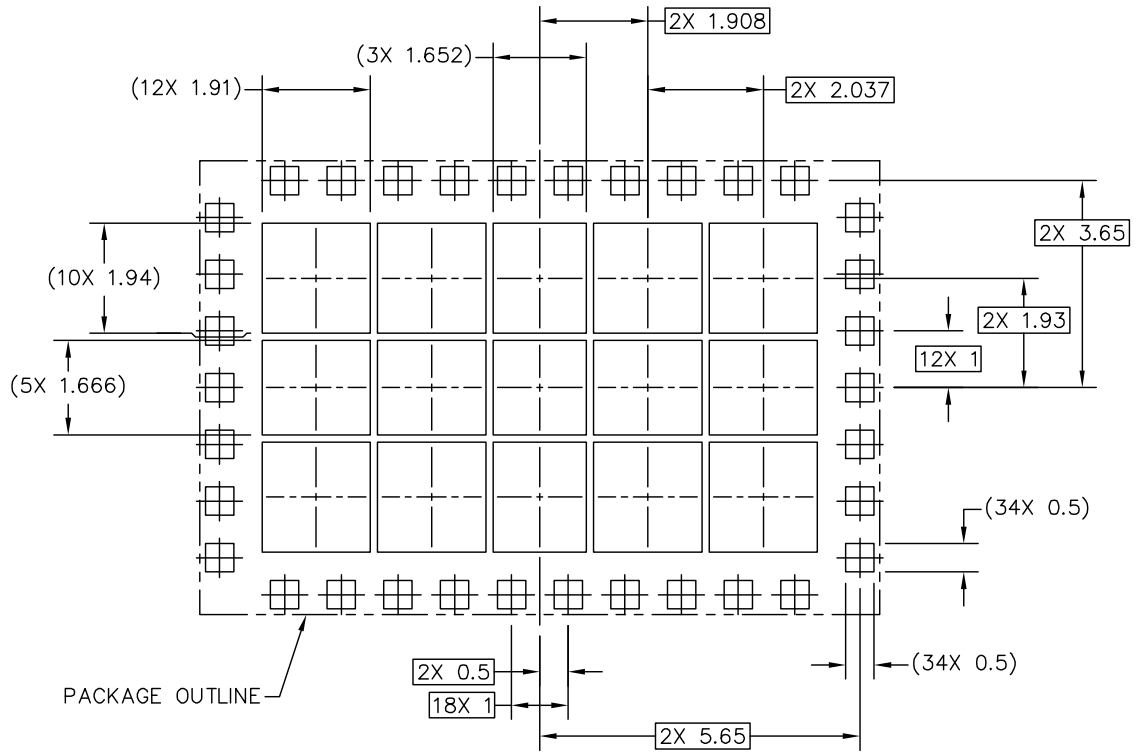


Figure 17. Package outline (12 mm × 8 mm Module) — bottom view

H–FC–PLGA–35 I/O
12 X 8 X 1.365 PKG, 1.0 PITCH

SOT2138–1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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DATE: 28 APR 2021

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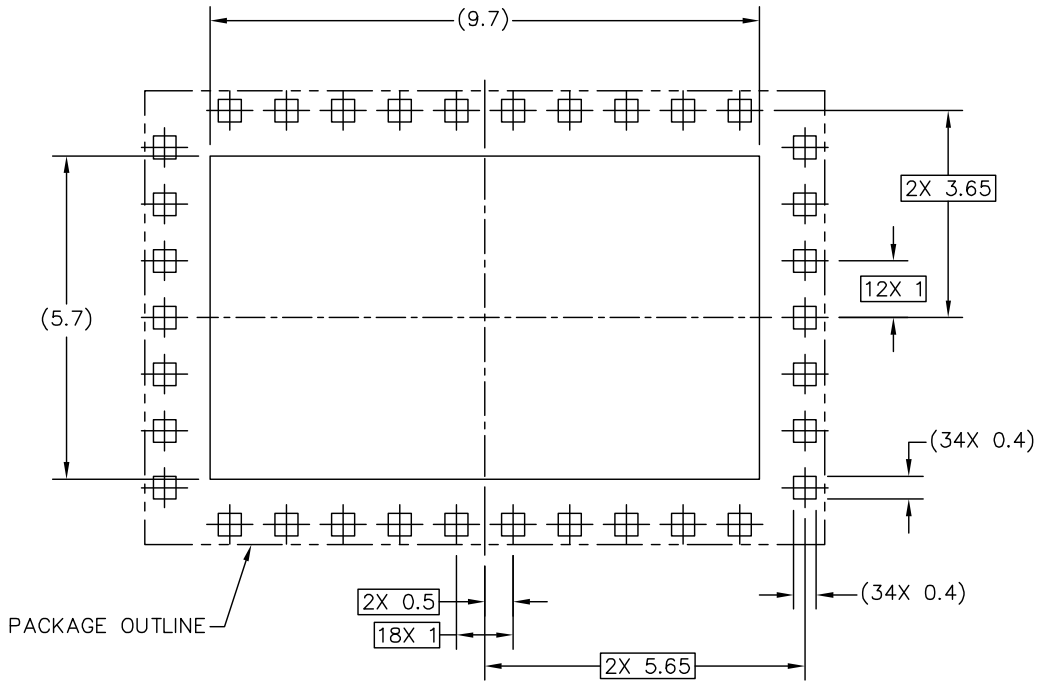
Figure 18. Package outline (12 mm × 8 mm Module) — PCB design guidelines: solder mask opening pattern

H–FC–PLGA–35 I/O
12 X 8 X 1.365 PKG, 1.0 PITCH

SOT2138–1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREAS

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA01773D	REVISION: O	PAGE: 4

Figure 19. Package outline (12 mm × 8 mm Module) — PCB design guidelines: I/O pads and solderable areas

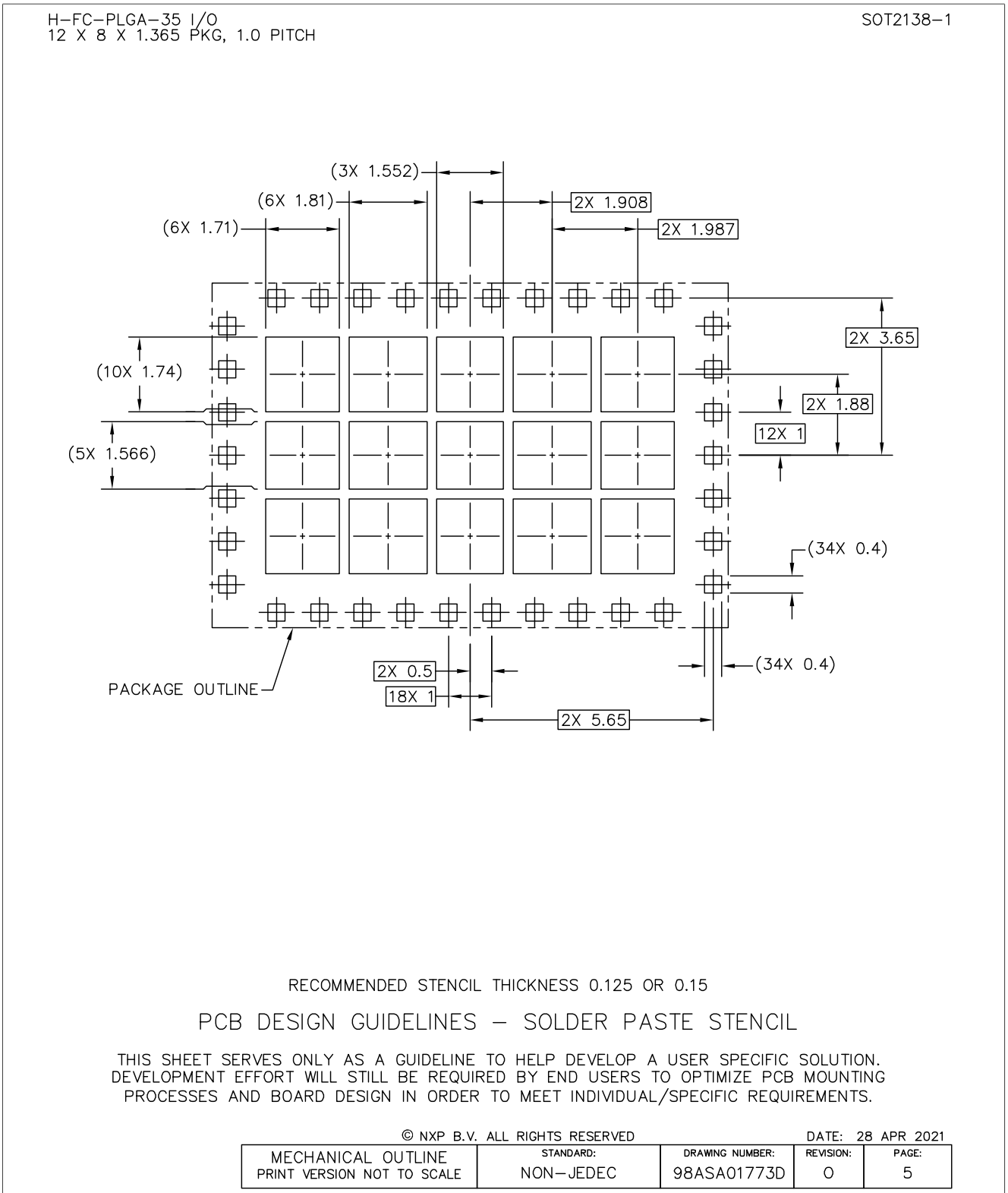

Figure 20. Package outline (12 mm × 8 mm Module) — PCB design guidelines: solder paste stencil

H–FC–PLGA–35 I/O
12 X 8 X 1.365 PKG, 1.0 PITCH

SOT2138–1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DIMENSION APPLIES TO ALL LEADS AND FLAG.
5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 35) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON–SOLDERMASK DEFINED (NSMD).

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Figure 21. Package outline (12 mm × 8 mm Module) — notes

17 Product software and tools

Refer to the following resources to aid your design process.

Development software

- Test, Debug and Analyzer Software

Development tools

- Printed Circuit Boards

18 Failure analysis

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

19 Revision history

The following table summarizes revisions to this document.

Table 25. Revision history

Document ID	Release date	Description
A5M26SG240 Rev. 1	8 November 2024	• Initial release of product data sheet

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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Contents