Freescale Semiconductor
Application Note

AN3820
Rev. 1.0, 3/2009

i.MX25 Power Management Using the MC34704

1 Overview

This document presents an analysis of using the MC34704 power management IC to supply a system based on the i.MX25. The focus was done on the i.MX25 itself, considering its needs in terms of voltage, current, and the power-up sequence. The DDR and Flash memory requirements were also taken into account. However, the MC34704 voltage capabilities are not limited to the scenarios presented within this document.

Contents

freescale™ semiconductor

2 i.MX25 Requirements

2.1 Voltage Requirements

Table 1 summarizes the approximate voltage requirements on i.MX25:

Table 1. i.MX25 Voltage Requirements

Parameter	Symbol	Min.	Typ.	Max.	Units
Core supply voltage (at 266 MHz)	QV_{DD}	1.15	1.34	1.52	V
Core supply voltage (at 400 MHz)		1.38	1.45	1.52	V
Coin Battery	V_{DD_BAT}	1.15	-	1.55	V
I/O supply voltage GPIO1 (NFC, CSI, SDIO)	NV_{DD_GPIO1}	1.75	-	3.6	V
I/O supply voltage GPIO2 (CRM, LCDC, JTAG, MISC)	NV_{DD_GPIO2}	3.0	3.3	3.6	V
I/O supply voltage DDR (Mobile DDR mode) (EMI1, EMI2)	NV_{DD_MDDR}	1.75	-	1.95	V
I/O supply voltage DDR (DDR2 mode) (EMI1, EMI2)	NV_{DD_DDR2}	1.75	-	1.9	V
I/O supply voltage DDR (SDRAM mode) (EMI1, EMI2)	NV_{DD_SDRAM}	1.75	-	3.6	V
USBPHY1 supply (HS) (USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD. USBPHY1_VDDA)	$V_{DD\_USBPHY1}$	3.17	3.3	3.43	V
USBPHY2 supply (FS) (USBPHY2_VDD)	$V_{DD\_USBPHY2}$	3.0	3.3	3.6	V
OSC24M supply (OSC24M_VDD)	V_{DD_OSC24M}	3.0	3.3	3.6	V
PLL supply (MPLL_VDD, UPLL_VDD)	V_{DD_PLL}	1.4	-	1.65	V
Supply of touch screen ADC (NVCC_ADC)	V_{DD_TSC}	3.0	3.3	3.6	V
External reference of touch screen ADC	V_{REF}	2.5	V_{DD_tsc}	V_{DD_tsc}	
Fusebox program supply voltage (FUSE_VDD)	$FUSEV_{DD}$	-	3.6	-	V

The i.MX25 processor consists of four major sets for the power supply voltage: digital logic domains (V_{DDn}), I/O power supplies (N_{VDDx}), analog power supplies, and the fuse voltage supply ($FUSE_{VDD}$). These voltage domains can be grouped together, depending on the operating mode and needs of the I.MX processor, and the specific application.

2.2 Power-up Sequencing

The external voltage regulators and power-on devices must provide the application's processor with a specific sequence of power and resets to ensure proper operation.

The recommended power-up sequences is as follows:

1. Assert the power on reset signal (POR = Low)
2. Turn on the Digital logic domain and I/O power supplies (V_{DDn} and N_{VCCx})
3. Turn on all Analog power supplies and $FUSE_{VDD}$
4. Negate the POR signal (POR = High)

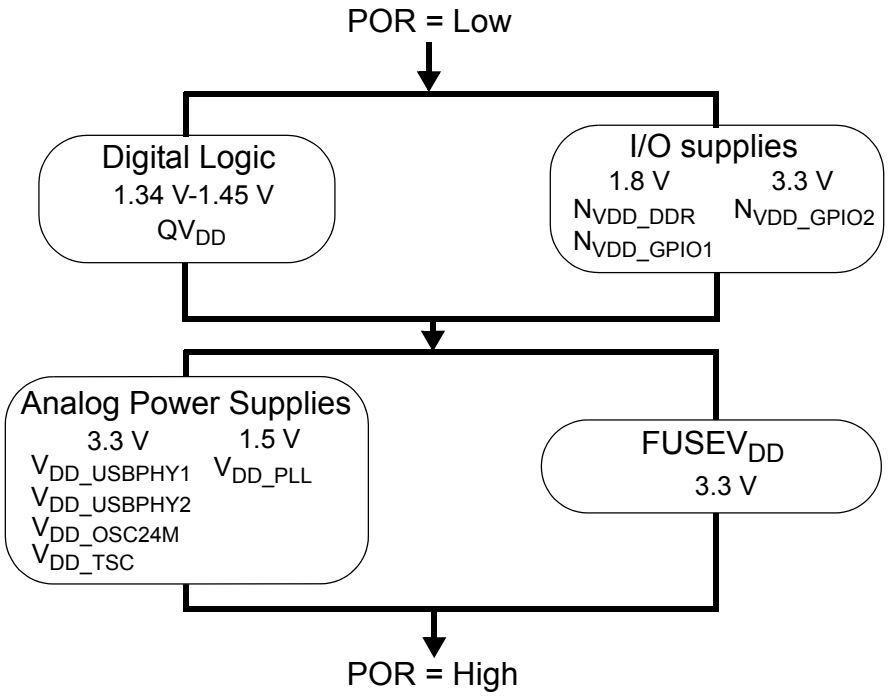

Figure 1. i.MX25 Recommended Power-up Sequencing

Some of the voltage domain may be powered-up out of the recommended sequence if necessary. However, it is important to power QV_{DD} before the $FUSEV_{DD}$, to avoid an unintentional fuse blown. Figure 1 shows the recommended power-up sequence and power terminal grouping to achieve successful a power-up.

Noticed that since the maximum operating voltage for the core voltage group is 1.52 V, caution must be taken in order to have a very tight regulation, and avoid overstressing or blowing the microprocessor terminals.

3 MC34704 PMIC

The MC34704 family features both a 5-channel (MC34704B) and an 8-channel (MC34704A) power management IC (PMIC), housed in a 56 pin QFN package with pin-to-pin compatibility between both ICs. It is meant to address power management needs for various components and loads, with a target overall efficiency of > 89% at typical loads.

The MC34704 accepts an input voltage from 2.7 V to 5.5 V, from various sources:

• 1-cell Li-Ion/Polymer (2.7 V to 4.2 V)

• 5.0 V USB supply or AC wall adapter

The total voltage supply range the IC accommodates is 2.7 V to 5.5 V.

Taking advantage of its buck/boost blocks, the MC34704 is a highly flexible power management unit. Output voltages can be ranged between 0.6 V to 3.6 V, even if low voltage is supplied by the battery.

Additionally, the Dynamic Voltage Scaling (DVS) feature allows programming the output voltages (±20% of the nominal voltage), with the I^2C bus on the fly. Hence, the dynamic power consumption of the i.MX can be dramatically reduced.

Features:

- 8 DC/DC switching regulators with up to ±2% output voltage accuracy
- Programable Switching Frequency from 250 KHz - 1.0 MHz and 750 KHz to 2.0 MHz
- Effective Efficiency from 85% to 95% on REG1 - REG5 and 65% to 78% on REG6 - REG8
- DVS (Dynamic voltage scaling) on all regulators.
- I^2C programmability
- OV/UV detection for each regulator
- Over-current limit detection and short-circuit protection.
- Thermal limit detection (except REG7)
- Internal compensation for REG1, REG3, REG6, and REG8
- True cutoff on all of the boost and buck-boost regulators.

4 MC34704 and i.MX25 Compatibility

4.1 Power Breakdown

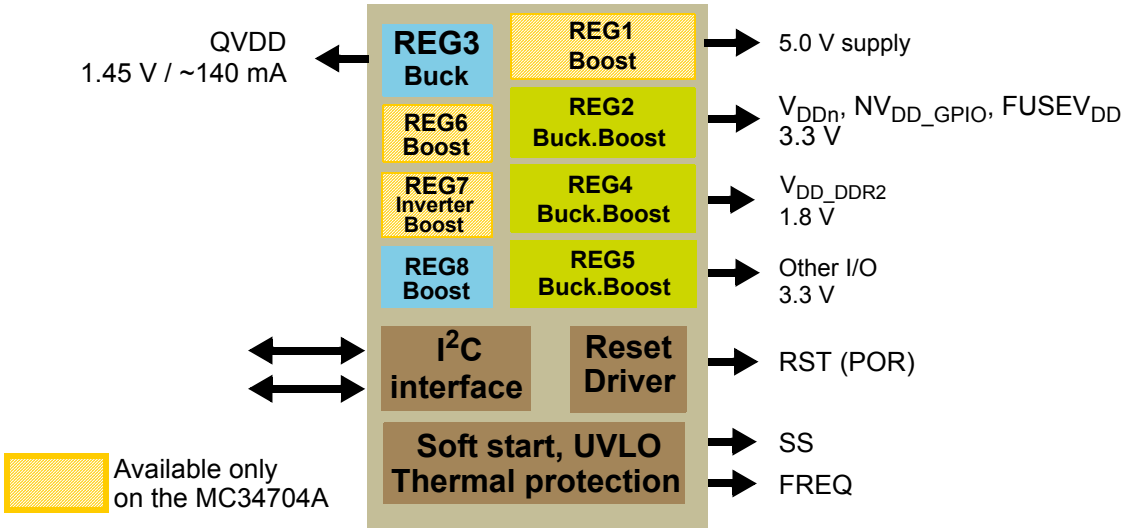

Figure 2. MC34704 block diagram

Figure 2 shows the block diagram for the MC34704 and the simplified voltage distribution compatible with the i.MX25 processor. Complementary LDO regulators may be needed in specific applications. A 1.5 V LDO is at least required to supply the PLL voltage.

Figure 3 provides the detailed Power Map for a complete solution utilizing the MC34704A as the core PMIC, complemented with various LDOs to provide some application oriented voltages.

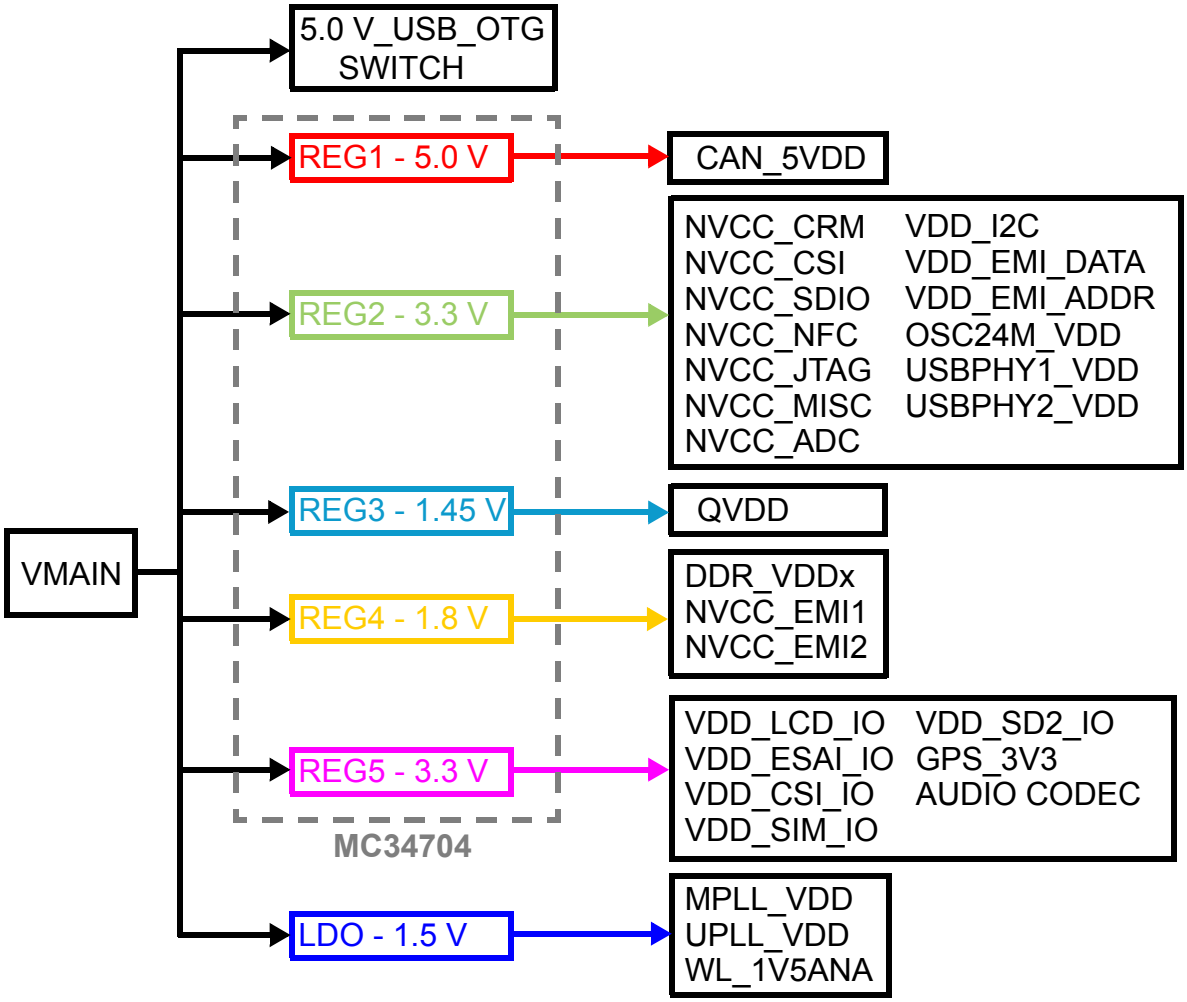

Figure 3. i.MX25 Power Detailed Power Map

4.2 Power Sequencing

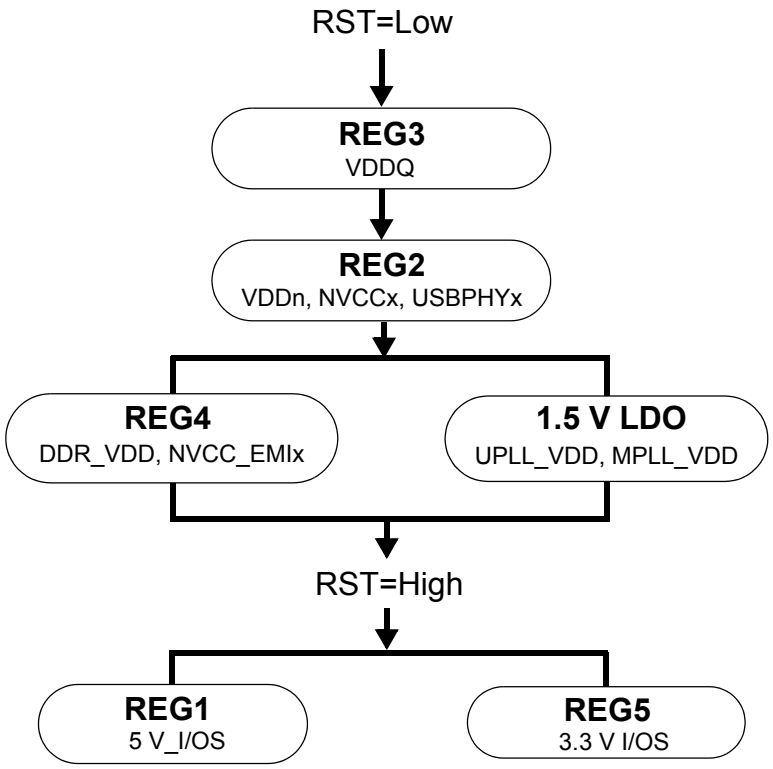

Figure 4. MC34704 power sequencing

The MC34704 provides standalone voltage on REG 2, 3, and 4, right after battery insertion or ON/OFF asserting. The LDO providing the 1.5 V is supplied from the main voltage supply (DC_5.0 V or USB). However, the output voltage is enabled with the REG2 output in order to assure proper sequencing. REG1 and REG5 are controlled via I^2C, and can be turned ON/OFF once the RST signal (POR) on the MC34704 is set high.

Note that even though this structure does not perfectly, follow the power-up sequence, it has been proven to work correctly, and may be counted as one of the recommended power-up sequences for the i.MX25 processor.

REG2, 3, and 4 can only be powered off in two ways:

1. By a hardware power-off, holding down the ON/OFF terminal for a specific amount of time (programmable).
2. By a soft power-off, by setting high the ALLOFF bit via I^2C.

Note that these two processes will shut down the device completely, including REG1, REG5, 1.5 V_LDO, and I^2C communication. To bring the device back up, generate a falling edge on the ON/OFF terminal (commonly using a push button.)

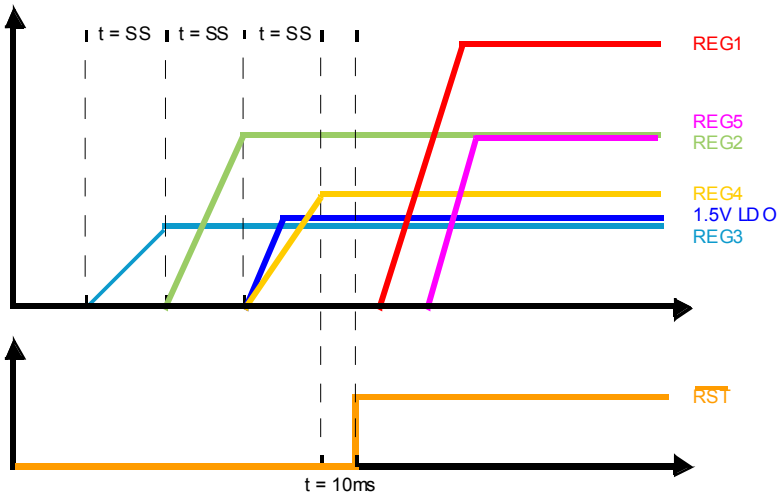

Figure 5. System Power-up Waveform

Figure 5 shows the power sequence waveforms during a Power-up cycle.

Note that REG1 through REG5 on the MC34704 ramp-up in a pre-defined soft start. The soft start is hardware configured and its value is selectable among 0.5, 2.0, 8.0, and 32 ms. The 1.5 V LDO waveform may reach its regulation point before or after REG4, depending on the selected soft start.

4.3 i.MX25 System Power Block Diagram

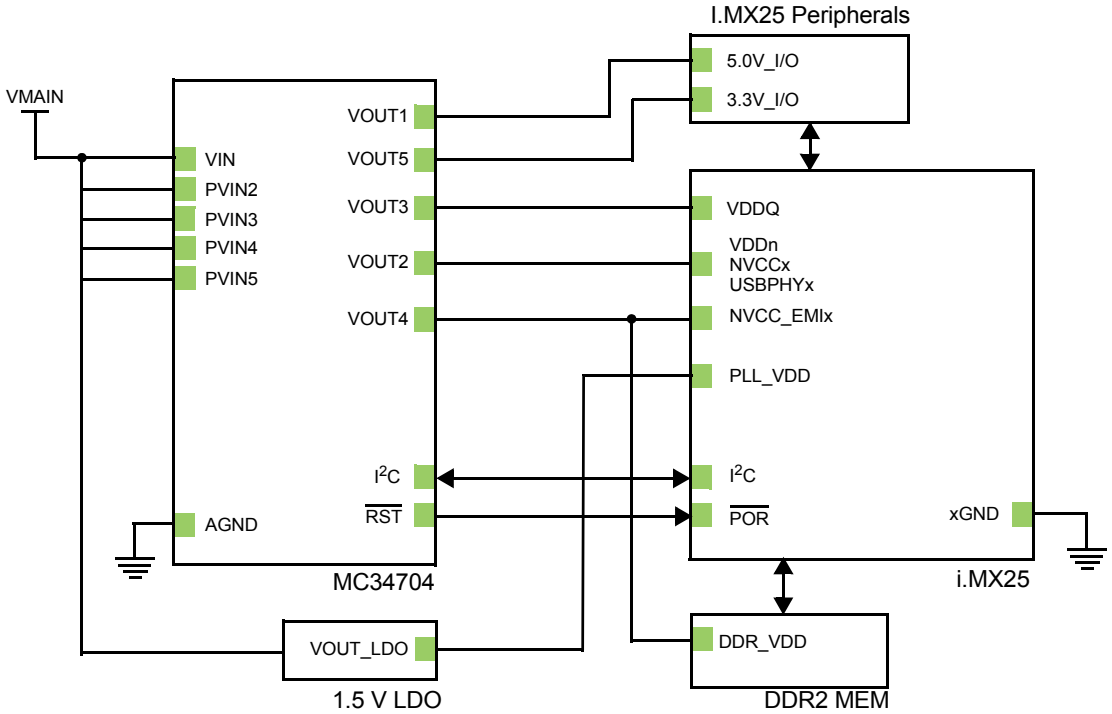

Figure 6. i.MX25 Power Pins

5 Software Considerations

The MC34704 is programmed through a plain I^{2}C protocol. The I.MX processor should include a firmware driver to translate the controlling instructions into I^{2}C commands, to allow register writing and flag reading for communication acknowledgement. Such driver structure is not defined in this document. It discusses only the software portion that concerns the MC34704, as well as the I^{2}C commands needed to interact with the MC34704.

5.1 I^{2}C Communication Protocol

The MC34704 is able to operate in two I^{2}C modes:

- Non-accurate mode: which uses a single repetition of register address and data to be read or written during one cycle. This mode is used as the default by the MC34704.
- Accurate mode: where each Address and Data word is sent twice to make sure the information written or read is valid.

To simplify the I^{2}C protocol, only non-accurate mode will be discussed in this document.

Figure 7 and Figure 8 show an example of a bits stream for an I^{2}C writing and reading command respectively.

7 bit Physical Address + (w) bit	ACK	Sub-Address (MSB=0)	ACK	Data	ACK
1010100 + 0	0	0XXXXXXX	0	XXXXXXXX	0

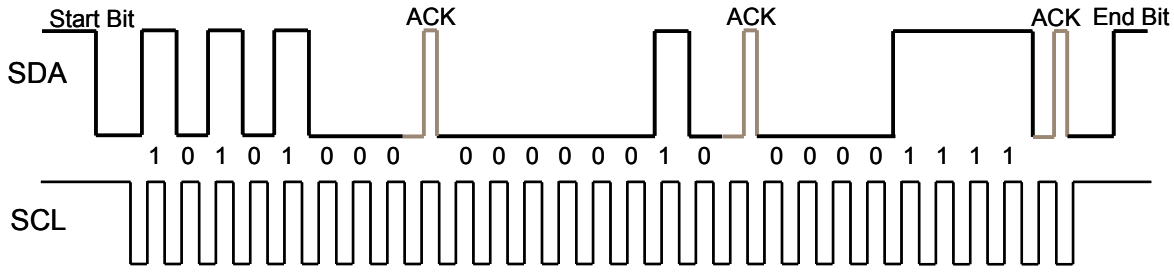

Figure 7. Writing Sequence I^{2}C Bit Stream.

7 bit Physical Add + (w) bit	ACK	Sub-Address (MSB=1)	ACK	RS	Physical Add + (r) bit	Data Read	ACK
1010100 + 0	0	1XXXXXXX	0	1	1010100+1	XXXXXXXX	0

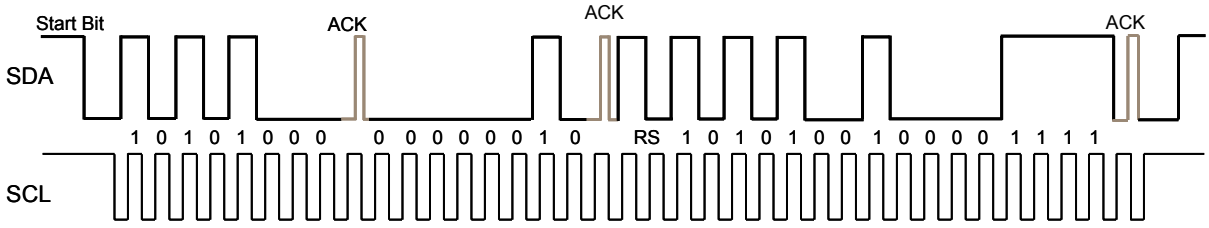

Figure 8. Reading Sequence I^{2}C Bit Stream.

By default, the MC34704's physical address is set to 0x54 in a 7-bit format. The extra bit to complete the 8-bit indicates the reading or writing mode as shown in Figure 7 and Figure 8. After each byte read or sent, the MC34704 answers with an acknowledge bit, indicating the bite was transferred successfully.

Figure 9 shows the basic I²C register table, including both configuration and fault notification registers for each regulator on the MC34704.

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
$00	Reserved	-							
$01	GENERAL1	-				SDDELAY[1:0]		CCDSEQ[1:0]	
$02	GENERAL2	-			ALLOFF	ONOFFA	ONOFFC	ONOFFD	ONOFFE
$03	GENERAL3	-			SHTD	COLDF	BATTYPE	SSTIME[1:0]	
$04	VGSET1	-			DVSSET1[3:0]				OVUVSET1
$05	VGSET2	-		TSDF1	SCF1	ILIMF1	UVF1	OVF1	DVSSTAT1
$06	REG2SET1	-			DVSSET2[3:0]				OVUVSET2
$07	REG2SET2	-		TSDF2	SCF2	ILIMF2	UVF2	OVF2	DVSSTAT2
$08	REG3SET1	-			DVSSET3[3:0]				OVUVSET3
$09	REG3SET2	-		TSDF3	SCF3	ILIMF3	UVF3	OVF3	DVSSTAT3
$0A	REG4SET1	-			DVSSET4[3:0]				OVUVSET4
$0B	REG4SET2	-		TSDF4	SCF4	ILIMF4	UVF4	OVF4	DVSSTAT4
$0C	REG5SET1	-			DVSSET5[3:0]				OVUVSET5
$0D	REG5SET2	-						SSSET5[1:0]	
$0E	REG5SET3	-		TSDF5	SCF5	ILIMF5	UVF5	OVF5	DVSSTAT5
$0F	REG6SET1	-			DVSSET6[3:0]				OVUVSET6
$10	REG6SET2	-						SSSET6[1:0]	
$11	REG6SET3	-		TSDF6	SCF6	ILIMF6	UVF6	OVF6	DVSSTAT6
$12	REG7SET1	-			DVSSET7[3:0]				OVUVSET7
$13	REG7SET2	-				FSW2[1:0]		SSSET7[1:0]	
$14	REG7SET3	-					UVF7	OVF7	DVSSTAT7
$15	REG8SET1	-			DVSSET8[3:0]				OVUVSET8
$16	REG8SET2	-	ILED[3:0]				REG8MODE	SSSET8[1:0]	
$17	REG8SET3	-		TSDF8	SCF8	ILIMF8	UVF8	OVF8	DVSSTAT8
$18	FAULTS	FLT8	FLT7	FLT6	FLT5	FLT4	FLT3	FLT2	FLT1
$19	I2CSET1	-							ACCURATE
$49	REG3DAC	3DAC7	3DAC6	3DAC5	3DAC4	3DAC3	3DAC2	3DAC1	3DAC0
$58	REG7CR0	EN[1:0]		-	DISCHG_B	-			
$59	REG7DAC	7DAC7	7DAC6	7DAC5	7DAC4	7DAC3	7DAC2	7DAC1	7DAC0

Figure 9. Basic I²C Register Table

5.2 Power-up Command Sequence

The Power on process is straight forward:

- If there is a battery insertion, REG3, 2, and 4 will turn on in that order, enabling I²C communication protocol as well as the i.MX processor power on sequence. The MC34704 will set the COLDF flag to acknowledge that power on was a result of a battery insertion. During the power on process, the MPU should acknowledge that power-up was a result of a battery insertion, and then send an ALLOFF I²C command to disable the power supply and shut down until a desired hardware power on is present.
- If the ON/OFF terminal detects a falling edge, then the MC34704 starts a power on cycle ramping up of regulator 3, 2, and 4. The COLDF bit is not set high, and so when the i.MX processor reads this register, it acknowledges it is an actual power up, and starts a full power on sequence. By now, the PMIC is providing

1.45 V, 1.8 V, 3.3 V, and 1.5 V, which is dispensed by the extra LDO, and the processor can administer the following configuration commands:

- REG2, REG3, and REG4 OV/UV response
- REG1 and REG5 OV/UV response
- REG5 Soft start timing (if desired)

- Now the processor can send a REG5 ON/OFF instruction via I^2C, when the 3.3 V peripherals rail is required, and also enable REG1 if the 5.0 V voltage rail is needed. Subsequently, all voltage rails can be dynamically scaled (DVS) up or down using the 4 bits (4:1) from the REGxSET register.
- The i.MX processor can send an I^2C power-off command for REG1 or REG5 independently or a complete shutdown by setting the ALLOFF bit on the GENERAL2 register when required.

5.3 Dynamic Voltage Scaling (DVS)

All regulators on the MC34704 allow voltage scaling, programmable through I^2C, Table 2 defines the DVS capability for each output as well as the I^2C register corresponding to each.

Table 2. MC34704 DVS Definition

REGULATOR	SCALING WINDOW	SCALING STEP	I2C REGISTER	ADDRESS	REGISTER BITS
REG1	-10% to 10%	2.5%	VGSET1	0x04	[4:1]
REG2	-17.5% to 17.5%	2.5%	REG2SET1	0x06	[4:1]
REG3	-17.5% to 17.5%	2.5%	REG3SET1	0x08	[4:1]
REG4	-10% to 10%	1.0%	REG4SET1	0x0A	[4:1]
REG5	-17.5% to 17.5%	2.5%	REG5SET1	0x0C	[4:1]

For REG3, the MC34704 provides fine DVS adjustment on 0.5% steps, to achieve voltage scaling below the -17.5% windows allowed with the default DVS. The following sequence should be followed to assure proper scaling without activating OV/UV fault flags.

1. Set the REG3SET1 register (ADD 0x08) to 0x10.
2. Mask the fault response by writing 0x80 to ADD 0x22.
3. Write a 0xAD to REG3DAC (ADD 0x49).
4. Decrease REG3DAC by one until reaching the desired value on REG3.
5. Clear the fault response masking by writing 0x00 to ADD 0x22.

6 MC34704 Power Supply Design

6.1 Components Selection and Consideration

6.1.1 Inductor Selection

VG serves as the internal supply for all gate drivers within the MC34704. L1 dimensions depend directly on the inductance value and the saturation current I_{SAT}. Chose an inductor with inductance value between 2.2 to 4.7 μH, and an I_{SAT} around 150 mA.

To select Inductors L2 - L5, choose inductance values between 3.0 to 4.7 μH, with an I_{SAT} of approximately twice the maximum current to be demanded from each regulator.

Note: make sure to use power inductors and not choke inductors for these components. Shielded “Drum Core” inductors with low DCR are recommended to improve the performance of the MC34704.

6.1.2 Capacitor and Resistor selection

Choose capacitors with at least twice the voltage rating as the maximum voltage that the capacitor will be exposed to. For output capacitors, use capacitance values from 10 to 22 μF.

Resistors are straightforward to choose. The important thing to consider, while calculating the output voltage of each regulator, is to take into consideration the resistor accuracy , especially on those voltage rails where the output voltage is close to the maximum voltage rating of the I.MX terminal. A miscalculation of the resistor accuracy may cause the output voltage to go slightly above the maximum allowed, overstressing or damaging the processor terminal in the application. Use 1% or smaller tolerance resistors to have good control of output voltage values.

Note: for more details on external component calculation, please refer to the MC34704 data sheet that can be found at www.freescale.com.

6.2 i.MX25 Power Management Schematic

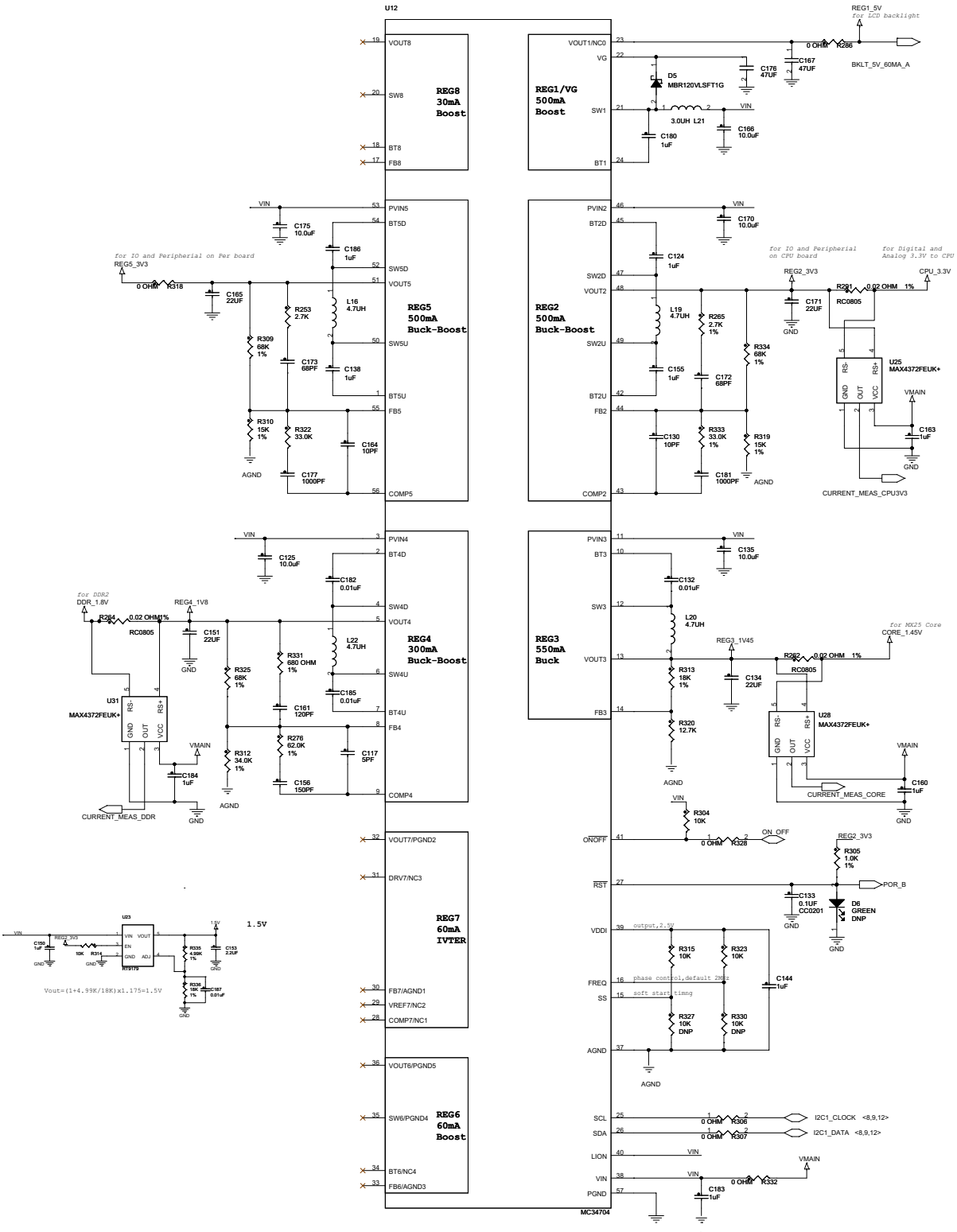

Figure 10. MC34704 + 1.5 V LDO Schematic

6.3 Layout Example

The following layout is an implementation of the MC34704 interacting with the i.MX25 in the PDK developed by Freescale. The layout stacking is defined based upon the i.MX requirements of a 10 layer PCB. Layer 2 and 8 correspond to GND planes, while layers 5 and 6 are power planes. For simplification, these layers will not be presented, since they do not provide significant information about the power management design. The remaining layers are dedicated to signal and voltage rail routing, and are shown in Figure 11 through Figure 17.

This layout design has been cropped to show components placement and routing, relating to the power supply design with the MC34704 (U10). However, some extra components may be shown as part of the complete system design using the i.MX25 chip.

6.3.1 Top Layer

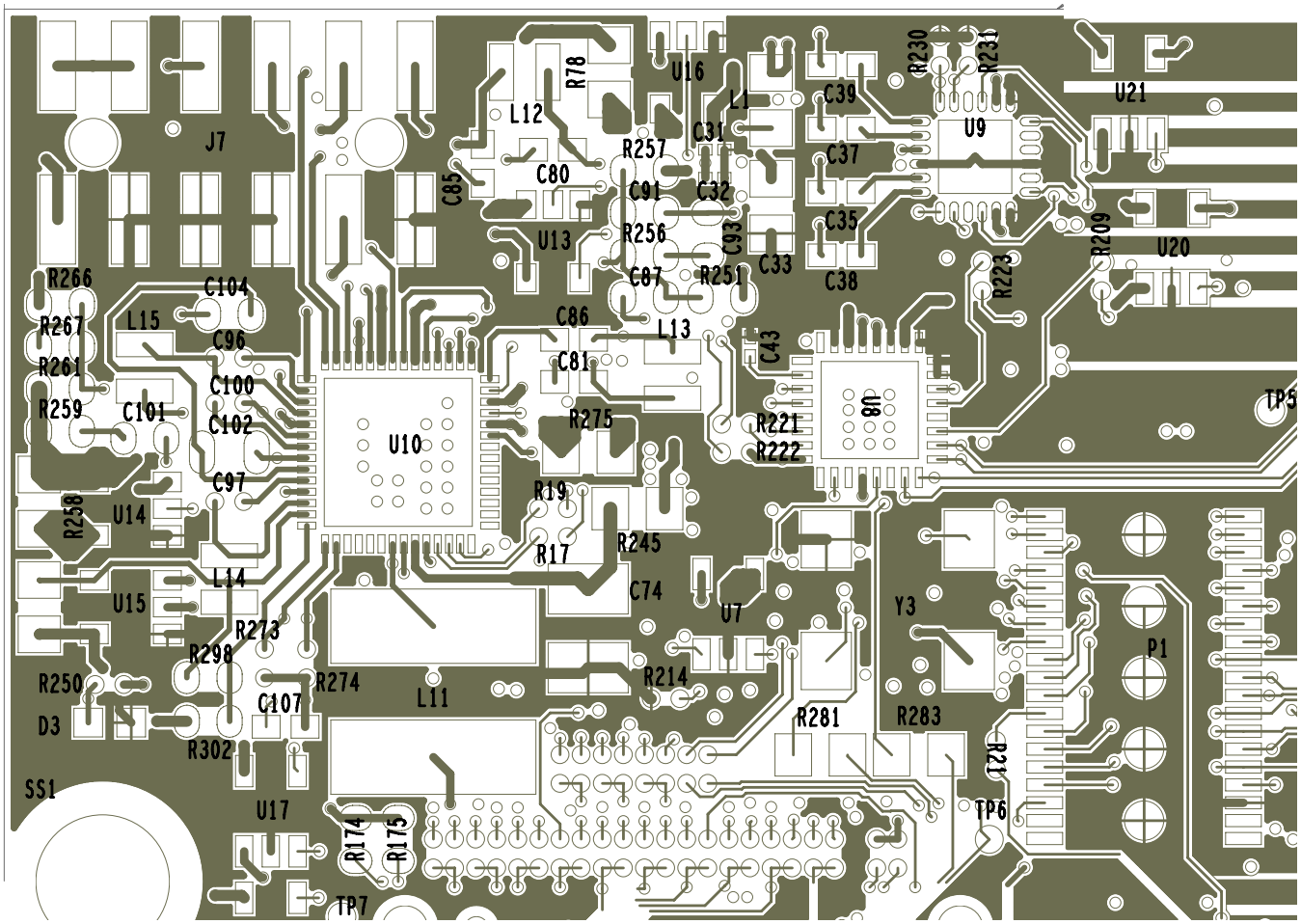

Figure 11. MC34704 Top Layer PCB Layout Implementation.

6.3.2 Internal Layer 1 (Signal)

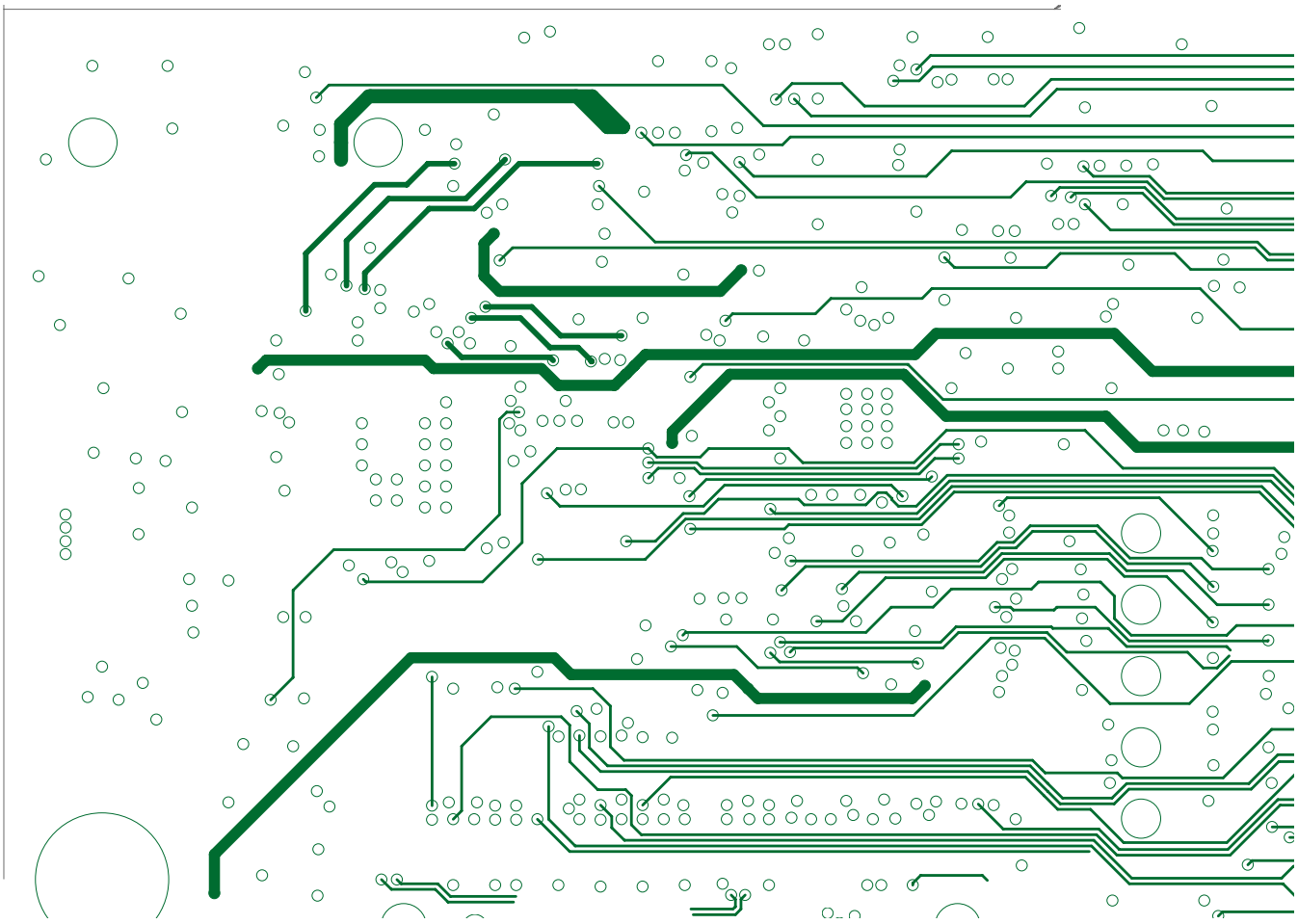

Figure 12. MC34704 Implementation Internal Layer 1

6.3.3 Internal Layer 2 (Signal)

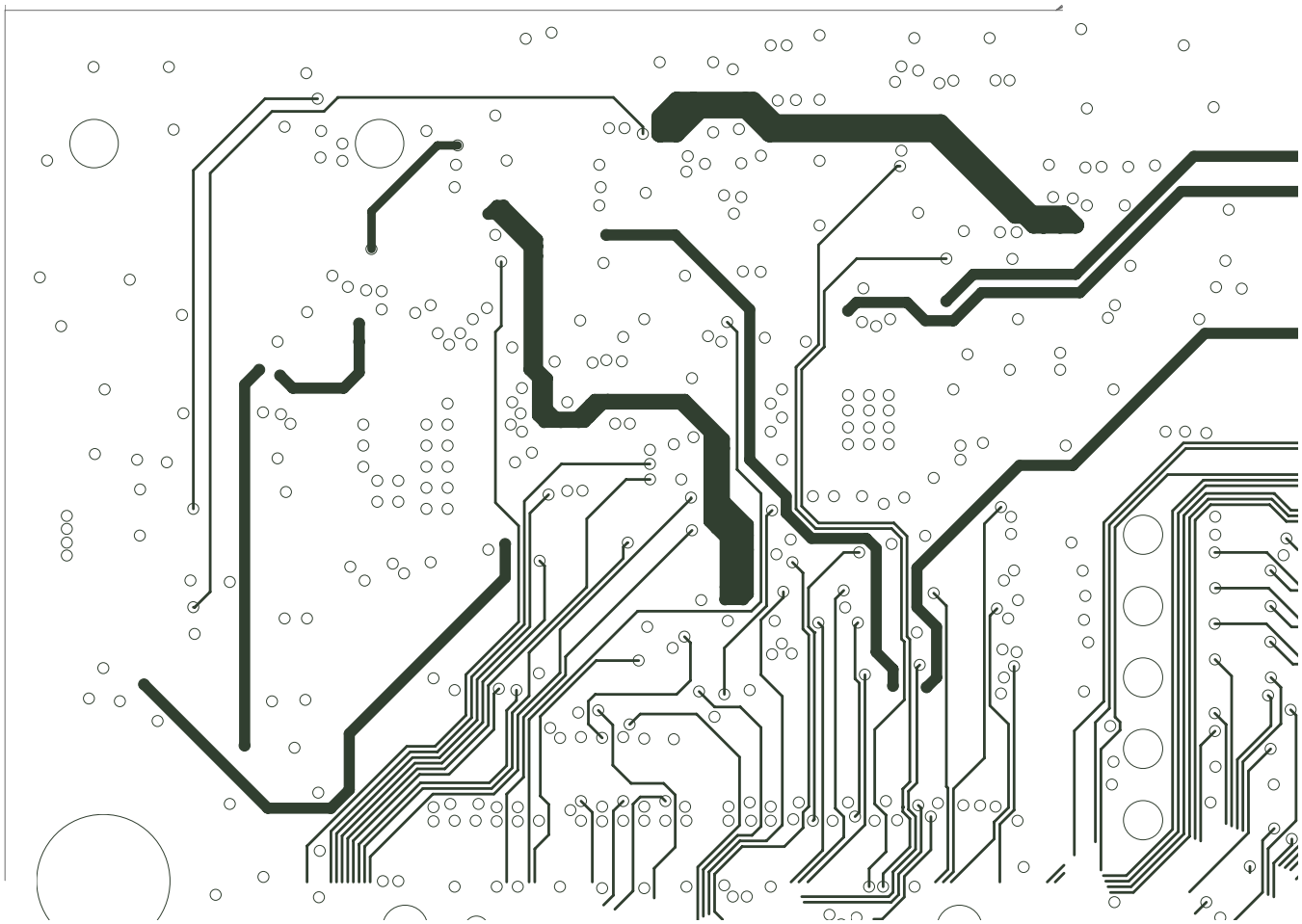

Figure 13. MC34704 Implementation Internal Layer 2

6.3.4 Internal Layer 3 (GND + Signals)

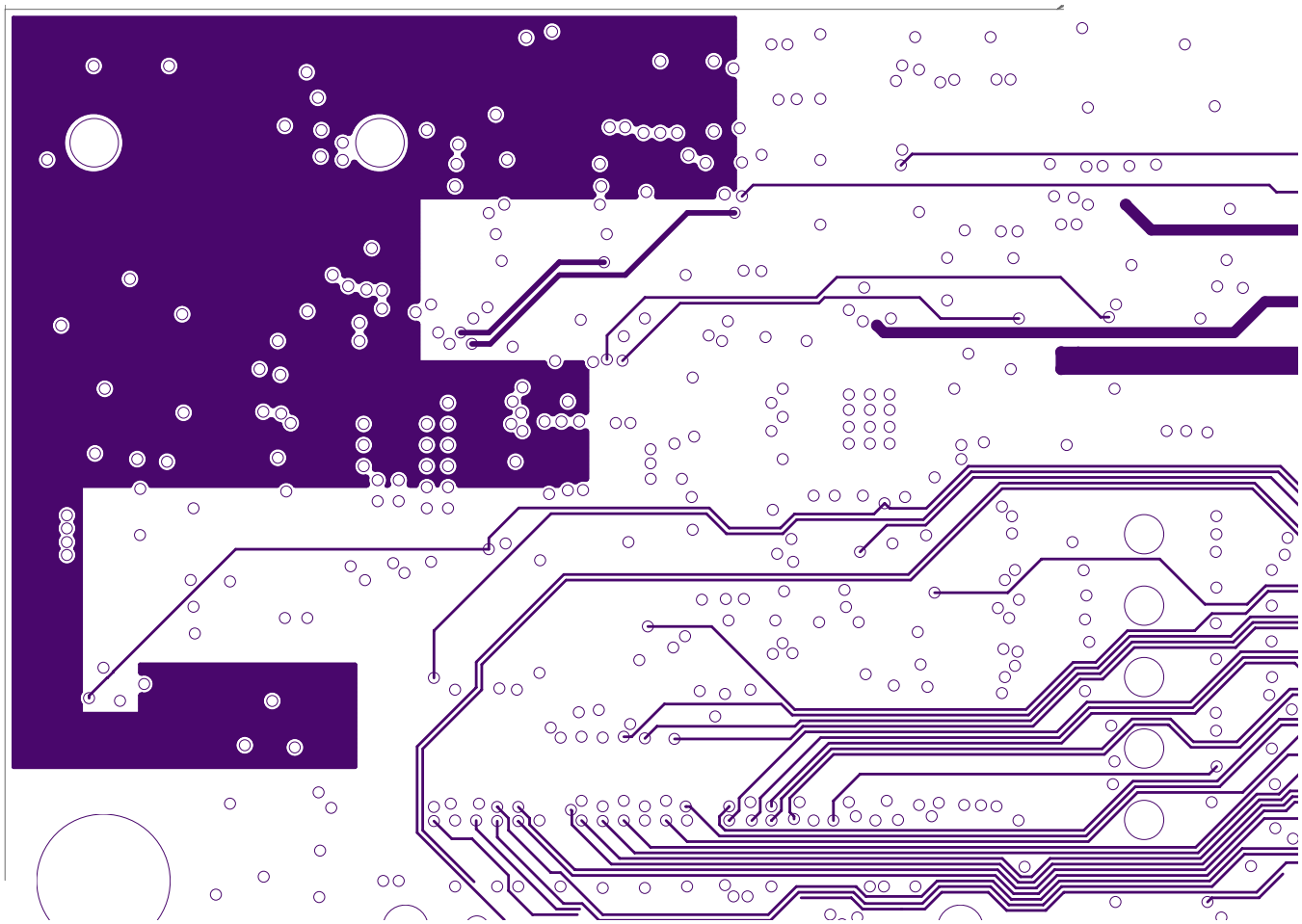

Figure 14. MC34704 Implementation Internal Layer 3

6.3.5 Internal Layer 4 (Signal)

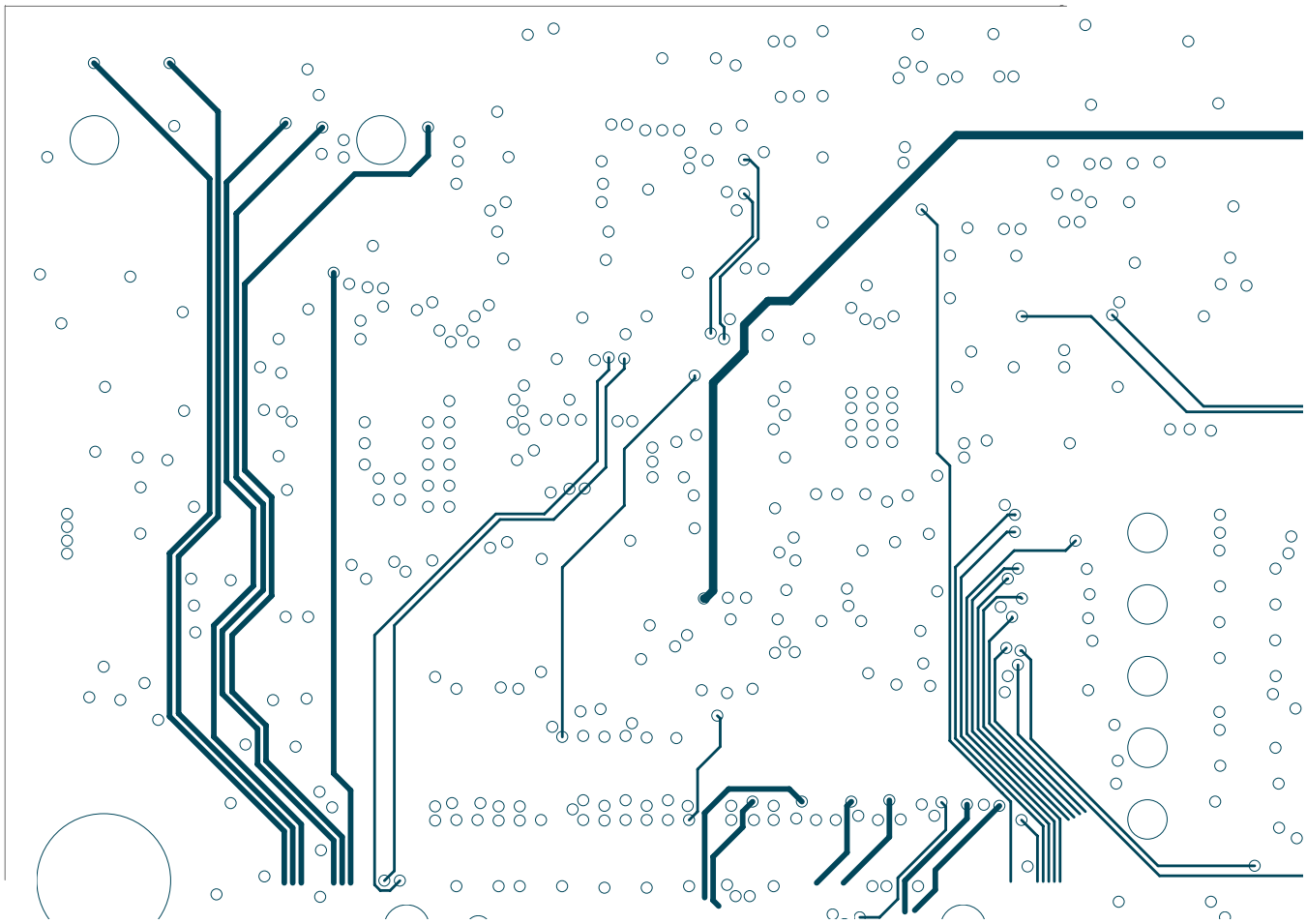

Figure 15. MC34704 Implementation Internal Layer 4

6.3.6 Bottom Layer

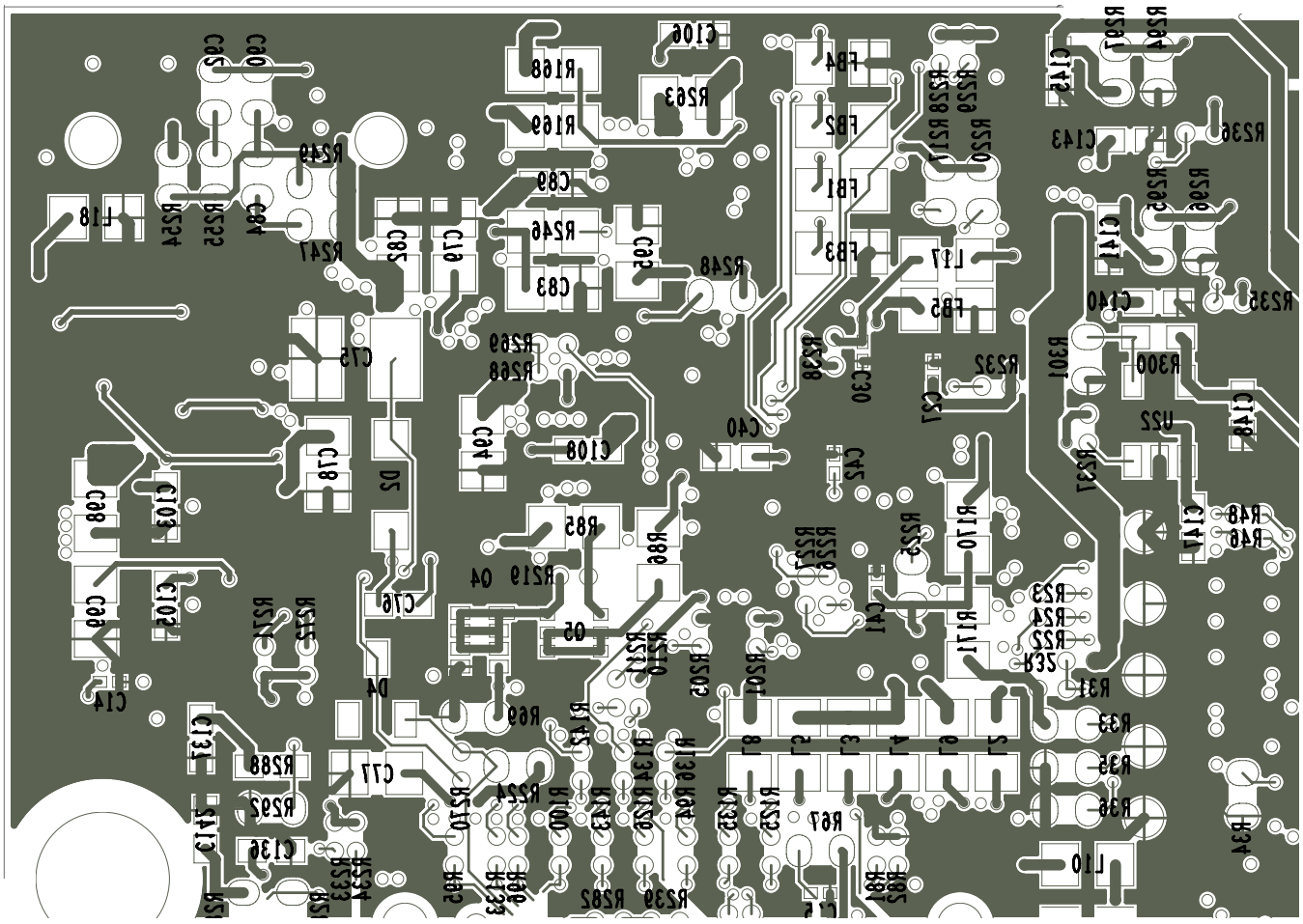

Figure 16. MC34704 Implementation Bottom Layer

6.3.7 All layers combination

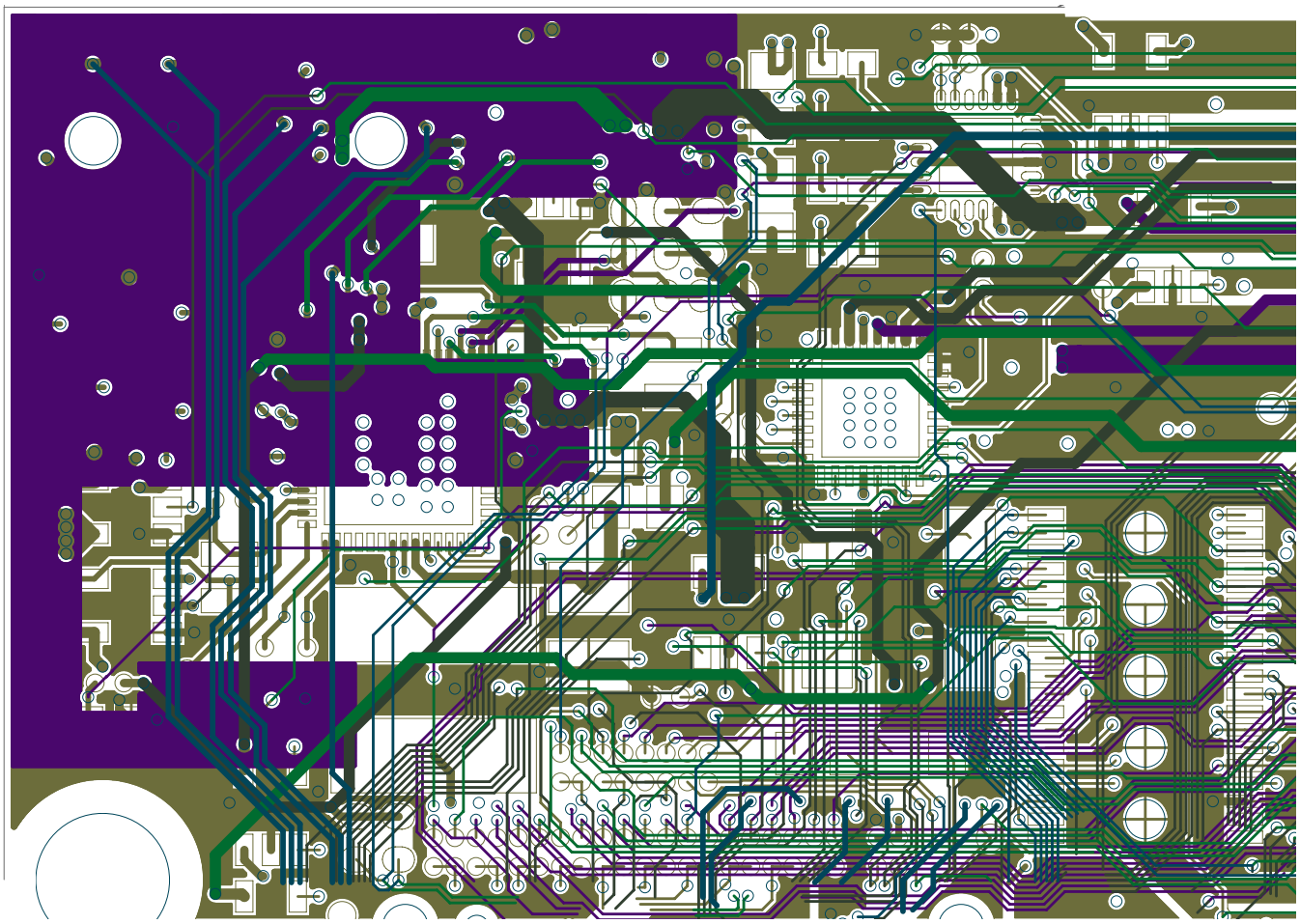

Figure 17. MC34708 All Layers Displayed

6.4 Layout Consideration

- Create a ground plane layer and tie it to ground signals with vias.
- Place test vias as close to the IC as possible, to ensure a good measurement values.
- P_{VIN}, V_{IN}, and V_{OUT} signals have to be tracked with a wide and straight copper area.
- Never trace the feedback signal in parallel to the SW signal.
- Ensure the SW inductor is placed as close to its pads as possible.
- The SW track must be as thin and short as possible.
- Make sure the I/O connectors are capable of managing the load current.

7 Bill of Material

Table 3. Simplified Bill of Material

Reference	Quantity	Part	Description[(1)]
C14	1	0.1 µF	CAP CER 0.1 µF 6.3 V 10% X5R 0201
C29, C96, C97, C100	4	0.01 µF	CAP CER 0.01 µF 25 V 10% X7R 0402
C74, C75	2	47 µF	CAP CER 47 µF 16 V 10% X5R 1210
C76, C80, C81, C85, C86, C107, C108, C146	8	1.0 µF	CAP CER 1.0 µF 25 V 10% X7R 0603
C77, C78, C79, C94, C95	5	10.0 µF	CAP CER 10 µF 16 V 10% X7R 0805
C82, C83, C98, C99	4	22 µF	CAP CER 22 µF 6.3 V 10% X5R 0805
C84, C87	2	68 PF	CAP CER 68 PF 50 V 5% C0G 0603
C90, C91	2	10 PF	CAP CER 10 PF 50 V 1% C0G 0603
C92, C93	2	1000 PF	CAP CER 1000 PF 25 V 5% C0G CC0603
C101	1	120 PF	CAP CER 120 PF 50 V 5% C0G 0603
C102	1	5.0 PF	CAP CER 5.0 PF 50 V 0.25 PF C0G 0805
C104	1	150 PF	CAP CER 150 PF 50 V 5% C0G 0603
C142	1	2.2 µF	CAP CER 2.2 µF 6.3 V 20% X5R 0402
D2	1	MBR120VLSFT1G	DIODE SCH RECT 1.0 A 20 V SMT
D3	1	GREEN	LED GREEN GAP ON GAP SM 0603
L11	1	3.0 µH	IND PWR 3.0 µH@10 KHZ 3.0 A 30% SMT
L12, L13, L14, L15	4	4.7 µH	IND PWR 4.7 µH@1.0 MHZ 1.2 A 20% SMT
R234, R268, R271, R272, R273, R274	6	10 K	RES MF 10 K 1/16 W 5% 0402
R247, R248	2	2.7 K	RES MF 2.70 K 1/10 W 1% 0603
R249, R251, R261	3	68 K	RES MF 68 K 1/10 W 1% 0603
R250	1	1.0 K	RES MF 1.0 K 1/16 W 1% 0402
R254, R257	2	15 K	RES MF 15.0 K 1/10 W 1% 0603
R255, R256	2	33.0 K	RES MF 33 K 1/10 W 1% 0603
R259	1	680 OHM	RES MF 680 OHM 1/10 W 1% 0603
R266	1	34.0 K	RES MF 34.0 K 1/10 W 1% 0603
R267	1	62.0 K	RES MF 62.0 K 1/10 W 1% 0603
R285	1	4.99 K	RES MF 4.99 K 1/10 W 1% 0603

Table 3. Simplified Bill of Material

Reference	Quantity	Part	Description[1]
R287, R298	2	18 K	RES MF 18.0 K 1/10 W 1% 0603
R302	1	12.7 K	RES MF 12.7 K 1/10 W 1% 0603
U10	1	MC34704	IC LIN DCDC PWR SWT 2.0 MHZ 2.7-5.5 V QFN56
U18	1	RT9179[1]	IC VREG LDO ADJ 1.175-4.5 V 300 MA 3-5.5 V SOT-23-5

Notes:

1. Freescale does not assume liability, endorse, or warrant components from external manufacturers referenced in drawings or tables. While Freescale offers component recommendations, it is the customer's responsibility to validate their application.

8 References

1. MC34704 data sheet MC34704
2. i.MX25 data sheet
3. i.MX25 PDK

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to http://www.freescale.com/epp.

AN3820
Rev. 1.0
3/2009

freescale™ semiconductor