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Application Note

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Time Domain Based Active Power Calculation

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Contents

1 Introduction

This application note describes the active energy calculation method used for single phase power meter based on the 8-bit microcontroller. It will discuss:

- The mathematical background for energy calculation in the time domain
- Different phenomena affecting calculation accuracy and how to deal with them
- The calculation algorithm used in the power meter by *LH60 Single Phase Power Meter Reference Design* (DRM133)

The described calculation method is suitable for active energy calculation for power meters compliant with EN50470.

Active energy calculation method is suitable for power meters which are suitable to measure (5)60A current range with B class accuracy.

2 Basic Math

2.1 Active, reactive, apparent, and total apparent power

Active power calculation in electric systems are easy to implement, but there are some topics worth discussing, starting with some background math.

Active power [W] is equal to voltage multiplied by the working component of the current:

$$P = \frac{1}{nT}\int_0^{nT} u(t)i(t)dt$$

Figure 1. Equation 1

Reactive power [VAR] is equal to the voltage multiplied by the magnetizing (reactive) current:

$$Q = \frac{1}{nT}\int_0^{nT} u(t-90°)i(t)dt$$

Figure 2. Equation 2

Apparent power [VA] is equal to the vector sum of active and reactive power, otherwise known as the triangle method, as shown in Figure 4.

$$S = \sqrt{P^2 + Q^2}$$

Figure 3. Equation 3

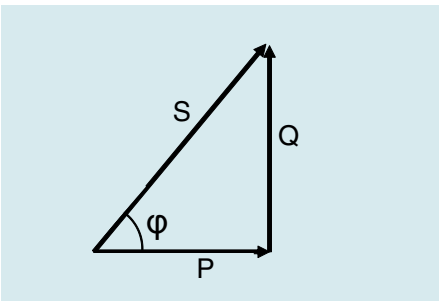

Figure 4. Apparent power calculation – triangle method

Total apparent power is the product of the RMS voltage and RMS current:

$$S_{tot} = U_{RMS} \times I_{RMS}$$

Figure 5. Total apparent power

In a pure sinusoidal system with no higher harmonics, the apparent power is equal to total apparent power. After harmonics are encountered in the system, then vector sum loose accuracy.

Active energy is the sum of active power in time:

$$E_P = P \times T$$

Figure 6. Equation 4

$$E_P = \int_0^{\infty} u(t)i(t)dt$$

Figure 7. Equation 5

Reactive energy is the sum of reactive power in time:

$$E_Q = Q \times T$$

Figure 8. Equation 6

$$E_Q = \int_0^{\infty} u(t - 90°) i(t) \mathrm{dt}$$

Figure 9. Equation 7

While the theory is now clear, there are some differences in real system situations. Due to various factors, we are not working with accurate voltage and current signals u(t) and i(t).

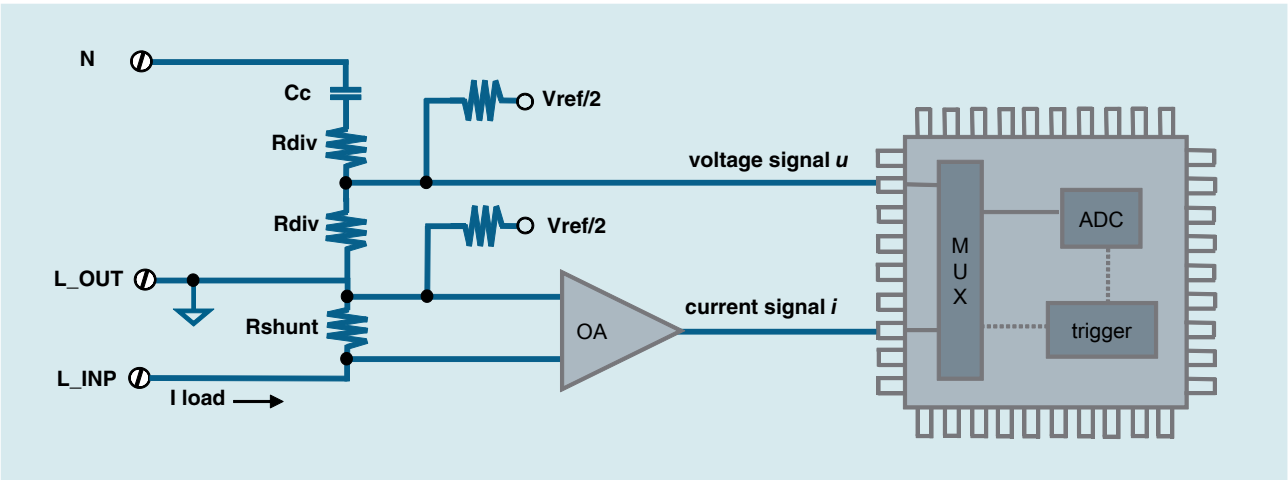

Figure 10. Voltage and current conditional circuits and connection to the MCU

The signal measured by the ADC is influenced by many errors. For simplicity, we omit error variation during temperature, aging, and so on here. The dominant errors in power meter signal condition circuits are signal offset, signal gain, and phase shift. Equations for real life voltage and current signals can be stated as follows:

$$i(t) = I_0 + G_i i \sin\left(\omega t + \varphi_{ie}\right)$$

Figure 11. Equation 8

$$u(t) = U_0 + G_u u \sin\left(\omega t + \varphi_{ue} + \varphi_{Cc}\right)$$

Figure 12. Equation 9

Where:

- i(t), u(t) - signal equivalent to current and voltage which is sampled by ADC
- I_0, U_0 - offset error , typically caused on signal biasing error (Vref/2), thermal offset of operational amplifier (OA), AD converter offset, resistors thermal shift
- G_i, G_u – gain error, usually due to OA gain error due to component variation and thermal shift, AD converter gain error, reference error. For our purposes, the gain error also includes signal “scaling factor”.
- φ_{Cc} – phase error introduced on Compensation capacitor (Cc)
- φ_{ie} , φ_{ue} – phase error due to shunt resistor impedance, time lag in OA, parasitic impedances on the resistors used

If we put real voltage and current signals to Figure 1 and derive it, the result is much more complex and dependent on other parasitic parameters, like offset and phase error.

$$P = \frac{1}{nT}\int_0^{nT} u(t)i(t)dt = \frac{1}{nT}\int_0^{nT}\left(U_0 + G_u u\sin\left(\omega t + \varphi_{Cc} + \varphi_{ue}\right)\right) \times \left(I_0 + G_i i\sin\left(\omega t + \varphi_{ie}\right)\right)dt$$

Figure 13. Equation 10

$$P = \frac{1}{nT}\int_0^{nT} U_0 I_0 + U_0 G_i i\sin\left(\omega t + \varphi_e\right) + I_0 G_u u\sin\left(\omega t + \varphi_{Cc} + \varphi_{ue}\right) + G_i i\sin\left(\omega t + \varphi_e\right) G_u u\sin\left(\omega t + \varphi_{Cc} + \varphi_{ue}\right)dt$$

Figure 14. Equation 11

As shown in Figure 13, offset and phase error must be removed to get a correct power value. The following assumptions can be made:

1. Mains voltage has $u_{mean} = 0$ by nature, therefore we can determine and remove voltage signal offset U_0 , so that the resulting signal has U_0=0. Signal offset is equal to signal mean value.
2. Actual active power is calculated on sine-wave borders where the following, Figure 15, is true:

$$\int_0^T u\sin(\omega t)dt = 0$$

Figure 15. Equation 12

Using previous assumptions, we can simplify Figure 14 to the following form:

$$P = \frac{1}{nT}\int_0^{nT} G_i i\sin\left(\omega t + \varphi_e\right) G_u u\sin\left(\omega t + \varphi_{Cc} + \varphi_{ue}\right)dt$$

Figure 16. Equation 13

We can start the calculation on the signal phase of our choice, therefore we can do the following:

- Subtract φ_{ie} from both signals, the frequency is the same
- Use $\varphi_e = \varphi_{ue} + \varphi_{Cc} - \varphi_{ie}$
- Substitute the gain factor $G = G_I * G_U$

$$P = G\frac{1}{nT}\int_0^{nT} i\sin(\omega t) u\sin\left(\omega t + \varphi_e\right)dt$$

Figure 17. Equation 14

In the calculation method proposed above, we must make the following assumptions to reach an accurate power and consecutively energy value:

- The voltage signal offset U_0 must be determined and then removed from signal samples to have $u_{mean} = 0$
- Phase error φ_e must be compensated
- Instantaneous power oscillates around its accurate value, and provides accurate value only on waveform border:

$$\int_0^T u\sin(\omega t)dt = 0$$

- Gain and scaling factors G must be set during calibration

2.2 Basic math – discrete form

In discrete form, we can rewrite Figure 17 using the same assumptions as in Active, reactive, apparent, and total apparent power. Power is the sum of products of voltage and current samples scaled to accurate value using gain factor G.

$$P = G\sum_{k=1}^{n} u_k i_k$$

Figure 18. Equation 15

$$E = \sum P$$

Figure 19. Equation 16

Samples u_k, i_k must have offset and phase error removed. Energy is then the endless sum of power.

3 Active Power Accuracy Affecting Phenomena

3.1 Sampling frequency

Figure 15 shows that power calculation is accurate only on the waveform border. Otherwise, instantaneous active power value oscillates around its real value. In the discrete calculation, the sampling window must be aligned to the mains sine wave. This leads the calculation algorithm to use variable sampling rate to have sampling frequency as multiples of the actual mains frequency. In our design, we have 64 samples per one mains sine wave. Therefore, the sampling frequency is 3200 samples/sec for 50 Hz mains frequency and changes as mains vary around 50 Hz.

We also synchronize sampling window to the mains sine wave phase, so the sampling window starts on 90° or 270°. Then we can halve the sine wave into two intervals which also fulfills the assumption of Figure 15.

$$\int_{-90^\circ}^{90^\circ} u\sin(\omega t)dt = 0$$

Figure 20. Equation 17

$$\int_{90^\circ}^{-90^\circ} u\sin(\omega t)dt = 0$$

Figure 21. Equation 18

3.2 Zero cross detection

Sampling frequency must be synchronized with frequency of the mains as treated in the previous section. The mains voltage signal is compared against a certain level on the comparator. The comparator output provides a signal whose edges are measured, and time information is used for ASC sampling frequency control. This ensures that the sampling window is aligned with the mains voltage signal.

3.3 Variable type used

The platform (core) used must also be considered based on:

- Its computational power
- Influence to the choose algorithm for active power calculation
- How many bits must be used in calculation to maintain accuracy over the required dynamic range

This application note describes active power calculation on an 8-bit platform, so the native variable length is 8 bits. Using wider variables increases the computationL power needed for arithmetic operations, which results in a higher CPU load, therefore using adequate variable length is essential. The AD converter provides 16-bit long result, so by multiplying current and voltage, we have a 32-bit wide result. If we multiply the 32-bit result with the 16-bit wide gain factor G, the result will be 48 bits, a length which is not supported in the C compiler. We must find a scale factor and keep the variables used for calculation in a reasonable format.

Here we are referring to 230 V at 5(60)B power meter and from the following table we see the current signal dynamic range where we have to provide accurate power calculation:

Table 1. Power meter dynamic range

	Istart	Imin	Itransition	Ireference	Imax
Current [A]	0.02	0.25	0.5	5	60
Accuracy [%]	One pulse in 30 min	1.5	1	1	1

The dynamic range needed with 1.5% accuracy for a worst case scenario is 60:0.25 = 240:1. But if we want to have, for example, approximately 2% accuracy for Istart, where dynamic range is 60:0.02 -> 3000:1, which is not mandatory by regulations, we need at least 6 bits for beginning -> 32*3000 = 96000 -> approximately 17 bits. This leads to a 24-bit wide variable to work with for active power calculation.

Although C compilers for an 8-bit core support only 16- or 32-bit long variables, it can be useful to build your own 24-bit long math libraries to lower the CPU load. Optimized ASM mathematic routines may also be more effective. For the algorithm, we must consider that if we use a high sampling frequency, calculation may eat significant CPU power only for energy calculation.

Table 2 shows the CPU cycles needed for 16- and 32-bit standard C library multiplication, 32*32 to 64 bit assembly-optimized function, and CPU load related for 3200 multiplications per second, which is actual power meter ADC sampling rate. CPU is running 19.2 MHz bus clock.

Table 2. CPU load for various mathematic routines

19.92 MHz CPU @ 3200 samples/s	Cycles / multiplication	Cycles / sec @ 3200	CPU load [%]
16*16 -> 16 @ C lib	220	704000	~3.5
32*32 -> 32 @ C lib	620	1984000	~10
32*32->64 @ASM optimized	635	2032000	~10.2
32+32-> @ 32 C lib	229	732800	~3.6

Table 2 shows that just one simple multiplication may take around 10% of CPU power, therefore we have to write code cautiously. A twice as wide calculation by optimized ASM routine may take a similar length of time as 32*32->32.

3.4 Calculation granularity

Computational power can also be saved by higher power calculation granularity, which is how often the active power is calculated and energy counters / LED pulse output are updated.

1. Figure 18 shows that gain factor G is multiplied with sum each n samples. We can determine optimal value n when the sum of product of samples of voltage and current is multiplied with gain factor G. We can theoretically choose a value from interval <1, ∞>. In this case, a larger n value leads to a lower CPU load. Choosing n=1 will lead to high CPU load, while energy counters will not be updated when n = ∞ .

$$P = G\sum_{k=1}^{n} u_k i_k$$

2. Figure 15 shows that a suitable value of n may be on the borders of the sine wave to fulfill the assumption. The sampling rate used in *LH60 Single Phase Power Meter Reference Design* (DRM133) gives us 64 samples per sine wave, which makes n = 64 a good option.

$$\int_0^T u\sin(\omega t)dt = 0$$

3. Calculation granularity also affects the time of periodic energy counter update and related power LED pulse jitter. The LED pulse output was used for accuracy testing previously. The n=64 interval means that the LED output is updated every 20 mS in the worst case signal jitter scenario. If the desired power meter accuracy step is 0.1%, we must measure for at least 20 seconds to negate jitter error. Finally, we proposed n = 32 with related half wave measure interval wherethe assumptions of Figure 20 and Figure 21 are fulfilled as well.

Half sine wave granularity n=32 for power and energy calculation is the optimal compromise of CPU computational power demand and power pulse LED signal jitter.

3.5 Offset removal

To remove signal offset, there are many aspects we must consider. Offset may be removed using special hardware to have a signal without offset error. A software-based solution such as applying a high-pass filter, or simply subtracting fixed offset U_{mean} from the signal can also be used. U_{mean} can also be determined from voltage signal samples.

Because of the cost of hardware solutions, we will deal only with software methods of removing offset.

3.5.1 High pass filter

IIR high pass filter is one option for removing offset from the voltage signal. Let's try to implement a simple first order filter with a -3 dB cutoff frequency of 0.15 Hz and sampling frequency 3200 s/sec. Such a filter has the following parameters:

$$y_n = b_1 \times x_n + b_2 \times x_{n-1} - a \times y_{n-1}$$

$$b_1 = 0.99968593938936,\ b_2 = -0.99968593938936,\ a = -0.999371878778719$$

$$y_n = 0.99968593938936 \times x_n - 0.99968593938936 \times x_{n-1} + 0.999371878778719 \times y_{n-1}$$

For the filter to work without significant errors for small signals, coefficients (a, b) and result y must be in 32-bit arithmetic. This leads to the two multiplications x*b and y*a [32*32->32] and two sum operations [32+32->32] for each sample. This leads to 1698 cycles per sample, which is the same as 30% of CPU computational power. We must filter both current and voltage samples to make the total CPU load 60% for offset removal only.

Using ASM and making some changes, we can get lower CPU load, but still it is not an acceptable CPU load. Therefore, using an FIR filter on 8-bit core is not optimal for 3200 samples/sec.

3.5.2 Fixed value subtraction

We can also subtract a fixed value from each sample. The fixed value can be determined during the calibration process. This method is sensitive to the thermal input offset drift on operational amplifier and causes significant errors.

3.5.3 Signal mean value calculation and removal

Determining signal mean value U_{mean} and subtracting this value from the incoming samples is the proposed for removing offset in the actual design. For the harmonic voltage signal, we know from Figure 15 that we expect mean value to be zero on the waveform border.

$$\int_0^T u\sin(\omega t)dt = 0$$

On real samples, we get a non-zero value over sine wave period, which is equivalent to mean value. In design, we typically average this value over several seconds. As a result, we have the voltage mean value, which is subtracted from incoming samples.

This method provides a precise, adaptive method for removing offset together with light CPU load.

3.6 Phase error correction

For Figure 17, we must have voltage and current signals phase-aligned. This means that for pure active load, both the voltage and current signal and its samples must have zero phase shift. In real application, both signals have phase errors as shown in Figure 11 and Figure 12.

However, the LH64 only has asingle AD converter, therefore we cannot sample voltage and current signal simultaneously. See Figure 22 to see the time lag (tl) between the voltage and current sample.

The tl between two samples of current and voltage in time domain may be transformed to signal phase shift in frequency domain. For example, 1.8 degree equals approximately 100 us for a 50 Hz signal.

The tl between voltage and current signal sample may be used to remove phase error φ_{ue}, φ_{ie} in Figure 16.

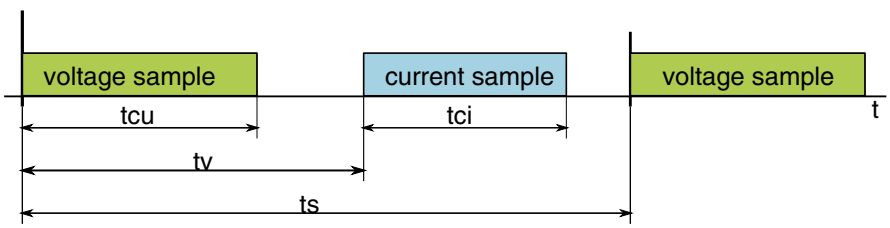

Figure 22. ADC current and voltage samples

The ADC sampling time is approximately 100 uS for voltage sample “tcu” which equals approximately 1.8 degree at 50 Hz. Therefore, the current signal has to be shifted by at least 1.8 degrees to be sampled in correct time/phase. Signal errors φ_{ue}, φ_{ie} are much smaller than 1.8 degree, therefore we can add an additional phase shift on capacitor C in the voltage signal to increase the time between the sample of voltage and current to the level acceptable by the AD converter. For the path, see Figure 23.

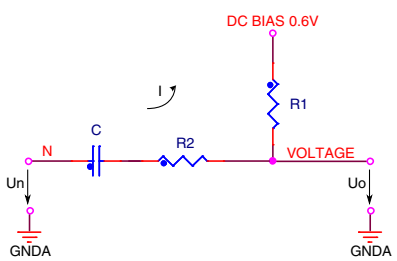

Figure 23. Voltage conditional circuit schematic

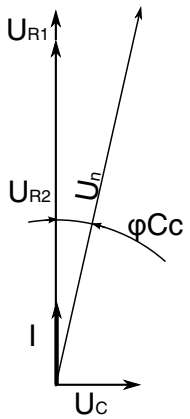

Figure 24. Voltage conditional circuit phasor

By controlling tl time via software, we can then compensate phase error between signals of voltage and current.

4 Calculation Flow Diagram

Now we can see the actual active power calculation diagram used in the *LH60 Single Phase Power Meter Reference Design* (DRM133). In the following diagram, we calculate more parameters, such as RMS voltage, RMS current, and reactive power. However, those parameters calculation are out of scope of this document.

Steps 1 and 2 on the calculation diagram in Figure 25 are performed with each incoming sample, so each is approximately 312 µs. At the beginning, we have two 16-bit samples, unsigned voltage sample and signed current sample:

- We subtract offsets from both voltage and current samples. Voltage sample is transformed to signed.
- Voltage and current samples are summed 64 times – one complete sine wave for following offsets calculation.
- Urms value calculation is done on the upper 8 bits of the voltage sample. We throw away the lower 8 bits to lower the CPU load, square it, and accumulate for 32 samples – half sine wave.
- Voltage and current samples are multiplied and accumulated 32 times – therefore our calculation granularity is ½ of the sine wave, approximately 10 ms at 50 Hz.
- Voltage samples are derivative and the result is multiplied with current signal sample and summed 32 times to get reactive power. Reactive power is used only for informative readings and does not need to be accurate.

Steps 3-6 are performed over 32 samples, so every 10 mS.

- Voltage and current offset value is either increased or decreased depending on its polarity. This controls offset value on the level, ensuring that the correct offset is removed from the voltage and current sample.
- For active/reactive power calculation, we subtract and save the lowest 16 bits to lower the actual value range. Then, depending on the psFiltOn variable state, 32-taps average filter is applied to smooth instantaneous power variation.
- Step calibration is done in the following step. We typically apply gain G on the signal. Gain is set during calibration process. We can also apply offset value to power, if needed.
- The signal out of the filter is adjusted by the factor of actual sampling rate, to compensate for sampling rate variation, and added to the energy counter and energy pulse generator.
- Power samples are summed approximately a hundred times a second for energy showed on the display.
- Urms value is summed over one second.

Steps 7-10 are performed once per second and are referred to values showed on the display:

- Depending on the pdFiltOn variable, active and reactive power samples are averaged on the four taps average filter.
- Active and reactive power values are updated on the display.
- Apparent power is calculated using the triangle method from active and reactive power.

- Urms value is also calibrated and updated on the display.
- Irms value is determined based on apparent power and Urms, and updated on the display.

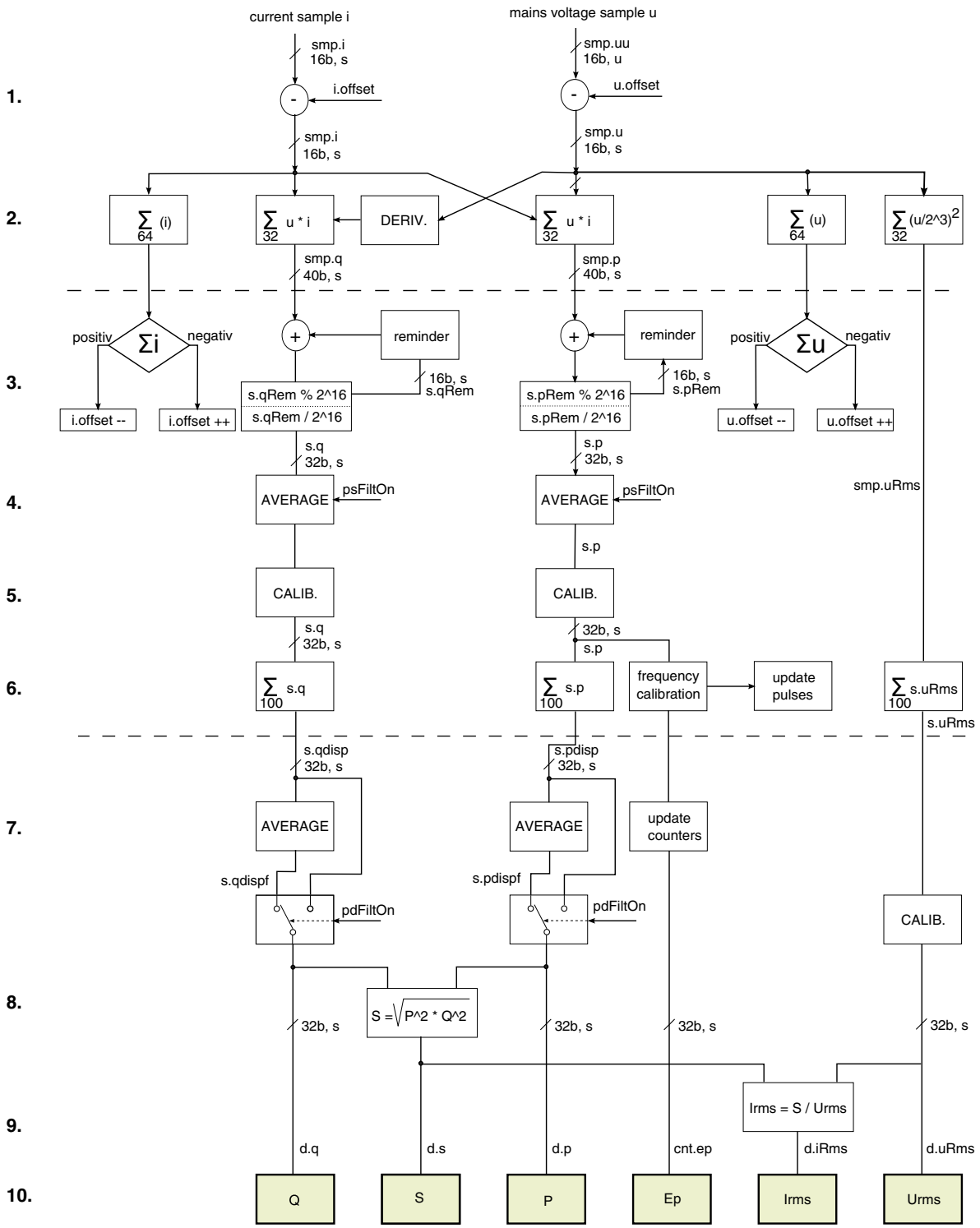

Figure 25. Active power calculation

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