Freescale Semiconductor
Application Note

AN3962
Rev. 2.0, 8/2010

PCB Layout Design Guide for Analog Applications

By: Edward Lee, Rafael Garcia Mora

1 Purpose

PCB Layout design is essential to better performance, reliability and manufacturability. Malfunctions from poor heat dissipation and noise, which may hurt the system stability, have become an increasing problem, and may therefore generate more failures and reliability malfunctions in production lines.

In this document, several considerations and guidelines for PCB layout design are discussed for better performance, reliability, and manufacturability.

2 Scope

This document discusses basics for layout, regulations, methods of noise isolation, and thermal considerations.

Contents

freescale™ semiconductor

3 General Design Guides

Producibility is related to the complexity of the design, and the specific printed board or printed board assembly. There are three producibility levels:

- Class 1: General Electronic Products
- Class 2: Dedicated Service Electronic Products
- Class 3: High Reliability Electronic Product

Class 1 products include consumer products, computers and their peripherals, and general military hardware. Class 2 products include communication equipment, sophisticated business machines, instruments and military equipment. Class 3 products include the equipment for commercial and military applications, where continued performance, or performance on demand is critical.

The complexity levels are specified as:

- Level A: General Design Complexity (Preferred)
- Level B: Moderate Design Complexity (Standard)
- Level C: High Design Complexity (Reduced Producibility)

Table 1 shows the general layout guidance for different classes. (Class A: simple single level consumer products; Class B: complex and multilevel general industrial products; Class C: high reliability medical and military products)

Table 1. Composite Board Design Guidance

Guidance	Class A	Class B	Class C
Number of conductor layers (Maximum)	6.0	12	20
Thickness of the total board (Maximum)	2.5 mm (0.100 in)	3.8 mm (0.150 in)	5.0 mm (0.200 in)
Board thickness tolerance	± 10% above nominal or 0.18 mm (0.007 in), whichever is greater	± 10% above nominal or 0.18 mm (0.007 in), whichever is greater	± 10% above nominal or 0.18 mm (0.007 in), whichever is greater
Thickness of dielectric (Minimum)	0.2 mm (0.008 in)	0.15 mm (0.006 in)	0.1 mm (0.004 in)
Minimum conductor width			
Internal	0.3 mm (0.012 in)	0.2 mm (0.008 in)	0.1 mm (0.004 in)
External	0.4 mm (0.016 in)	0.25 mm (0.010 in)	0.1 mm (0.004 in)
Conductor width tolerance			
Unplated 2.0 oz/ft^2	+0.1 mm (0.004 in) -0.15 mm (0.006 in)	+0.05 mm (0.002 in) -0.13 mm (0.005 in)	+0.025 mm (0.001 in) -0.08 mm (0.003 in)
Unplated 1.0 oz/ft^2	+0.05 mm (0.002 in) -0.08 mm (0.003 in)	+0.025 mm (0.001 in) -0.05 mm (0.002 in)	+0.025 mm (0.001 in) -0.025 mm (0.001 in)
Protective plated (metallic etch resist over 2.0 oz/ft^2 copper)	+0.20 mm (0.008 in) -0.15 mm (0.006 in)	+0.10 mm (0.004 in) -0.10 mm (0.004 in)	+0.05 mm (0.002 in) -0.05 mm (0.002 in)
Minimum conductor spacing	0.3 mm (0.012 in)	0.2 mm (0.008 in)	0.1 mm (0.004 in)
Annular ring plated-through hole (minimum)			
Internal	0.20 mm (0.008 in)	0.13 mm (0.005 in)	0.05 mm (0.002 in)
External	0.25 mm (0.010 in)	0.20 mm (0.008 in)	0.13 mm (0.005 in)
Feature location tolerance (master pattern, material movement, and registration) (diameter of true position)			
Up to 300 mm (12.0 in)	0.85 mm (0.034 in)	0.55 mm (0.022 in)	0.30 mm (0,012 in)
Up to 450 mm (18.0 in)	1.0 mm (0.040 in)	0.60 mm (0.024 in)	0.45 mm (0.018 in)
Up to 600 mm (24.0 in)	1.15 mm (0.046 in)	0.85 mm (0.034 in)	0.55 mm (0.022 in)

Table 1. Composite Board Design Guidance

Guidance	Class A	Class B	Class C
Master pattern accuracy			
• Feature location (diameter of true position)			
Up to 300 mm (12.0 in)	0.10 mm (0.004 in)	0.08 mm (0.003 in)	0.05 mm (0.002 in)
Up to 450 mm (18.0 in)	0.13 mm (0.005 in)	0.10 mm (0.004 in)	0.08 mm (0.003 in)
Up to 600 mm (24.0 in)	0.15 mm (0.006 in)	0.13 mm (0.005 in)	0.10 mm (0.004 in)
• Feature size tolerance	0.08 mm (0.003 in)	0.05 mm (0.002 in)	0.025 mm (0.001 in)
Board thickness to plated hole diameter (maximum)	3:1	6:1	10:1
Hole location tolerance (diameter of true position)			
Up to 300 mm (12.0 in)	0.40 mm (0.016 in)	0.30 mm (0.012 in)	0.10 mm (0.004 in)
Up to 450 mm (18.0 in)	0.50 mm (0.020 in)	0.40 mm (0.016 in)	0.20 mm (0.008 in)
Up to 600 mm (24.0 in)	0.6 mm (0.024 in)	0.50 mm (0.020 in)	0.30 mm (0.012 in)
Unplated hole diameter tolerance (unilateral)			
0.0 - 0.8 mm (0 - 0.032 in)	0.16 mm (0.006 in)	0.10 mm (0.004 in)	0.06 mm (0.002 in)
0.85 - 1.6 mm (0.033 - 0.063 in)	0.20 mm (0.008 in)	0.16 mm (0.008 in)	0.10 mm (0.004 in)
1.65 - 5.0 mm (0.064 -0.200 in)	0.30 mm (0.012 in)	0.20 mm (0.008 in)	0.16 mm (0.006 in)
Plated hole diameter tolerance (unilateral) for minimum hole diameter maximum board thickness ratios greater than 1:4 add 0.05 mm(0.002 in)			
0.0 - 0.8 mm (0 - 0.032 in)	0.20 mm (0.008 in)	0.16 mm (0.006 in)	0.10 mm (0.004 in)
0.85 - 1.6 mm (0.033 - 0.063 in)	0.30 mm (0.012 in)	0.20 mm (0.008 in)	0.10 mm (0.004 in)
1.65 - 5.0 mm (0.064 -0.200 in)	0.40 mm (0.016 in)	0.30 mm (0.012 in)	0.20 mm (0.008 in)
Conductor to edge of board (minimum)			
Internal layer	2.5 mm (0.100 in)	1.25 mm (0.050 in)	0.65 mm (0.025 in)
External layer	2.5 mm (0.100 in)	2.5 mm (0.100 in)	2.5 mm (0.100 in)

Notes

1.The number of conductor layers should be the optimum for the required board function and good producibility.

When considering the producibility of the PCB, there are certain guidelines for layout. For example, when drilling and plating through holes, there are limitations related to the hole size. Table 2, describes the recommended minimum hole size for plated through holes.

Table 2. Minimum Hole Size for Plated-Through Holes

Board Thickness	Class 1	Class 2	Class 3
<1.0 mm(0.040 in)	Level C 0.15 mm (0.006 in)	Level C 0.2 mm (0.008 in)	Level C 0.25 mm (0.010 in)
1.0 mm -> 1.6 mm (0.040 -> 0.063 in)	Level C 0.2 mm (0.008 in)	Level C 0.25 mm (0.010 in)	Level B 0.3 mm (0.012 in)
1.6 mm -> 2.0 mm (0.053 -> 0.080 in)	Level C 0.3 mm (0.012 in)	Level B 0.4 mm (0,016 in)	Level B 0.5 mm (0.020 in)
>2.0 mm(0.080 in)	Level B 0.4 mm (0.016 in)	Level A 0.5 mm (0.020 in)	Level A 0.6 mm (0.024 in)

Notes: If copper in the hole is greater than 0.03 mm(0.0012 in), the hole size can be reduced by one class

The component mounting of the layout also effects the reliability and the producibility of the board, so It is important to consider PCB flexing. To avoid cracking when the PCB is flexed, it's advantageous to place the components in a vertical direction of the longer direction of the PCB. See Figure 1.

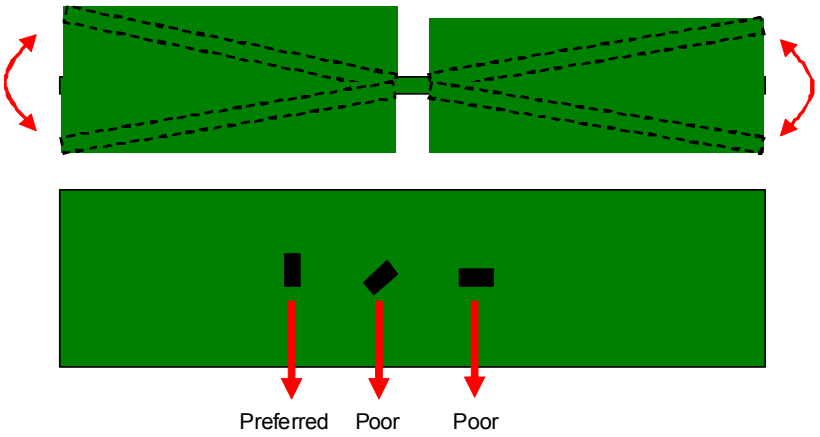

Figure 1. Component Mounting Direction

3.1 Minimum Trace Width

To calculate what minimum width is required to handle a certain amount of current, it requires several parameters, including the operating temp range, maximum current which will flow through the trace, copper thickness, etc. There is simple rule of thumb, which can be applied for most of the applications. For 1.0 oz/ft^2 of copper thickness, in most of the commercial applications, 1.0 mm/A is required as a minimum trace width.

3.2 Clearance in Primary Circuits

When considering the insulation distance between two traces (or components), it is important to understand the difference of clearance and the creepage distance. Figure 2 shows the definition of these two distances.

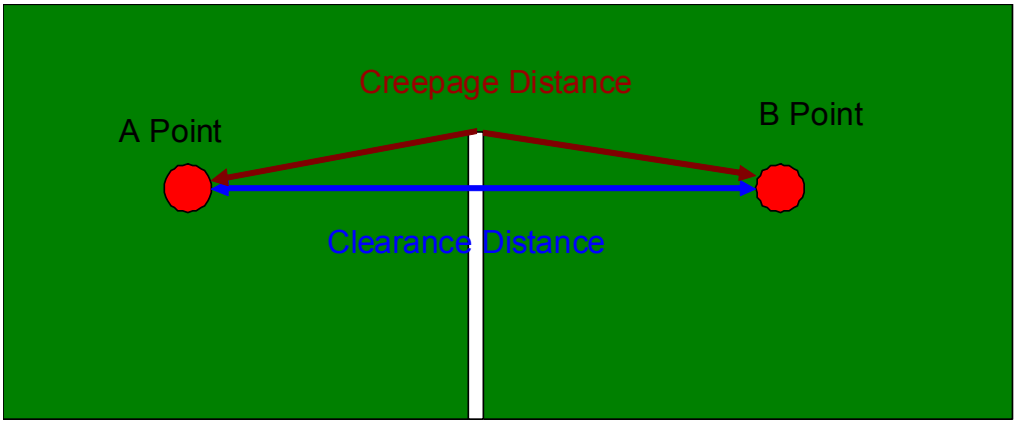

Figure 2. Clearance and Creepage Distance

Clearance distance is defined as the shortest distance through the air between two conductive elements. The creepage distence is defined as the shortest distance on the surface of an insulating material between two conductive elements. As shown in Figure 2, with a slit between two conductive points, the creepage distance is increased by detouring the slit.

Clearance in primary circuits must comply with the minimum dimension in Table 3, and where appropriate, Table 4. The relevant conditions in these tables must be considered.

Table 3. Minimum Clearances for Insulation in Primary Circuits, and Between Primary and Secondary Circuits (mm)

Circuits subject to Installation Category II																
Insulation working voltage up to and including		Nominal mains supply voltage ≤ 150 V (Transient rating 1500 V)						Nominal mains supply voltage > 150 V ≤ 300 V (Transient rating 2500 V)						Nominal mains supply voltage > 300 V ≤ 600 V (Transient rating 400 V)		
V peak or dc V	V rms (sinusoidal) V	Pollution degrees 1 and 2			Pollution degree 3			Pollution degrees 1 and 2			Pollution degree 3			Pollution degrees 1, 2, and 3		
		Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R
71	50	0.4	1.0 (0.5)	2.0 (1.0)	0.8	1.3 (0.8)	2.6 (1.6)	1.0	2.0 (1.5)	4.0 (3.0)	1.3	2.0 (1.5)	4.0 (3.0)	2.0	3.2 (3.0)	6.4 (6.0)
210	150	0.5	1.0 (0.5)	2.0 (1.0)	0.8	1.3 (0.8)	2.6 (1.6)	1.4	2.0 (1.5)	4.0 (3.0)	1.5	2.0 (1.5)	4.0 (3.0)	2.0	3.2 (3.0)	6.4 (6.0)
420	300	Op 1.5 B/S 2.0(1.5) R 4.0(3.0)												2.5	3.2 (3.0)	6.4 (6.0)
840	600	Op 3.0 B/S 3.2(3.0) R6.4(6.0)														
1,400	1.000	Op/B/S 4.2 R 6.4														

Table 3. Minimum Clearances for Insulation in Primary Circuits, and Between Primary and Secondary Circuits (mm)

Circuits subject to Installation Category II																	
Insulation working voltage up to and including		Nominal mains supply voltage ≤ 150 V (Transient rating 1500 V)						Nominal mains supply voltage > 150 V ≤ 300 V (Transient rating 2500 V)						Nominal mains supply voltage > 300 V ≤ 600 V (Transient rating 400 V)			
V peak or dc V	V rms (sinusoidal) V	Pollution degrees 1 and 2			Pollution degree 3			Pollution degrees 1 and 2			Pollution degree 3			Pollution degrees 1, 2, and 3			
		Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R	
2,800	2,000							Op/B/S/R 8.4									
7,000	5,000							Op/B/S/R 17.5									
9,800	7,000							Op/B/S/R 25									
14,000	10,000							Op/B/S/R 37									
28,000	20,000							Op/B/S/R 80									
42,000	30,000							Op/B/S/R 130									

Notes

2. This table is applicable to equipment that will not be subject to transients exceeding Installation Category II, according to IEC 664. The appropriate transient voltage ratings are given in parentheses at the top of each nominal mains supply voltage column. Where higher transients are possible, additional protection might be necessary on the mains supply, to the equipment or to the installation.
3. The values in the table are applicable to OPERATIONAL (Op), BASIC(B), SUPPLEMENTARY(S), and REINFORCED INSULATION (R).
4. The values in parentheses are applicable to BASIC, SUPPLEMENTARY, or REINFORCED INSULLATION, only if the manufacturing is subject to a quality control program that provides at least the same level of assurance as the example given in UL1950 annex R.2. In particular, DOUBLE and REINFORCED INSULLATION shall be subject to ROUTINE TESTING for electric strength.
5. All BASIC, SUPPLEMENTARY, and REINFORCED INSULLATION parts of the PRIMARY CIRCUIT are assumed to be at not less than the normal supply voltage, with respect to earth.
6. Linear interpolation is permitted between the nearest two points for WORKING VOLTAGES between 2,800 V and 42,000 V peak or dc, the calculated spacing being rounded up to the next higher 0.1 mm increment.
7. The CLEARANCE shall be not less than 10 mm, for an air gap serving as REINFORCED INSULATION between a part at a HAZARDOUS VOLTAGE, and an accessible conductive part of the ENCLOSURE of floor standing equipment, or the non-vertical top surface of desk top equipment.

Table 4. Additional Clearances for Insulation in Primary Circuits with Repetitive Peak Voltages Exceeding the Peak Value of the Mains Supply Voltage

Nominal mains supply voltage ≤ 150 V		Nominal mains supply voltage > 150V ≤ 300V	Additional clearance (mm)	
Pollution degrees 1 and 2	Pollution degree 3	Pollution degrees 1,2 and 3	Operational, basic or Supplementary insulation	Reinforced Insulation
Maximum repetitive peak voltage V	Maximum repetitive peak voltage V	Maximum repetitive peak voltage V		
210 (210)	210 (210)	420 (420)	0	0
298 (288)	294 (293)	493 (497)	0.1	0.2
386 (366)	379 (376)	567 (575)	0.2	0.4
474 (444)	463 (459)	640 (652)	0.3	0.6
562 (522)	547 (541)	713 (729)	0.4	0.8
650 (600)	632 (624)	787 (807)	0.5	1.0
738 (678)	716 (707)	860 (884)	0.6	1.2
826 (756)	800 (790)	933 (961)	0.7	1.4
914 (839)	-	1,006 (1,039)	0.8	1.6
1,002 (912)	-	1,080 (1,116)	0.9	1.8
1,090 (990)	-	1,153 (1,193)	1.0	2.0
-	-	1,226 (1,271)	1.1	2.2
-	-	1,300 (1,348)	1.2	2.4
-	-	- (1,425)	1.3	2.6

Notes: The values in parentheses in **Table 4.** shall be used 1) when the values in parentheses in **Table 3.** are used in accordance with note 3 of **Table 3.** and 2) for Operational Insulation.

3.3 Clearances in Secondary Circuits

Clearances in Secondary circuits shall meet the minimum dimension of Table 5. The relevant conditions in the table shall be taken into consideration.

Table 5. Minimum Clearance in Secondary Circuits (mm)

Insulation working voltage up to and including		Nominal mains supply voltage ≤ 150 V (maximum transient in secondary circuit 800 V, ref note 13)						Nominal mains supply voltage > 150 V, ≤ 300 V (Maximum transient in secondary circuit 1500 V, ref note 13)						Nominal mains supply > 300 V, ≤ 600 V (Maximum transient in secondary circuit 2500 V, ref note 13)			Circuits not subjected to transient overvoltage (ref note 11)		
V peak or dc V	V rms (sinusoidal) V	Pollution degrees 1 and 2			Pollution degree 3			Pollution degrees 1 and 2			Pollution degree 3			Pollution degrees 1,2, and 3			Pollution degrees 1 and 2		
		Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R
71	50	0.4 (0.2)	0.7 (0.2)	1.4 (0.4)	1.0 (0.8)	1.3 (0.8)	2.6 (1.6)	0.7 (0.5)	1.0 (0.5)	2.0 (1.0)	1.0 (0.8)	1.3 (0.8)	2.6 (1.6)	1.7 (1.5)	2.0 (1.5)	4.0 (3.0)	0.4 (0.2)	0.4 (0.2)	0.8 (0.4)
140	100	0.6 (0.2)	0.7 (0.2)	1.4 (0.4)	1.0 (0.8)	1.3 (0.8)	2.6 (1.6)	0.7 (0.5)	1.0 (0.5)	2.0 (1.0)	1.0 (0.8)	1.3 (0.8)	2.6 (1.6)	1.7 (1.5)	2.0 (1.5)	4.0 (3.0)	0.6 (0.2)	0.7 (0.2)	1.4 (0.4)
210	150	0.6 (0.2)	0.9 (0.2)	1.8 (0.8)	1.0 (0.8)	1.3 (0.8)	2.6 (1.6)	0.7 (0.5)	1.0 (0.5)	2.0 (1.0)	1.0 (0.8)	1.3 (0.8)	2.6 (1.6)	1.7 (1.5)	2.0 (1.5)	4.0 (3.0)	0.6 (0.2)	0.7 (0.2)	1.4 (0.4)
280	200	Op 1.1(0.8), B/S 1.4 (0.8), R 2.8 (1.6)												1.7 (1.5)	2.0 (1.5)	4.0 (3.0)	1.1 (0.2)	1.1 (0.2)	2.2 (0.4)
420	300	Op 1.6 (1.0), B/S 1.9 (1.0), R 3.8 (2.0)												1.7 (1.5)	2.0 (1.5)	4.0 (3.0)	1.4 (0.2)	1.4 (0.2)	2.8 (0.4)
700	500	Op/B/S 2.5 R 5.0																	
840	600	Op/B/S 3.2 R 5.0																	
1,400	1,000	Op/B/S 4.2 R 5.0																	
2,800	2,000	Op/B/S/R 8.4																	
7,000	5,000	Op/B/S/R 17.5																	
9,800	7,000	Op/B/S/R 25																	
14,000	10,000	Op/B/S/R 37																	
28,000	20,000	Op/B/S/R 80																	
42,000	30,000	Op/B/S/R 130																	

Table 5. Minimum Clearance in Secondary Circuits (mm)

Insulation working voltage up to and including		Nominal mains supply voltage ≤ 150 V (maximum transient in secondary circuit 800 V, ref note 13)						Nominal mains supply voltage > 150 V, ≤ 300 V (Maximum transient in secondary circuit 1500 V, ref note 13)						Nominal mains supply > 300 V, ≤ 600 V (Maximum transient in secondary circuit 2500 V, ref note 13)			Circuits not subjected to transient overvoltage (ref note 11)		
V peak or dc V	V rms (sinusoidal) V	Pollution degrees 1 and 2			Pollution degree 3			Pollution degrees 1 and 2			Pollution degree 3			Pollution degrees 1,2, and 3			Pollution degrees 1 and 2		
		Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R	Op	B/S	R

Notes

8. The values in the table are applicable to OPERATIONAL (Op), BASIC (B), SUPPLEMENTRARY(S), REINFORCED (R) insulation
9. The values in parentheses are applicable to BASIC, SUPPLEMENTARY, or REINFORCED insulation only if manufacturing is subject to a quality control program that provides at least the same level of assurance as the example given in UL1950 annex R.2. In particular, the DOUBLE and REINFORCED insulation shall be subject to routine testing for electric strength.
10. The calculated spacing being rounded up to the next higher 0.1 mm increment for a working voltage between 2,800 V and 42,000 V peak or DC, linear interpolation is permitted between the nearest two points.
11. The values are applicable to DC secondary circuits which are reliably connected to earth and have capacitive filtering which limits the peak to peak ripple to 10% of the DC voltage.
12. Reserved for future use.
13. Where transients in the equipment exceed this value, the appropriate higher clearance shall be used.
14. The clearance shall be not less than 10 mm for an air gap serving as reinforced insulation between a part at a hazardous voltage, and an accessible conductive part of the enclosure of floor standing equipment, or of the non-vertical top surface of desk top equipment.
15. Compliance with a clearance value of 8.4 mm or greater is not required, if the insulation involved passes an electric strength test.

3.4 Creepage Distances

Creepage distances shall be not less than the appropriate minimum values specified in Table 6.

Table 6. Minimum Creepage Distances (mm)

Working voltage up to and including V_{RMS} or DC	Operational, Basic, and Supplementary Insulation							
	Pollution degree 1	Pollution degree 2			Pollution degree 3			
	Material group	Material group			Material group			
	I,II,IIIa+IIIb	I	II	IIIa + IIIb	I	II	IIIa + IIIb	
50	Use the appropriate CLEARANCE from Table 3 or Table 5	0.6	0.9	1.2	1.5	1.7	1.9	
100		0.7	1.0	1.4	1.8	2.0	2.2	
125		0.8	1.1	1.5	1.9	2.1	2.4	
150		0.8	1.1	1.6	2.0	2.2	2.5	
200		1.0	1.4	2.0	2.5	2.8	3.2	
250		1.3	1.8	2.5	3.2	3.6	4.0	
300		1.6	2.2	3.2	4.0	4.5	5.0	
400		2.0	2.8	4.0	5.0	5.6	6.3	
600		3.2	4.5	6.3	8.0	9.6	10.0	
1,000		5.0	7.1	10.0	12.5	14.0	16.0	

Table 6. Minimum Creepage Distances (mm)

Working voltage up to and including V_{RMS} or DC	Operational, Basic, and Supplementary Insulation						
	Pollution degree 1	Pollution degree 2			Pollution degree 3		
	Material group	Material group			Material group		
	I,II,IIIa+IIIb	I	II	IIIa + IIIb	I	II	IIIa + IIIb

Notes

16. The values for creepage distances for REINFORCED Insulation are twice the values in the table for BASIC insulation.
17. If the creepage distance derived from Table 6 is less than the applicable clearance from Table 3, Table 4, and Table 5, as appropriate, then the value for that clearance shall be applied as the value for the minimum creepage distance.
18. Material group I 600 ≤ CTI (Comparative tracking index)
19. Material group II 400 ≤ CTI < 600
20. Material group IIIa 175 ≤ CTI < 400
21. Material group IIIb 100 ≤ CTI < 175
22. The CTI rating refers to the value obtained in accordance with method A of IEC 112.
23. Where the material group is not known, material group IIIb shall be assumed.
24. Reserved for future use
25. It is permitted to use minimum creepage distances equal to the applicable clearances for glass, mica, ceramic, or similar materials.
26. Linear interpolation is permitted between the nearest two points, the calculated spacing being rounded to the next higher 0.1 mm increment

4 Power Ground Separation (Noise Isolation)

If there is a PCB with zero ohm impedance, no consideration for the noise coupling caused by the common impedance and the current which flows through it is needed. It is not possible for real applications to make a zero ohm trace, or to reduce the impedance to a negligible level.

Trace impedance becomes troublesome for analog engineers when designing the layout which handles huge switching current in analog applications.

The resistance of the PCB trace can be calculated by following formula.

$$R = 1.7e{-}6 \times L/A \div (1 + (3.9e - 3 \times (T - 25)))Ohms$$

Copper Resistivity: 1.7e-6 Ohm*cm

Copper Temp_Co: 3.9e-3 /°C

For 1.0 oz/ft^2 copper (35 μm thickness copper), 1.0 mm width trace, the resistance would be around 12.3 mOhm/inch at 25°C.

In addition, it is difficult to provide enough layers due to the cost of the PCB. Generally, a single sided printed board price is about $0.2 x /inch^2, a double sided printed board price is about $1.0 x/inch^2, and a multi-layered (7-layer) printed board price is about $5.0 x/inch^2. There should always be an adequate number of layers available. It is important to design the PCB layout for noise isolation within a limited number of layers.

The main purpose of the separation between power ground and signal ground is to prevent the high voltage ripples caused by high current flow in the power path from spreading into the sensitive analog blocks.

Ground pin of C_{OUT} in Figure 3, will have a voltage ripple generated by I_{SW}, I_D, or IL, and the resistance of the trace.

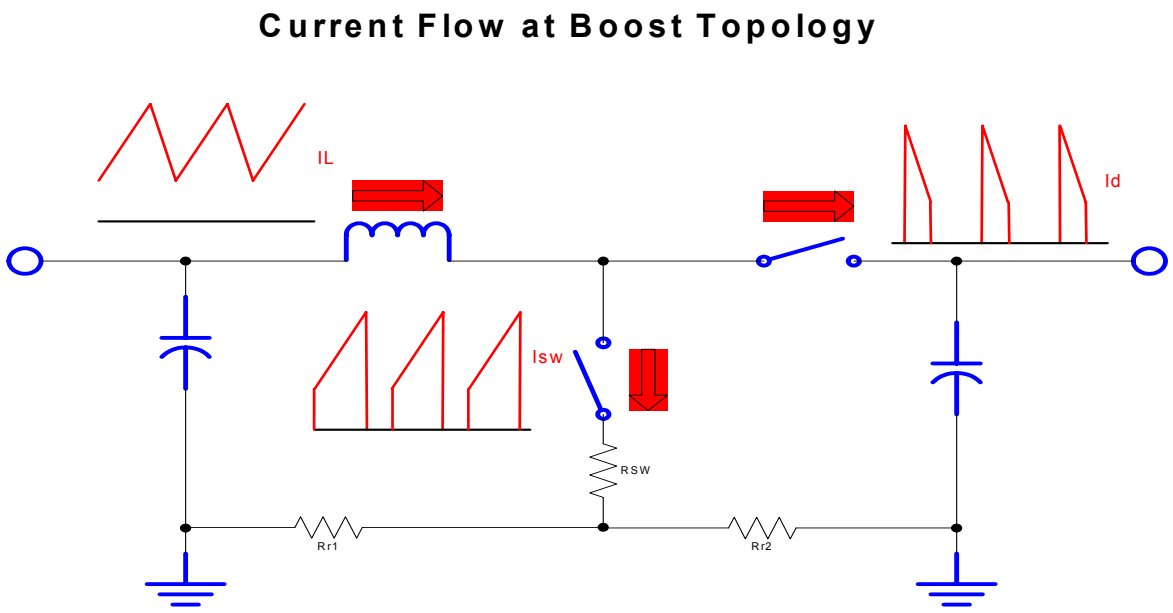

Figure 3. Current Flow of the Boost Converter

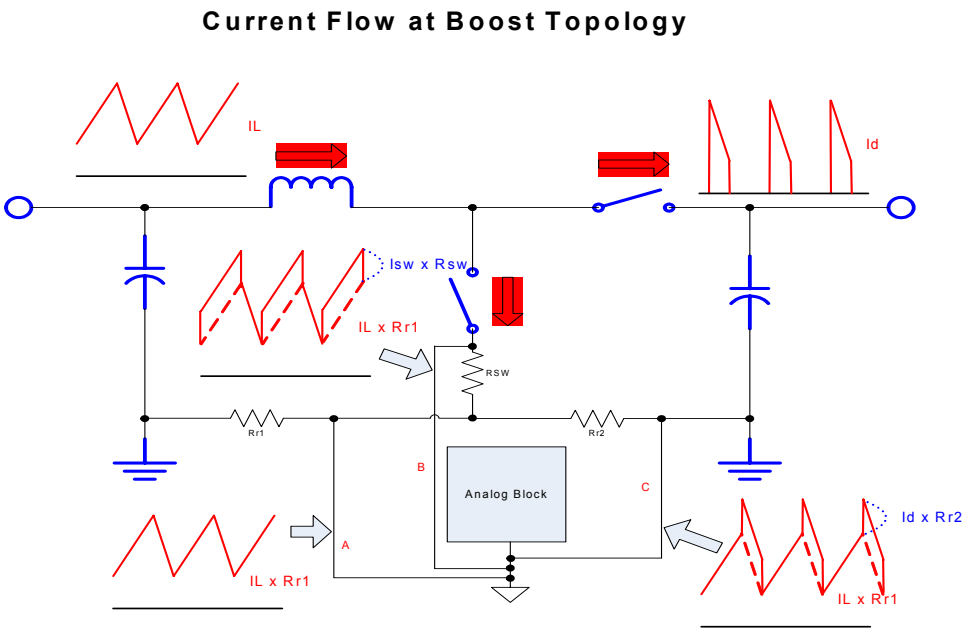

Figure 4. Ground Noise Expression

As shown in Figure 4, each ground connection point A, B, and C will have a different voltage ripple, which will be reflected to the connected Analog block. This may cause unwanted performance issues.

The connection point of power ground and analog ground should be carefully managed, to avoid this problem when doing the layout. The rule of thumb is to connect these two grounds prior to the input capacitor, and close to the input connector or input voltage supply. By doing this, two main benefits can be expected: the common impedance is reduced, and the switching ripple (or noise) will be filtered by the capacitor.

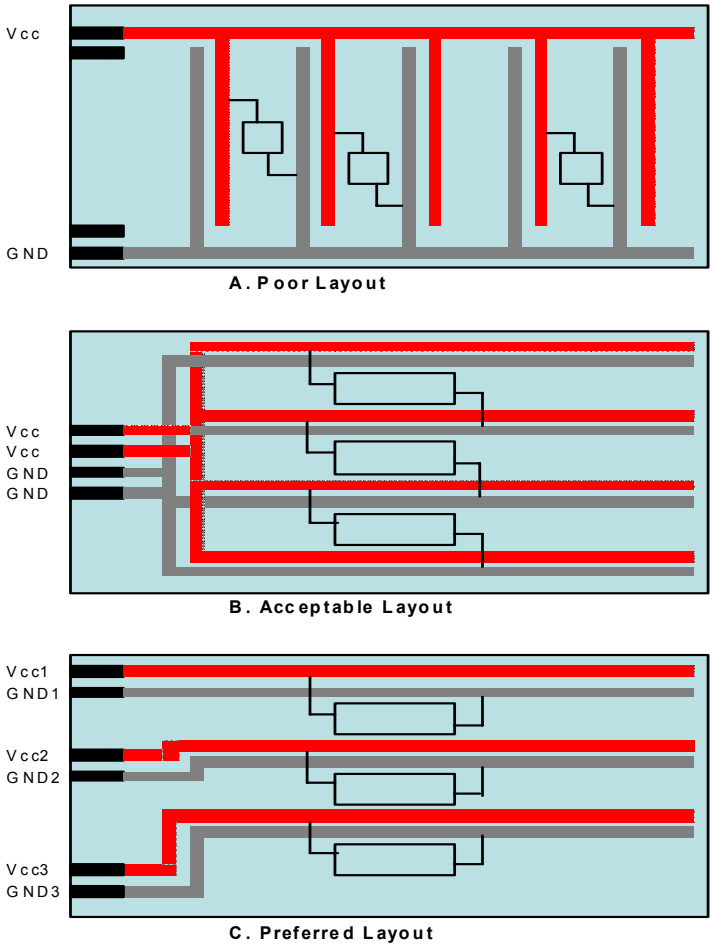

Figure 5. Voltage/Ground Distribution Concepts

5 Thermal Considerations

In applications without an external heat sink or fans to limit component temperatures within a reliable range, the PCB trace would be the only thermal path to distribute the heat generated by the components. The following equation represents the trace thermal resistance.

$$\theta trace = ThermalResistivity \times t / A$$

Copper_Thermal_Resistivity = 2.49 mmK/W (at 300 K)

For 1.0 oz/ft^2 copper (35 mm thickness copper), 1.0 mm width trace, the thermal resistance of the trace per inch is 2.8°C/Watt.

The best way to dissipate heat from the components is to attached the components' case (the main body which will be used as a thermal path of the components) directly to the wide solid plane of the copper surface. If it is difficult to expand the plane area, due to other circuits or pins, for example with the TQFN package, it is better to make a thermal path with as many vias as possible to the other layer's solid planes.

Table 7 shows the simulation results of the 32 pin 5x5 QFN and 56 pin 8x8 QFN, by changing the number of vias of the exposed pad, changing the copper thickness, and changing the number of layers. The JEDEC JESD51 specification was used for this simulation.

5.1 Standard Thermal Resistances

Table 7. Thermal Resistance data

Rating			Value	Unit	Notes
Junction to Ambient (Natural Convection)	Single Layer Board (1s)	$R_{\theta JA}$	103	°C/W	(27), (28)
Junction to Ambient (Natural Convection)	Four Layer Board (2s2p)	$R_{\theta JA}$	36	°C/W	(27),(29)
Junction to Ambient (@200 ft/min)	Single Layer Board (1s)	$R_{\theta JMA}$	87	°C/W	(27),(29)
Junction to Ambient (@200 ft/min)	Four Layer Board (2s2p)	$R_{\theta JMA}$	30	°C/W	(27),(29)
Junction to Board		$R_{\theta JB}$	15	°C/W	(30)
Junction to Case (Bottom)		$R_{\theta JC}$	4	°C/W	(31)
Junction to Package Top	Natural Convection	$R_{\theta JT}$	10	°C/W	(32)

Notes

27. Junction temperature is a function of the die size, on chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
28. Per JEDEC JESD 51-2 with the single layer board (JESD 51-3) horizontal
29. Per JEDEC JESD51-6 with the board (JESD 51-7) horizontal
30. Thermal Resistance between the die and the printed circuit board, per JEDEC, JESD 51-8. Board temperature is measured on the top surface of the board near the package.
31. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
32. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature, per JEDEC, JESD51-2.

Figure 6 shows the thermal model of the 5x5 QFN package with 9 vias.

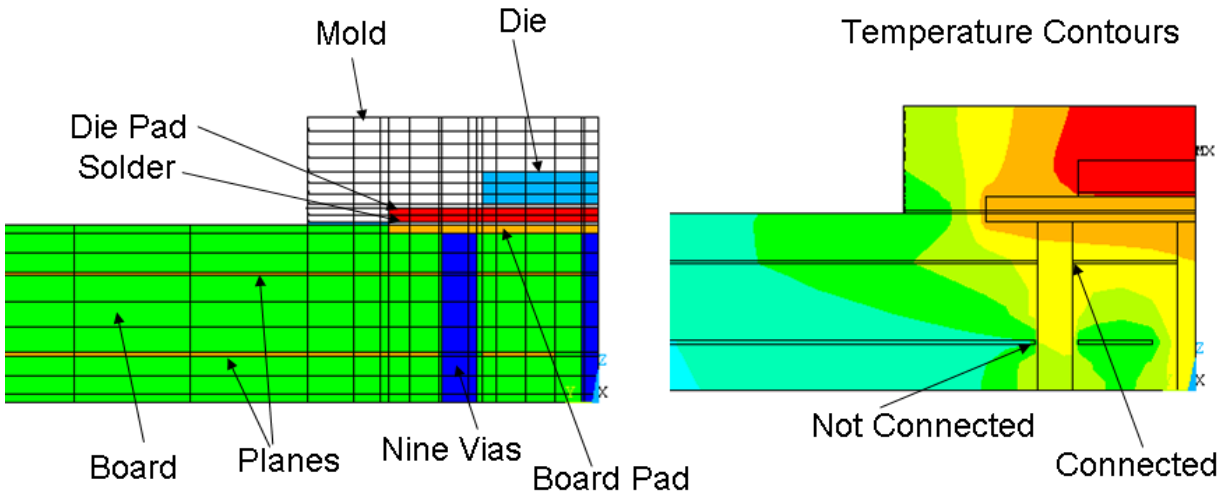

Figure 6. Thermal Model of a 32 pin 5x5 QFN Package

The QFN package has very low thermal resistance from the die to the mounting surface: 3.8°C/W for this die size.

Figure 7 shows the relationship between thermal resistance and the copper thickness of the boards. In this simulation, the board vias are connected on the plane, isolated from the others. There is one top surface trace layer. For simplicity the planes are modelled as solid planes.

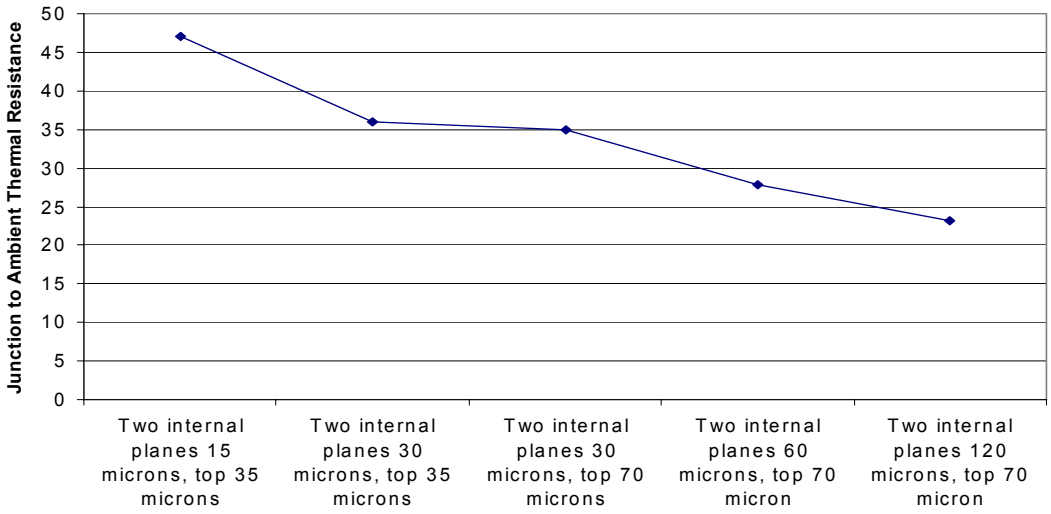

Figure 7. Thermal Resistance vs. Copper Thickness

Figure 8 shows how having an effective board area is important to reduce the thermal resistance. The temperature of the device becomes significantly hotter below an effective board area of 50 x 50 mm^2.

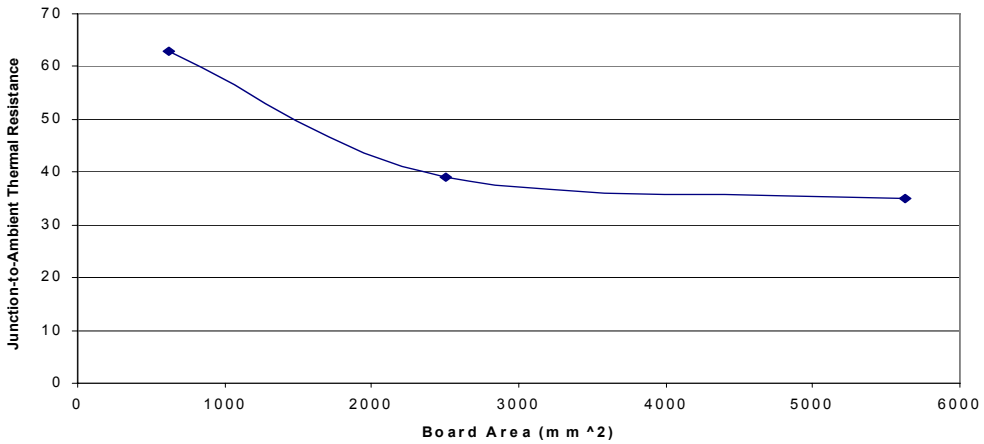

Figure 8. Effective Board Area vs. Junction to Ambient Thermal Resistance

Table 8 is the comparison table between a 32 pin 5x5 QFN package and a 56 pin 8x8 QFN package.

According to the simulation, with same number of vias, the thermal capacity of these two package does not show a significant difference. However, as the number of vias is increased on the 8x8 QFN package, the temperature of the device decreased by approximately 8.0°C with same package.

Table 8. Case Temperature with Difference Vias.

Package	T_{CASE} at 2.0 W at T_A = 25°C
32 pin 5x5 QFN, 3.6 mm flag, 9 vias	85°C
56 pin 8x8 QFN, 3.6 mm flag, 9 vias	88°C
56 pin 8x8 WFN, 3.6 mm flag, larger pad, 25 vias	76°C

The most efficient way to dissipate the heat from a QFN package is to increase the number of vias on the exposed pad, and increase the exposed pad size as much as possible.

6 References

1. IPC-D-330
2. UL1950
3. JEDEC JESD 51

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

AN3962
Rev. 2.0
8/2010