Freescale Semiconductor
Application Note

Document Number: AN3585
Rev. 1.1, 07/2008

PCB Layout Design Guidelines for Radio Board Using the MC13853 LNA

1 Abstract

Radio printed circuit boards (PCB) must effectively integrate the devices and other elements while avoiding signal transmission problems associated with RF lines and components interacting with each other. The purpose of this document is to provide general guidelines for successful radio PCB design using the MC13853 LNA. The MC13853 has three bands, a low band and two high bands, in a QFN16 package.

The most critical aspects of radio frequency (RF) circuitry are addressed and it is highly recommended to follow these design guidelines to achieve best RF performance.

Note that these guidelines and example layout figures are based on the RFX300-31 RF subsystem daughter card supporting WCDMA/EDGE 3G terminals.

Contents

1 Abstract 1
2 PCB Layers 2
3 Components and Placement Recommendations 3
4 Trace Requirements 14
5 Grounding 17
6 References 17
7 Revision History 18

© Freescale Semiconductor, Inc., 2007, 2008. All rights reserved.

freescale™ semiconductor

2 PCB Layers

This section describes the PCB technology and PCB stack-up.

2.1 PCB Layer Structure

In this guideline, a classical PCB stack-up of 8 layers (2-4-2) is described. The PCB layering structure is shown in Figure 1, the PCB Layering Structure. The dielectric constant (εr) of the FR4 material used in this example is 4.2.

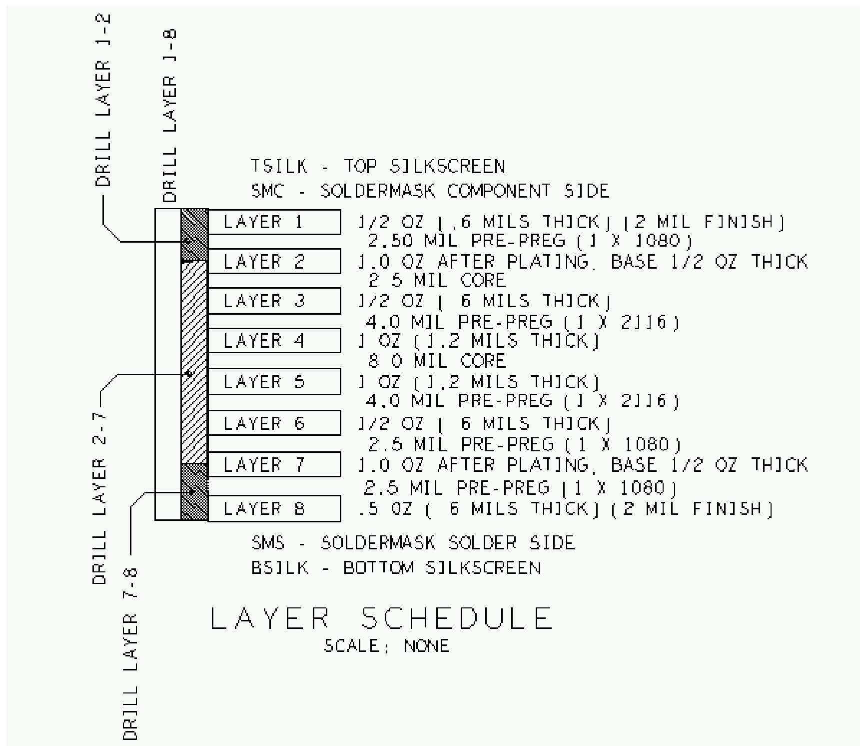

Figure 1. PCB Layering Structure

2.2 Layer Rules

An effective layer function assignment reaches best RF performances and significantly reduces electromagnetic interference (EMI) problems. The RF circuit layout is the main concern for the layer function assignment. A solid ground plane next to the power distribution layers creates a set of low ESR capacitors, thus reducing system noise. Each radio has its own specific constraint, but this is a basic reference for radio board design.

Table 1. PCB Layer Assignment

Layer Number	Layer Rule	
	RF Signals	Baseband Signals
1	Microstrips, Ground for striplines	Component interconnections
2	Ground cutouts below microstrips and over striplines	Vertical traces
3	Striplines, Ground for microstrips	Horizontal traces, DC distribution
4	Main ground, Ground for striplines	Main ground
5	Ground, Ground over striplines	Ground, DC distribution
6	Striplines, Sensitive trace	Horizontal traces
7	Ground cutouts below striplines	Vertical traces
8	Ground for striplines	Component interconnections

3 Components and Placement Recommendations

3.1 Component Placement

The basic principle of component placement is to try and follow the natural signal flow: From the antenna through the switch, the LNA, the SAW filter, the TRX to the BB.

The following guidelines provide the basic ideas for component placement:

- Place the antenna, switch, Tx and Rx sections on the top of the radio board.
- Put the BB section to the bottom of the RF section.
- Place the PA close as possible to the Antenna Switch to minimize insertion loss.
- Place the MMM7210 and the PA in positions that ensure a direct and short as possible Tx path.
- Place the SAW filter close as possible to MMM7210 to minimize the distance of Rx differential lines.
- When placing components, note the potential routing of circuits between subsystems, including clocks and crystal circuits. Refer to Figure 2 for IC placement for a 2G+3G application on the RFX300-31 RF subsystem daughter card.

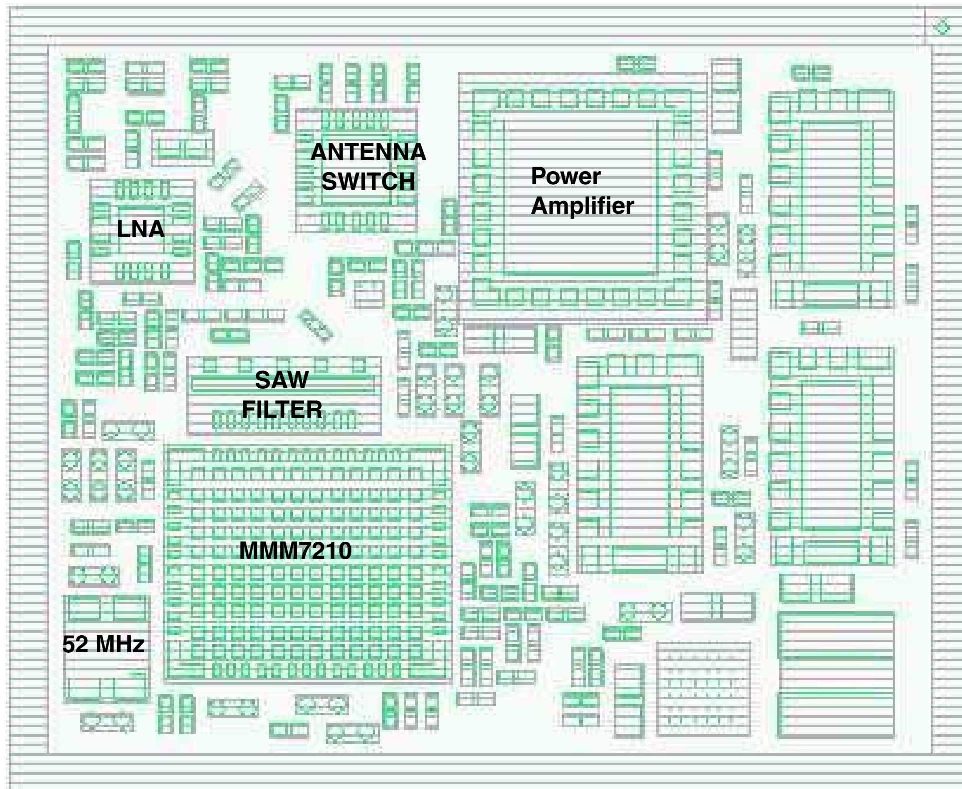

Figure 2. RFX300-31 DCard Parts Placement

Figure 3 shows the LNA portion of the schematic of the Freescale RFX300-31 sub-system board with the component designators shown. This can be used to locate the components in the subsequent layout figures. Note that components C346, L33, C342, L36, C341 and L38 are placeholders for notch filters on the inputs, if needed. Components C337, C340 and C339 are input shunt capacitor placeholders for each band, if needed. Figure 4 shows the general LNA and matching component locations, the top level ground layer, the microstrip traces between components, along with the input and output match areas circled. In Figure 5, the 50 ohm RF input lines and DC feed line are shown.

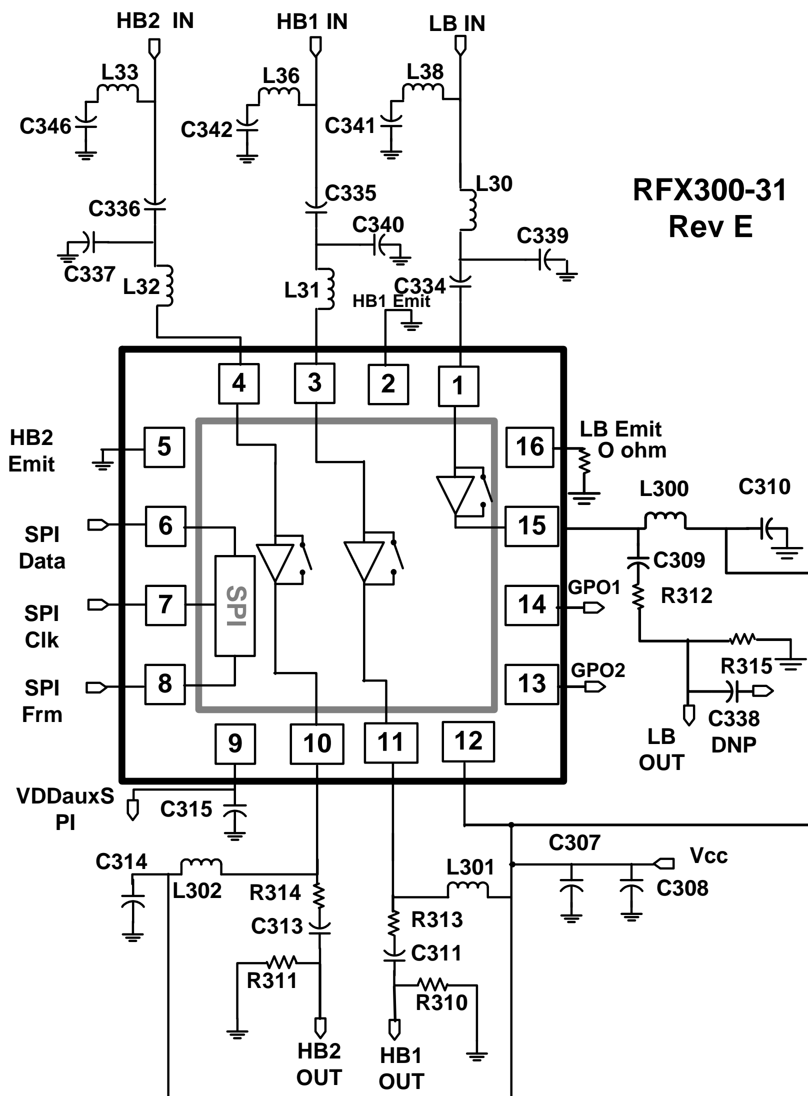

Figure 3. LNA and Matching Component Schematic for the RFX300-31 Sub-system Board

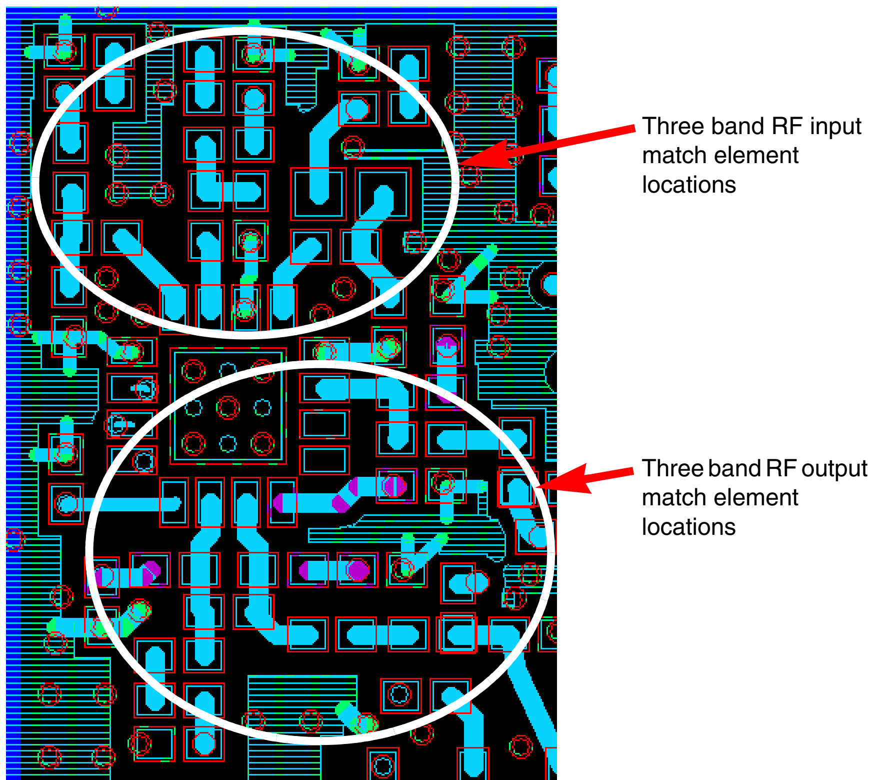

Figure 4. LNA and Matching Component Layout

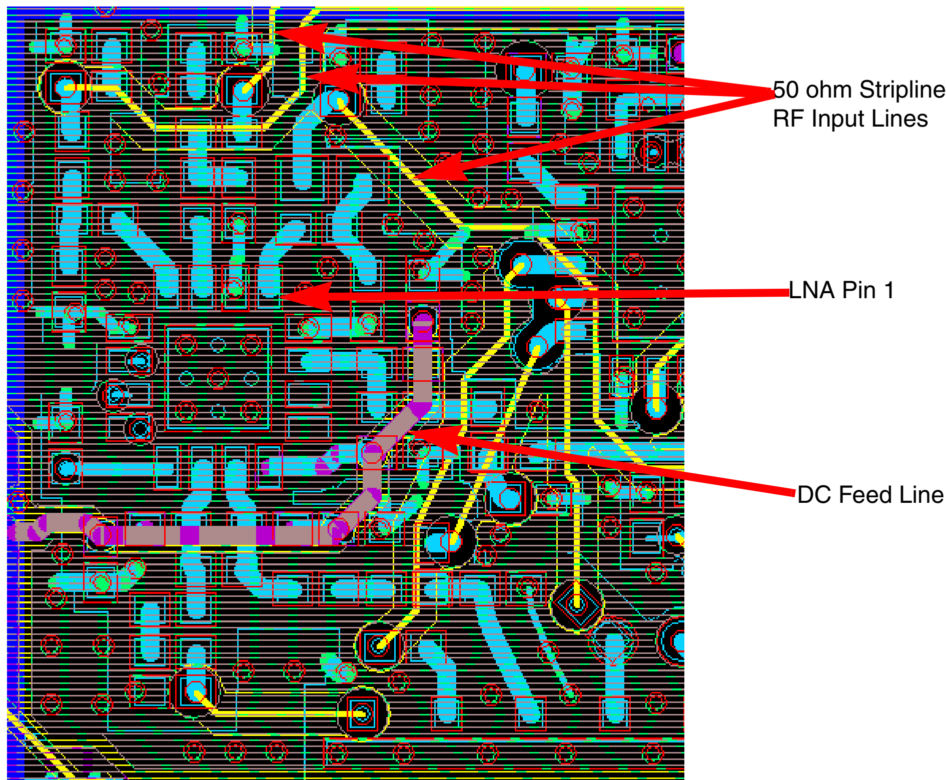

Figure 5. LNA and Matching Component Layout Showing RF Lines and DC Feed Line

3.2 Component Recommendations

- Select low ESR capacitors for IC decoupling. Ceramic NPO material capacitors are preferred.
- Select the proper RF bypass capacitor value to place on supply and control line. For 0402 RF bypass capacitors use 33pF
- For 0402 size inductors, the Murata LQG15HS series is recommended.

3.3 LB Component Placements

On the MBC13853 QFN16 package, pin 1 is the LB RFin pin. The components of the LB input match should be arranged outward from pin 1, as shown in Figure 6. They should also be arranged so they are spaced as far away as practical from the HB1 RFin matching elements. The HB1 emitter pin between the LBin and HB1in pins provides additional spacing. The LB matching component closest to the package is a capacitor, which is rotated away from the package. This is followed by the input inductor, which is also oriented so that it is rotated perpendicular to the HB1 inductor. The RF 50 ohm input line connects to the inductor, along with placeholders for two notch filter elements to ground.

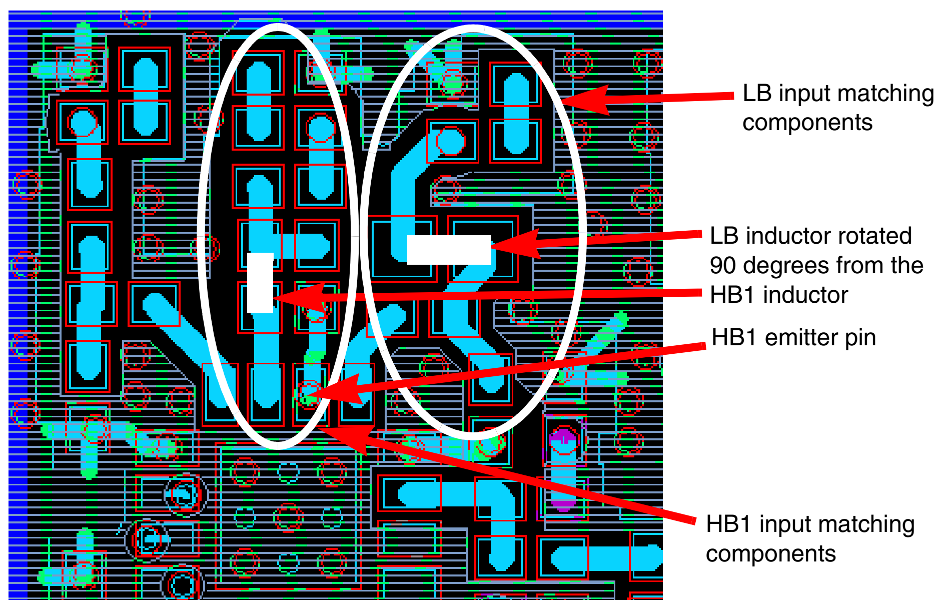

Figure 6. LNA Input Matching

Figure 7 shows the LB output match. RFout is on pin 15 of the package. The matching components on this pin are arranged to follow the direction towards the SAW filter and away from the RFin trace and components and also away from LB emitter pin 16. This is especially true of the feed inductor. It is moved out away from the LB emitter connection using a microstrip trace. RF and AC bypass capacitors should be placed close to the feed inductor.

In Figure 7, the RFX300-31 rev. E layout shows the LB emitter pin 16 connected through a trace directly to ground, as is done for the HB1 and HB2 emitter pins. From a performance standpoint, it is best to not connect the LB emitter pin directly to ground. The preferred method is to connect the LB emitter pin to ground using a 0 ohm resistor. Either a 402 or 201 size resistor can be used with nearly equivalent performance. Connecting the LB emitter pin directly to ground results in lower IM2 and IP3 performance.

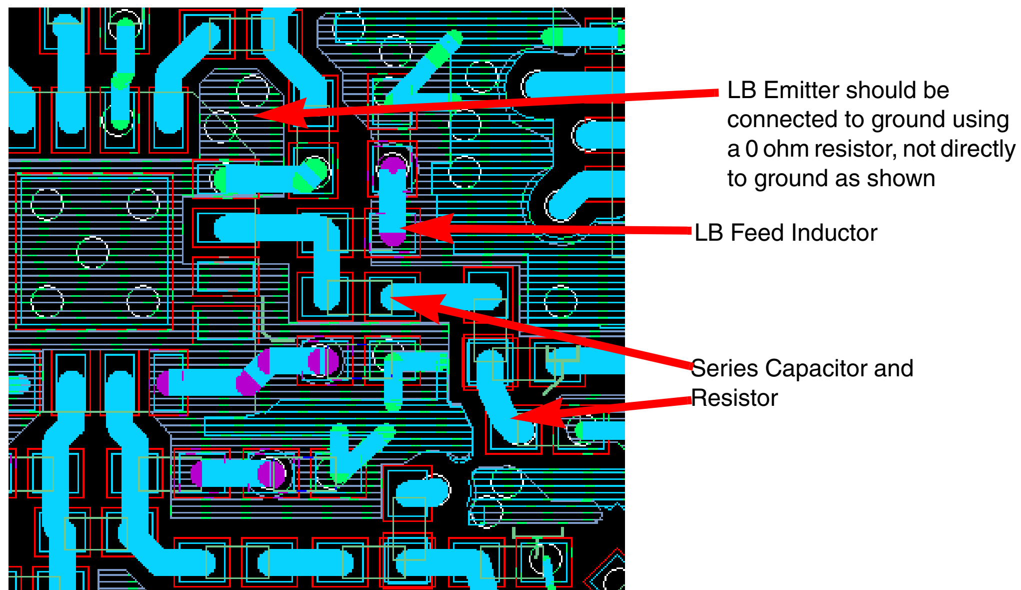

Figure 7. LB Emitter on Pin 16 and Output Matching on Pin 15

3.4 HB1 Component Placement

Pin 2 on the QFN16 package is the HB1 emitter. This pin is connected directly to ground as shown in Figure 8. Bringing the ground plane to this pin also serves to isolate the LB RFin components and trace from the HB1 components and trace. Placing vias to the internal ground planes is recommended. In this layout two vias are used with a trace between them that also helps isolate the LBin and HB1in paths and components.

As with the LB RFin path, the HB1 RFin path must also be designed so as to be moved as far from the HB2 RFin trace and components as can be made feasible so as to maximize the isolation between the two high band RF signal paths, as shown in Figure 8. In this layout, the HB2 trace leaves the package pin at a 45 degree angle. Also important is to have the match inductor oriented at 90 degrees relative to the match inductor used for the HB2 RF in path, so as to minimize mutual coupling between the two. Pin 2 is the HB1 emitter and should be connected directly to ground. Nearby vias to internal ground planes are recommended. The shunt capacitor matching component should have a short, low inductive path from the ground side to the HB1 emitter pin.

In Figure 9 the HB1 output matching is shown. Note the placement of pads for a short between the lines close to the package pins to allow for an output sharing configuration. The HB1 DC feed inductor is placed as close to the HB1 output pin as possible.

The HB1 RFout line on pin 11 is designed so as to maximize the spacing from the HB2 RFout trace by having the components emanating away from the HB2 components.

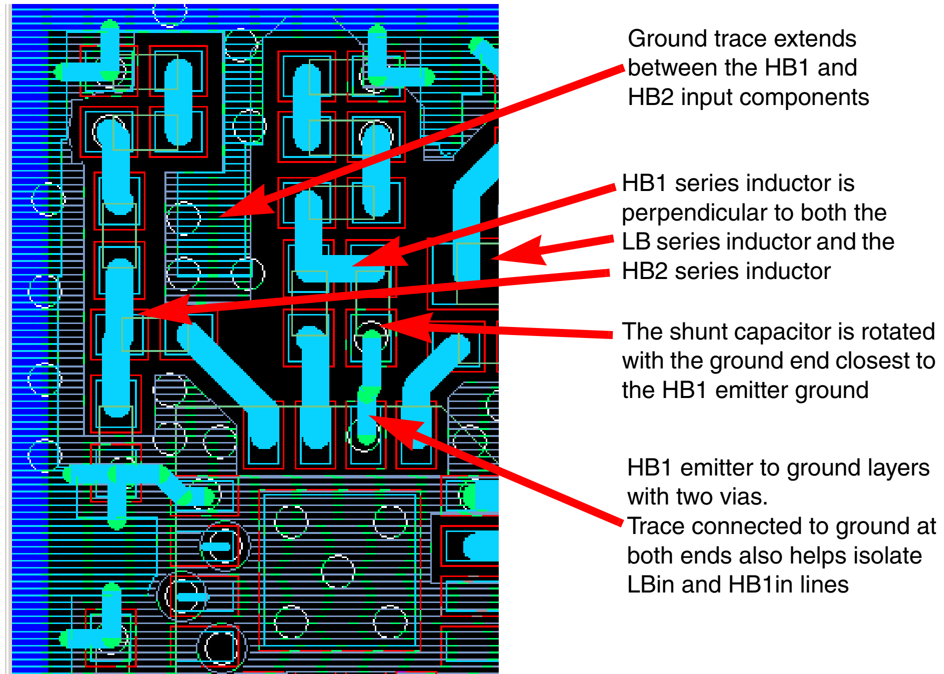

Figure 8. HB1 input Matching

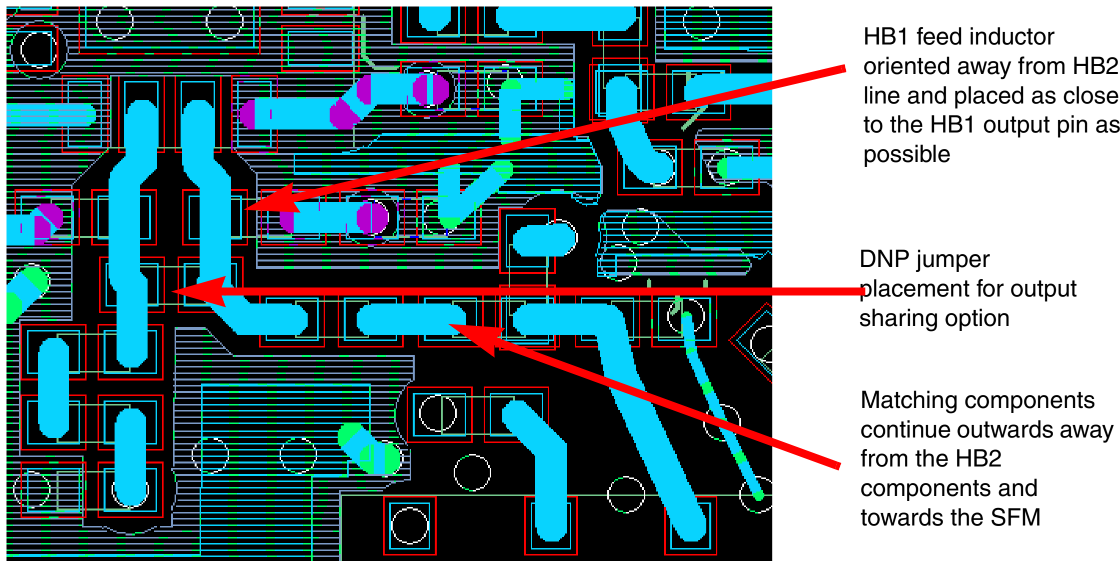

Figure 9. HB1 Output Matching

3.5 HB2 Component Placement

Pin 4 of the QFN16 package is the HB2 RFin pin. The match components and RFin line should be arranged to be spaced as far as possible away from the HB1 RFin components to maximize isolation between the two RF paths, as shown in Figure 10.

Pin 5 is the HB2 emitter and should be connected directly to ground. Nearby vias to internal ground planes are recommended.

The HB2 output inductor is rotated away from the HB1 output inductor as shown in Figure 11. The HB2 DC feed inductor is placed as close to the HB1 output pin as possible. The output matching components are moved away from the HB1 components and separated from them by a ground area.

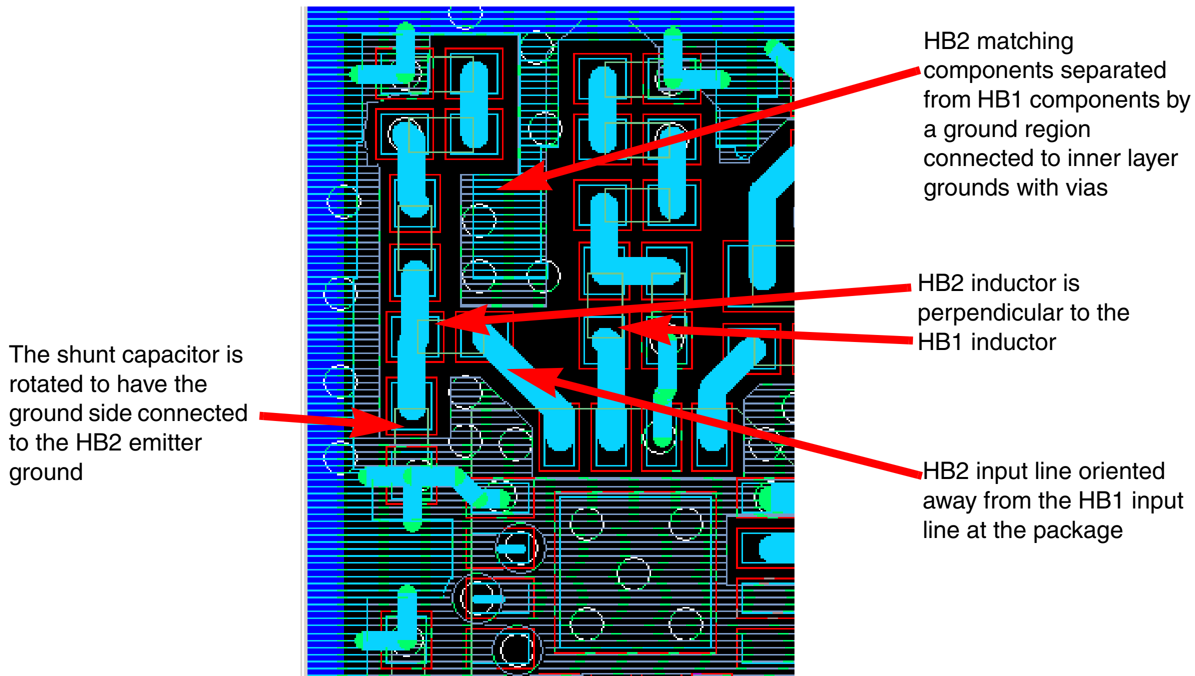

Figure 10. HB2 Input

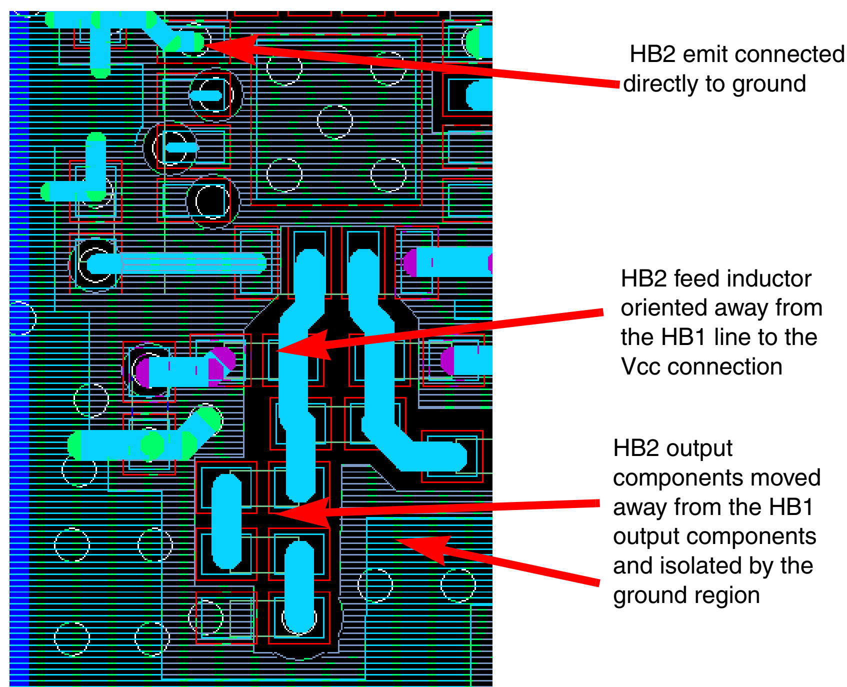

Figure 11. HB2 Output

3.6 RF Components Keep Out Area

Figure 12 highlights the keep out areas under RF matching components. RF lines and DC lines are not run under RF components. DC lines that do run under RF traces are on layer 5 and are perpendicular to the RF trace, when possible. Observance of RF keep out areas on the first internal layer under the RF signal pins and all matching elements for the three LNAs is essential for realizing the available gain and achieving optimum noise figure and return losses. Try to shield the RF traces with a ground plane. In this case, layer 4 is the ground shield.

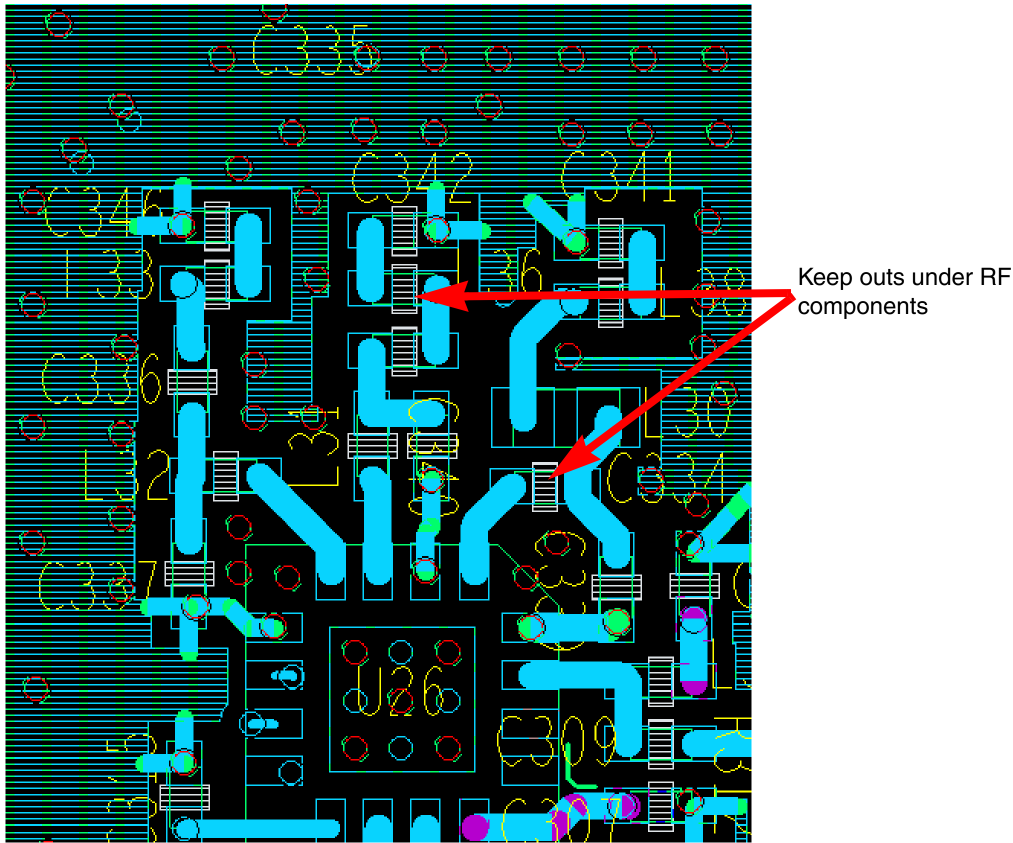

Figure 12. Keep outs for routing under RF components

4 Trace Requirements

4.1 RF Signals

- The RF trace routing is always the top priority and it is necessary to route every RF trace according to the impedance matching technique.
- Impedance controlled traces are implemented by either microstrips or striplines.
  — The microstrip should be used within a shielded area (with a metal shield cavity) of outer layers for short interconnection between components.
  — The stripline can provide good isolation even in an unshielded area (without a metal shield cavity) because it is completely bounded by an upper and lower layer of the ground plane. It is suitable for RF signals and sensitive lines.
- Any circuit trace on the PCB has characteristic impedance associated with it. This impedance is dependent on width (W) of the trace, thickness (T) of the trace, dielectric constant (εr) of the material used, and height (H) between the trace and reference plane. Many microwave CAD tools are available and can support the designer to compute trace width.

- Coplanar clearances (G) must be at least the trace width (W) and at least twice the height H1 or H2. This reduces the parasitic capacitance, which potentially alters the trace impedance and increases the losses.
- Width of controlled impedance trace should be wide enough to maintain reasonable insertion loss and manufacturing reliability. Cutting out inner layers ground areas next to the microstrip or the stripline trace layer, increase the effective substrate height; therefore, increasing the width of the RF trace.
- Microstrip and Stripline Models show the inner ground cut out of the microstrip and the stripline.
- Cut out ground fill under RF signal pads to reduce stray capacitance losses.
- Avoid parallel routing and crossing of RF traces and from under signal pads.
- Keep the routing direct and short. For a long trace, use the stripline.
- Use the microstrip for RF traces on the components side.
- Avoid multiple transitions between the layers.
- Avoid routing RF trace with sharp corners. A smooth radius is recommended.
- Isolate the Rx and Tx paths by ground.
- Fill the area around the RF traces with ground and ground vias to connect inner ground layers for isolation.

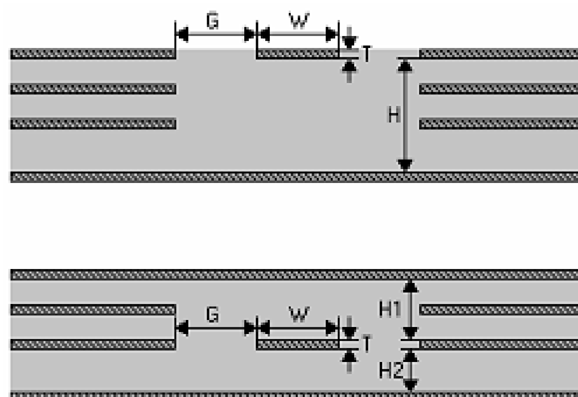

Figure 13. Microstrip and Stripline Model

- Use controlled impedance RF traces:

  Rx paths into the LNA:

  – 50Ω LNA inputs and outputs. Microstrip line (width=0.286 mm) on top layer + Stripline on layer 6 (width=0.105 mm/Ground layers 5 and 8)

  – Refer to Figure 14 for a routing example of HB1 and HB2 input stripline lines. Note the stripline RF lines are clear of other signal lines and vias. Layer 5 serves as the ground over the stripline and layer 8 serves as the ground below the stripline. These ground reference layers should be at equal electromagnetic potential. Tie the two ground references together, in particular along the RF trace, with adequate vias. Note the grounding wall with vias in between the RF traces to isolate RF paths. In Figure 15 the microstrip lines on the top layer used to connect the RF matching components are shown. The striplines shown in Figure 14 are on layer 6.

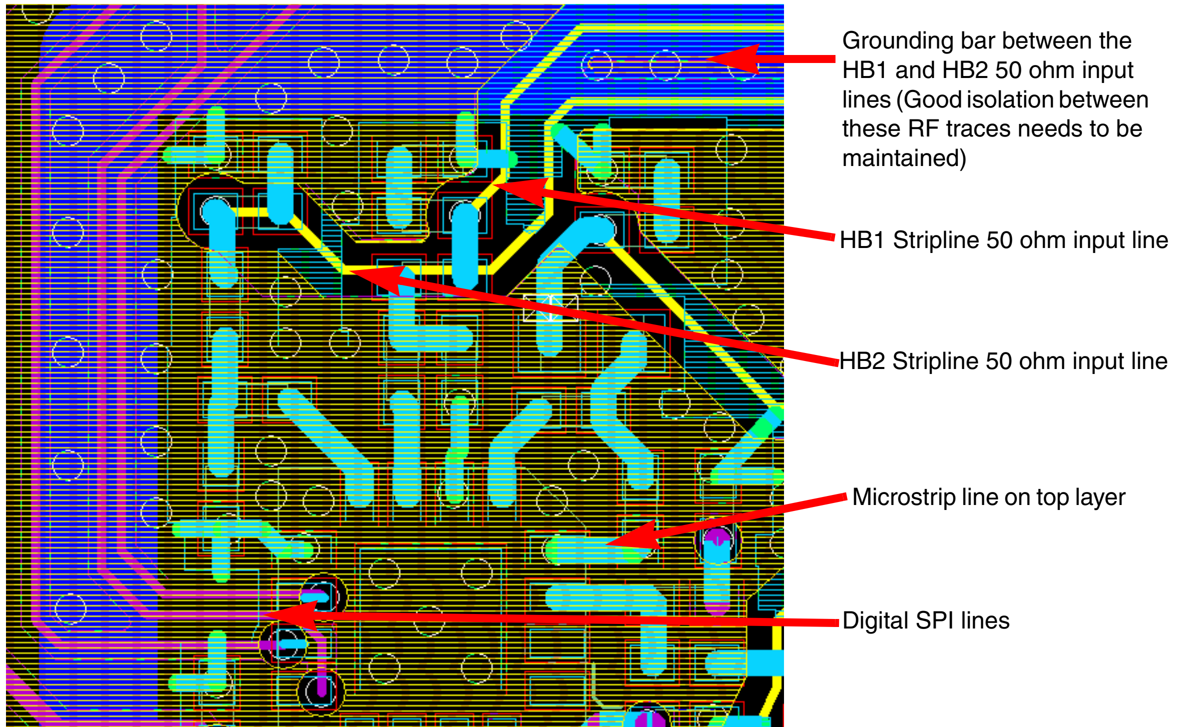

Figure 14. HB1 and HB2 LNA Stripline Input Lines

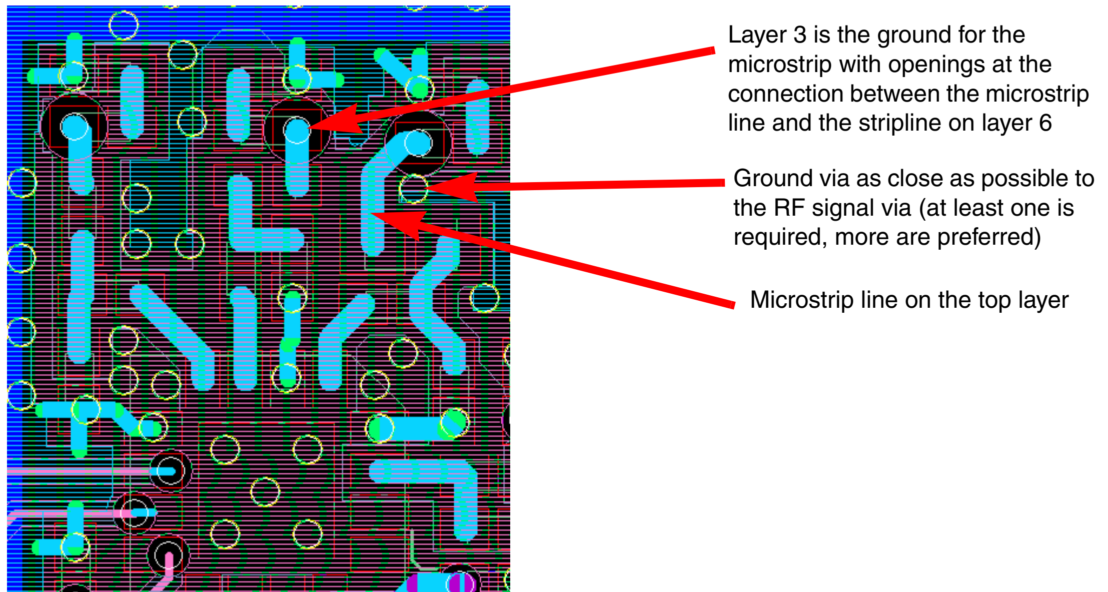

Figure 15. Microstrip Lines Used to Connect the RF Matching Components

4.2 DC Distribution

There are a number of guidelines pertaining to the DC lines. See Figure 16 for reference.

- Use several signal vias for layer transitions of the main DC supply and its ground

- Connect signals and ground directly by the vias on pads.
- Put ground vias along microstrips, striplines and non-RF sensitive lines for better isolation.
- Add ground vias on the outer ground filled area to connect to the inner ground layers for improving grounding isolation.
- Avoid perforating the Vcc line trace with noisy vias.
- Add multiple ground vias under the LNA for proper grounding to inner ground layers.
- Add multiple vias to connect the inner layer DC supply line to surface supply pins to minimize voltage drop.
- Do not route Vcc under 52 MHz crystal even if the routing is under several layers of ground.

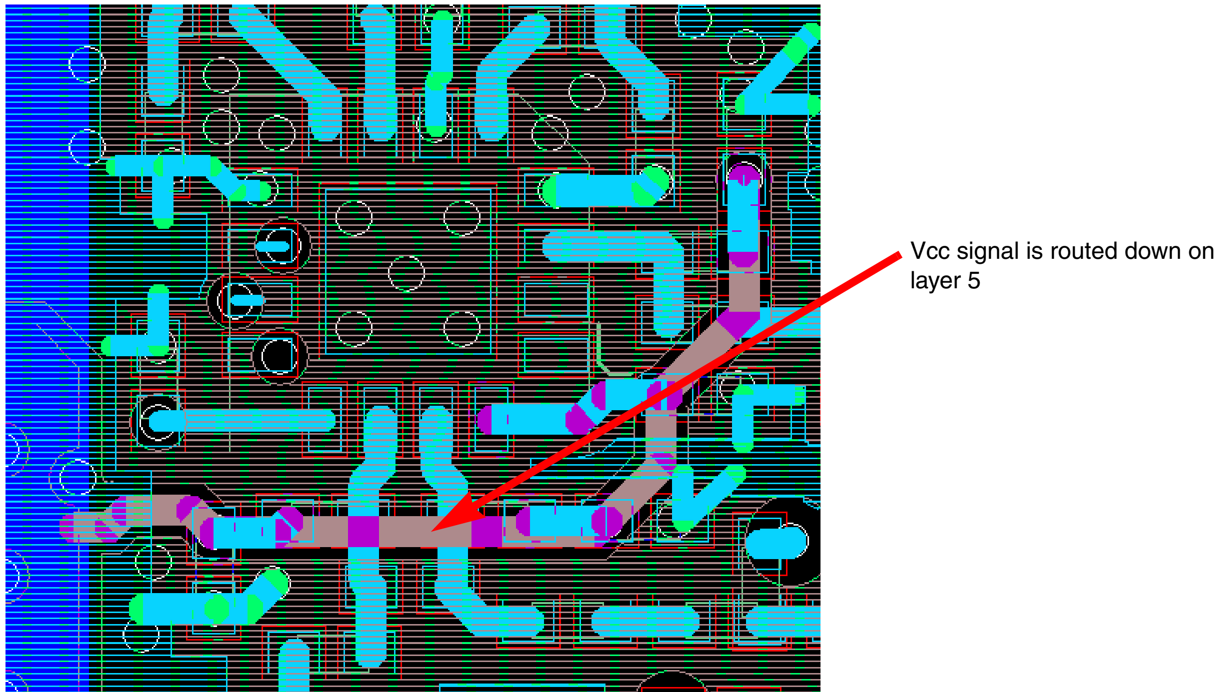

Figure 16. DC Line Showing Routing

5 Grounding

For grounding, follow these guidelines:

- Make the internal ground area as solid as possible. Do not break the ground into pieces.
- Provide good solid ground by using multiple vias.
- Fill as much ground as possible in the area between the walls of shield cavities and outline of the RF section.
- Connect each ground pin or via to the ground plane individually. A daisy chain connection to the ground pins shares the ground path, which increases the return current loop.
- Use ground via *stitching* to transition from top layers to inner ground layers.

- The PCB pattern under the LNA must bridge the ground pins (pins 2, 5 and 16) and the ground pad. Add ground vias to inner ground layers for each ground pin.

6 References

For more information refer to the following documents. Freescale documents are located at: http://www.freescale.com.

- *MC13853 Data Sheet - Tri-Band Low Noise Amplifiers with Bypass Switches* (document number: MC13853)

7 Revision History

Table 2 summarizes revisions to this document since the release of the previous version (Rev. 1.0).

Table 2. Revision History

Location	Revision
Figure 3	Revised drawing.
Section 3.3, “LB Component Placements	Removed sentence “The shunt capacitor should have a short, low inductance path from the ground side to the LB emitter pin.“ from the first paragraph. Replaced final paragraph in section.
Figure 6	Removed text for LB Shunt Capacitor note.
Figure 7	Revised text for LB Emitter note.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

***For Literature Requests Only*:**
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals”, must be validated for each customer application by customer’s technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2007, 2008. All rights reserved.

Document Number: AN3585
Rev. 1.1
07/2008

freescale™
semiconductor