AN14468

Power supply IC PCA9460 for i.MX 8ULP powering guide

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Document information

Information	Content
Keywords	PCA9460, i.MX 8ULP, PMIC
Abstract	This application note provides information regarding i.MX 8ULP MPU and peripheral devices power connections using the PCA9460 power management IC

1 Overview

The PCA9460 is a power management IC (PMIC) designed for i.MX 8ULP applications processor. This IC implements the power supply voltage, controls the power up/down sequence and supports the frequent dynamic voltage transitions to align with the i.MX 8ULP operating modes for a very power efficient MPU + PMIC system solution. It can support power supply voltage for peripheral devices connected to the i.MX 8ULP. The PCA9460 PMIC incorporates power supply design for applications using the i.MX 8ULP.

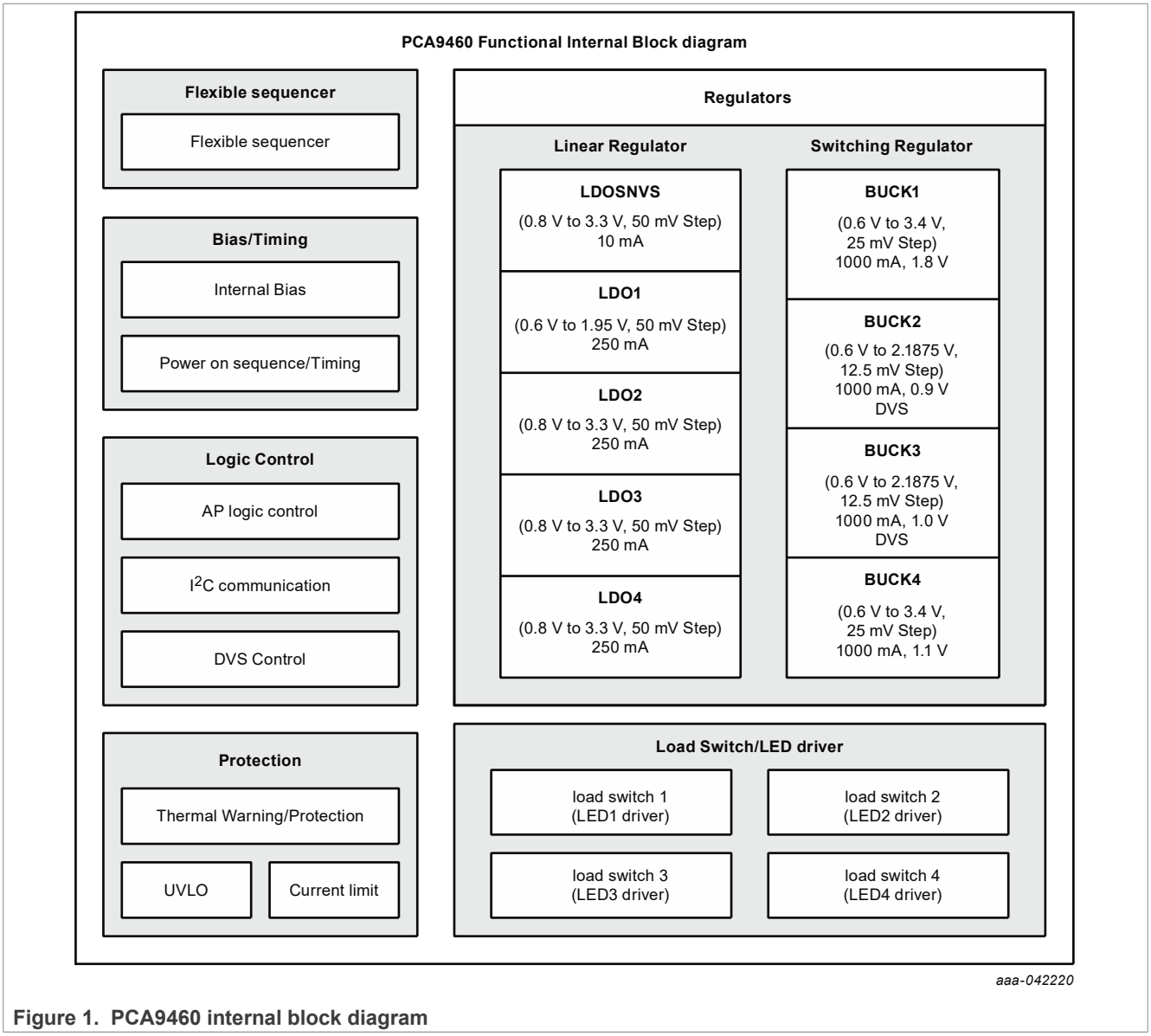

Figure 1. PCA9460 internal block diagram

1.1 Features

- PMIC optimized for i.MX 8ULP
  - Compatible with all i.MX 8ULP operating modes
  - Supports power supply voltage and required power up/down sequences

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- Supports powering LPDDR4/4X/3 memory
- High efficiency 4-channel BUCK regulator (BUCK1~4)
  - 1 A buck regulator two channels (BUCK1, 4)
  - 1 A buck regulator two channels with DVS function[1] (BUCK2, 3)
- 5-channel linear regulator (LDO_SNVS, LDO1~4)
- – i.MX 8ULP BBSM mode[2] 10 mA LDO for IO power one channel (LDO_SNVS)
  - 200 mA LDO one channel (LDO1~4)
- 4-channel load switch (LSW1~4)
  - Used as load switch or LED driver with 150 mΩ on-resistance
- I2C communication interface (Fast Plus Mode max: 1 MHz): PCA9460 control
- Temperature range (T_{amb}): - 40 °C ~ +105 °C
- WL-CSP 42-pin (7 x 6 bump array): Size 2.86 mm x 2.46 mm x 0.4 mm

2 Block diagram

Figure 2 shows a block diagram of the PCA9460.

1 DVS (Dynamic Voltage Scaling): This control dynamically changes the PCA9460 power supply voltage according to the i.MX 8ULP operation mode. The voltage slew rate at the time of change can also be set.

2 BBSM (Battery Backed Security Module) mode: In the i.MX 8ULP, only the built-in RTC and some functions (wake-up, etc.) are operating. The power is supplied only to the BBSM power supply from PCA9460 (NVCC_BBSM_1P8).

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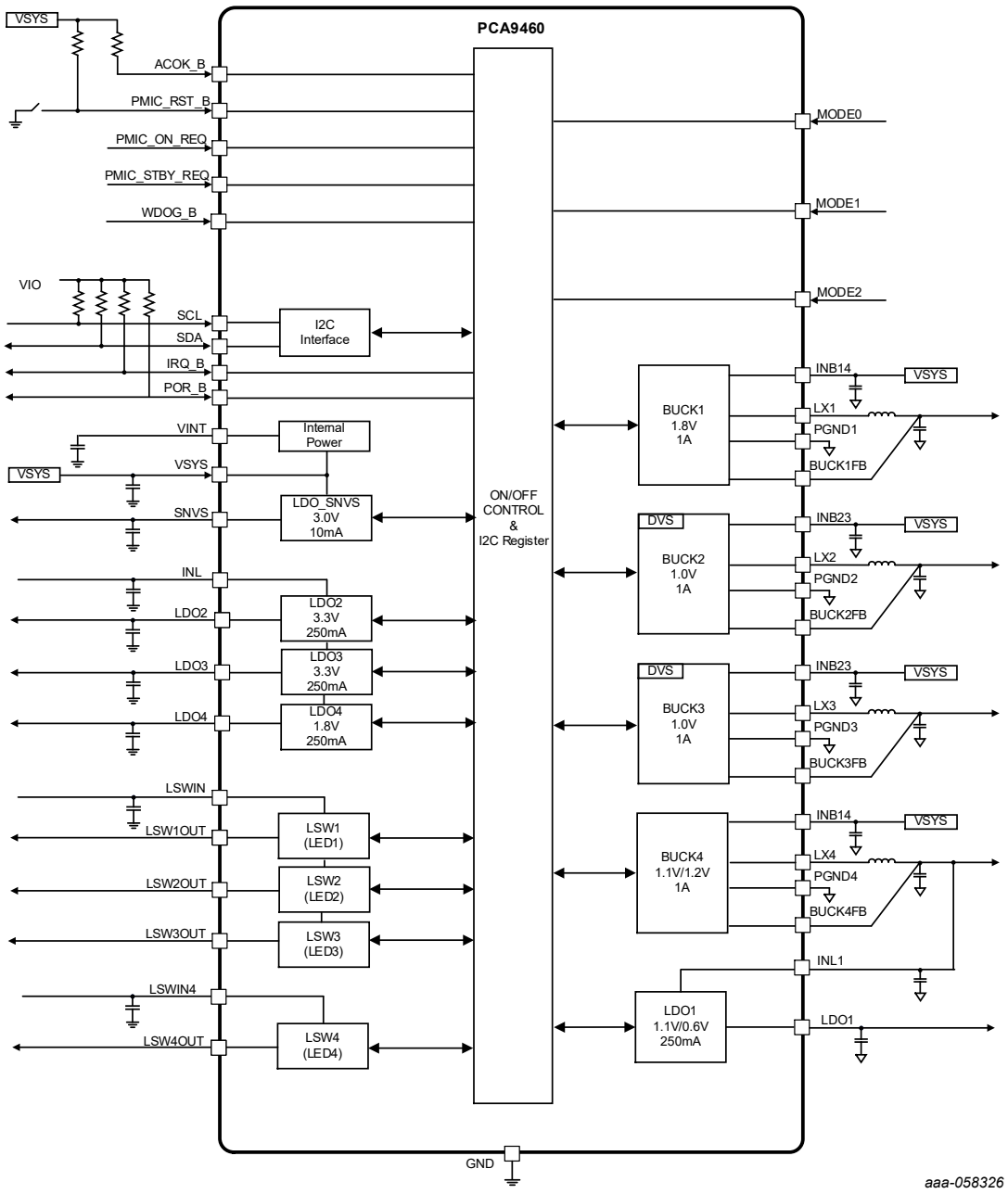

Figure 2. PCA9460 block diagram

- The VSYS pin is the power supply input pin for the PCA9460. PCA9460 state transitions to the power supply mode shown in Table 4 according to the VSYS input voltage value. The guaranteed operating range is 2.7 V to 5.5 V, and the absolute maximum rating is -0.5 V to 6.0 V. Each BUCK input should be supplied with the same power supply as VSYS.

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3 Power supply table and connection diagram

3.1 i.MX 8ULP and peripheral device power supply table

The PCA9460 supports power supply to i.MX 8ULP and peripheral devices. Table 1 shows the supply voltage to each peripheral device.

Table 1. i.MX 8ULP and peripherals power supply table

MPU Memory	PCA9460					
	1.0V	1.8V	1.2V	1.1V	0.6V	3.3V
i.MX 8ULP	✓	✓	✓	✓	✓	✓
LPDDR4		✓		✓		
LPDDR4x		✓		✓	✓	
LPDDR3		✓	✓			
NAND (eMMC)		✓				✓
pSRAM(Oct SPI)		✓				
NOR/NAND(Oct SPI)		✓				

All of the i.MX 8ULP internal logic and interface can be supplied from the PCA9460. Power supplies for memory/storage (DDR, pSRAM, NOR/NAND) and other devices can also be supplied from the PCA9460.

3.2 i.MX8ULP and peripheral device power connection diagram

PCA9460A (LPDDR4), PCA9460B (LPDDR4X), and PCA9460C (LPDDR3) power connection diagrams for connecting the PCA9460 and i.MX 8ULP differ depending on the type of DDR memory used.

Figure 3 shows the power connection diagram between the PCA9460A/C and DDR3 or DDR4 and the power connection diagram to peripheral devices.

Figure 4 shows the power connection diagram between the PCA9460B and DDR4X and the power connection diagram to peripheral devices.

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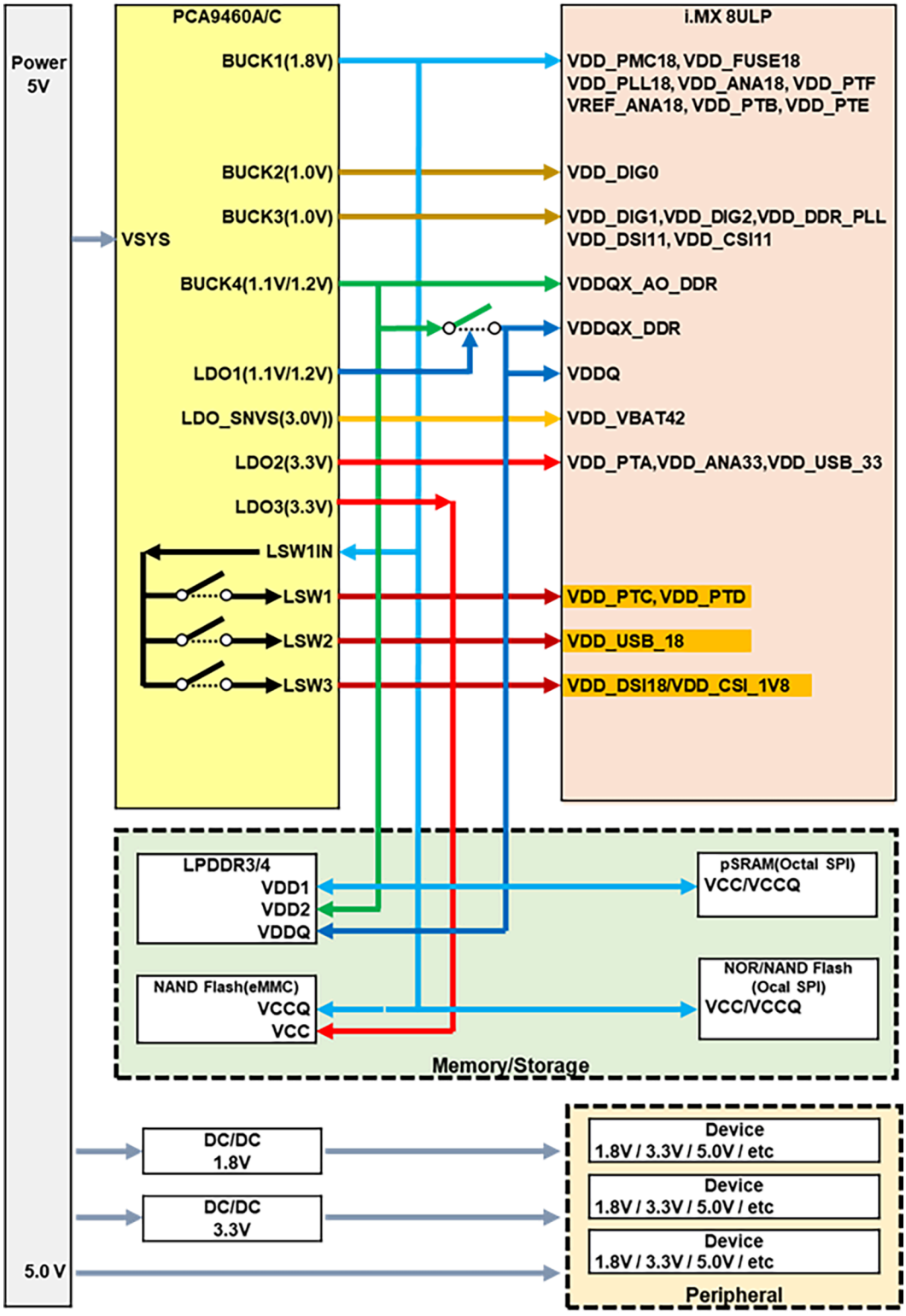

Figure 3. i.MX 8ULP processor and DDR3/4 power tree

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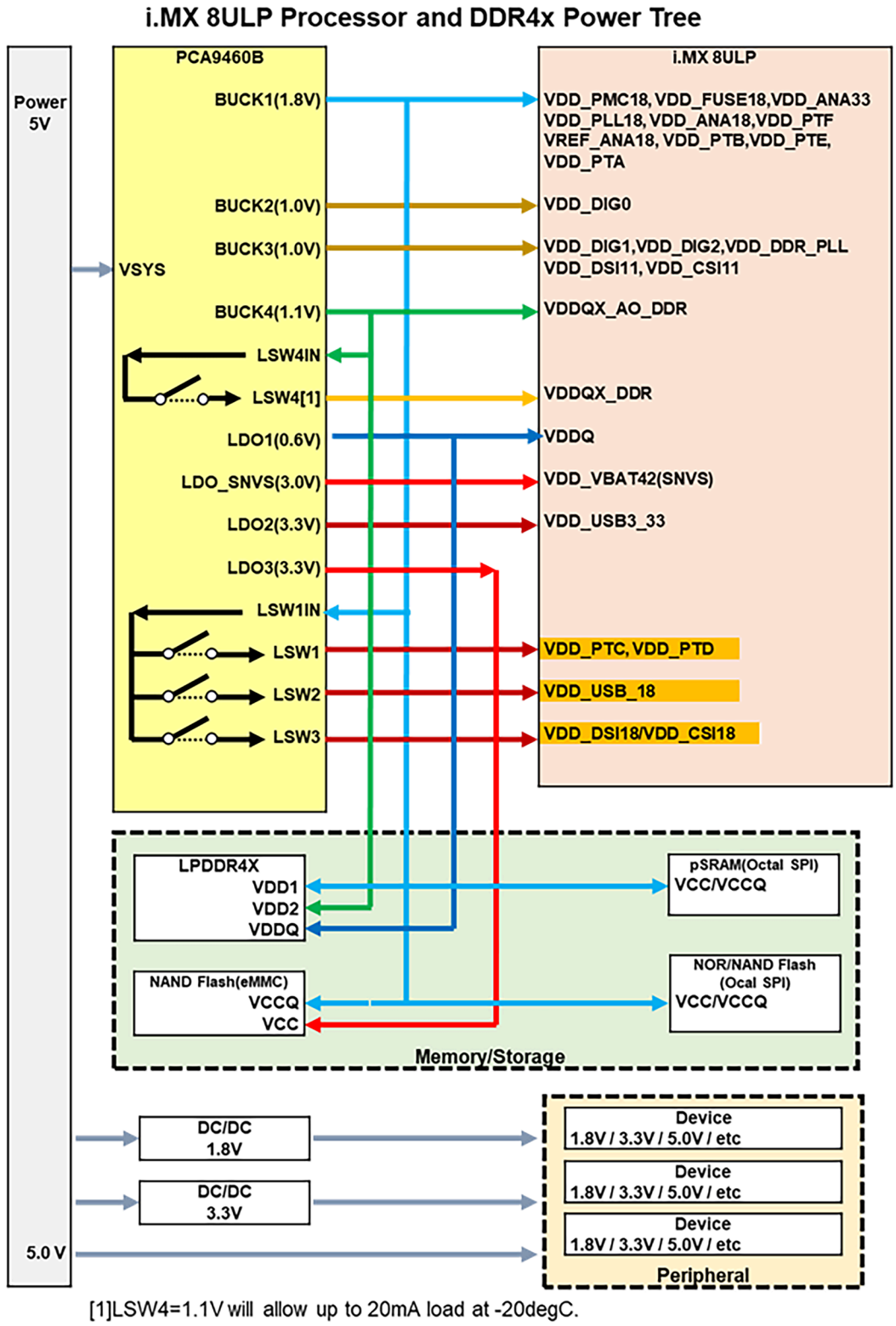

Figure 4. i.MX 8ULP processor and DDR4X power tree

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4 Connection by DDR memory type

The i.MX 8ULP supports three types of DDR memory (LPDDR4/LPDDR4X/LPDDR3). The product and output voltage values used differ depending on the type of DDR memory used: PCA9460A (LPDDR4), PCA9460B (LPDDR4X), and PCA9460C (LPDDR3).

Table 2 shows a comparison table of PCA9460 model numbers by DDR memory type and BUCK4/LDO1 voltage corresponding to DDR memory.

Table 3 shows the connection diagram by DDR memory type.

Table 2. PCA9460 model numbers by DDR memory type

Type	DRAM	Difference	
		BUCK4	LDO1
PCA9460A	LPDDR4	1.1V	1.1V
PCA9460B	LPDDR4X	1.1V	0.6V
PCA9460C	LPDDR3	1.2V	1.2V

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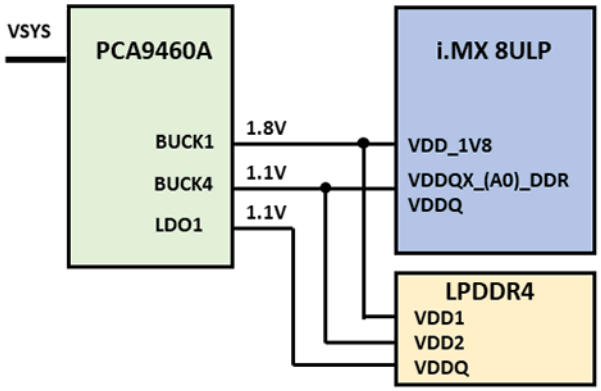
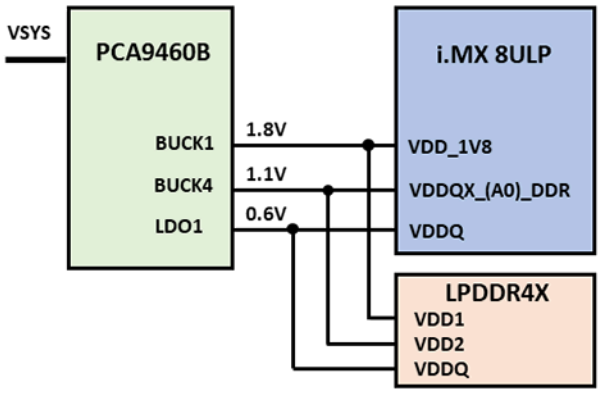
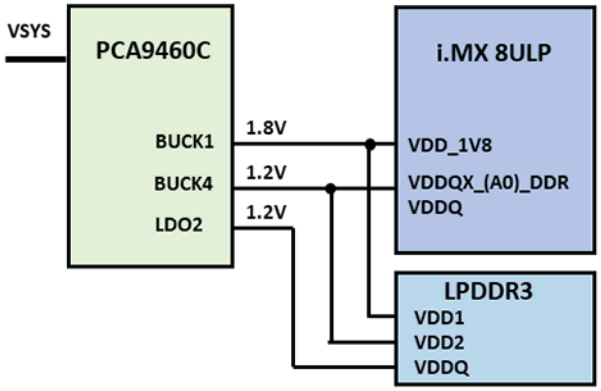
Table 3. Connection diagrams by DDR memory type

Memory	PCA9460	Schematic
LPDDR4 VDD1=1.8V VDD2/VDDQ=1.1V	BUCK1=1.8V BUCK4=1.1V LDO1=1.1V	
LPDDR4X VDD1=1.8V VDD2=1.1V VDDQ=0.6V	BUCK1=1.8V BUCK4=1.1V LDO1=0.6V	
LPDDR3 VDD1=1.8V VDD2=1.2V VDDQ=1.2V	BUCK1=1.8V BUCK4=1.2V LDO1=1.2V	

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5 Operating mode transition

5.1 Operating mode

The PCA9460 has five power operating states: OFF State, SNVS State, RUN State, PWRUP State, and PWRDN State. In the RUN state, there are three operating modes: ACTIVE mode, STANDBY mode, and DPSTANDBY mode.

5.1.1 OFF state

In the OFF state, PCA9460 has no VSYS pin voltage.

When the VSYS pin voltage falls below the VSYS_POR (Power On Reset) threshold voltage, the PMIC transitions to OFF mode from any other mode. In this state, all regulators are turned off and all internal registers of the PMIC are reset.

5.1.2 SNVS state

In the SNVS state, PCA9460 supplies power to the SNVS block of the i.MX 8ULP.

When VSYS exceeds the VSYS_UVLO rising threshold, the PCA9460 enters SNVS (secure nonvolatile storage mode). LDO_SNVS is turned on within 20 ms. After LDO_SNVS is turned on, it monitors the power-on source signal and enters the PWRUP state LDO_SNVS is turned on within 20 ms.

5.1.3 PWRUP state

In the PWRUP mode, PCA9460 regulator starts power up sequence.

When the internal signal PMIC_ON_SRC generated by the status of the PMIC_ON_REQ, PMIC_RST_B, and ACOK_B signals is asserted HIGH during the SNVS state, the power-on sequence initiates power-up of the regulator.

See Section 5.3.1 for power up sequence.

5.1.4 RUN state

In the RUN mode, PCA9460 regulators are turned on.

The PCA9460 transitions to the RUN state after the PWRUP state. When PMIC_ON_SRC is asserted LOW, the PCA9460 transitions to the PWRDN State.

5.1.4.1 ACTIVE mode

When the PCA9460 transitions from the PWRUP state to the RUN state, it first transitions to the ACTIVE mode. Then it transitions to STANDBY mode or DPSTANDBY mode depending on the PMIC_STBY or PMIC_DEEP_STBY signal.

5.1.4.2 STANDBY mode

When PMIC_STBY is HIGH and the STANDBY_CFG bit in the SYS_CFG1 register is set to “0b”, the PCA9460 enters STANDBY mode.

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5.1.4.3 DPSTANDBY mode

When PMIC_STBY is HIGH and the STANDBY_CFG bit in the SYS_CFG1 register is set to “1b”, the PCA9460 enters DPSTANDBY mode.

5.1.5 PWRDN state

In the PWRDN state, PCA9460 regulator starts the power down sequence.

See Section 5.3.2 for power down sequence.

5.2 Operating mode transition table

5.2.1 State transition table for VSYS terminals and major terminals

The state transitions of the VSYS pin and major pins are shown in Table 4. The "*" in the table means that the input signal level has no effect on the operating mode transitions.

Table 4. State transition table for VSYS pin and major pins

	I/O	OFF State	SNVS State	PWRUP State	ACTIVE mode	STANDBY mode	DPSTANDBY mode	PWRDN State
VSYS	I	< VSYS_UVLO	> VSYS_UVLO	> VSYS_UVLO	> VSYS_UVLO	> VSYS_UVLO	> VSYS_UVLO	> VSYS_UVLO
PMIC_ON_SRC	I	*	LOW	HIGH	HIGH	HIGH	HIGH	LOW
PMIC_STBY_REQ	I	*	*	*	LOW	HIGH	HIGH	*
STANDBY_CFG bit	bit	*	*	*	*	0	1	*
POR_B	O	LOW	LOW	LOW	HIGH	HIGH	HIGH	LOW

5.2.2 Regulator state transition table by mode of operation

Table 5 shows the operating conditions of the regulator in each operating mode. The "*" in the table means that the output signal level is undefined.

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Table 5. Regulator state transition table by operating mode

	OFF State	SNVS State	PWRUP State	ACTIVE mode	STANDBY mode	DPSTANDBY mode	PWRDN State
BUCK1	OFF	OFF	*	1.8V	1.8V	1.8V	*
BUCK2	OFF	OFF	*	1.0V	1.0V	1.0V	*
BUCK3	OFF	OFF	*	1.0V	1.0V	1.0V	*
BUCK4	OFF	OFF	*	1.1/1.2V	1.1/1.2V	1.1/1.2V	*
LDO1	OFF	OFF	*	0.6/1.1/1.2V	0.6/1.1/1.2V	0.6/1.1/1.2V	*
LDO2	OFF	OFF	*	3.3V	3.3V	3.3V	*
LDO3	OFF	OFF	*	3.3V	3.3V	3.3V	*
LDO4	OFF	OFF	*	1.8V	1.8V	1.8V	*
LDO_SNVS	OFF	3.0V	3.0V	3.0V	3.0V	3.0V	3.0V

5.3 Power up/down sequence

Figure 5 shows the power up/down sequence.

POK in Figure 5 means output power good or power OK and indicates that 85 % of the set output voltage has been reached.

PUD_T1~16 Gr indicates the order of rise and fall control for each BUCK and LDO.

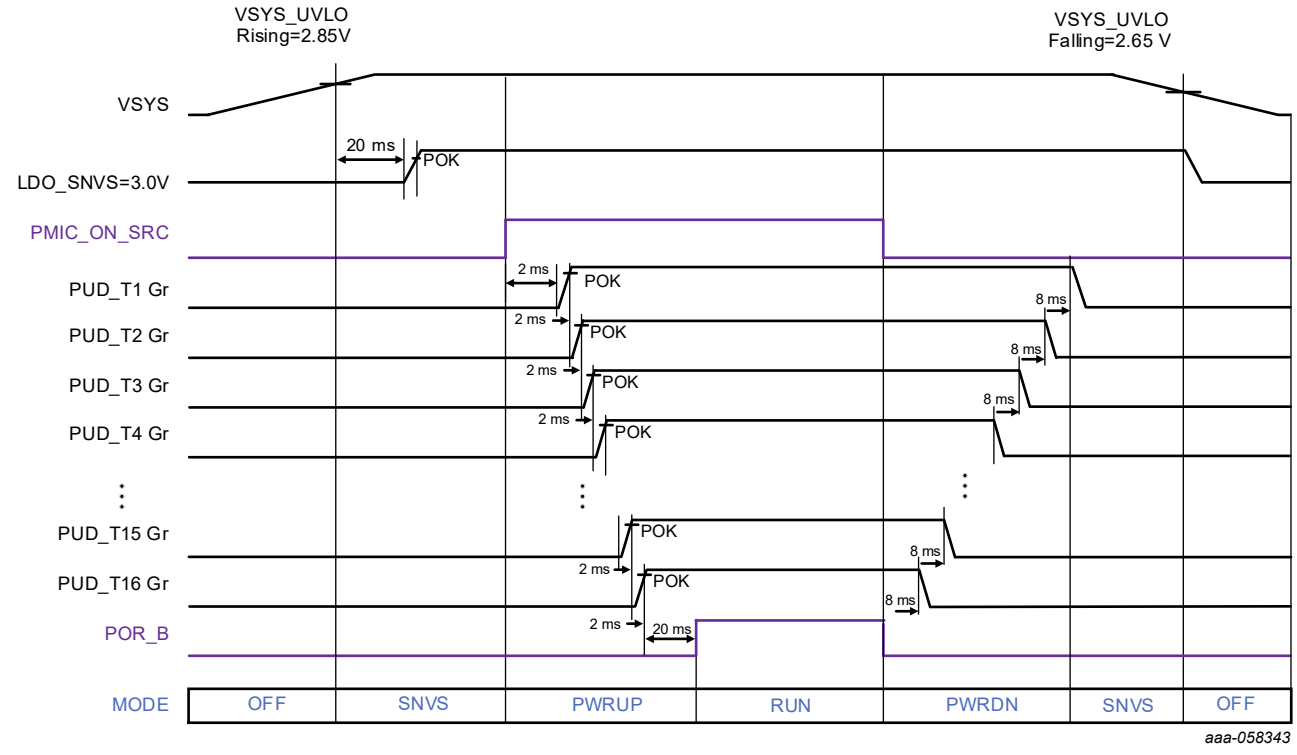

Figure 5. Power up/down sequence

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5.3.1 Power up sequence

When the VSYS pin voltage exceeds the VSYS_UVLO (under voltage lock out) voltage, the device transitions to SNVS state and LDO_SNVS starts output after 20 ms.

When a HIGH level signal is applied to the PMIC_ON_SRC signal from the i.MX 8ULP in SNVS State, it transitions to PWRUP State. 2 ms after that point, the power up sequence starts and each regulator rises in the order of PUD_T1 Gr, PUD_T2 Gr,...,PUD_T15 Gr, PUD_T16 Gr, and PUD_T16 Gr, in that order. When each regulator output voltage reaches POK, the next regulator starts rising at 2 ms intervals. The last PUD_T16 Gr output voltage reaches POR, and 20 ms later the POR_B signal (i.MX 8ULP reset release) rises and the RUN state is entered.

5.3.2 Power down sequence

When a LOW level is applied to the PMIC_ON_SRC signal in the RUN state including ACTIVE/STANDBY/DPSTANDBY mode, the state changes to the PWRDN state, the POR_B signal falls, and the power down sequence starts. Thereafter, each regulator output is stopped at 8 ms intervals in the reverse order of the power up sequence. When the last PUD_T1 Gr stops, it transitions to SNVS state.

5.4 STANDBY mode transition

Figure 6 shows the transition between ACTIVE mode and STANDBY mode controlled by the PMIC_STBY_REQ pin. The PCA9460 transitions from ACTIVE mode to STANDBY mode. On the other hand, when a LOW level signal is applied to the PMIC_STBY_REQ pin, the PCA9460 returns to ACTIVE mode.

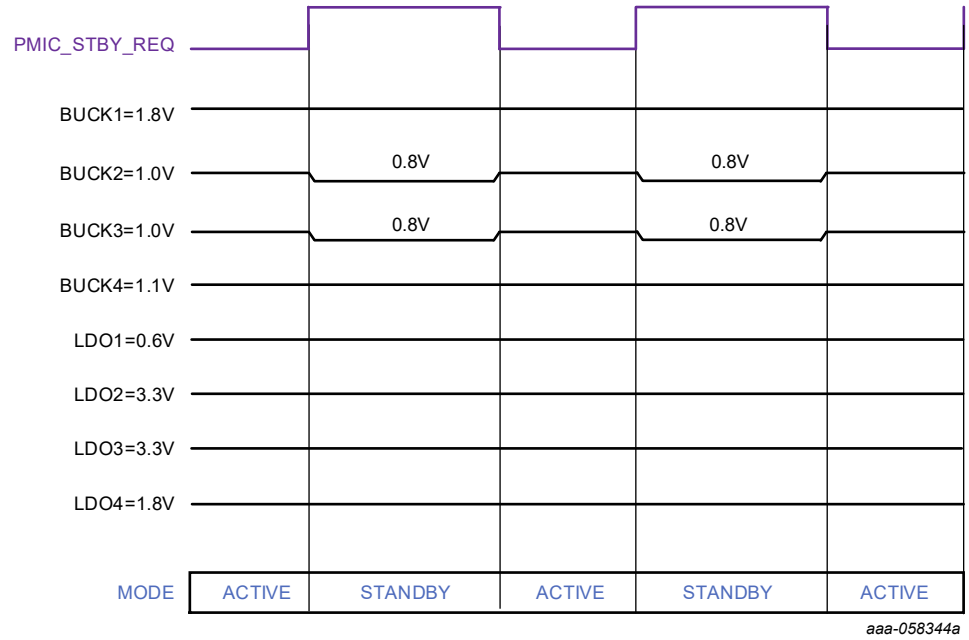

Figure 6. STANDBY mode transition

BUCK2 and BUCK3 of the PCA9460 have the DVS (dynamic voltage scaling) function, which allows the output voltage to be changed between BUCKxOUT_DVS0 (Active mode voltage setting) and BUCKxOUT_STBY (STANDBY mode voltage setting) depending on the PMIC_STBY_REQ pin status.

In the example in Figure 6, BUCK2 and BUCK3 are set to 1.0 V during ACTIVE mode, and BUCK2 and BUCK3 are set to 0.8 V during STANDBY mode.

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6 System function blocks

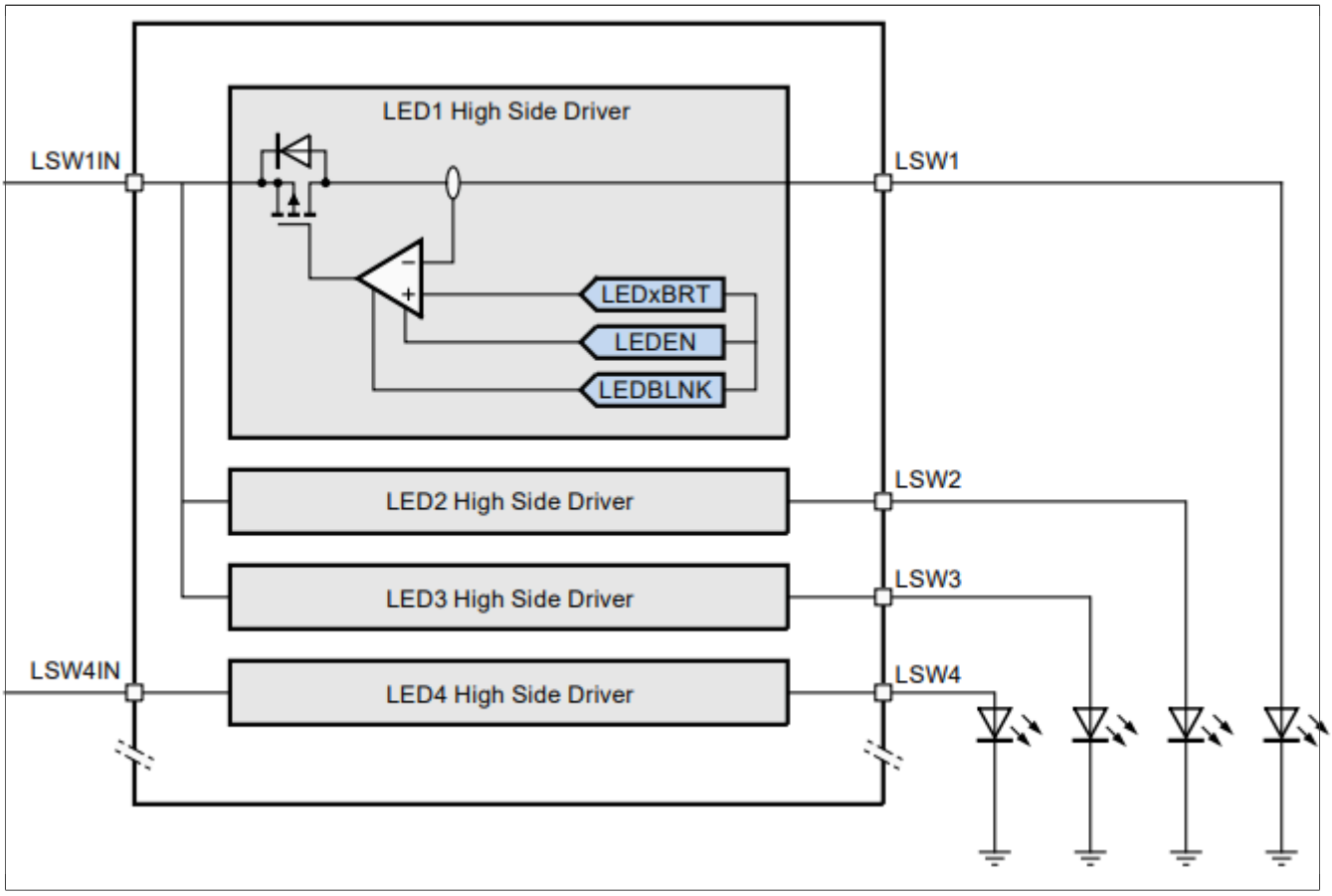
6.1 Load switch and LED driver

The PCA9460 has four built-in switches that can be configured via I2C to be load switches or LED drivers.

Load switch: Power can be deactivated to the i.MX 8ULP or devices on board depending on the situation.

LED drivers: can provide added value to LED lighting such as brightness change, blinking, dimming, etc.

Table 6. Built-in load switch/LED driver



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3. MCIMX8ULP-EVK evaluation kit: http://www.nxp.com/MCIMX8ULP-EVK

8 Revision history

Table 7. Revision history

Document ID	Release date	Description
AN14468 v.1.0	21 January 2025	• Initial version

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