AN14459

Differences Between S12ZVM and S32M2xx

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Document information

Information	Content
Keywords	S12ZVM, S32M24x, S32M27x
Abstract	This application provides the main differences between the S12ZVM and the S32M2xx family, and the general considerations when migrating.

1 Introduction

This document provides the main differences between the S12ZVM and the S32M2xx family, and the general considerations when migrating. This document intends not only to have a general overview of the two devices but also provide the users the tools to evaluate any possible migration from the S12ZVM platform to the newest S32M2xx platform.

Although the focus is going to be mostly on S32M244 device (Cortex M4F, grade 0, and 512 kB device) this comparison applies as well for the remaining S32M2 family members (Cortex M7, Grade 1, etc).

2 High level change summary

Taking the S12ZVM as a reference point, Table 1 below shows the high level changes and presents the features for S32M24x and S32M27x family members. This table also includes a difference column to indicate the degree of change.

This “difference” column is classified as high, mid and low. Even though features marked as high requires a big change in the SW, users are not expected to change/migrate/create the low level drivers, as part of the basic software enablement, S32M2 include evaluation software and drivers, rather user should be able to see the possibility to implement their application level in this new platform.

Table 1. S12ZVM and S32M2xx

	Family name	S12ZVM	Diff	S32M24x	S32M27x
Memory & Security	Embedded Flash	Up to 256KB	M	Up to 512 kB	Up to 1 MB
	OTA	SW	M	SW	HW (A/B swap)
	D-Flash	NA	H	64 kB	64 kB
	EEPROM	Up to 1 kB	H	4 kB (via D-Flash / Flex NVM)	SW EEEPROM driver
	Total RAM	Up to 32 kB	M	Up to 64 kB (*)	Up to 128 kB (*)
	Security solution	NA	H	CSEc	HSE_B
Safety	Safety / ASIL	A	M	B	B
	Internal Safety Monitor (Watchdogs)	WDOG	H	WDOG, EWM & AE_WDOG	POR_WDOG, SWT & AE_WDOG
Core/ performance	Core	S12Z CPU core	H	Arm® Cortex-M4F	Arm® Cortex-M7
	Frequency [MHz]	Up to 50 MHz	M	Up to 80 MHz	Up to 120 MHz
	DMA	NA	H	16ch	12ch
Communication	CAN	1xCAN2.0	H	1xCANFD	C – 2x CAN-FD* L – 3x CAN-FD*
	Serial comm	1xSCI	H	1x LPUART(**)	C – 2xLPUART* L – 3x LPUART*
	SPI	1xSPI	H	2x LPSPI (**)	C – 1xLPSPI L – 2x LPSPI
	I2C	NA	H	1x LPI2C	1 x LPI2C
	FlexIO	NA	H	7ch	9ch
Analog & Timers	12-bit ADC	2xADC	M	2xADC (C - 6ch, 7ch)	2xADC

Table 1. S12ZVM and S32M2xx*...continued*

	Family name	S12ZVM	Diff	S32M24x	S32M27x
		(up to 16ch)		(L - 8ch, 7ch) (*)	16 ch each ADC (check the IOMUX for the pin availability)
	CMP	NA	H	1 x LPCMP (3x external channel inputs)	1 x LPCMP (4x external channel inputs)
	Timer/PWM	1xPMF (6ch)	H	4xFTM (C - 6ch,5ch,7ch,2ch) (L - 6ch,6ch,7ch,2ch) (*)	2xEMIOS (C -15ch, 5ch) (L -16ch, 6ch) (*)
	PDB, BCTU, LCU, TRGMUX, PTU	PTU	H	TRGMUX PDB	TRGMUX LCU BCTU
	Other Timers	TIM	M	LPIT, LPTMR, RTC	LPIT, STM, RTC
Integrated Components	Integrated 12V regulator	Yes	L	Yes	Yes
	Supply for external components	ZVMC256 Only. (20 mA)	M	5V (30 mA)	5V (30 mA)
	Physical interface option	LIN or CAN	M	LIN/CXPI or CAN/ CANFD	1x LIN/CXPI or 1x CAN/CANFD
	MOSFET Gate Driver Unit (GDU)	6 ch (3 ph)	L	6 ch (3 ph)(*)	6 ch (3 ph)(*)
	Temperature sensor	Yes	L	Yes (*)	Yes (*)
	High Voltage Input	ZVMC256 Only	L	Yes(*)	Yes(*)
	Current Sense	2xOpAmp	M	1xDPGA (*)	1xDPGA (*)
	Battery monitoring	Yes	L	Yes	Yes

Note:

- **C is for CAN variant. L is for L variant.*
- *** One more UART interface for use with LIN Phy, One more SPI interface for use with AE.*

3 Platform architecture

S32M24x, S32M27x and S12ZVM architectures are different, while S12ZVM incorporates a propieatary CPU core, S32M2 family integrates an Arm Cortex (M4 and M7), also there are differences in the memory architectures and peripheral connections, in the following figures we can see the architectures of both families.

The Figure 1 shows the block diagram for S12ZVM, the Figure 2 shows the block diagram for S32M24x, Figure 3 show the block diagram for S32M27x. LIN and CAN Phy interfaces are available in both families, but only one per variant (LIN variant has a LIN Phy and CAN variant has a CAN Phy).

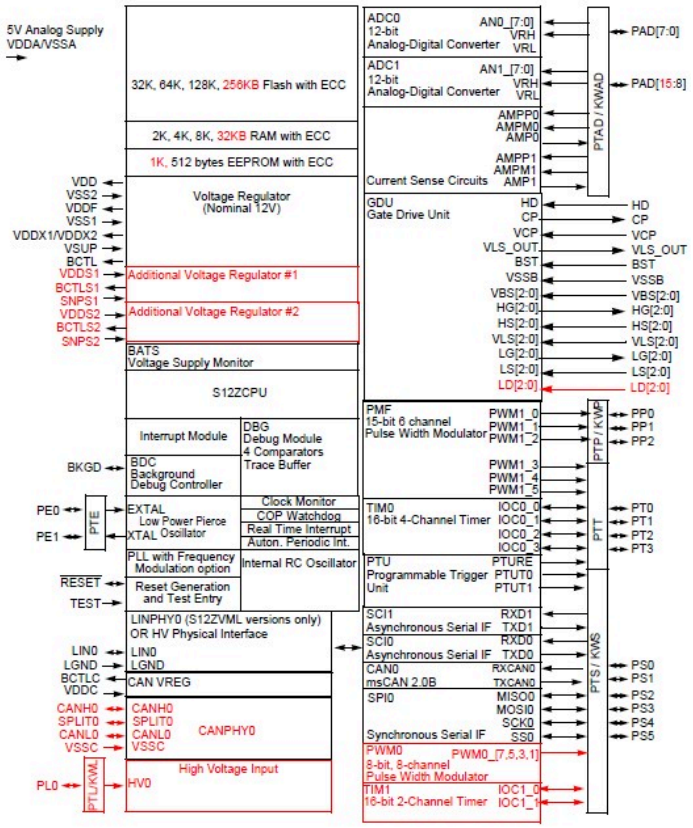

Figure 1. S12ZVM block diagram

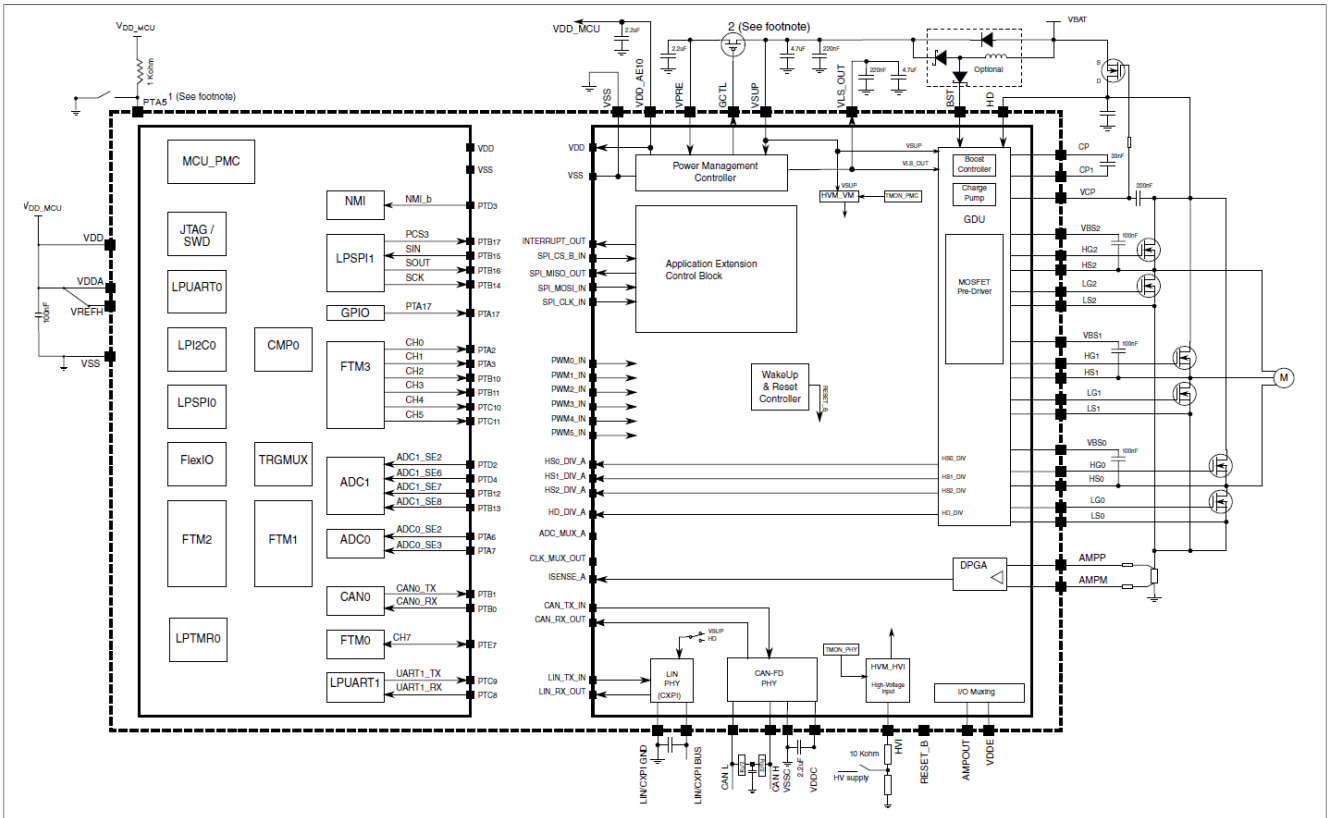

Figure 2. S32M24X block diagram

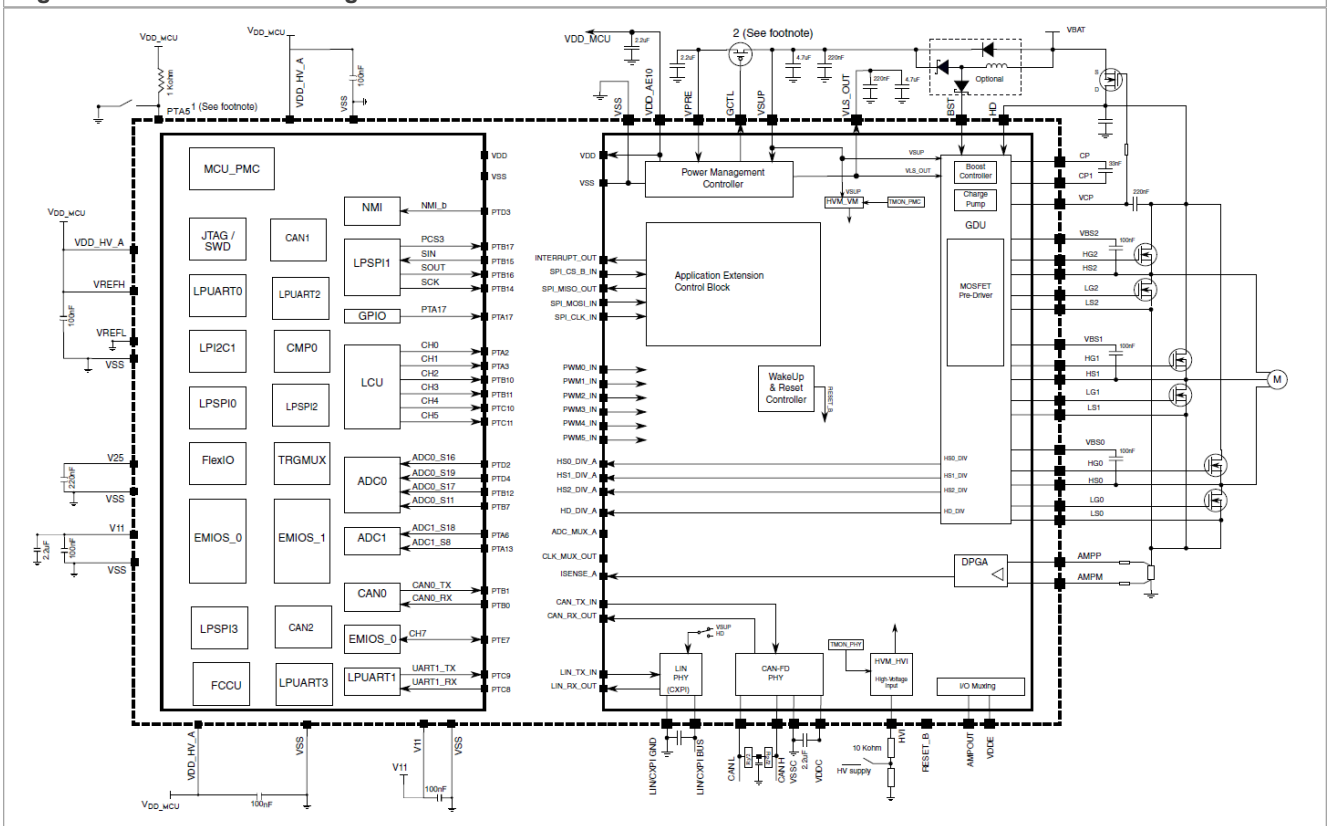

Figure 3. S32M27X block diagram

Table 2. Platform differences

Feature	S12ZVM	S32M24x	S32M27x
Core	S12ZCPU	Arm Cortex M4F	Arm Cortex M7
	Up to 50MHz	Up to 80MHz	Up to 120MHz
TCM support	No	No	Yes
eDMA	No	Yes	Yes
XBAR	No	Single Bus	Single Bus
Communication between application extension and the main core	NA	Via SPI	Via SPI
Low power RAM	No	Yes(*)	32KB
Security core	No	cSEC	HSE_B

Note: **No size specified on S32M24X devices because on low power modes, all the SRAM can retain the information.*

The S32M2xx family offers faster CPUs, higher performance on both peripherals and CPU, with the advantages on the core architecture (moving to ARM Cortex M4F in the case of S32M24x and ARM Cortex M7 for S32M27x), features such as low power RAM, communication through the extension at SPI frequencies (up to 10MHz for the AE).

Also, the S32M2xx family offers security cores for tasks such as encryption, decryption, etc.

4 Memory and OTA

Please find below an extended comparison between the different memories and their interfaces between S12ZVM and S32M2xx.

Table 3. Memory general differences

Feature	S12ZVM	S32M24x	S32M27x
Embedded Flash	Up to 256KB (*)	Up to 512 kB	Up to 1 MB
Data Flash	NA	64 kB	64 kB
Flash memory controller cache	NA	Yes (single speculative prefetch buffer only)	Yes (256-bit may be buffered in each of prefetch buffer for AHB Port0 and Port1)
Random-access memory (RAM)	Up to 32 kB (*)	Up to 64 kB (Including 4 kB of FlexRAM)	Up to 128 kB SRAM (including 96 kB of TCM)
FlexRAM (also available as system RAM)	NA	Up to 4 kB	NA
Tightly coupled memory (TCM)	NA	NA	64 kB DTCM and 32 kB ITCM
Low power SRAM memory	NA	RAM retained in all modes	Up to 32 KB with Standby mode retention
Error Correcting Code	Yes	Yes	Yes
Cache	NA	4 KB	8 KB data and 8 KB instruction cache

Table 3. Memory general differences*...continued*

Feature	S12ZVM	S32M24x	S32M27x
EEPROM	Up to 1 kB	Up to 4 kB (Via 64 kB D-Flash / FlexNVM / 4 kB FlexRAM).	Software

There are significant improvements regarding memory architecture from S21ZVM devices to S32M2 family, each of the S32M2 variant have its own particularities that contribute to have a better performance and the best usage of the resources.

4.1 RAM

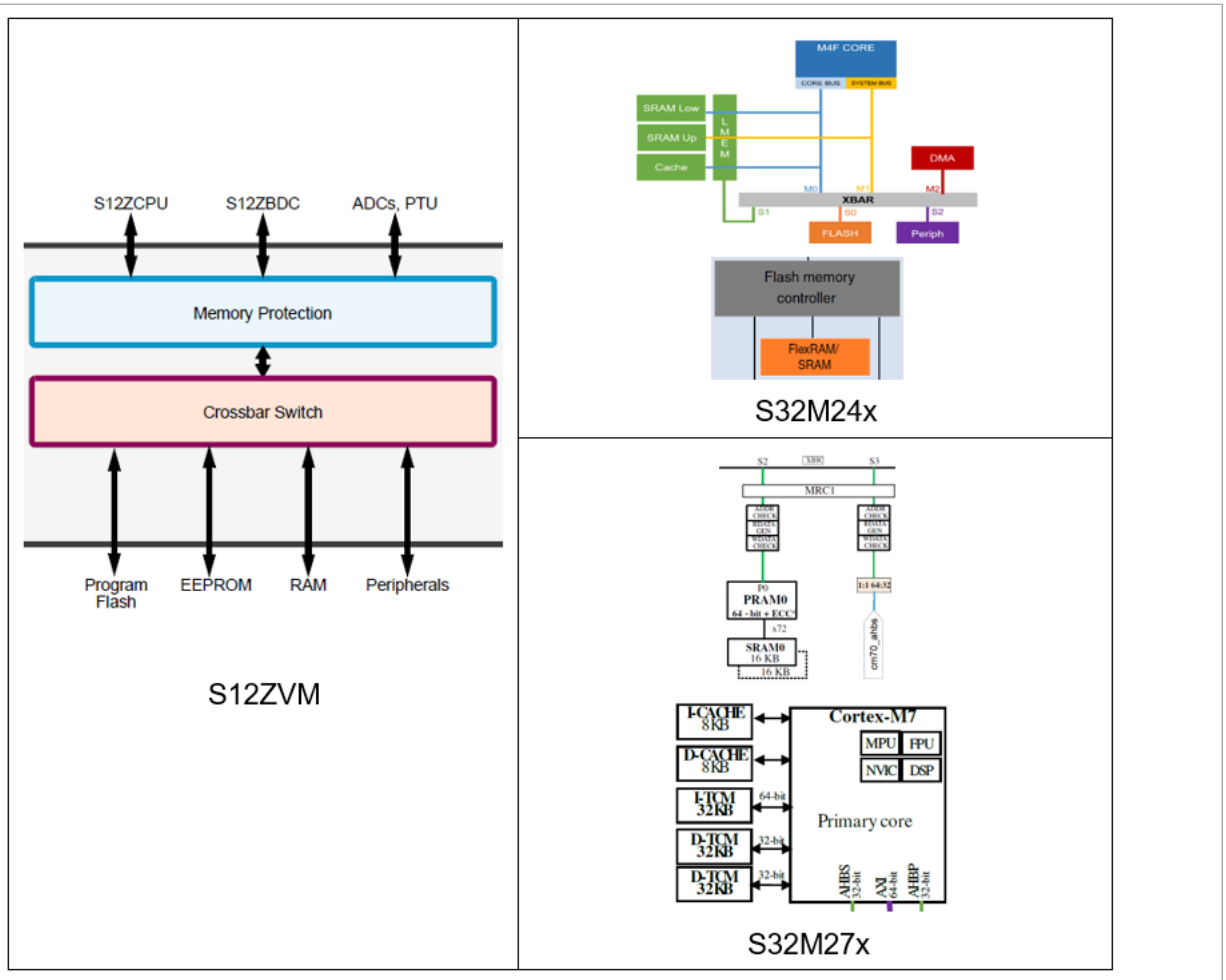

Figure 4. RAM block diagram example

In terms of RAM memory, we can find that the main differences lie in the size and performance.

The max size of RAM memory we can have in Carcassone (CC) is only in the S12ZVMC256 with 32 kB, and excluding this device, most of the CC devices have below 8 kB of RAM memory. On S32M2 devices we not only have more memory (64 kB to 128 kB), but also we have a better performance.

While in Carcassone devices we find an access port of 16 bit, in S32M2 devices we have 32 and 64 bits for S32M24x and S32M27x, representing better access timings. Also, it is important to consider that S32M27x have the TCM memory which is a single clock cycle access memory, giving the best option for variable constantly changing (i.e. PWM for motor control variable).

4.2 Flash

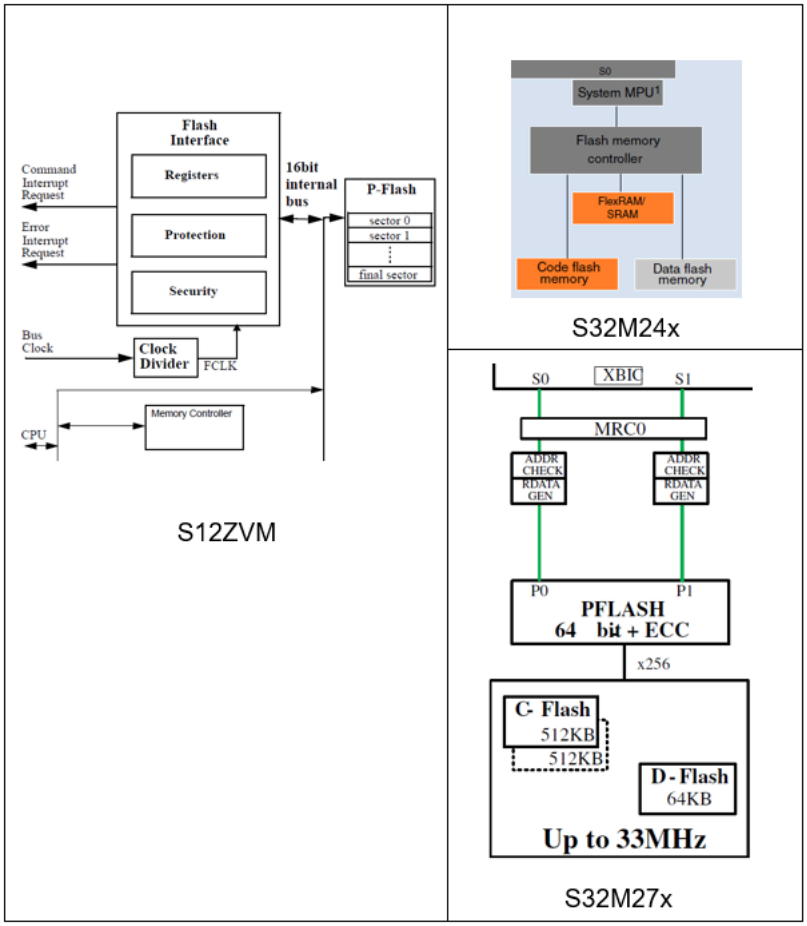

Figure 5. Flash block diagram example

Similar to the RAM, the Flash memory is other of the features that improve mainly in performance and sizes on the S32M2.

On S32M2 we can find flash memory from 256 kB to 1 MB, and added to this we also have 64 kB of Data Flash memory region. D-Flash memory can be used for data storage; data which does not change constantly and could keep its value through POR.

On S12ZVM we can find up to 256 kB of flash memory (only in ZVMC256), and we don't have a Data Flash, but it does have a EEPROM memory, this will be discussed in the EEPROM, FlexNVM and TCM section.

Now, in terms of the access port we also have a better performance on S32M2 devices, for CC we find a 16 bits port, while in S32M2 we find 32bit and 64bits port for the FTFC (S32M24x) and PFLASH (S32M27x) controllers.

4.3 EEPROM, FlexNVM and TCM

S12ZVM includes an EEPROM memory which can be used for data storage (the same way that the D-Flash on S32M2 family), this block of memory can go up to 1 kB (only on ZVMC256). This size of memory represents a limitation in comparation with the D-Flash included in S32M2.

We remark here the FlexNVM memory of the S32M24x devices which via a D-Flash partition used as backup, and with the FlexRAM as RAM buffer interface to the user, allows an emulated EEPROM by hardware. This

EEEPROM programs data automatically into the FlexNVM block using a hardware built-in filing system and allow a high endurance flash interface.

For the case of the S32M27x, FlexNVM interface is not supported, but if required, user could implement a EEPROM by software using a typical emulation EEPROM algorithm, as reference we can consult AN4868.

5 Clock, power management, reset & boot

5.1 Power management & operating modes

One of the main differences in the S12ZVM and the S32M2 is the power modes. The typical power modes in the legacy cores (i.e. S12ZVM) are Run, Wait, and Stop mode, while in the ARM® Cortex (S32M2) architectures we found Run, Sleep, and Deep Sleep modes. Nevertheless, in S32M2 family (and other S32 families), we can found its own power modes implementations.

While S32M2xx family use ARM Cortex M cores, the S32M2 family offers additional power modes, in combination with the AE:

Table 4. S32M24x power modes

S32M24x Power Mode	MCU Power Mode	AE Power Mode	MCU VDD
RUN_SiP	RUN	RUN	Powered
SLEEP_SiP	VLPS	SLEEP	Powered (low power)
DEEPSLEEP_SiP	MCU powered OFF	DEEP SLEEP	Unpowered

While ARM offers Run, Sleep and Deep Sleep modes, in combination with AE power modes, we can get the following modes:

- AE RUN Mode:
  - MCU can use the following power modes:
    - RUN
    - VLPR
    - VLPS
- AE Sleep Mode:
  - MCU can use the following power modes:
    - VLPS
- AE Deep Sleep Mode
  - MCU is unpowered

Table 5. S32M27x Power Modes

S32M27x Power Mode	MCU Power Mode	AE Power Mode	MCU VDD
RUN_SiP	RUN	RUN	Powered
DEEPSLEEP_SiP	MCU powered OFF	DEEPSLEEP	Unpowered

For the S32M27x, we can use Run mode in the AE with Run or Standby mode of the MCU. While in DeepSleep, the MCU gets unpowered

A very important topic to keep in mind when developing low power applications on these platforms is the behavior of the chip when waking up, we need to follow a sequence in order to avoid an overcurrent while AE is in sleep mode and we are going back to RUN mode in the MCU side.

The power mode transition of the S32M2xx is available in S32M2 power modes for the system-in-a-package chapter of the RM (both S32M24x and S32M27x RM), refer to it for the power mode transitions and considerations using the different power modes.

S32M24x SiP as well as the S12ZVM can use any interrupt available for wakeup, since we have the AWIC in S32M24x(Asynchronous Wake-Up Interrupt Controller). S32M27x SiP incorporates the WKPU to configure wake-up events.

In the following table, we have the available modules in low power modes of the MCU.

- FF: Full functionality (SW configurable)
- Async operation: FF with alternate clock source

Table 6. S12ZVM & S32M2x module operation in low power mode

Modules	S12ZVM Stop	S32M24x Stop	S32M24x VLPS	S32M27x Standby
System				
Core	Off	Off	Off	Off
LVD / LVR	LVR Active	Both Active	LVR Active	LVR Active
DMA	NA	Async operation	Async operation	Off
Watchdog	Active in Pseudo Stop	Async op. (STOP1) FF (STOP2)	Async operation	FF
Clocks				
LPO	NA	FF	FF	Off
PLL	Active in Pseudo Stop	FF	Off	Off
Internal Reference Clock	Off	FF	SIRC FF FIRC Off	FF
SXOSC / SOSC / FXOSC	Active in Pseudo Stop	FXOSC/SOSC FF	Off	FF
Communication				
UART	FF in wait mode Off in stop (Wakeup option)	Async op. (STOP1) FF (STOP2)	Async operation	OFF
LPSPI	FF in wait mode Off in stop (Wakeup option)	Async op. (STOP1) FF (STOP2)	Async operation	OFF
I2C	NA	Async op. (STOP1) FF (STOP2)	Async operation	OFF
FlexIO	NA	Async op. (STOP1) FF (STOP2)	OFF	OFF
CAN	FF in wait mode Off in stop (Wakeup option)	PNET (CAN0)	OFF	OFF
Timers				
LPIT / RTI0 / TIM	FF in wait mode Off in stop (No wakeup)	Async op. (STOP1) FF (STOP2)	Async operation	FF

Table 6. S12ZVM & S32M2x module operation in low power mode...*continued*

Modules	S12ZVM Stop	S32M24x Stop	S32M24x VLPS	S32M27x Standby
System				
LPTMR	NA	Async op. (STOP1) FF (STOP2)	Async operation	NA
RTC	NA	Async op. (STOP1) FF (STOP2)	FF	FF
Safety				
CRC	NA	Available in STOP2	OFF	OFF
Analog				
CMP	NA	Low-speed and High-speed (STOP1) FF (STOP2)	Low-speed compare	FF
ADC	FF in wait mode Off in stop (No wakeup)	OFF (STOP1) FF (STOP2)	OFF	OFF
Human Machine Interface				
PIM / PORT / SIUL2	FF	Async op. (STOP1) FF (STOP2)	Off	Off
Integrated components				
Integrated regulator	RPM (reduced performance mode)	MCU – AE/RUN (Full performance mode) AE – LPM	MCU&AE – SLEEP (Low power mode)	MCU&AE – SLEEP (Low power mode)
CAN Phy		Listen Only	Listen Only	Sleep
LIN Phy		Listen Only	Listen Only	Sleep
HVI		Low power	Low power	Low power
GDU		Low power	Off	Off
DPGA		Low power	Off	Off

In S32M24x we have different wake-up sources, while in SLEEP_SiP we can have wake up from the MCU or the AE, in DEEPSLEEP_SiP only AE wake-up sources are available since the MCU is powered off.

While in the S32M27x, only the DEEPSLEEP_SiP mode is available (MCU+AE low power mode) and only the AE wake-up sources are available.

The Cortex M0+, M4 and M7 have the Asynchronous Wake-up Interrupt Controller (AWIC), additionally, the S32M27x incorporates the WKPU unit to configure wake-up events, however, what we compared in the table below are the available wake-up sources.

Table 7. S32M24x & S32M27x wake-up sources

S32M24x - Stop and VLPS	S32M27x - Standby
Available System Resets (RESET_b, POR, JTAG)	
Any enabled pin interrupt	Up to 60 GPIO pins (check the IOMUX in the RM for the available ones)
ADCx	Not available in Standby mode

Table 7. S32M24x & S32M27x wake-up sources...*continued*

S32M24x - Stop and VLPS	S32M27x - Standby
CMP	Analog CMP (round-robin)
LPI2C0	Not available in Standby mode – Pin wakeup and then peripheral enablement is required
LPUART	
LPSPI	
LPTMR0	
RTC	RTC (API or timeout)
CAN0 (PNET)	Not available in Standby mode – Pin wakeup and then peripheral enablement is required
Non-maskable interrupt (NMI)	Single NMI pin.
WDOG	SWT0
FlexIO	Not available in Standby mode – Pin wakeup and then peripheral enablement is required
LPIT	RTI event
CRC	Not available in Standby mode
SGC	

5.2 Clocking architecture

In terms of clock sources, S32M24x and S32M27x are quite similar. If we ignore a few punctual differences (regarding some configuration registers and SoC integration aspects) we could summarize the clock sources comparison in the following table, they offer higher clock sources than the S12ZVM and also offer higher frequencies.

Table 8. S12ZVM, S32M24x and S32M27x clock sources

S12ZVM	S32M24x	S32M27x	Key comments
IRC 1MHz	Fast IRC 48 MHz	Fast IRC 48 MHz	Default clock source after reset in both architectures. S32M27x: cannot be disabled in RUN mode.
	Slow IRC 8 MHz	Slow IRC 32 KHz	S32M27x: can no longer be selected as the system clock.
XOSCLCP (4-20)MHz	SOSC (4-40) MHz	FXOSC (8-40) MHz	S32M27x: Two configurable params were added (amplifier transconductance and stabilization counter value). S32M27x: can no longer be selected as the system clock.
	LPO 128 KHz	SXOSC (32.768 KHz)	Intended RTC clock source for both architectures. S32M27x: new param added (stabilization counter value). S32M27x: SXOSC does not support trimming (as LPO).
IPLL (12.5-50)MHz	System PLL (90-160) MHz	PLL (48-320) MHz	S32M27x: VCO freq. up to 1280 MHz (S32M24x up to 320 MHz). S32M27x: Programmable frequency modulation and Lock detection circuitry were added. S12ZVM: VCO freq. up to 100MHz

When designing with S32M24x family, after selecting the desired system clock source (PLL, FIRC, SIRC, or SOSC) the user has to worry about three main clock nodes: CORE, BUS, and FLASH.

In S32M27x there are more clock nodes, they can be configured through different dividers and multiplexers, offering the CORE_CLK, AIPS_PLAT_CLK, AIPS_SLOW_CLK, HSE_CLK and DCM_CLK as the main ones, other clock nodes can be generated for peripherals such as FlexCAN.

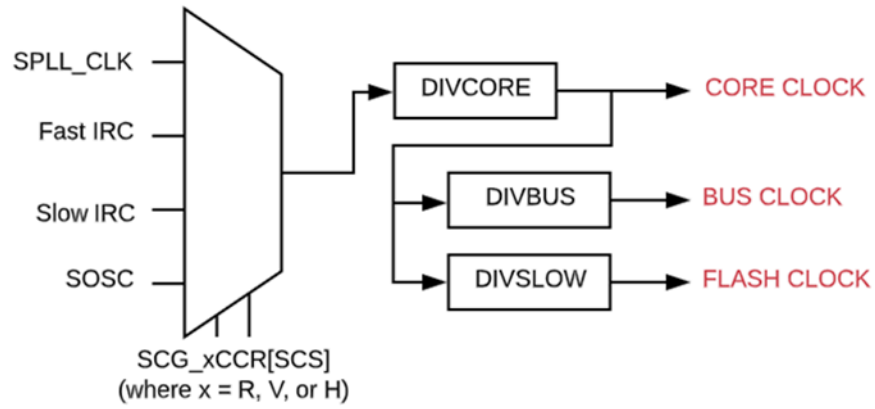

Figure 6. S32M24x system clocking

On the other hand, when moving forward with S32M27x chips, we have fewer options to clock the system (PLL or FIRC), but the number of system clock nodes increases, Figure 7 show some of the clocking nodes, there are more nodes such as FlexCAN clocking or STM0_CLK.

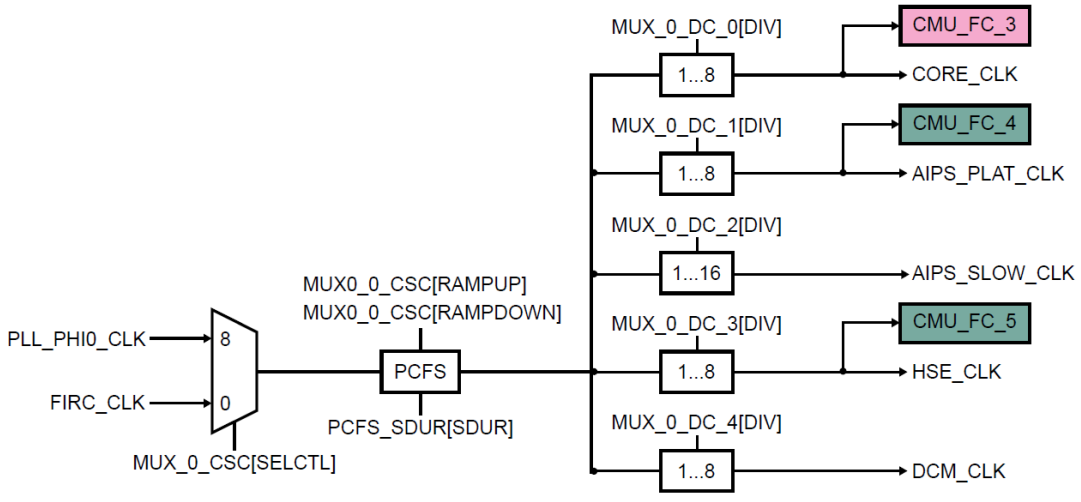

Figure 7. S32M27x system clocking

5.2.1 Considerations to migrate to S32M2XX family.

An important point to highlight is how the clocking nodes are distributed to the peripherals within each platform. For S32M24x, each clock source has two divided branches, offering eight asynchronous peripheral clock sources for most peripherals.

In the S32M27x architecture, CORE_CLK, AIPS_PLAT_CLK and AIPS_SLOW_CLK nodes are in charge of feeding the SoC modules. Some peripheral clocking examples are compared below. For more detail please refer to the corresponding RM.

In the S12ZVM architecture, there are Bus Clock, System clock, Core Clock and Oscillator clock, peripherals such as MSCAN can use the external oscillator clock, while SPI uses the Bus Clock, and it can be derived from IRC or PLL.

Table 9. S12ZVM/S32M24x/S32M27x module clocking examples

IP	S12ZVM	S32M24x	S32M27x
MSCAN/ FlexCAN Protocol Engine	Oscillator Clock Bus clock	SOSCDIV2_CLK	AIPS_PLAT_CLK
		SYS_CLK	FXOSC_CLK
			FIRC_CLK
PMF / FTM / eMIOS Counter Clock	Core Clock	SOSCDIV1_CLK	CORE_CLK
		SIRCDIV1_CLK	
		FIRC_DIV1_CLK	
		SPLLDIV1_CLK	
		TCLKn (Pad)	
		RTC_CLK	
		SYS_CLK	
ADC Conversion Clock	System Clock	SOSCDIV2_CLK	CORE_CLK
		SIRCDIV2_CLK	
		FIRCDIV2_CLK	
		SPLLDIV2_CLK	

As we can see in the previous table, the S32M2xx family offers more clock options, in the case of the S32M27x, Core Clock can run up to 120MHz, it can be provided from the PLL with a divider so higher operation frequencies of some peripherals are possible.

As we can see in Table 10, S32M24x and S32M27x offers different features compared to S12ZVM in the way clock system is managed, offering more clock sources and nodes for peripheral clock feeding. Also in case of S32M27x there are more clock monitoring units for safety applications.

Table 10. S12ZVM/S32M24x/S32M27x clock features

Feature	S12ZVM	S32M24x	S32M27x
System Clocking settings (multiplexers and dividers) are done by	CPMU (Clocks, Reset & Power Management Unit)	SCG (System Clock Generator)	MC_CGM (Clock Generation Module)
Peripheral clock gating is performed by	CPMU	PCC (Peripheral Clock Controller)	MC_ME (Mode Entry Module)
Clock Monitoring Units	S12ZVM offers two clock monitors, for the PLL and for the Oscillator (XOSCLCP)	S32M24x has 2 instances to monitor clocking operation in safety-relevant applications, for System OSC and System PLL	Four new instances were introduced (6 in total), and two of them are frequency meters. We can monitor FXOSC, FIRC, SIRC, CORE_CLK, AIPS_PLAT_CLK and HSE_CLK
	CLKOUT pins for allowing the view of internal clocks are supported in both S32M2xx systems.		

5.3 Reset and boot

Broadly speaking, there are up to four different types of reset in the S32M2xx family, below are the reset sources in a nutshell. For more specific details, refer to the corresponding RM.

Table 11. S12ZVM/S32M24x/S32M27x reset sources

Event Type	S12ZVM	S32M24x reset sources	S32M27x reset sources
Power-on Reset (POR)	Supply voltage drops below specification	Supply voltage drops below specification	Supplies voltage drops below specification POR Watchdog time-out
System Reset	Asserting RESET pin		
	LVR (Low Voltage Reset)		
	COP / WDOG / SWT reset request Software reset OSC failure PLL loss of lock		
	NA		CMU detects a failure of: • CORE_CLK • AIPS_PLAT_CLK • HSE_CLK
	NA	Core attempts to enter Stop mode, but not all modules acknowledge the request	STANDBY exit (Destructive)
	NA		Self-Test Control Unit (STCU) • Self test done • Unrecoverable fault
	NA		Fault Collection & Control Unit (FCCU) Failure to react. Reset reaction
Debug Reset	NA	MDM-AP (resets via JTAG/SWD) JTAG module	
HSE Reset	NA		HSE SWT Timeout HSE boot reset Tamper Detect SNVS Tamper Detect

Note: *Many reset functions for the chip as well as the reset sequence monitoring are managed by the Reset Control Module (RCM) in S32M24x, and by the Reset Generation Module (MC_RGM) in the S32M27x.*

In terms of boot, the Table 12 presents the general considerations for both S32M24x and S32M27x.

Table 12. S32M2xx boot considerations

Event Type	S32M24x	S32M27x
System RAM ECC initialization	Yes	Yes
Vector Table Offset Register (VTOR) initialization	Yes	Yes
Watchdogs	Disable watchdog (WDOG) if not required.	Enable corresponding watchdog (SWTx) if required by application.

Table 12. S32M2xx boot considerations*...continued*

Event Type	S32M24x	S32M27x
Flash configuration	16 bytes of configuration data located at address 0x400: Contains boot options, Pflash/Dflash protection settings and flash security setting.	Device Configuration Format (DCF) records: A set of records stored in UTEST memory area to configure certain registers of the device during system boot.
Memory/resources protection	NXP System MPU configuration	ARM Cores MPUs configuration.XRDC Module to configure access policies of the bus masters to memory, peripherals and pin resources. -> If HSE security usage enabled: Application needs to provide static XRDC configuration structure. The structure is read by SBAF boot firmware to configure XRDC accordingly. -> If HSE security usage disabled: Application to configure XRDC in runtime.
Other	NA	Boot header A piece of data installed by the application, containing mainly the application cores to enable, boot address for each core, pointer to XRDC configuration (if HSE security usage enabled) and optional authentication tag.

6 Security

S32M2xx family integrates security modules, in S32M24x we have the CSEc module, it implements a comprehensive set of cryptographic functions. S12ZVM does not offer security modules.

S32M27x offers HSE-B, an engine powered by an ARM Cortex M0+, it supports different ciphering modes, a hash engine, random number generator. The S32M27x offers a Crypto driver which is a SW API that offers the capability to create the applications with the security integrated with an API, offering the possibility to integrate the same code as S32K3 family with HSE-B Crypto API.

In order to use HSE-B in S32M27x, the HSE firmware needs to be installed in the flash memory.

Also, Crypto driver can be used along with RTD drivers available for both S32M27x and S32M24x, offering the possibility to migrate the code from the family with almost the same configuration.

Table 13. S32M27x and S32M24x security considerations

		S32M27x	S32M24x
Security System		HSE-B	CSEc
Location in SoC architecture		Independent subsystem	Embedded within Flash Controller
Firmware Upgradable		Yes	No
Security Ciphers	Symmetric	AES-128/192/256 (50+ keys)	AES-128
	Cipher modes	ECB, CBC, CMAC, GMAC, CTR, OFB, CCM, GCM	ECB, CBC

Table 13. S32M27x and S32M24x security considerations...*continued*

		S32M27x	S32M24x
	Asymmetric	RSA (up to 4096 bytes) & ECC (up to 521 bytes)	No
	Hash	Miyaguchi-Preneel, SHA-2/SHA-3 (up to 521 bytes)	Miyaguchi-Preneel
Secure boot		Up to 32 flexible memory regions to verify. Authentication tag can be CMAC, GMAC or RSA/ECC signature	Secure boot as specified in SHE. Single memory area for verification using CMAC.
Random Number Generator		TRNG & PRNG (AIS & NIST compliant)	TRNG
Attack Resistance		Side Channel Resistance / Environment Monitoring	No
Code Flash		12 KB (used) shared memory with EEPROM emulation	<128 KB in Secured part of PFlash
Data Flash		2 x 8 KB (for Key Storage)	Depends on the number of keys, shared memory with EEPROM emulation
Requirement coverage		SHE+, Global-B, CYS 2200+, FCA Specification Customer Applications	SHE+ Global-B CYS 2200
Host Interface		Commands sent through the MU (Messaging Unit) registers. Input/output data shared through System RAM. Errors read from MU registers	Commands and input/output data sent through the CSE_PRAM dedicated memory. Error flags sent back also through CSE_PRAM. Status read through flash controller registers.

7 Safety

S32M2xx family covers ASIL B hardware requirements, along with the microcontroller, a safety library is provided to use with the family. The safety differences between S12ZVM, S32M24x and S32M27x is provided as following:

Table 14. S12ZVM/S32M24x/S32M27x safety differences

Feature	S12ZVM	S32M24x	S32M27x
Memory Protection Unit (MPU)	NXP proprietary	NXP proprietary	ARM*
Error Injection Module (EIM) Error Reporting Module (ERM)	Both	Both**	
Temperature sensor	YES (monitored via ADC)		
eDMA Controller	DMA controller	Yes**	
Clock monitoring units	2	2	6
Interconnect bus	Crossbar switch	Crossbar switch (AXBS-Lite) + Peripheral Bridge (AIPS-Lite) **	
External Watchdog Monitor	Yes		Yes, Resolved via FCCU
PMC (Power management control)	Yes	PMC with ASIL B	PMC with ASIL B

Table 14. S12ZVM/S32M24x/S32M27x safety differences...*continued*

Feature	S12ZVM	S32M24x	S32M27x
		AE Power Management Controller	AE Power Management Controller

Note:

- **New features added using XRDC module.*
- **New features added using XRDC module*

Either S12ZVM or S32M2xx family, we can achieve ASIL-B, but only the S32M2xx family is a SafeAssure solution:

Figure 8. Functional Safety overview

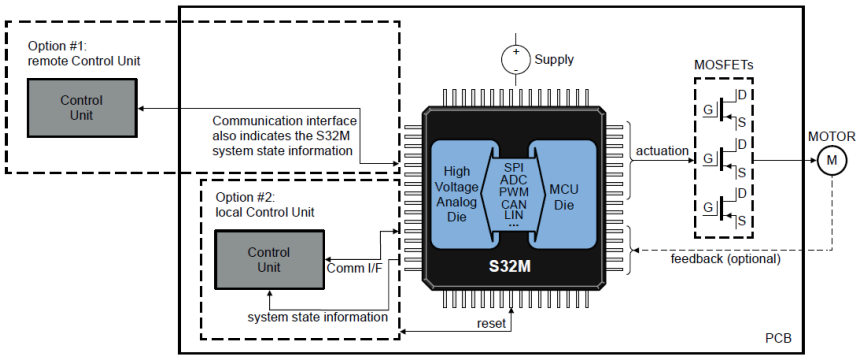

Figure 9. S32M2 as integrated solution for motor control application

7.1 Considerations on safety for S32M2xx and S12ZVM.

ASIL B application running on S12ZVM can be migrated to S32M2xx family, for S32M27x a safety software framework is offered. To migrate the application, some considerations need to be determined in order to verify the safety application.

8 Timing, cross triggering and ADC

This set of IP modules are commonly used, together, for many automotive use cases: ADC, BCTU, eMIOS, LCU and TRGMUX. shows the main differences between S32M24x and S32M27x.

S12ZVM does not offer a TRGMUX that allows to interconnect the different peripherals

Table 15. S32M24x and S32M27x TRGMUX differences

TRGMUX	S32M24x	S32M27x
I/O	Inputs: 255 Outputs: 128	Inputs: 128 Outputs: 158 Added eMIOS odis signals Added LPUART RX, TX, IDLE Added LCU1_LCU2 I/O support

Table 16. S12ZVM, S32M24x and S32M27x ADC differences

ADC	S12ZVM	S32M24x	S32M27x
Instances / Channels	ADC: Up to 8 external channels	ADC_0: Up to 16 single-ended external analog inputs ADC_1: Up to 16 single-ended external analog inputs	ADC_0: 16 standard channels 32 external channels* ADC_1: 16 standard channels 32 external channels*
Resolution	12-bit resolution (configurable)	12-bit resolution (configurable)	14-bit resolution (configurable)
Self-Test	No ADC Self-test		ADC Self-test

Note: **Check the IOMUX spreadsheet in RM for the external ADC pins availability.*

Table 17. S12ZVM, S32M24x and S32M27x timer differences

Timer Modules	S12ZVM	S32M24x	S32M27x
	PMF/TIM	FTM	eMIOS
Instances and Channels	Up to 6 independent PWM signals or three complementary PWM pairs (PMF). Up to 4 channels (TIM)	4 FTM instances with 8 channels each.	2 eMIOS instances eMIOS0: 24 channels (X/G/H/Y) eMIOS1: 24 channels (types: X/H/Y)
Prescales and Counter Buses	Prescaler divide by 1, 2, 4, 8, 16, 32, 64 or 128 (TIM) Prescaler divide by 2, 4, 8 for prescaler A and B(PMF)	Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128	Global prescaler from 1 to 256. Local prescaler for channels, from 1 to 16 Counter buses B, C, D, and E can be driven by Unified Channels 0,8,16, and 24, respectively. Counter bus A can be driven by Unified Channel 23. Counter bus F can be driven by a specified Unified Channel
Operation Modes	• PWM (PMF) • Input capture • Output Compare	• Simple Input Capture, • Output compare, • Edge-Aligned PWM mode	• General-Purpose Input/Output (GPIO) • Single-Action Input Capture (SAIC) • Single-Action Output Compare (SAOC) • Input Pulse-Width Measurement (IPWM)

Table 17. S12ZVM, S32M24x and S32M27x timer differences*...continued*

Timer Modules	S12ZVM	S32M24x	S32M27x
			• Input Period Measurement (IPM) • Double-Action Output Compare (DAOC) • Pulse/Edge Counting (PEC) • Modulus Counter (MC) • Modulus Counter Buffered (MCB) • Output Pulse-Width and Frequency Modulation Buffered (OPWFMB) • Center Aligned Output Pulse Width Modulation with Dead Time Insertion Buffered (OPWMCB) • Output Pulse-Width Modulation Buffered (OPWMB) • Output Pulse-Width Modulation with Trigger (OPWMT)
Fault Control	Yes, for the PMF	Up to 4 fault inputs for global fault control	No fault inputs for global fault control

Table 18. S12ZVM, S32M24x and S32M27x LCU differences

LCU	S12ZVM	S32M24x	S32M27x
Instances	None		2x3 logic cells with programmable logic function for generating output results LCU logic cells: 3 Added 3 logic cell to allow 12 phase motor control applications (requires 24 PWM outputs)
I/O	None		2x12 inputs to logic cells and 2x12 outputs from logic cells LCU signal inputs: 2x12 LCU signal outputs: 2x12
Fault Control	None		Fault inputs for global Fault control

Table 19. S12ZVM, S32M24x and S32M27x PTU, PDB and BCTU differences

Programmable delay block	S12ZVM	S32M24x	S32M27x
	PTU	**PDB**	**BCTU**
Trigger Inputs	2 trigger input sources 1 Software trigger source	2 Trigger input sources 1 Software trigger source	Number of channels: 47 (eMIOS and TRGMUX inputs) 1 Software trigger source

Table 19. S12ZVM, S32M24x and S32M27x PTU, PDB and BCTU differences*...continued*

Programmable delay block	S12ZVM	S32M24x	S32M27x
ADC hardware trigger	2 Trigger outputs for ADC and PMF	8 Configurable PDB channels for ADC hardware trigger	Trigger outputs to 2 ADCs, support of 32 ADC channels.
Complementary Logic	No	none	1 Priority selection logic per ADC
Memory Self Resources	No	none	1 List of ADC channels 2 FIFOs

8.1 S12ZVM, S32M24x and S32M27x considerations

8.2 PWM capabilities

S32M24x and S32M27x supports more PWM channel outputs using the FTM/eMIOS compared to the S12ZVM, which is capable to generate up to 6 independent PWM signals or 3 complementary pairs. S32M2xx family supports more PWM channels, in case of the S32M24x, deadtime is inserted using the FTM, while in the S32M27x deadtimes are inserted using LCU.

8.3 ADC

S32M27x supports ADC Self-test function while S32M24x and S12ZVM does not support it. Also, BCTU for S32M27x supports FIFO for the ADC conversion sequences.

8.4 LCU

LCU is a programmable logic cell unit, that can generate PWM, complementary pairs, decode signals, etc. (for more information refer to S32M27x RM). It is only available on S32M27x family.

9 AE modules

S32M2xx incorporates an Analog Extension module that integrates different analog peripherals such as GDU, DPGA, temperature sensor and many other.

To configure the Analog Extension in S32M2xx a SPI interface is required (there is a SPI routed internally in all S32M2 family devices), it can go up to 10MHz in the SPI clock, also SPI messages act as a wake-up source for AE when the AE is in sleep mode and MCU is in low power mode.

AE can act as a wake-up source for MCU, with the NMI in MCU, AE send an interrupt to MCU when an interrupt is detected on AE. Configuring the NMI as wake-up source allows us to go from low power modes to RUN mode.

S32M2xx incorporates a WDOG in AE, so the use of a WDOG apart from the MCU is possible with the AE built-in WDOG.

9.1 GDU and DPGA

Both S32M2xx family and S12ZVM incorporates a Gate Driver Unit, in S32M24x and S32M27x the modules is the same and it has different features against the S12ZVM, the GDU in both cases allow us to drive up to 6 MOSFETs for driving a three phase motor in motor control applications, also S32M2xx family incorporates a DPGA (Differential Programmable Gain Amplifier)

Table 20. S12ZVM and S32M2xx GDU comparison

Features	S12ZVM	S32M2xx
Charge Pump	Yes	Yes, with integrated diodes
Phase voltage measurement	Yes, with ADC	Yes, with ADC
Slew rate control	Yes	
Undervoltage detection on FET pre-driver	Yes	Yes
Fault handling	Yes: Overcurrent Overvoltage Undervoltage Power bridge fault	Yes, for: Overvoltage on HD pin External FET desaturation Supply over voltage Low voltage on VLS pin High current from the DC motor Overcurrent with DPGA
Boost converter	Yes (external inductor and diode)	
Blanking time	Yes	Yes
Delay measurement	No	Yes, can measure the delay between PWM and the feedback signal
Interrupts	GDU Overcurrent GDU Desaturation (High side and low side) GDU High HD voltage GDU Low VLS	DPGA Overcurrent GDU Desaturation (High side and low side) GDU HD High voltage Low VLS (with PMC)
Low power operation	Yes, in Run mode, Wait mode (all features available) Stop mode: GDU is disabled	Yes, in RUN mode and SLEEP_SiP all features are available, in DEEPSLEEP_SiP GDU is disabled.
Operation frequency	Bus clock	42MHz

- Both families offers differential amplifiers to measure current, it can be sensed with an ADC on S32M2 family or S12ZVM family.
- DPGA is a differential amplifier with programmable gain, it allows to have single-shunt motor control applications with a reduced BOM compared to S12ZVM.
- GDU can configure thresholds for the interrupt detection of high voltage.

9.2 High Voltage Input (HVI)

Both S12ZVM and S32M2xx family incorporates high voltage inputs.

In case of S12ZVM there is one high voltage input pin with wake-up capability, also the pin is mapped to an internal ADC channel.

In S32M2xx there are 2 high voltage inputs, and can act as wake-up options. Reading the voltage on the pin is possible with the on-chip ADC.

Also, S32M2 family incorporates a voltage monitor for the high voltage input. The voltage monitor is dedicated to high voltage Input 0 (HVI0) for battery voltage monitoring.

Table 21. S12ZVM and S32M2xx HVI differences

	S12ZVM	S32M2xx
Number of high voltage inputs	1	2
ADC measurements	Yes	Yes
Interrupts	Yes	Yes
Voltage monitor	No	Yes (for battery monitoring)
HVI sources	External pin	High voltage input (external pin) Buffered input Unbuffered input Refer to RM for configuration information and all the sources.

9.3 External sensor supply

Both S12ZVM and S32M2xx support external sensor supply, while in S12ZVM the maximum current is 20mA, in the S32M2xx family it goes up to 30mA.

The pin in S32M2xx is the VDDE (it needs to be configurated in the AE).

9.4 AE PMC

S32M2 incorporates a PMC (Power Management Controller) in the Analog Extension.

Internal AE PMC provides supply to internal MCU (S32K1 or S32K3 for S32M24 and S32M27 respectively), incorporates different regulators for GDU, CAN PHY/LIN PHY, DPGA, monitors, etc.

The PMC uses two bandgap references, the first one for all the regulators and the second one for all monitors (low-voltage detection, high-voltage detection). This is a safety feature in the AE PMC. This AE PMC is the same for both S32M24x and S32M27x.

In case of S12ZVM, it incorporates a regulator that allows voltage inputs from 3.5V to 40V.

S32M2 supports voltage inputs from -0.3V to 42V.

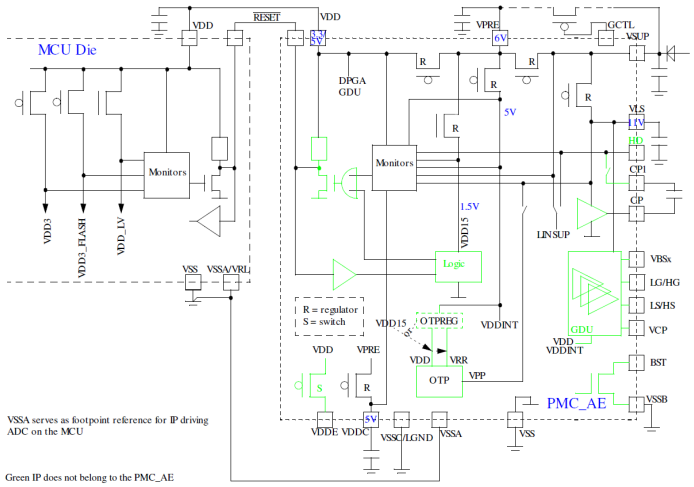

Figure 10. S32M2xx PMC_AE block diagram

10 Communication Modules

10.1 CAN

The S32M7x incorporates an upgraded FlexCAN peripheral, with multiple new capabilities added for the reception of CAN-FD frames of up to 64-bytes payload length; such as reception in First-in-first-out order (RX FIFO) and DMA transfers, both handled entirely by hardware.

The next table summarizes the differences between FlexCAN in S32M24x and S32M27x.

Also, both families offer an integrated CAN PHY (available on S32M2 ‘C’ products), in S32M2 family the integrated CAN PHY offers CAN Classic and CAN FD support.

S12ZVM integrated CAN PHY offers CAN Classic support.

Table 22. Differences between S12ZVM and S32M2 family CAN controller

Feature	S12ZVM	S32M24x	S32M27x
CAN-FD	No	Only available in few instances	Available in all instances
Reception FIFO (RX FIFO)	Yes, five receive buffers	For CAN 2.0B frames	For CAN classic and CAN-FD
Timestamping timer	16-bit wide	16-bit wide	32-bit with added tick sources
DMA transfers	No	Only for classic CAN	Available for both CAN and CAN-FD
Message buffers	3 transmit buffers with internal priorization	All instances have up to 32 message buffers (MB’s)	FlexCAN0, FlexCAN1 and FlexCAN2 instances have 96, 64 and 64 MB’s of 8-byte payload size respectively. All other instances have up to 32MB
Pretended Networking (PNET)	Not supported	Available in FlexCAN0	Not supported
ECC memory	Not available	Not available	Each byte of FlexCAN memory is associated with 5 parity bits

10.2 FlexIO

FlexIO is a configurable peripheral consisting in different shift registers, timers and options to provide different functionalities, for example, UART, I2C, SPI, generate PWM, etc.

This feature is only available in S32M2 family (not available in S12ZVM).

Table 23. FlexIO parameters

	S32M24x	S32M27x
Number of timers	4	8
Number of pins	8	16
Number of shift registers	4	8

10.3 UART

The LPUART includes registers to control baud rate, select options, report status, and store transmit/receive data. Access to an address outside the valid memory map generates a bus error. The LPUART supports full-duplex, asynchronous, NRZ serial communication and comprises a baud rate generator, transmitter, and receiver block. The transmitter and receiver operate independently, although they use the same baud rate generator.

S12ZVM incorporates Serial Communication Interface (SCI) for serial communication and LIN support. Both S12ZVM and S32M2 integrates LINPHY on selected devices (in case of S32M2, the 'L' version of the SiP). Main differences between UART support are available in the next table:

Table 24. S12ZVM and S32M2 Serial communication differences

	S12ZVM	S32M24x	S32M27x
LIN support	Yes		
DMA support	No	Yes	Yes
Instances	2	Up to 2	Up to 4
TXFIFO	No	4 word	4 word
RXFIFO	No	4 word	4 word

10.4 Serial Peripheral Interface (SPI)

The LPSPI is a Low Power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus, either as a master and/or as a slave.

S12ZVM incorporates a SPI interface, the differences are listed in the next table:

Table 25. SPI differences between S12ZVM and S32M2

	S12ZVM	S32M24x	S32M27x
Max word size	16 bits	32 bits	32 bits
Slave operation	Yes	Yes	Yes
Master operation	Yes	Yes	Yes
DMA support	No	Yes	Yes
Rx FIFO	No	4 words	4 words
Instances	Up to 1 instance	Up to 4 instances	Up to 3 instances
Maximum bitrate	12.5 Mbps	15Mbps	20Mbps (LPSPI0)

10.4.1 Considerations on S32M2 LPSPI.

In S32M2 family, one LPSPI instance is routed internally for communication with the Analog Extension, it can run up to 10Mbps for AE communication, so one instance is not available for free use, refer to S32M24x RM or S32M27x RM for more information about AE communication.

10.5 Inter-Integrated Circuit (I2C) interface

The LPI2C is a Low Power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master and/or as a slave.

- The LPI2C implements logic support for standard-mode, fast-mode, fast-mode plus and ultra-fast modes of operation.
- The LPI2C is designed to use little CPU overhead, with DMA offloading of FIFO register accesses.

The LPI2C module also complies with the System Management Bus (SMBus) Specification, version 3. The SMBus is a single ended simple two-wire bus, which is typically used for low bandwidth communications.

S12ZVM does not support I2C.

Table 26. S32M2 I2C features

Feature	S32M27x	S32M24x
I2C max communication speed (Slave mode)	up to 3.4 MHz	up to 400kHz
I2C max communication speed (master mode)	up to 400kHz	up to 400kHz
SMBus support	Yes	Yes
RXFIFO	4 word	4 word
TXFIFO	4 word	4 word
DMA support	Yes	Yes
# of instantiation	1	1

11 Pin management and characteristics

The pin configuration between S12ZVM, S32M24x and S32M27x is different, but in the case of S32M2xx, the family have pin compatibility reducing the changes that need to be done in the PCB design.

The S32M24x has two modules for the pin configuration PORT and GPIO. The S32M27x has one module to handle the pin configuration called Signal Integration Union Lite (SIUL2).

S12ZVM offers different ports with different capabilities, whether ADC, GPIO, GPIO with pull support, etc. Also analog functions such as HVI, GDU or communication with CAN/LIN phy are supported in the SiP, depending on the device.

S32M24x and S32M27x support different configuration on the pins. A pin can be configured as ADC, comparator input, SPI, CAN, etc.

S32M2 offers other pins for GDU, HVI, CAN/LIN PHYs, etc. Refer to S32M2 IOMUX spreadsheet (available in S32M24x and S32M27x RM) for all the available pins.

11.1 Port and pin assignment

Table 27. . S12ZVM and S32M2 pin and port assignment

S12ZVM	S32M24x (PORT register)	S32M27x (SIUL2_MSCR register)
PAD[15:0] (ADC inputs or GPIO)	PORTA[0-31]	MSCR0 - MSCR31
PE[1:0] (General I/O signals, GPIO, support pull-down)	PORTB[0-31]	MSCR32 - MSCR63
PP[2:0] (GPIO with wake-up capability, support pull-up or pull-down)	PORTC[0-31]	MSCR64 - MSCR95
PS[5:0] (GPIO with wake-up capability, support pull-up or pull-down)	PORTD[0-31]	MSCR96 - MSCR127

Table 27. . S12ZVM and S32M2 pin and port assignment*...continued*

S12ZVM	S32M24x (PORT register)	S32M27x (SIUL2_MSCR register)
PT[3:0] (GPIO with pull-up or pull-down support)	PORTE[0-31]* *NOTE: Up to PTE16 is supported	MSCR128 - MSCR159* Note: Up to MSCR144 is supported
AN0[7:0], AN1[7:0] (ADC input signals)		

11.2 S32M24x vs S32M27x pin features

PORTn_PCR is the register that contains the specific pad settings (pull up, interrupt status flag, pin mux control, etc).

SIUL2_MSCR is the register that contains the description of control signals (pull up, output enable, input enable, etc.).

Table 28. S32M24x and S32M27x pin features

	S32M24x	S32M27x
Pull Up / Pull Down	Yes	
Pad keeping	No	Yes
Slew rate control	No	Yes
Drive strength	Yes	
Input filter	Yes	Supported for RESET pad only (PTA5)
Pin mux control	Yes (PCR_MUX)	Yes (MSCR_SSS)
GPIO	Yes Alternative 1	Yes Alternative 0
GPIO input	Yes (PTx_PDIR)	Yes (GPDIx_PDI)
GPIO output	Yes (PTx_PDOR)	Yes (GPDOx_PDO)

11.3 External interrupt

The S32M24x configure the external interrupts by port. Meaning that any pin can be used as an external interrupt. To configure an external interrupt the S32M24x has the PORTx_PCRn[IRQC] register.

The S32M27x configure the external interrupt by a specific pin. To know which pin can be used as an external interrupt refer to “S32M27x_IOMUX” spreadsheet available in S32M27x RM. To configure an external interrupt the S32M27x has the following registers.

- DIRER
- DIRSR
- IREEER / IFEER
- DISR

12 Hardware & pinout

Pinout is different between S32M2 family and S12ZVM. For the S32M2 design guidelines, refer to S32M2 HW design guidelines document. S12ZVM is offered in up to 80-pin LQFP-EP package while the S32M2 family

offers 64-pin LQPFP-EP package. For pinout reference, see “S32M24x_IOMUX” and “S32M27x_IOMUX” spreadsheets for pinout references.

Also, different hardware is available for S32M2, evaluation boards are available for both families and both variants (CAN, LIN) (S32M244 and S32M276).

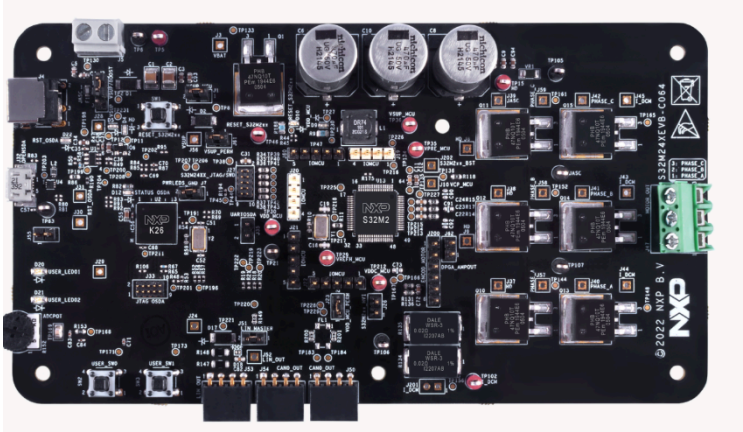

Figure 11. S32M24xEVB-C064

A reference design demonstration for S32M276 CAN version shows us the S32M2 BOM and size reduction compared to S12ZVM , it allows the customer to view the reduced BOM capabilities of the S32M2 family compared to S12ZVM.

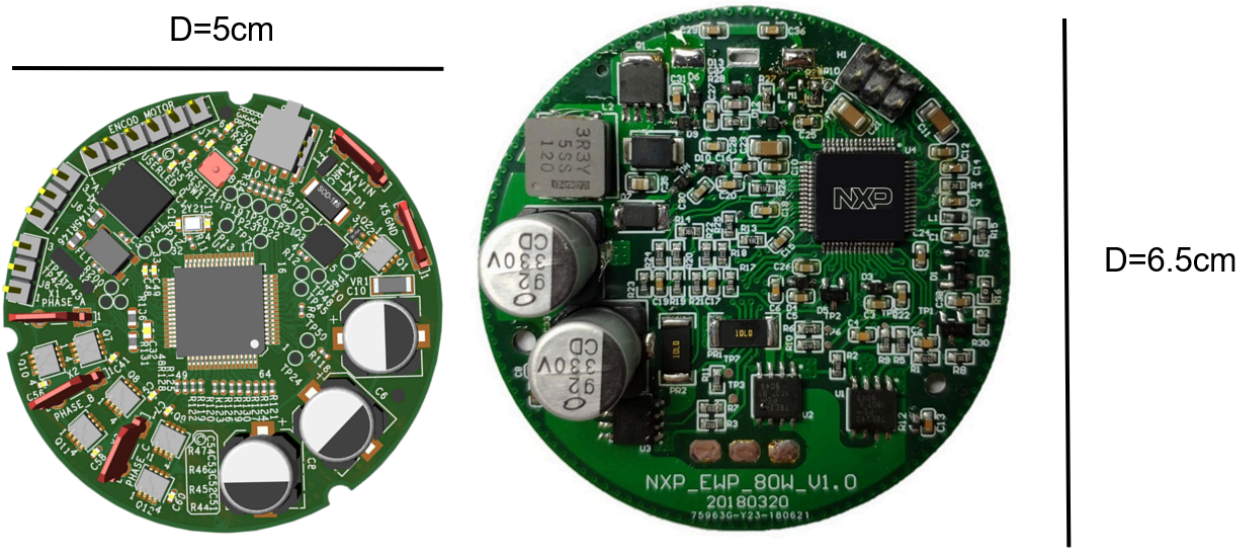

Figure 12. S32M24xEVB-C064

In Figure 12, both reference designs are for 3-phase motor control applications.

We can see S32M276 offers a lower size, and a BOM reduction to get the motor control functionality.

13 Software and tools for S32M2

S32 Design Studio supports S32M24x and S32M27x.

There are different software and tools for S32M2 family:

- FreeMaster
- RTD
- MCAL
- AUTOSAR support (through RTD and MCAL)
- HSE Firmware (For S32M27x)
- Safety framework
- LIN Stack

13.1 Debugging capabilities

The S32M2 devices has implemented the ARM Core sight debug IP, however S32M27x has enhanced debug capabilities.

S12ZVM incorporates a less-powerful debugging capabilities than S32M2 family. It incorporates a proprietary debug support, incorporating trace capabilities. Refer to S12ZVM RM for debug capabilities.

S32M2 family incorporates powerful debug capabilities, going even further with the S32M27x, the following table enlists the S32M2 debug support:

Table 29. S32M2 debug capabilities

S32M24x	S32M27x
MTB	CTI
MTB_DWT	DWT
N.A.	BPU
N.A.	ITM
N.A.	SWO
N.A.	MDM_AP
N.A.	SDA_AP

14 Additional supporting documentation and material

For more details, please refer to the following documents:

- S32M24x and S32M27x series reference manual
- HSE related information:
  - HSE Firmware Reference Manual
  - HSE_Service_Reference Manual
- S32M2 HW design guidelines
- S32M2 software packages containing RTDs

15 Revision history

Table 30. Revision history

Document ID	Release date	Description
AN14459 v.1.0	14 November 2014	Initial release

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