AN14447

Low power implementation on MCXA156 MCU series

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Document information

Information	Content
Keywords	AN14447, MCXA156 MCU series, Low power, Power consumption, Wake-up time
Abstract	This application note introduces the power domains, power modes, highlights configurations, wake up, and low power and wake-up optimization for the MCXA156 series of MCUs. It also provides a demo to change the low power configurations and reproduce the typical power consumption and wake-up time data listed in the MCXA156 data sheet.

1 Introduction

The MCXA156 series of MCUs expand the MCX Arm® Cortex®-M33 product offerings with multiple high-speed connectivity. These MCUs can operate up to 96 MHz and include several serial peripherals, timers, analog devices and are characterized by low power consumption.

The power-efficient operating modes are as follows:

- 64 µA/MHz in Active mode
- 1.81 mA in Sleep mode
- 32.26 µA in Deep Sleep mode
- 8.2 µA in Power Down mode
- 412 nA in Deep Power Down mode

This application note mainly describes the following contents of MCXA156 series of MCUs:

- Power domains and power supplies
- Power modes and low power entry
- Power related configurations
- Wake-up sources and wake-up time
- Low power and wake up optimization
- Low power demo

2 Power domains and power supplies

As shown in Figure 1, the device contains the SYSTEM domain, CORE domain, SRAM domain, ANALOG domain, and USB domain. For specific modules contained in each domain, refer to the Power domain assignments for modules table in the *MCXA156 Reference Manual*. See Section 8 "References".

- The SYSTEM domain is mainly used for power management, which contains SPC, HVD/LVD/POR, FRO16K, WUU, and other modules.
- The CORE domain is used mainly for digital logic that contains CM33, NVIC, DMA, FRO192M, LPUART, and other modules.

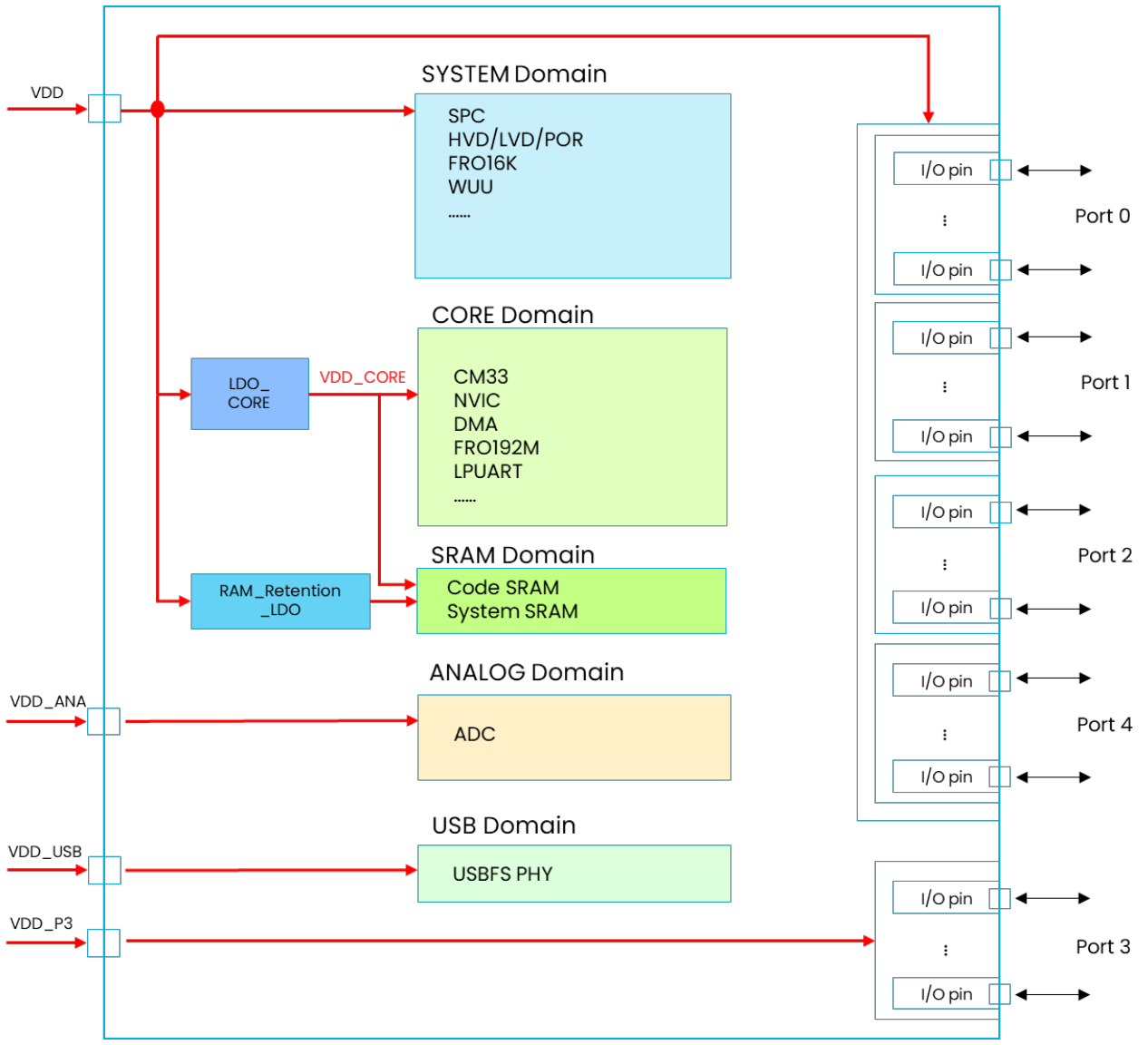

Figure 1. Power domains and power supplies

Table 1 shows the power supply and corresponding voltage range of each power domain. The power supply of the CORE domain is the output voltage VDD_CORE of LDO_CORE, which is 1.0 V and 1.1 V in active mode. It can be a lower voltage in Power Down mode. When VDD_CORE is 1.1 V, the core can reach up to 96 MHz. When VDD_CORE is 1.0 V, the core can reach up to 48 MHz. The power supply of SRAM domain is the output voltage of LDO_CORE or RAM_Retention_LDO, and RAM_Retention_LDO supports SRAM retention switches

in Power Down and Deep Power Down mode. Table 1 also shows the power supply and corresponding voltage range of the remaining power domains.

Table 1. Power supplies and voltage range

Power domain	Power supply	Voltage range
CORE	LDO_CORE	Mid voltage (1.0 V), Normal voltage (1.1 V) (Active, Sleep, and Deep Sleep mode)
		Retention voltage (Power Down mode)
		OFF (Deep Power Down mode)
SRAM	LDO_CORE	Mid voltage (1.0 V), Normal voltage (1.1 V) (Active and Sleep mode)
	RAM_Retention_LDO	Retention voltage (Deep Sleep, Power Down, and Deep Power Down mode)
SYSTEM	VDD	1.71 – 3.6 V
ANALOG	VDD_ANA	1.61 – 3.7 V
USB	VDD_USB	3.0 – 3.6 V
VDD_P3	VDD_P3	1.71 – 3.6 V or 1.14 – 1.32V

3 Power modes and low power entry

This section describes power modes and low power entry controllers.

3.1 Power modes

The device supports Active, Sleep, Deep Sleep, Power Down, and Deep Power Down. Table 2 describes the status of Clock, CORE domain, SYSTEM domain, FLASH, SRAM, PORT and IO in different power modes. It also helps users compare the status of these modules in different power modes. Users can easily find the status of these modules in a certain power mode.

Table 2. Modules status and power modes

Mode Name	CORE domain	CM33	SYSTEM domain	Flash	SRAM	PORT[4]	IO
Active	ON	ON	ON	ON	ON	ON	ON
Sleep	ON	Static[1]	ON	ON	ON	ON	ON
Deep Sleep	Static/LP[2]	Static	ON	Static	Static	Static	ON
Power Down	Static	Static	ON	OFF	Static/OFF	Static	Static
Deep Power Down	OFF[3]	OFF	ON	OFF	Static/OFF	OFF	Static

Note:

1. *Static means the module in state retention status. (no clock but the data can be kept).*
2. *LP means can be active with an asynchronous functional clock.*
3. *OFF means power down.*
4. *PORT provides support for pad control functions.*

The following sections introduce the features of different power modes.

3.1.1 Active

Active mode is the default mode after RESET operation. In this mode:

- Clocks to CPU, memories, and peripherals are enabled.
- CPU execution is possible.
- Adjust VDD_CORE to the minimum possible value based on the required frequency to achieve optimal power consumption.

3.1.2 Sleep

Below are the salient characteristics of Sleep mode:

- CPU clock is OFF.
- System and Bus clock remain ON
- Most modules can remain operational
- Use **ACTIVE_CFG** register to control LDO_CORE voltage level and drive strength

3.1.3 Deep Sleep

Below are the salient characteristics of Deep Sleep mode:

- CPU clock, System clock, and Bus clock are OFF.
- SRAM is in static status (SRAM cannot be accessed, but the data is retained).
- System oscillator clock (SOSC), Slow internal reference clock (SIRC), and Fast internal reference clock (FIRC) can be enabled by configuring the corresponding STEN bit.
- Some modules can remain operational with low power asynchronous clock sources.

3.1.4 Power Down

It is the lowest power mode that can retain all registers. Below are the salient characteristics of Power Down mode:

- The CPU clock, System clock, and Bus clock are OFF.
- Flash memory is powered off.
- Place CORE domain of the chip into static state.
- Supports four SRAM retention switches and must retain at least one SRAM array (For details, refer to the *On-chip regulators* table in the *System Power Control (SPC)* chapter in the *MCXA156 Reference Manual*.)
- Configure the SPC LP_CFG[CORELDO_VDD_LVL] bits to 0000b (retention voltage).

3.1.5 Deep Power Down mode

The device wakes from Deep Power Down mode through the Reset routine. Below are the salient characteristics of Deep Power Down mode:

- The CPU clock, System clock, and Bus clock are OFF.
- The flash memory is powered off.
- The CORE domain is powered off.
- The SYSTEM domain remains ON.

This mode supports four SRAM retention switches and supports all SRAM arrays powered off. (For details, refer to the *On-chip regulators* table in the *System Power Control (SPC)* chapter in the *MCXA156 Reference Manual*.)

3.2 Low power entry

The bit fields CKCTRL[CKMODE] and PMCTRLMAIN[LPMODE] control the power mode entry as shown in Table 5. The CKCTRL[CKMODE] field configures the amount of clock gating when the core enters a low power mode because of WFI or WFE.

Table 3 shows the functions corresponding to different CKMODE values.

- Configuring `CKMODE` greater than `0` requires the `SLEEPDEEP` field in the Arm core to become `1`.
- Configuring `PMCTRLMAIN[LPMODE]` greater than `0` requires writing `1111b` to `CKMODE`.

Table 3. Function of CKMODE field

CKCTRL[CKMODE]	Function
0000b	No clock gating
0001b	Core clock gated
1111b	Core, platform, and peripheral clocks are gated, and the core enters the low power mode

PMCTRLMAIN[LPMODE] selects the desired low power mode when a core executes a WFI or WFE instruction. If the protection level is not enabled using Power Mode Protection (PMPROT), writes to this field are blocked. Table 4 shows the functions corresponding to different LPMODE values.

Table 4. Function of the LPMODE bit field

PMCTRLMAIN[LPMODE]	Function
0000b	Active/Sleep
0001b	Deep Sleep
0011b	Power Down
1111b	Deep Power Down

Table 5 shows all the configurations of the device to enter the low power mode.

Table 5. Power mode entry

Power mode	CKCTRL[CKMODE]	PMPROT[LPMODE]	PMCTRLMAIN[LPMODE]
Active	0000b	0000b	0000b
Sleep	0000b	0000b	0000b
	0001b		
Deep Sleep	1111b	0001b	0001b
Power Down	1111b	0011b	0011b
Deep Power Down	1111b	1111b	1111b

4 Power configurations

This section describes the regulator and voltage detector configurations, Low Power Request (LPREQ) pin, and async DMA.

4.1 Regulator and voltage detectors configurations

Table 6 shows the power-related hardware configurations. ACTIVE_CFG and ACTIVE_CFG1 registers configure the hardware in Active and Sleep mode, such as LDO_CORE voltage level and drive strength. Autonomous change to use LP_CFG and LP_CFG1 when in low power mode (Deep Sleep, Power Down, and Deep Power Down).

Table 6. Power-related hardware configurations

Register Name	Associated function
ACTIVE_CFG LP_CFG	• Configures – LDO_CORE voltage level – LDO_CORE drive strength • Enables – HVDs, LVDs – Bandgap, BG buffer – VDD voltage detect – Low-power current reference IREF
ACTIVE_CFG1 LP_CFG1	• Enables – CMPs and CMP DACs – USB 3V detect

4.2 Low Power Request (LPREQ) pin

The LPREQ pin asserts after low power entry and negates after low power wake up.

SPC controls the state of the LPREQ pin based on how you configure Low-Power Request Configuration (LPREQ_CFG). You control the LPREQ pin in Active mode. SPC controls the pin when the chip transitions from Active to a Low Power mode, and after wakeup from these Low Power modes.

To use the LPREQ pin:

1. Specify the pin polarity (LPREQ_CFG[LPREQPOL])
2. Enable the pin output (LPREQ_CFG[LPREQOE])
3. Configure the pin mux for the desired pin using the PORT PCR registers.

Figure 2 shows the waveform of the LPREQ pin, where the explanation of the waveform is listed below:

- CTIMER_MATCH: Hardware toggles IO to indicate wake up event.
- LPREQ_PIN: LPREQ_CFG[LPREQPOL]=1b, LPREQ_CFG[LPREQOE]=1b, which means that the pin becomes low after low power entry and high after wake up.

Figure 2. Waveform of LPREQ pin

4.3 Async DMA

Deep Sleep mode and Power Down mode support the use of async DMA to wake up partially and the device automatically re-enters the low power mode after DMA completes its task.

Async DMA can be introduced by the following points:

- The async DMA does not require CPU involvement. However, it still requires the bus clock, which wakes up the MCU from Deep Sleep or Power Down to Sleep mode.
- When async DMA requires to access the register of a peripheral, enable the Bus clock of the peripheral before entering low power mode by using the MRCC_GLB_CCx and MRCC_GLB_ACCx registers. When async DMA needs to access SRAM, the SRAM should not be set to retention state in Sleep mode.
- When async DMA is completed, that is, CHx_CSR[DONE] is set, the MCU automatically enters the original low power mode.
- Set CHx_CSR[ERQ] and CHx_CSR[EARQ].
- Table 7 lists all the hardware trigger sources of async DMA and the corresponding slot number. Only modules in LP status (not Static status under Deep Sleep or Power Down modes) support async DMA. For example, FlexCAN is in Static under Deep Sleep mode. Therefore, it cannot support async DMA.

Table 7. Async DMA configuration

Slot Number	DMA request description	Module name
1	Wake up event	WUU0
3	Receive request	LPI2C2
4	Transmit request	LPI2C2
5	Receive request	LPI2C3
6	Transmit request	LPI2C3
11	Receive request	LPI2C0
12	Transmit request	LPI2C0
13	Receive request	LPI2C1
14	Transmit request	LPI2C1
15	Receive request	LPSPI0
16	Transmit request	LPSPI0
17	Receive request	LPSPI1
18	Transmit request	LPSPI1
21	Receive request	LPUART0
22	Transmit request	LPUART0
23	Receive request	LPUART1

Table 7. Async DMA configuration*...continued*

Slot Number	DMA request description	Module name
24	Transmit request	LPUART1
25	Receive request	LPUART2
26	Transmit request	LPUART2
27	Receive request	LPUART3
28	Transmit request	LPUART3
29	Receive request	LPUART4
30	Transmit request	LPUART4
49	Counter match event	LPTMR0
51	FIFO Request	ADC0
52	FIFO Request	ADC1
53	DMA_request	CMP0
54	DMA_request	CMP1
56	FIFO Request	DAC0
60	Pin event request 0	GPIO0
61	Pin event request 0	GPIO1
62	Pin event request 0	GPIO2
63	Pin event request 0	GPIO3
64	Pin event request 0	GPIO4
71	Shift Register 0 request	FlexIO0
72	Shift Register 1 request	FlexIO0
73	Shift Register 2 request	FlexIO0
74	Shift Register 3 request	FlexIO0

5 Wake up information

Table 8 displays the typical wake-up time and wake-up sources in different low power modes, where the typical wake-up time values are taken from the *MCXA156 datasheet*. (See Section 8 "References".)

Table 8. Wake-up information

Symbol	Description	Wake-up source	Typical wake-up time
tSLEEP	Sleep -> Active	All peripherals	0.23 µs
tDSLEEP	Deep Sleep -> Active	Async peripherals	7.1 µs
tPWDN	Power Down -> Active	WUU, Reset pin	16.6 µs
tDPWDN	Deep Power Down -> Active	WUU, Reset pin	1.44 ms

6 Low power and wake up optimization

This section explains various methods for optimizing power consumption and factors to consider for wake-up optimization.

6.1 Power consumption optimization

Following are the different ways of optimizing power consumption:

- **Regulator**
  - Configure the appropriate voltage level and drive strength.
  - In Power Down mode, LDO_CORE can provide retention voltage to the CORE domain.
- **Peripherals**
  - Disable unused analog peripherals by configuring the ACTIVE_CFG1 and LP_CFG1 registers.
- **Memories**
  - Flash
    - Configure the FLASHCR register to place the flash memory in Low-Power state.
  - SRAM
    - Use Auto clock gating by configuring the RAM_CTRL register of SYSCON.
    - SRAM can be individually retained or powered down by using software in the Power Down and Deep Power Down mode.
- **Clocks**
  - Select and configure the appropriate CPU_CLK/SYSTEM_CLK.
  - Disable unused clock sources.
  - Configure the MRCC_GLB_CC0/ MRCC_GLB_CC1/ MRCC_GLB_ACC0/ MRCC_GLB_ACC1 registers to disable or enable automatic clock gating the clocks to modules.
- **Monitors**
  - Disable unused voltage monitors (HVDs/LVDs).
- **I/O pins**
  - For unused I/O pins, the default configuration(floating input) should be used, in which case the leakage current is minimized. With the default configuration, the input buffer and the internal pull resistor are disabled.
  - While using I/O pins, power consumption can be reduced by increasing the resistance of the external resistor appropriately.

6.2 Wake-up time consideration

Consider the following points relating to the wake-up time:

- SLOW_CLK frequency
  - The wake-up process is implemented through CMC. SLOW_CLK is the clock source of CMC and its frequency is equal to ¼ SYSTEM_CLK.
- Different VDD_CORE level
  - Recovery time required for different voltage levels. For details, refer to the “*Low Power Wake-Up delay*” table in the *Reference Manual*.
- The longer time of clock recovery time and flash recovery time.
- Interrupt latency.

7 Demo operation

This section describes the steps, setup and results for a demo to change the low power configurations and reproduce the typical power consumption and wake-up time data as mentioned in the MCXA156 datasheet.

7.1 Hardware requirement

- FRDM-MCXA156 board
- One Type-C USB cable

Note:

1. *To measure the power consumption, use the MCU-Link Pro or a multimeter.*
2. *To measure the wake-up time, rework the FRDM-MCXA156 to connect SW2-4 to J1-1 and use an oscilloscope or logic analyzer.*

7.2 Software requirements

- MCUXpresso IDE v11.9.0 or later.
- SDK_2.16.0_FRDM-MCXA156.

7.3 Setup

The following sections describe the steps to perform the demo.

7.3.1 Hardware connection

Use a Type-C USB cable to connect J21 of FRDM-MCXA156 board and the USB port of the PC.

7.3.2 Importing the Project

Use the steps below for importing the Project:

1. As shown in Figure 3, open MCUXpresso IDE 11.9.0. In the **Quick Start Panel**, choose **Import from Application Code Hub**.

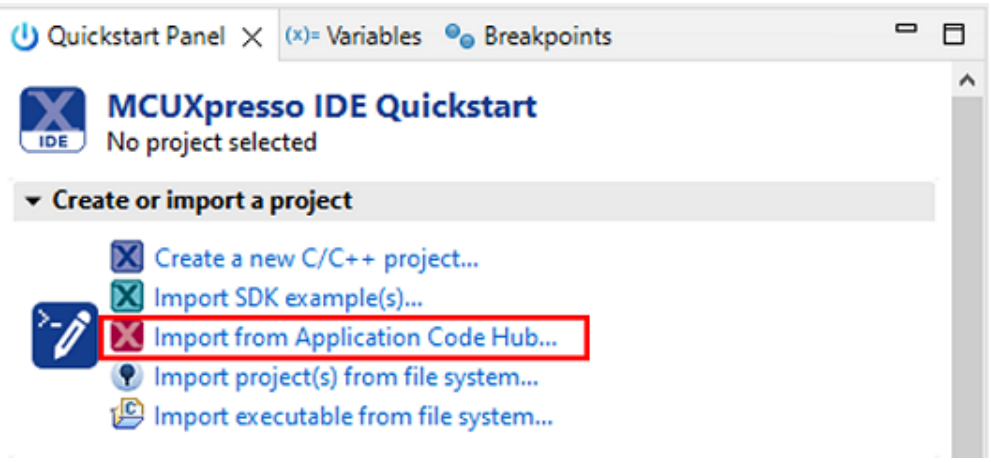

Figure 3. Import from Application Code Hub

2. As shown in Figure 4, enter the **demo name** in the search bar.

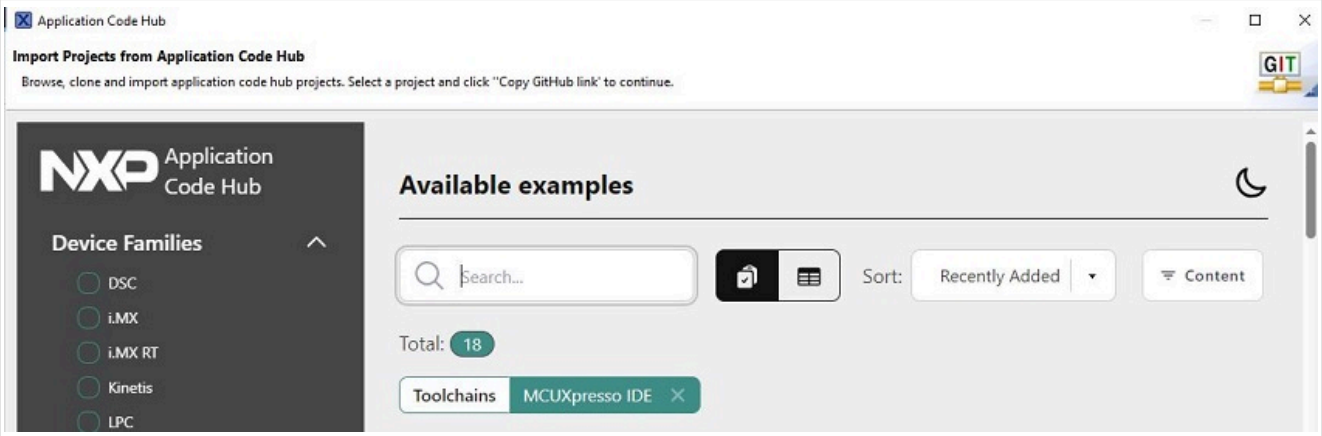

Figure 4. Search demo

3. As shown in Figure 5, click the**Copy GitHub link** icon. MCUXpresso IDE automatically retrieves project attributes. After this step, click **Next**.

Figure 5. Copy GitHub link

4. Select the **main** branch and then click **Next**. Now, select the **MCUXpresso project** and then click the **Finish** button to complete the import.

Note: *Install the SDK_2.16.0_FRDM-MCXA156 on your MCUXpresso IDE after performing these steps.*

7.3.3 Building and flashing the project

Follow the steps mentioned below to build and flash the Project:

1. As shown in Figure 6, click **Build** button from the toolbar, then wait for the build to complete.

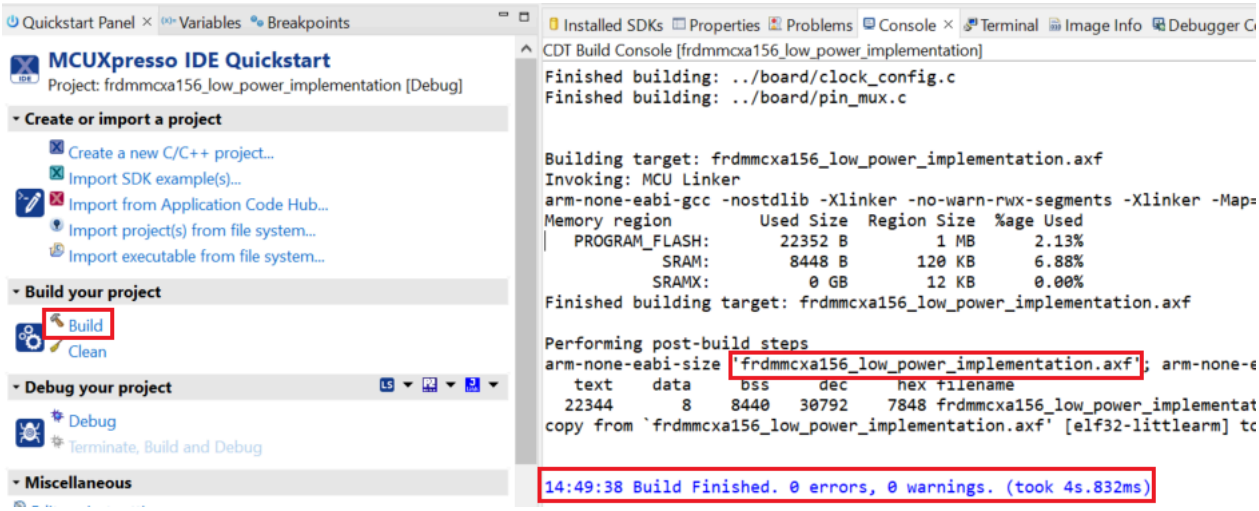

Figure 6. Build the project

2. As shown in Figure 7, select the **GUI Flash Tool** from the toolbar to program the executable to the board.

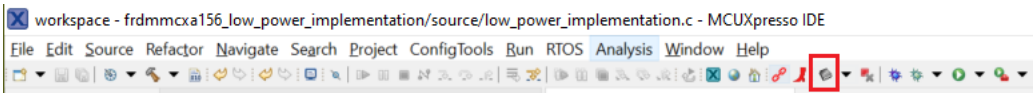

Figure 7. Download the project

7.3.4 Selecting the low power mode and the corresponding configurations

1. Open a serial terminal with a 115200 baud rate.
2. Follow the prompts in Figure 8 and enter one of the keys from A to E to enter a different low power mode.

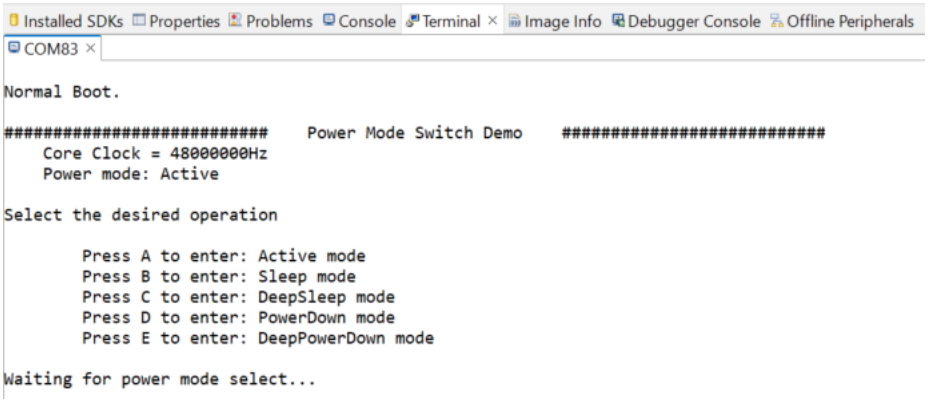

Figure 8. Select low power mode

3. Different low power modes provide different configurations. Therefore, you must select the corresponding configuration according to the prompts. Figure 9 shows the configurations provided in Deep Power Down mode.

```
Select the desired Core Frequency and LDO configuration:

        A: CPU_CLK=96MHz(FRO192M), VDD_CORE=1.1V
        B: CPU_CLK=48MHz(FRO192M), VDD_CORE=1.0V
        C: CPU_CLK=12MHz(FRO12M) , VDD_CORE=1.0V

        Select CPU_CLK=48MHz(FRO192M), VDD_CORE=1.0V

Configure the RAM retention:

        A: No RAM retained
        B: All RAM retained
        C: RAMX0/X1, RAMA0~A3 retained
        D: RAMX0/X1/A0 retained
        E: RAMA0 retained
        F: RAMX0/X1 retained
```

Figure 9. Select low power configurations

4. *Figure 10* shows the entire configuration process, and press **SW2** button on FRDM-MCXA156 to wake up the MCU.
   Note: *Press the **Wakeup** button only when the prompt message appears. Pressing it otherwise would result in a wake-up failure.*

```
Installed SDKs  Properties  Problems  Console  Terminal  Image Info  Debugger Console  Offline Peripherals
COM83
Normal Boot.

##########################    Power Mode Switch Demo    ##########################
    Core Clock = 48000000Hz
    Power mode: Active

Select the desired operation

        Press A to enter: Active mode
        Press B to enter: Sleep mode
        Press C to enter: DeepSleep mode
        Press D to enter: PowerDown mode
        Press E to enter: DeepPowerDown mode

Waiting for power mode select...

        Deep Power Down: The whole core domain is power gated.

Wakeup Button Selected As Wakeup Source.

Select the desired Core Frequency and LDO configuration:

        A: CPU_CLK=96MHz(FRO192M), VDD_CORE=1.1V
        B: CPU_CLK=48MHz(FRO192M), VDD_CORE=1.0V
        C: CPU_CLK=12MHz(FRO12M) , VDD_CORE=1.0V

        Select CPU_CLK=48MHz(FRO192M), VDD_CORE=1.0V

Configure the RAM retention:

        A: No RAM retained
        B: All RAM retained
        C: RAMX0/X1, RAMA0~A3 retained
        D: RAMX0/X1/A0 retained
        E: RAMA0 retained
        F: RAMX0/X1 retained

        Select No RAM retained

Entering DeepPowerDown mode...
Please press SW2 to wakeup.(Please only press the wakeup button when this message appears, otherwise it will result in failure to wake up!)
```

Figure 10. All prompts

7.3.5 Measuring power consumption

The following sections describe the steps for measuring power consumption on the FRDM-MCXA156 board.

7.3.5.1 Use MCU-Link Pro and MCUXpresso IDE to measure power consumption

Follow the steps below to measure power consumption using MCU-Link Pro and MCUXpresso IDE:

1. Connect MCU-Link Pro and FRDM-MCXA156 according to Table 9. Then, connect MCU-Link Pro and FRDM-MCXA156 to the host PC.

Table 9. MCU-Link Pro and FRDM-MCXA156 connection

MCU-Link Pro	FRDM-MCXA156
J9-1	JP2-1
J9-3	JP2-2
J9-2	J3-14

2. Follow the steps in Figure 11 to measure the current using MCUXpresso IDE.

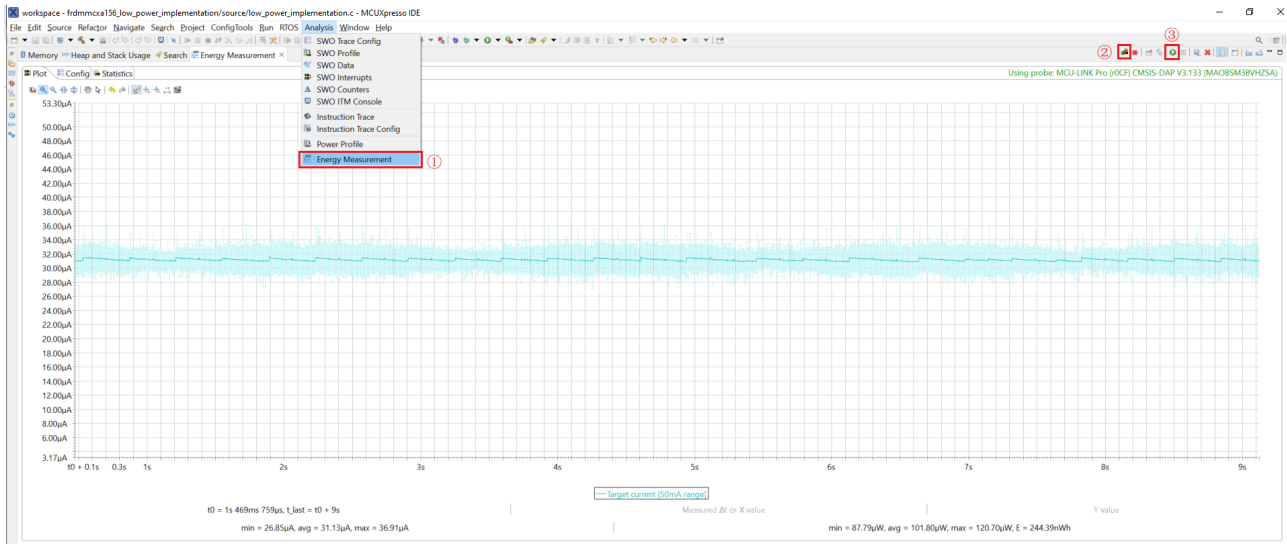

Figure 11. MCUXpresso energy measurement

7.3.5.2 Use multimeter to measure power consumption

You can also use an multimeter to measure the current at JP2 jumper of the FRDM-MCXA156 board.

7.3.6 Measuring wake-up time

As shown in Figure 12, get the wake-up time by measuring the delay between the falling edges of J1-1 (P1_7) and J6-1 (P3_30) using an oscilloscope or logic analyzer.

Figure 12. Measuring wake-up time

7.4 Reference results

The power consumption and wake-up time in Table 10 are provided as a reference.

Note:

- Different samples, temperature, and measuring instruments affect test results.
- Before measuring each data, POR is recommended.
- This demo is not configured exactly the same as the data sheet, so the test data may be slightly different.
- Refer to “Power mode transition operating behaviors” table in MCXA156 data sheet that lists wake-up time, and “Power consumption operating behaviors” section in MCXA156 data sheet that describes different power consumption data.

Table 10. Reference results

Power mode	Description	Tested power consumption	Power consumption in data sheet	Tested wake-up time	Wake-up time in data sheet
Sleep	VDD_CORE=1.1 V CPU_CLK = 96 MHz	3.429 mA	3.34 mA	0.15 µs	N/A
Sleep	VDD_CORE=1.0 V CPU_CLK = 48 MHz	1.804 mA	1.81 mA	0.27 µs	0.23 µs
Sleep	VDD_CORE=1.0 V CPU_CLK = 12 MHz	0.446 mA	0.43 mA	1.086 µs	N/A
Deep Sleep	VDD_CORE=1.1 V CPU_CLK = 96 MHz FRO12M disabled	256.27 µA	257.98 µA	6.552 µs	N/A
Deep Sleep	VDD_CORE=1.0 V CPU_CLK = 48 MHz FRO12M disabled	31.07 µA	32.26 µA	7.284 µs	7.1 µs
Deep Sleep	VDD_CORE=1.0 V CPU_CLK = 48 MHz FRO12M enabled	107.13 µA	104.53 µA	7.281 µs	N/A
Deep Sleep	VDD_CORE=1.0 V CPU_CLK = 12 MHz FRO12M disabled	31.02 µA	N/A	14.274 µs	N/A
Power Down	VDD_CORE= 1.1 V CPU_CLK = 96 MHz All RAM retained	254.37 µA	N/A	7.514 µs	N/A
Power Down	VDD_CORE=retention voltage CPU_CLK = 48 MHz All RAM retained	10.58 µA	9.47 µA	16.848 µs	16.6 µs
Power Down	VDD_CORE = retention voltage CPU_CLK = 48 MHz RAM X0/X1 and RAM A0 retained	9.28 µA	8.20 µA	16.848 µs	N/A
Power Down	VDD_CORE = retention voltage CPU_CLK = 12 MHz All RAM retained	10.53 µA	N/A	23.758 µs	N/A

Table 10. Reference results...*continued*

Power mode	Description	Tested power consumption	Power consumption in data sheet	Tested wake-up time	Wake-up time in data sheet
Deep Power Down	VDD_CORE = 1.0V CPU_CLK = 48 MHz All RAM OFF FRO16K enabled	0.65 µA	0.60 µA	1.44 ms	1.44 ms
Deep Power Down	VDD_CORE = 1.0 V CPU_CLK = 48 MHz ALL RAM retained FRO16K enabled	2.37 µA	2.19 µA	1.44 ms	N/A
Deep Power Down	VDD_CORE = 1.0 V CPU_CLK = 48 MHz RAM X0/X1 and A0-A3 retained FRO16K enabled	1.71 µA	1.57 µA	1.44 ms	N/A
Deep Power Down	VDD_CORE = 1.0 V CPU_CLK = 48 MHz RAM X0/X1 and A0 retained FRO16K enabled	1.02 µA	0.93 µA	1.44 ms	N/A
Deep Power Down	VDD_CORE = 1.0 V CPU_CLK = 48 MHz RAM A0 retained FRO16K enabled	0.87 µA	0.79 µA	1.44 ms	N/A
Deep Power Down	VDD_CORE = 1.0 V CPU_CLK = 48 MHz RAM X0/X1 retained FRO16K enabled	0.90 µA	0.82 µA	1.44 ms	N/A

8 References

Refer to the below documents for more information:

- *MCXA156 Data Sheet* (*MCXAP100M96FS6*)
- *MCXA156 Reference Manual* (*MCXAP100M96FS6RM*)
- *MCXA156* documents are available on the URL: *MCX-A156 documentation*

Note: *Refer only to documents related to 'MCXA156'; they are different for 'MCXA153'.*

Additional references are listed below:

- For MCXA series product information, refer to the URL: MCXA series
- For FRDM-MCXA156 board-related resources and documentation, refer to: FRDM-MCXA156 Board and FRDM-MCXA156 Board Documentation
- For more information about MCU-Link Pro, refer https://www.nxp.com/design/design-center/software/software-library/mcu-link-pro-debug-probe:MCU-LINK-PRO
- For details about the MCUXpresso Integrated Development Environment (IDE), refer to the URL: MCUXpresso IDE

Note: *Some of the documents listed above might not be accessible. To obtain access, contact your local NXP field applications engineer (FAE) or sales representative.*

9 Revision history

Table 11 summarizes the revisions to this document.

Table 11. Document revision history

Document ID	Release date	Description
AN14447 v.1.1	16 October 2024	Minor update; added a note in Section 8 "References"
AN14447 v.1.0	15 October 2024	Initial public release

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