AN14413

Power supply IC i.MX 93 for PCA9451A powering guide

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Document information

Information	Content
Keywords	PCA9451A, i.MX 93x, PMIC
Abstract	This application note provides information regarding peripheral device power connection using the PCA9451A

1 Overview

The PCA9451A is a power supply IC (PMIC: Power Management IC) designed for i.MX 93 application processor. This IC provides the power supply voltage required for the i.MX 93 and controls the power-up/ down sequence and operating modes. It can support power supply voltage for peripheral devices connected to the i.MX 93. The PCA9451A PMIC incorporates power supply design for applications using the i.MX 93.

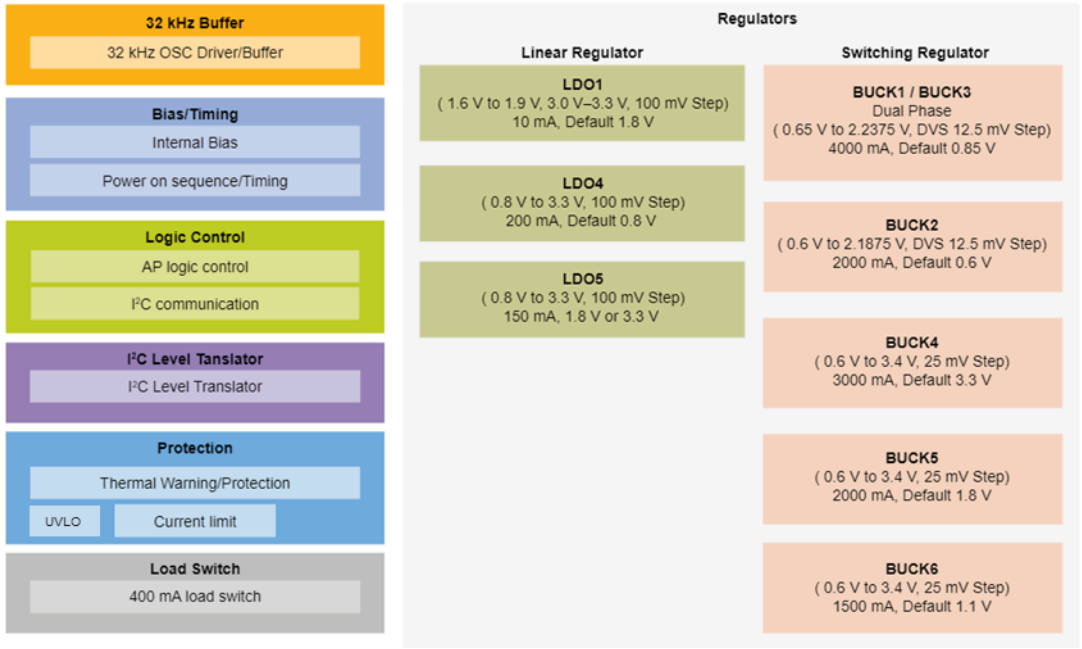


Figure 1. PCA9451A internal block diagram

1.1 Features

- PMIC optimized for i.MX 93
  - Compatible with all i.MX 93 operating modes
  - Supports power supply voltage and required Power Up/Down sequences
- Supports powering LPDDR4/4x memory
- 6-channel BUCK regulator (BUCK1~6)
  - Two channels of 2 A BUCK regulators (BUCK1, 3)
  - BUCK1 and BUCK3 can be connected in dual phase (working in tandem) to provide 4 A output
  - Equipped with DVS function[1]
  - 3 A BUCK regulator 1 channel (BUCK4)
  - Two channels of 2 A BUCK regulators (BUCK2,5)
  - 1.5 A BUCK regulator 1 channel (BUCK6)
- 3-channel Linear regulator (LDO1,4,5)
  - i.MX 93 BBSM mode[2] 10 mA LDO for IO power 1 channel (LDO1)
  - 200 mA LDO 1 channel (LDO4)

1 DVS (Dynamic Voltage Scaling): This control dynamically changes the PCA9451A power supply voltage according to the i.MX 93 operation mode. The voltage slew rate at the time of change can also be set.

2 BBSM (Battery Backed Security Module) mode: In the i.MX 93, only the built-in RTC and some functions (wake-up, etc.) are operating. The power is supplied only to the BBSM power supply from PCA9451A (NVCC_BBSM_1P8).

  - 150 mA LDO 1 channel (LDO5)
- 400 mA Load switch 1 channel (Load SW)
- Equipped with protection and monitoring functions
  - Output voltage monitoring and overcurrent protection
  - Input undervoltage monitoring
  - Temperature monitoring
- 32.768 kHz crystal oscillation driver mounted
- I2C communication interface (Fast Plus Mode max. 1 MHz): PCA9451A control
- I2C level translator on board (1.8 V to 3.3 V or 5 V)
- Temperature range (Tamb): - 40 °C ~ +105 °C
- HVQFN 56-pin: Size 7 mm x 7 mm x 0.4 mm

2 Block diagram

Figure 2 shows a block diagram of the PCA9451A.

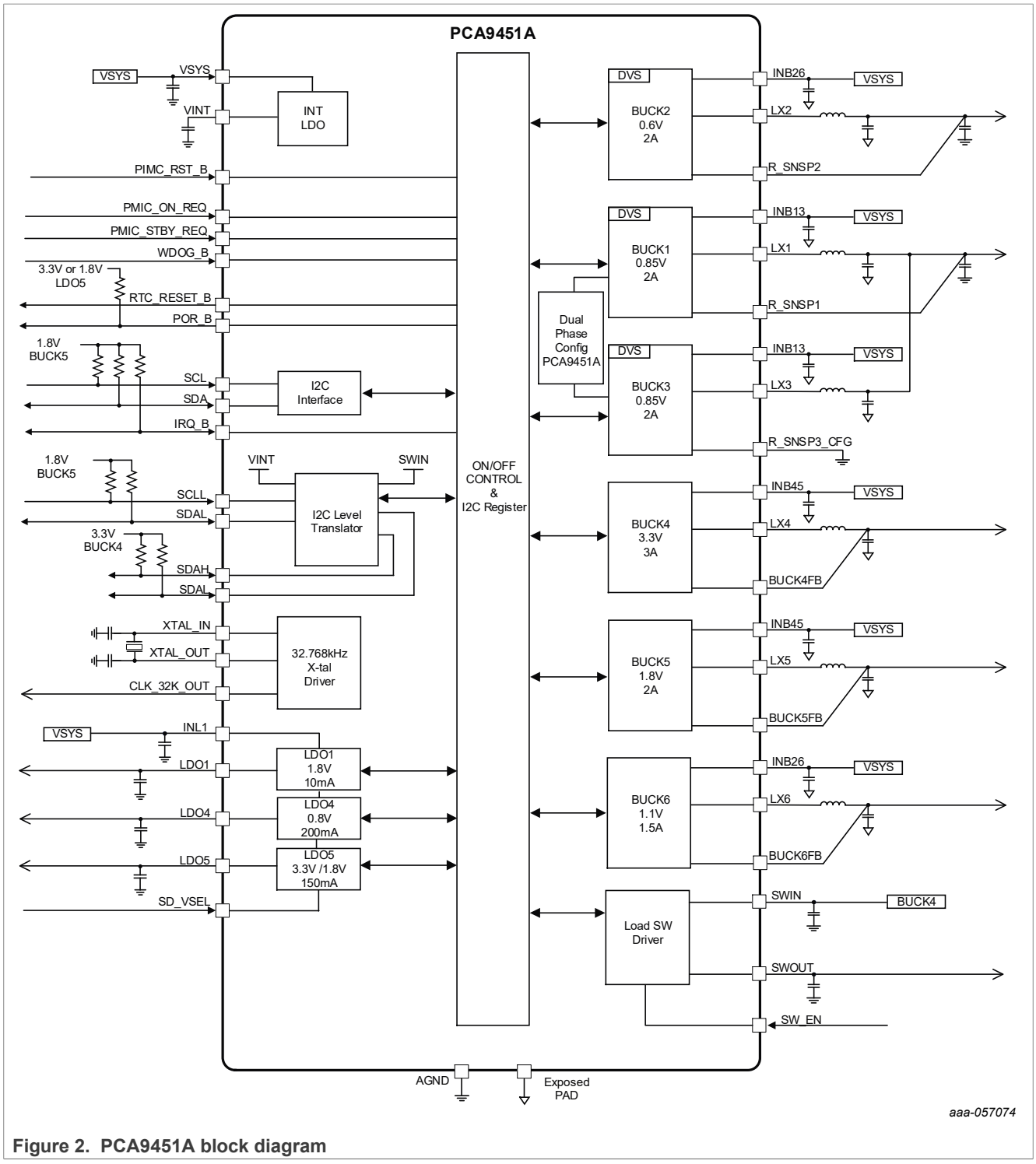


Figure 2. PCA9451A block diagram

- The VSYS pin is the power supply input pin of the PCA9451A. PCA9451A state transitions to the power supply mode shown in Table 2 according to the VSYS input voltage value. The guaranteed operating range is

2.7 V to 5.5 V, and the absolute maximum rating is -0.5 V to 6.0 V. Each BUCK input should be supplied with the same power supply as VSYS.

- The SWIN pin is the input pin for the Load SW and is mainly used as a 3.3 V power supply for the SD CARD. When using the Load SW, SWIN pin should be connected to the BUCK4 output (3.3 V).
- BUCK1 and BUCK3 regulators are used as dual phase mode. BUCK1 and BUCK3 regulator are controlled by BUCK1 registers.

3 Power supply table and connection diagram

3.1 i.MX 93 and peripheral device power supply table

The PCA9451A supports power supply to i.MX 93 and peripheral devices. Table 1 shows the supply voltage to each peripheral device.

Table 1. i.MX 93 and peripherals power supply table

MPU Peripherals	Power 5V							
	PCA9451						External Power Supply	
	0.85V/4A	0.6V / 2A	1.1V / 1.5A	1.8V / 2A	3.3V / 3A	Load SW	3.3V	5V
i.MX93	✓	✓	✓	✓	✓			
LPDDR4			✓	✓				
LPDDR4X		✓	✓					
NAND Flash				✓	✓			
Wi-Fi/Bluetooth				✓	✓			
Camera				✓	✓		✓	✓
Display				✓	✓		✓	✓
Audio Codec					✓			✓
Ethernet				✓	✓			
PDM MIC/MQS					✓			
USB Type-C					✓			✓
MicroSD						✓		
CAN-FD								✓

All of the i.MX 93 internal logic and interface power can be supplied from the PCA9451A. The PCA9451A can power memory (DDR, Flash, SD Card), Wi-Fi/Bluetooth and other devices. However, additional power supplies may be required for Camera, Display, Audio Codec, USB, etc., depending on the required current and voltage.

3.2 i.MX 93 and peripheral device power connection diagram

Figure 3 shows the power supply connection diagram for the i.MX 93 and peripheral devices. The "Selectable voltage 1.8 V or 3.3 V for I/F" in the figure means that either BUCK4 (3.3 V) or BUCK5 (1.8 V) can be selected and connected for connection to the power supply starting with NVCC_.

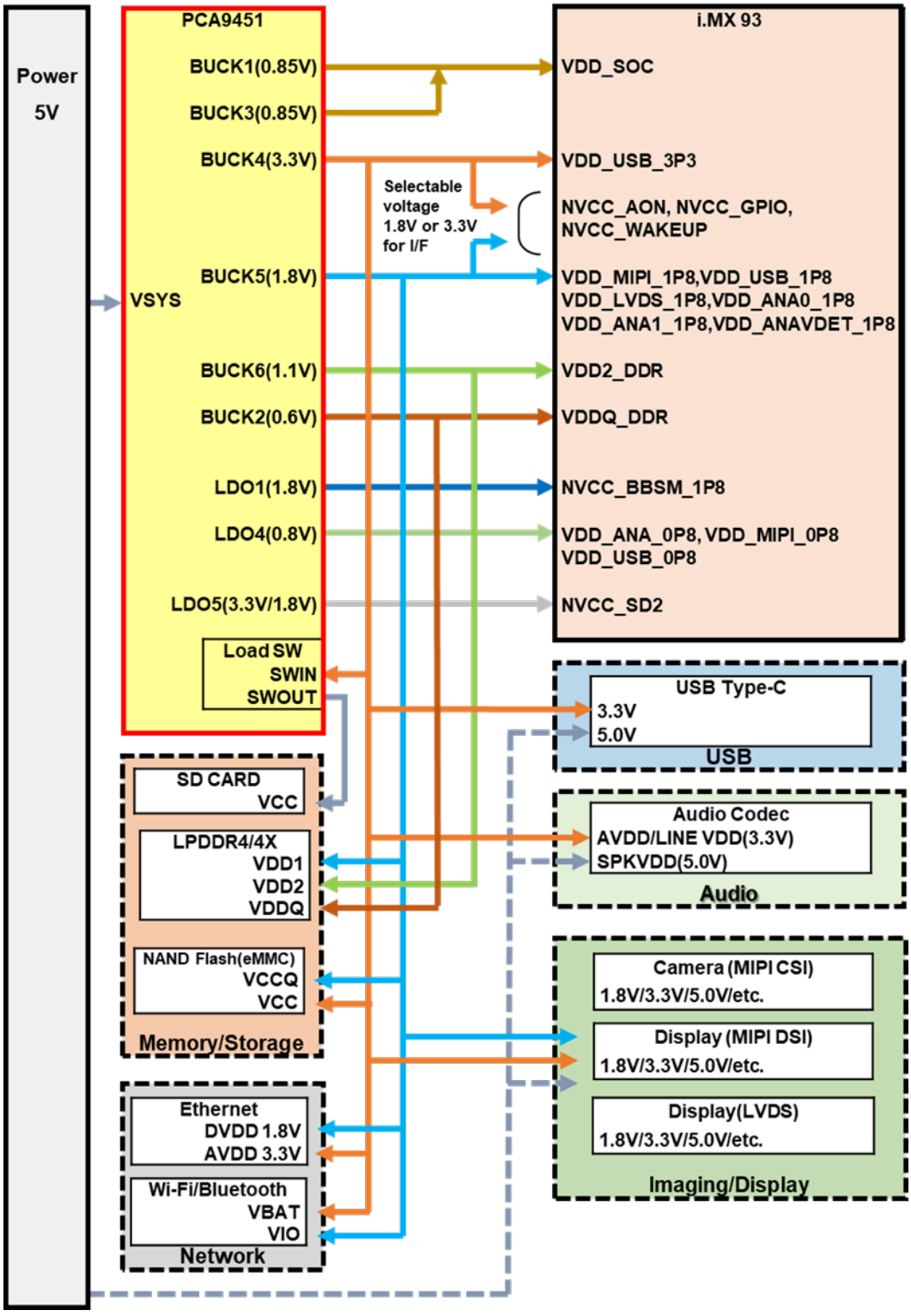
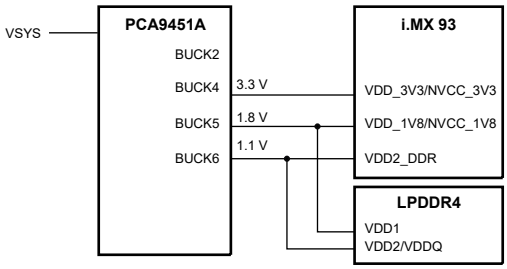
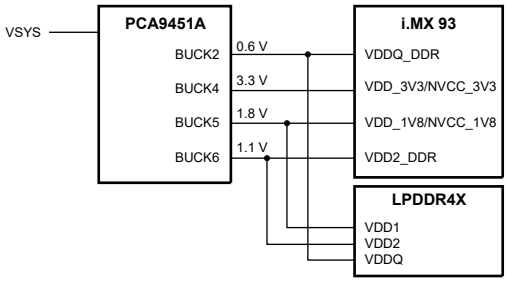


Figure 3. i.MX 93 and peripheral device power connection diagram

4 Connection by DDR memory type

The i.MX 93 supports two types of DDR memory(LPDDR4 and LPDDR4x).The PCA9451A can support the supply voltage required for each memory by setting BUCK2 or BUCK6. BUCK6 supplied 1.1V to VDDQ when LPDDR4 is used, and BUCK2 supplied 0.6V to VDDQ when LPDDR4x is used. Figure 4 shows a connection diagram for each DDR memory type.

Memory	PCA9451A	Schematic
LPDDR4 VDD1 = 1.8 V VDD2/VDDQ = 1.1 V	BUCK5 = 1.8 V BUCK6 = 1.1 V	
LPDDR4X VDD1 = 1.8 V VDD2 = 1.1 V VDDQ = 0.6 V	BUCK2 = 0.6 V BUCK5 = 1.8 V BUCK6 = 1.1 V	

aaa-057073

Figure 4. Connection diagram by DDR memory type

5 Operation mode transition

5.1 Operating mode

The PCA9451A has seven operating modes: OFF mode, READY mode, SNVS mode, PWRUP mode, RUN mode, STANDBY mode, and PWRDN mode, controlled by the input voltage on the VSYS pin and an external control signal.

5.1.1 OFF mode

In the OFF mode, PCA9451A has no VSYS pin voltage.

When the VSYS pin voltage falls below the VSYS_POR (Power On Reset) threshold voltage, the PMIC transitions to OFF mode from any other mode. In this mode, all regulators are turned off and all internal registers of the PMIC are reset.

5.1.2 READY mode

In the READY mode, PCA9451A only operates its internal logic.

When the voltage on the VSYS pin exceeds the VSYS_POR threshold voltage, the device transitions to READY mode from OFF mode. The internal LDO is enabled and ready to transition to SNVS mode.

5.1.3 SNVS mode

In the SNVS mode, PCA9451A supplies power to the SNVS (BBSM) block of the i.MX 93.

When the voltage on the VSYS pin exceeds the VSYS_UVLO (Under Voltage Lock Out) voltage, LDO1 start to output, powering the SNVS block of the i.MX 93 and providing a clock from the 32.768-kHz crystal oscillator driver.

5.1.4 PWRUP mode

In the PWRUP mode, PCA9451A regulator starts Power UP sequence.

For Power Up sequence, see Section 5.3.1.

5.1.5 RUN mode

In the RUN mode, PCA9451A regulators are on.

When the PMIC_ON_REQ pin (which requests the transition to RUN mode from SNVS mode) goes HIGH, all regulators start to output voltage according to the Power UP sequence.

5.1.6 STANDBY mode

In the STANDBY mode, PCA9451A supplies the required voltage when the i.MX 93 is in standby mode. When the PMIC_STBY_REQ pin (which requesting the transition to STANDBY mode from RUN mode) goes HIGH, BUCK1/3 and BUCK2 operate at a preset low voltage or turned off. The other regulators continue to operate as in the RUN mode.

5.1.7 PWRDN mode

In the PWRDN mode, PCA9451A regulator starts the Power Down sequence.

See Section 5.3.2 for Power Down sequence.

5.2 Operating mode transition table

5.2.1 State transition table for VSYS terminals and major terminals

The state transitions of the VSYS pin and major pins are shown in Table 2. The "*" in the table means that the input signal level has no effect on the operating mode transitions.

Table 2. State transition table for VSYS pin and major pins

	I/O	OFF mode	READY mode	SNVS mode	PWRUP mode	RUN mode	STANDBY mode	PWRDN mode
VSYS	I	< VSYS_POR	> VSYS_POR	> VSYS_UVLO	> VSYS_UVLO	> VSYS_UVLO	> VSYS_UVLO	> VSYS_UVLO
PMIC_ON_REQ	I	*	*	LOW	HIGH	HIGH	HIGH	LOW
PMIC_STBY_REQ	I	*	*	*	*	LOW	HIGH	*
POR_B	O	LOW	LOW	LOW	LOW	HIGH	HIGH	LOW
RTC_RESET_B	O	LOW	LOW	HIGH	HIGH	HIGH	HIGH	HIGH

The POR_B pin is the reset signal output pin to the i.MX 93, and the RTC_RESET_B pin is the reset signal output pin for the 32.768 KHz crystal oscillator driver. A HIGH output indicates reset release, and a LOW output indicates reset status.

5.2.2 Regulator state transition table by mode of operation

Table 3 shows the operating conditions of the regulator in each operating mode. The "*" in the table means that the output signal level is indefinite.

Table 3. Regulator state transition table by operating mode

	OFF mode	READY mode	SNVS mode	PWRUP mode	RUN mode	STANDBY mode	PWRDN mode
BUCK1/BUCK3	OFF	OFF	OFF	*	0.85V	0.85V	*
BUCK2	OFF	OFF	OFF	*	0.6V	0.6V	*
BUCK4	OFF	OFF	OFF	*	3.3V	3.3V	*
BUCK5	OFF	OFF	OFF	*	1.8V	1.8V	*
BUCK6	OFF	OFF	OFF	*	1.1V	1.1V	*
LDO1	OFF	OFF	1.8V	1.8V	1.8V	1.8V	1.8V
LDO4	OFF	OFF	OFF	*	0.8V	0.8V	*
LDO5	OFF	OFF	OFF	*	1.8V or 3.3V	1.8V or 3.3V	*

5.3 Power up/down sequence

Figure 5 shows the Power Up/Down sequence.

POK in Figure 5 means Output Power good or Power OK, indicating that 85% of the set output voltage has been reached.

VINT in Figure 5 shows the output of the internal LDO, and CLK_32K_OUT shows the output of the 32.768 kHz crystal oscillation driver.

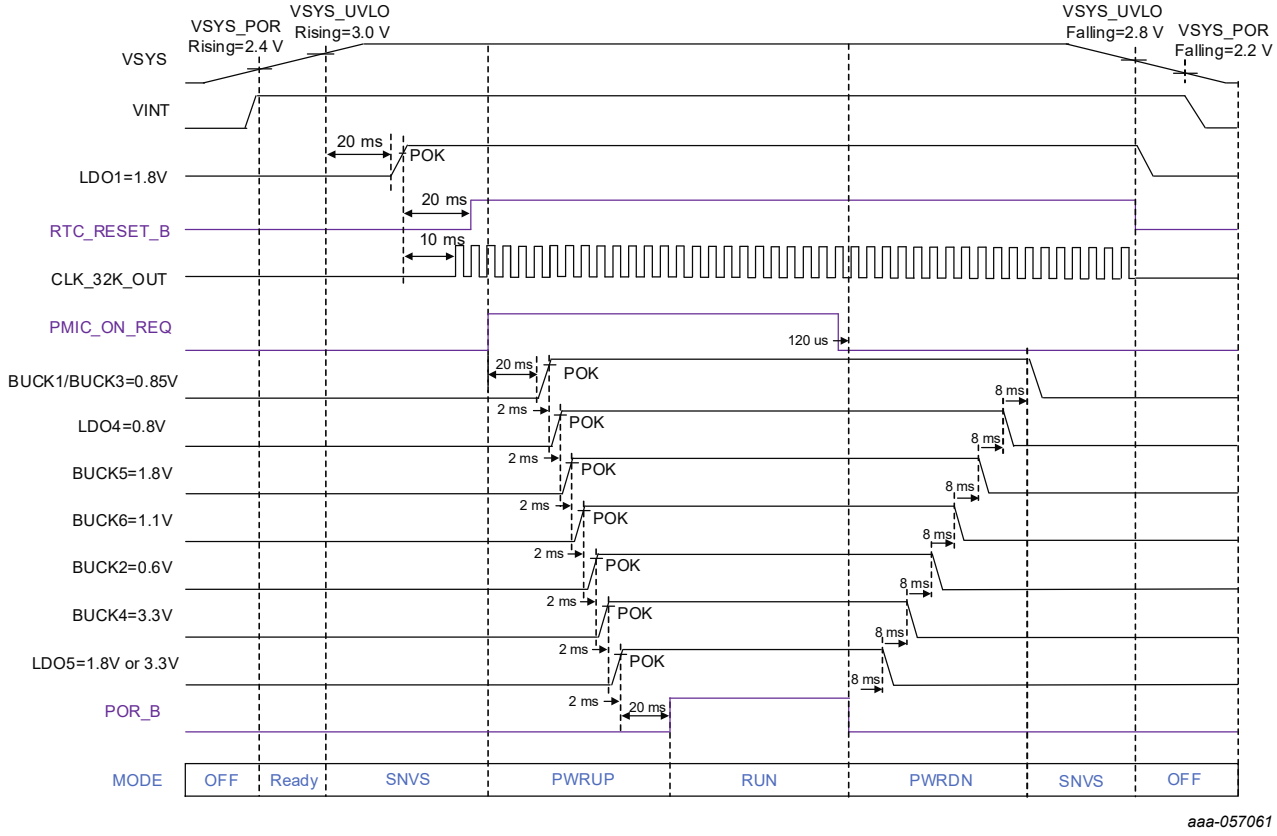


Figure 5. Power up/down sequence

5.3.1 Power up sequence

When the VSYS pin voltage exceeds the VSYS_POR threshold voltage, the device transitions to READY mode from OFF mode and internal LDO (VINT) is enabled.

When the VSYS pin voltage exceeds the VSYS_UVLO (Under Voltage Lock Out) voltage, the device transitions to SNVS mode and LDO1 starts output after 20 ms. When LDO1 reaches POK, CLK_32K_OUT starts output after 10 ms and RTC_RESET_B asserts HIGH after 20 ms.

When a HIGH level signal is applied to the PMIC_ON_REQ pin from the i.MX 93 in the SNVS mode, the mode transitions to the PWRUP mode. After 20ms from that point, the Power Up sequence starts and each regulator starts up in the order BUCK1/3, LDO4, BUCK5, BUCK6, BUCK2, BUCK4, LDO5. When the output voltage of each regulator reaches POK, the next regulator begins to rise after an interval of 2 ms. The last LDO5 output voltage reaches POR, and 20 ms later the POR_B signal (i.MX 93 reset release) rises and the RUN mode is entered.

5.3.2 Power down sequence

When a low level is applied to the PMIC_ON_REQ pin in RUN mode or STANDBY mode, the IC transitions to PWRDN mode after debounce time (120 us) and the POR_B signal falls to start the Power Down sequence. Each regulator starts powering down at 8 ms intervals in the reverse order of the Power Up sequence. When the last BUCK1/3 finishes power down, it transitions to SNVS mode.

When the VSYS pin voltage falls below the VSYS_UVLO (Under Voltage Lock Out) voltage, LDO1 and 32.768-kHz clock supply are stopped and the device transitions to OFF mode. LDO (VINT) is stopped.

5.4 STANDBY mode transition

Figure 6 shows the transition between RUN mode and STANDBY mode controlled by the PMIC_STBY_REQ pin. i.MX 93 applies a HIGH level signal to the PMIC_STBY_REQ pin, the PCA9451A goes from RUN to STANDBY mode. When the i.MX 93 applies a LOW level signal to the PMIC_STBY_REQ pin, the PCA9451A goes back to RUN mode.

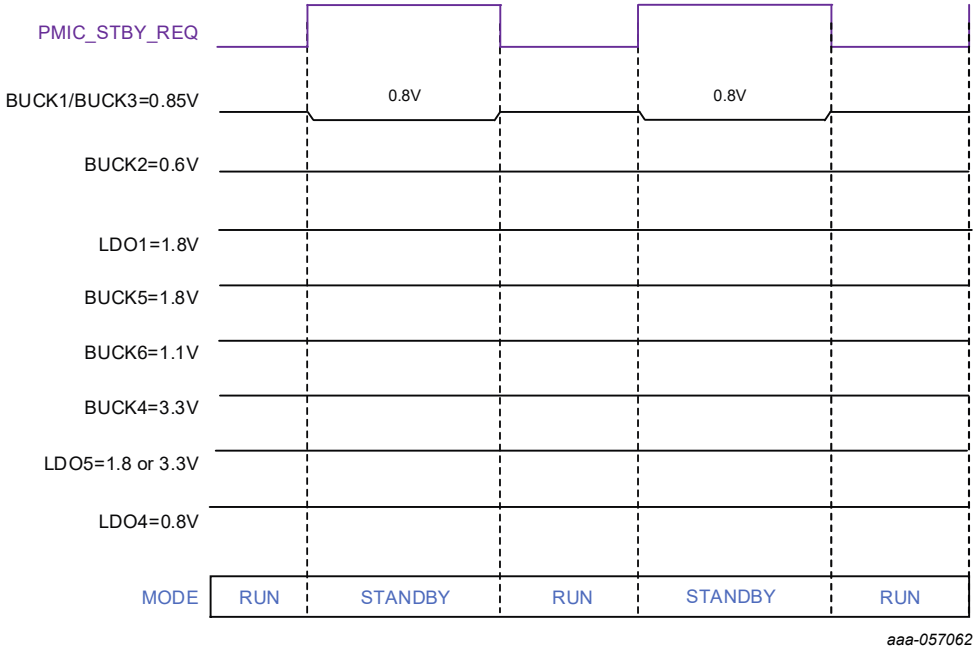


Figure 6. STANDBY mode transition

BUCK1/3 and BUCK2 can be set to different output voltages for RUN mode and STANDBY mode, respectively. This function reduces the overall system power consumption during STANDBY mode.

In the example shown in Figure 6, BUCK1/3 = 0.85 V during RUN mode, and BUCK1/3 = 0.8 V during STANDBY mode.

6 System function blocks

6.1 32.768 kHz crystal oscillator driver

The PCA9451A has a 32.768 kHz crystal driver that provides an accurate clock to the i.MX 93. This clock can be used to drive the RTC in the i.MX 93. The PCA9451A outputs a clock continuously unless it is in OFF mode. This feature allows the i.MX 93 to use a high precision, internal RTC, eliminating the need for an external RTC.

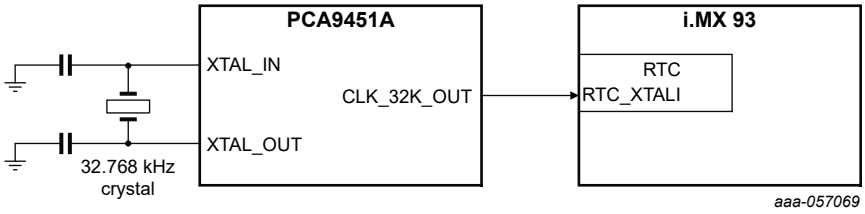


Figure 7. 32.768kHz crystal oscillator driver connection example

6.2 I2C level translator

The PCA9451A has a level translator for I2C. 1.8 V, the voltage of the I2C interface of the i.MX 93, can be passed through this I2C level translator to enable communication with peripheral devices with 3.3 V/5 V I2C interfaces.

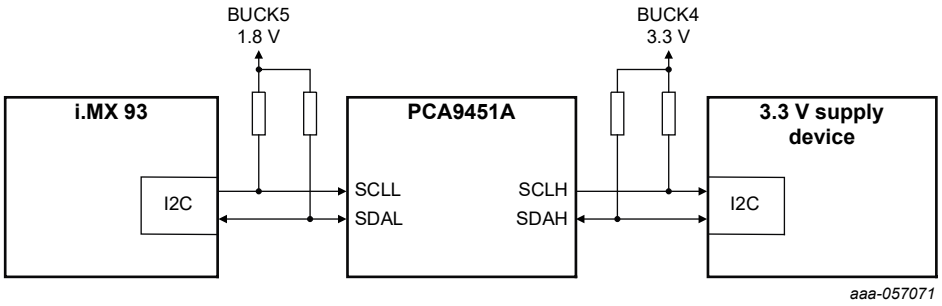


Figure 8. I2C level translator connection example

In the example shown in Figure 8, SCLL and SDAL on the low-voltage side are connected to BUCK5 = 1.8 V, and SCLH and SDAH on the high-voltage side are connected to BUCK4 = 3.3 V. The integrated IC level translator in the PCA9451A allows the i.MX 8M Plus to communicate with peripherals with a 3.3 V or 5 V IC interface without the need for additional level translation circuitry.

7 References

1. PCA9451A product information: https://www.nxp.com/pca9451A
2. PCA9451A data sheet: https://www.nxp.com/docs/en/data-sheet/PCA9451.pdf
3. PCA9451A application note: https://www.nxp.com/docs/en/application-note/AN13698.pdf
4. Evaluation Board Information: http://www.nxp.com/pca9451a-evk
5. MCIMX93-EVK (i.MX 93 with PCA9451A and LPDDR4X): http://www.nxp.com/i.MX93EVK

8 Revision history

Table 4. Revision history

Document ID	Release date	Description
AN14413 v.1.0	10 September 2024	• Initial version

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Tables

Tab. 1. i.MX 93 and peripherals power supply table 6
Tab. 2. State transition table for VSYS pin and major pins 10
Tab. 3. Regulator state transition table by operating mode 10
Tab. 4. Revision history 15

Figures

Fig. 1. PCA9451A internal block diagram 2
Fig. 2. PCA9451A block diagram 4
Fig. 3. i.MX 93 and peripheral device power connection diagram 7
Fig. 4. Connection diagram by DDR memory type 8
Fig. 5. Power up/down sequence 11
Fig. 6. STANDBY mode transition 12
Fig. 7. 32.768kHz crystal oscillator driver connection example 13
Fig. 8. I2C level translator connection example 13

Contents

1 Overview 2
1.1 Features 2
2 Block diagram 4
3 Power supply table and connection diagram 6
3.1 i.MX 93 and peripheral device power supply table 6
3.2 i.MX 93 and peripheral device power connection diagram 6
4 Connection by DDR memory type 8
5 Operation mode transition 9
5.1 Operating mode 9
5.1.1 OFF mode 9
5.1.2 READY mode 9
5.1.3 SNVS mode 9
5.1.4 PWRUP mode 9
5.1.5 RUN mode 9
5.1.6 STANDBY mode 9
5.1.7 PWRDN mode 9
5.2 Operating mode transition table 10
5.2.1 State transition table for VSYS terminals and major terminals 10
5.2.2 Regulator state transition table by mode of operation 10
5.3 Power up/down sequence 11
5.3.1 Power up sequence 11
5.3.2 Power down sequence 12
5.4 STANDBY mode transition 12
6 System function blocks 13
6.1 32.768 kHz crystal oscillator driver 13
6.2 I2C level translator 13
7 References 14
8 Revision history 15
Legal information 16