AN14395

EMC Guidelines for MCXA14x/15x MCU Designs

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Document information

Information	Content
Keywords	AN14395, MCXA14x/15x, EMC, MCXA153, MCU, EMI model, Bypass circuit, Decoupling circuit, Inter-board interface, Communication interface, Debug interface, PCB stack-up, USB High Speed signal, Shield connection, Signal return path, Digital filter
Abstract	This document introduces how to conduct a reasonable EMC design based on the MCXA14x/15x MCU, which helps the users maintain the robustness of the product's EMC performance.

1 Introduction

This document introduces some common methods to improve the Electromagnetic compatibility (EMC) performance based on the MCXA14x/15x MCU. It uses MCXA153 as an example to introduce the basic methods of EMC design. In addition, this document can be used as a guide or reference for customers in practical applications. It helps the customers in saving money and time, and improve product stability.

1.1 EMC significance

The importance of EMC within electronic devices has become more prominent with the development of the internal structure of contemporary electronic products. The EMC of a product directly determines the working performance of the product. Therefore, the EMC issue is given higher priority in the first stage of the product design itself.

1.2 Basic EMC concepts

Electromagnetic interference (EMI) is one of the major problems in modern electronic systems. To prevent the project schedule delays caused by the EMI problems, designers must pay attention to this issue in the early stages of design and then conduct preanalysis, prediction, and design the product.

The designers are expected to have good EMC knowledge and practical experience at all stages of product design, to make the product comply with the corresponding EMC standards before it becomes a commodity.

Figure 1 shows a simple EMI model consisting of EMI sources, coupling paths, and the affected devices.

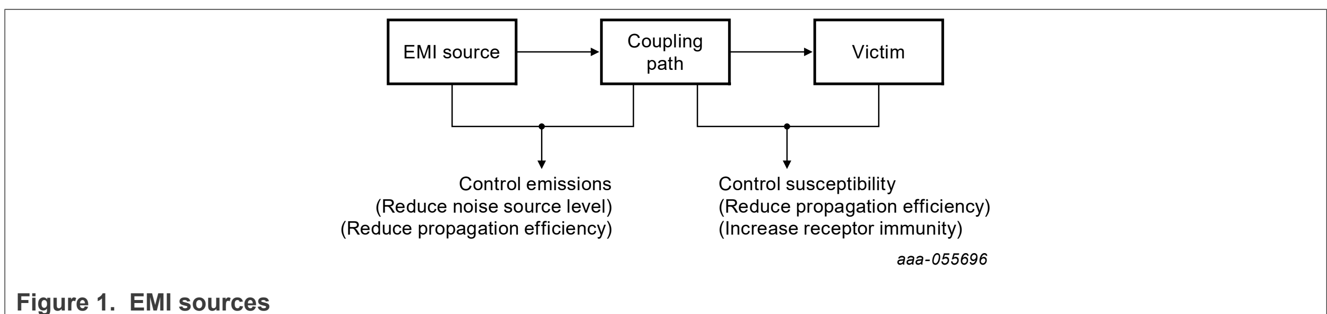

Figure 1. EMI sources

In Figure 1, the EMI problems in the system can be eliminated by reducing the noise of the EMI source, changing the coupling path, and improving the anti-interference ability of the receptor.

- To reduce the noise of EMI sources:
  - Reduce the loop area of the noise source
  - Use slower rising and falling edge signals in the noise source
  - Reduce the drive signal
  - Increase filtering
  - Shield the noise source circuit
- To change the coupling path:
  - Move the receptor away from the noise source.
  - Avoid PCB trace coupling and power supply coupling between the receptor and noise source.
- To improve the anti-interference ability of the receptor:
  - Reduce the loop area of the PCB circuit related to the receptor.
  - Provide low-impedance return paths and reference power planes for signal lines associated with the affected device.

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1.3 Basic principles of EMC design

Any problem occurrence in the electronic compatibility of the product causes a rework in the product design. To avoid this situation, the subsequent topics of this document are designed to help the designers understand better on how to enhance the immunity (sensitivity) and meet the radiation requirements.

Although the modern electronic systems have different immunity requirements, the radiated immunity (RI) and the electrostatic discharge (ESD) test methods are similar.

The following list provides the common issues in the boards, which can be reduced through basic design solutions:

- EMI interference: In the radiation immunity test, the EMI caused by high-energy and high-frequency environments may damage to circuit components in the system (EUT). To solve the EMI problem, a basic design method is implemented in which the sensitive components (microcontrollers) are moved away from the working environment.
  Note: *The working environment signal and power lines are in the high spectrum range, such as 10MHz-900MHz.*
- ESD current: Based on the ESD characteristics, the short-term high-energy energy pulses generating the spectrum range, such as DC-300MHz are introduced into the system. These may inturn damage to some of the sensitive components in the system. To prevent the ESD current and energy from being an input to the sensitive components, the basic solution is introduced which provides high impedance on signal and the power lines relative to the case ground.
- Radiation: In the system, the electromagnetic generation radiation must be reduced as much as possible so that it does not affect the other equipment. The basic design techniques are used in RI and ESD to resolve these radiation issues. The basic approach is to eliminate high-frequency interference voltages and currents generated by the test system.
- Coupling: Segmentation is the use of physical separation to reduce the coupling between different types of circuit, particularly by the power and ground tracks.
  Figure 2 shows a typical example of separating four different circuits using the segmentation technique. In the ground plane, the unmetallized moat is used to isolate the four ground planes. The L and C provide filtering for each part of the board, coupling between different circuit power planes is reduced. High speed digital circuits are placed near the power supply inlet because of their higher transient power demand.
  The interface circuit requires ESD and transient suppression components and circuits. For the L and C, use different values of L and C filter components instead of one large L and C. Because, they can provide different filtering characteristics for different circuits.

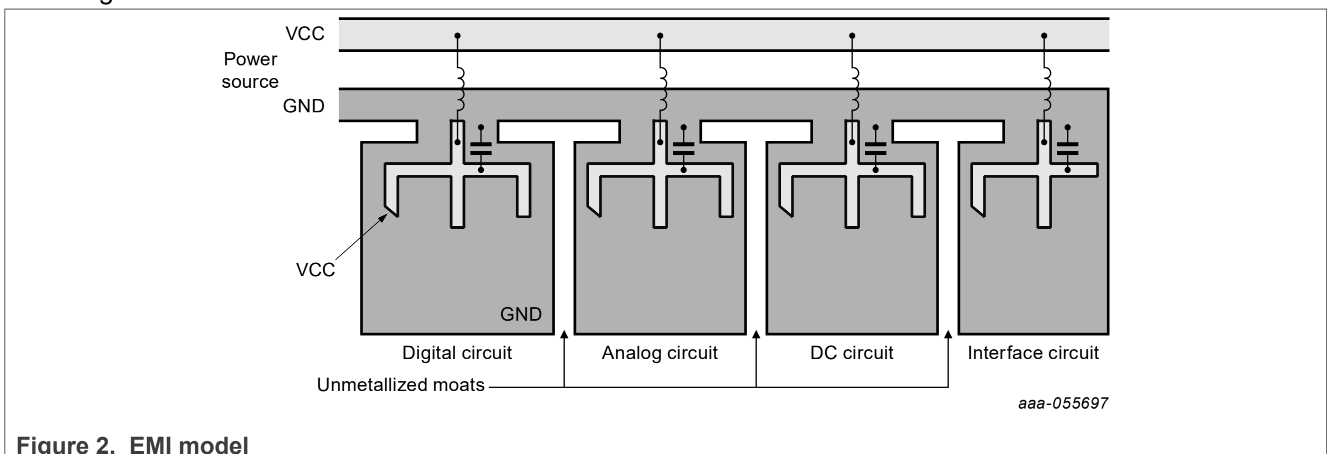

Figure 2. EMI model

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2 PCB design

In the board design, some key circuits design play a decisive role in EMC/EMI/ESD performance, such as:

- Crystal oscillator circuit
- Reset circuit
- Unused pin configuration
- Inter-board interface
- Communication Interface
- Power configuration

Details of these design aspects are presented in the subsequent sections of this document. The MCXA153 processor is used as an example to introduce the relevant design rules.

2.1 Crystal oscillator circuit

The MCXA14x/15x MCU uses an external 8 MHz crystal oscillator as the main clock reference. Also, it allows the use of an external clock source.

- External clock: An active crystal oscillator can be used as an external reference clock. The active crystal oscillators generally have better ESD performance than crystal oscillators. Hence through experience, it is recommended to use the active crystal oscillators. The ESD performance of systems using the active crystal oscillators is improved by about 2KV when compared to the systems using passive crystal oscillators.
- Internal clock: Usage of internal clock as the reference clock improves the EMC performance greatly.

2.2 Reset circuit

Figure 3 shows the reference reset circuit. It is recommended to place an RC circuit close to the Reset pin to reduce the noise impact.

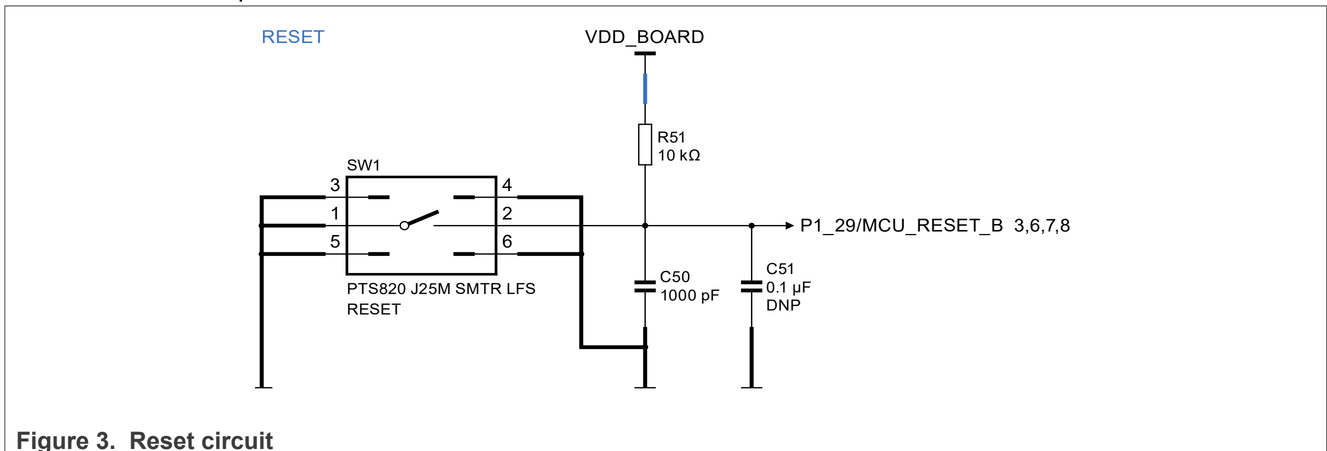

Figure 3. Reset circuit

2.3 Unused pin configuration

The unused pins may affect the EMC performance, which can lead to increase in power consumption and the corresponding GPIO state may change under harsh EMC conditions. For example, a pin with a high impedance input can switch states frequently under harsh EMC conditions, which increases power consumption and cause other EMC problems.

Note: *It is recommended to avoid connecting the unused pins directly to GND. The GPIO configuration registers may change under poor EMC conditions. If the output level is high, then in this case a large current is generated and the pin gets damaged.*

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Generally, data sheets provide recommendations for unused pin connections. For details, refer to the following configurations:

- To determine whether the unused pins are allowed to float, refer the data sheet.
- If a pin is allowed to float, it is configured as a GPIO and outputs 0 or 1.
- If the pin is not allowed to float, it is recommended to pull it down to GND through a resistor, such as 10 kOhm.

2.4 Inter-board interface

For the signals transmitted between the boards, you must take care of the signal loop design. If the signal loop is relatively large, it may receive the interference noise easily and radiate noise. For example, Figure 4 shows the AC signal with long high-impedance signal loop from the power board to the processor control board (from VDDA through the operational amplifier (U28) to AGND). Therefore, a lot of noise occurs which is coupled to the processor.

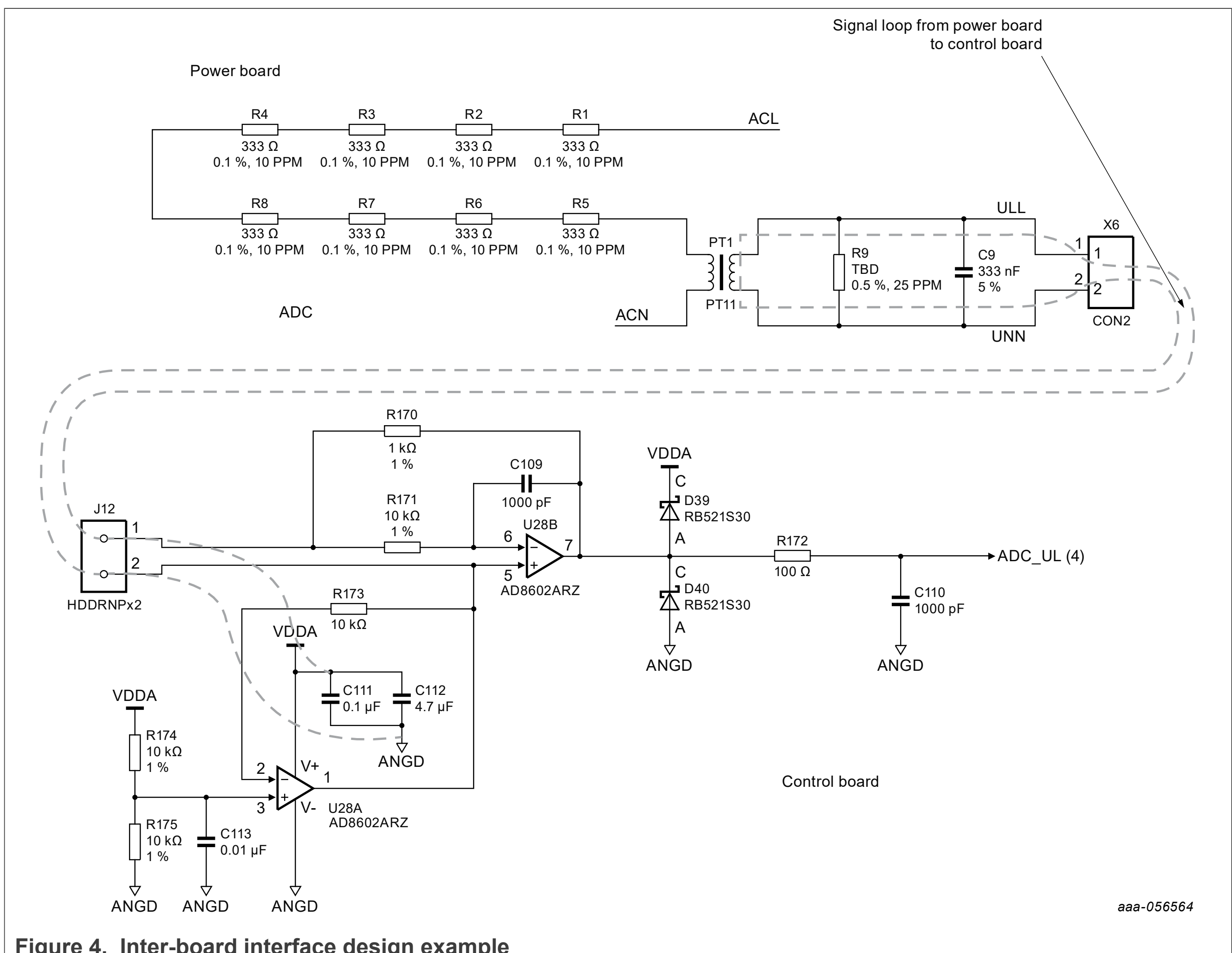

Figure 4. Inter-board interface design example

Figure 4 also shows the following options to shorten the signal loop:

1. Move PT1 to the processor control board to shorten the input signal loop. Experiments have proven that the modified direct contact discharge test results increased from 4 KV to 8 KV, thereby improving the EMC performance.

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2. Move the operational amplifier circuit to the power board and connect VDDA and AGND from the control board to the power board. This results in a relatively smaller loop between the ADC signal, VDDA and AGND, thereby improving the EMC performance.

For situations where the processor signal is directly connected to the connector, it is recommended to introduce the TVS components as ESD protection. Figure 5 shows a low-cost solution using the RC components. For the R and C value, the operating frequency of the signal is taken into consideration, and the RC time constant is required to be much smaller than the signal period.

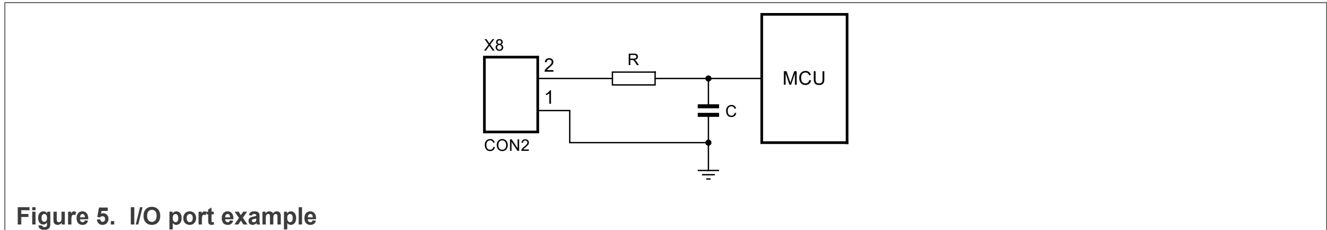

Figure 5. I/O port example

If there are high-speed signals or clock signals on the interface, it radiates the noise easily. It is recommended that the ground wire must be close to the high-speed signal or clock signal. In addition, the matching resistors can be reserved on the board which can reduce the energy of the signal circulation path and signal harmonics. Some devices support the software to adjust the signal drive capability. The software can be used to reduce the signal drive capability which in turn reduces the harmonic noise radiation.

2.5 Communication interface

In communication interfaces, several measures are taken to improve the EMI and ESD performance as given below:

- To suppress transient voltages, use TVS diodes on the signal return path of the connector .
- To isolate high-frequency noise, connect a ferrite bead between the connector's power and the board's power.
- To eliminate high-frequency common-mode noise, connect a common-mode choke between the differential signals in parallel between the connector's metal shield and circuit board ground.

2.5.1 USB

To improve the ESD performance, it is recommended to take the following measures:

- Use TVS arrays to protect VBUS, D+, D-, and ID signals.
- Use a common mode choke when connecting the USB differential signals to improve EMI performance.
- Connect ferrite beads in series to the power pins (VBUS, GND) to isolate high-frequency noise.
- Isolate the USB case and board ground with RC or ferrite beads to improve ESD performance.

Figure 6 shows the schematic diagram of the USB part of MCXA153.

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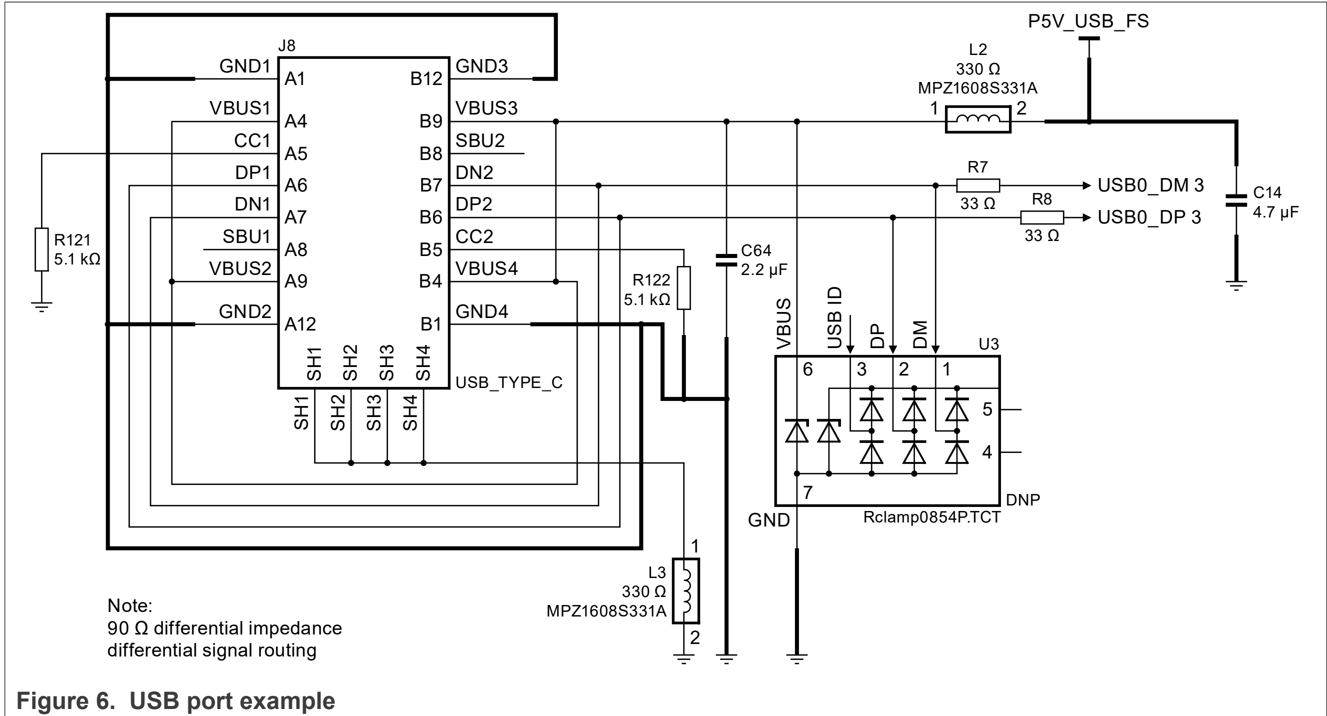

Figure 6. USB port example

2.5.2 Debug interface

The debugging interface is widely used in product design and mainly in the product development stage. Some key signals are easily interfered in harsh environments. To reduce the interference, TVS protection can be added, or a 0 ohm resistor can be connected in series to the debugging interface.The stage during development is used for debugging. To protect the sensitive signals from easy interference, the 0 ohm resistor is removed during the mass production stage.

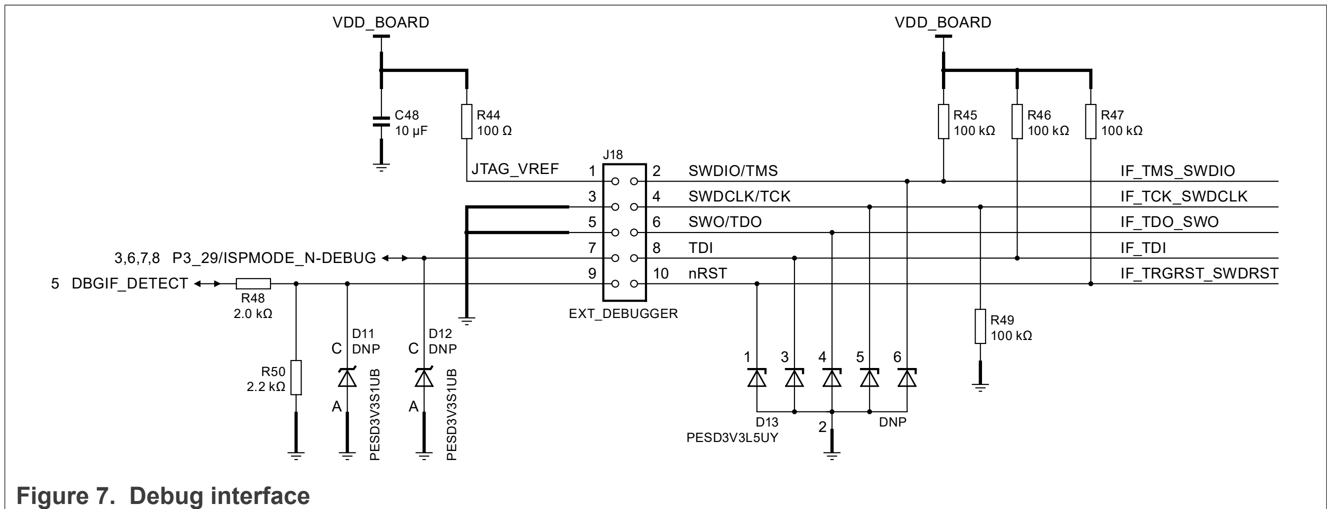

Figure 7. Debug interface

2.6 Effect of ground jump

The MCXA14x/15x MCU contains multiple power domains, such as VDD_ USB, VDD_ANA, VDD_ CORE, and VDD_SYS.

Multiple IOs change from logical state 1 to 0 or from 0 to 1 at the same time, which causes:

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- Parasitic capacitance and inductance to charge and discharge frequently, thus causing ground failure.
- Power supply failure, which affects some sensitive signals. Especially, the signals with same power domain as these are parallel interfaces.

Suggestions to avoid ground interferences and power suppy failure are given below:

1. Follow the layout recommendations for the high-speed signals as shown in Section 3.
2. Do not locate sensitive signals and parallel interfaces in the same power domain.
3. Add an RC circuit to the sensitive signal input for reducing the external noise influence.

2.7 Power topology

At the beginning of the design, priority should be given to power topology design, including power device selection, voltage distribution in different power domains, and system power-on timing. It is recommended to make a list of all the required power supplies before system design, which can help the designers to have a clear understanding of the entire power supply framework design.

In this context, the power supply design of MCXA153 is taken as an example to list the power supplies in the system and the corresponding information.

Table 1. Power supplies

Power supply name	Default voltage (V)	Introduction
SYS_5V0	5.0	• Power input, AC-DC adapter or USB VBUS. • Powers the DCDC converter and USB host.
LDO_3V3	3.3	• Derived from LDO On board. • Provides power to the processor and most onboard components.
VDD_MCU	3.3	• Derived from LDO_3V3. • Powers the main power supply of the processor.
VDD_ANA	3.3	• Derived from LDO_3V3. • Provides power to the processor and onboard analog components. VDDA.
USB0_VBUS	5.0	VBUS for USB.

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3 PCB layout

3.1 PCB stack-up and multi-layer board layout designs

This section provides different ways to reduce the EMI and EMC of the boards using PCB stack-up design.

In addition, it provides recommended measures to reduce the impedance of power and ground planes in multilayer board layout design.

3.1.1 PCB stack-up design

The MCXA14x/15x MCU has a large number of signal interfaces. Therefore, it is recommended to use either a 2-layer or 4-layer PCB design.

3.1.1.1 2- layer PCB stack-up structure

The 2-layer board usage reduces the cost to a minimum. For the MCXA14x/15x MCUs, it can meet the basic requirements in most applications.

Figure 8 shows the stacking diagram of a 2-layer board using FR4 dielectric substrate.

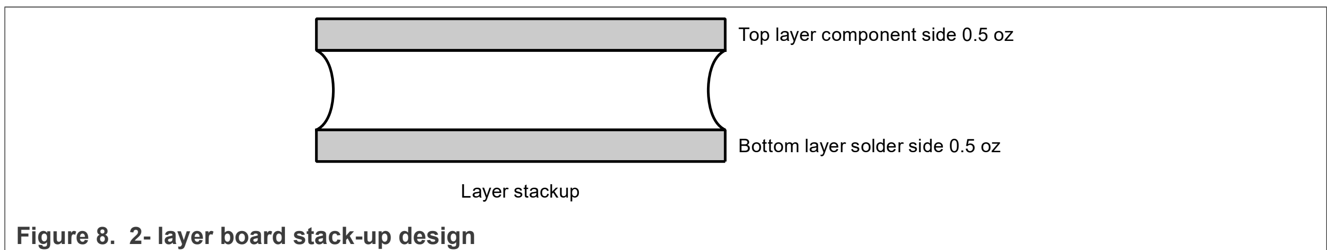

Figure 8. 2- layer board stack-up design

3.1.1.2 4- layer PCB stack-up structure

The 4-layer PCB stack design has certain advantages and benefits for high-speed signals. First, the ground plane and power plane can provide good reference planes for the characteristic impedance design of high-speed and differential signals. In addition, the ground and power planes provide shorter return paths for current and reduce the ground-to-power impedance. The size of the equivalent loop antenna is directly related to the size of the current loop, and the size of the antenna directly affects the generation of noise. Therefore, reducing the equivalent antenna loop can effectively avoid EMI interference and improve EMC performance.

Figure 9 shows an example of a 4-layer board stack-up design.

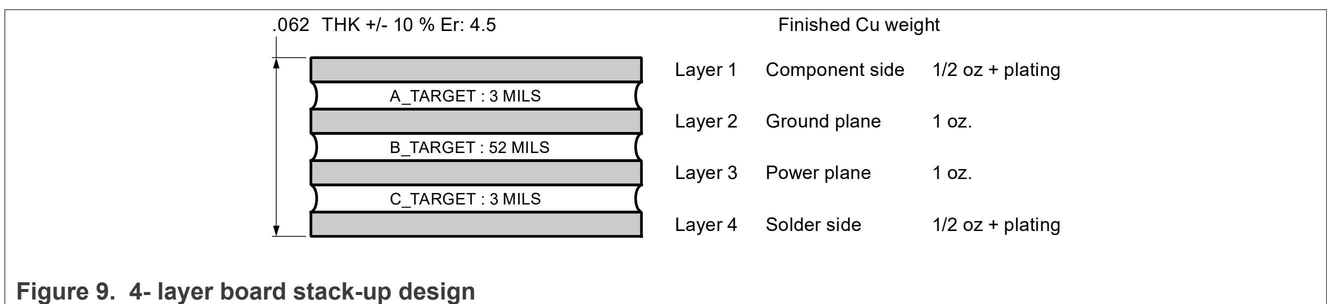

Figure 9. 4- layer board stack-up design

3.1.2 Power and ground impedances reduction

In the multi-layer board layout design, it is generally recommended to set up the power planes and ground planes separately. This reduces the impedance of the power and ground loops.

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Following are the recommendations to maintain or reduce the impedance of the power and ground planes:

- Refer to Rule 20-H. The 20-H rule is a guideline for the design of power and ground layers in multilayer boards. The main principle of this rule is to extend the edge of the ground layer from the edge of the power layer by about 20 times the distance between the two planes. This reduces the impact of fringe field radiation at the edge of the board.
- Place as many vias as possible on the power layer and ground plane, and maintain the integrity of the power layer and the ground plane.
- Place vias in appropriate locations. This reduces the impedance of the power layer and the ground plane, helping to provide a low-impedance return path for the signal.
- Avoid signal traces crossing different reference planes. Otherwise, signal integrity issues are introduced. At the same time, when dividing the multiple power planes and ground planes, give priority to the layout and routing of sensitive signals.

3.2 Layout

When designing the PCB layout, there are some recommended key points which need more attention. Before placing components, circuits with different functions should be classified, such as power supplies, analog circuits, digital circuits, and high-speed interface connectors. These circuits should be placed in different areas of the PCB board.

Recommended points to consider during PCB designing:

- The placement of power circuit near the power input terminal. Component placement should be in the order from high voltage to low voltage.
- The placement of decoupling capacitor of the LDO regulator should be as close as possible to the input and output ports.
- Compared to digital circuits, analog circuits are more susceptible to external interference signals. Therefore, the analog circuits must be placed away from the high-voltage and high-speed digital circuits to reduce coupling paths for noise interference.
- An adequate clearance between the high-speed interface connectors and the sensitive components must be maintained.
- The placement of RF, AD/DA, and analog sensor circuits, as they are sensitive to noise.
- The placement of crystal must be close to the MCU and surrounded by the ground wires to keep a safe distance from the other sensitive components.

3.3 Bypass and decoupling

To bypass the parasitic inductance, you must follow the below given recommendations:

- Place the small-capacity and large-capacity decoupling capacitors nearby the MCU power pin, such that the current must first pass through the capacitor and then enter the power pin.
- Place the decoupling capacitors as close as possible to the power pins. It is very important for the processor to ensure that the parasitic inductance of the filter circuit is minimized and the power supply has the ability to provide transient high current.
- Take care of the current return path of the decoupling capacitor and bypass capacitor, and ensure that the return path is as short as possible.

Figure 10 shows the decoupling capacitor routing.

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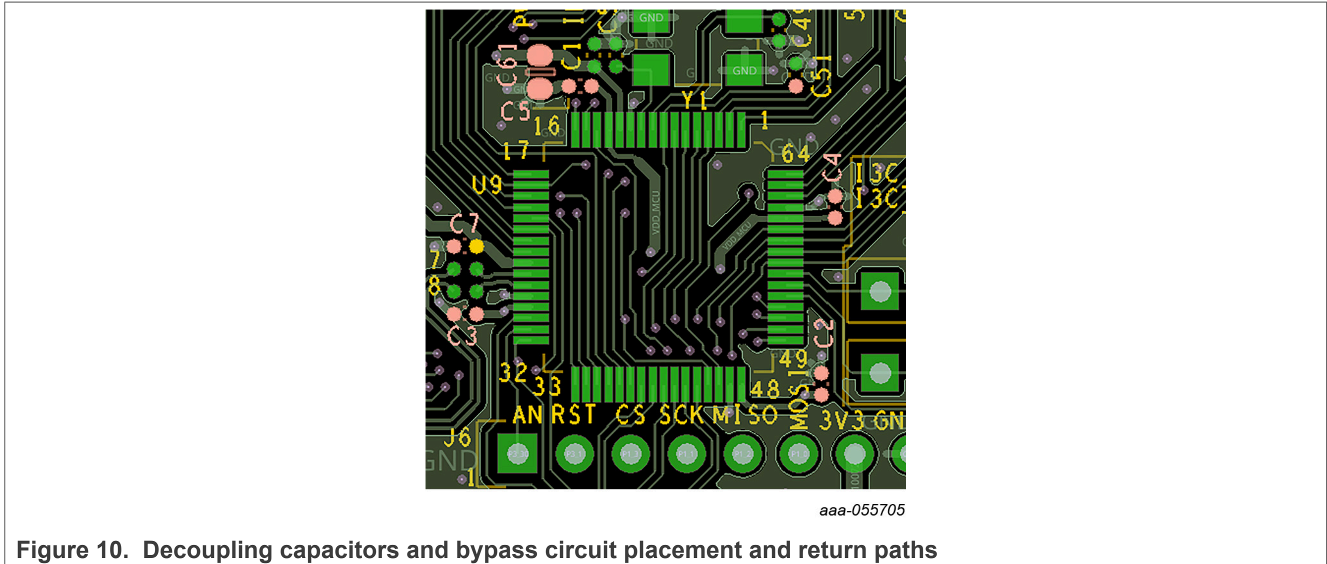

Figure 10. Decoupling capacitors and bypass circuit placement and return paths

3.4 Crystal oscillator circuit

The two types of crystal oscillator circuits used are:

- Passive crystal oscillator: Connected between the XTALIN and XTALOUT pins of the microcontroller
- Active crystal oscillator

Generally, the crystal oscillator generates noise and it is a device susceptible to interference. Therefore, you must ensure that the crystal oscillator wiring is proper.

Here are some of the recommended layout options:

- Traces between the crystal and XTALIN/XTALOUT should be as short as possible. Also, keep the lengths of both traces equal.
- Place the load capacitor and feedback resistor close to the crystal to reduce the effects of parasitic inductance.
- The crystal must be isolated from other circuit components by ground wires.
- The ground plane must be directly beneath the components and the traces that are associated with the crystal.
- Other signal lines should avoid passing through the adjacent layers of the crystal .
- Increasing the driving strength of the crystal oscillator drive circuit results in better EMS performance. But, it may also increase the power consumption and can cause EMI problems.
- Use an active crystal oscillator for better EMS performance.

3.5 USB high speed signal

The following are guidelines for USB high-speed signal routing:

- High-speed signals (USB) avoid crossing different reference planes.
- Avoid slots, holes, and splits in the reference planes.
- When conversion between different reference planes is necessary, provide ground return vias within 100-mil of the signal layer conversion vias.
- Data, address, clock, and control signal lines should have impedance matching and trace length control (the length difference depends on the bus speed), and maintain the same number of vias.

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Note: *The propagation delay and impedance control must be considered to ensure good communication between the devices.*

3.6 Shielded connection

Some connectors are in metal and can have either conductive shells, exposed shells, or accessible to components, such as USB and network interface sockets. Therefore, ESD performance should be considered when designing.

Here are some of the basic design guidelines for Shielded connections:

- A separate shield ground should be placed under the connector (network interface/USB).
- The shell ground of the connector should be connected to the ground of the PCB board using RC or ferrite beads. Proper care should be taken during selection of the connection location and component parameters, which are crucial to EMC and EMI performance.
- Enclosure ground loops should be kept as small as possible to avoid crossing critical signals or components, such as microcontrollers.

Figure 11 shows an example of Shield connection.

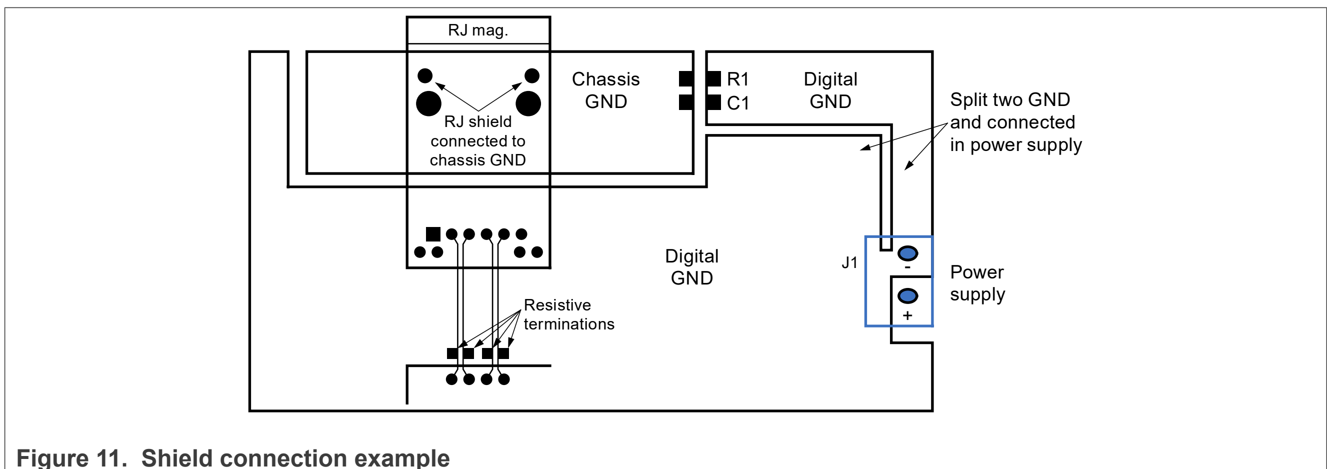

Figure 11. Shield connection example

Recommendation:

The Shielding ground should be connected to the power ground through an RC circuit or ferrite beads rather than connecting directly to the digital ground of the PCB. This prevents noise from seriously interfering with the digital ground and thus protects the sensitive signals.

3.7 Isolation

Isolation is often used in designing, such as isolating strong current and weak current, or different power supplies. In this context, RS485 circuit is used in the MCXA concentrator as an example to introduce the layout method.

An Optical isolator IC is used for isolation between the RS485 receiver and the system MCU. To improve the isolation performance, an isolation gap is set under the RS485 receiver, and this isolation gap is applied to all the planes (top/power/ground/bottom) to ensure good isolation performance.

Figure 12 shows an example of RS485 isolation circuit.

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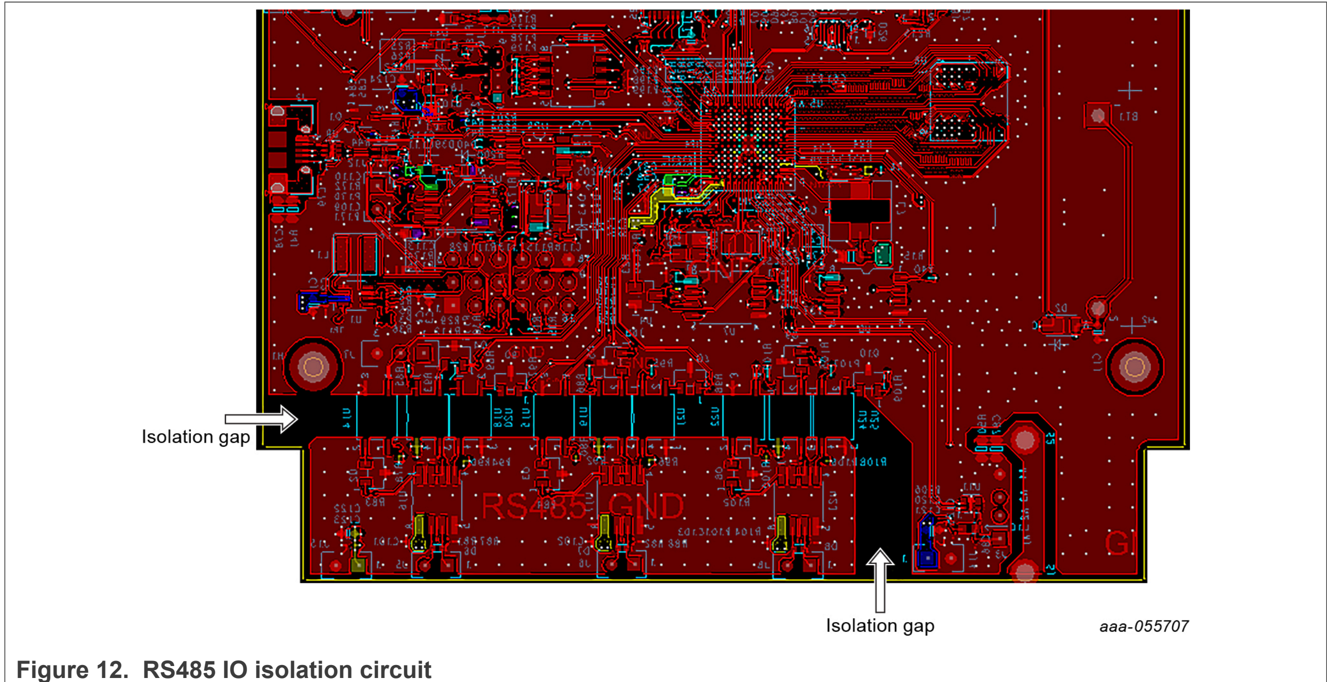

Figure 12. RS485 IO isolation circuit

3.8 Signal return path

It is known that a circuit is a closed loop between a source device and a terminal device. Regarding the signal return path and power supply loop, the signal return path has always received higher attention. In reality, both signal and power have their own return paths. The ground plane can be the reference plane for signals and power, but the power plane can also be the reference plane for signals. The smaller the loop area, the smaller the impedance, and the smaller is the impact of crosstalk and electromagnetic interference (EMI).

Figure 13 shows a DC-DC conversion circuit. By placing the decoupling capacitor close to the input and output ports, the return signal can flow directly from the Top layer to the source, which inturn minimizing the current return path and impedance.

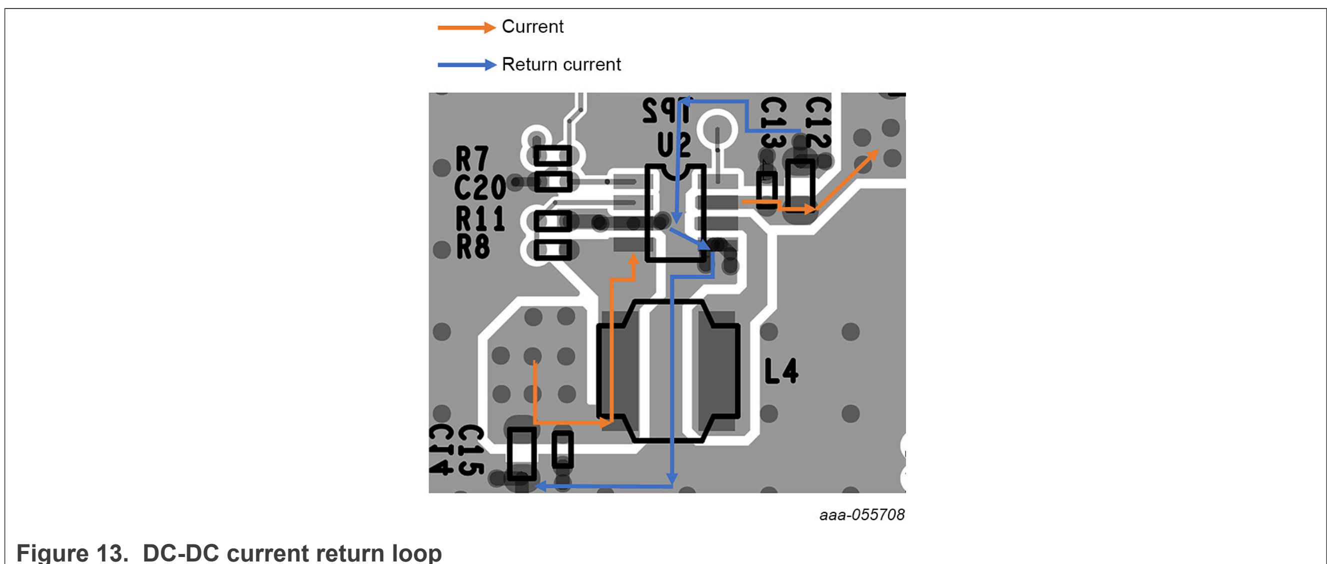

Figure 13. DC-DC current return loop

When considering the signal return path, ensure to avoid the disconnect points in the current loop path. The smaller the area of the current loop, the better the EMC performance.

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4 Software design

Good software design is a good way to improve EMC performance. It also improves the system stability without adding any additional costs.

4.1 Filter configuration for certain peripherals

To avoid noise interference, some peripherals support digital filters, such as the LPI2C, QDC in the MCXA14x/15x MCU. This function can filter the input noise according to a specified width. Figure 14 shows how to introduce a digital filtering device.

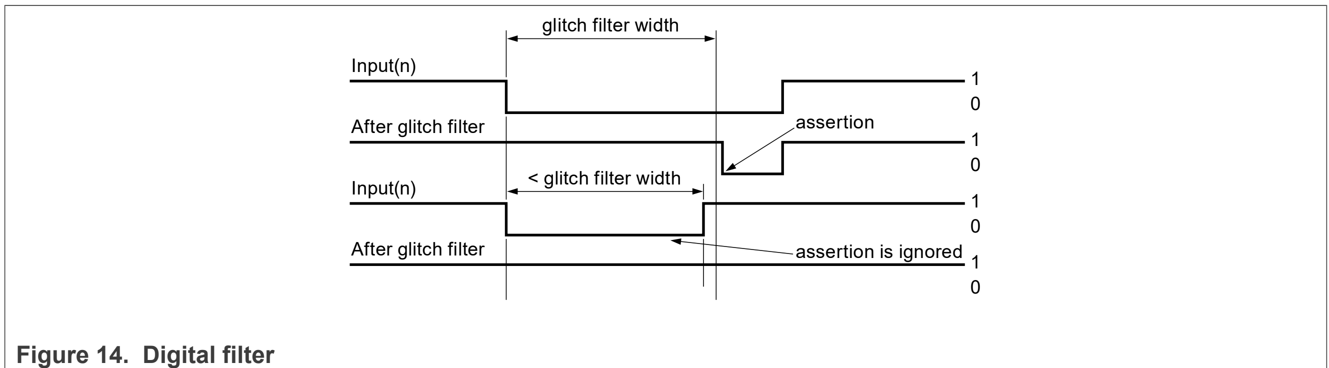

Figure 14. Digital filter

Figure 14 shows that the noise is filtered out and you can configure the filter width according to the application. To improve the EMC performance, it is recommended to enable the filter.

Consider the MCXA concentrator as an example. In the EFT test, the LPI2C filter started to work abnormally in the 4 kV test. After enabling the LPI2C filter, it can also pass the EFT test at 4.5 kV.

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5 EMC testing

Taking MCXA153 as an example, the EMC performance is evaluated based on the IEC61000-4-2 standards.

5.1 Test System Setup

Figure 15 shows the EMC test items. The EMC package includes various test items conducted in board level at NXP internal laboratory.

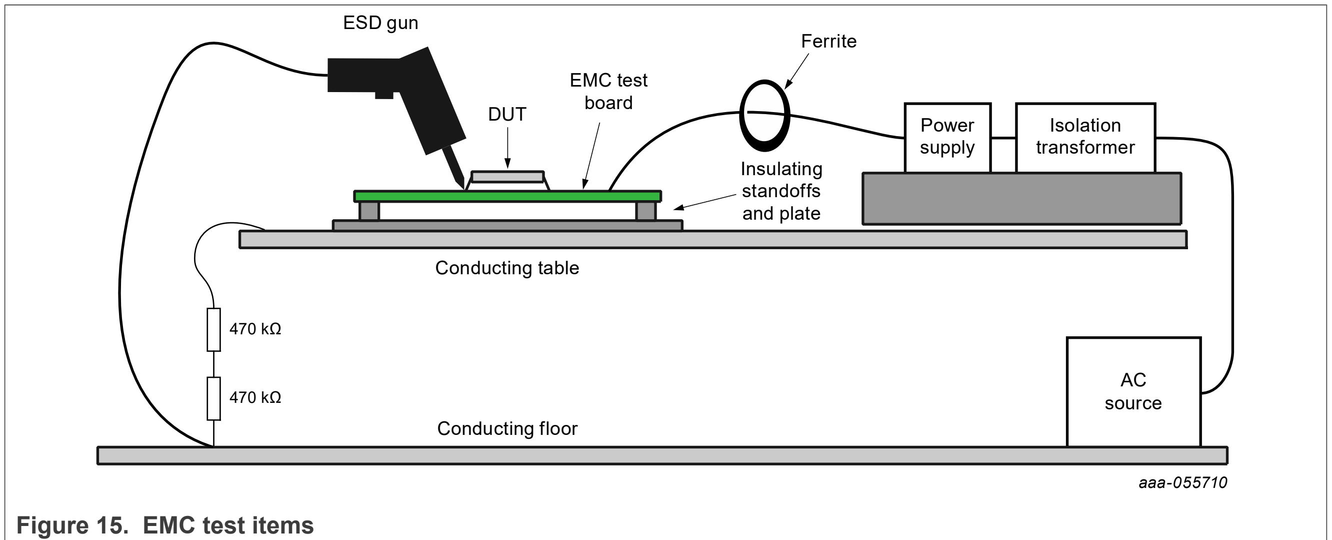

Figure 15. EMC test items

Table 2. EMC test items

EMC Test	Descriptions	Test Environment	Test Site
IEC61000-4-2 (ESD)	Direct Contact Discharge	Board Level	Internal

5.2 Test Result

The EMC test result focuses on board level EMC evaluation of MCXA153 (FRDM-MCXA153).

Table 3 shows the summarized results for each EMC test.

Table 3. MCXA153VLH PESD, IO Pins, and negative polarity injections

Board level EMC Test for FRDM-MCXA153	
MCU	MCXA153
Mask set	P07H
EMC Test	FRDM-MCXA153
IEC61000-4-2 (ESD) Direct Contact Discharge	Passed (+5 kV, -3 kV)

- For IO Pins under the positive ESD pulse injection:
  - Pin P0_3(52) was damaged at +8 kV injection
  - Pin P2_0(14), Pin XTAL48M(9)
  - Pin P2_7(21), Pin P1_4(62) occurred latch-up failure at +5 kV, +6 kV, +7 kV and +8 kV injection respectively.
  - Some Pins occurred self-reset failure

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  - The lowest level was +4 kV injected at Pin USB0_DM(26)
- For IO Pins under the negative ESD pulse injection:
  - P0_0(49) and Pin P0_3(52) were damaged at -7 kV injection
  - All pins under testing occurred latch-up failure except RESET_B(8) Pin
  - The lowest level was -4 kV injected at Pin XTAL48M(9), Pin P2_7(21), Pin P3_13(37), Pin P3_6(44), Pin P0_0(49) and Pin P0_3(52)
  - Pin RESET_B(8), Pin P2_7(21), and Pin P0_3(52) occurred self-reset failure at -2 kV, and -3 kV injection respectively
- For Power and GND Pins under the positive ESD pulse injection:
  - No Pin was damaged during testing
  - No latch-up failure was occurred during testing
  - Pin VDD_USB(25) occurred self-reset failure at +7 kV injection
  - The other Pins have passed +8 kV testing
- For Power and GND Pins under the negative ESD pulse injection:
  - No Pin was damaged during testing
  - No latch-up failure was occurred during testing
  - All the Pins under testing occurred self-reset failure, except Pin VSS(11,61)
  - The lowest level was -6KV injected at Pin VDD(29,60)

In the most extreme environments, additional protection of the microcontroller may be required. For more information about enhancing the transient immunity of microcontrollers, see AN2764.

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6 References

For additional information, you can refer to the following documents:

- AN2321, Designing for Board Level EMC
- AN3747, Pad Layout Application Note
- MCXA1XX Reference Manual from www.nxp.com

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7 Revision history

Table 4 summarizes the revisions to this document.

Table 4. Revision history

Document ID	Release date	Description
AN14395 v.1	22 July 2024	Initial public release

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Definitions

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