AN14389

MCX W71 Bluetooth LE Power Consumption Analysis

Rev. 1.0 — 10 September 2024 Application note

Document information

Information	Content
Keywords	AN14389, MCX W71, Low Power, Bluetooth LE
Abstract	This document provides information about the power consumption of MCX W71 wireless MCXs.

1 Introduction

This document provides information about the power consumption of MCX W71 wireless MCXs, how the hardware is designed and optimized for low-power operation, and how the software is configured to achieve the best low-power profile. The role of this document is to offer an overview and guidance on achieving the best low-power profile while maintaining the system's high performance. The setup and the procedures to measure the current consumption of the MCX W71 chip are also described in this document.

The power consumption of wireless devices is a critical requirement for the fast-coming Internet of Things (IoT) world. As a result, the hardware has been gradually improved and optimized from a power consumption perspective, and new communication standards have been developed. Bluetooth Smart (also known as Bluetooth Low Energy or Bluetooth LE) is part of these new standards developed for long-term battery operation, typically for years.

MCX W71 is radio-based MCX that supports the Bluetooth LE v5.2 protocol. The prerequisites for understanding this document are that the reader has good knowledge of the Bluetooth Smart protocol and basic knowledge about Arm MCX architecture and radio communication basics.

2 Acronyms and abbreviations

Table 1 defines the acronyms and abbreviations used in this document.

Table 1. Acronyms and abbreviations

Acronym	Description
ADC	Analog-to-digital converter
ADV	Advertising
Arm	Advanced RISC Machine (RISC – Reduced Instruction Set Computer)
Bluetooth LE	Bluetooth Low-Energy aka Bluetooth Smart
BPSK	Binary Phase-Shift Keying
BTLL	Bluetooth Link-Layer
CMP	Comparator module
DAC	Digital-to-Analog Converter
DC	Direct Current
DSM	Deep Sleep Mode
DUT	Device Under Test
ESR	Equivalent Series Resistance
FRDM	Freedom board
GAP	Generic Access Profile
GFSK	Gaussian Frequency Shift Keying
GPIO	General Purpose Input / Output
IEEE	Institute of Electrical and Electronics Engineers
IoT	Internet of Things
ISM	Industrial Scientific and Medical bands
LE	Low Energy
LL	Link-Layer

Table 1. Acronyms and abbreviations...*continued*

Acronym	Description
LLS	Low-Leakage Stop
LLWU	Low-Leakage Wake-up Unit
LPTMR	Low-power Timer
LPUART	Low-power UART
MBAN	Medical Body Area Network
MCX	Microcontroller Unit
NBU	Narrow Band Unit
O-QPSK	Offset Quadrature Phase Shift Keying
PC	Personal Computer
PDU	Protocol Data Unit
PMC	Power Management Controller
POR	Power-On Reset
RTOS	Real-time Operating Systems
RX	Reception
SAR	Successive Approximation Register ADC
SCGC	System Clock Gating Control register
SIM	System Integration Module
SMPS	Switched Mode Power Supply
SRAM	Static Random Access Memory
TMR	Timer
TSM	Transceiver Sequence Manager
TX	Transmission
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VLLS	Very Low Leakage Stop
XCVR	Transceiver

3 Bluetooth Smart power metrics

The following bullet lists the Bluetooth Smart power metrics.

- FRDM MCX W71 board is used to perform the several current measurements
- Low-power (central and peripheral) reference design application software is used (similar to the temperature sensor in Low-power mode) to set the device in different modes for the current measurements. The revision software used is the SDK PRC2 Release Candidate 2 (RC2) (1st August 2022).
- CM33 (core main power domain) and NBU (core radio power domain) could be active in of the state as follows:
  - Sleep mode
  - Deep sleep mode
  - Power-down mode

- Deep-power down mode
- CM33 is woken up (core wake-up power domain) and performs system initialization and some pre-processing
- Transceiver Narrow Band Unit (NBU) is woke-up and ready to operate. The CM33 may enter in Inactive mode if the software allows it.
- Transceiver is performing one or more RX / TX sequences
- CM33 is processing the received or transmitted packets
- Transceiver is put back in Sleep mode
- CM33 enters low-power (Deep sleep mode)

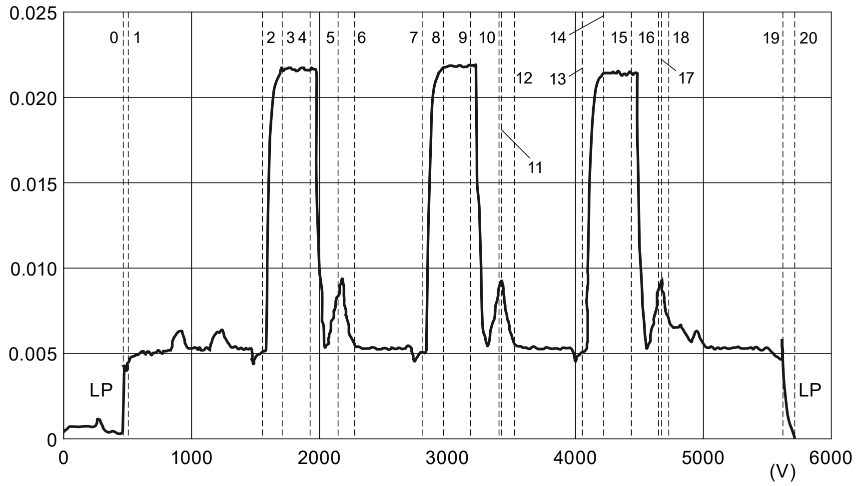

Figure 1. Typical operation cycle of a wireless low-power end device

Figure 1 shows how current consumption, varies over time for each operation cycle of the device.

At power-up, the system performs the so-called power-on reset, and after that it performs the system initialization. On the completion of initialization, the system enters in Low-power mode. There are several Low-power modes available for both MCXs and the radio, but usually the software defines only the most suitable combinations of CM33 and XCVR Low-power modes, for example, Deep-sleep mode for CM33 and NBU.

The timings shown in Figure 1 are explained in Table 2.

Table 2. Timings of a typical low-power device

Event - Peripheral	Event - Peripheral
LP. SoC in Deep Sleep mode	10. TX to RX transition
0. SoC awakes from Deep Sleep mode	11. XCVR Active RX
1. CM33 run: Pre-processing	12. XCVR RX warm down
2. XCVR TX warmup	13. CM33 STOP: RX to TX
3. XCVR Active TX	14. XCVR TX warmup
4. TX to RX transition	15. XCVR Active TX
5. XCVR Active RX	16. TX to RX transition
6. XCVR RX warm down	17. XCVR Active RX
7. CM33 STOP: RX to TX	18. XCVR RX warm down
8. XCVR TX warmup	19. CM33 RUN: Post-processing
9. XCVR Active TX	20. SoC going to Deep Sleep mode

Table 2. Timings of a typical low-power device...*continued*

Event - Peripheral	Event - Peripheral
-	LP. SoC in Deep Sleep mode

The time the transceiver switches from RX to TX is called RX to TX turnaround time, an essential parameter of the transceiver.

When the radio is operational, the CM33 performs various tasks, like serving interrupts or controlling various peripherals. Therefore, the best metric to be applied is current consumption over time, considering the average current of all implied entities.

3.1 Bluetooth Smart (LE)

Bluetooth Smart (Bluetooth Low Energy or Bluetooth LE) is a promising candidate for low-power communication and a good candidate for automotive applications (key fob and anchor) and IoT deployments. Bluetooth LE operates at a 2.4 GHz Industrial Scientific and Medical (ISM) band and uses Gaussian Frequency Shift Keying (GFSK) modulation. The bandwidth bit period product is 0.5, and the modulation index is 0.5 (between 0.45 and 0.55).

Bluetooth LE uses 1 MHz wide, 40 channels, each separated by 2 MHz, or 2 MHz wide channels or long range (S=2 / S=8), three channels for advertising packets, and 37 channels for data exchange. The channels are numbered from 0 to 39.

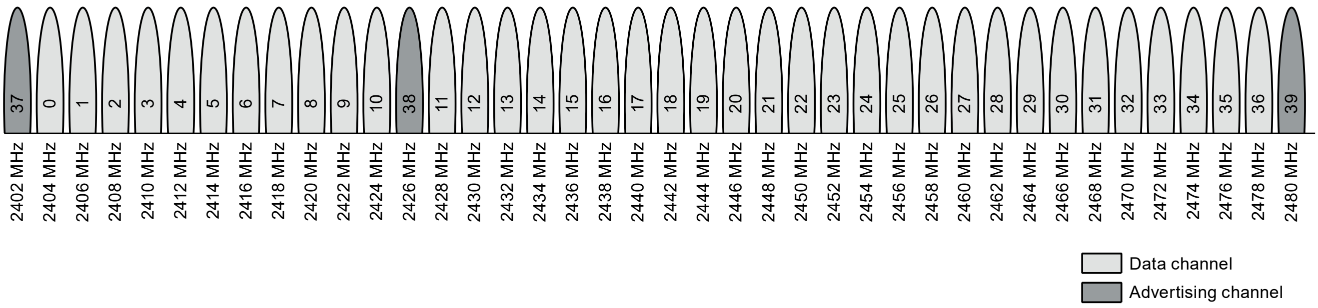

Figure 2. Bluetooth LE radio channels

The low-energy is achieved by having a low-duty cycle of transmission and / or reception of data and by using short advertising and data packets. An asynchronous and connection-less Link-Layer ensures low latency and fast transactions.

At the Generic Access Profile (GAP) layer level, the roles that Bluetooth LE devices may have are GAP central and GAP peripheral. For more details, see Figure 3.

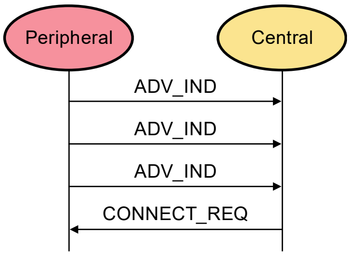

Figure 3. GAP central and GAP peripheral

The peripheral starts sending advertising data to the central. If central is willing to establish a connection with the peripheral, it sends a connection request to the advertiser. Data exchange starts after the connection is established. For more details, see Figure 4.

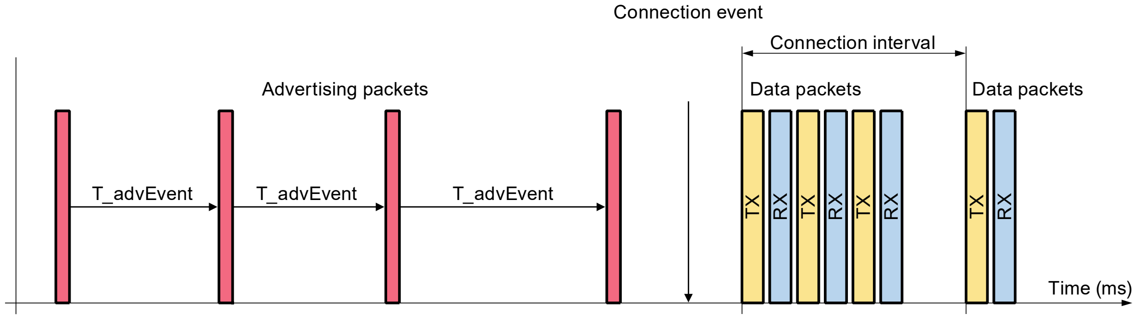

Figure 4. Bluetooth LE advertising and connection events

According to Bluetooth LE specifications, there are four types of advertising packets:

1. `ADV_IND` - Connectable undirected advertising
2. `ADV_DIRECT_IND` - Connectable directed advertising
3. `ADV_NONCONN_IND` - Non-connectable undirected advertising
4. `ADV_SCAN_IND` - Scannable undirected advertising (also known as `ADV_DISCOVER_IND`)

All the above types advertising packets except the non-connectable advertising packets are using a TX followed by an RX sequence, as shown in Figure 5. It is since after sending the advertising packet, the device is waiting for a Scan request or Connect request from a peer device, if any.

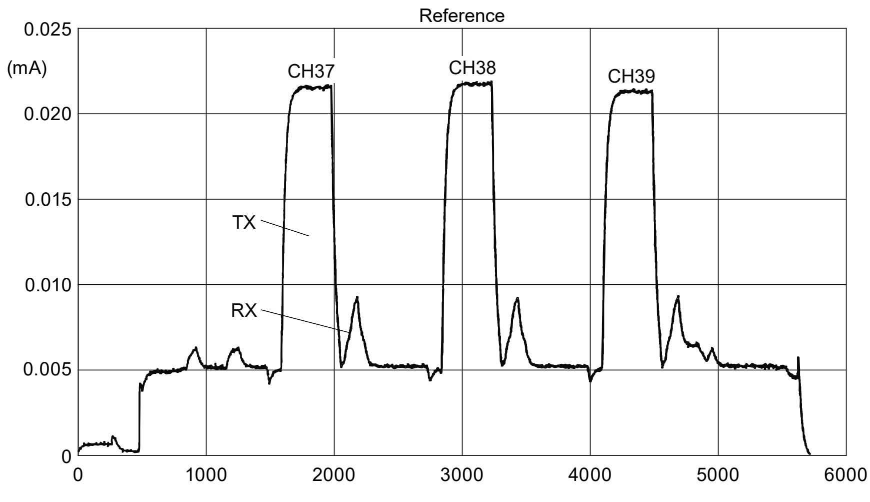

Figure 5. Current consumption vs. time in ADV phase for a Bluetooth LE peripheral device

The current variation with the time when system is in a typical advertising event is shown in Figure 5. All three advertising channels are used. For each channel, a TX operation followed by an RX operation is performed.

Another feature of Bluetooth LE is that the advertising events have a random temporal component, according to Bluetooth LE specifications. For more details, see Figure 6.

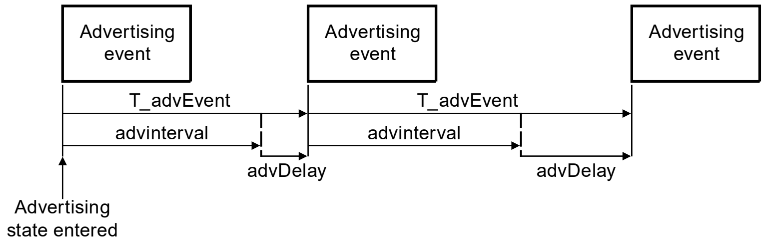

Figure 6. Advertising events occurring at unequal intervals

Equation:

$$T\_advEvent = advInterval + advDelay$$

Where:

- `advInterva`: Integer multiple of 0.625 ms, with a range from 20 ms to 10.24 s
- `advDelay`: Pseudo-random value generated by the Link-Layer, with a range from 0 ms to 10 ms

Therefore, a minimum advertising event interval is 20 ms and a maximum interval is 10.25 s.

Bluetooth LE is designed and implemented for ultra-low power battery operated devices, but the actual power consumption of a real Bluetooth LE device strongly depends on:

- Bluetooth LE application profile
- Application duty cycle
- TX power
- Software management of low-power modes
- Board design and layout

4 Kinetis low-power features

MCX W71 is an ultra-low power, highly integrated single-chip devices that enable Bluetooth Low Energy (Bluetooth LE - 1 Msps, 2 Msps, 500 ksps (LR S=2), 125 ksps (LR S=8)) version 5.2 and generic FSK (at 250 kbit/s, 500 kbit/s, 1000 kbit/s, and 2000 kbit/s) RF connectivity for portable, extremely low-power embedded systems (Z version) and automotive (A version). MCX W71 supports up to 24 simultaneous Bluetooth LE connections as either a master, a slave, or any combination. MCX W71 is designed for applications that center on bridging the embedded world to smartphones to enhance the human interface experience, share-embedded data with the cloud, or enable wireless firmware updates.

Leading the automotive applications is the digital key, where the smartphone can be used as an alternative to the key / smart FOB for unlocking and personalizing the driving experience. But also to provide, select, and authorize access when a key is not needed while sharing your car with others.

MCX W71 integrates a Bluetooth LE 5.2 compliant radio transceiver operating in the 2.4 GHz ISM band supporting a range of generic FSK, an Arm Cortex - M3+, Cortex - M33, up to 1 MB Flash and up to 128 kB SRAM, Bluetooth LE Link-Layer hardware and peripherals optimized to meet the requirements of the target applications. The RF section of MCX W71 is optimized to require very few external components, achieving the smallest RF footprint possible on a printed-circuit board. NXP provides a certified Bluetooth LE stack to support MCX W71.

Extreme long battery life is achieved through the efficiency of code execution in the Cortex - M3+, Cortex - M33 core and the multiple low-power operating modes of the MCX W71. Additionally, an integrated DC-DC converter enables a wide operating range from 1.8 V to 3.6 V in Buck mode. The DC-DC in Buck mode allows MCX W71 to operate from a single coincell battery with a significant reduction of peak RX and TX current consumption. The DC-DC in Buck mode allows a single alkaline battery to be used throughout its entire useful voltage range of 1.8 V to 3.6 V. The integrated `SYS_LDO` regulator operates from 1.71 V to 3.6 V. Radio analog operates from 1.2 V to 3.6 V. Radio PA operates from 1.1 V to 2.4 V.

4.1 MCX W71 hardware support for low-power operation

MCX W71 SoC is designed and built with hardware features that allow the chip to operate in various Low-power modes. The features are as follows:

- Multiple CM33 and NBU power modes, including low leakage with memory retention modes
- Bluetooth LE Link-Layer, Deep sleep mode support
- Peripheral modules clock gating
- Several peripheral Doze modes
- DC-to-DC converter
- Transceiver Sequence Manager (TSM) that assures that transceiver analog and digital blocks are not consuming power when no RX / TX sequence is in progress
- Dedicated Power Management Controller (PMC)
- Low-power peripherals (LPTMR, LPUART) that can be configured as wake-up sources to exit a particular low-power state

The software is responsible for configuring all the hardware to achieve the best power scheme required by the applications. As is presented in the following chapters, the chip Low-power modes are combinations of CM33 and LL / Packet processor Deep-sleep modes. The clock gating of peripherals as well as GPIO states before entering Low-power mode, are in charge of the application developer. The connectivity software package provides callbacks that are called before entering Low-power mode and after exiting Low-power mode. The system shall enter Low-power mode when the system is in idle, and all the software layers agree on that. The system shall exit from Low-power mode each time a synchronous or asynchronous event is happening and requires to be processed.

4.1.1 CM33 and NBU Power modes

The PMC module provides various power options to allow the user to optimize and personalize the power consumption regarding the level of functionality that the application requests. Based on Arm architecture power modes, there are four power modes defined as:

1. Sleep mode
2. Deep sleep mode
3. Power-down mode
4. Deep Power-down mode

From the software connectivity perspective, all the following modes could be considered linked to the type of application:

- `DEEP SLEEP 1` mode
- `DEEP SLEEP 2` mode
- `POWER DOWN 1` mode
- `DEEP POWER DOWN 1` mode
- `SMART POWER SWITCH 1` mode

For the details about all the listed power modes, see the MCX W71 reference manual.

4.1.2 Link-Layer Power modes

The Bluetooth Link-Layer (BTLL) has the following power modes available:

- IDLE

- RUN
- DSM

For Bluetooth LE, the connectivity software package implements there are thirteen low-power modes are available for the MCX W71 SoC, see Table 3:

Table 3. Low-power modes for Bluetooth LE applications

Deep Sleep mode (As defined in Connectivity framework)	Regulators	RAM retention (packet RAM and System RAM CM33)	Core Main Power domain	Core Wake up power domain	Core RF power domain	Peripheral	NBU and Edge Lock	Clock
Deep Sleep 1	all regulators in Low Power mode	All RAM retained in bare metal	Deep Sleep	Deep Sleep	Deep Sleep	Disabled	Deep Sleep (Disabled)	OSC32K enabled
Deep Sleep 2 (default)	all regulators in Low Power mode	16KB of RAM retained All radio RAM retained	Deep Sleep	Deep Sleep	Deep Sleep	Disabled	Disabled	OSC32K enabled
Power Down 1	all regulators in Low Power mode	16KB of RAM retained, All radio RAM retained	Power down	Power down	Power down	Disabled	Disabled	FRO32K enabled
Deep Power Down 1	LDO_ CORE and DCDC off, LDO_SYS in low power	8KB of RAM retained, No radio RAM retained	Deep Power Down	Deep Power Down	Deep Power Down	Disabled	Disabled	FRO32K enabled
Smart power switch DPD1	All regulators OFF	8kB RAM retained, No radio RAM retained	Deep Power Down	Deep Power Down	Deep Power Down	Disabled	Disabled	FRO16K enabled

Note: *Bluetooth LE is using a common radio transceiver digital block, the Transceiver Sequence Manager (TSM) that is used to sequence on / off the analog regulators and circuits needed for RX / TX operations so that these circuits only consume power during RX / TX.*

See the MCX W71 connectivity framework for more details.

4.1.3 XCVR power modes

The MCX W71 transceiver is coupled with the CM33 and CM3 / NBU. Whenever the CM33 enters Low-power mode, the transceiver analog regulators are powered-off. Depending on the Low-power mode, the digital transceiver logic is power-gated or has its state retained.

4.1.4 DC-to-DC converter

The DC-to-DC module is a Switched Mode Power Supply (SMPS) and has two operational modes:

- Buck: Vin = 1.71 V to 3.6 V

The module is configurable through internal registers to operate in Buck mode: `Vdcdc_in` for input and `DCDC_LX` for DC-to-DC output, with CM33 in RUN mode, where peripherals are disabled.

For the detailed information about DC-to-DC converter, see *MKW4xZ/3xZ/3xA/2xZ DC-DC Power Management* (document AN5025).

4.1.5 GPIO, analog pins, and clock gating

A clock gating mechanism was implemented to reduce power dissipation. For example, whenever a peripheral is not used, it can be turned off using the SCGCx registers in the SIM module. Clock gating applies to each peripheral, including the GPIO module. Pruning the clock to a peripheral assures that the internal peripheral circuitry does not have switch states and, therefore, no power consumption, except for the leakage currents.

CAUTION: *After reset, the clock gating bits are cleared, and this implies that before using any peripheral, the corresponding clock gating bit must be set, otherwise, any access to peripheral registers can cause a hardware fault.*

Note: *To turn off a peripheral clock (gate off), the peripheral must be turned off prior to clock.*

The user application must control and set the state of the GPIO ports before the device goes to sleep as well as after the device exits the low-power state. The connectivity software provides callback functions that are called before the device enters a low-power state and after it wakes up.

Related to the analog pins, the device has several analog blocks that have selectable reference voltages. The main blocks are the 16-bit SAR Analog to Digital Converter (ADC) and Comparator Module (CMP). The board design shall consider the chip analog pins and use them appropriately.

The external analog inputs are typically shared with digital I / O. To improve the performance in the presence of noise, or when the source impedance is high, it is recommended to use capacitors on these inputs. The capacitors shall be placed as close as possible to chip analog pins.

For more details, see the NXP reference designs for MCX W71 and the chip reference manual.

4.2 Software configuration for low-power operation

This section lists the information about software configuration for low-power operation.

4.2.1 Bluetooth Smart application configuration

The Connectivity Software package offers various Bluetooth LE demo projects. The Low-power (LP) project is used to perform the current profile measurements. This project is available at the following relative path (PRC2 RC2 August 2022):

```
<installation_path><SDK revision>\boards\FRDMMCXW71\wireless_examples\reference_
design\bluetooth\lp\bm\iar
```

Or

```
<installation_path><SDK revision>\boards\FRDMMCXW71\wireless_examples\reference_
design\bluetooth\lp\bm\iar
```

To set the device for advertising and connect current measurements, the MCX W71 SDK includes the Low Power (LP) in the Reference Design application folder (based on a temperature sensor in Low-power mode). It requires some changes to allow the application to enter and leave Low-power mode. BareMetal or FreeRTOS versions of the application are used.

Foe more information, see the MCX W71 low-power connectivity design user guide to set a different low-power mode. This document is located in the SDK set of documents.

Different built are described in section Section 4.2.1.1 to set the FRDM-MCX W71 in different states:

Low-power application:

- Advertising and connection events: (default software setting at +10 dBm)
  - MCX Deep Sleep mode 2, All RAM retained, NBU Deep Sleep mode, RF output power = +10 dBm (default)
- Deep sleep mode 2 (DSM2)

The FRDM MCX W71 board is used to perform the current consumption. It is programmed with the Low-power binary (advertising event and connect events).

4.2.1.1 Preparing software

See the "Low Power Connectivity Design User's Guide.pdf" document to set all the different modes measured in this report. This document is available in the SDK document package use MCXXpresso SDK Builder to download. For more details, see Table 4.

Table 4. Deep sleep modes available in the SDK software

Deep-sleep mode	Regul.	RAM retention	Core main power domain	Core wake-up power domain	Core RF power domain	Peripherals	NBU and Edge Lock	Clock
Deep Sleep 2	All regulators in Low-power mode	16 KB of RAM retained All radio RAM retained	Deep sleep	Deep sleep	Deep sleep	Disabled	Deep sleep (disabled)	OSC32K (enabled)

5 Power measurements and timing analysis

This section lists the details about the following bullet points:

- Setup test environment and DUT
- Measuring the current consumption
- Advertising extension
- Scan extension
- Channel selection algorithm #1 and #2
- High-duty cycle advertising
- Reports

5.1 Setting up test environment and DUT

This section explains how to set up the testing environment, what hardware tools and boards are needed, and all the steps that must be taken prior to taking measurements.

All the measurements are performed using Keysight:

- Power analyzer: CX3322A
- Current probe: CX1101A

For more details, see Figure 7.

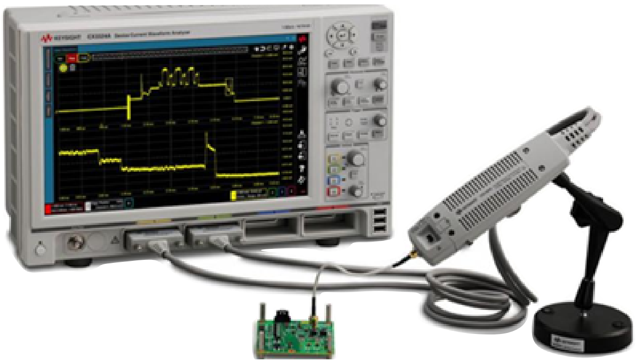

Figure 7. Keysight CX3322A power analyzer and CX1101A current probe

An external source powers the FRDM-MCX W71 board, and the power analyzer module 1 is used as an ampere meter. The power source was programmed to deliver 3.6 V DC. One pair of premium cables is needed to supply the board, while the other is needed to measure current. To prevent unintended spikes, power losses, or board resets, the connections between the power analyzer and the FRDM board must be flawless. For more details, see Figure 8 and Figure 9.

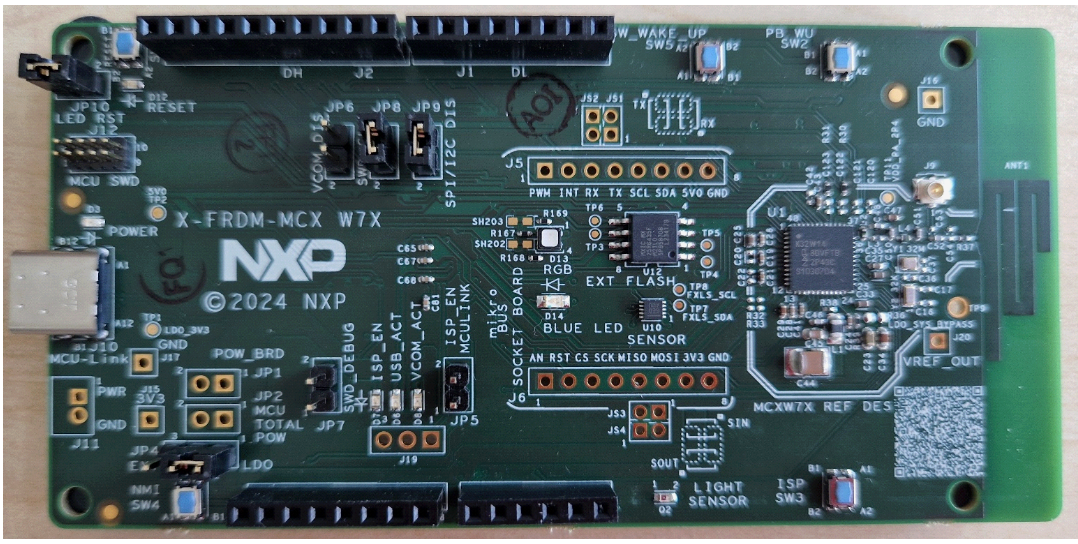

Figure 8. FRDM-MCX W71 board - TOP

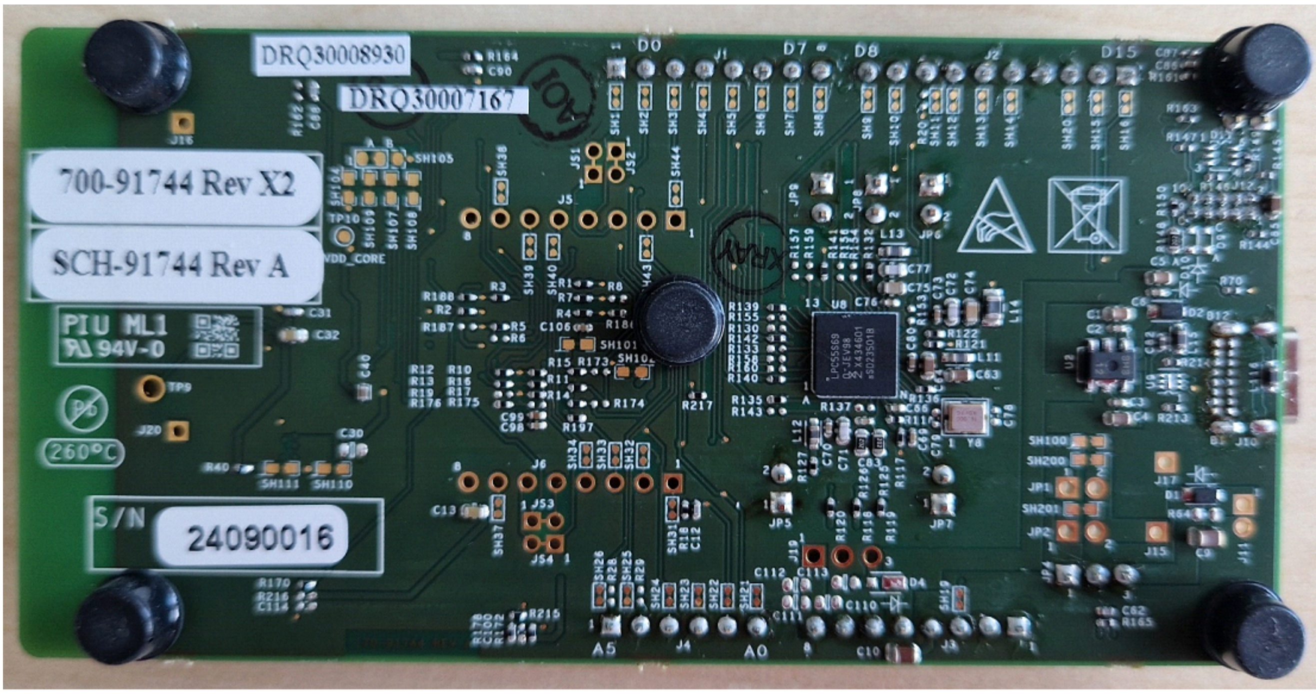

Figure 9. FRDM-MCX W71 board - BOTTOM

The current measurements are performed in the Buck modes using the FRDM-MCX W71 board.

For more details, see Table 5, Figure 10, and Figure 11.

Table 5. Header power consumption access points

Current names	Header number	Shunt
Ireg	JP2:1-2	SH201
Idd_LDO_CORE	-	SH110
Idd_RF	-	SH111
Idd_ANA	-	SH109
Idd_dcdc/Idd_IO_D	-	SH107
Idd_IO_ABC	-	SH108
Idd_Switch	-	SH105-B (cut SH105-A)

Note: `Ireg` = `Idd_LDO_Core` + `Idd_RF + Idd_ANA` + `Idd_dcdc` + `Idd_IO_ABC` + `Idd_Switch`

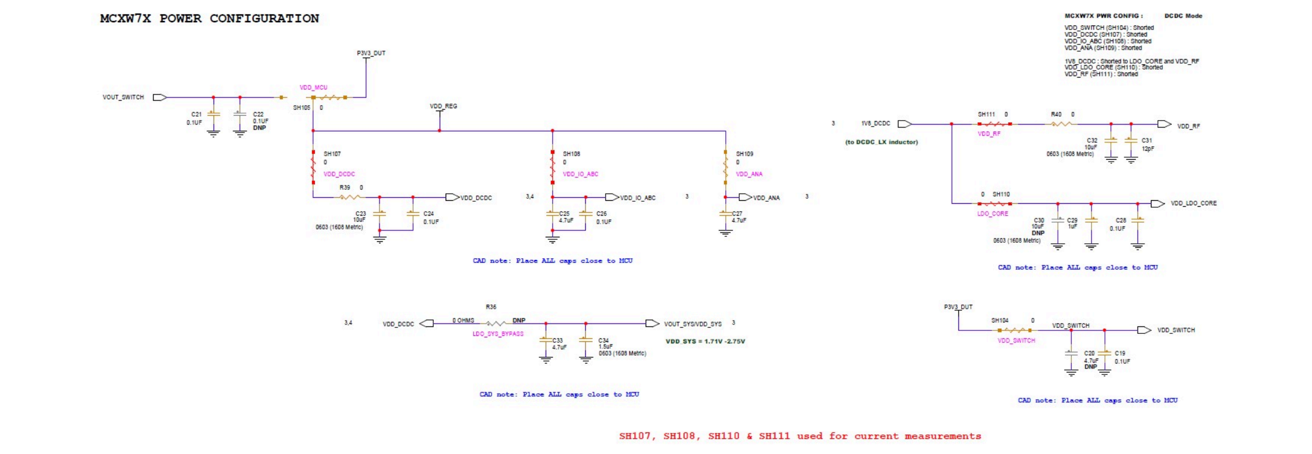

Figure 10. FRDM schematic, current header positions

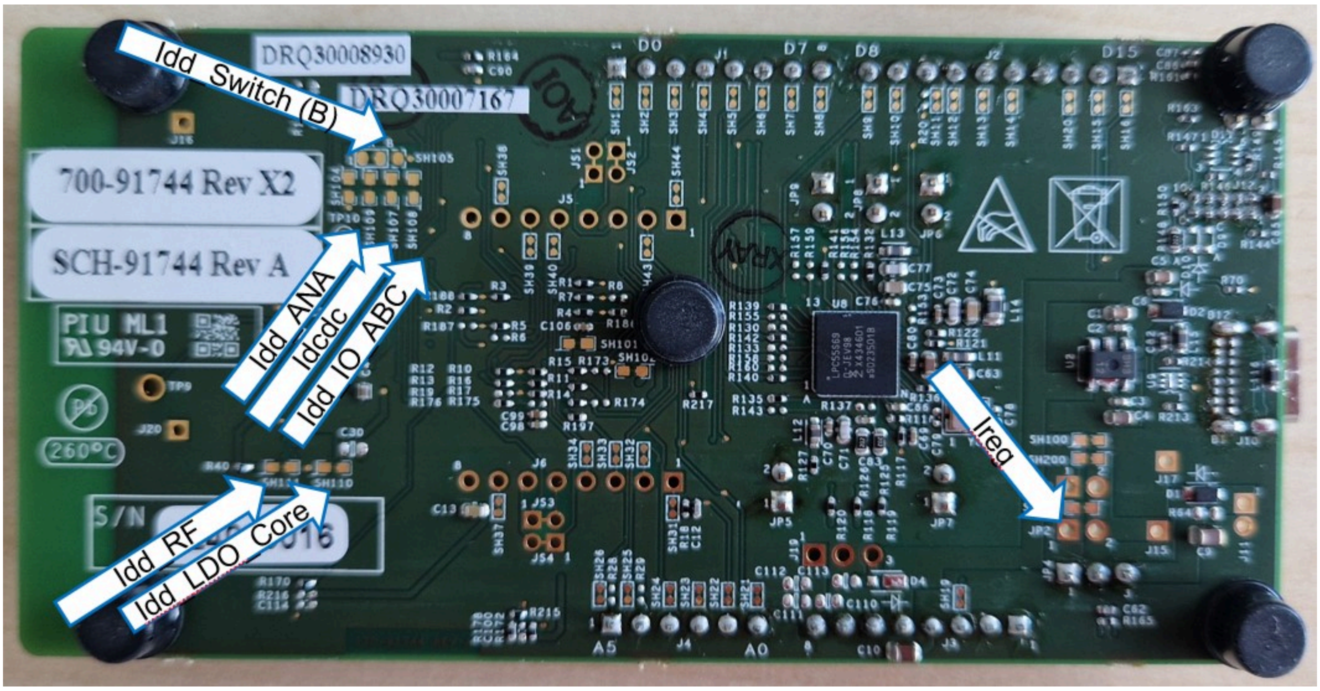

Figure 11. FRDM-MCX W71 board, current shunt – Bottom view

5.1.1 Preparing hardware

The FRDM is not configured to avoid peak of current below at each BLE event startup. To do this set up, a ferrite bead (BLM15HD182SN1) and a 3.3 ohm serial resistor are attached to the Vbat wire. Both the `Vdd_dcdc` (effective in Buck mode) and the `Vdd_RF` are connected to 3.3 ohm serial resistors, see Figure 12.

These components smooth the current peaks but the general consumption also. That means the shape of the `Ibat` current consumption is not sharp. In case you want to analyze the different steps of the current consumption, you could remove these four components.

In this application note, the measurements and current consumption are done without the serial resistors on advertising, and also in connect events and scan events.

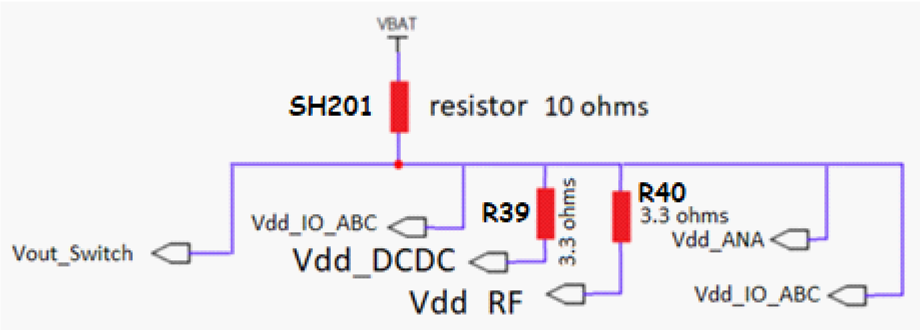

Figure 12. Serial resistors to limit the peak of current

Figure 13 and Figure 14 shows the Ibat waveforms during an advertising event with and without the serial components:

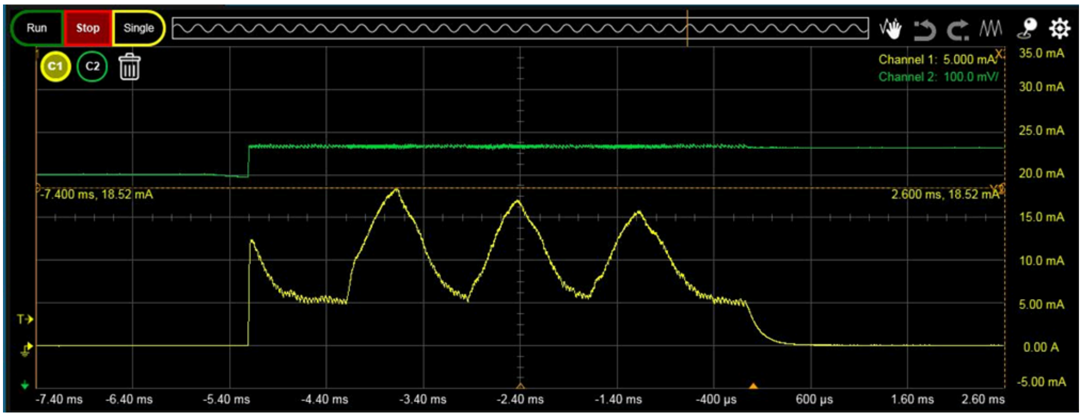

Figure 13. `Ibat` **(yellow curve) during advertising event using serial components (default hardware setting)**

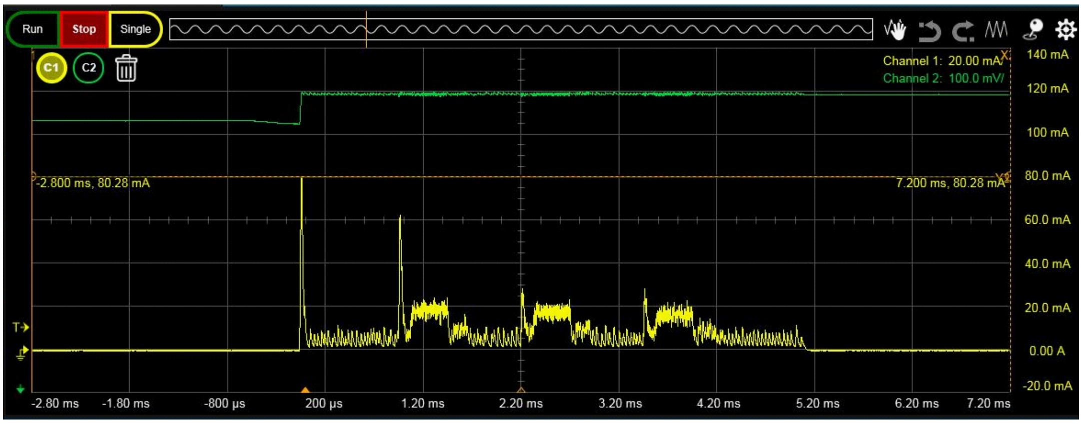

Figure 14. `Ibat` **(yellow curve) during advertising event removing serial components (hardware setting used for the current analysis)**

5.1.2 Current measurement

The FRDM MCX W71 is configured in the buck mode. The whole current consumption is measured in this mode. The DCDC bypass mode is not available in the FRDM MCX W71 board.

5.1.3 `Ireg` current measurement example

Follow the steps as listed to measure the `Ireg` current:

1. Cut the `SH201` shunt.
2. Solder a 2x1 header on `JP2` (MCX TOTAL POW silkscreen).
3. Connect the current probe to `JP2:1-23` to measure the global power consumption (`Ireg`) of the MCX W71.
4. Supply the FRDM-MCX W71 board through the USB type-C connector (`J10`).

For more details, see Figure 15.

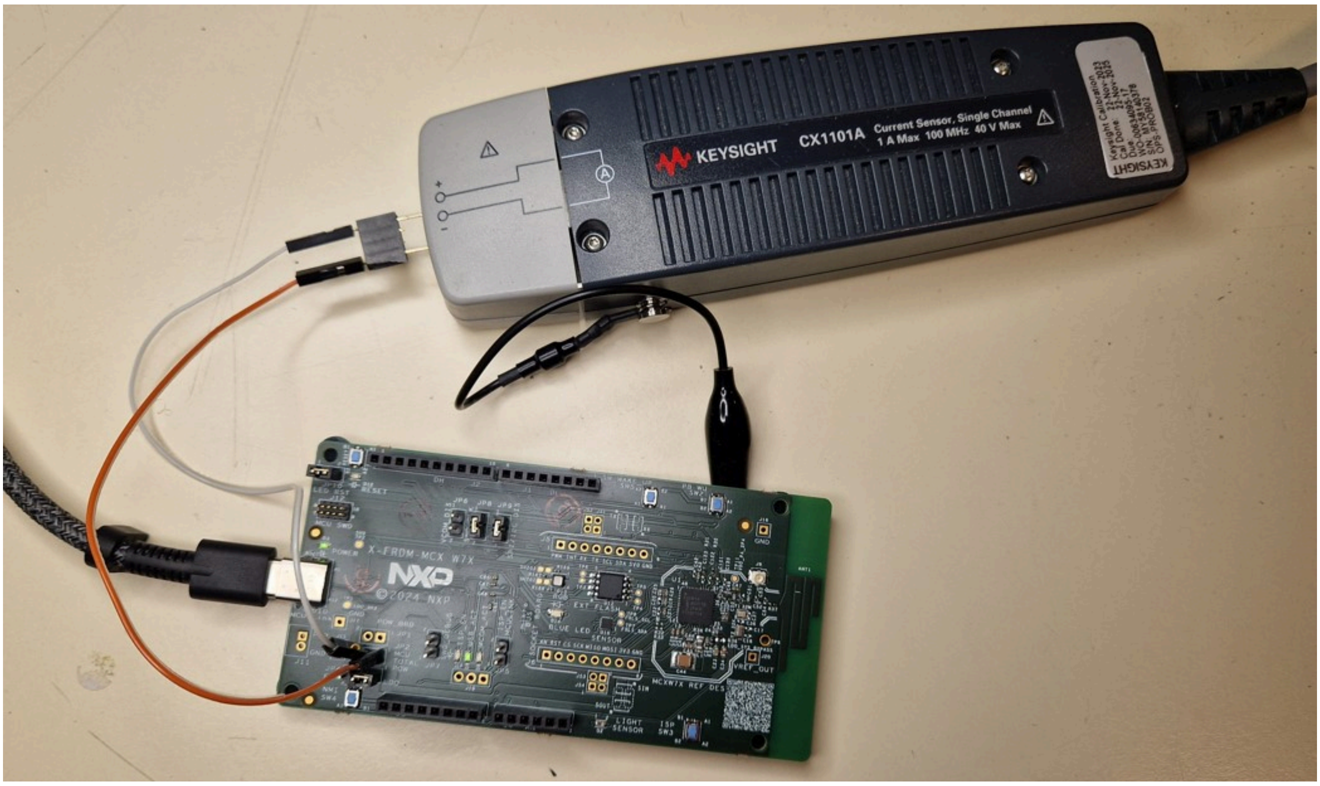

Figure 15. FRDM-MCX W71 board, current probe connected to JP2:1-2 example

If the board has SMA connector, C4 capacitor is populated and C3 not populated, then a SMA antenna is required to be connected to the board, for more details Figure 16.

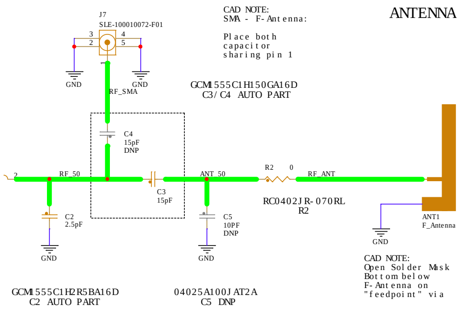

Figure 16. SMA configuration

5.2 Measuring current consumption

This section gives the information to set up the hardware and software to measure current consumption using the FRDM-MCX W71 board.

5.2.1 Instruction

Follow the instruction as listed to measure the current consumption:

1. Choose the Buck mode. See Section 5.2.2.3.1.
2. Connect the board to a PC and download the `LP_peripheral` (advertising or connect) or `LP_master` (scan) project created as in Section 4.2 to the board.
3. Set the output voltage of the external power source to 3.6 V.
   CAUTION: *Voltage range must be within 1.71 V and 3.6 V.*
4. Connect `J16` (GND) to the power source, see Figure 17.
   CAUTION: *Ensure that the power source is disabled while connecting the power connector to the board to avoid any damage.*
5. Connect the Keysight CX3322A power analyzer and CX1101A current probe to `JP5-3` and to the power source, Figure 17.
   For more details related to connections, see Figure 18.

Figure 17. JP5-3, GND TP18

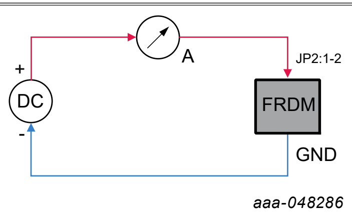

Figure 18. Connection block diagram

6. Switch ON the external power supply.

The current measurement is performed by using the power analyzer built-in display and a USB flash memory stick to save the results.

5.2.2 Measurements and results

All the measurements within the following subsection are done with:

- CM33 in Deep Sleep mode
- Flash in Doze mode, RF output at +10 dBm (10 mW), see file `app_preinclude.h`, at `../Connectivitiy_test_bm/source/`).
- Power supplies at 3.6 V
- Room temperature at 25 °C)

MCX W71 device is coming from a typical process. All the measurement and results are listed in the following subsections. For summary results, see Section 5.7.

Note: *How to use the power analyzer is not explained in this document.*

5.2.2.1 Overview

This section gives an overview of a 20 seconds sequence after a power-up `LP_peripheral` application. For more details, see Figure 19.

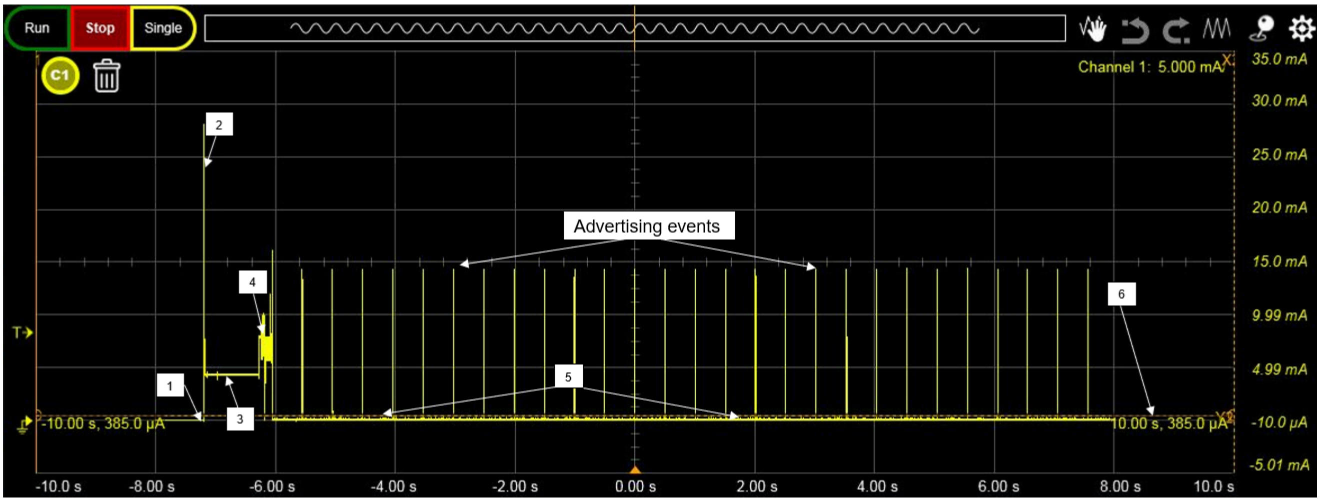

Figure 19. MCX W71 SoC current consumption sequence

Figure 19 shows the current consumption of the MCX W71 SoC during different operational phases:

Table 6. Different operational phase current consumption

Phase	Description
1	Power-on reset (POR), just after the SoC is connected to power supply. The spike from the figure is about 26 mA and is because of the coupling capacitors as well as the SoC internal circuitry (regulators, clock oscillators, MCX, radio digital, radio analog, and so on).
2	MCX is initialized among all the software: low-level drivers, framework, RTOS, Bluetooth LE stack, application
3	MCX running
4	The MCX leaves Deep Sleep mode 2 and resumes its execution. The Bluetooth LE Link-Layer goes to RUN state
5	Between advertising events, the system enters in Deep Sleep mode 2
6	After a disconnect, the SoC enters in Deep Sleep mode 2

5.2.2.2 Deep sleep modes

When the SoC is connected to the power supply, a power-up spike occurs due to coupling of the board to power supply. After MCX POR:

- Software execution begins
- Clocks and peripherals are enabled and configured
- Connectivity Framework is initialized
- Real-time operating systems (RTOS) tasks are initialized and started
- Bluetooth LE stack is up and running
- Bluetooth LE application is started

Once all these steps are completed, the system could enters in a different Deep Sleep mode. The default Deep Sleep mode is the `Deep Sleep mode 2` (sorted the list from lowest to highest current consumption). For more details, see Section 4.1.

The initialization phase before the system enters Deep Sleep mode, it takes several milliseconds depending of the Deep Sleep mode chosen.

For the different use cases, the device operates directly in `Deep Sleep mode x`.

5.2.2.3 Power-On reset

The FRDM-MCX W71 board is set in the Buck mode configuration by default.

The binary file setting used is: Buck mode, `Deep Sleep mode 2` for both CM33 and CM3 / NBU with 48 MHz clock mode, automatic start advertising.

The very first POR timing is 900 ms from power-up to first TX advertising. For more details, see Figure 20 and Table 7.

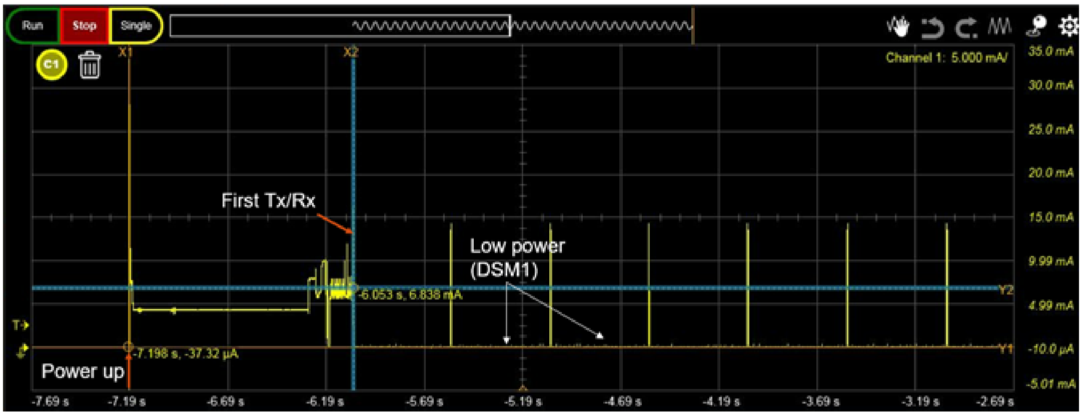

Figure 20. FRDM-MCX W71 SoC first POR timing

Table 7. POR timing at 900 ms

Type of wake-up	Timing (ms) (HW + SW initialization)
POR	900

The other reset (button pressed / software reset) timings are 108 ms from power-up to first TX advertising, see Figure 21 and Table 8.

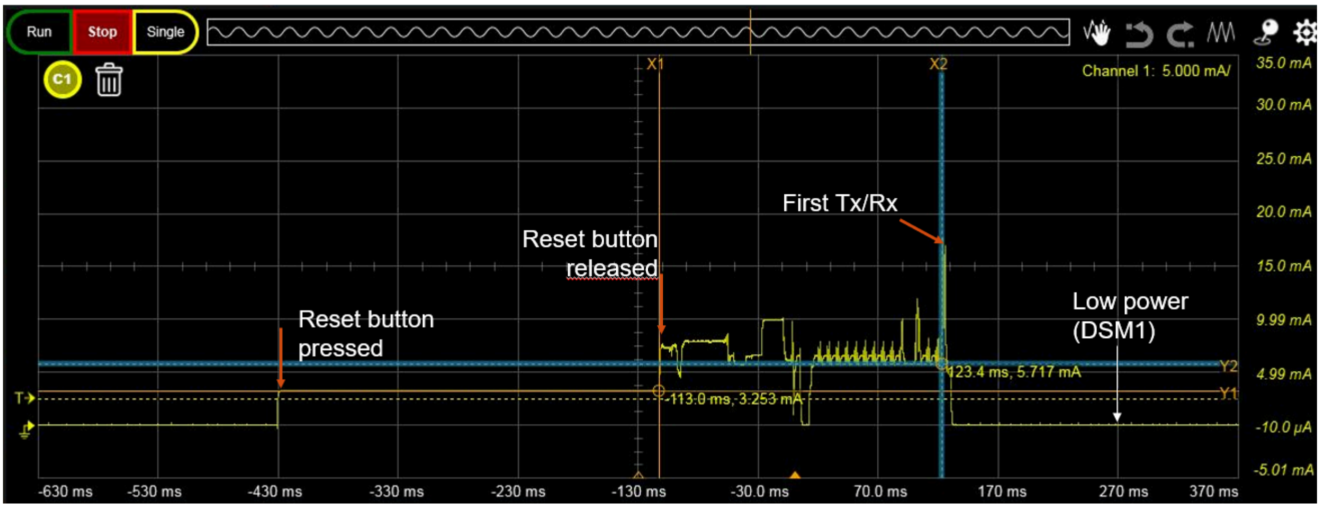

Figure 21. SoC reset timing

Table 8. Reset timings at 108 ms

Type of wake-up	Timing (ms) (HW + SW initialization)	Power consumption (mA) (HW + SW initialization)
First Reset (POR)	900	4.8
Other reset	108	7.65

5.2.2.3.1 Buck mode

In the Buck mode, the `Deep Sleep mode 2` is used, where the FRDM jumpers are in buck configuration.

The device enters in `Deep Sleep mode 2` automatically after power-up. The device enters in Advertising mode when the SW1 button is pressed. For more details, see, Figure 22 and Table 9.

The binary file setting used as in Buck mode: `lp_MCXW71_buck.srec`, advertising period 500 ms with payload and connectable.

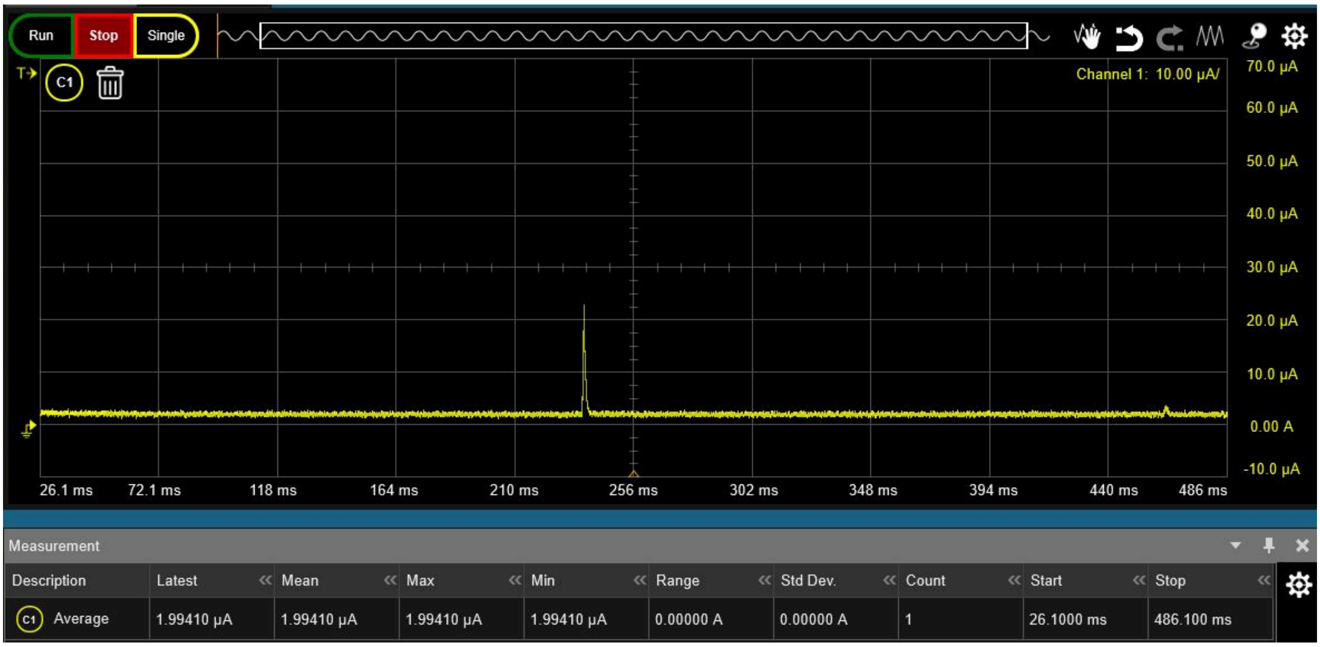

Figure 22. `Deep Sleep mode 2` - Buck mode

Table 9. `Deep Sleep mode 2` current consumption between events in Buck mode

Measured current			
DCDC_IN=3.0 V	**Avg**	**Max**	**Min**
DCDC_IN=3.0 V	1.99 µA	1.72 µA	2.49 µA

The low-power current consumption is measured at 1.99 µA @ 3.0 V between advertising events.

For the Low-power summary, see Table 10, Figure 23, and Table 11.

Table 10. `Deep Sleep mode 2` current consumption between events in Buck mode

Deep sleep mode	Regul.	RAM retention	Core Main Power domain	Core Wake up power domain	Core RF power domain	Peripherals	DC-to-DC	Current consumption at 3 V
Deep sleep 2	all are in Low-power mode	16 k RAM retained	Deep sleep	Deep sleep	Deep sleep	Disabled	Buck	1.99 µA

Note: *DC-to-DC peak information in Buck mode, the DC-to-DC peaks occur every 500 ms. The nominal DC-to-DC peak is represented in the below figure. Nominal DC-to-DC peak timing is around 500 us for advertising period of 500 ms.*

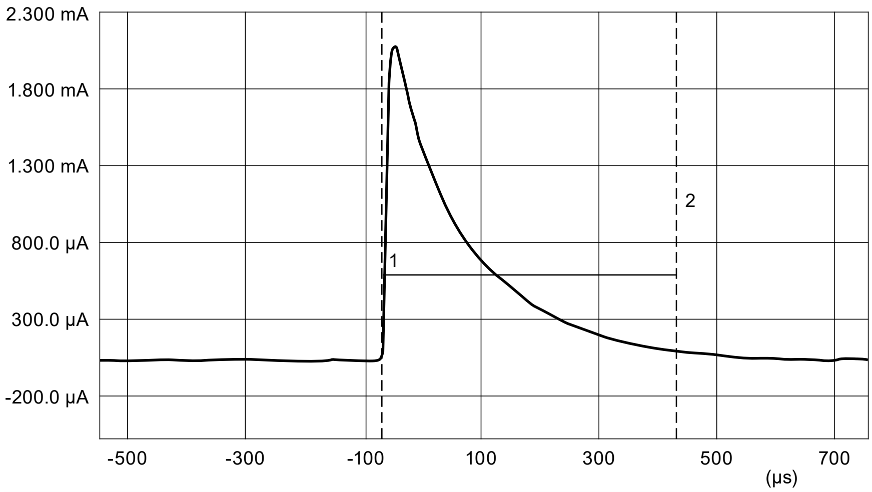

Figure 23. Nominal DC-to-DC peak - Buck mode

Table 11. DC-to-DC peak consumption between advertising events - Buck mode

Buck mode	Idd_REG (total consumption)		
State	Time (ms)	Current (µA)	mA x mS
DC-to-DC peak Consumption	0.500	614	0.307 mA-mS
Charge Integral: 85.27 pAh			

5.2.2.4 Advertising mode

An advertising event is where the Bluetooth LE peripheral device broadcasts some information in order to either share it or become connected to a Bluetooth LE central device, such as a smartphone. The device wakes-up and broadcasts packets on three separate channels and listens on each of these channels for scan requests or connection requests.

Figure 24 and Table 12 shows the current consumption during the advertising event using data rate at 1 Mbit/s and without serial components (setting for coin cells to avoid peak of current).

The binary file settings used are:

- 48 MHz clock
- Advertising with X bytes TX payload, Y bytes RX payload and connectable
- RF output +10 dBm, 1 Mbit/s

Buck mode: Wake-up from Low-power mode `Deep sleep mode 2`

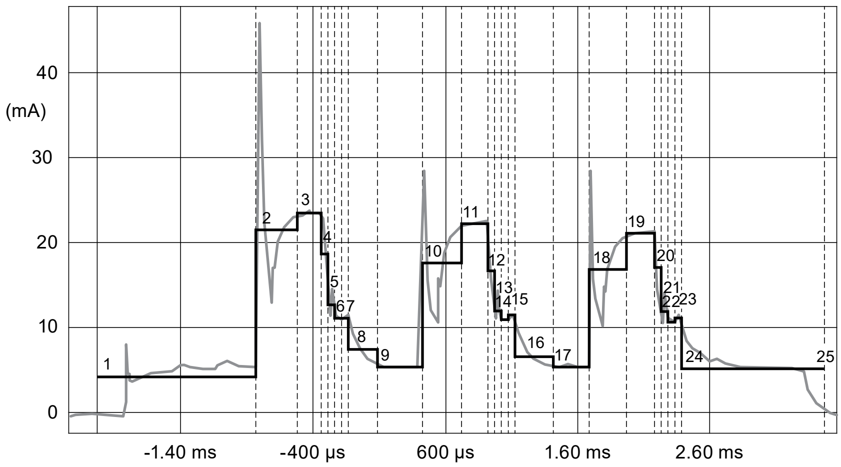

Figure 24. Current consumption - advertising event period

Table 12. Advertising event

No.	ADV event timing
1	Pre-processing
2	TX warm-up
3	Active TX
4	TX warm-down
5	TX to RX transition
6	RX warm-up
7	Active RX
8	RX warm-down
9	MCX stop
10	TX warm-up
11	Active TX
12	TX worm-down
13	TX to RX transition
14	RX warm-up
15	Active RX
16	RX warm-down
17	MCX stop
18	TX warm-up
19	Active TX
20	TX warm-down
21	TX to RX transition
22	RX warm-up
23	Active RX
24	RX warm-down
25	Post-processing

Test environment: Advertising

Table 13. Test environment

DC-to-DC mode	Buck
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V
RF output power	+0 dBm
MCX clock mode	48 MHz
RAM size	128k
Data rate	1 Mbit/s
Payload	Tx:31 bytes; Rx:0 Byte
Connectable	Yes
Flash	Doze
CM33	Deep Sleep mode 2
Setting	Advertise from low-power DSM2 Slave to Master
Software	LP_Peripheral (2.15.2 MR2 release)

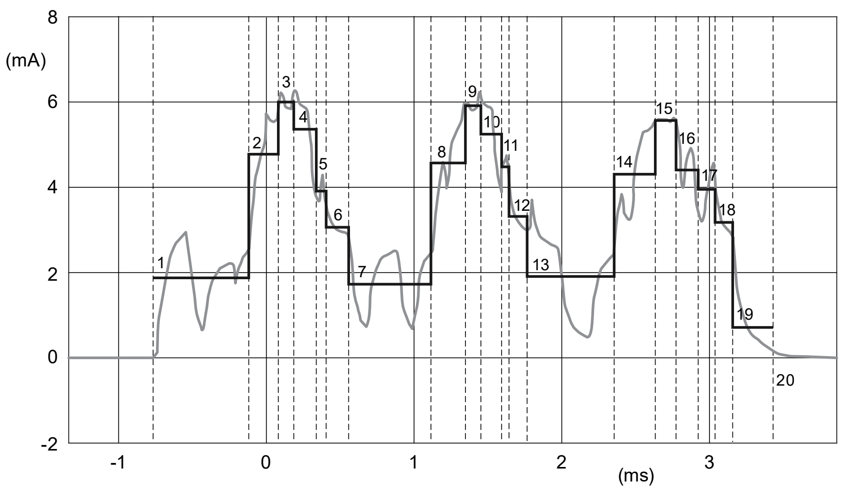

Figure 25. Advertising current profile event after `DSM2` mode, Buck mode

Table 14. Advertising current profile event after `DSM2` mode, Buck mode

Buck mode	`Idd_REG` (total consumption)			Spread: +/- 3sigma
State	Time (ms)	Current (mA)	mA x mS	-
Pre-Processing	0.650 ms	2.900 mA	1.885 mA-ms	+/-0.04 mA
TX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms	-
TX1 Level	0.328 ms	6.860 mA	2.250 mA-ms	+/-0.04 mA
TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms	-
TX1 to RX1 Transition	0.050 ms	6.840 mA	0.342 mA-ms	-
RX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms	-
RX1 Level	0.080 ms	6.948 mA	0.556 mA-ms	+/-0.08 mA

Table 14. Advertising current profile event after DSM2 mode, Buck mode*...continued*

Buck mode	Idd_REG (total consumption)			Spread: +/- 3sigma
State	**Time (ms)**	**Current (mA)**	**mA x mS**	**-**
RX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms	-
MCX Stop	0.280 ms	1.800 mA	0.503 mA-ms	-
TX2 Rise	0.080 ms	6.840 mA	0.547 mA-ms	-
TX2 Level	0.328	6.860 mA	2.250 mA-ms	+/-0.04 mA
TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms	-
TX1 to RX1 Transition	0.050 ms	6.840 mA	0.342 mA-ms	-
RX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms	-
RX2 Level	0.080 ms	6.948 mA	0.556 mA-ms	+/-0.08 mA
RX2 Fall	0.020 ms	6.840 mA	0.137 mA-ms	-
MCX Stop	0.280 ms	1.800 mA	0.503 mA-ms	-
TX3 Rise	0.080 ms	6.840 mA	0.547 mA-ms	-
TX3 Level	0.328 ms	6.860 mA	2.250 mA-ms	+/-0.05 mA
TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms	-
TX1 to RX1 Transition	0.050 ms	6.840 mA	0.342 mA-ms	-
RX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms	-
RX3 Level	0.080 ms	6.948 mA	0.556 mA-ms	+/-0.07 mA
RX3 Fall	0.020 ms	6.840 mA	0.137 mA-ms	-
Post-Processing	0.275 ms	2.750 mA	0.756 mA-ms	-
Active Consumption	3.458 ms	4.973 mA	**17.195 mA-ms**	+/-0.05 mA
Charge Integral: 4.78 nAh				

Advertising connectable vs non-connectable comparison:

Table 15. Test environment

DC-to DC mode	Buck	
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	
RF output power	+0 dBm	
MCX clock mode	48 MHz	
RAM size	128k	
Data rate	1 Mbit/s	
Payload	Tx:31 bytes; Rx:0 Byte	
Connectable	Yes	
Flash:	Doze	
CM33:	Deep Sleep mode 2	
Setting:	Advertise from low-power DSM2	

Table 15. Test environment*...continued*

DC-to DC mode	Buck	
	Slave to Master	
Software:	LP_Peripheral (2.15.2 MR2 release)	

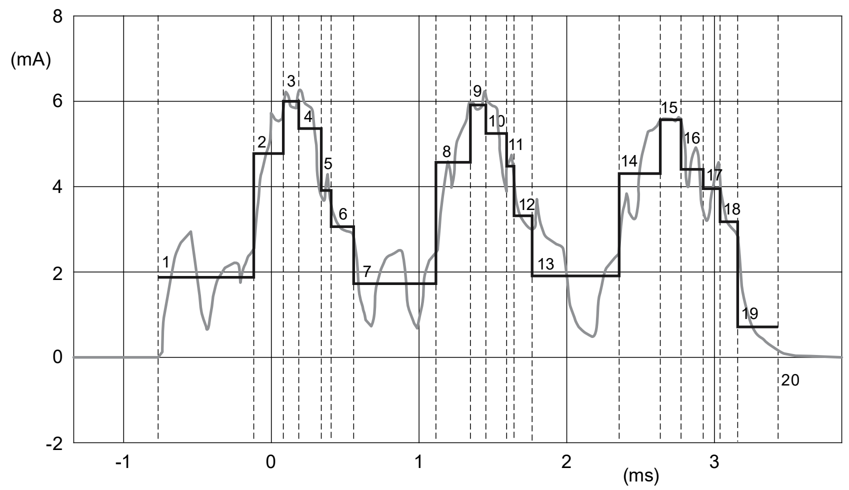

Figure 26. Advertising current profile event after DSM2 mode, buck mode, non connectable

Table 16. Advertising current profile event after DSM2 mode, buck mode, non connectable

	Buck mode	**Idd_REG (total consumption)**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
ADVERTISING non-connectable	Pre-Processing	0.650 ms	2.900 mA	1.885 mA-ms
	TX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms
	TX1 Level	0.328 ms	6.860 mA	2.250 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms
	MCX Stop	0.510 ms	1.800 mA	0.917 mA-ms
	TX2 Rise	0.080 ms	6.840 mA	0.547 mA-ms
	TX2 Level	0.328 ms	6.860 mA	2.250 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms
	MCX Stop	0.510 ms	1.800 mA	0.917 mA-ms
	TX3 Rise	0.080 ms	6.840 mA	0.547 mA-ms
	TX3 Level	0.328 ms	6.860 mA	2.250 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms
	Post-Processing	0.275 ms	2.750 mA	0.756 mA-ms
	Active Consumption	3.228 ms	5.452 mA	13.278 mA-ms
	Charge Integral: 3.69 nAh			

Advertising connectable power consumption is equal to 4.97 mA during 3.46 ms (4.78 nAh) in buck mode.

Advertising non connectable power consumption is equal to 5.45 mA during 3.23 ms (3.69 nAh) in buck mode.

Table 17. Connectable vs non connectable advertising comparison, buck mode

DC-to-DC mode	connectable	Duration event (ms)	Power consumption (mA)	Total power (nAh)
Buck	No	3.228 ms	5.452 mA	3.69 nAh
Buck	Yes	3.458 ms	4.973 mA	4.78 nAh

Summary:

Table 18. Detailed current profile during advertising event

48 MHz clock using 32KHx Crystal	Buck mode Vdd_dcdc=3 V, Vdd_RF=Vdd_LDO_Core=1.25 V	
	DSM2	
	T= 25 °C	
Advertising consumption on 1 event at +0 dBm	3.458 ms	
	4.973 mA	
	4.78 nAh	
Advertising consumption details at +0 dBm		
TX Active (+0 dBm) – MCX STOP	5.060 mA	
RX Active - MCX STOP	5.148 mA	
TX Warm-up - MCX STOP	5.040 mA	
TX Warm-down - MCX STOP	5.040 mA	
RX warm-up - MCX STOP	5.040 mA	
RX warm-down - MCX STOP	5.040 mA	
TX to RX transition - MCX STOP (Advertising event)	5.040 mA	

Table 19. Pre and post-processing timing during advertising

48 MHz clock using 32KHx Crystal	Buck mode Vdd_dcdc=3 V, Vdd_RF=Vdd_LDO_Core=1.25 V
	DSM2
	T= 25 °C
ADV Pre-processing Time	0.650 ms
ADV Postprocessing Time	0.275 ms

Table 20. Pre and post-processing and MCX consumption during advertising

48 MHz clock using 32KHx Crystal	Buck mode Vdd_dcdc=3 V, Vdd_RF=Vdd_LDO_Core=1.25 V
	DSM2
	T= 25 °C
ADV pre-processing	2.900 mA
Radio Post-processing	2.750 mA
MCX STOP	1.800 mA

Table 21. Advertising current consumption event

Advertising	Duration (ms)	power consumption (mA)	Energy (nAh)
Buck mode Vdd_dcdc=3 V, Vdd_RF=Vdd_LDO_Core=1.25 V	3.458 ms	4.973 mA	4.78 nAh

Table 22. Global summary current consumption event versus main voltage

Advertising	1.71 V	1.8 V	2.1 V	2.4 V	2.7 V	3 V	3.3 V	3.6 V	Unit
buck mode	4.10	4.24	4.53	4.82	4.60	4.21	3.91	3.56	nAh

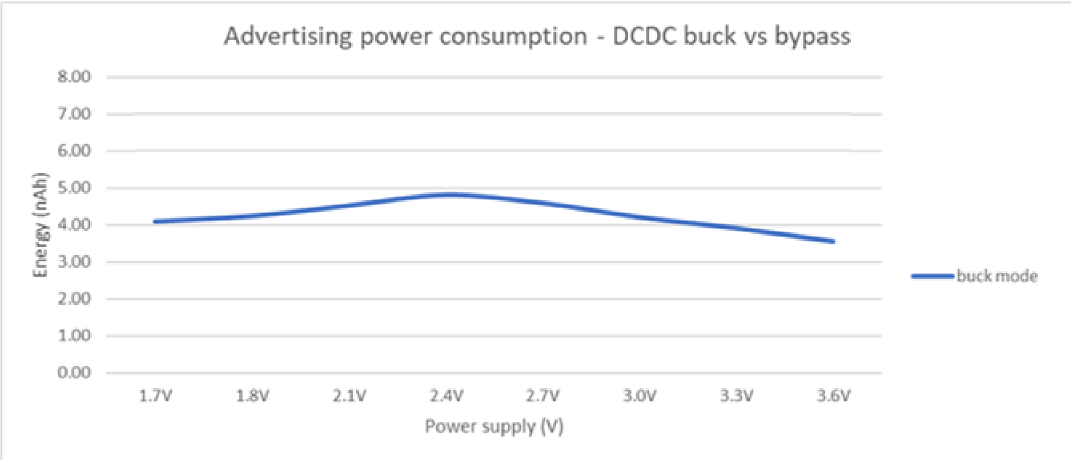

Figure 27. Global Advertising event power consumption profile in buck mode, DSM2 vs main power supply

Table 23. Buck mode, summary current consumption event versus main voltage and temperature

Advertising buck	1.7 V	1.8 V	2.1 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	
-40°C	3.97	4.15	4.48	4.67	4.50	4.13	3.84	3.48	nAh
-20°C	4.03	4.21	4.52	4.73	4.56	4.17	3.88	3.52	nAh
25°C	4.10	4.24	4.53	4.82	4.60	4.21	3.91	3.56	nAh
65°C	4.30	4.75	5.00	5.28	5.02	4.66	4.26	3.96	nAh
85°C	4.94	5.40	5.62	6.04	5.60	5.16	4.74	4.16	nAh
105°C	5.84	6.19	6.54	7.02	6.62	6.07	5.58	5.05	nAh
120°C	6.25	6.76	7.46	7.99	7.65	6.98	6.42	5.94	nAh

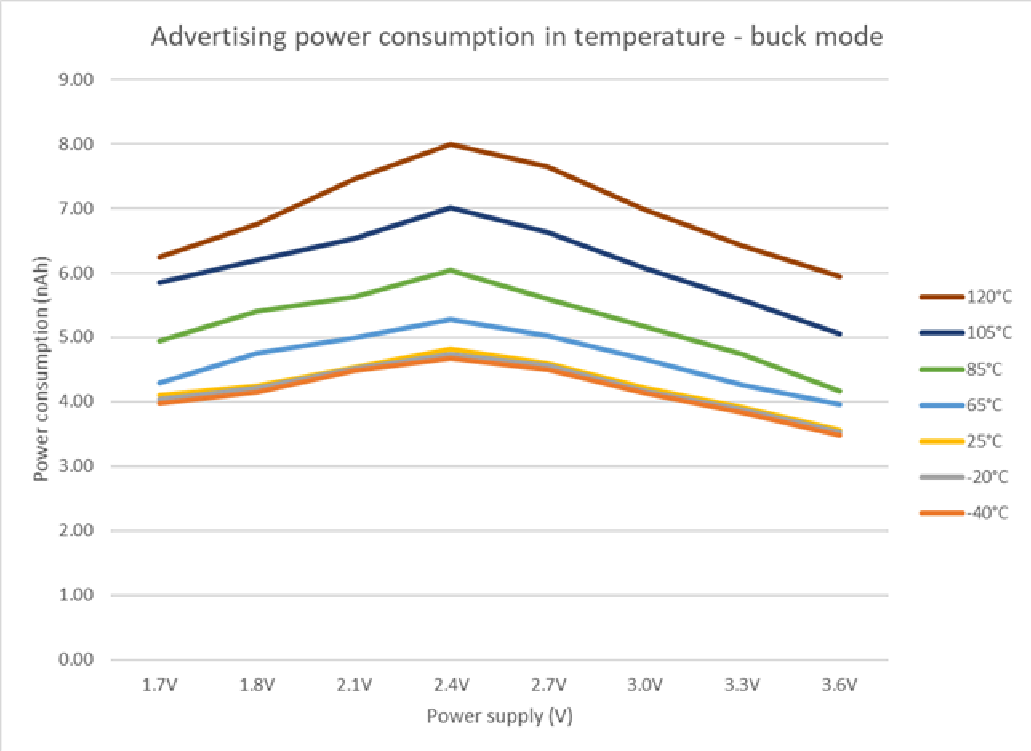

Figure 28. Global Advertising event power consumption profile in buck mode vs voltage and temperature, DSM2 vs main power supply

5.2.2.5 Connection mode

NXP android app is used to perform connection, see Figure 29.

Figure 29. IoT Toolbox

On the central side (in this case, a smartphone or a tablet with Bluetooth LE 5.x available), the following application must be installed: IoT Toolbox, available on the Google play store and Apple iTunes (IoT toolbox version 5.0.9 minimum).

The Thermometer application must be used. For measuring advertising events, there is no need for a connecting device, but for measuring connection events, it is mandatory. To connect to the FRDM-MCX W71 board, the procedure is simple and straightforward:

- Open IoT Toolbox
- Power-up FRDM-MCX W71 board and press `SW1` to start advertising
- On Android application the `FSL_Thermo` must be reported at scan phase
- Connect to `FSL_Thermo` peripheral
- Wait for measurements

Templates:

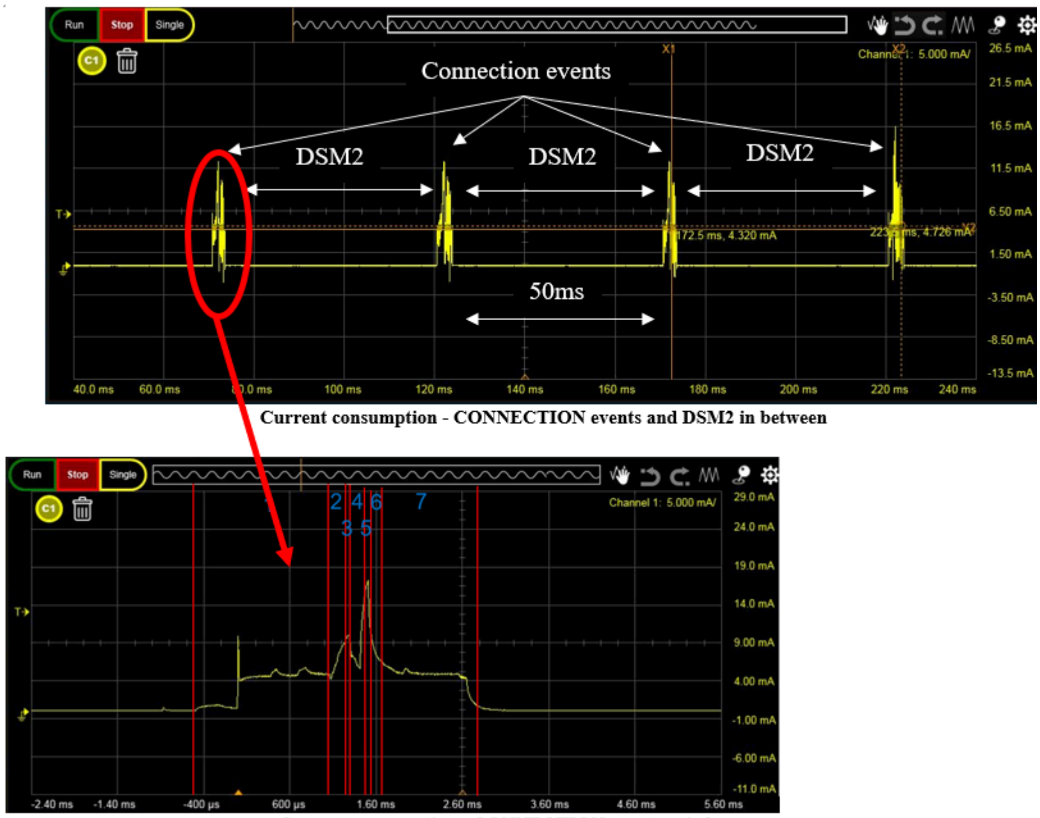

Figure 30. Current consumption during the connect event period

Table 24. Event

No.	Adv event timing
1	Pre-processing
2	TX warm-up
3	Active RX
4	RX to TX transition
5	Active TX
6	TX warm-down

Table 24. Event...*continued*

No.	Adv event timing
7	Post-processing

Note: *In the Figure 30, both use cases are used: Low power Deep Sleep mode 2 (DSM2) is activated between the Connection events.*

Figure 30 shows the current consumption during the connect event.

The binary file settings used (slave) are:

- 48 MHz clock
- Advertising with RX Y bytes payload, X TX payload and connectable
- RF output +0 dBm

Buck mode: Wake-up from low-power mode `Deep Sleep mode 2`

The smartphones are the master, which defines the data rate during the connection. Four data rates are considered:

- 1 Mbit/s
- 2 Mbit/s
- 500 kbit/s (LR S=2)
- 125 kbit/s (LR S=8)

In the `app_preinclude.h`, the `gAppExtAdvEnable` must be enabled to get the LR connection.

If enabled, the OPT Host lib is required (must set `lib_ble_5-2_OPT_host_cm33_iar.a` as lib in linker setting) `*/ #define gAppExtAdvEnable_d 1`

Test environment: Connect 1 Mbit/s

Table 25. Test environment

DC-to-DC mode	Buck
Supply	**Vdd_DCDC = 3 V** **Vdd_RF = 1.25 V** **VddLDO_Core=1.25 V**
RF output power	+0 dBm
MCX clock mode	48 MHz
RAM size	128k
Data rate	1 Mbit/s
Payload	Tx:0 bytes; Rx:2 Bytes
Connectable	Yes
Flash	Doze
MCX	Deep Sleep Mode 2 (DSM2)
Setting	Advertise from low-power DSM2 Slave to Master
Software	Low-power (2.12.5 MR2 release)

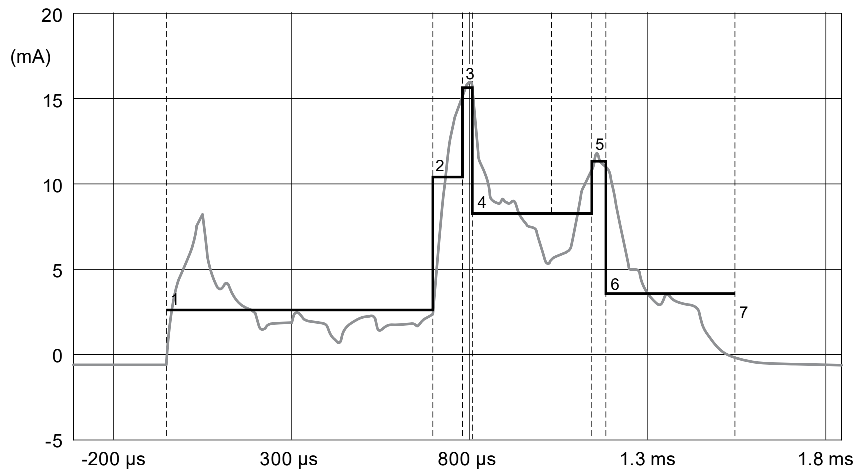

Figure 31. Connect profile in buck mode, DSM2 (MCX DSM2, flash doze), 1 Mbit/s

Table 26. Connect current consumption in buck mode, DSM2 (MCX DSM2, flash doze), 1 Mbit/s

CONNECTION (1 packet exchange)				
1 Msps	**Buck mode**	**Idd_REG (total consumption)**		
	State	**Time(ms)**	**Current(mA)**	**mA x mS**
CONNECTION	Pre-Processing	0.750 ms	2.717 mA	2.038 mA-ms
	RX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms
	RX1 Level	0.080 ms	6.948 mA	0.556 mA-ms
	RX1 to TX1 Transition	0.150 ms	6.840 mA	1.026 mA-ms
	TX1 Level	0.096 ms	6.860 mA	0.659 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms
	Post-Processing	0.360 ms	4.825 mA	1.737 mA-ms
	Active Consumption	1.536 ms	4.361 mA	6.699 mA-ms
Charge Integral: 1.86 nAh				

Test environment: Connect 2 Mbit/s

Table 27. Test environment

DC-to-DC mode	**Buck**
Supply	**Vdd_DCDC = 3 V** **Vdd_RF = 1.25 V** **VddLDO_Core=1.25 V**
RF output power	+0 dBm
MCX clock mode	48 MHz
RAM size	128k
Data rate	2 Mbit/s
Payload	Tx:0 bytes; Rx:2 Bytes
Connectable	Yes
Flash	Doze
MCX	Deep Sleep Mode 2 (DSM2)
Setting	Advertise from low-power DSM2

Table 27. Test environment...*continued*

DC-to-DC mode	Buck
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V
	Slave to Master
Software	Low-power (2.12.5 MR2 release)

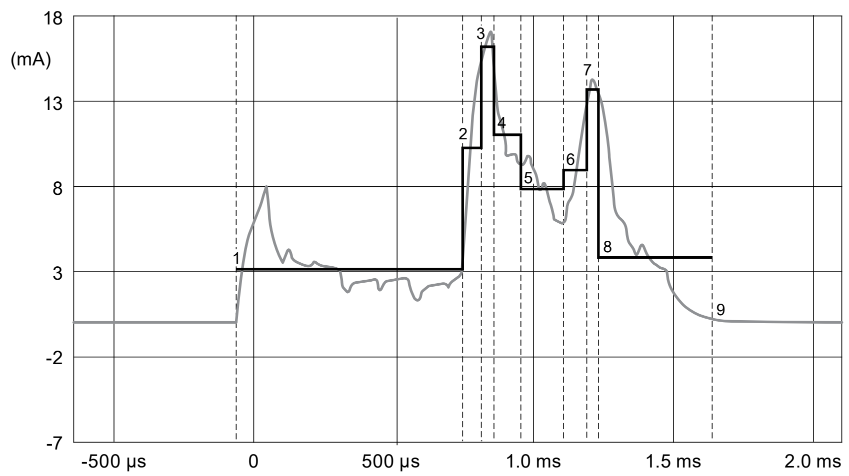

Figure 32. Connect profile in buck mode, DSM2 (MCX DSM2, flash doze), 2 Mbit/s

Table 28. Connect current consumption in buck mode, DSM2 (MCX DSM2, flash doze), 2 Mbit/s

CONNECTION (1 packet exchange)				
2 Msps	**Buck mode**	**Idd_REG (total consumption)**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
CONNECTION	Pre-Processing	0.750 ms	1.089 mA	0.816 mA-ms
	RX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms
	RX1 Level	0.044 ms	6.948 mA	0.306 mA-ms
	RX1 to TX1 Transition	0.150 ms	6.840 mA	1.026 mA-ms
	TX1 Level	0.052 ms	6.860 mA	0.357 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms
	Post-Processing	0.360 ms	4.825 mA	1.737 mA-ms
	Active Consumption	1.456 ms	3.383 mA	4.926 mA-ms
	Charge Integral: 1.37 nAh			

Test environment: Connect 500 kbit/s (coded LR S2)

Table 29. Test environment

DC-to-DC mode	Buck
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V
RF output power	+0 dBm
MCX clock mode	48 MHz

Table 29. Test environment...*continued*

DC-to-DC mode	Buck
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V
RAM size	128k
Data rate	500 kbit/s
Payload	Tx:0 bytes; Rx:2 Bytes
Connectable	Yes
Flash	Doze
MCX	Deep Sleep Mode 2 (DSM2)
Setting	Advertise from low-power DSM2 Slave to Master
Software	Low-power (2.12.5 MR2 release)

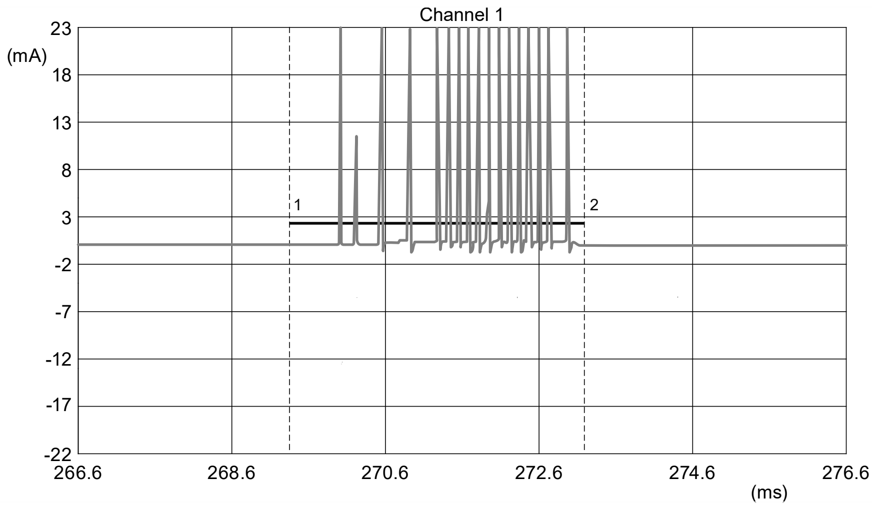

Figure 33. Connect profile in buck mode, DSM2 (MCX DSM2, flash doze), 500 kbit/s LR S2

Table 30. Connect current consumption in buck mode, DSM2 (MCX DSM2, flash doze), 500 kbit/s LR S2

CONNECTION (1 packet exchange)				
500 ksps	Buck mode	Idd_REG (total consumption)		
	State	Time(ms)	Current(mA)	mA x mS
CONNEC TION	Pre-Processing	0.750 ms	2.726 mA	2.175 mA-ms
	RX1 Rise	0.080 ms	6.840 mA	0.313 mA-ms
	RX1 Level	0.160 ms	6.948 mA	0.960 mA-ms
	RX1 to TX1 Transition	0.150 ms	6.840 mA	0.629 mA-ms
	TX1 Level	0.192 ms	6.860 mA	0.816 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.095 mA-ms
	Post-Processing	0.360 ms	4.825 mA	0.641 mA-ms
	Active Consumption	1.712 ms	4.626 mA	7.920 mA-ms
	Charge Integral: 2.20 nAh			

Test environment: Connect 125 kbit/s (coded LR S8)

Table 31. Test environment

DC-to-DC mode	Buck
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V
RF output power	+0 dBm
MCX clock mode	48 MHz
RAM size	128k
Data rate	125 kbit/s
Payload	Tx:0 bytes; Rx:2 Bytes
Connectable	Yes
Flash	Doze
MCX	Deep Sleep Mode 2 (DSM2)
Setting:	Advertise from low-power DSM2 Slave to Master
Software	Low-power (2.12.5 MR2 release)

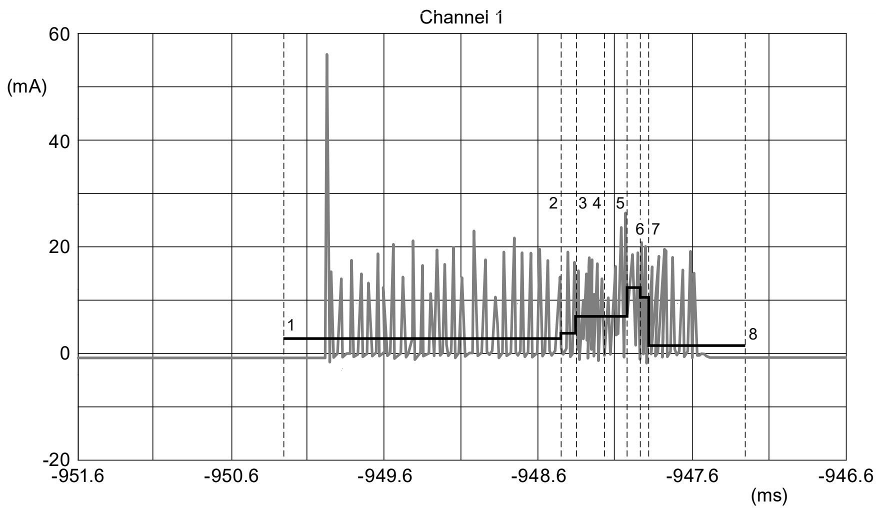

Figure 34. Connect profile in buck mode, DSM2 (MCX DSM2, flash doze), 125 kbit/s LR S8

Table 32. Connect current consumption in buck mode, DSM2 (MCX DSM2, flash doze), 125 kbit/s LR S8

CONNECTION (1 packet exchange)				
125 ksps	Buck mode	Idd_REG (total consumption)		
	State	Time(ms)	Current (mA)	mA x mS
CONNECTION	Pre-Processing	0.750 ms	2.731 mA	2.048 mA-ms
	RX1 Rise	0.080 ms	6.840 mA	0.547 mA-ms
	RX1 Level	0.640 ms	6.948 mA	4.447 mA-ms
	RX1 to TX1 Transition	0.150 ms	6.840 mA	1.026 mA-ms
	TX1 Level	0.768 ms	6.860 mA	5.268 mA-ms
	TX1 Fall	0.020 ms	6.840 mA	0.137 mA-ms
	Post-Processing	0.360 ms	4.825 mA	1.737 mA-ms
	Active Consumption	2.768 ms	5.495 mA	15.210 mA-ms

Table 32. Connect current consumption in buck mode, DSM2 (MCX DSM2, flash doze), 125 kbit/s LR S8...*continued*

CONNECTION (1 packet exchange)				
125 ksps	Buck mode	Idd_REG (total consumption)		
	State	Time(ms)	Current (mA)	mA x mS
	Charge Integral: 4.23 nAh			

Summary:

Table 33. Connect current consumption (MCX DSM2, flash doze)

48 MHz clock using 32KHx Crystal	Buck mode Consumption (3 V)
	DSM2
	T= 25 °C
CONN pre-processing 1 Mbit/s	4.361 mA
CONN pre-processing 2 Mbit/s	3.383 mA
CONN pre-processing 500 kbit/s	4.626 mA
CONN pre-processing 125 kbit/s	5.495 mA

Table 34. Connect timing (MCX DSM2, flash doze)

Radio/Profile Timing Parameters (ms)	Buck mode Consumption (3 V)
48 MHz clock using 32 kHz crystal	DSM2
	T= 25 °C
Conn Pre-processing Time – 1 Mbit/s	0.750 ms
Conn Post-processing Time - 1 Mbit/s	0.360 ms
Conn Pre-processing Time – 2 Mbit/s	0.750 ms
Conn Post-processing Time - 2 Mbit/s	0.360 ms
Conn Pre-processing Time – 500 kbit/s	0.750 ms
Conn Post-processing Time - 500 kbit/s	0.360 ms
Conn Pre-processing Time – 125 kbit/s	0.750 ms
Conn Post-processing Time - 125 kbit/s	0.360 ms

Table 35. Connect current consumption event

CONNECT	Vdcdc_in=3 V	DSM2		
1 Mbit/s	buck	1.536 ms	4.361 mA	1.861 nAh
2 Mbit/s	buck	1.456 ms	3.383 mA	1.368 nAh
LR S2, 500 kbit/s	buck	1.712 ms	4.626 mA	2.200 nAh
LR S8, 125 kbit/s	buck	2.768 ms	5.495 mA	4.225 nAh

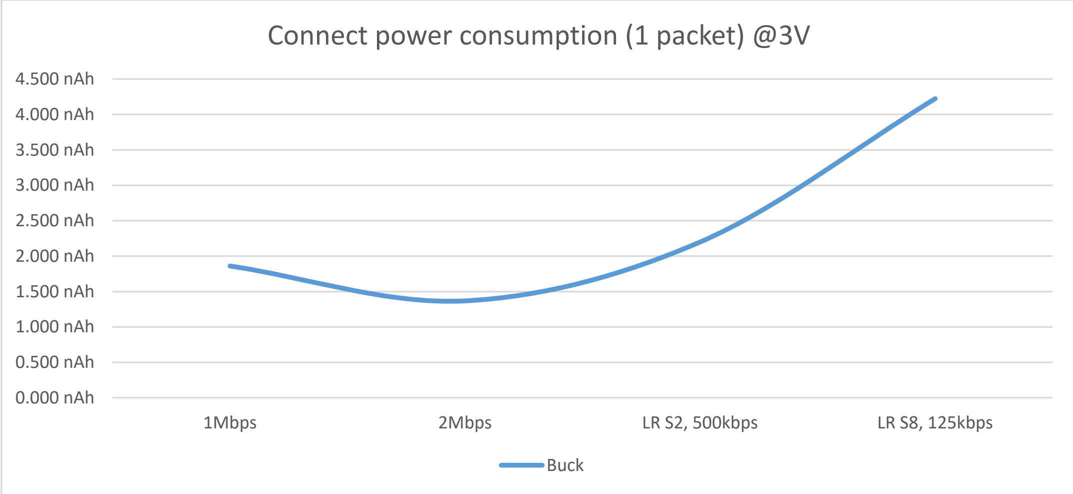

Figure 35. Connect profile vs data rate and DC-to-DC modes, DSM2 (MCX DSM2, Flash Doze)

5.2.2.6 Scan mode

Using the steps listed in Section 4.2, partial Bluetooth LE scenario (Temperature Collector Application) is shown in Figure 36. The main events and phases are listed in Table 36 including all the plots that follow depicts current.

Buck modes are used:

- DSM2 Mode is activated between the scan events.

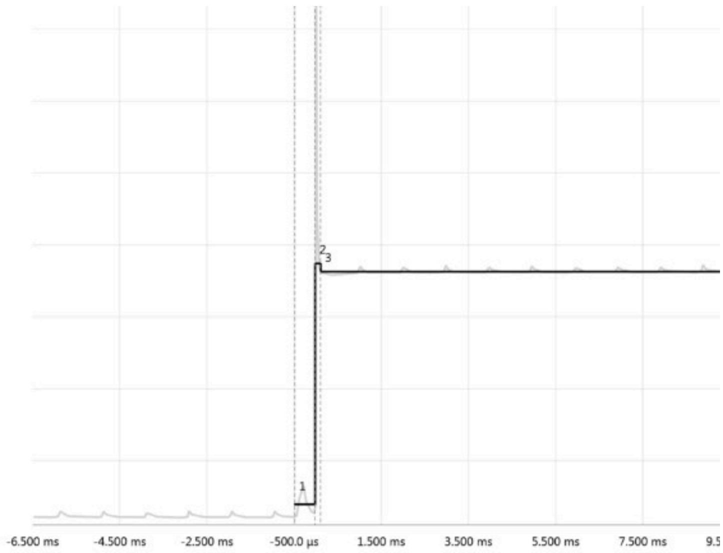

Figure 36. Current consumption - Scan event period

Table 36. Scan events

No.	Event
1	Pre-processing
2	RX warmup
3	Active RX

Table 36. Scan events*...continued*

No.	Event
4	RX warm down
5	Post-processing

Figure 37 shows the current consumption during the scan event.

The binary file settings used are:

- 48 MHz clock
- Scanning

Buck mode: Wake-up from low-power mode `Deep Sleep mode 2`

Test environment: Scan mode

Table 37. Test environment

DC-to-DC mode	Buck
Supply	**Vdd_DCDC = 3 V** **Vdd_RF = 1.25 V** **VddLDO_Core=1.25 V**
RF output power	na
MCX clock mode	48 MHz
RAM size	128k
Data rate	1 Mbit/s
Payload	na
Connectable	Yes
Flash	Doze
MCX	DSM2
Setting	Advertise from low-power DSM2 Slave to Master
Software	Low Power (2.12.5 MR2 release)

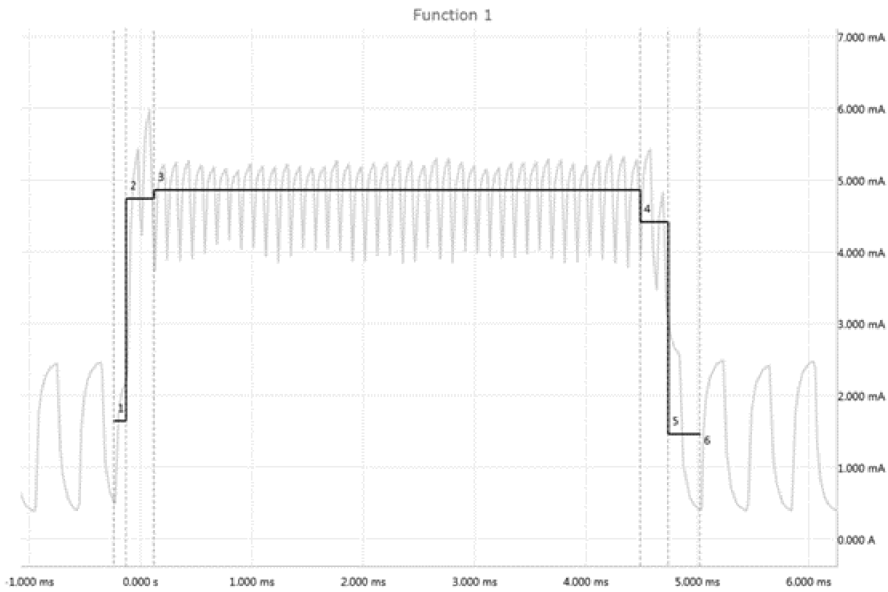

Figure 37. Scan profile in Buck mode, DSM2 (MCX DSM2, flash doze)

Table 38. Scan current consumption in Buck mode, DSM2 (MCX DSM2, flash doze)

Scanning				
Buck	**Scanning windows**	**4.0 ms**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
Scan	Scan pre-processing	1.900 ms	2.668 mA	5.069 mA-ms
	RX warm-up	0.080 ms	6.840 mA	0.547 mA-ms
	RX Scan	4.000 ms	7.463 mA	29.851 mA-ms
	RX warm-down	0.020 ms	6.840 mA	0.137 mA-ms
	Scan Post-process	0.150 ms	4.550 mA	0.683 mA-ms
	Active Consumption	6.150 ms	Avg= 5.672 mA	36.287 mA-ms
	Charge Integral: 10.08 nAh			

Summary:

Table 39. Scan current timing (MCX DSM2, Flash Doze)

Radio/Profile Timing Parameters (ms)	Buck mode Consumption (3.6 V)
	DSM2
48 MHz FEE Mode using 32 kHz crystal	**T= 25 °C**
Scan Preprocessing Time	1.900 ms
Scan Postprocessing Time	0.150 ms

Table 40. Scan current consumption event

	Vdcdc_in=3.6 V	DSM2 (ms)	DSM2 (mA)	DSM2 (nAh)
Scan	buck	6.150 ms	5.672 mA	10.08 nAh

5.3 Advertising extension

Bluetooth 5.x allows advert packets to be transmitted in the data channels (although the specification prefers to label them as secondary advert channels):

- Increases advertising data length
- Allows advertising on data channels
- Enables long-range connection establishment
- Enables chaining and periodic advertising

In this case, the new primary advert points to an auxiliary packet that specifies a “connectionless” train of packets that hop at a known Cadence.

That auxiliary packet provides the Cadence information and the access address code.

Table 41 and Figure 38 shows the current consumption during the advertising event at 1 Mbit/s, 2 Mbit/s, and coded and advertising extension event using data rate at 1 Mbit/s, 2 Mbit/s, and coded.

The binary file settings used:

- 48 MHz clock
- Advertising Extension with PDU 8 bytes for channels 37, 38, 39 and PDU Y bytes (X bytes payload) and connectable
- RF output +0 dBm

Buck mode: Wake-up from low-power mode `Deep Sleep mode 2`

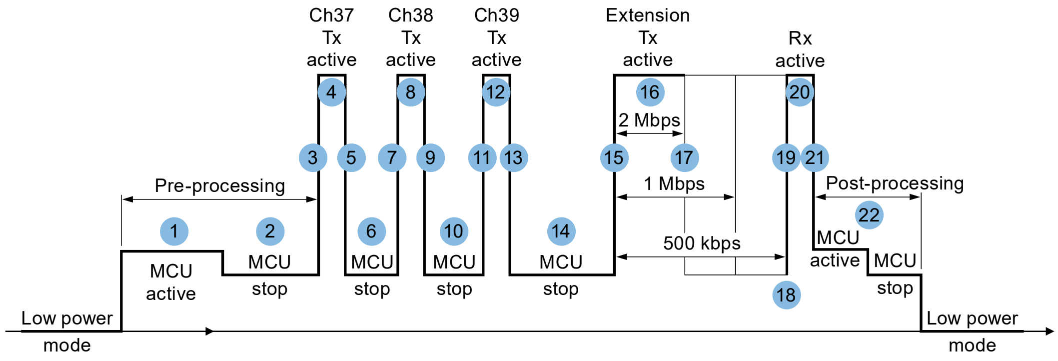

Figure 38. Current consumption - advertising event period

Table 41. Advertising extension event

No.	ADV event timing
1	Pre-processing / MCX active
2	Post-processing / MCXstop
3	TX warm-down
4	TX active
5	TX warm-down
6	MCX stop
7	TX warm-up
8	TX active
9	TX warm-down
10	MCX stop

Table 41. Advertising extension event*...continued*

No.	ADV event timing
11	TX warm-up
12	TX active
13	TX warm-down
14	MCX stop
15	TX warm-up
16	TX active
17	TX warm-down
18	TX to RX
19	RX warm-up
20	RX active
21	RX warm-down
22	Post-processing

Test environment: Advertising extension 1 Mbit/s 1 Mbit/s

Table 42. Test environment

DC-to-DC mode	Buck	
Supply	**Vdd_DCDC = 3 V** **Vdd_RF = 1.25 V** **VddLDO_Core=1.25 V**	
RF output power	+0 dBm	
MCX clock mode	48 MHz	
RAM size	128k	
Data rate	1 Mbit/s 1 Mbit/s	
Payload	For CH37.38 and39 : PDU size 2 bytes (2 bytes payload), For Secondary CH: PDU size 2, payload size Tx 31bytes, Rx 0bytes	
Connectable	Yes	
Flash	Doze	
MCX	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

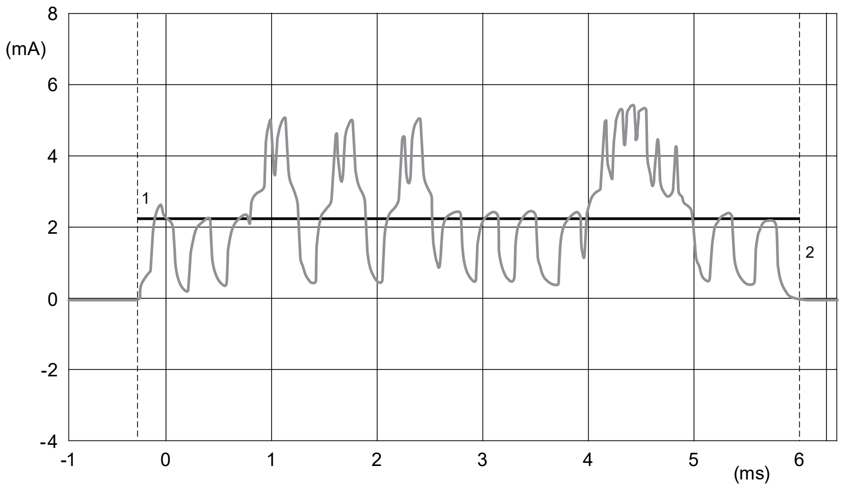

Figure 39. Advertising extension current profile event after DSM2 mode, Buck mode, 1 Mbit/s 1 Mbit/s

Table 43. Advertising extension current consumption in Buck mode, DSM2 (MCX DSM2, flash doze), 1 Mbit/s 1 Mbit/s

	Buck mode	Idd_REG (total consumption)		
	State	Time (ms)	Current (mA)	mA x mS
ADV	Active Consumption	2.421 ms	4.598 mA	11.132 mA-ms
Charge Integral: 3.09 nAh				

Test environment: Advertising extension 1 Mbit/s 2 Mbit/s

Table 44. Test environment

DC-to-DC mode	Buck	
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	
RF output power	+0 dBm	
MCX clock mode	48 MHz	
RAM size	128k	
Data rate	1 Mbit/s 2 Mbit/s	
Payload	For CH37.38 and39 : PDU size 2 bytes (2 bytes payload), For Secondary CH: PDU size 2, payload size Tx 31bytes, Rx 0 bytes.	
Connectable	Yes	
Flash	Doze	
MCX	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

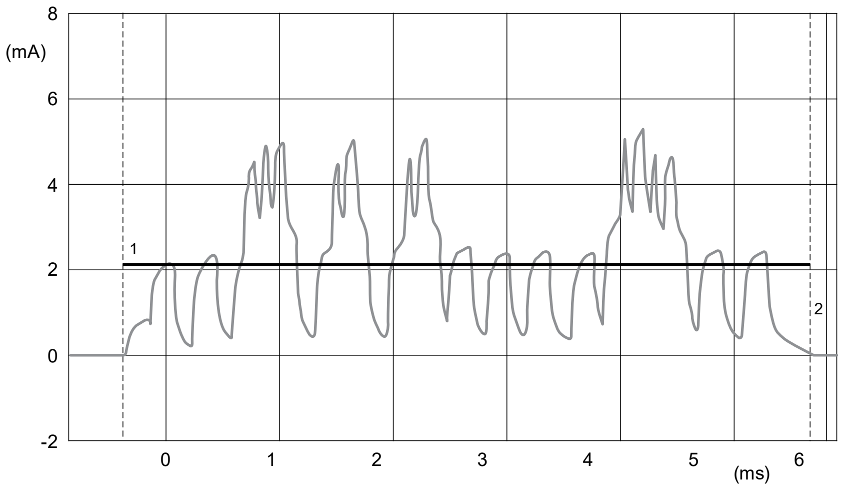

Figure 40. Advertising extension current profile event after DSM2 mode, Buck mode, 1 Mbit/s 2 Mbit/s

Table 45. Advertising extension current consumption in Buck mode, DSM2 (MCX DSM2, flash doze), 1 Mbit/s 2 Mbit/s

	Buck mode	Idd_REG (total consumption)		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
ADV	Active Consumption	2.225 ms	4.097 mA	**9.116 mA-ms**
-	**Charge Integral:** 2.53 nAh			

Test environment: Advertising extension, 1 Mbit/s coded

Table 46. Test environment

DC-to-DC mode	BUCK	
Supply	**Vdd_DCDC = 3 V** **Vdd_RF = 1.25 V** **VddLDO_Core=1.25 V**	
RF output power	+0 dBm	
MCX clock mode	48 MHz	
RAM size	128 k	
Data rate	1 Mbit/s coded	
Payload	For CH37.38 and39: PDU size 2 bytes (2 payload), For secondary CH: PDU size 2 bytes, payload size 31 bytes.	
Connectable	Yes	
Flash	Doze	
MCX	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

Table 47. Advertising Extension current consumption in Buck mode, DSM2 (MCX DSM2, flash doze), 1 Mbps coded

	Buck mode	Idd_REG (total consumption)		
	State	Time (ms)	Current (mA)	mA x mS
ADV	Active Consumption	2.829 ms	5.442 mA	15.395 mA-ms
Charge Integral: 4.28 nAh				

Test environment: Advertising extension coded 1 Msps

Table 48. Test environment

DC-to-DC mode	Buck	
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	
RF output power	+0 dBm	
MCX clock mode	48 MHz	
RAM size	128 k	
Data rate	Coded 1 Msps	
Payload	For CH37.38 and39 : PDU size 2 bytes (payload 31 bytes), For Secondary CH: PDU size 2 bytes, payload size 2 bytes	
Connectable	Yes	
Flash	Doze	
MCX	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

Test environment: Advertising extension coded 2 Mbit/s

Table 49. Test environment

DC-to-DC mode	Buck	
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	
RF output power	+0 dBm	
MCX clock mode	48 MHz	
RAM size	128k	
Data rate	Coded 2 Mbit/s	
Payload	For CH37.38 and39 : PDU size 2 bytes (payload 31 bytes), For Secondary CH: PDU size 2 bytes, payload size 2 bytes	
Connectable	Yes	
Flash	Doze	
MCX	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

Test environment: Advertising extension coded coded

Table 50. Test environment: Advertising extension Coded Coded

DC-to-DC mode	**Buck**	
Supply	**Vdd_DCDC = 3 V** **Vdd_RF = 1.25 V** **VddLDO_Core=1.25 V**	
RF output power	+10 dBm	
MCX clock mode	48 MHz	
RAM size	128 k	
Data rate	Coded Coded	
Payload	For CH37.38 and39 : PDU size 6 bytes (payload 31 bytes), For Secondary CH: PDU size 2 bytes, payload size Tx:31 bytes; Rx:2 bytes	
Connectable	Yes	
Flash	Doze	
MCX	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

Summary table:

Table 51. Advertising Extension summary table

		Idd_REG (total consumption)			
Advertising	**State**	**Time (ms)**	**Current (mA)**	**mA x mS**	**Charge Integral**
1 Msps 1 Msps	Buck mode	2.421 ms	4.598 mA	11.132 mA-ms	3.09 nAh
1 Msps 2 Msps	Buck mode	2.225 ms	4.097 mA	9.116 mA-ms	2.53 nAh
1 Msps coded	Buck mode	2.829 ms	5.442 mA	15.395 mA-ms	4.28 nAh
Coded 1 Msps	Buck mode	5.031 ms	3.998 mA	20.114 mA-ms	5.59 nAh
Coded 2 Msps	Buck mode	4.014 ms	3.851 mA	15.458 mA-ms	4.29 nAh
Coded coded	Buck mode	6.609 ms	4.720 mA	31.194 mA-ms	8.67 nAh

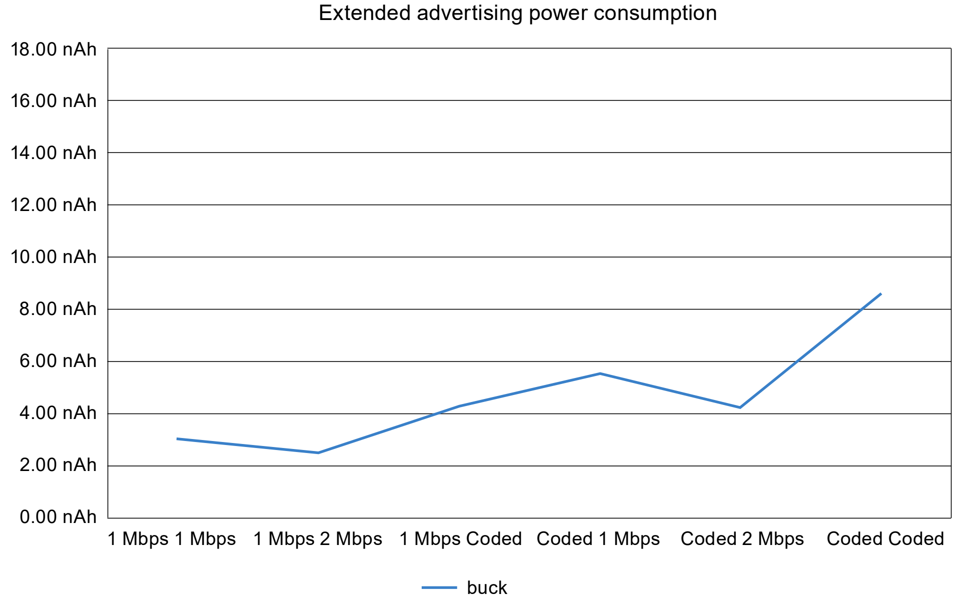

Figure 41. Advertising extension power consumption versus data rate modes

Summary data:

Table 52. Advertising Extension consumption summary table

Advertising Extension	Unit: nAh	Vdd_Reg (V) power supply (Ambient, 25 °C)							
-		1.7 V	1.8 V	2.1 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V
1 Mbit/s 1 Mbit/s	Buck	8.66 nAh	8.34 nAh	4.22 nAh	3.58 nAh	3.39 nAh	3.09 nAh	2.86 nAh	1.81 nAh
1 Mbit/s 2 Mbit/s	Buck	7.92 nAh	7.31 nAh	3.73 nAh	3.13 nAh	2.88 nAh	2.53 nAh	2.42 nAh	1.67 nAh
1 Mbit/s coded	Buck	11.96 nAh	11.53 nAh	5.83 nAh	4.95 nAh	4.68 nAh	4.28 nAh	3.96 nAh	2.51 nAh
Coded 1 Mbit/s	Buck	15.63 nAh	15.07 nAh	7.62 nAh	6.47 nAh	6.12 nAh	5.59 nAh	5.17 nAh	3.28 nAh
Coded 2 Mbit/s	Buck	12.01 nAh	11.58 nAh	5.86 nAh	4.97 nAh	4.70 nAh	4.29 nAh	3.97 nAh	2.52 nAh
Coded coded	Buck	24.23 nAh	23.36 nAh	11.81 nAh	10.03 nAh	9.49 nAh	8.67 nAh	8.02 nAh	5.08 nAh

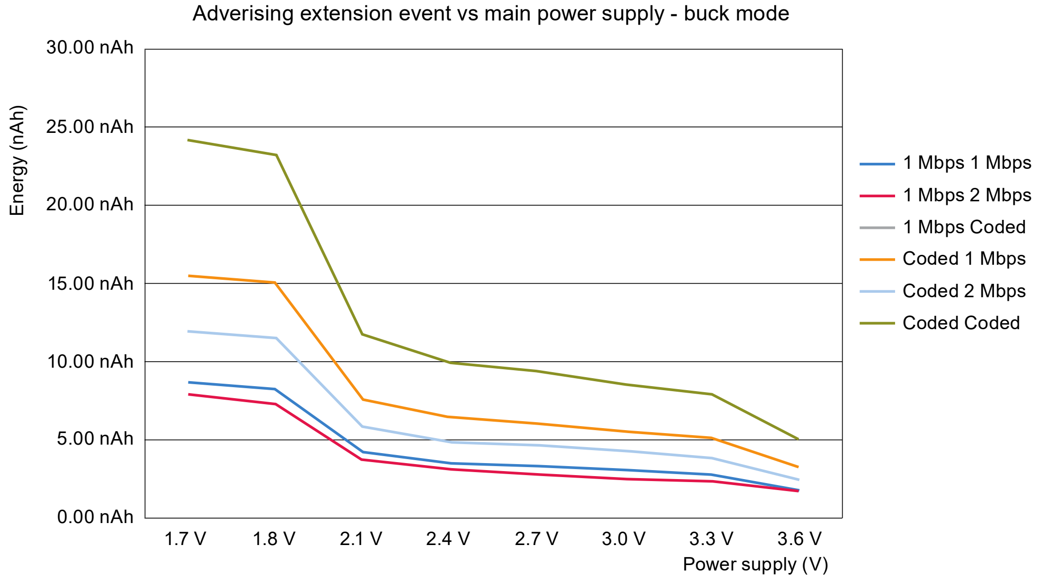

Figure 42. Advertising extension consumption event, buck mode

5.4 Scan extension

Using the steps listed in Section 4.2, partial Bluetooth LE scenario (Low-power application) has captured, as shown in Figure 43. The main events and phases are listed in Table 53 including all the plots that follows depicts current.

Both use cases are used:

- DSM2 Mode is activated between the scan events.

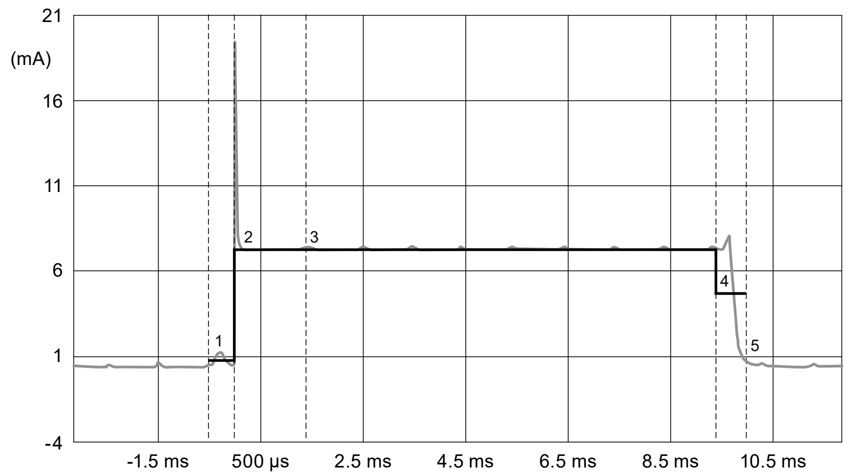

Figure 43. Current consumption - Scan extension event period

Table 53. Scan extension events

No.	Event
1	Pre-processing
2	RX warmup

Table 53. Scan extension events...*continued*

No.	Event
3	Active RX
4	RX warm down
5	Post-processing

Figure 44 shows the current consumption during the Scan extension event using data rate at 1Mbps and coded (S2, 500 kbit/s). Buck mode graphs are provided as example.

The binary file settings used are:

- 48 MHz clock
- Scan extension
- Connectable

Buck mode: Wake-up from Low-power mode `Deep Sleep mode 2`

Test environment: Scan extension 1 Mbit/s 1 Mbit/s

Table 54. Test environment

DC-to-DC mode	Buck	
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	
RF output power	na	
MCX clock mode	48 MHz	
RAM size	128 k	
Data rate	1 Msps 1 Mbit/s	
Payload	empty	
Connectable	Yes	
Flash	Doze	
MCX	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low Power (2.12.5 MR2 release)	

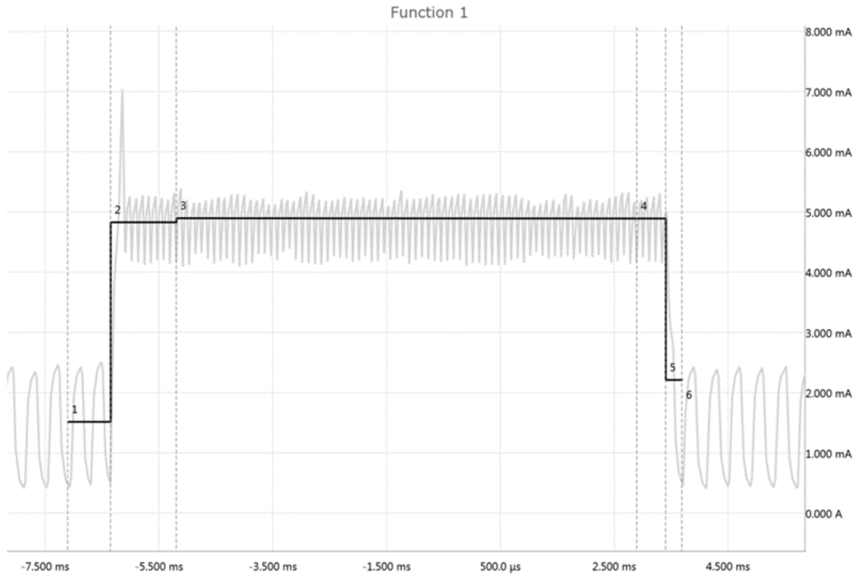

Figure 44. Scan extension current profile event after DSM2 mode, Buck mode, 1 Mbit/s 1 Mbit/s

Table 55. Scan extension current consumption in Buck mode, DSM2 (MCX DSM2, flash doze), 1 Mbit/s 1 Msps

Scanning				
Buck	**Scanning windows**	**4.00 ms**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
Scan	Scan pre-processing	1.550 ms	2.660 mA	4.123 mA-ms
	RX warm-up	0.160 ms	9.260 mA	1.482 mA-ms
	RX Scan	4.000 ms	4.860 mA	19.440 mA-ms
	RX warm-down	0.200 ms	8.900 mA	1.780 mA-ms
	Scan Post-process	0.700 ms	3.530 mA	2.471 mA-ms
	Active Consumption	6.610 ms	Avg= 5.842 mA	29.296 mA-ms
Charge Integral: 8.14 nAh				

Test environment: Scan extension 1 Mbit/s Coded

Table 56. Test environment

DC-to-DC mode	Buck	
Supply	**Vdd_DCDC = 3 V** **Vdd_RF = 1.25 V** **VddLDO_Core=1.25 V**	
RF output power	na	
MCX clock mode	48 MHz	
RAM size	128 k	
Data rate	1 Msps Coded (LR S2)	
Payload	empty	
Connectable	Yes	
Flash	Doze	

Table 56. Test environment*...continued*

DC-to-DC mode	Buck	
Supply	Vdd_DCDC = 3 V Vdd_RF = 1.25 V VddLDO_Core=1.25 V	
MCX	DSM2	
Setting	Advertise from low-power DSM2 Slave to Master	
Software	Low-power (PRC2 RC2 release)	

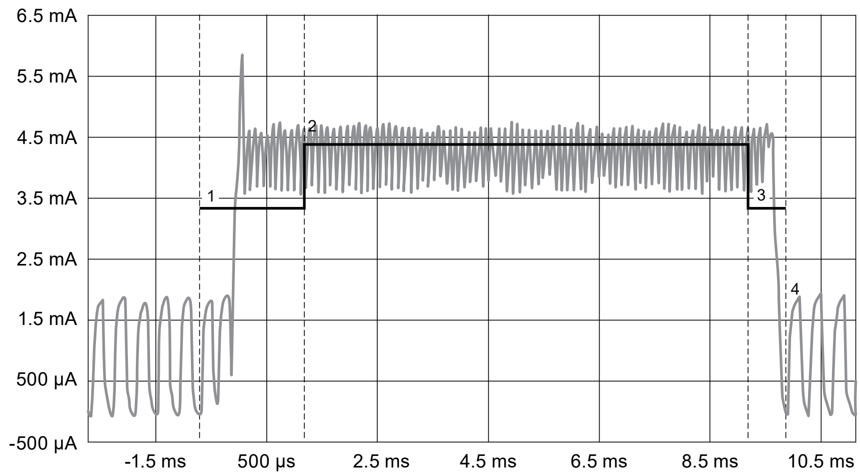

Figure 45. Scan extension current profile event after DSM2 mode, Buck mode, 1 Mbit/s Coded

Table 57. Scan extension current consumption in Buck mode, DSM2 (MCX DSM2, flash doze), 1 Mbit/s Coded

Scanning				
Buck	**Scanning Windows**	**4.000 ms**		
	State	**Time (ms)**	**Current (mA)**	**mA x mS**
Scan	Scan pre-processing	1.550 ms	2.690 mA	4.170 mA-ms
	RX warm-up	0.160 ms	9.800 mA	1.568 mA-ms
	RX Scan	4.000 ms	4.860 mA	19.440 mA-ms
	RX warm-down	0.200 ms	6.270 mA	1.254 mA-ms
	Scan Post-process	0.700 ms	1.947 mA	1.363 mA-ms
	Active Consumption	6.610 ms	Avg= 5.113 mA	27.794 mA-ms
Charge Integral: 7.72 nAh				

Timing data:

Table 58. Scanning extension timing table

No.	State	Timing (ms)	
		Buck	
		DSM2	
		1M1M	1MCoded
1	Pre processing	1.550 ms	1.550 ms
2	RX warm-up	0.160 ms	0.160 ms
3	RX active	4.000 ms	4.000 ms
4	RX warm down	0.200 ms	0.200 ms
5	Post-processing	0.700 ms	0.700 ms
6	Total	6.610 ms	6.610 ms

Table 59. Scanning extension consumption table

No.	State	Consumption (mA)	
		Buck	
		DSM2	
		1M1M	1MCoded
1	Pre processing	2.660 mA	2.690 mA
2	RX warm-up	9.260 mA	9.800 mA
3	RX active	8.800 mA	8.900 mA
4	RX warm down	8.900 mA	6.270 mA
5	Post-processing	3.530 mA	1.947 mA
6	Total	6.630 mA	5.921 mA

Summary data:

Table 60. Scanning extension consumption summary table

Scan	Unit: nAh	1.7 V	1.8 V	2.1 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V
Scan 1 Mbit/s	Buck	7.55 nAh	7.54 nAh	7.44 nAh	7.62 nAh	7.30 nAh	6.54 nAh	6.01 nAh	5.62 nAh
Scan Ext. 1 Mbit/s	Buck	9.34 nAh	9.38 nAh	9.32 nAh	9.45 nAh	9.08 nAh	8.14 nAh	7.49 nAh	7.00 nAh
Scan Ext. Coded 500 kbit/s	Buck	8.89 nAh	8.92 nAh	8.81 nAh	9.00 nAh	8.62 nAh	7.72 nAh	7.17 nAh	6.68 nAh

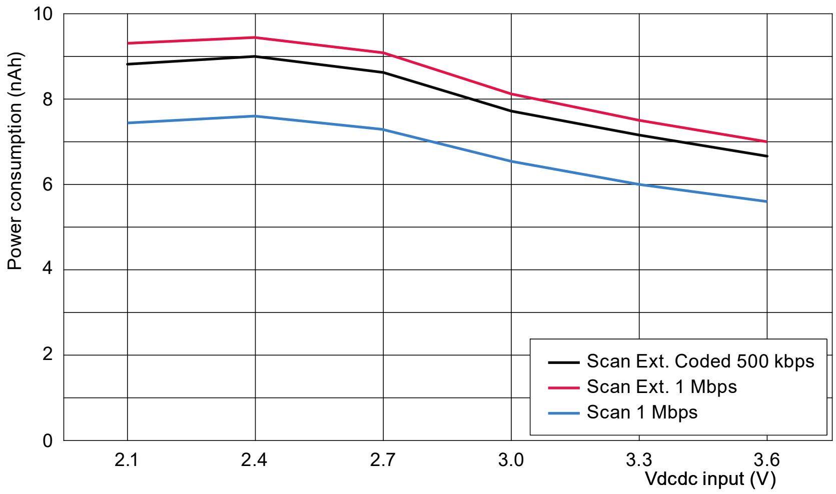

Figure 46. Scanning extension consumption event, buck mode

5.5 Channel selection algorithm #1 and #2

Channel selection algorithm #1 is the legacy method that only supports channel selection for connection events. Channel selection algorithm #1 consists of two stages: calculation of the unmapped channel index followed by mapping this index to a data channel index from the set of used channels.

Channel selection algorithm #2 supports channel selection for both connection events and periodic advertising packets. At the start of an event, which can be a connection event or a periodic advertising packet, the algorithm described here generates an event channel index (which is a data channel index or secondary advertising channel index, as appropriate). Some of the CSA #2 claims are

- Channel selection algorithm #2 (CSA #2) is a more complex and harder to track algorithm for obtaining the channel index for the next event.
- It is more effective at avoiding interference and multi-path fading effects than Channel Selection Algorithm #1, especially in high-throughput use cases.

5.6 High duty cycle advertising

High-duty cycle advertising able faster connection setup. No specific power consumption is done for this mode.

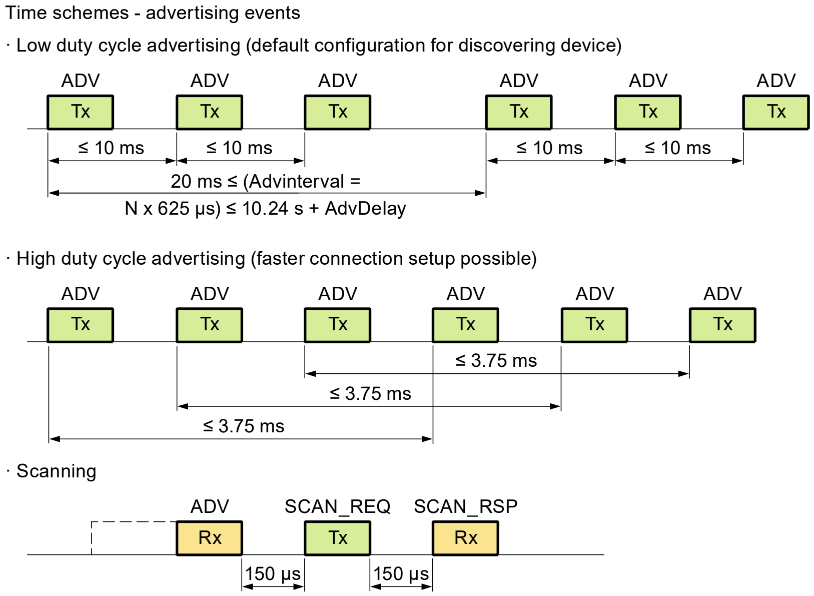

Figure 47. Low and high duty cycle advertising

5.7 Reports

Table 61 provide power consumption at 3.0 V in buck modes, at ambient temperature (+25 °C)

Table 61. SoC measurements summary table (ambient temperature, 3 V)

Deep sleep mode	Regul.	RAM retention	Core Main Power domain	Core Wake up power domain	Core RF power domain	Peripherals	DC-to-DC	Current consumption at 3 V
Deep Sleep 1	all are in Low-power mode	16 K RAM retained	Deep Sleep	Deep Sleep	Deep Sleep	Disabled	Buck	1.99 µA

Note: **Active mode: Buck mode (Vdcdc_in=3 V,), clock 48 MHz, CM33* `Deep Sleep mode 2`

Note: *Condition of measurement: Vdcdc_in=3 V, 25 °C (Ambient)*

Table 62. Wake-up timing summary table

Type of wake-up	Timing (ms) (HW+SW initialization)	Power consumption (mA) (HW+SW initialization)
First Reset (POR)	900 ms	4.8 mA
Other reset	108 ms	7.65 mA

Power consumption summary tables:

Table 63. Event power consumption summary table

1 event, Vdcdc_in=3 V, 25 °C		DSM2 (ms)	DSM2 (mA)	DSM2 (nAh)
Advertising	buck	3.458 ms	4.973 mA	4.78 nAh
MCX	buck	0.280 ms	1.800 mA	0.14 nAh
Connect-1Mbps	buck	1.536 ms	4.361 mA	1.86 nAh
Connect-2Mbps	buck	1.456 ms	3.383 mA	1.37 nAh

Table 63. Event power consumption summary table*...continued*

1 event, Vdcdc_in=3 V, 25 °C		DSM2 (ms)	DSM2 (mA)	DSM2 (nAh)
Connect-500 kbit/s	buck	1.712 ms	4.626 mA	2.20 nAh
Connect-125 kbit/s	buck	2.768 ms	5.495 mA	4.23 nAh
Scan	buck	6.150 ms	5.672 mA	10.08 nAh

Table 64. Advertising Power consumption summary table

48 MHz clock using 32MHx Crystal	Buck mode Consumption (3 V)
	DSM2
	T= 25 °C
Advertising consumption on 1 event at +0 dBm	3.458 ms
	4.973 mA
	4.78 nAh
Advertising consumption details at +0 dBm	
TX Active (+0 dBm) – MCX stop	5.060 mA
RX Active - MCX STOP	5.148 mA
TX Warm-up - MCX STOP	5.040 mA
TX Warm-down - MCX STOP	5.040 mA
RX warm-up - MCX STOP	5.040 mA
RX warm-down - MCX STOP	5.040 mA
TX to RX transition - MCX STOP (advertising event)	5.040 mA

Table 65. Pre-Post processing, MCX consumption summary table

48 MHz FEE Mode using 32MHx Crystal	Buck mode Consumption (3 V)
	DSM2
	T= 25 °C
ADV pre-processing	2.900 mA
CONN pre-processing - 1 Mbit/s	4.361 mA
CONN pre-processing - 2 Mbit/s	3.383 mA
CONN pre-processing - LRS2	4.626 mA
CONN pre-processing - LRS8	5.495 mA
Radio Post-processing	2.750 mA
MCX STOP	1.800 mA

Table 66. MCX power consumption summary table

MCX DSM2 consumption	Buck mode consumption (3 V)
	DSM2
	T= 25 °C
Timing period (ms)	0.280 ms
Consumption (mA)	1.800 mA
MCX DSM2consumption (nAh)	0.140 nAh

Timings summary table:

Table 67. Advertising and connection timing summary table

Radio/Profile Timing Parameters (ms)	Buck mode Consumption (3 V)
48 MHz clock using 32 MHz crystal	DSM2
	T= 25 °C
ADV Pre-processing Time - 1 Mbit/s	0.650 ms
ADV Post-processing Time - 1 Mbit/s	0.275 ms
Conn Pre-processing Time – 1 Mbit/s	0.750 ms
Conn Post-processing Time - 1 Mbit/s	0.360 ms
Conn Pre-processing Time - 2 Mbit/s	0.750 ms
Conn Post-processing Time - 2 Mbit/s	0.360 ms
Conn Pre-processing Time - 500 kbit/s	0.750 ms
Conn Post-processing Time - 500 kbit/s	0.360 ms
Conn Pre-processing Time - 125 kbit/s	0.750 ms
Conn Post-processing Time - 125 kbit/s	0.360 ms
SCAN Pre-processing Time - 125 kbit/s	1.900 ms
SCAN Post-processing Time - 125 kbit/s	0.150 ms

6 Revision history

Table 68. Revision history

Document ID	Release date	Description
AN14389 v.1.0	10 September 2024	• Initial version

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