AN14012

i.MX 93 to i.MX 91 Design Compatibility Guide

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Document information

Information	Content
Keywords	AN14012, i.MX 93, i.MX 91, design compatibility
Abstract	Hardware Product Design Focus. This document provides an overview of how to design a product using the i.MX 93 device when the final product utilizes the i.MX 91 device.

1 Introduction

The i.MX 91 is designed as a subset of the i.MX 93. This document provides an overview of how to design a product using the i.MX 93 device when the final product utilizes the i.MX 91 device.

The document focuses on the hardware features and the requirements to ensure a smooth transition between the two application processors.

This can also be expanded to product families that extend new customer features by upgrading from i.MX 91 to i.MX 93, while maintaining production costs by utilizing the same product PCB design within the product family.

2 Feature comparison

Section 2 provides a quick feature comparison of the i.MX 93 and i.MX 91 devices. This is intended as a quick introduction to the devices. For detail, see the device-specific data sheet *i.MX 91 Application Processors Data Sheet for Industrial Products* (document IMX91IEC) and *i.MX 93 Application Processors Data Sheet for Industrial Products* (document IMX93IEC).

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Table 1. Feature comparison

Feature	i.MX 93 device	i.MX 91 device
Main CPU	• 2x Arm Cortex-A55 @ 1.7 GHz Overdrive mode • L2 cache 64 kB • L3 cache 256 kB	• 1x Arm Cortex-A55 @ 1.4 GHz Nominal mode • L2 cache 256 kB
Microcontroller	M33	N/A
On-chip memory	• Boot ROM (256 kB) for Cortex-A55 • Boot ROM (256 kB) for Cortex-M33 • On-chip RAM (640 kB)	• Boot ROM (256 kB) for Cortex-A55 • On-chip RAM (384 kB)
DDR	16x LPDDR4/4x-3733[1]	16x LPDDR4-2400[2][3]
Memory	• 3x SD / SDIO3.0 / eMMC 5.1 • FlexSPI flash • FlexSPI with XIP	• 3x SD / SDIO3.0 / eMMC 5.1 • FlexSPI flash • FlexSPI with XIP
Graphics	PXP	N/A
Display	• LCDIF display controller • 24-bit parallel RGB • 4-lane MIPI DSI • 4-lane LVDS	• LCDIF display controller • 24-bit parallel RGB
Camera	• 8-bit parallel YUV / RGB camera • 2-lane MIPI CSI	• 8-bit parallel YUV / RGB camera
Synchronous Audio Interface (SAI) modules	• 3x SAI modules, up to 768 kHz • (SAI1) 2 TX and 1 RX • (SAI2) 4 TX and 4 RX • (SAI3) 1 TX and 1 RX	• 3x SAI modules, up to 384 kHz • (SAI1) 2 TX and 1 RX • (SAI2) **1** TX and **1** RX [4] • (SAI3) 1 TX and 1 RX
Audio (additional)	• S/PDIF • 8-channel Pulse Density Modulation (PDM) input	• S/PDIF • 8-channel Pulse Density Modulation (PDM) input
Connectivity	• (2x) USB 2.0	• (2x) USB 2.0

Table 1. Feature comparison*...continued*

Feature	i.MX 93 device	i.MX 91 device
	• (2x) Gigabit Ethernet • (8x) UART • (2x) I3C • (8x) I^2C • (8x) SPI • (2x) CAN-FD • (2x) 32-pin FlexIO • (4x) ADC	• (2x) Gigabit Ethernet • (8x) UART • (2x) I3C • (8x) I^2C • (8x) SPI • (2x) CAN-FD • (4x) ADC
Package	• 11 x 11 mm – 306-pin FCCSP, 0.5 mm pitch • 9 x 9 mm – 208-pin FCCSP, 0.5 mm pitch	• 11 x 11 mm – 306-pin FCCSP, 0.5 mm pitch • 9 x 9 mm – 208-pin FCCSP, 0.5 mm pitch

[1] For the i.MX 93 9 x 9 mm package, the maximum rate of LPDDR4x / LPDDR4 is 3200 MT/s.
[2] The i.MX 91 device supports LPDDR4 only.
[3] For the i.MX 91 9 x 9 mm package, the maximum rate of LPDDR4 is also 2400 MT/s.
[4] The i.MX 91 SAI2 only has 1 TX and 1 RX.

3 Key considerations for hardware design

Table 1 provides a quick insight into the functional blocks that changed between the i.MX 93 and i.MX 91 devices. The following sections focus on the key considerations between the i.MX 93 and i.MX 91 devices that affect the hardware design. The key features are:

- DDR interface
- Video interfaces
- Audio interfaces
- IOMUX selections
- Power supplies

The following sections provide an in-depth description of how to manage the hardware differences between the i.MX 93 and i.MX 91 devices.

3.1 DDR interface

The LPDDR4 speed of i.MX 91 is up to 2400 MT/s for both 11x11 and 9x9 package, while i.MX 93 11x11 package is up to 3733 MT/s and 9x9 package is up to 3200 MT/s.

The package delays are also different between i.MX 91 and i.MX93. These differences do not impact the board level design compatibility, i.MX 91 can still follow the same PCB layout as i.MX 93, that can highly save the transfer effort from i.MX 93 to i.MX 91.

3.2 Video interfaces

The i.MX 91 device removes the MIPI CSI, MIPI DSI, LVDS interfaces, only leaves the 8-bit parallel YUV/RGB camera and 24-bit parallel RGB display. It is suited for use-cases without high-performance displays.

3.3 Audio interfaces

Both i.MX 93 and i.MX 91 devices have three SAI interfaces, however, i.MX 93 has 4-TX / 4-RX for SAI2, while i.MX 91 only has 1-TX / 1-RX. For compatibility consideration, it is better to design SAI2 as 1-TX / 1-RX.

The sample rate of all three SAI interfaces of i.MX 93 can be up to 768 kHz, while i.MX 91 could be up to 384 kHz. However, that should be enough for most audio applications.

Table 2. Audio port comparison

Port	i.MX 93 device	i.MX 91 device	Comments
SAI1	2-TX / 1-RX	2-TX / 1-RX	Same
SAI2	4-TX / 4-RX	1-TX / 1-RX	i.MX 93 has more channels
SAI3	1-TX / 1-RX	1-TX / 1-RX	Same
S/PDIF	1-TX / 1-RX	1-TX / 1-RX	Same
PDM	Up to 8-Mics	Up to 8-Mics	Same

3.4 IOMUX selections

For the i.MX devices, the IOMUX refers to the module that multiplexes each I/O pin. This programmable module provides SW selection of multiple I/O features on each of the I/O pins. For detail on IOMUX selections, refer to the device reference manual.

Even though i.MX 91 is a reduced subset of i.MX 93, the IOMUX add new I/O selections to increase design flexibility. Therefore, the i.MX 91 provides new IOMUX options that are not available on the i.MX 93. When designing for dual 9x usage, you must ensure that the I/O features are available on both the i.MX 93 and i.MX 91 devices.

Table 3 highlights these changes:

- The bold text indicates selections, which are deleted on i.MX 91.
- The normal text indicates selections, which are added on i.MX 91, and not available on i.MX 93.

Table 3. Different IOMUX selections

I/O pad	Alt2	Alt3	Alt6	Alt7
GPIO_IO28	can1.TX	-	-	-
GPIO_IO29	can1.RX	-	-	-
ENET1_MDC	-	-	i2c1.SCL	-
ENET1_MDIO	-	-	i2c1.SDA	-
ENET1_TD3	-	-	i2c2.SCL	-
ENET1_TD2	-	-	i2c2.SDA	-
ENET1_TX_CTL	spi2.SCK	-	-	-
ENET1_TXC	spi2.SIN	-	-	-
ENET1_RX_CTL	spi2.PCS0	-	-	-
ENET1_RXC	spi2.SOUT	-	-	-
ENET2_MDC	-	-	isi.PCLK	-
ENET2_MDIO	-	-	isi.D[0]	-
ENET2_TD3	-	-	isi.FRAME_VALID	-
ENET2_TD2	**sai2.RX_DATA[1]**[1]	-	isi.LINE_VALID	-
ENET2_TD1	**sai2.RX_DATA[2]**[1]	-	isi.D[1]	-
ENET2_TD0	**sai2.RX_DATA[3]**[1]	-	isi.D[2]	-

Table 3. Different IOMUX selections...*continued*

I/O pad	Alt2	Alt3	Alt6	Alt7
ENET2_TX_CTL	-	-	isi.D[3]	-
ENET2_TXC	-	-	isi.D[4]	-
ENET2_RX_CTL	-	-	isi.D[5]	-
ENET2_RXC	**sai2.TX_DATA[1]**[1]	-	isi.D[6]	-
ENET2_RD0	**sai2.TX_DATA[2]**[1]	-	isi.D[7]	-
ENET2_RD1	**sai2.TX_DATA[3]**[1]	-	isi.D[8]	-
ENET2_RD2	-	-	isi.D[9]	-
SD1_CLK	-	spi2.SCK	-	-
SD1_CMD	-	spi2.SIN	-	-
SD1_DATA0	-	spi2.PCS0	-	-
SD1_DATA1	-	spi2.SOUT	-	-
SD1_DATA2	-	spi2.PCS1	-	-
SD1_DATA3	-	spi1.PCS1	-	-
SD1_DATA4	-	spi1.PCS0	-	-
SD1_DATA5	-	spi1.SIN	-	-
SD1_DATA6	-	spi1.SCK	-	-
SD1_DATA7	-	spi1.SOUT	-	-
SD3_CLK	uart1.CTS_B	-	-	-
SD3_CMD	uart1.RTS_B	-	-	-
SD3_DATA0	uart2.CTS_B	-	-	-
SD3_DATA1	uart2.RTS_B	-	-	-
SD3_DATA2	i2c4.SDA	-	-	-
SD3_DATA3	i2c4.SCL	-	-	-
SD2_CD_B	-	i2c1.SCL	-	sai3.TX_SYNC
SD2_CLK	-	i2c1.SDA	-	-
SD2_DATA0	-	uart1.TX	-	-
SD2_DATA1	-	uart1.RX	-	-
SD2_DATA2	-	uart2.TX	-	-
SD2_DATA3	-	uart2.RX	-	-
UART2_TXD	-	-	-	sai3.TX_SYNC
SAI1_TXD0	-	-	sai1.MCLK	-

[1] Selection that is deleted on the i.MX 91 device.

3.5 Power supplies

The power supply of the i.MX 91 device has a few differences from the i.MX 93 device, however, both have two same PMICs PCA9451A and PF9453. This section illustrates the power supply differences and design compatibility of the two devices.

3.5.1 Power architecture comparison

Figure 1 and Figure 2 are the power architecture diagrams for i.MX 93 and i.MX 91, respectively.

The main differences between the i.MX 93 and i.MX 91 power architectures are:

1. The i.MX 91 device does not have the following power supplies: VDD_MIPI_0P8, VDD_MIPI_1P8, VDD_LVDS_1P8.
2. The i.MX 91 device merges the VDDQ_DDR with VDD2_DDR supplies, as it only supports LPDDR4.

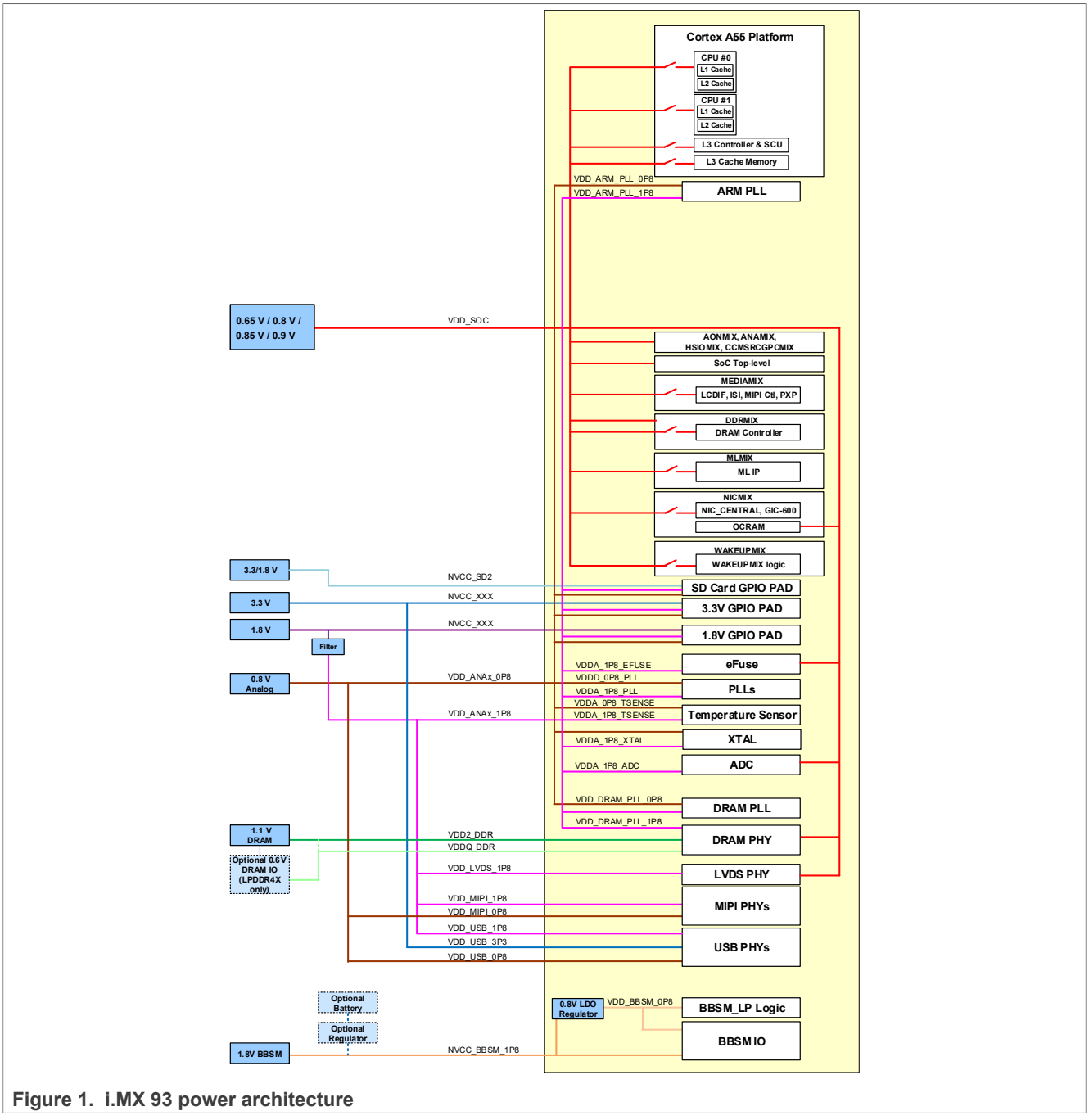

Figure 1. i.MX 93 power architecture

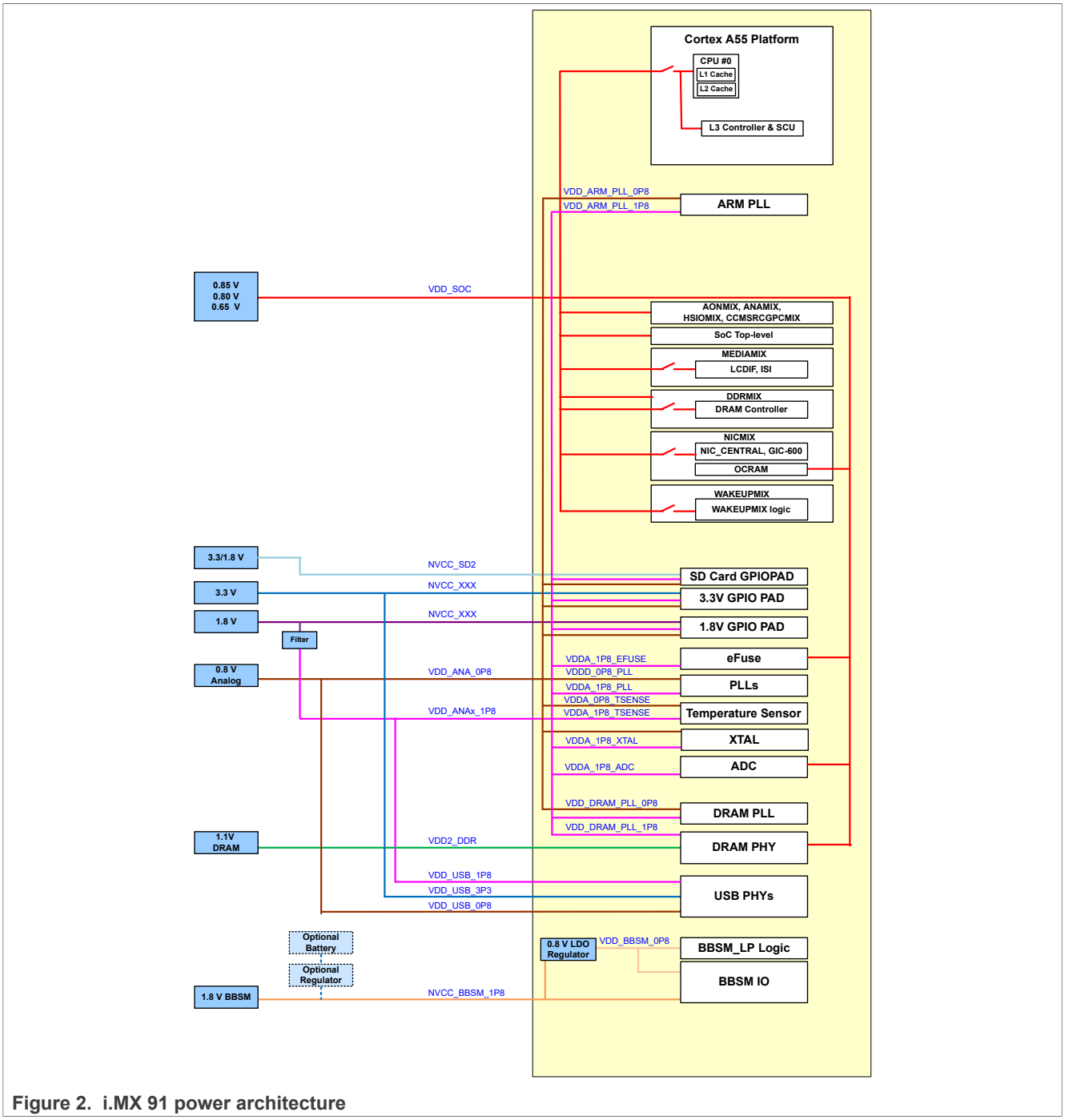

Figure 2. i.MX 91 power architecture

3.5.2 Power operating range

Table 4 and Table 5 illustrate the power operating range differences between i.MX 93 and i.MX 91.

Table 4. i.MX 93 operating range

Parameter description	Symbol	Min	Typ	Max	Unit	Comment
Power supply for SoC logic and Arm core	VDD_SOC	0.85	0.90	0.95	V	Power supply for SoC, Overdrive mode[1]

Table 4. i.MX 93 operating range*...continued*

Parameter description	Symbol	Min	Typ	Max	Unit	Comment
		0.80	0.85	0.90	V	Power supply for SoC, Nominal mode
		0.76	0.80	0.84	V	Power supply for SoC, Low-drive mode
		0.61	0.65	0.70	V	Power supply for SoC, Suspend mode
Digital supply for PLLs, temperature sensor, LVCMOS I/O, MIPI, and USB PHYs	VDD_ANA_0P8	0.76	0.80	0.84	V	-
	VDD_MIPI_0P8[2]					
	VDD_USB_0P8					
1.8 V supply for PLLs, eFuse, temperature sensor, LVCMOS voltage detect reference, ADC, 24 MHz Xtal, LVDS, MIPI, and USB PHYs	VDD_ANAx_1P8 [3]	1.71	1.80	1.89	V	-
	VDD_LVDS_1P8[2]					
	VDD_MIPI_1P8 [2]					
	VDD_USB_1P8					
Voltage supply for DRAM PHY	VDD2_DDR [4]	1.06	1.10	1.14	V	-
Voltage supply for DRAM PHY I/O	VDDQ_DDR[4]	1.06	1.10	1.14	V	LPDDR4
		0.57	0.60	0.67	V	LPDDR4X

[1] The i.MX 93 device can support up to Overdrive mode, 1.7 GHz, i.MX 91 can only support up to Nominal mode, 1.4 GHz.
[2] The i.MX 93 device has VDD_MIPI_0P8, VDD_MIPI_1P8, VDD_LVDS_1P8, however, the i.MX 91 device does not have these power supplies.
[3] VDD_ANAx_1P8 refers to VDD_ANA0_1P8, VDD_ANA1_1P8, and VDD_ANAVDET_1P8.
[4] The i.MX 93 device has separate power supplies for VDD2_DDR and VDDQ_DDR. VDDQ_DDR can be 1.1 V for LPDDR4 and 0.6 V for LPDDR4X. The i.MX 91 device only has one power supply for VDD2_DDR, can only be 1.1 V for LPDDR4.

Table 5. i.MX 91 operating range

Parameter description	Symbol	Min	Typ	Max	Unit	Comment
Power supply for SoC logic and Arm core	VDD_SOC	0.80	0.85	0.90	V	Power supply for SoC, nominal mode [1]
		0.76	0.80	0.84	V	Power supply for SoC, Low-drive mode
		0.61	0.65	0.69	V	Power supply for SoC, Suspend mode
Digital supply for PLLs, temperature sensor, LVCMOS I/O, and USB PHYs	VDD_ANA_0P8	0.76	0.80 / 0.85	0.90	V	-
	VDD_USB_0P8					
1.8 V supply for PLLs, eFuse, temperature sensor, LVCMOS voltage detect reference, ADC, 24 MHz Xtal, and USB PHYs	VDD_ANAx_1P8 [2]	1.71	1.80	1.89	V	-
	VDD_USB_1P8					
Voltage supply for DRAM PHY and I/O	VDD2_DDR [3]	1.06	1.10	1.14	V	LPDDR4 only

[1] The i.MX 93 device can support up to Overdrive mode, 1.7 GHz, i.MX 91 can only support up to Nominal mode, 1.4 GHz.

[2] VDD_ANAx_1P8 refers to VDD_ANA0_1P8, VDD_ANA1_1P8, and VDD_ANAVDET_1P8.
[3] The i.MX 93 device has separate power supplies for VDD2_DDR and VDDQ_DDR. VDDQ_DDR can be 1.1 V for LPDDR4 and 0.6 V for LPDDR4X. The i.MX 91 device only has one power supply for VDD2_DDR, can only be 1.1 V for LPDDR4.

3.5.3 Estimated maximum current

Power consumption is highly dependent on the application. Estimating the maximum supply current required for the power supply design is difficult because the use cases that require maximum supply current are not the realistic cases.

To help illustrate the effect of the application on power consumption, data was collected while running consumer standard benchmarks that are compute and graphic intensive. The results can be used as guidelines for the power supply design.

Table 6. Maximum supply current for i.MX 93

Power rail	Max current	Unit
VDD_SOC	2700	mA
VDD_ANA_0P8	50	mA
VDD_ANAx_1P8[1]	250	mA
NVCC_BBSM_1P8	2	mA
NVCC_GPIO, NVCC_WAKEUP, NVCC_AON	Imax = N x C x V x (0.5 x F) Where: • N: Number of I/O pins supplied by the power line C—Equivalent external capacitive load • V: I/O voltage • (0.5 x F): Data change rate. Up to 0.5 of the clock rate (F) • In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz	
VDDQ_DDR	160	mA
VDD2_DDR	525	mA
VDD_MIPI_0P8 (for MIPI CSI-2 2-lane RX PHY)	18	mA
VDD_MIPI_0P8 (for MIPI-DSI 2-lane TX PHY)	33	mA
VDD_MIPI_1P8 (for MIPI CSI-2 2-lane RX PHY)	2.5	mA
VDD_MIPI_1P8 (for MIPI-DSI 4-lane TX PHY)	9.5	mA
VDD_USB_3P3 (for USB PHY)	25.2	mA
VDD_USB_1P8 (for USB PHY)	36.2	mA
VDD_USB_0P8 (for USB PHY)	22.2	mA
VDD_LVDS_1P8	45	mA

[1] VDD_ANAx_1P8 refers to VDD_ANA0_1P8, VDD_ANA1_1P8, and VDD_ANAVDET_1P8.

Table 7. Maximum supply current for i.MX 91

Power rail	Max current	Unit
VDD_SOC	1500	mA
VDD_ANA_0P8	50	mA
VDD_ANAx_1P8[1]	150	mA
NVCC_BBSM_1P8	2	mA

Table 7. Maximum supply current for i.MX 91*...continued*

Power rail	Max current	Unit
NVCC_GPIO, NVCC_WAKEUP, NVCC_AON	Imax = N x C x V x (0.5 x F) Where: • N: Number of I/O pins supplied by the power line C—Equivalent external capacitive load • V: I/O voltage • (0.5 x F): Data change rate. Up to 0.5 of the clock rate (F) • In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz	
VDD2_DDR	400	mA
VDD_USB_3P3 (for USB PHY)	25.2	mA
VDD_USB_1P8 (for USB PHY)	36.2	mA
VDD_USB_0P8 (for USB PHY)	22.2	mA

[1] VDD_ANAx_1P8 refers to VDD_ANA0_1P8, VDD_ANA1_1P8, and VDD_ANAVDET_1P8.

3.5.4 Power sequence

The i.MX 91 device has fewer power supplies than i.MX 93, however, the power sequences are similar in both the devices. For detail on power sequences, see *i.MX 91 Application Processors Data Sheet for Industrial Products* (document IMX91IEC) and *i.MX 93 Application Processors Data Sheet for Industrial Products* (document IMX93IEC).

3.5.5 PMIC

The NXP PMIC PCA9451A and PF9453 can be used for both i.MX 93 and i.MX 91. Table 8 and Table 9 illustrate the differences of power connections.

Table 8. PCA9451A power connections

SEQ	Regulator	Vol (V)	Max I (mA)	PWR rails	i.MX 93 voltage (V)	i.MX 91 voltage (V)	Comment
T0	LDO1	1.8	10	NVCC_BBSM_1P8	1.8	1.8	-
T1	BUCK1 / BUCK3[1]	0.85	4000	VDD_SOC	0.9 / 0.85 / 0.8 / 0.65	0.85 / 0.8 / 0.65	Dual phase for i.MX 93; Single phase for i.MX 91 to save external components
T2	LDO4	0.8	200	• VDD_ANA_0P8 • VDD_xxx_0P8	0.8	0.8	-
T3	BUCK5	1.8	2000	• NVCC_1P8 • VDD_ANAx_1P8 • VDD_xxx_1P8	1.8	1.8	-
T4	BUCK6	1.1	1500	• VDD2_DDR • VDDQ_DDR[2]	1.1	1.1	Combined for LPDDR4
T5	BUCK2	0.6	2000	• VDDQ_DDR [3]	0.6 V	Not used	0.6 V for LPDDR4X only
T6	BUCK4	3.3	3000	• NVCC_3P3 • VDD_USB_3P3	3.3	3.3	-
T7	LDO5	3.3/1.8	150	• NVCC_SD2	3.3/1.8	3.3/1.8	-

[1] i.MX 91 only needs BUCK1 as the maximum current is less than 2A.
[2] The i.MX93 device VDDQ_DDR must be supplied at 1.1 V for LPDDR4, however, the i.MX 91 device does not have VDDQ_DDR.
[3] The i.MX93 device VDDQ_DDR must be supplied at 0.6 V for LPDDR4X, using BUCK2. The i.MX 91 device does not need.

Table 9. PF9453 power connections

SEQ	Regulator	Vol (V)	Max I (mA)	PWR rails	i.MX 93 voltage (V)	i.MX 91 voltage (V)	Comment
T0	LDO_ SNVS	1.8	10	• NVCC_BBSM_1P8	1.8	1.8	-
T1	BUCK2 [1]	0.85	2000	• VDD_SOC	0.9 / 0.85 / 0.8 / 0.65	0.85 / 0.8 / 0.65	-
T2	LDO2 [2]	0.8	200	• VDD_ANA_0P8 • VDD_xxx_0P8	0.8	0.8	Only QFN package has LDO2
T3	BUCK3	1.8	2000	• NVCC_1P8 • VDD_ANAx_1P8 • VDD_xxx_1P8	1.8	1.8	-
T4	BUCK1	1.1	2000	• VDD2_DDR • VDDQ_DDR [3]	1.1	1.1	Combined for LPDDR4
T5	BUCK4	3.3	2500	• NVCC_3P3 • VDD_USB_3P3	3.3	3.3	-
T6	LDO1	3.3 / 1.8	150	• NVCC_SD2	3.3 / 1.8	3.3 / 1.8	-

[1] The max current of BUCK2 is 2 A. It could only support limited applications of i.MX 93.
[2] Only QFN package has LDO2, WLCSP package must use external LDO to supply VDD_ANA_0P8, or use LDO1 to supply VDD_ANA_0P8.
[3] PF9453 only supports LPDDR4, VDD2, and VDDQ must be combined at 1.1 V.

Disabling PCA9451A BUCK2 and BUCK3 can reduce the BOM cost for an i.MX 91 application, the input pins and feedback pins must be connected to the power input, and the LX pins can be left open, external inductors and capacitors are not needed (see Figure 3).

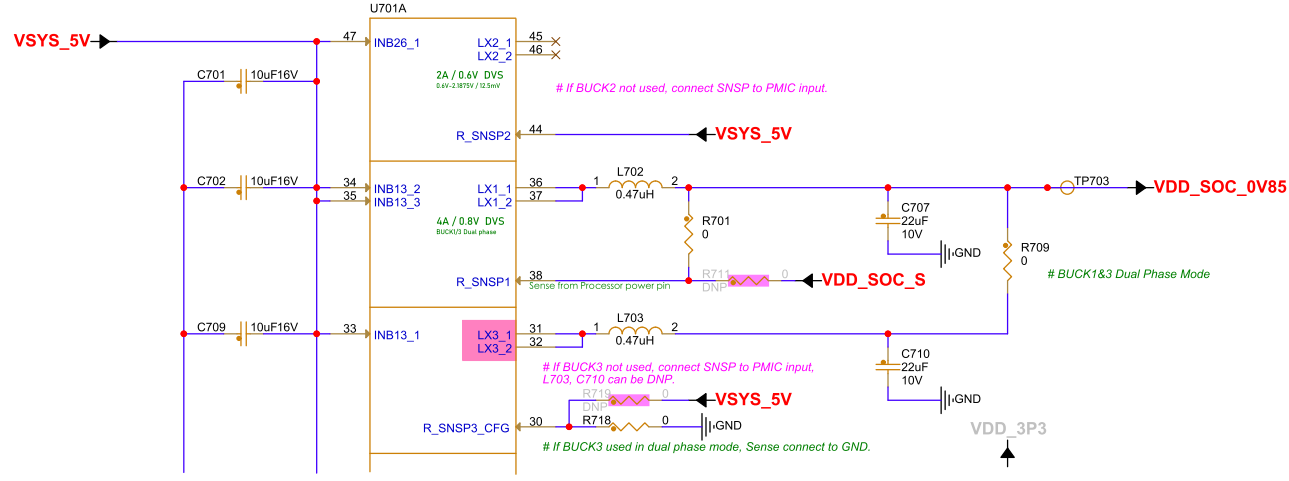

Figure 3. Disabling PCA9451A BUCK2/3

4 Package and ball map

Both, i.MX 93 and i.MX 91, have two packages:

1. 11x11 mm package with 0.5 mm pitch and 306 pads.
2. 9x9 mm package with 0.5 mm pitch and 208 pads.

For detail on package and ball-map information, see *i.MX 91 Application Processors Data Sheet for Industrial Products* (document IMX91IEC) and *i.MX 93 Application Processors Data Sheet for Industrial Products* (document IMX93IEC).

4.1 11x11 package pin list

Table 10 describes the 11 x 11 package pins that have changed in i.MX 91.

Table 10. 11x11 package changed pin list

BGA pin number	i.MX 93 pin name	i.MX 91 pin name	Comments
G6	VDDQ_DDR	VDD2_DDR	i.MX 91 only supports LPDDR4, all the VDDQ_DDR pins are changed to VDD2_DDR, and can only supply 1.1 V.
J6	VDDQ_DDR	VDD2_DDR	
J7	VDDQ_DDR	VDD2_DDR	
L6	VDDQ_DDR	VDD2_DDR	
B3	LVDS_CLK_P	NC	• These pins are not connected (NC) for i.MX 91, they are only connected to the solder ball for mechanical stability. • For the i.MX 91 based design only, these pins can be floating. • For compatible design with i.MX 93, these pins connections can be the same as i.MX 93.
A3	LVDS_CLK_N	NC	
B5	LVDS_D0_P	NC	
A5	LVDS_D0_N	NC	
B4	LVDS_D1_P	NC	
A4	LVDS_D1_N	NC	
B2	LVDS_D2_P	NC	
A2	LVDS_D2_N	NC	
C1	LVDS_D3_P	NC	
B1	LVDS_D3_N	NC	
E10	MIPI_CSI1_CLK_P	NC	
D10	MIPI_CSI1_CLK_N	NC	
B11	MIPI_CSI1_D0_P	NC	
A11	MIPI_CSI1_D0_N	NC	
B10	MIPI_CSI1_D1_P	NC	
A10	MIPI_CSI1_D1_N	NC	
E6	MIPI_DSI1_CLK_P	NC	
D6	MIPI_DSI1_CLK_N	NC	
B6	MIPI_DSI1_D0_P	NC	
A6	MIPI_DSI1_D0_N	NC	
B7	MIPI_DSI1_D1_P	NC	
A7	MIPI_DSI1_D1_N	NC	
B8	MIPI_DSI1_D2_P	NC	
A8	MIPI_DSI1_D2_N	NC	

Table 10. 11x11 package changed pin list*...continued*

BGA pin number	i.MX 93 pin name	i.MX 91 pin name	Comments
B9	MIPI_DSI1_D3_P	NC	
A9	MIPI_DSI1_D3_N	NC	
D8	MIPI_REXT	NC	
F6	VDD_LVDS_1P8	NC	
G8	VDD_MIPI_0P8	NC	
F8	VDD_MIPI_1P8	NC	

4.2 9x9 package pin list

Table 11 describes the 9 x 9 package pins that have changed in i.MX 91.

Table 11. 9x9 package changed pin list

BGA Pin number	i.MX 93 pin name	i.MX 91 pin name	Comments
F5	VDDQ_DDR	VDD2_DDR	i.MX 91 only supports LPDDR4, all the VDDQ_DDR pins are changed to VDD2_DDR, and can only supply 1.1 V.
H5	VDDQ_DDR	VDD2_DDR	

5 References

Table 12 lists additional documents and resources that can be referred to for more information. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

Table 12. Related documentation/resources

Document	Link/how to access
i.MX 93 Application Processors Data Sheet for Industrial Products	IMX93IEC
i.MX 93 Hardware Design Guide	IMX93HDG
i.MX 91 Application Processors Data Sheet for Industrial Products	IMX91IEC
i.MX 93 Evaluation Kit	i.MX93EVK
i.MX 91 Evaluation Kit	i.MX91EVK

6 Acronyms and abbreviations list

Table 13 defines the acronyms and abbreviations used in this document.

Table 13. Acronyms and abbreviations

Acronym	Definition
ADC	analog-to-digital converter
BGA	ball grid array
BOM	bill of materials

Table 13. Acronyms and abbreviations...*continued*

Acronym	Definition
CAN	controller area network
CPU	central processing unit
CSI	camera serial interface
DDR	double data rate
DRAM	dynamic random-access memory
DSI	display serial interface
eMMC	embedded multi-media card
FlexIO	flexible input/output
I^2C	inter-integrated circuit
I/O	input/output
IOMUX	input-output multiplexer
LDO	low dropout
LVDS	low voltage differential signaling
MIPI	mobile industry processor interface
MIPI-DSI	mobile industry processor interface-display serial interface
NDA	non-disclosure agreement
PCB	printed-circuit board
PHY	physical interface of the OSI model
PMIC	power management integrated circuit
QFN	quad flat no lead
RAM	random-access memory
ROM	read-only memory
SAI	synchronous audio interface
SoC	system-on-chip
S/PDIF	sony/philips digital interconnect format
SPI	serial peripheral interface
SW	software
UART	universal asynchronous receiver/transmitter
USB	universal serial bus
WLCSP	wafer level chip scale package

7 Revision history

Table 14 summarizes revisions to this document.

Table 14. Revision history

Revision number	Date	Description
AN14012 v1.0	22 November 2024	Initial public version

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