AN13792

How to Enable an Asynchronous Interrupt and Wake up from a Low-power Mode

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Document information

Information	Content
Keywords	AN13792, RT1180, low power, wake up, asynchronous interrupt
Abstract	This application note introduces how to use an asynchronous interrupt to wake up the system from a low-power mode.

1 Introduction

The i.MX RT1180 crossover MCU family includes a GB Time Sensitive Networking (TSN) switch to enable real-time rich networking integration that handles both time-sensitive and industrial real-time communication. The i.MX RT1180 supports multiple protocols, bridging communications between real-time Ethernet and industry 4.0 systems. For ultimate design flexibility, this family includes:

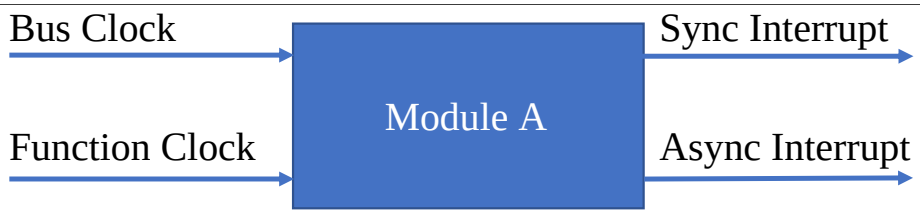
- A state-of-the-art EdgeLock secure enclave
- A dual-core architecture with both an 800 MHz Cortex-M7 and a 240 MHz Cortex-M33

Low power is also a key point on RT1180. This application note introduces how to use an asynchronous interrupt to wake up the system from a low-power mode.

2 Synchronous and asynchronous interrupts

The definitions of synchronous and asynchronous interrupts are as below:

- Synchronous interrupt: The interrupt generated with bus clock, with the abbreviation of **Sync interrupt** used below.
- Asynchronous interrupt: The interrupt generated without bus clock, with the abbreviation of **Async interrupt** used below.



Bus Clock	Function Clock	Sync Interrupt	Async Interrupt
Enabled	Enabled	Y	—
Disabled	Enabled	N	Y

Figure 1. Clock and interrupt diagram

Figure 1 shows a clock and interrupt diagram. For some low-power-mode cases, the bus clock is shut down. To wake up the whole system from those low-power mode cases, the asynchronous interrupt can be used. Meanwhile, make sure that the power supply of this module is turned on during the low-power mode.

Many peripherals support the Async interrupt. To check whether a peripheral supports asynchronous interrupt, see the interrupt chapter in Reference Manual.

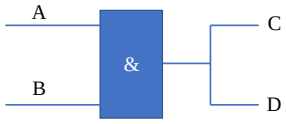
Table 1. Clock and interrupt diagram

19	LPUART1	OR	TX interrupt
19		OR	Async TX interrupt
19		OR	RX interrupt
19		OR	Async RX interrupt
57	GPIO2	OR	Interrupt 0
57		OR	Async interrupt 0

3 Enable asynchronous interrupts

The Async interrupt is not enabled when the bus clock is disabled. To enable the Async interrupt, configure some registers. There is a handshake step before entering a low-power mode. The purpose of handshake is to ensure that before the CPU issues a low-power instruction WFI, all peripherals complete all transmissions and no longer receive new transmissions. Then, it safely enters the low-power consumption. When the handshake is completed, the asynchronous interrupt function is automatically enabled.

If a peripheral is not assigned to a domain, the handshake must complete in two registers. Send the `stop_requset` from M33 side (`GPR_SHARED8` and `GPR_SHARED9`) and M7 side (`GPR_SHARED12` and `GPR_SHARED13`). When both `stop_request` are sent and the peripheral completes all transmissions, the `stop_ack` signal is asserted.



A	B	C	D
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

A: CAN1_STOP_REQ from GPR_SHARED8

B: CAN1_STOP_REQ from GPR_SHARED12

C: CAN1_STOP_ACK from GPR_SHARED_STATUS1

D: CAN1_STOP_ACK from GPR_SHARED_STATUS5

NOTE: Assuming the peripheral completed transmissions

Figure 2. Handshake

Take CAN1 as an example. Send the `CAN1_STOP_REQ` from `GPR_SHARED8 bit[24]` and `GPR_SHARED12 bit[24]`:

```
CCM->GPR_SHARED_CTRL[8].GPR_SHARED |= 1<<24;
CCM->GPR_SHARED_CTRL[12].GPR_SHARED |= 1<<24;
```

Then, check whether the transmission completes or not. Check `GPR_SHARED_STATUS1 bit[3]` and `GPR_SHARED_STATUS5 bit[3]`:

```
while((CCM->GPR_SHARED_STATUS[1] & 0x8) == 0); //Check bit3
while((CCM->GPR_SHARED_STATUS[5] & 0x8) == 0); //Check bit3
```

If a peripheral is assigned to a domain, send only one `stop_request`. Take CAN1 as an example. Assign CAN1 to CM33 domain and send the `CAN1_STOP_REQ` from `GPR_SHARED8 bit[24]`:

```
CCM->GPR_SHARED_CTRL[8].GPR_SHARED |= 1<<24;
```

Then, check whether the transmission completes or not. Check `GPR_SHARED_STATUS1 bit[3]`:

```
while((CCM->GPR_SHARED_STATUS[1] & 0x8) == 0); //Check bit3
```

Before entering a low-power mode, make sure that all the peripherals have completed transmissions. Take care of the handshake sequence. DMA/ENET (bus masters) completes the handshake first and then flash/memories (bus slaves). Based on this, enable the Async interrupt.

4 Example: Enable a GPIO async interrupt

Take RGPIO4 on RT1180 as an example, when RT1180 enters the Sleep mode, all of the bus on RT1180 shut down the async interrupt and can be used as the wake-up source. After configuring the GPIO interrupt function, users can use the following code to enable the async interrupt. After the handshake steps, CPU cannot configure GPIO, so it is more appropriate to call the handshake step before WFI.

```
void gpio_async_config()
{
 CCM->GPR_SHARED_CTRL[8].GPR_SHARED |= 1<<19;
 CCM->GPR_SHARED_CTRL[12].GPR_SHARED |= 1<<19;
 while((CCM->GPR_SHARED_STATUS[0] & (1<<19)) == 0); //Check bit19
 while((CCM->GPR_SHARED_STATUS[4] & (1<<19)) == 0); //Check bit19
}
```

When GPIO wakes up the system, clean the interrupt flag by operating the GPIO register. As mentioned above, CPU cannot configure the GPIO4 after the handshake step. So before clearing the GPIO interrupt flag, users must **Cancel the handshake** and restore from Stop mode to Run mode. Then, CPU can configure the GPIO.

```
void GPIO4_0_IRQHandler()
{
 CCM->GPR_SHARED_CTRL[8].GPR_SHARED &= ~(1<<19);//Cancel handshake first
 CCM->GPR_SHARED_CTRL[12].GPR_SHARED &= ~(1<<19); //Cancel handshake first
 RGPIO_ClearPinsInterruptFlags(RGPIO4, 0, 1 <<16); //Clean the interrupt flag
 SDK_ISR_EXIT_BARRIER;
}
```

5 Note about the source code in the document

Example code shown in this document has the following copyright and BSD-3-Clause license:

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6 Revision history

Table 2 summarizes the revisions to this document.

Table 2. Revision history

Document ID	Release date	Description
AN13792 v.1	27 May 2024	Initial public release

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