AN13227

Hardware Design Considerations for KW45B41Z and K32W148 Bluetooth LE Devices

Rev. 2 — 8 June 2023 Application note

Document Information

Information	Content
Keywords	Bluetooth LE devices, KW45, K32W148
Abstract	This application note describes printed-circuit board (PCB) design considerations for the KW45B41Z83AFTA, and KW45B41Z82AFTA and K32W1480VFTAT MKW35A, MKW36A, MKW35Z, and MKW36Z 40-pin HVQFN (6x6) and 48-pin Laminated QFN (HVLQFN-7x7 pitch 0.5 mm) wettable flank) package and KW45B41Z83AFPA and KW45B41Z82AFPA MKW35A, MKW36A, MKW35Z, and MKW36Z 40-pin HVQFN (6x6) and 40-pin Laminated QFN (HVLQFN-6x6 pitch 0.5 mm) wettable flank) package

1 Introduction

This application note describes printed-circuit board (PCB) design considerations for the following packages:

- KW45B41Z83AFTA, and KW45B41Z82AFTA and K32W1480VFTAT MKW35A, MKW36A, MKW35Z, and MKW36Z 40-pin HVQFN (6x6) and 48-pin Laminated QFN (HVLQFN-7x7 pitch 0.5 mm) wettable flank) package.
- KW45B41Z83AFPA and KW45B41Z82AFPA MKW35A, MKW36A, MKW35Z, and MKW36Z 40-pin HVQFN (6x6) and 40-pin Laminated QFN (HVLQFN-6x6 pitch 0.5 mm) wettable flank) package.
- Included are layouts of the component copper layer, solder mask, and solder paste stencil.

These recommendations are only intended as guidelines. Depending on the assembly house used and the other components on the board, these recommendations may have to be amended.

2 QFN component copper layer

2.1 48-pin HVQFN

Figure 1 shows a recommended component copper layer. This layer is also called the *top metal layer* and the components are soldered to this layer. The footprint for the 48-pin “wettable” HVQFN package (7x7x0.85 mm) consists of 48 IC contact pads and 9 centered ground pads. The copper pattern is shown in Figure 1.

Use 0.25 mm via holes to connect to the ground plane layers. They are required for RF grounding and help to prevent solder float.

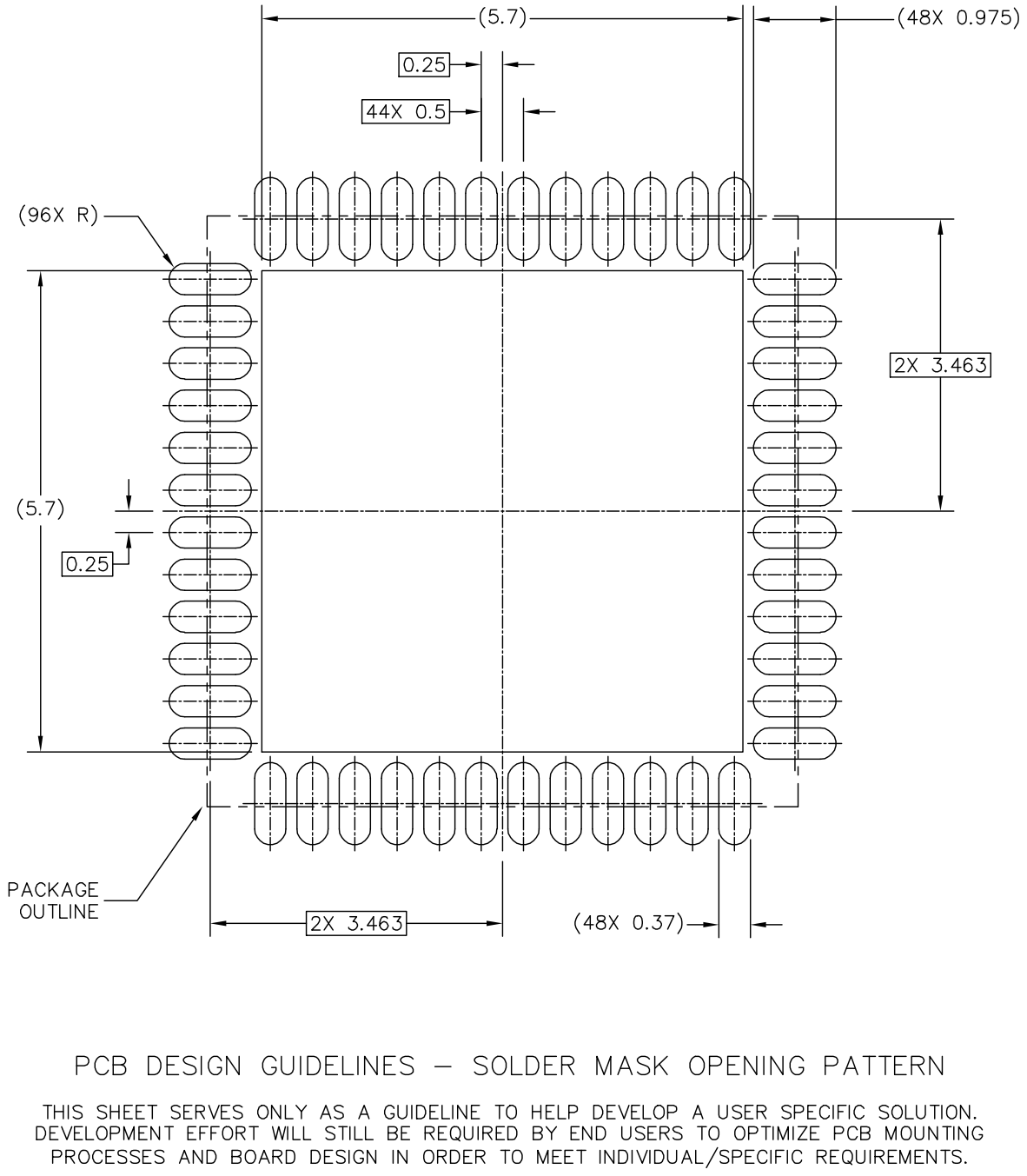


Figure 1. 48-pin HVQFN component solder mask opening pattern

2.1.1 48-pin HVQFN solder mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 2 shows a recommended solder mask pattern. The pattern represents openings in the solder mask.

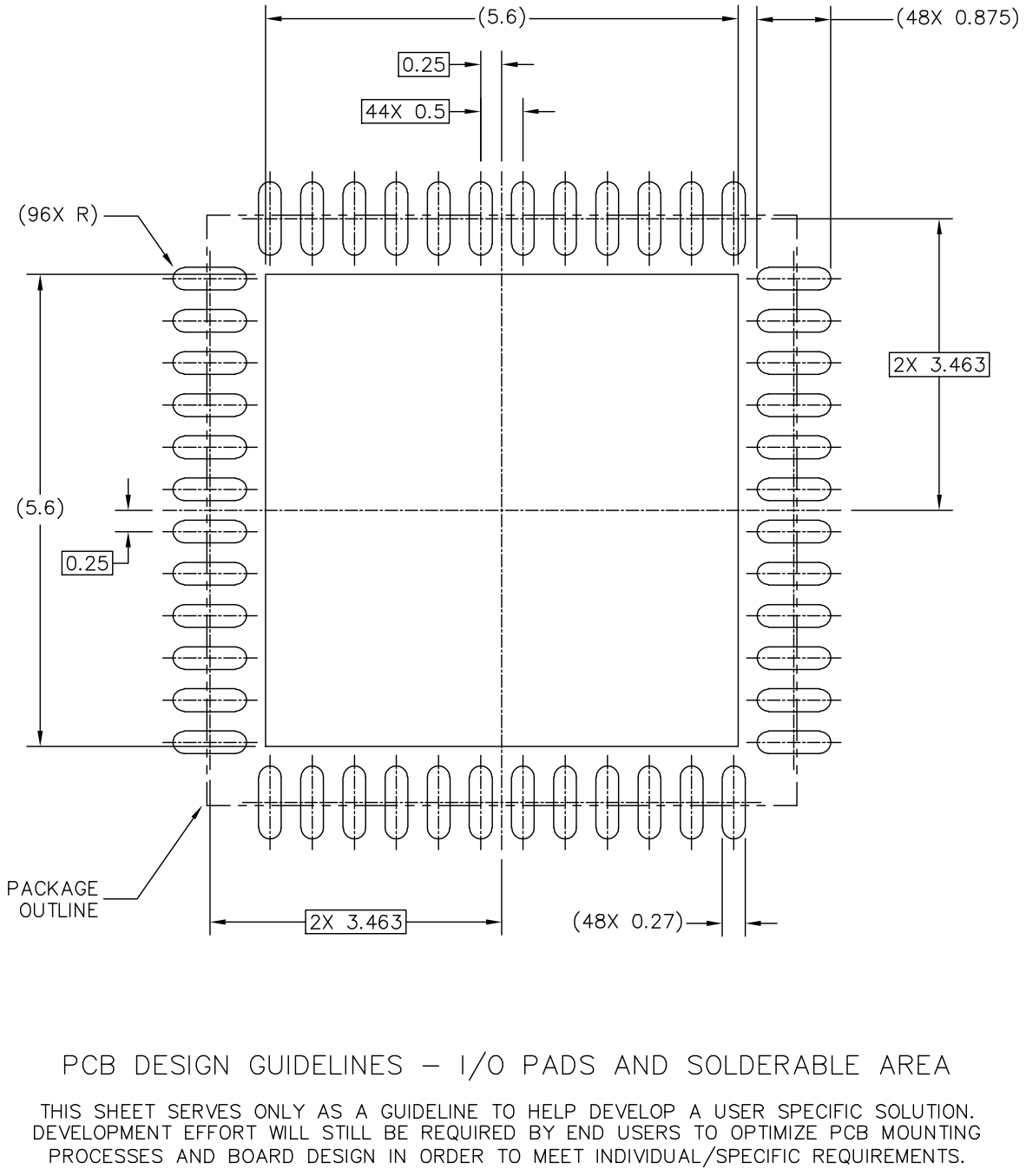


Figure 2. 48-pin HVQFN I/O pads and solderable area

2.1.2 48-pin HVQFN solder paste stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 3 shows a recommended solder stencil pattern. Stencil thickness should be approximately 0.1 mm.

If too much solder is being applied, alternate patterns and opening sizes can be used. For more information, see the following section.

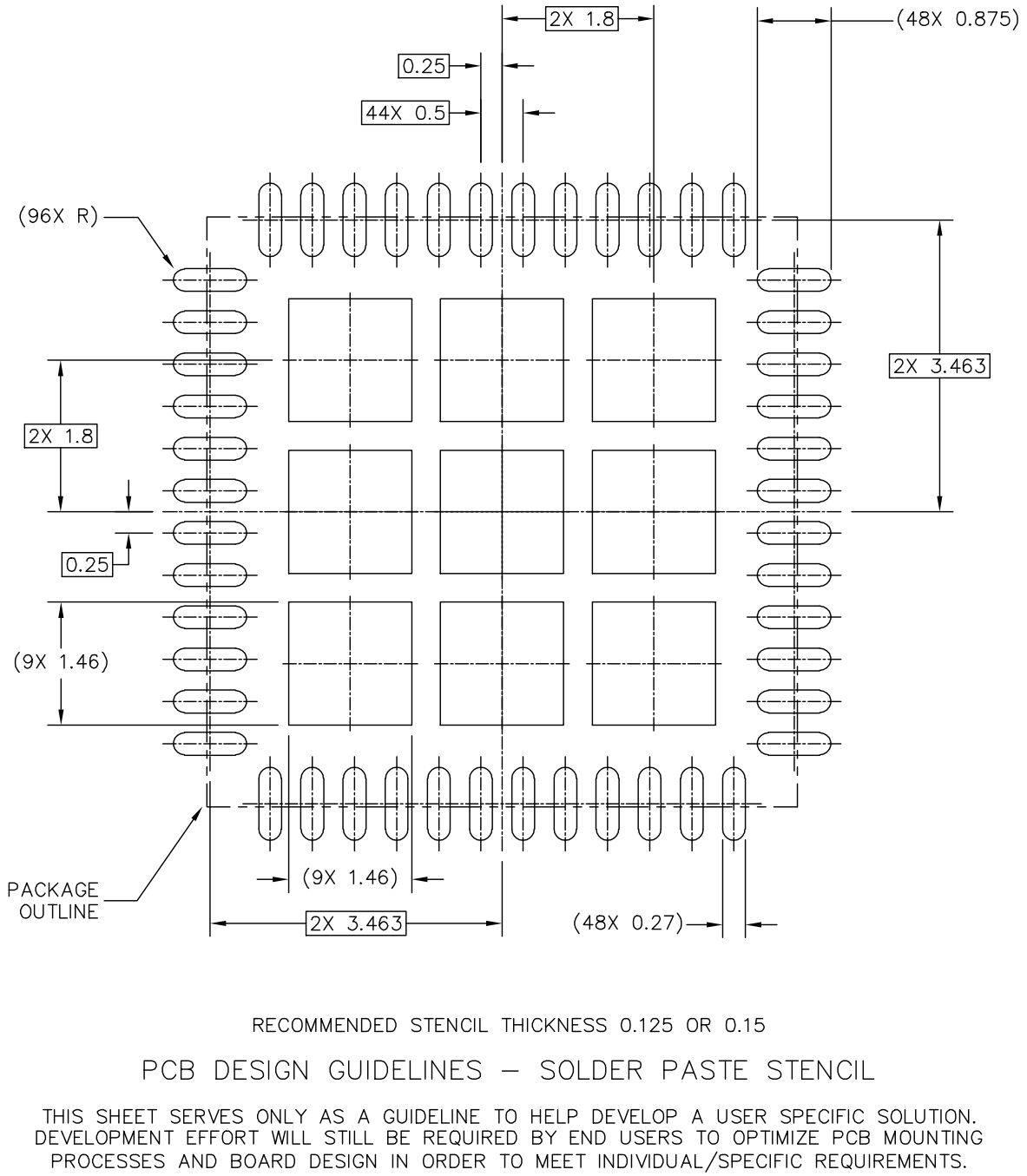


Figure 3. 48-pin HVQFN solder paste stencil

2.2 40-pin HVQFN

Figure 4 shows a recommended component copper layer. This layer is also called the *top metal layer* and the components are soldered to this layer. The footprint for the 40-pin “wettable” HVQFN package (6x6x0.85 mm) consists of 40 IC contact pads and 16 centered ground pads. The copper pattern is shown in Figure 4.

Use 0.25 mm via holes to connect to the ground plane layers. They are required for RF grounding and help to prevent solder float.

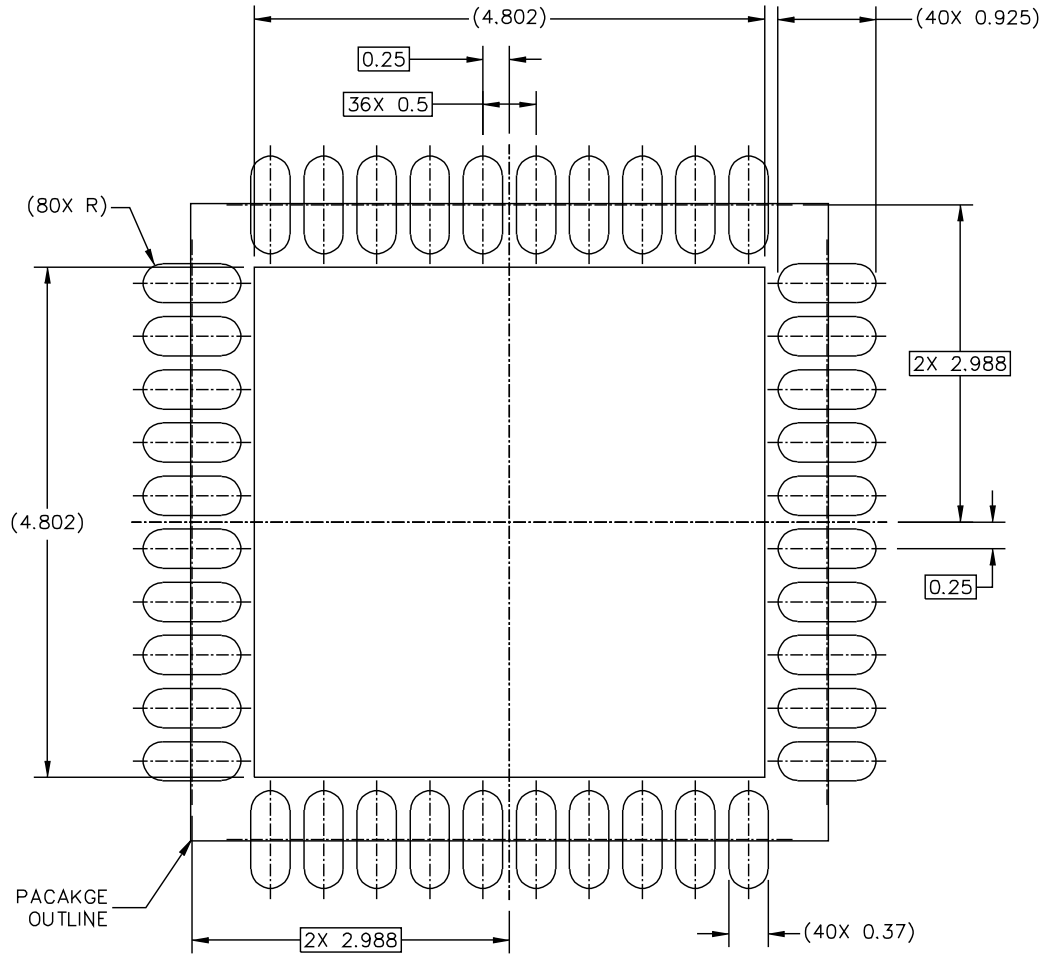


Figure 4. 40-pin HVQFN component solder mask opening pattern

2.2.1 40-pin HVQFN solder mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 5 shows a recommended solder mask pattern. The pattern represents openings in the solder mask.

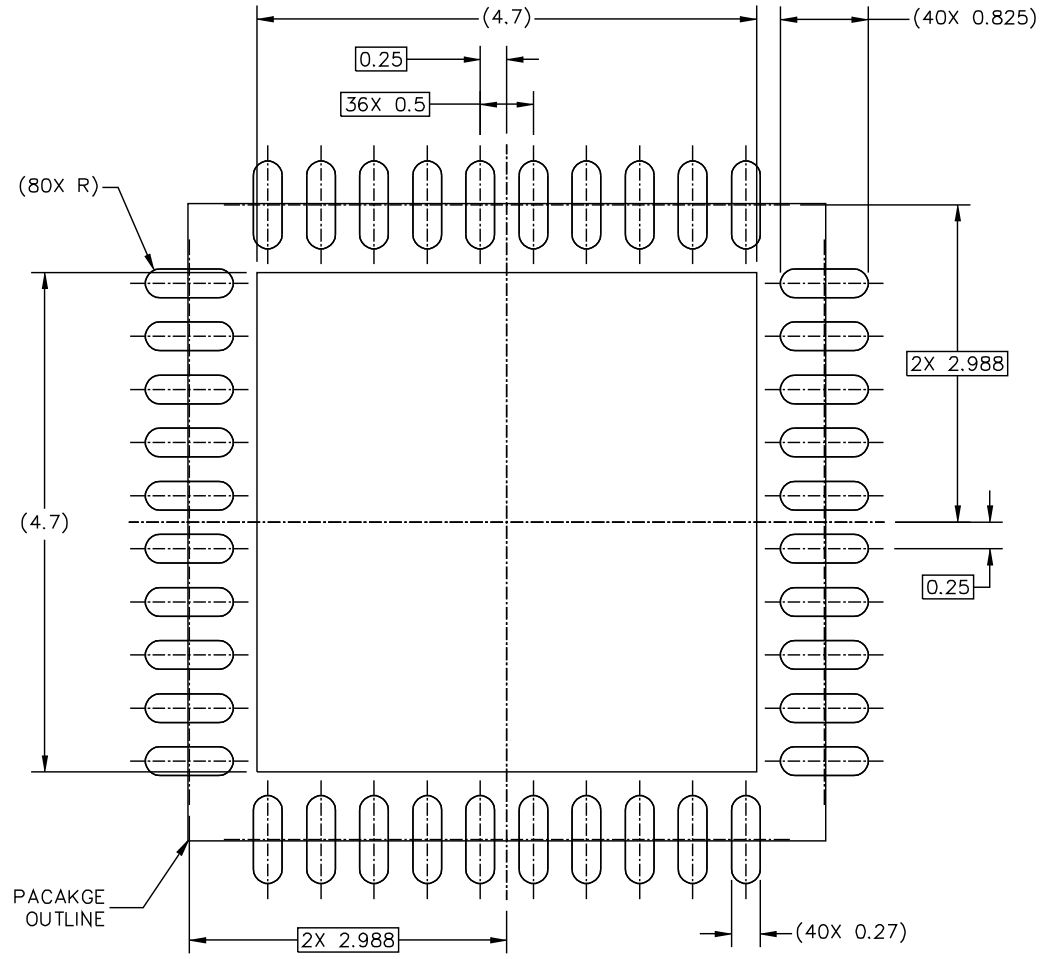


Figure 5. 40-pin HVQFN I/O pads and solderable area

2.2.2 40-pin HVQFN solder paste stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 6 shows a recommended solder stencil pattern. Stencil thickness should be approximately 0.1 mm.

If too much solder is being applied, alternate patterns and opening sizes can be used. For more information, see the following section.

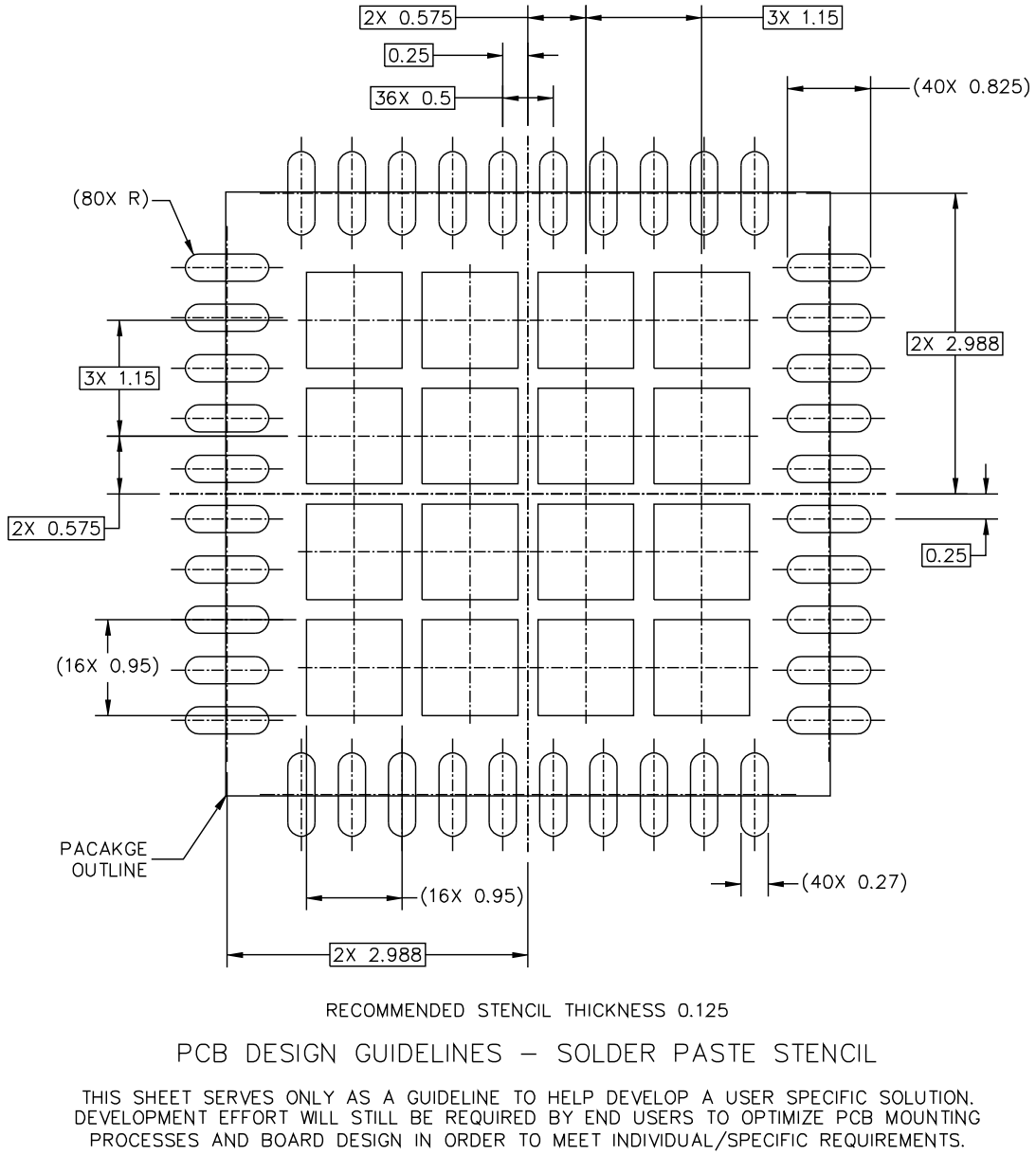


Figure 6. 40-pin HVQFN solder paste stencil

2.3 QFN problems with excess solder

Excess solder may cause the QFN to float or bridge between the package contacts. To apply correct amount of solder paste to the PCB, consider the following:

- Stencil thickness
- Other components mounted on the PCB
- Manufacturing equipment
- Assembly house experience

3 QFN package dimensions

3.1 48-pin HVQFN package

Figure 7 shows the 48-pin HVQFN package dimensions.

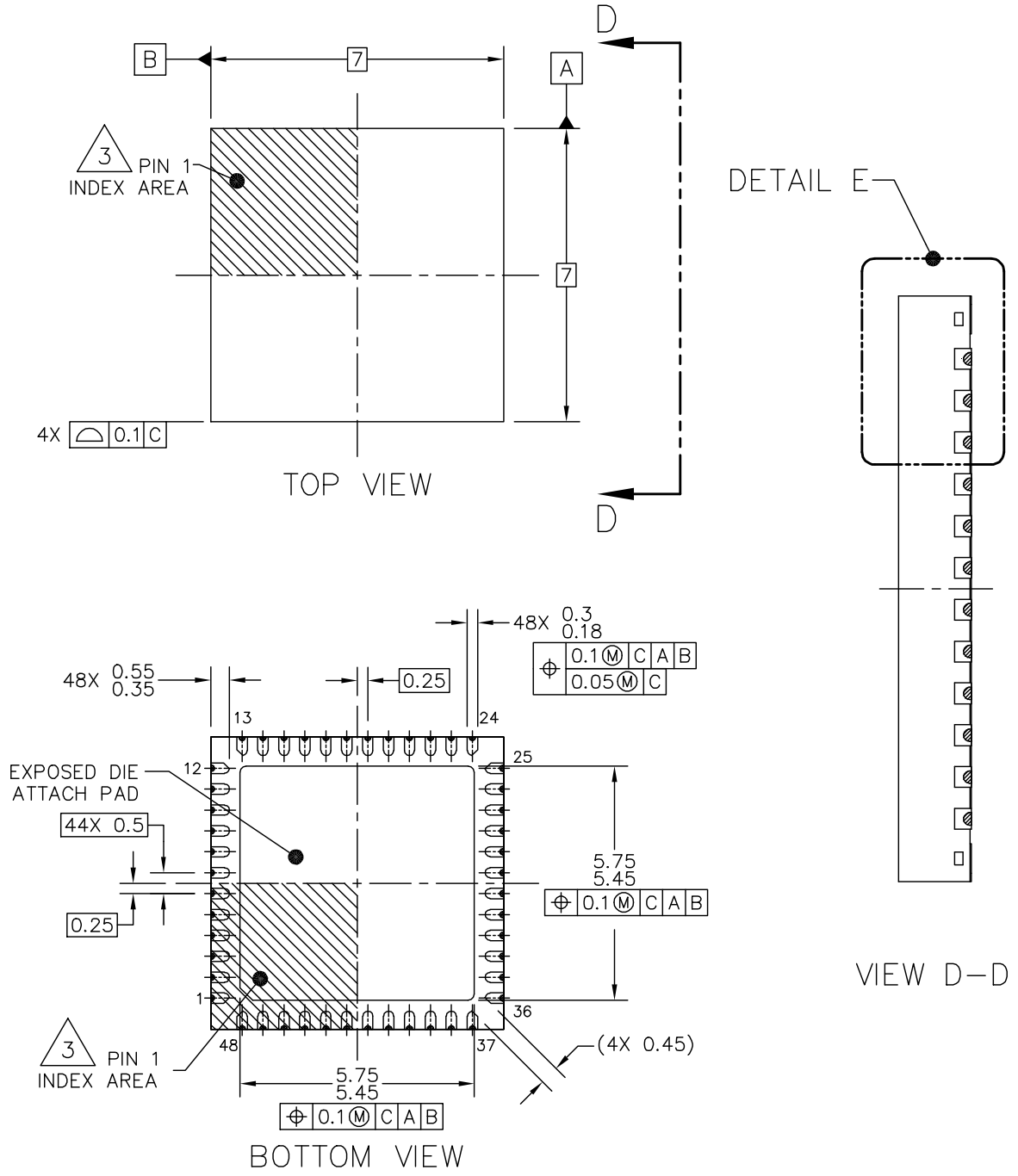


Figure 7. 48-pin HVQFN package dimensions

3.1.1 48-pin HVQFN device marking details

The *KW45B41Z83AFTA* and *KW45B41Z82AFTA* devices are in the 48-pin HVQFN (7x7x0.85 mm pitch 0.5 mm). Figure 8 shows device marking examples for the HVQFN device.

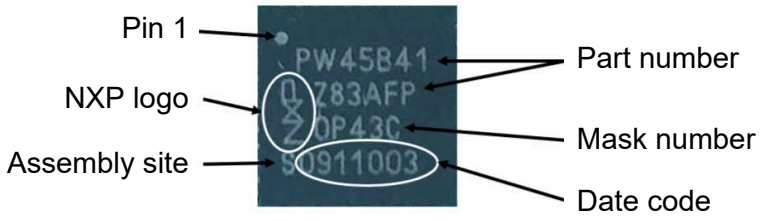


Figure 8. 48-pin HVQFN device marking

Figure 9. PK32W148 device

Note:

Your device part number may differ from the part number shown in Figure 8.

The K32W1480 device is in the 48-pin HVQFN (7x7x0.85 mm pitch 0.5 mm).

3.2 40-pin HVQFN package

Figure 10 shows the 40-pin HVQFN package dimensions.

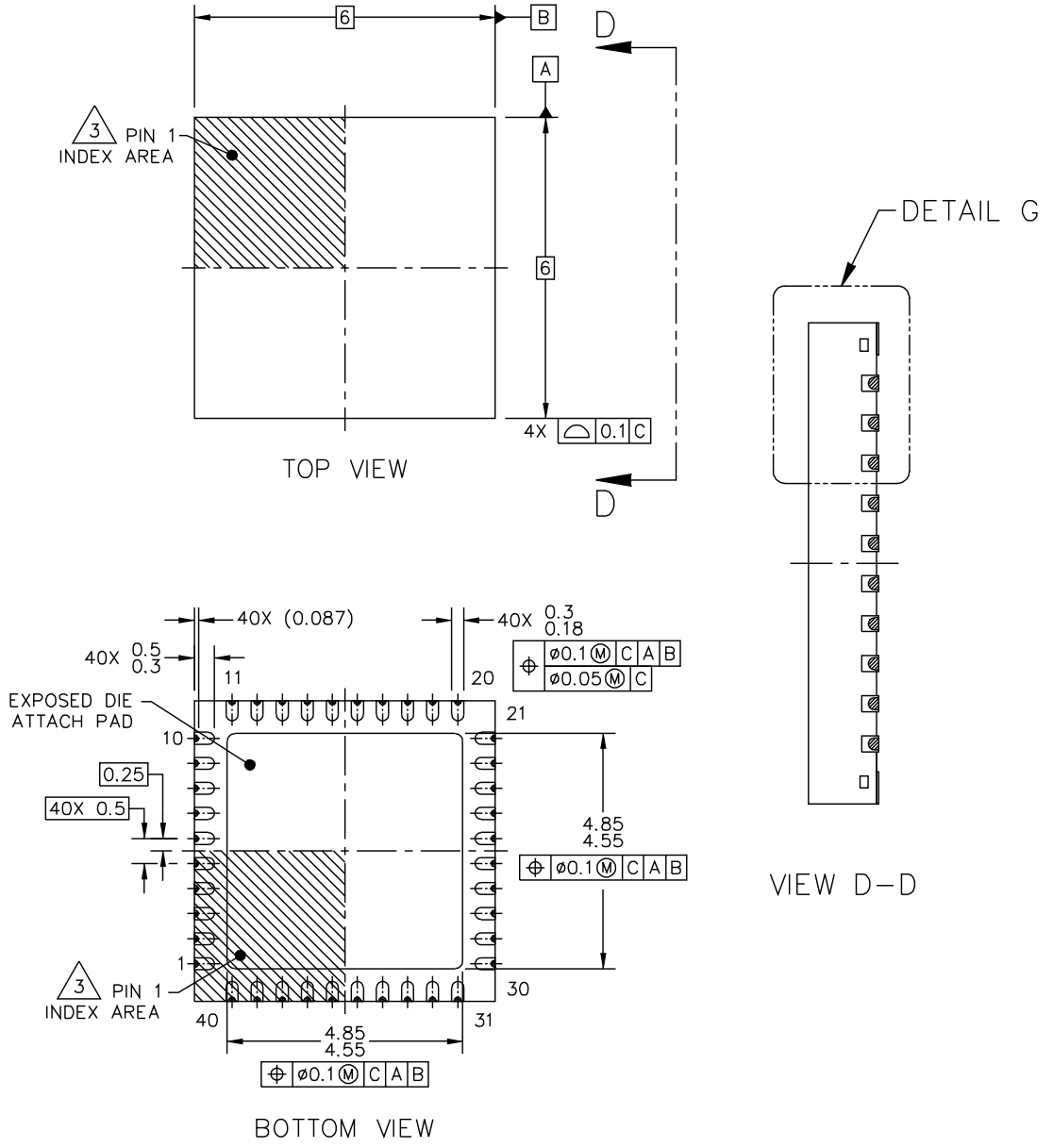


Figure 10. 40-pin HVQFN package dimensions

3.2.1 40-pin HVQFN device marking details

The *KW45B41Z83AFPA* and *KW45B41Z82AFPA* devices are in the 40-pin HVQFN (6x6x0.85 mm pitch 0.5 mm) package. Figure 11 shows device marking examples for the HVQFN device.

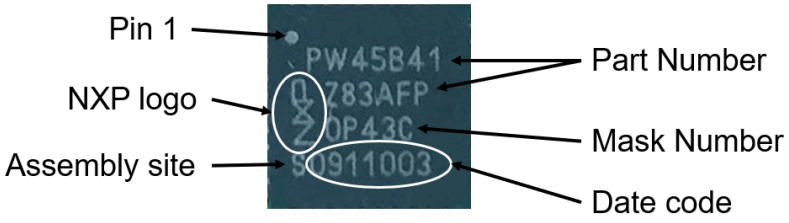


Figure 11. 40-pin HVQFN device marking

Note: *Your device part number may differ from the part number shown in Figure 11.*

4 QFN soldering profile

Figure 12 shows a recommended soldering profile for a 48-pin HVQFN package in a board size of approximately 3.20 inches × 2.10 inches.

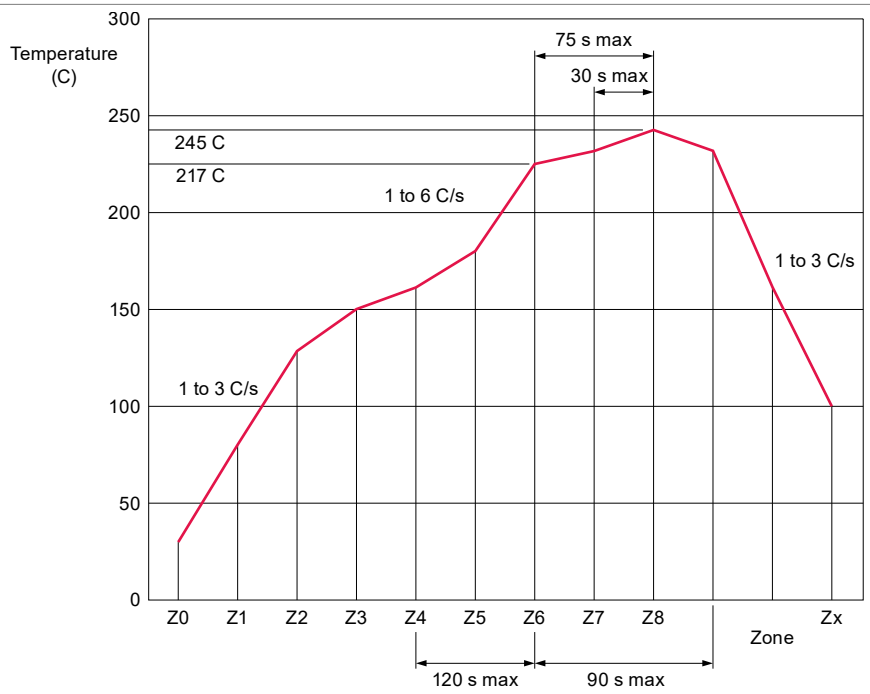


Figure 12. QFN soldering profile

5 Design and board layout considerations

To have a successful wireless hardware development, the proper device footprint, RF layout, circuit matching, antenna design, and RF measurement capability are essential. RF circuit design, layout, and antenna design are specialties requiring investment in tools and experience. With available hardware reference designs from NXP, RF design considerations, and the guidelines contained in this application note, hardware engineers can successfully design Bluetooth LE radio boards with good performance levels. Figure 13 shows the **KW45B41Z** and **K32W148** Evaluation Kit (EVK), containing the KW45B41Z device and all necessary I/O connections.

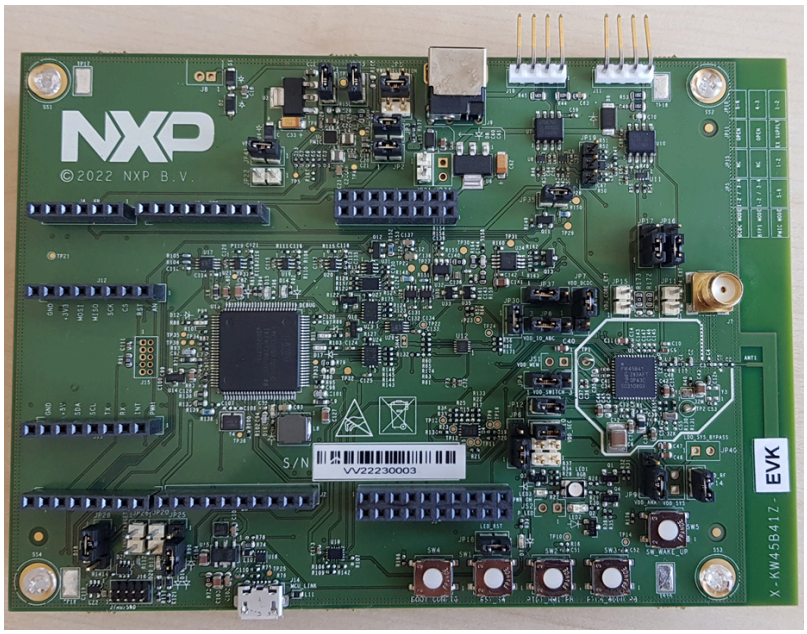


Figure 13. KW45B41Z and K32W148 development board

The device footprint and layout are critical and the design implementation affects the RF performance. For these reasons, using NXP recommended RF hardware reference designs are important for successful board performance. Additionally, the reference platforms are optimized for radio performance. If the recommended footprint and design are followed exactly in the RF region of the board, then the sensitivity, output power, harmonic and spurious radiation, and range have a high likelihood of first-time success.

The following subsections describe important considerations when implementing a wireless hardware design starting with the device footprint, RF circuit implementation, and antenna selection. Figure 14 shows an example of a typical layout with the critical RF section, which must be copied exactly for optimal radio performance. The less critical layout area can be modified without reducing radio performance.

Note: *Exact dimensions are not given in this document, but can be found in the design files for the* ***KW45B41Z and K32W148*** *board.*

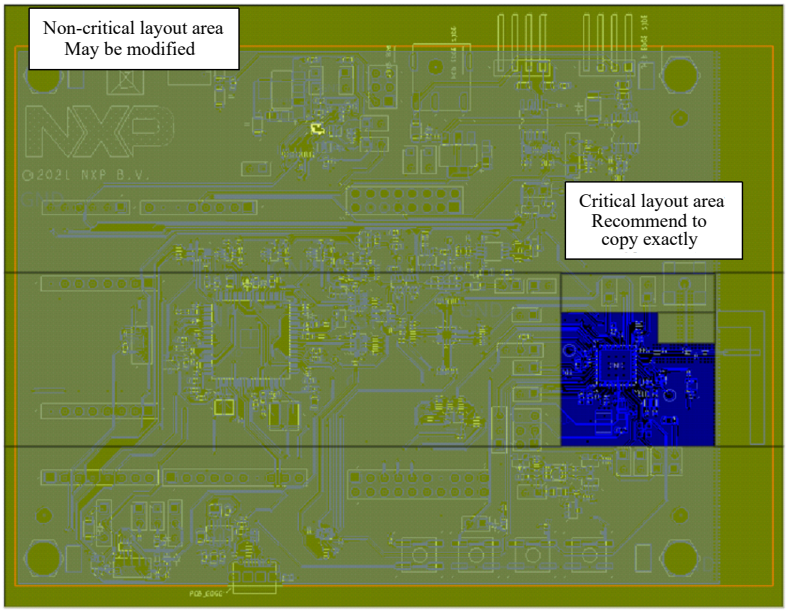


Figure 14. Critical layout areas

5.1 KW45/K32W148 device footprint

The footprint of the device largely influences the performance of the wireless link. As a result, a great deal of care has been put into creating a footprint so that receiver sensitivity and output power are optimized to enable board matching and minimal component count. NXP highly recommends copying the die flag exactly as it is shown in Figure 15, including via locations. Deviation from these parameters can cause performance degradation.

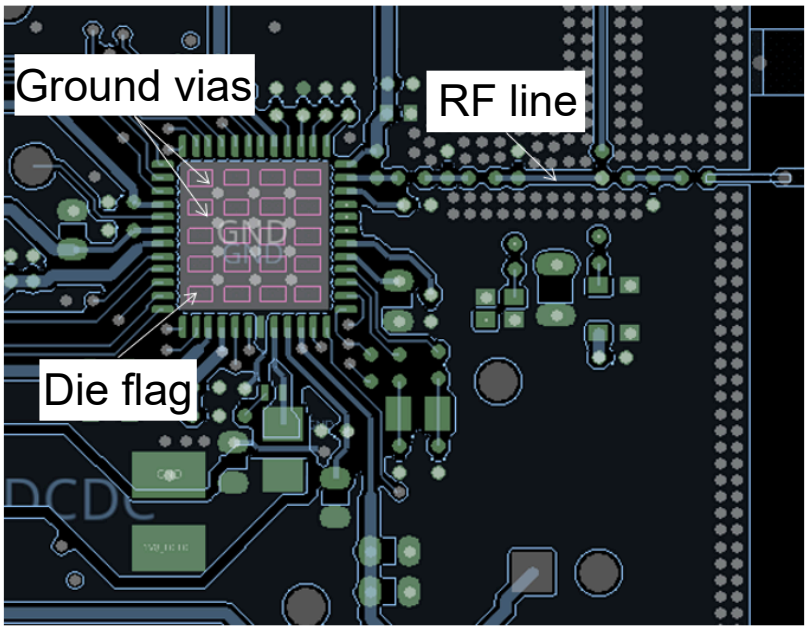


Figure 15. Critical layout of die flag area

The critical areas of the device die flag are as follows:

- Ground vias and locations
- RF output and ground traces
- Die flag shape
- Test pins

As shown in Figure 15 for transmission lines, it is important to copy not just the physical layout of the circuit, but also the PCB stackup. Any small change in the thickness of the dielectric substrate under the transmission line has a significant change in impedance. All this information can be found in the fabrication notes for each board design. As an illustration, consider a 50 Ω trace that is 18 mils wide over 10 mils of FR4. If that thickness of FR4 is changed from 10 to 6 mils, the impedance is only about 36 Ω.

When the top layer dielectric becomes too thin, the layers do not act as a true transmission line, even though all the dimensions are correct. There is no universal industry agreement on the thickness at which this occurs, but NXP prefers to use a top layer thickness of no less than 8-10 mils. The use of a correct substrate like the FR4 with a dielectric constant of 4.3 helps you to achieve a good RF design.

A possible way to improve and reach acceptable EMC during the radio certification is as follows:

- A specific attention must be taken on four pins, PTC0, 1, 2, and 3, if they are used in the application.
- Four decoupling capacitors of 3 pF are mandatory on those pins and they should be positioned closely to the KW45 pins.
- Wires from those four pins must be under-layer.
- If the customer hardware design rules allow it, NXP recommends putting the vias under the KW45 package.

Figure 16 shows an example of the recommended layout:

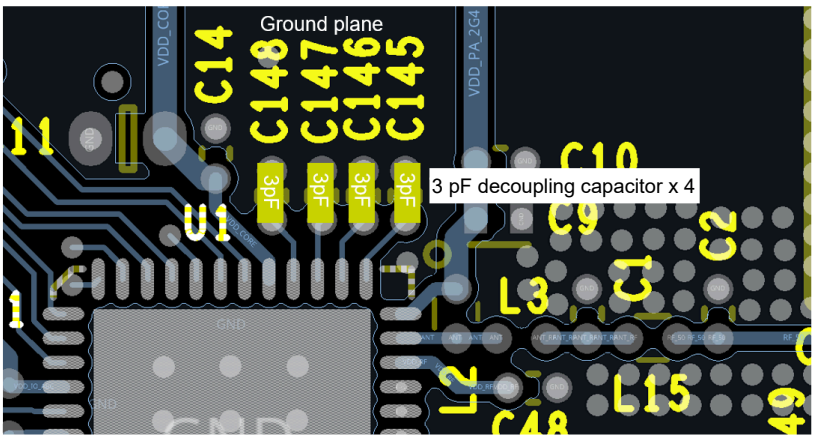


Figure 16. EMC layout recommendation

The recommendations to design a good DC-DC supply layout are as follows:

1. **C38** and **C39** must be as close as possible to the DC-DC VDD but not so much to the DC-DC VSS. Place them with the LX connection to the inductor passing between their terminals. It is critical to reduce the loop formed by the DC-DC VDD/VSS pins and those capacitors. Add more vias to the ground plane.
2. Place **C7** in a way that its connection to inductor L1 is where it is now and the VSS connection gets close to the chip. To connect the VSS to the ground plane better, add vias.
3. Move **C6** closer to the IC and add vias, as shown in this example.
4. Similar to**C7**, **C8** may be helpful for emissions over 300 MHz.
5. **L1** is 1 µH for KW45//K32W148 instead of10 µH on the KW35/36/37/38/39 reference design.

Note: *The most important thing to contain emissions is to have short connection and small area loops. Ensure to bring those caps closer to the chip. Additionally, preserving the ground plane underneath those components as it is on the current layout helps to reduce the effect of the inductor not being really close to the chip.*

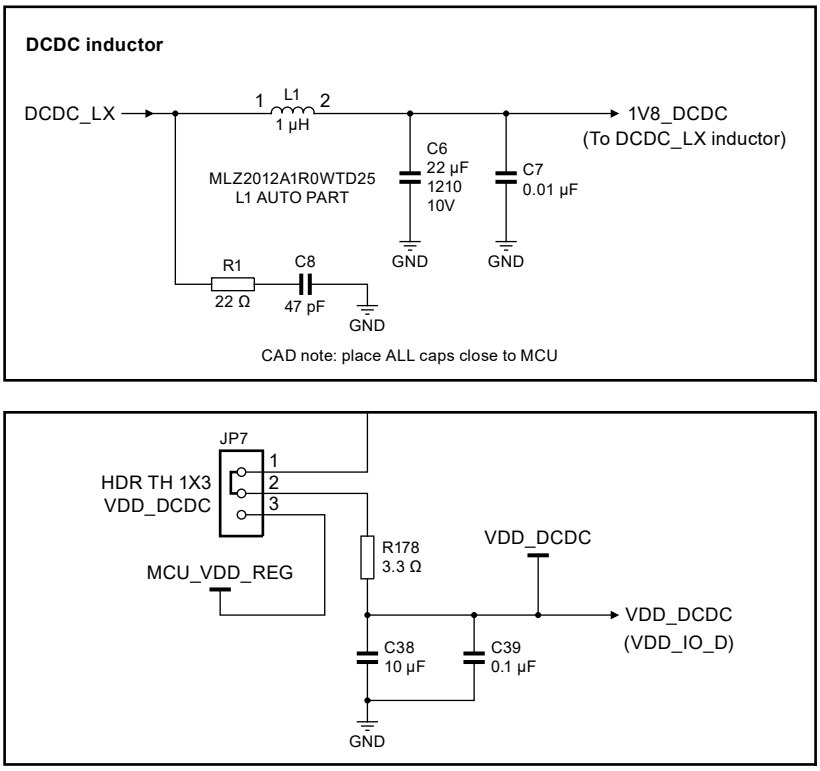


Figure 17. DC-DC supply schematic

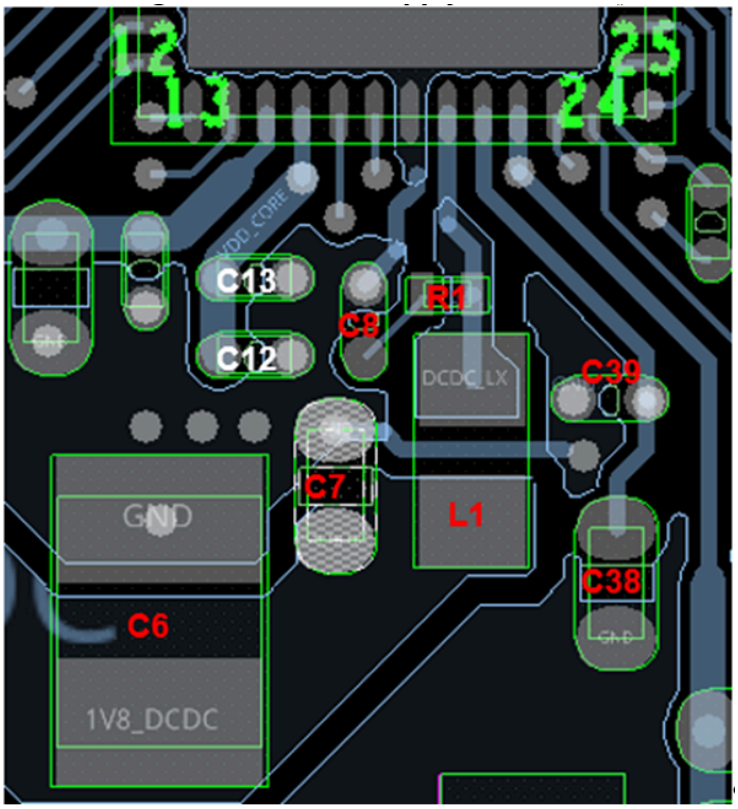


Figure 18. DC-DC supply layout

The recommendations to perform a good radio layout are as follows:

- The value of capacitor **C48** used for an RF short is 12 pF.
- **C10** must be as close to **L2** as possible.
- **C49** = 22 µF on VDD_RF can be placed as DNP.
- The pullup inductor **L2** placement must follow the layout example.
- The antenna-matching components must be close to the DUT and each other, as on the current layout.
- For the best isolation, place **C48** with the ANT_RF line.
- The VDDRF line must be isolated with VDDRF_line. Copy the current layout.
- Isolate the VDDRF and UART signals.
- Isolate VDD_PA_2P4GHZ from PTC0.
- The power planes that create huge fat nets are for VDD_ANA and VDD_SYS. There is no benefit from reducing the power plane.

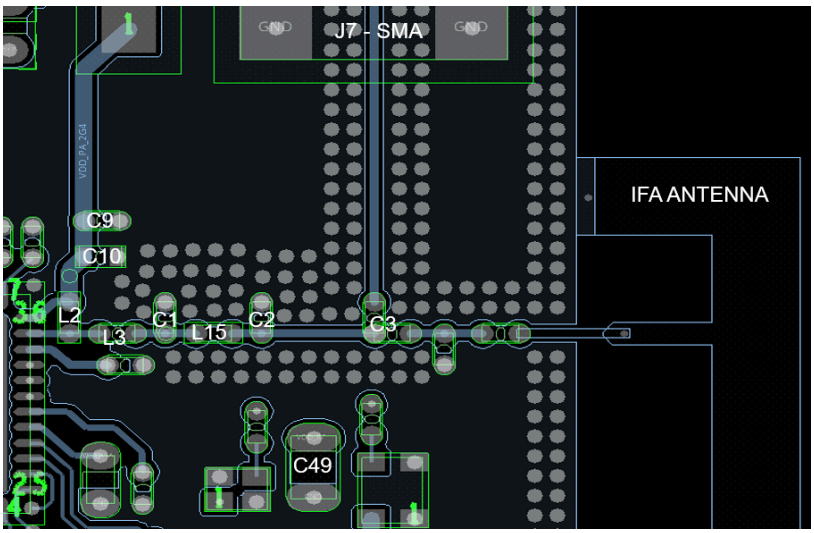


Figure 19. Radio layout

The recommendations to perform a good crystal layout are as follows:

- The 32 MHz and 32 kHz wire lengths must be as symmetric as possible.
- The 32 kHz quartz and DUT (KW45/K32W148) are not required to be as close as possible.

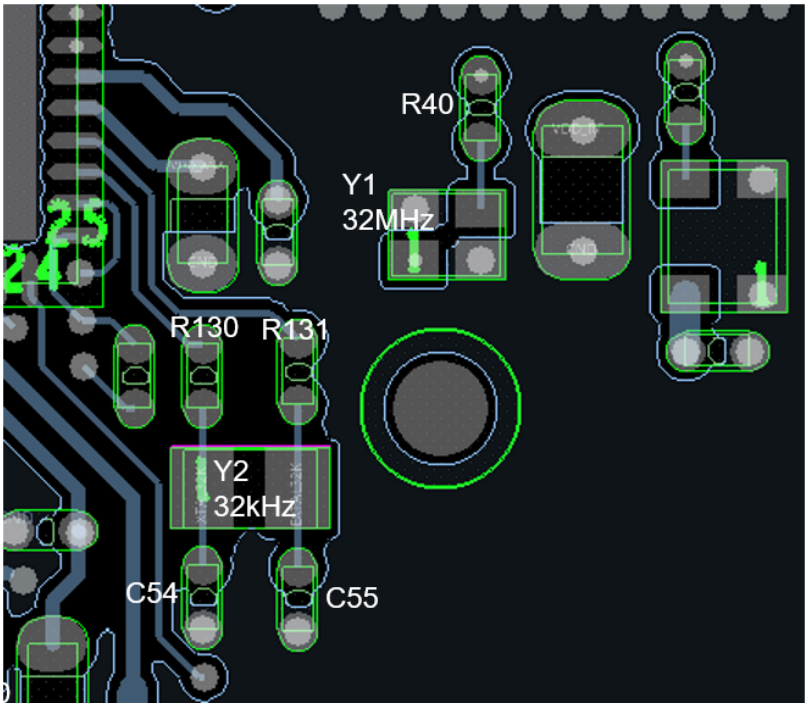
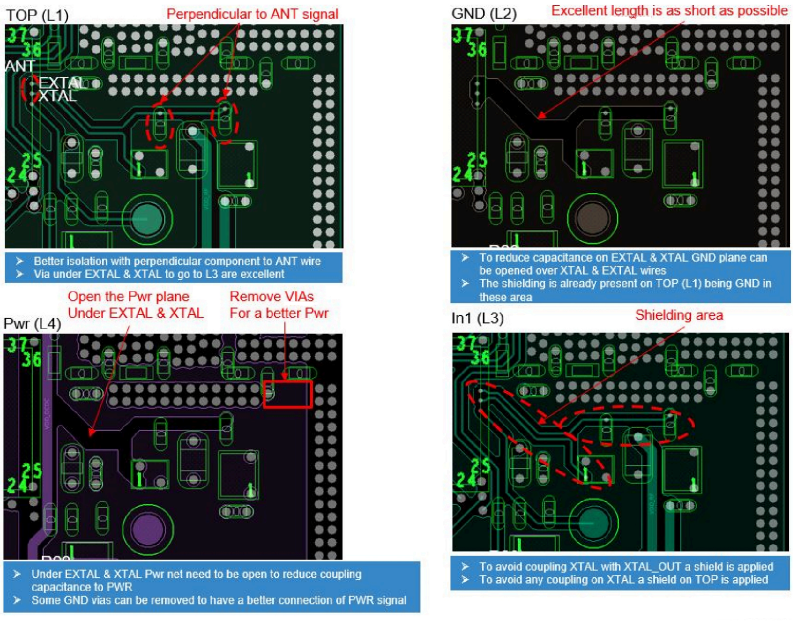


Figure 20. Crystal layout

Figure 21 shows additional layout recommendation around the 32 MHz crystal:



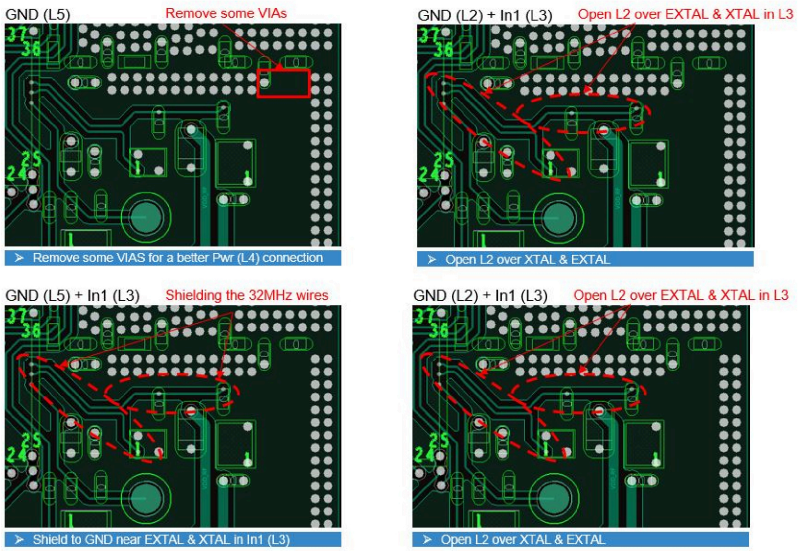


Figure 21. 32 MHz crystal

5.1.1 RF circuit topology and matching

Transmission lines have several shapes, such as microstrip, coplanar waveguide, and stripline. For Bluetooth LE applications built on FR4 substrates, the types of transmission lines typically take the form of microstrip or coplanar waveguide (CPW). The dielectric constant of the board material, trace width, and the board thickness between the trace and the ground define these two structures.

For CPW, the gap between the trace and the top edge ground plane, define the transmission line. These parameters are used to define the characteristic impedance of the transmission line (trace) that is used to convey the RF energy between the radio and the antenna.

KW45 has a single-ended RF output with a two component matching network composed of a shunt capacitor and a series inductor. These two elements transform the device impedance to 50 Ω. The value of these components may vary depending on your specific board layout. The recommended RF-matching network is shown in Figure 22.

Avoid routing traces near or parallel to RF transmission lines or crystal signals. Maintaining a continuous ground under an RF trace is critical to maintain the characteristic impedance of that trace. Avoid any routing on the ground layer that results in disrupting the ground under the RF traces.

Complexity is the main factor that determines whether the design of an application board can be two-layer, four-layer, or more. The recommended board stackup for either a two-layer or four-layer board design is as follows:

- Two-layer stackup:
  - Top: RF routing of transmission lines, signals, and ground
  - Bottom: RF reference ground, signal routing, and general ground
- Four-layer stackup:
  - Top: RF routing of transmission lines
  - L2: RF reference ground
  - L3: DC power
  - Bottom: Signal routing

For more information, see *NXP IEEE 802.15.4 / ZigBee Package and Hardware Layout Considerations* (document ZHDCRM)

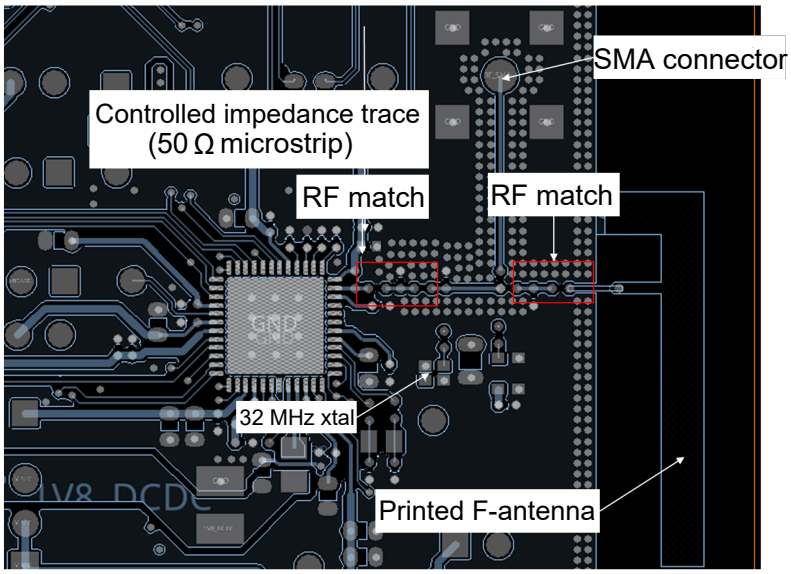


Figure 22. RF matching network

5.2 Antenna considerations

There is a large variety of antenna types to choose from when designing a wireless system. These include small-footprint chip antennas, trace antennas, loop monopole, and dipole. Each of these antennas has their own set of pros and cons, depending on the goal of the application. NXP recommends using proven antenna implementations used in many of our hardware reference designs. For more information on compact antenna designs, see *Compact Integrated Antennas* (document AN2731).

The recommendations for good antenna performance are as follows:

- Be mindful of critical dimensions:
  - Critical dimensions should be copied exactly.
  - The customer final board sizes may differ from the NXP reference designs. As a result, the last leg of the trace antenna must be made longer to allow for final board tuning.
  - Antenna tuning may be required to operate at the proper frequency. The minimum return loss must be centered at 2440 MHz. A 10dB return loss looking into the antenna at the band edges is sufficient for good range and receive sensitivity.
- Antenna impedance is 50 Ω.
  - This is maintained from the RF matched port/pin to the antenna feed.
  - The example uses microstrip topology but you can also use a co-planer waveguide with ground. In this case, the dimensions change, so be careful when changing from one topology to another.
- The antenna should be reasonably clear of metallic objects and oriented properly with the ground plane.
- Always check the antenna in its final environment, including the PCB, components, case enclosure, hand effects (if appropriate), and battery. Plastic and other materials in the near-field may cause detuning.
- Actual antenna performance can be evaluated in various ways.For example, range testing, measuring radiated signal level under controlled conditions, and characteristic testing in an anechoic chamber.

6 Revision history

The Table 1 lists the substantive changes done to this document since the initial release.

Table 1. Revision history

Revision number	Date	Substantive changes
2	7 June 2023	Updated Section 5.1
1	31 January 2023	Replaced "KW455656B41Z" to "KW45B41Z" Multiple editorial changes
0	15 December 2022	Initial release

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Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

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Date of release: 8 June 2023
Document identifier: AN13227