AN11654

BGS8L2 LTE LNA with bypass switch evaluation board

Rev. 1 — 17 July 2015 Application note

Document information

Info	Content
Keywords	BGS8L2, LTE, LNA
Abstract	This document explains the BGS8L2 LTE LNA evaluation board
Ordering info	Board-number: OM17005 12NC: 9340 695 57598
Contact information	For more information, please visit: http://www.nxp.com

Revision history

Rev	Date	Description
1	20150717	First publication

Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

NXP Semiconductors' BGS8L2 LTE LNA Evaluation Board is designed to evaluate the performance of the LTE LNA in its typical application, using:

- NXP Semiconductors' BGS8L2 LTE Low Noise Amplifier
- A matching inductor
- A decoupling capacitor

NXP Semiconductors' BGS8L2 is a low-noise amplifier with bypass switch for LTE receiver applications in a plastic, leadless 6 pin, extremely thin small outline SOT1232 at 1.1 x 0.7 x 0.37mm, 0.4mm pitch. The BGS8L2 features gain of 13 dB and a noise figure of 0.85 dB at a current consumption of 5.2 mA. The Bypass switch insertion loss is 1.9 dB. Its superior linearity performance removes interference and noise from co-habitation cellular transmitters, while retaining sensitivity. The LNA components occupy a total area of approximately 2.5 mm^2.

In this document, the application diagram, board layout, bill of materials, and typical performance are given, as well as some explanations on LTE related RF-parameters like input third-order intercept point IIP3, gain compression and noise.

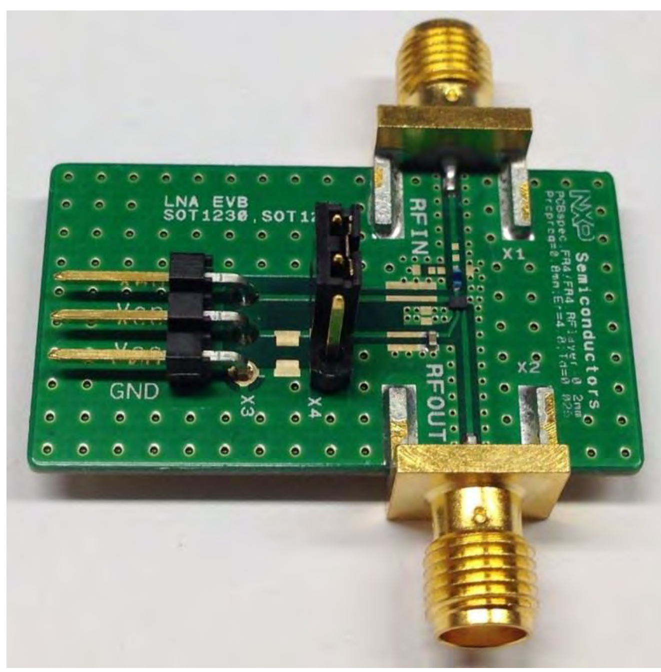


Fig 1. BGS8x2 LTE LNA evaluation board (used for BGS8L2, BGS8M2 and BGS8H2)

2. General description of application & product

Modern cellular phones have multiple radio systems, so problems like co-habitation are quite common. Since the LTE diversity antenna needs to be placed far from the main antenna to ensure the efficiency of the channel, a low noise amplifier close to the antenna is used to compensate the track-losses (and SAW-filter losses when applicable) on the printed circuit board. A LTE receiver implemented in a mobile phone requires a low current consumption and low Noise Figure. All the different transmit signals that are active in smart phones and tablets can cause problems like inter-modulation and compression. Therefore also a high linearity is required.

2.1 BGS8L2

NXP Semiconductors' BGS8L2 LTE low noise amplifier is designed for the LTE low band. The integrated biasing circuit is temperature stabilized, which keeps the current constant over temperature. It also enables the superior linearity performance of the BGS8L2. The BGS8L2 is also equipped with an enable function that allows it to be controlled via a logic signal. In disabled mode it consumes less than1 µA.

The output of the BGS8L2 is internally matched between 728 MHz and 960 MHz, whereas only one series inductor at the input is needed to achieve the best RF performance. The input and output are AC coupled via an integrated capacitor.

It requires only two external components to build a LTE LNA having the following advantages:

- Low noise
- System optimized gain
- High linearity under jamming
- 1.1 x 0.7 x 0.37, 0.4mm pitch: SOT1232
- Low current consumption
- Short power settling time

2.2 Series inductor

The evaluation board is supplied with Murata LQW15 series inductor of 8.2 nH. This is a wire wound type of inductor with high quality factor (Q) and low series resistance (Rs) like the Murata LQW15A series (see Table 1). This type of inductor is recommended in order to achieve the best noise performance. High Q inductors from other suppliers can be used. If it is decided to use other low cost inductors with lower Q and higher Rs the noise performance will degrade.

Table 1. Series Inductor options

Type	Murata	Size 0201	Size 0402	Size 0603	Comment
Multilayer Non-Magnetic Core	LQG		15H NF↑↑	18H NF↑	
Film	LQP	03T NF↑↑	15M NF↑		
Wirewound Non-Magnetic Core	LQW		15A **Default**	18A NF↓	Lowest NF

2.3 BGS8x2: Advantage of integrated By-pass function

The major advantage of having a bypass-switch option is the very low current consumption (<1µA) when LTE LNA is not needed in the receive chain (at high RSSI/CQI level, 3~5dB higher than the Sensitivity level). Fig 2 gives a graphical explanation of this advantage.

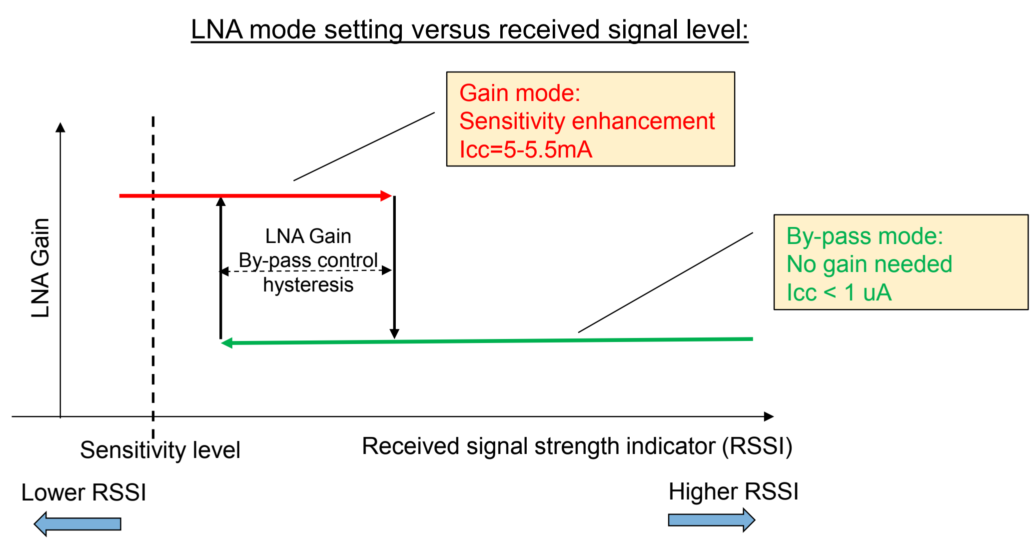


Fig 2. LNA mode setting versus received signal level

To avoid frequently switching between Gain- and bypass-mode around chosen Receiver Signal Strength Indicator (RSSI) switching level, one should take a Hysteresis Loop into consideration in the switching logic of the control chip (transceiver or baseband chip), see Fig 2.

3. BGS8L2 LTE LNA evaluation board

The BGS8L2LNA evaluation board simplifies the RF evaluation of the BGS8L2 LTE LNA applied in a LTE front-end, often used in mobile cell phones. The evaluation board enables testing of the device RF performance and requires no additional support circuitry. The board is fully assembled with the BGS8L2 including the input series inductor and decoupling capacitor. The board is supplied with two SMA connectors for input and output connection to RF test equipment. The BGS8L2 can operate from a 1.5 V to 3.1 V single supply and consumes typical 5.2 mA.

3.1 Application Circuit

The circuit diagram of the evaluation board is shown in Fig 3. With jumper JU1 the control input can be connected either to Vcc (Gain-mode) or GND (Bypass mode).

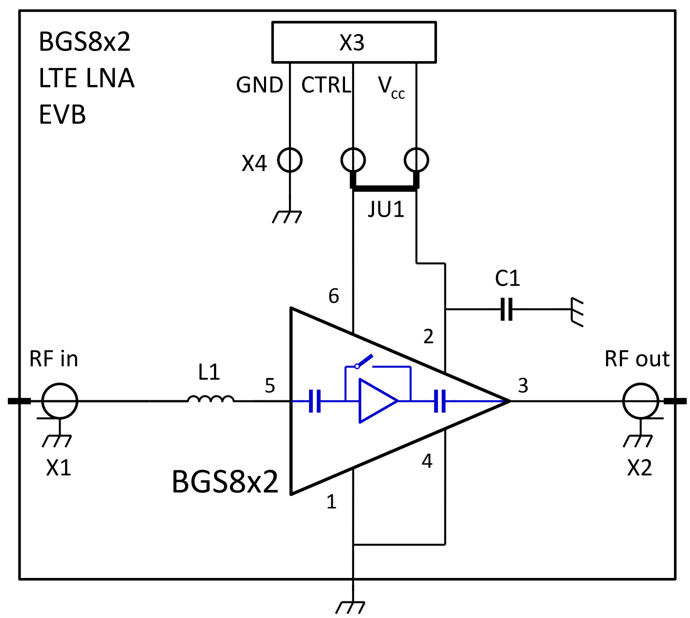


Fig 3. Circuit diagram of the BGS8x2 LNA evaluation board (used for BGS8L2, BGS8M2 and BGS8H2)

3.2 Bill of materials

Table 2. BOM of the BGS8L2 LTE LNA evaluation board

Designator	Description	Footprint	Value	Supplier Name/type	Comment
M	BGS8L2	1.1 x 0.7 x 0.37mm^3, 0.4mm pitch		NXP	SOT1232
PCB		20 x 35mm		BGS8L2 LTE LNA EV Kit	
C1	Capacitor	0402	1µF	Murata GRM1555	Decoupling
L1	Inductor	0402	8.2nH	Murata LQW15	Input matching
X1, X2	SMA RD connector	-	-	Johnson, End launch SMA 142-0701-841	RF input/ RF output
X3	DC header	-	-	Molex, PCB header, Right Angle, 1 row, 3 way 90121-0763	Bias connector
X4	JUMPER Stage	-	-	Molex, PCB header, Vertical, 1 row, 3 way 90120-0763	Connect Ven to Vcc or separate Ven voltage
JU1	JUMPER				

3.3 PCB Layout

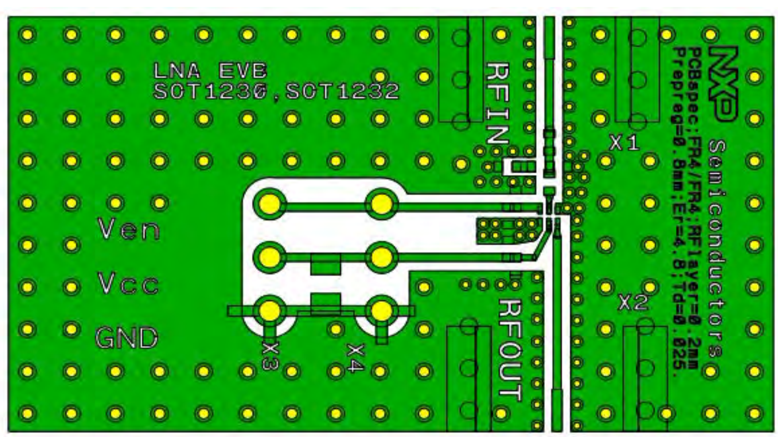
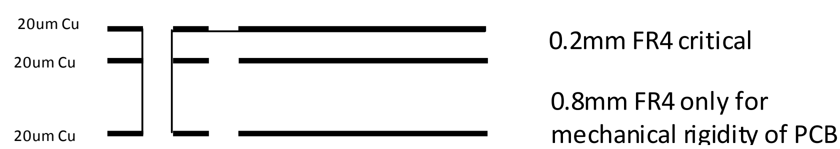


Fig 4. Printed-Circuit Board layout of the BGS8x2 LNA evaluation board (used for BGS8L2, BGS8M2 and BGS8H2)

A good PCB layout is an essential part of an RF circuit design. The LNA evaluation board of the BGS8L2 can serve as a guideline for laying out a board using the BGS8L2.

- Use controlled impedance lines for all high frequency inputs and outputs.
- Bypass Vcc with decoupling capacitors, preferably located as close as possible to the device.
- For long bias lines it may be necessary to add decoupling capacitors along the line further away from the device.
- Proper grounding of the GND pins is also essential for good RF performance.
- Either connect the GND pins directly to the ground plane or through vias, or do both, which is recommended.

The material that has been used for the evaluation board is FR4 using the stack shown in Fig 5.



(1) Material supplier is ISOLA DURAVER; εr = 4.6-4.9: $T\delta = 0.02$

Fig 5. Stack of the PCB material

4. Required Measurement Equipment

In order to measure the evaluation board the following is necessary:

- ✓ DC Power Supply up to 30 mA at 1.5 V to 3.1 V
- ✓ Two RF signal generators capable of generating RF signals at the LTE operating frequencies between 728 MHz and 960 MHz.
- ✓ An RF spectrum analyzer that covers at least the LTE operating frequencies of 728 MHz to 960 MHz as well as a few of the harmonics. Up to 6 GHz should be sufficient.
  "Optional" a version with the capability of measuring noise figure is convenient
- ✓ Amp meter to measure the supply current (optional)
- ✓ A network analyzer for measuring gain, return loss and reverse isolation
- ✓ Noise figure analyzer and noise source
- ✓ Directional coupler
- ✓ Proper RF cables

5. Connections and setup

The BGS8L2 LTE LNA evaluation board is fully assembled and tested (see Fig 6). Please follow the steps below for a step-by-step guide to operate the LNA evaluation board and testing the device functions.

1. Connect the DC power supply to the V_{cc} and GND terminals. Set the power supply to the desired supply voltage, between 1.5 V and 3.1 V, but never exceed 3.1 V as it might damage the BGS8L2.
2. Jumper JU1 is connected between the V_{cc} terminal of the evaluation board and the V_{en} pin of the BGS8L2.
3. Connect the RF signal generator and the spectrum analyzer to the RF input and the RF output of the evaluation board, respectively (Fig 6). Do not turn on the RF output of the signal generator yet, set it to approximately -30 dBm output power at center frequency of the wanted LTE-band and set the spectrum analyzer at the same center frequency and a reference level of 0 dBm.
4. Turn on the DC power supply and it should read approximately 5 mA.
5. Enable the RF output of the generator: The spectrum analyzer displays a tone around –17 dBm.
6. Instead of using a signal generator and spectrum analyzer one can also use a network analyzer in order to measure gain as well as in- and output return loss, P1dB and IP3 (see Fig 7).
7. For noise figure evaluation, either a noise figure analyzer or a spectrum analyzer with noise option can be used. The use of a 5 dB noise source, like the Agilent 364B is recommended. When measuring the noise figure of the evaluation board, any kind of adaptors, cables etc. between the noise source and the evaluation board should be minimized, since this affects the noise figure (see Fig 8).

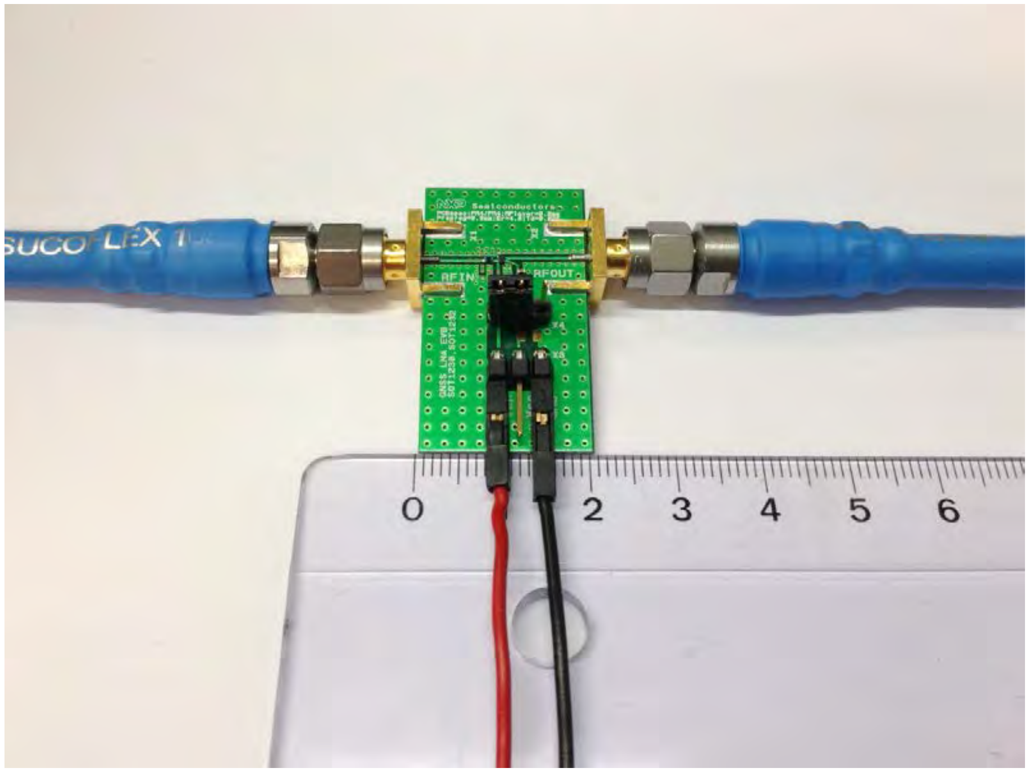


Fig 6. Evaluation board including its connections

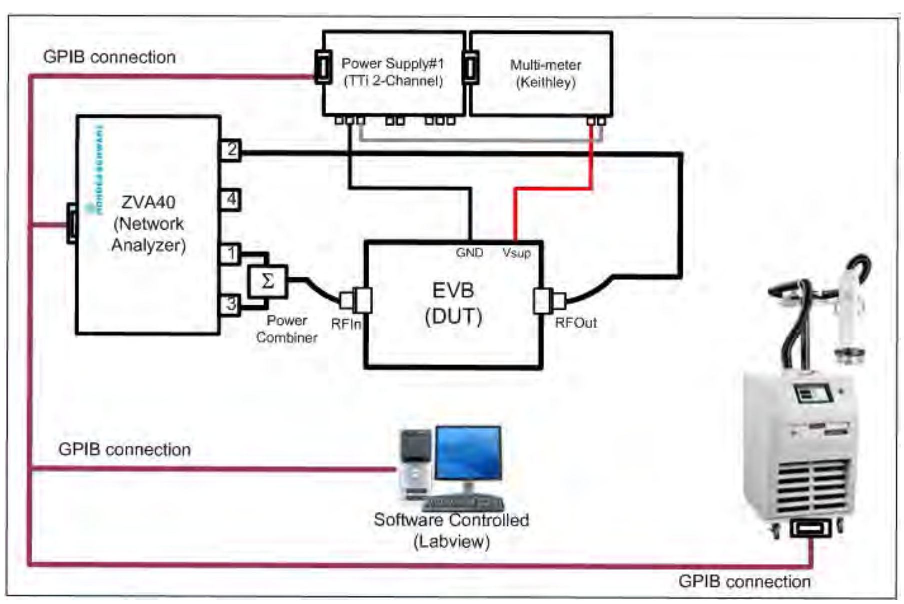


Fig 7. 2-Tone Setup for 50Ω LNA board tests (S-Parameters, P1dB and 2-Tone-tests)

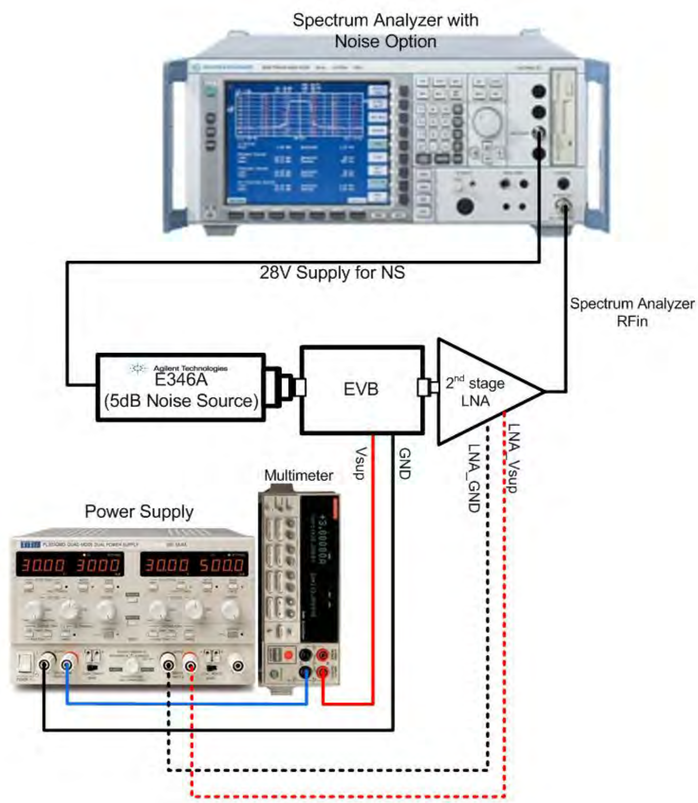


Fig 8. Setup diagram for 50Ω LNA-board NF-Measurements.

6. Evaluation Board Test Results

6.1 S-Parameters

The measured S-Parameters and stability factor K are given in the figures below. For the measurements, a BGS8L2-LNA EVB is used ((see Fig 6). Measurements have been carried out using the setup shown in Fig 7.

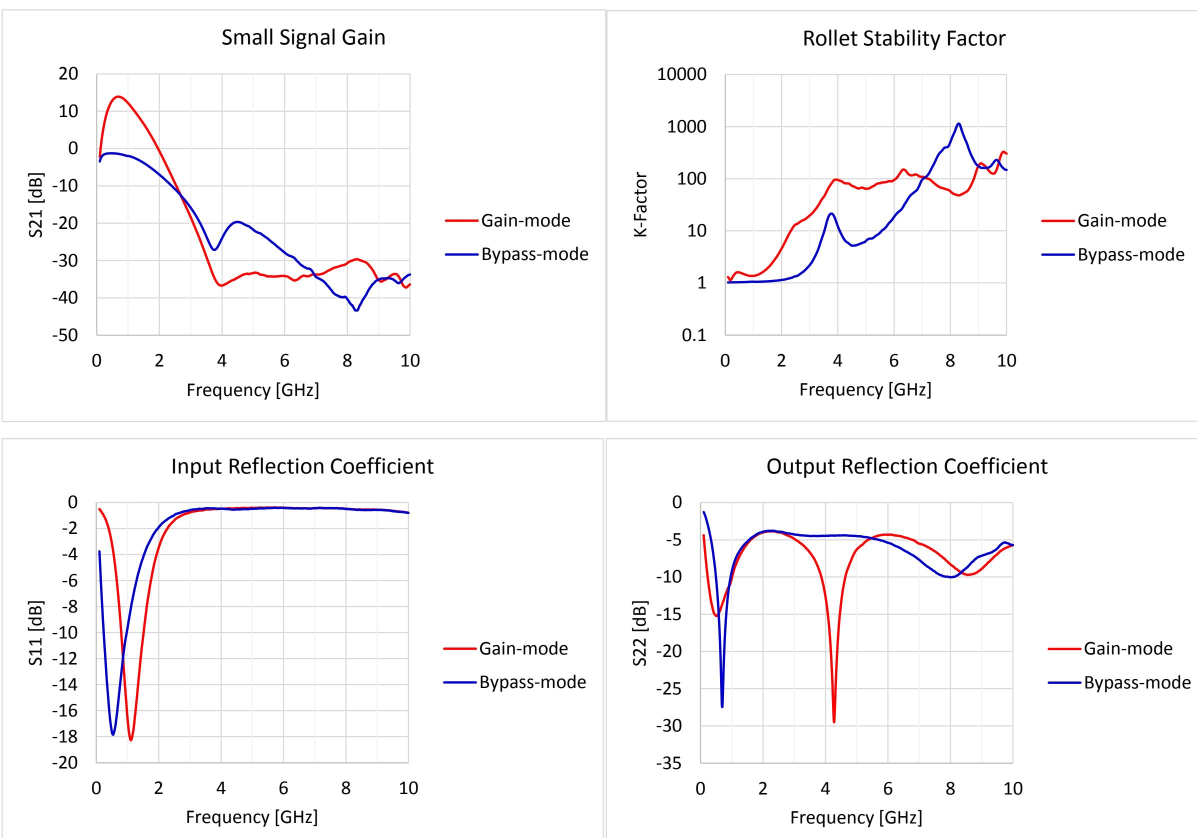


Fig 9. BGS8L2 S-Parameters (typical values). Vcc=2.8V, Pin=-30dBm. Gain mode and Bypass mode

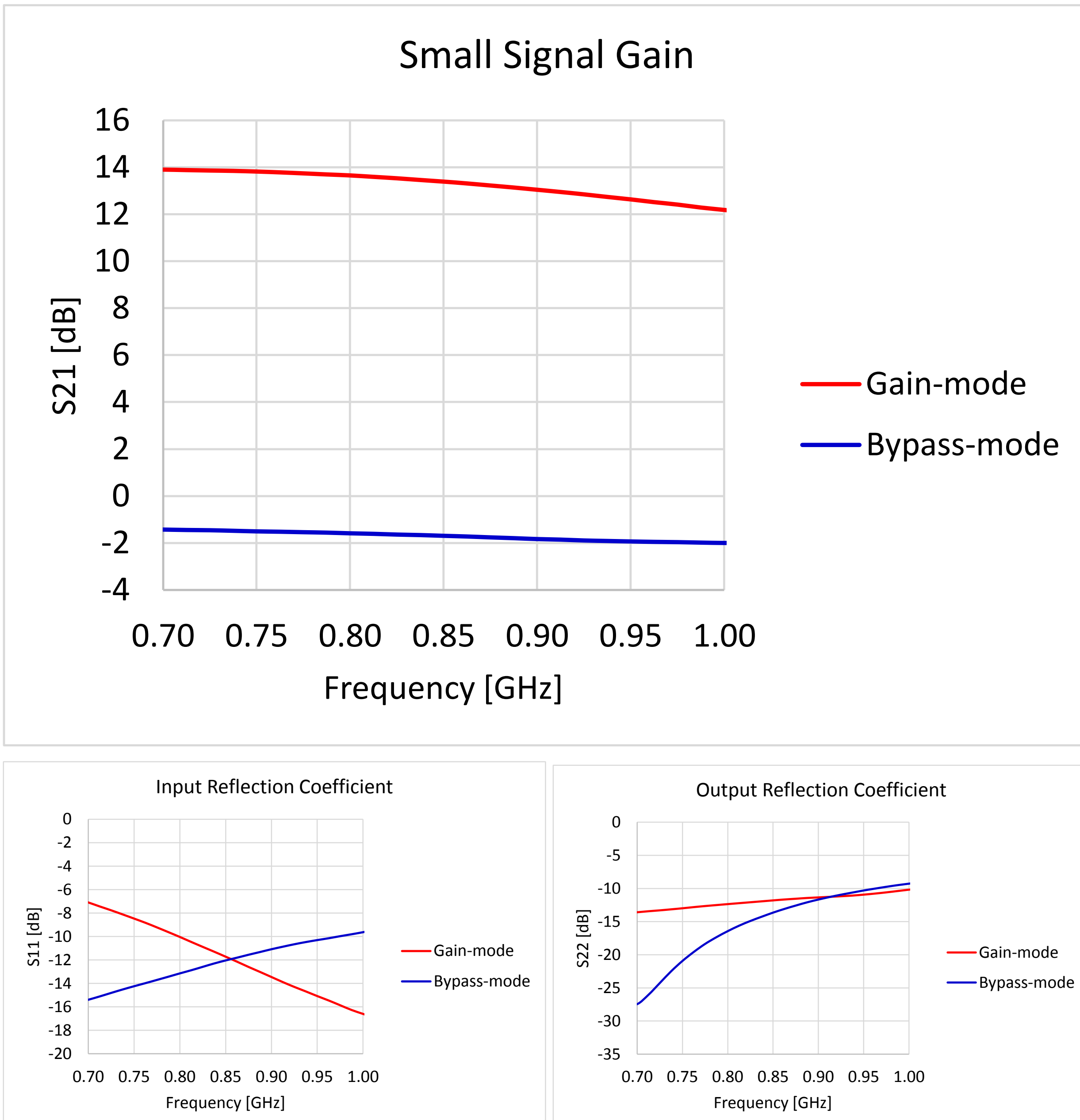
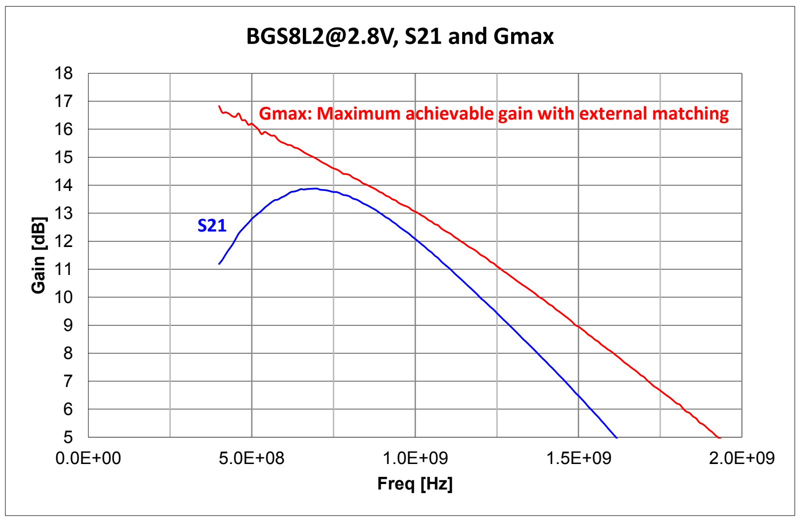


Fig 10. BGS8L2 S-Parameters (typical values). Vcc=2.8V, Pin=-30dBm, Gain mode and Bypass mode (Frequency range zoomed in).

6.2 Improving the Gain by optimized matching

The design of the BGS8x2 LTE LNA's are optimized for best RF-performance using only one input matching coil. In some cases, the Gain can be increased if more in- and output components are used. Fig 11 gives the theoretical maximum gain (Gmax) using (ideal) optimized in- and output matching circuits, and S21 (typical measured performance) of a BGS8L2 demoboard.



Freq [MHz]	Gmax [dB]	S21 [dB]	S11 [dB]	S22 [dB]	S12 [dB]
740	14.7	13.8	-8.2	-21.9	-23.3
880	13.9	13.1	-12.5	-12.0	-21.9
940	13.5	12.6	-14.4	-10.2	-21.5

Fig 11. S21 and Maximum achievable gain (Gmax) typ. values (Gain mode)

Fig 12 gives an implementation of an improved matching circuit using 3 inductors to increase the Gain.

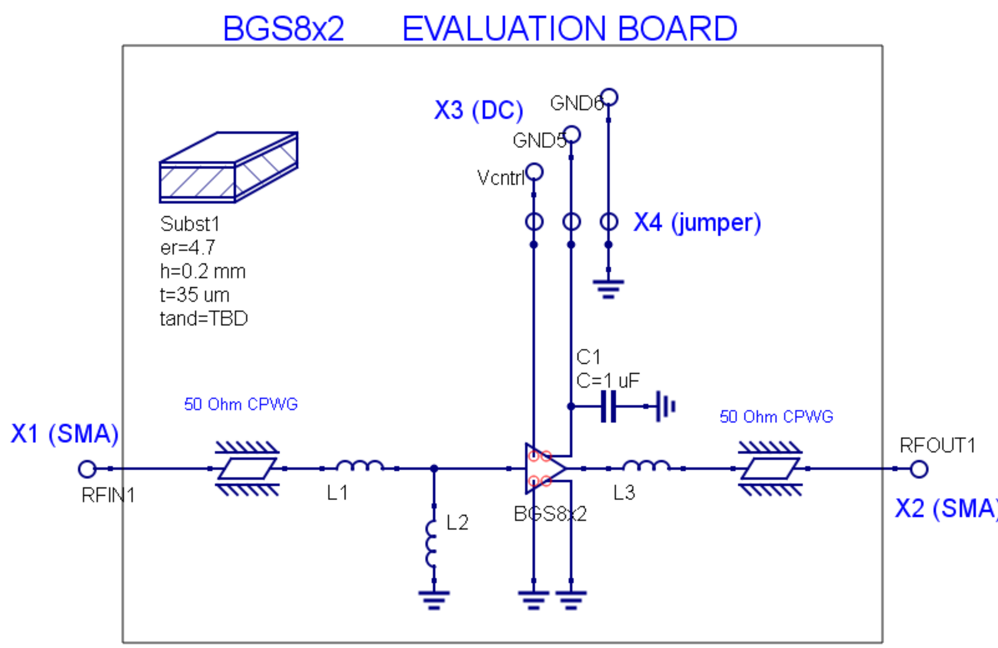


Fig 12. Circuit diagram of the BGS8x2 LNA evaluation board using 2 input and one output inductor to optimize the Gain.

6.3 1dB gain compression

Strong in-band cell phone TX jammers can cause linearity problems and result in third-order intermodulation products in the LTE frequency band. In this chapter the effects of these strong signals is shown. For the measurements, a BGS8L2-LNA EVB is used ((see Fig 6). Measurements have been carried out using the setup shown in Fig 7. The gain as function of input power of the DUT was measured between port RFin and RFout of the EVB at the low LTE center frequencies. The figures below show the gain compression curves at LNA-board.

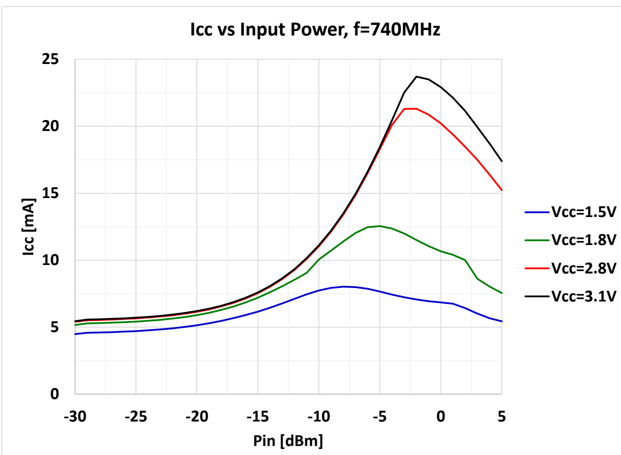


Fig 13. Icc versus input power , f=740MHz (band 17)

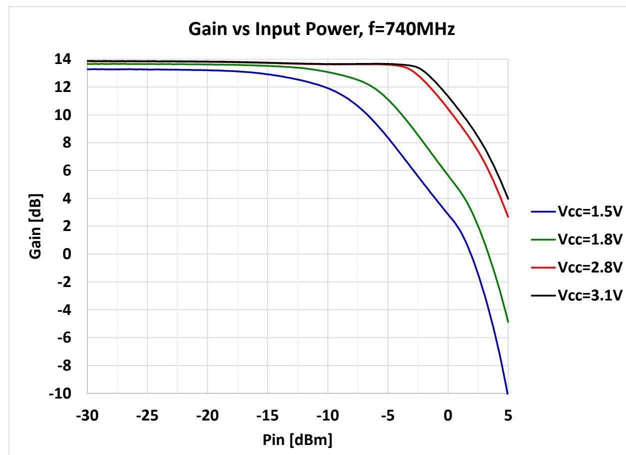


Fig 14. Gain versus input power , f=740MHz (band 17)

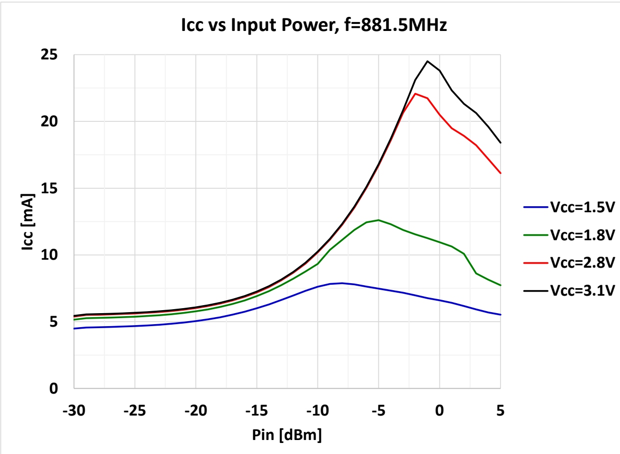


Fig 15. Icc versus input power , f=881.5MHz (band 5)

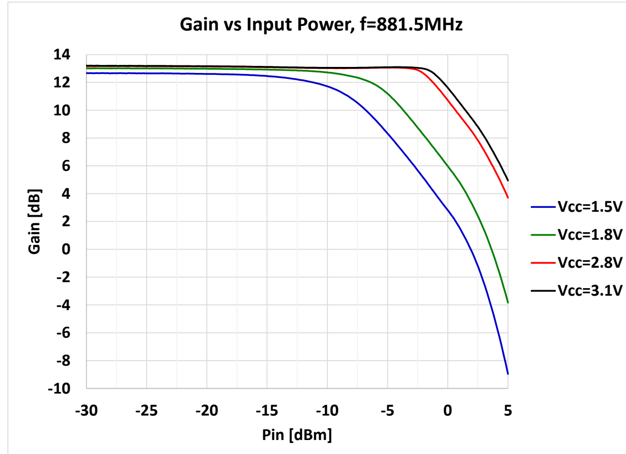


Fig 16. Gain versus input power , f=881.5MHz (band 5)

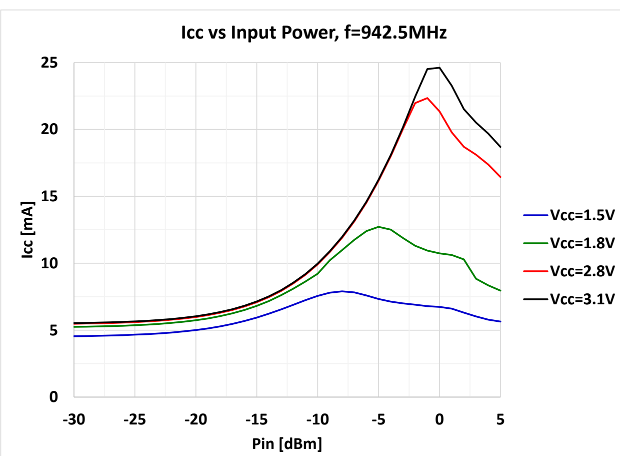


Fig 17. Icc versus input power , f=942.5MHz (band 8)

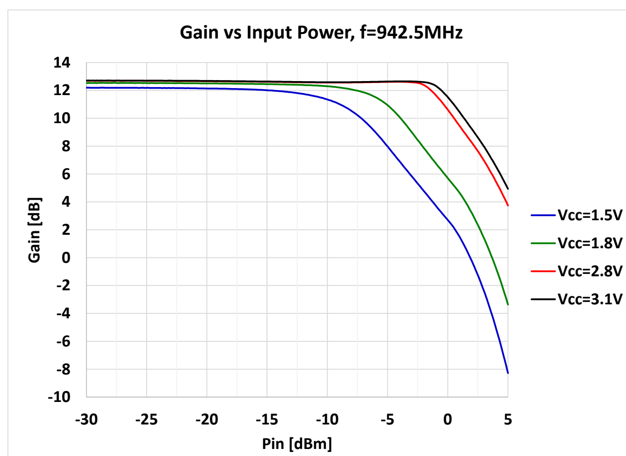


Fig 18. Gain versus input power , f=942.5MHz (band 8)

6.4 IIP3 2-Tone Test

The figures below show measured input-IP3-results of the DUT measured with a 2-Tone test at the LTE-bands. For the measurements, a BGS8L2-LNA EVB is used (see Fig 6). Measurements have been carried out using the setup shown in Fig 7.

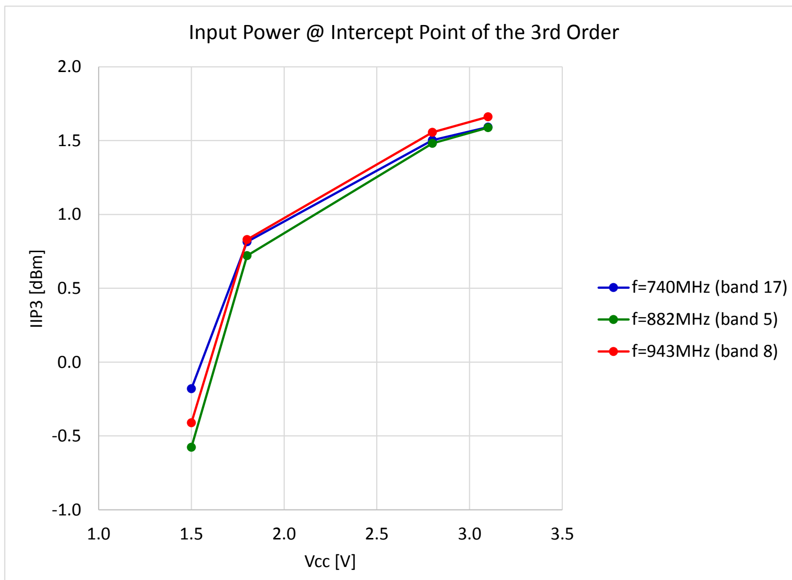


Fig 19. IIP3=F(Vcc), Pin=-30dBm

6.5 Enable Timing Test

The following diagram shows the setup to test LNA Turn ON and Turn OFF time.

Set the waveform generator to square mode and the output amplitude at 3Vrms with high output impedance. The waveform generator has adequate output current to drive the LNA therefore no extra DC power supply is required which simplifies the test setup.

Set the RF signal generator output level to -20dBm at a frequency between 728 MHz and 960 MHz and increase its level until the output DC on the oscilloscope is at 5mV on 1mV/division, the signal generator RF output level is approximately -3dBm.

It is very important to keep the cables as short as possible at input and output of the LNA so the propagation delay difference on cables between the two channels is minimized.

It is also critical to set the oscilloscope input impedance to 50ohm on channel 2 so the diode detector can discharge quickly to avoid a false result on the Turn OFF time testing.

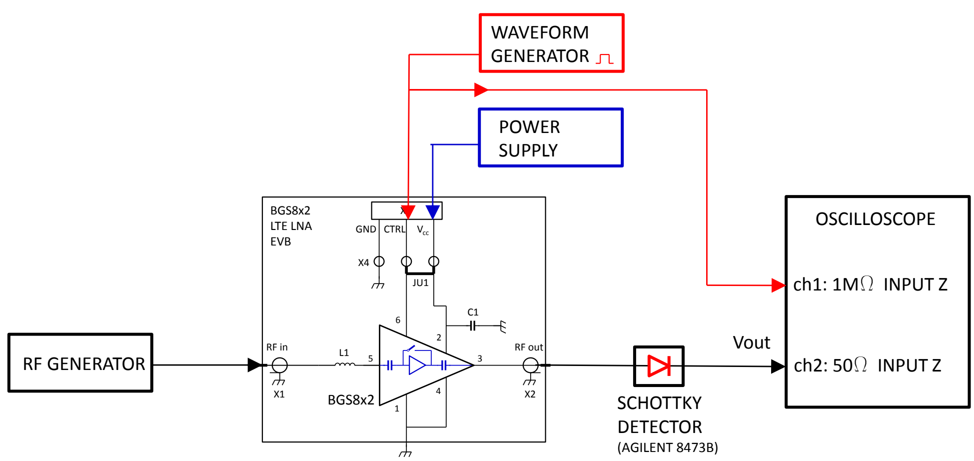


Fig 20. Setup Enable Timing Test

Fig 21 and Fig 22 show the measured Ton and T_bypass test.

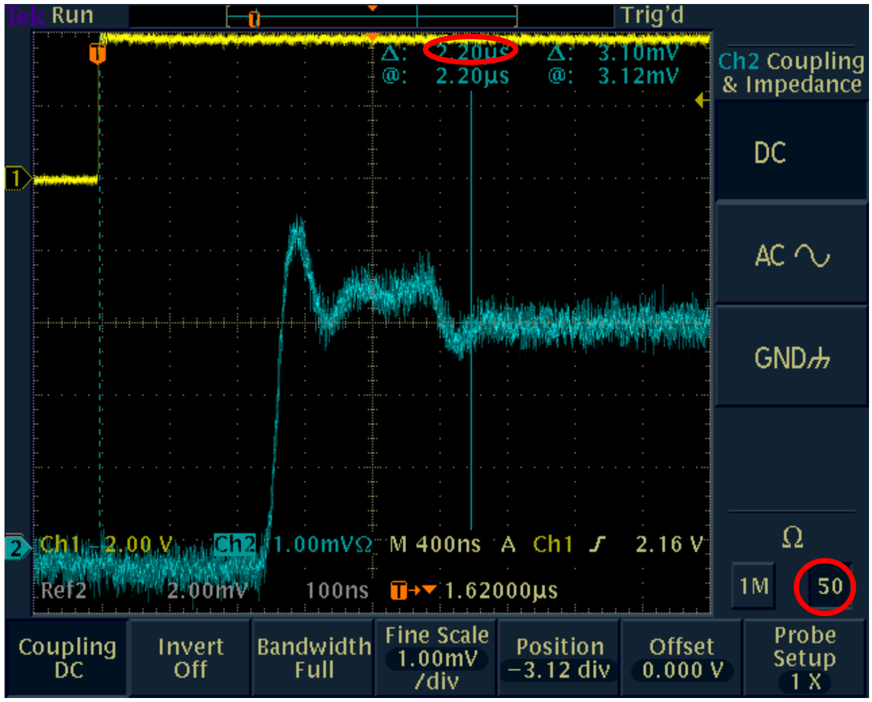


Fig 21. Results Enable Timing Test. Frq=880MHz, Pin=-20dBm, Vcc=2.8V : Ton~2.2 µs.

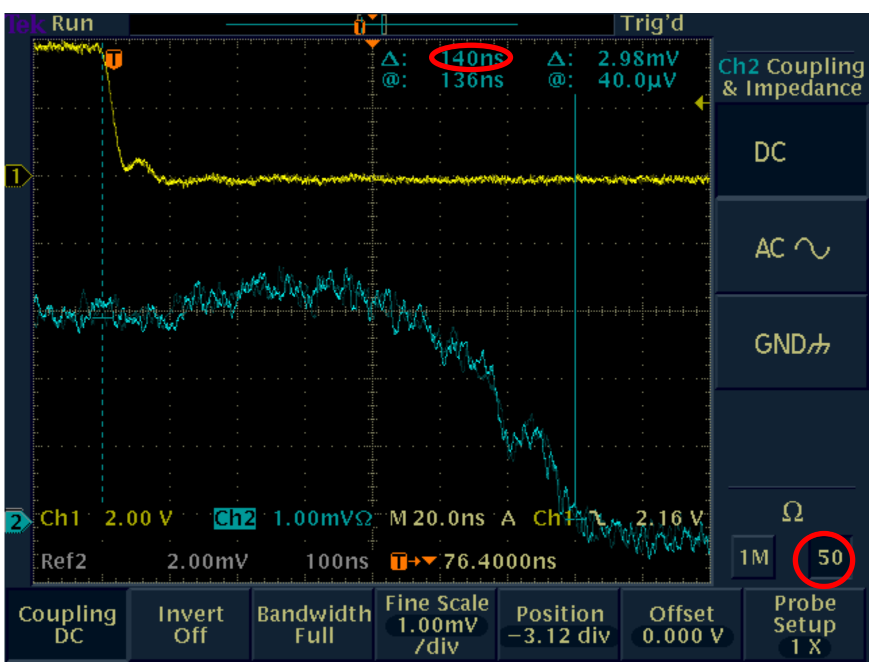


Fig 22. Results Enable Timing Test. Frq=880MHz, Pin=-20dBm, Vcc=2.8V : T_Bypass~140 ns.

7. Typical LNA evaluation board results

Table 3. Typical results measured on the evaluation Board.

728 MHz ≤ f ≤ 960 MHz; Venable ≥ 0.8 V; Pi < -40 dBm; Tamb = 25°C input matched to 50 Ω using a 8.2 nH inductor unless otherwise specified.

Mode	Symbol	Parameter	Conditions	Note	Unit	Evaluation 1.8V	Evaluation 2.8V
Gain Mode	ICC	supply current	Vctrl ≥ 0.8 V		mA	5.0	5.2
	Gp	power gain	f = 740 MHz		dB	13.5	13.5
			f = 882 MHz		dB	13.0	13.0
			f = 943 MHz		dB	12.5	12.5
	RLin	input return loss	f = 740 MHz		dB	7.5	8.0
			f = 882 MHz		dB	12.0	12.0
			f = 943 MHz		dB	13.0	14.0
	RLout	output return loss	f = 740 MHz		dB	21.0	21.0
			f = 882 MHz		dB	11.0	12.5
			f = 943 MHz		dB	10.0	10.5
	ISL	isolation	f = 740 MHz		dB	23.0	23.0
			f = 882 MHz		dB	22.0	22.0
			f = 943 MHz		dB	21.5	21.5
	NF	noise figure	f = 740 MHz	[1]	dB	0.90	0.90
			f = 882 MHz	[1]	dB	0.90	0.90
			f = 943 MHz	[1]	dB	0.95	0.90
	Pi(1dB)	input power at 1dB gain compression	f = 740 MHz		dBm	-7.5	-2.0
			f = 882 MHz		dBm	-6.0	-1.0
			f = 943 MHz		dBm	-5.5	-0.5
	IP3i	input third order intercept point	fc = 740 MHz	[2]	dBm	1.0	1.5
			fc = 882 MHz	[3]	dBm	1.0	1.5
			fc = 943 MHz	[4]	dBm	1.0	1.5
	K	rollet stability factor	f = 740 MHz			1.4	1.4
			f = 882 MHz			1.4	1.4
			f = 943 MHz			1.4	1.4
			minimum value	[5]		1.2	1.2
Bypass Mode	ICC	supply current	Vctrl ≤ 0.3 V		uA	< 1	< 1
	Gp	power gain	f = 740 MHz		dB	-1.6	-1.6
			f = 882 MHz		dB	-2.0	-1.9
			f = 943 MHz		dB	-2.0	-2.0
	RLin	input return loss	f = 740 MHz		dB	14.5	15.0
			f = 882 MHz		dB	11.5	11.5
			f = 943 MHz		dB	10.5	11.0
	RLout	output return loss	f = 740 MHz		dB	12.5	13.0
			f = 882 MHz		dB	11.0	11.5
			f = 943 MHz		dB	10.5	11.5
	Pi(1dB)	input power at 1dB gain compression	f = 740 MHz		dBm		>10
			f = 882 MHz		dBm		>10
			f = 943 MHz		dBm		>10
	IP3i	input third order intercept point	fc = 740 MHz		dBm		>27
			fc = 882 MHz		dBm		>27
			fc = 943 MHz		dBm		>27

[1] PCB Losses are included
[2] Average IIP3 (dBm) --> f1 = 740 MHz; f2 = 741 MHz; Pi = -30 at both frequencies
[3] Average IIP3 (dBm) --> f1 = 882 MHz; f2 = 883 MHz; Pi = -30 at both frequencies
[4] Average IIP3 (dBm) --> f1 = 943 MHz; f2 = 944 MHz; Pi = -30 at both frequencies
[5] Minimum Value for Pin = -30 dBm; 0.1 GHz < f < 10 GHz

8. Legal information

8.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

8.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

8.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

9. List of figures

10. List of tables

11. Contents

For more information, visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 17 July 2015

Document identifier: AN11654