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Motorola's 56F8300 Benefits in Industrial Applications

White Paper

Motorola 56F8300 Hybrid Controller Family

MOTOROLA.COM/SEMICONDUCTORS

Motorola's 56F8300 Benefits in Industrial Applications

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Contents

1. Introduction

1.1 Overview

Motorola hybrid and microcontrollers have a long and distinguished history in industrial and control applications. The new 56F8300 Series is the latest addition to the widely adopted 56F800 portfolio of high-performance, Flash-based hybrid controllers. The 56F8300 devices combine the capabilities of a microcontroller with the signal processing performance of a Digital Signal Processor (DSP), and the raw protocol and control processing power of a 32-bit RISC. Some of the features and benefits of the 56F8300 solutions that this paper will explore are:

- **Exceptional integration of powerful internal peripherals**--significantly lowers system costs
- **High-performance, reliable internal Flash memory**--offers flexibility in development, production and inventory with the reliability and performance traditionally associated with read-only memory
- **High 60MHz/60 MIPS performance**--enables a broad range of applications at a lower cost
- **Hybrid MCU/DSP core architecture**--speeds development and lowers component count
- **Integrated safety features for high reliability**--creates safer, lower-risk, more reliable end products
- **Extended temperature operation**--allows innovative end products that can be used in the harshest environments
- **Powerful, award-winning CodeWarrior™ Integrated Development Environment**--lowers software development costs and frees your software developers
- **Innovative Processor Expert™ rapid application development tool**--dramatically speeds software development and the developer's learning curve

These elements mean that the 56F8300 Series of components is ideally suited for a broad range of industrial applications. The 56F8300 Series is a part of the greater Motorola Embedded Flash portfolio, as shown in **Figure 1-1**.

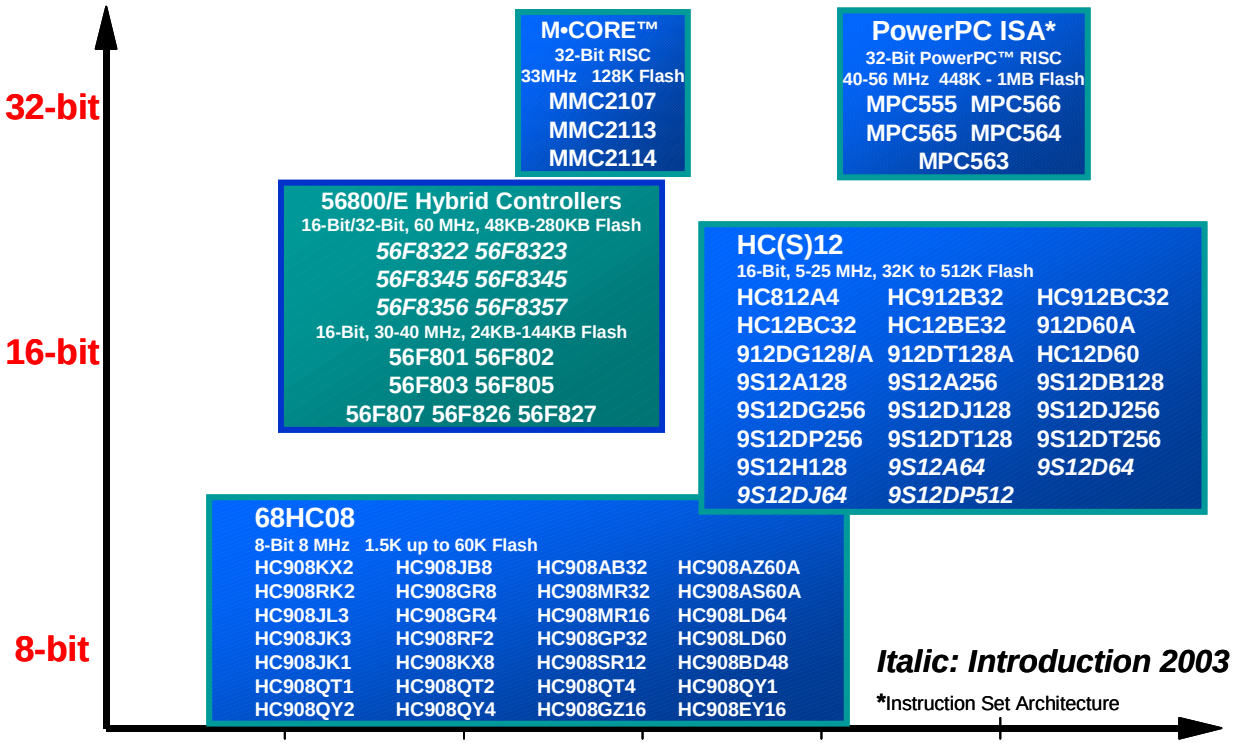


Figure 1-1. Motorola's Controller Continuum

Figure 1-2 illustrates the broad portfolio of 56800/E components; all are code compatible. The 56F800 series are based on the original 56800 core and offer the best of both MCU and DSP functionality. The 56F8300 Series is based around the enhanced version of the 56800 core, the 56800E, and offers improved DSP and MCU performance, as well as improved 32-bit capability. The 56850 series are RAM-based and targeted for high performance voice, multimedia, telecom, and hybrid networking applications.

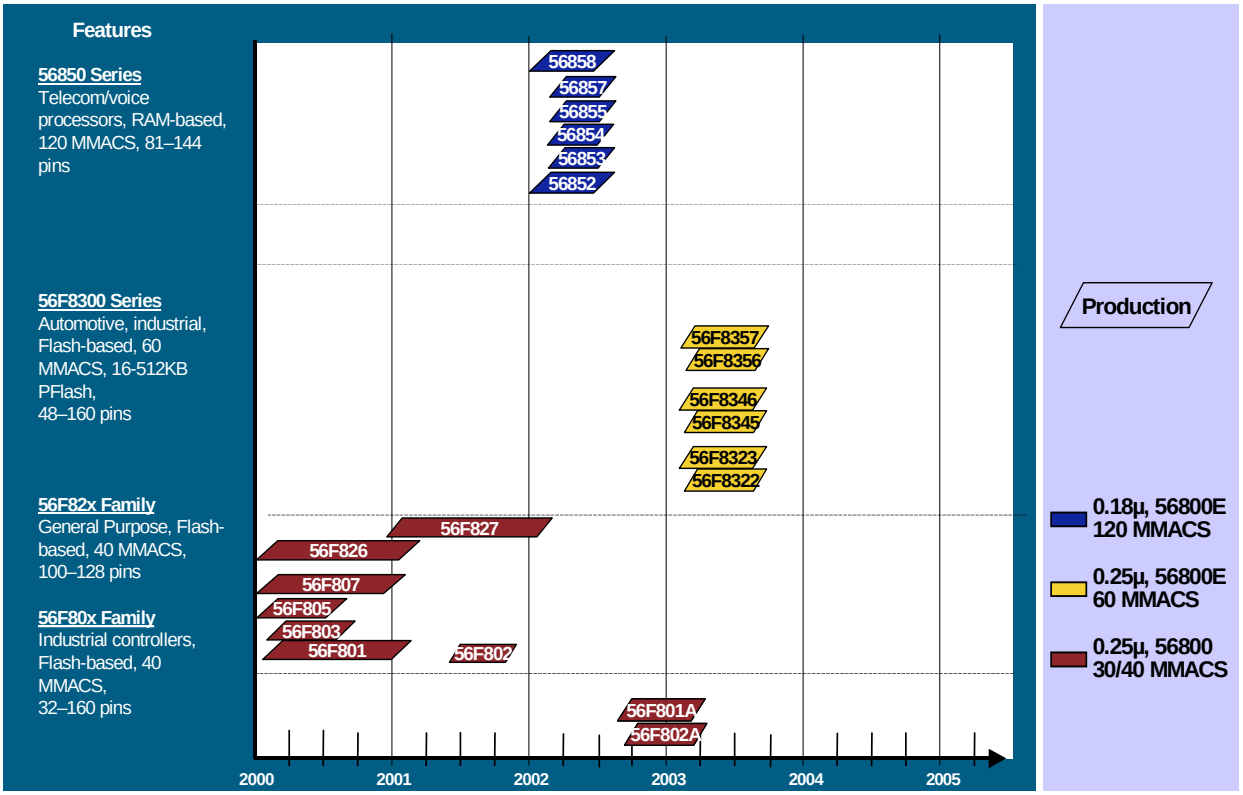
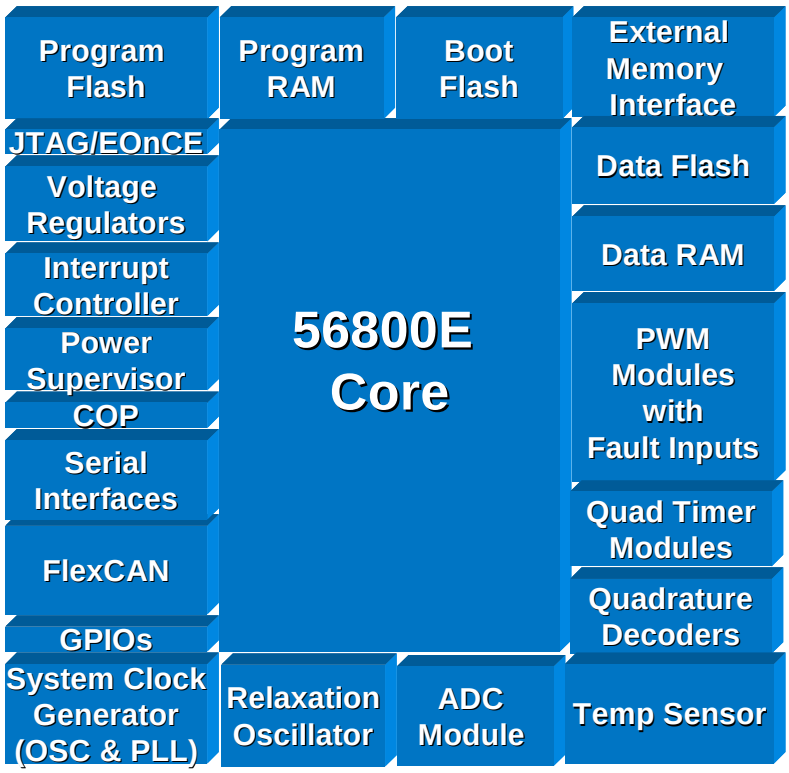


Figure 1-2. Motorola Hybrid Controller Portfolio

The 56F8300 devices are the highest-performance Flash-based hybrid controllers in the portfolio. The components in the 56F8300 Series have a broad range of package, memory, and peripheral configurations. **Table 1** and **Figure 1-3** show the details of the 56F8300 portfolio.

Table 1: 56F8300 Portfolio Details

	56F8322	56F8323	56F8345	56F8346	56F8356	56F8357
Performance	60MHz	60MHz	60MHz	60MHz	60MHz	60MHz
Temperature Range	-40°C to +105°C or -40°C to +125°C	-40°C to +105°C or -40°C to +125°C	-40°C to +105°C or -40°C to +125°C	-40°C to +105°C or -40°C to +125°C	-40°C to +105°C or -40°C to +125°C	-40°C to +105°C or -40°C to +125°C
Voltage (Core / I/O)	2.6V / 3.3V	2.6V / 3.3V	2.6V / 3.3V	2.6V / 3.3V	2.6V / 3.3V	2.6V / 3.3V
Program Flash	32KB	32KB	128KB	128KB	256KB	256KB
Program RAM	4KB	4KB	4KB	4KB	4KB	4KB
Data Flash	8KB	8KB	8KB	8KB	8KB	8KB
Data RAM	8KB	8KB	8KB	8KB	16KB	16KB
BootFlash	8KB	8KB	8KB	8KB	16KB	16KB
Flash Security	Yes	Yes	Yes	Yes	Yes	Yes
External Memory Interface	No	No	No	Yes	Yes	Yes
Regulator (On-Chip / Off-Chip)	On-Chip	On-Chip / Off-Chip	On-Chip / Off-Chip	On-Chip / Off-Chip	On-Chip / Off-Chip	On-Chip / Off-Chip
On-Chip Relaxation Oscillator	Yes	Yes	No	No	No	No
Quad Timer	2	2	4	4	4	4
Quadrature Decoder	1 x 4 channel	1 x 4 channel	2 x 4 channel	2 x 4 channel	2 x 4 channel	2 x 4 channel
PWM	1 x 6 channel	1 x 6 channel	2 x 6 channel	2 x 6 channel	2 x 6 channel	2 x 6 channel
PWM Fault Input	1	3	4 + 4	3 + 4	3 + 4	4 + 4
PWM Chip Select Pins	0	3	3+ 3	3+ 3	3+ 3	3+ 3
12-bit ADC	2 x 3 channel	2 x 4 channel	4 x 4 channel	4 x 4 channel	4 x 4 channel	4 x 4 channel
Temperature Sensor	Yes	Yes	Yes	Yes	Yes	Yes
FlexCAN	1	1	1	1	1	1
SCI (UART)	2	2	2	2	2	2
SPI (Synchronous)	2	2	2	2	2	2
GPIO (Maximum)	21	27	49	62	49	76
JTAG/EOnCE	Yes	Yes	Yes	Yes	Yes	Yes
Package	48 LQFP	64 LQFP	128 LQFP	144 LQFP	144 LQFP	160 LQFP



Package: From 48 up to 160 pin LQFP

Figure 1-3. 56F8300 Block Diagram

The 56F8300 Series offers an excellent complement of peripherals and a broad range of memory and packages. Some of the 56F8300 Series's benefits include:

- **High performance 56800E hybrid core**
  - Superior 16-bit, fixed-point signal processing performance provided by the bus architecture and the hybrid controller core
  - Excellent control and protocol processing capability and code density
  - Superior 32-bit performance provided by the internal 32-bit-wide buses and registers
- **Performance-leading Flash memory**
  - Unbeatable, field-proven reliability in the harshest environments
  - Features that enable emulation of EEPROM
  - Flexible, full in-circuit flash programability
  - Performance-enhancing interfacing and bus structure, enabling the greatest signal processing capability from Flash in the controller continuum portfolio
  - Flash block protection features for IP protection

- **Flexible External Memory Interface (EMI)**
  - Some 56F8300 devices include a flexible External Memory Interface that enables glueless connection with programmable chip selects and separate wait state generation, enabling the most cost-effective and lowest chip count possible when interfacing to external memory or peripherals
  - The EMI interface can be configured as GPIO
- **Voltage regulator and power supervisor**
  - The chips come equipped with an on-board voltage regulator and power supervisor. When supplied with a 3.3V voltage, the chip creates all the internal voltages required.
  - Includes features such as Power-On Reset (POR) and low-voltage detection, thereby eliminating external components and saves system costs
- **On-chip Relaxation Oscillator**
  - Some 56F8300 devices are equipped with a precision on-chip factory trimmed oscillator (0.25% of 8 MHz), enabling the elimination of an external crystal and providing system cost savings
- **On-chip Clock Synthesis (OCCS)**
  - 56F8300 hybrid controllers are equipped with on-chip crystal and ceramic resonator oscillator drive circuitry, enabling the direct connection of an external crystal or ceramic resonator
  - The OCCS capability includes a flexible, programmable Phase Locked Loop (PLL), enabling selection of an exact operating frequency
  - The OCCS also includes unique loss-of-lock detection, enabling the detection of a cut crystal and the proper safety-critical shut down
- **Quad Timer**
  - 56F8300 devices are equipped with powerful timer modules. Each timer module has four independent 16-bit timers that can be:
    - Cascaded
    - Used for input capture
    - Used to generate output waveforms
    - Used to trigger the ADC
    - Used to generate auxiliary PWM waveforms
    - Used as a Digital-to-Analog Converter (DAC) when utilized in conjunction with an external low-pass filter
- **Quadrature Decoder**
  - Full-featured, four-input decoder with:
    - 32 bit directional position tracking
    - Programmable digital filtered inputs
    - Integral watchdog timer to flag a non-rotating shaft condition
    - Ability to calculate velocity measurement
- **Three-Phase PWM module**
  - The high-performance 15-bit PWMs can be used in edge-aligned and center-aligned modes, as well as in complementary and independent modes and have programable dead-time generation
  - These PWM modules have a sophisticated set of programmable fault lines that do not require a system clock for proper operation
  - These and other features make these PWM modules industry leaders in safety, reliability, and performance

- **Analog to Digital Converter (ADC) Module**
  - Each high performance 12-bit ADC has two sample and hold circuits, enabling simultaneous or sequential conversion at a rate of up to 1.2 µs per conversion
  - ADCs can be used in single-ended or differential modes and have a sophisticated set of unique features, including:
    - self calibration
    - high/low and zero crossing detection
    - power saving modes
  - ADCs can be triggered through variety of methods, including PWM synchronization
  - ADC inputs have on-chip current protection circuitry, enabling their use in the harshest of industrial applications
- **Temperature Sensor**
  - Enables the measurement of the device's operating temperature, which can be important in safety-critical or harsh temperature environments
  - Highly accurate sensor which can measure 1°C increments
  - Each component is factory-calibrated for reliable operation
  - The temperature sensing function can be configured to provide an interrupt when a certain threshold is reached, thereby providing over-temperature detection with zero overhead
- **FlexCAN**
  - This powerful second generation Controller Area Network (CAN) module is fully version 2.0 A/B compliant
  - Features include:
    - Time stamps based on a 16-bit, free-running timer
    - Programable wake-up functionality with integrated low-pass filter
    - 16 Transmit (Tx) / Receive (Rx) buffers
    - This peripheral enables the reliable and flexible networking of processors and intelligent devices at speeds up to 1Mbps
- **Serial Communication Interface (SCI)**
  - This module operates as a full duplex Universal Asynchronous Receiver Transmitter (UART)
  - Fully interrupt-driven and programmable, providing a multitude of operating modes and baud rates
- **Serial Peripheral Interface (SPI)**
  - This synchronous serial interface is double-buffered
  - Operates in wide variety of modes, rates, and bit lengths, enabling the glueless connection to external peripherals and other processors at rates up to 30Mbps
- **General Purpose Input/Output (GPIO)**
  - All digital pins for the on-board peripherals can also be individually assigned to be GPIO and individually assigned a direction
  - In addition to I/O capability, the GPIO can also generate interrupts
  - Each GPIO has programmable pull-ups
  - The GPIO also has a push-pull mode to efficiently implement a keypad interface

- **Computer Operating Properly (COP)**
  - Assists software recovery from runaway code
  - The COP is a free-running down counter which, once enabled, is designed to generate a reset when reaching zero
  - Software must periodically service the COP to clear the counter and prevent a reset
  - The COP enhances end system reliability and safety
- **JTAG/EOnCE™**
  - This enhanced on-board emulation module enables true full-rate emulation without the need for expensive hardware emulators
  - To perform powerful, non-intrusive real-time debugging, simply attach to the processor with the industry-standard JTAG interface

The 56F8300's truly impressive set of features demonstrates why Motorola is the world leader in embedded processors. These components are applicable to a broad range of industrial applications, such as:

- Compressors
- Smart appliances
- Home security
- Instrumentation
- Data acquisition
- Factory automation
- Metering
- Industrial networking
- Lifts / elevators / cranes
- HVAC blowers & fans
- Uninterruptible Power Supplies
- Switching Power Supplies

The following section will describe these features in more depth and how they can help to develop cost-effective applications.

2. The Motorola Flash Story

In 1994, Motorola was the first to develop and ship large-volume, low-cost Flash MCUs and has continued to be the embedded Flash leader. With the introduction of the performance-leading 56F8300 Series of processors, Motorola offers a portfolio of more than 65 different embedded Flash devices. With over 200 million units shipped, Motorola is not only the performance leader, but also the leader in field-proven reliability and quality. Flash-based MCU and Hybrid MCU/DSP solutions from Motorola are used in a broad range of products, including PC mice; high-temperature automotive devices; performance-demanding factory automation; and industrial networking applications. Motorola has a solution for every 8/16/32-bit embedded Flash processing need.

When taking your products to the next level with Flash, it is critical to choose a partner with the right field-proven technology. Motorola is the embedded Flash leader and the 56F8300 Series of hybrid MCU/DSP controllers is the latest offering in Motorola's Flash portfolio.

Motorola's dedicated research and development group for Non-Volatile Memory (NVM) technology has an impressive record of accomplishments. **Figure 1-4** shows the history of Motorola's progressing Flash technology. NVM technology is used in a variety of product families, all sharing a common functionality set.

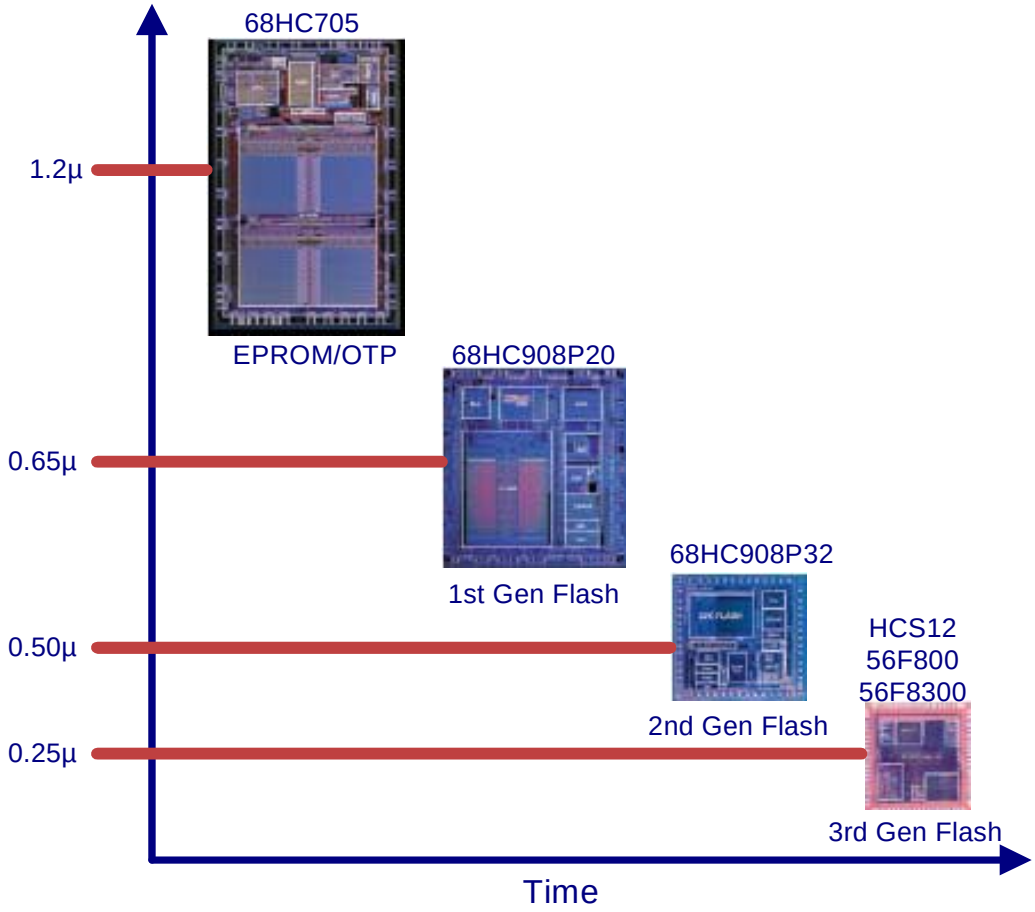


Figure 1-4. Flash Generations

Table 2 shows some of the capabilities, features and benefits of Motorola's third generation Flash NVM.

Table 2: Motorola Third Generation Flash Block Features

Feature	Benefits
In-application reprogrammability	Cost-effective programming changes and field software upgrades via in-application programmability and reprogrammability
Extremely fast programming, as fast as 16 bits in 20µs	Reduces production programming costs through ultra-fast programming
Flash programming across the full operating supply voltage with no extra programming voltage	Cost-effective reprogrammability for battery- and line-operated applications
A minimum of up to 10K write/erase cycles across temperature • Up to 100K write/erase cycles typical	Eliminates the need and cost for external serial data EEPROM
Flexible block protection and security	Protects code from unauthorized reading and guards against unintentional erasing/writing of user-programmable segments of code
Embedded Flash industry leader • A dedicated engineering team working on next-generation Flash and NVM technologies • First to ship volume Flash MCUs	Technology leadership from Motorola provides Flash MCUs that are cost competitive with industry OTP solutions--and even more cost effective over the long term
Large and rapidly growing family of Flash MCUs and hybrid MCU/DSPs	Motorola provides integrated Flash MCU solutions from 8-bit MCUs (priced at less than $1) to performance-leading Hybrid MCU/DSP embedded Flash solutions
Flash MCUs and MCU/DSPs available off the shelf	Whether you need a sample or high-volume production quantities, Motorola can meet your Flash MCU and MCU/DSP needs

The superior features and performance of Motorola's Flash greatly aid in the development of cost-effective industrial applications.

Many applications need to store a small amount of data in a non-volatile fashion that can be updated in the field. This can be configuration data for a specific installation, the state of the unit before it was turned off, data associated with specific users, or a host of other data. The nature of this data requires it to be updated under software control, must be programmed quickly, and is typically some form of data structure that must be updated on a word-by-word basis. In a typical design, this requires an EEPROM storage device or memory block. The unique properties of Motorola Flash technology allow the Flash to very effectively emulate EEPROM. For this emulation, the features required in the Flash are a small erase block size; high Flash endurance; no special programming voltages; Flash that can be

programmed on a word-by-word basis; and a rapid programming speed; Motorola's Flash has all of these. Software routines to perform the EEPROM emulation are also provided by the Processor Expert rapid application development tool.

Because Motorolas' Flash is inexpensive, exceptionally reliable in even the harshest environments, and can be programmed quickly at rates required by mass manufacturing, development, manufacturing, and support of applications can be done much more efficiently and inexpensively. Since the "final" application software can be programmed into the parts just before they are shipped to the customer, the development cycle can be effectively shortened, with lower risk. The software can be developed "just in time" and delivered after the boards have already been manufactured. Testing time and expense can be eliminated by not having to commit to ROM parts that might have to thrown away if a bug crops up late in the process. Even very high-volume, cost-conscious applications can be developed using inexpensive Flash components, simplifying the entire supply chain and greatly lowering the risk of being stuck with ROM parts that are not programmed with the proper software.

Costs associated with programming Flash components are rarely considered at the beginning of a project but can be significant. Fortunately, the options supplied by Motorola's 56F8300 Flash parts lead the industry in minimizing programming costs and providing the greatest available flexibility. The parts can be programmed out of circuit with a commercially available bulk programmer by the end user or by a third party. Stable, large-volume applications can also be programmed at the factory. The parts also have a number of options for in-circuit programming. The components can be programmed serially via the JTAG port by using a third party program or via an open source program, `flash_over_jtag`, supplied by Motorola. The components are also shipped with a resident Serial Boot Loader in the BootFlash of the components that can be used for production Flash programming. Also, the larger members of Motorola's 56F8300 Series can be programmed at a very high rate, in what is termed a parallel Flash programming mode, by using modern in-circuit test tools.

The 56F8300 devices have the best and safest field upgrade capability. Each component is equipped with a unique Flash block, called BootFlash. This area of Flash can be used to store a special boot program that handles field upgrades. And, since it is an entirely separate Flash block, even if something as catastrophic as an interruption in the power supply occurs while program Flash is being overwritten, the BootFlash is still correct and in place. When the power returns, reprogramming can be completed. Every BootFlash is programmed at the factory with a default Serial Boot Loader that fully supports factory programming as well as field updates. Additionally, because of the small block erase size supported on the components, the field upgrades can update just a small portion of the Flash memories if required. The Serial Boot Loader supports this partial update capability. The Serial Boot Loader source code is provided so that a customer can modify it and quickly create his own custom boot programs. If desired, the BootFlash can be used for normal program code, thereby increasing the size of available program memory.

The 56F8300 devices' Flash security protects your valuable intellectual property by entirely disabling the ability for the internal memories to be read by any external means. Under the direction of your internal software, the Flash can be unlocked by use of a password. This enables the customer to customize his own mechanisms for determining a trusted external party, or simply not enabling any back door mechanism at all. The Flash also has Flash protection capability, so that the Flash blocks can be secured from unintentional erasing by an errant program.

Even with all these industry leading features, the most important feature is the reliability and quality that you get with Motorola Flash. Motorola has been supplying high-reliability, extended temperature-range Flash to the most demanding customers for many years. This ensures that the Flash in the Motorola component you use is qualified and tested to meet and beat the specifications in the data sheet and can be used worry-free in the harshest environments.

3. The Pace-Setting Performance and Features of the 56F8300 Hybrid Controllers

3.1 56F8300 Series Core Features

The 56F8300 Series of devices is the latest set of components using the highly successful 56800/E hybrid 16-bit MCU/DSP core. The 56F8300 Series utilizes the enhanced 56800 core, 56800E, that has a number of improvements over the 56800 and blurs the line between 16-bit and 32-bit architectures.

Figure 1-5 shows the 56800E core architecture.

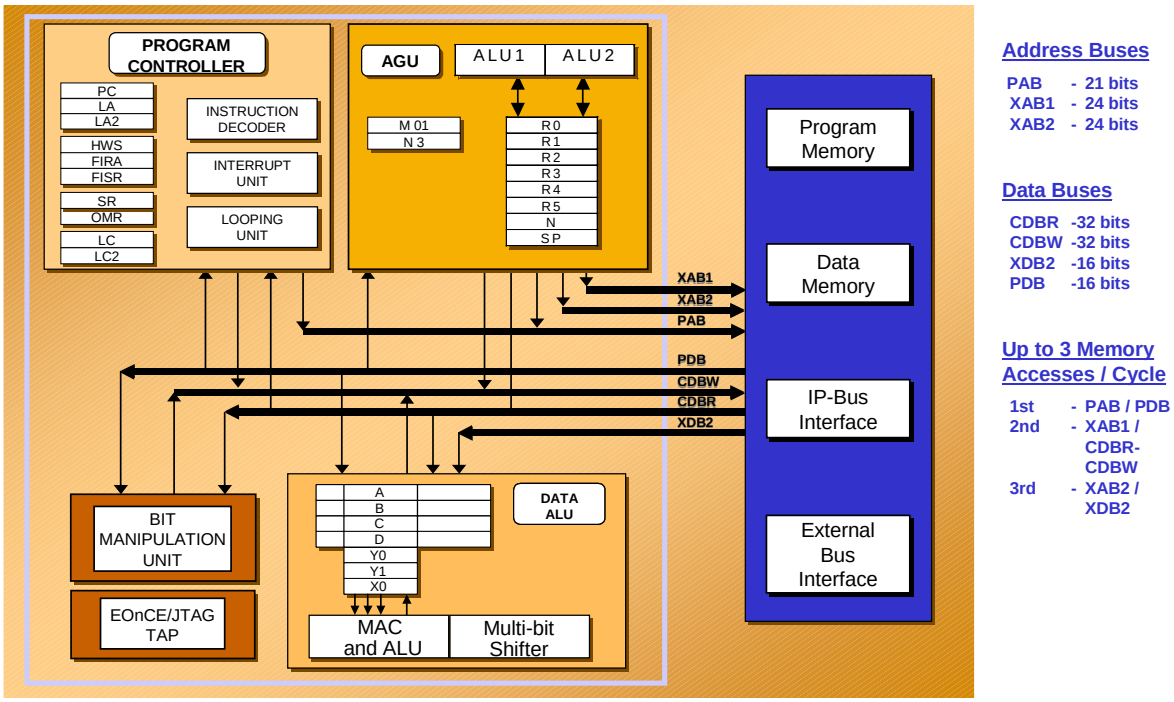


Figure 1-5. 56800E Core Architecture

Key features of the 56800E core include:

- Fully source code-compatible with the 56800 core
- Efficient 16-bit engine with dual Harvard architecture
- Up to 200 Million Instructions Per Second (MIPS) at 200MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four (4) 36-bit accumulators, including extension bits
- Flexible bit manipulation unit with 16- & 32-bit bidirectional shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops (zero overhead)
- Three (3) internal address buses and one (1) external address bus
- Four (4) internal data buses and one (1) external data bus
- Internal 32-bit data buses

- Move operations supporting native single cycle 8-, 16-, and 32-bit data types
- Linear memory space: 4MB program and 32MB data
- Instruction set supports both MCU and DSP functions
- Five (5) software interrupt levels
- Fast interrupt support with arbitrary ISR length
- 19 different controller-style addressing modes and instructions for compact code
- Designed for efficient C-compiler and local variable support
- Software subroutine and interrupt stack, with depth limited only by memory
- JTAG/Enhanced OnCE debug interface for real-time hardware debugging

The 56F8300 Series couples this impressive core with an equally impressive set of peripherals, internal memories, and operating temperature range. Here are some of the features of the 56F8300 processor Series:

- As many as 60 Million Instructions Per Second (MIPS) at 60MHz core frequency
- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Wide range of on-chip memory configurations
- Flash memory security
- Operating range of -40°C to +125°C (at full speed)

The 56F8300 is source code-compatible with all 56F800 components, creating a very easy migration path for users who require increased performance or memory space. The 56F8300 shares many of the peripherals, instruction set, and toolset of Motorola's 8/16 MCU families, providing an excellent roadmap for users of these components.

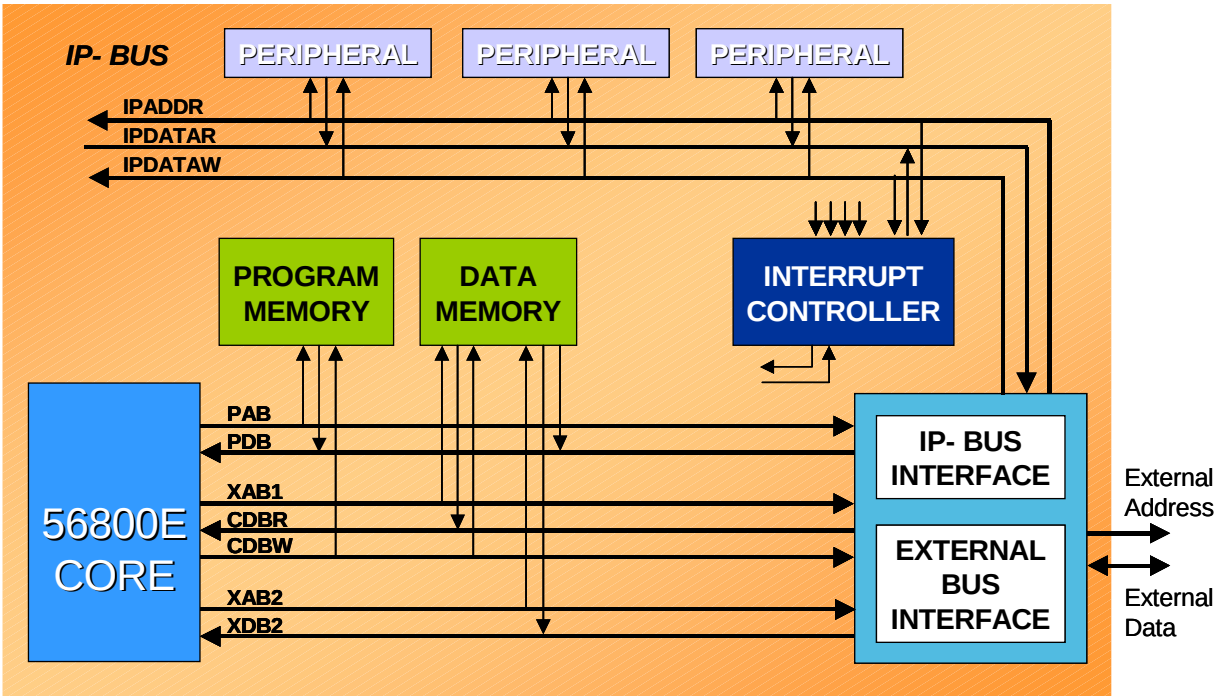


Figure 1-6. 56F8300 System Architecture

The 56800E core has a very powerful bus structure that maximizes the performance of the internal memory. **Table 3** shows the types of memory in the 56F8300 and how each can be used. The Program Flash, RAM, and BootFlash areas are flexible and can store program code or data. The BootFlash is a separate Flash block that comes from the factory programmed with a standard Boot Loader. The BootFlash can be used as program or data space if a special Boot Loader is not required in the application. By making the boot memory Flash-based, the 56F8300 gives the customer the flexibility to replace the standard Boot Loader with his own custom implementation. And since the BootFlash is a separate block of memory, there is an extra level of protection, so that even if power is lost while reprogramming the Program Flash, the device will still boot correctly when power is restored.

The Data Flash and RAM are very flexible and support native 8-bit, 16-bit, or 32-bit types. This means that 8-bit data types, such as a “char” in C, can be very effectively packed and manipulated in memory. But at the same time, 32-bit data types can be moved in a single cycle via the internal 32-bit data buses present in the entire line of 56800E processors.

Table 3: Memory Configuration

Type	Features
Program Flash	Program/Data, 16-bit
Program RAM	Program/Data, 16-bit
Data Flash	Data, 8/16/32-bit
Data RAM	Data, 8/16/32-bit
BootFlash	Program/Data, 16-bit

The 56800E internal bus structure is a modified Harvard architecture with seven internal program and data buses, two of them 32 bits wide. The internal data RAM is dual-ported, so it supports dual accesses in a single cycle. The Data Flash can also be accessed at the same time as the Data RAM. This enables both single- and dual-parallel reads, as well as a program fetch on a single cycle; coupled with the interruptible no-overhead hardware do loops, it gives 56F8300 devices the greatest signal processing performance when operating from Flash.

The number, width, and flexibility of the internal bus structure and how they are connected to the internal memories can be critical in determining how well a processor can zoom through signal processing chores and can efficiently service interrupt-intensive control applications. Serious performance bottlenecks can occur in the absence of the right instructions in the core, the correct bus structure, and the proper memory interface. These bottlenecks can cause performance to be up to six times slower in signal processing than in a 56F8300 device. An advanced hybrid architecture must support the proper number and width of buses to perform true dual-parallel reads and requires an interruptible, zero-overhead do loop support in the instruction set to be able to properly perform the signal processing functions.

The 56F8300 performance is easy to understand: Real 60MHz Flash operation over the entire operational temperature range, with the right structure, number, and width of internal buses to perform control-oriented signal processing without bottlenecks.

The 56F8300 devices' advanced architecture is the successful merger of several types of processors. When Motorola created the 56800E core, it challenged its world-class core designers to create a core incorporating the best points of its 8-bit, 16-bit, and 32-bit MCU cores with the performance of its digital signal processing cores. The designers succeeded with the 56800E. The 56F8300 devices merge the 56800E core with Motorola's best-in-class Flash memory technology and the exceptional level of integration customers have come to expect from the number one supplier of embedded processors. The result is a 56F8300 Series that offers:

- Signal processing power of a DSP
- Ease of programming of a 16-bit MCU
- 32-bit performance with 16-bit code density

3.2 Internal Peripherals

3.2.1 External Memory Interface (EMI)

The EMI peripheral connects directly into the core buses for optimum performance. This high-performance peripheral enables a glueless connection to external memory and peripherals. **Figure 1-7** shows the EMI's block diagram.

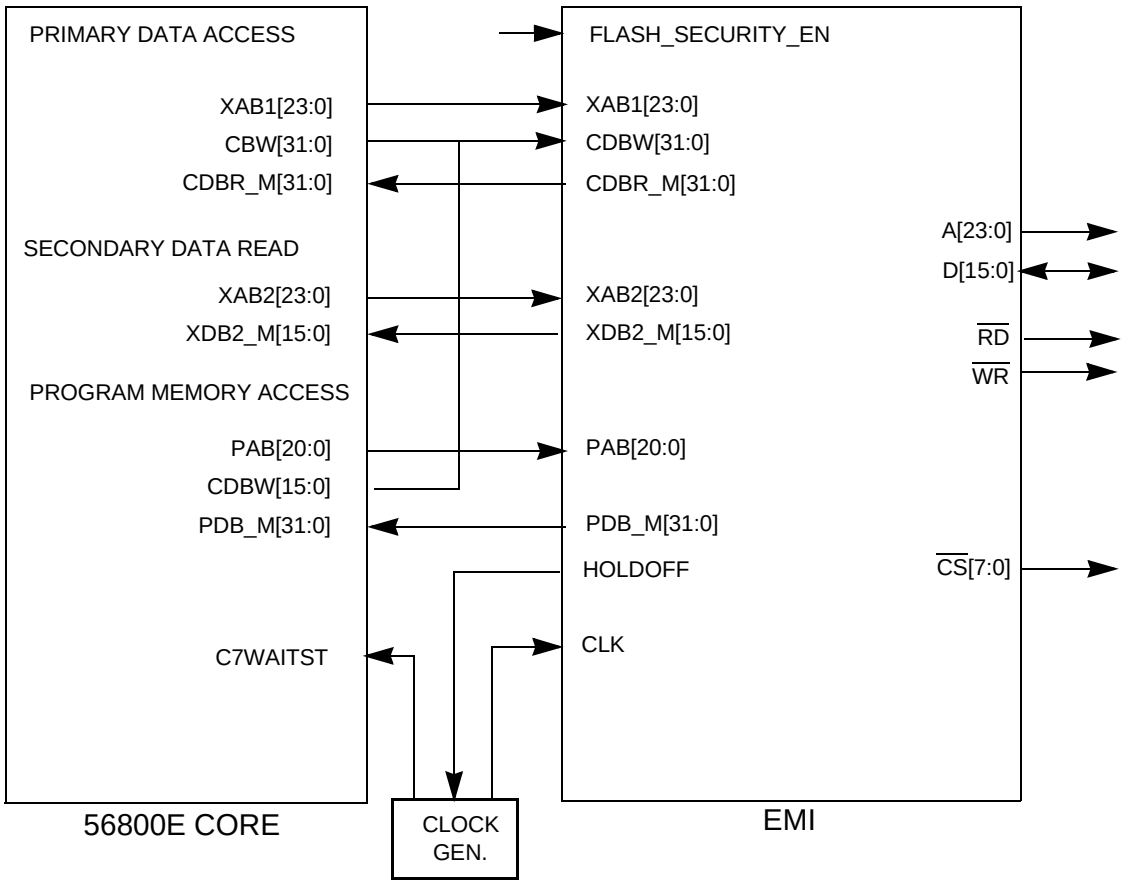


Figure 1-7. EMI Block Diagram

The External Memory Interface:

- Can convert any internal bus memory request to a request for external memory
- Can manage multiple internal bus requests for external memory access
- Has up to eight Chip Select ($\overline{CSn}$) configurable outputs for external device decoding
  - Each $\overline{CS}$ can be configured for program space, data space, (both) program and data space, or neither (disabled)
  - Each $\overline{CS}$ can be configured for read-only, write-only, or read/write access
  - Each $\overline{CS}$ can be configured for the number of wait states required for device access
  - Each $\overline{CS}$ can be configured for the size and location of its activation
  - Each $\overline{CS}$ is independently configured for setup and hold timing controls for both read and write
- Supports disabling external P-space access if Flash Security mode is enabled on a chip
- Supports access rates up to 60MHz
- Supports accessing up to 4MB program space and an additional 32MB data space

With these features and performance, the EMI peripheral can interface to a wide variety and number of memory mapped devices and external memory speeds without the need for external glue circuitry. This saves on system costs, decreases part count, and improves reliability. The operation of the EMI is completely transparent to the software, with the peripheral handling any type of transaction the core requests.

3.2.2 Voltage Regulator and Power Supervisor

The on-board voltage regulator and power supervisor peripherals simplify board design, lower the system cost, and improve the reliability of designs using the 56F8300. With the use of the internal voltage regulator, the 56F8300 can be supplied using a low cost 3.3V supply and it will internally regulate for the other voltages required to operate the internal digital core logic and internal analog peripherals, such as the oscillator and PLL. The hardware design is further simplified by the power supervisor peripheral, which provides power-on reset and low-voltage detection interrupts.

Some of the features and benefits of the voltage regulator are:

- Allows the entire device to be powered by a single 3.3V
- Several internal regulators available
  - One for internal 56F8300 core
  - One or more for internal analog circuitry
- Regulators converts 3.3V input to 2.5V operating voltage
  - Reduces overall system cost
  - Controls power usage
  - Controls system noise floor
- I/O ports designed to interface at a TTL-compatible level
- Can be disabled to reduce power consumption

Some of the features and benefits of the power supervisor are:

- Holds device in reset until there is enough voltage (V_{DD} > 1.8V) for on-chip logic to operate at the oscillator frequency
  - Precludes any problems associated with false restart

- Low-voltage detectors generate high-priority interrupts
  - Two low-voltage detect signals are used to initiate a software-controlled shutdown when the supply voltage drops below acceptable levels (either 2.2V or 2.7V)
- Reduced system cost
  - Eliminates need for external power monitor

3.2.3 On-Chip Relaxation Oscillator and On-chip Clock Synthesis (OCCS)

The OCCS enables the use of a wide variety of clocking sources and operating frequencies. Some of the features and benefits of the OCCS peripheral are:

- Several dynamically selectable system clock sources available
  - Internal 8MHz relaxation oscillator (on some chips)
  - External 8MHz ceramic resonator
  - External 8MHz crystal
  - External clock source
- Dynamically programmable Phase Locked Loop (PLL) enables operating frequency up to 60MHz
  - Configurable power/speed options
- Generates an interrupt if either loss of clock, or loss of lock, or both, occur
  - Improves system safety and reliability
- Internal oscillator drive circuitry enables use of crystal or ceramic resonator
  - Lower system cost by eliminating active external components
  - Lower system cost using low-cost ceramic resonator

The features of the OCCS offer superior system cost savings while providing greater flexibility in selecting the operating frequency that provides the proper performance while utilizing the least amount of power. The loss of lock and loss of clock detection provide greater safety and reliability by ensuring that the proper operating frequency is present. Even if the external clock source is entirely lost, the PLL continues to operate for a specified number of clock cycles, enabling safe system shutdown.

The 56F8322 and 56F8323 devices are equipped with an internal 8MHz relaxation oscillator that can be used with the clock source. The internal relaxation oscillator has high accuracy because it is factory trimmed to 0.25% of 8MHz at room temperature. Over the full operating temperature range, this variation will stay within 2% of 8MHz. By using the internal temperature sensor and profile of frequency-to-temperature provided in the data sheet, the trim values can be adjusted for temperature variations and a frequency accuracy better than 2% can be maintained. The internal relaxation oscillator provides system cost savings by eliminating the need for external components entirely. The internal relaxation oscillator lowers system part count, system cost, and improves system reliability.

3.2.4 Quad Timer Module

The 56F8300 devices have from two to four Quad Timer modules. Each Quad Timer module is an exceptionally powerful timer that offers an unprecedented number of features, which includes these features and benefits:

- Four 16-bit general purpose up/down timers per module
- Individually programmable
  - Input capture trigger
  - Output compare capture
  - Clock source
- Pins available as general I/O when timer(s) not in use
- Input pins may be shared within a Quad Timer module
- Counters in module can be daisy-chained to yield longer counter lengths
- Up to 12 operation modes:
  - Fixed-Frequency PWM Mode
  - Variable-Frequency PWM Mode
  - Stop Mode
  - Count Mode
  - Edge-Count Mode
  - Gated-Count Mode
  - Quadrature-Count Mode
  - Signed-Count Mode
  - Triggered-Count Mode
  - One-Shot Mode
  - Cascade-Count Mode
  - Pulse-Output Mode

These timers can be used effectively for a wide variety of system applications from power factor correction to implementing a low-cost Digital-to-Analog Converter (DAC), as shown in **Figure 1-8**.

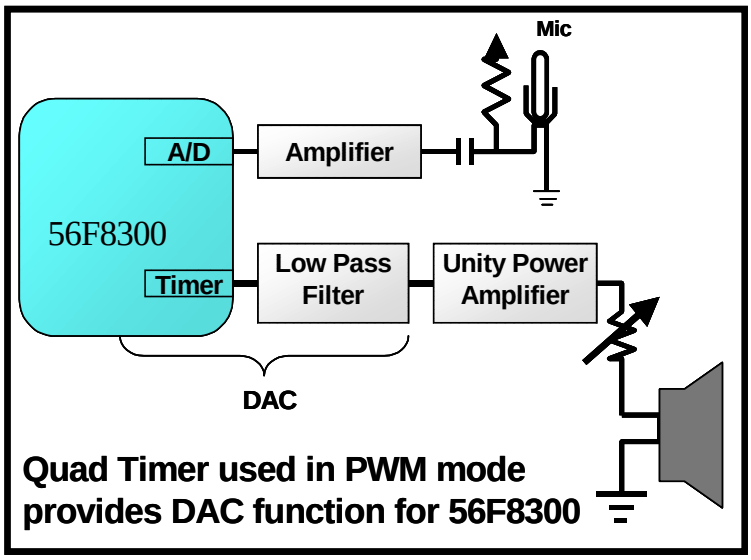


Figure 1-8. Sample Use of Quad Timer

The powerful features of the Quad timer module, the ability to flexibly connect modules to external I/O pins, and its flexible operating frequency/clocking, lower system costs by simplifying external circuitry and software.

3.2.5 Quadrature Decoder

The 56F8300 Quadrature Decoder is a very feature-rich peripheral that not only provides the interface to a encoder but also provides added features which facilitate software development. Some of the features and benefits of the Quadrature Decoder are:

- Four inputs per decoder
  - Phase A
  - Phase B
  - Index
  - Home
- Captures all four transitions on two-phased inputs
  - Extracts actual shaft position and direction
  - 32-bit position counter; initialized by software or external events
  - Pre-loadable 16-bit revolution register
- Index input
  - Resets position counter
  - Begins integrating a new revolution value
- Home input
  - Initializes position counter
- Configurable glitch filter for inputs
- Can operate as single-phase pulse accumulators
- Watchdog timer detects non-rotating shaft condition

- 16-bit revolution counter based on index signal
- 16-bit “delta count” velocity measurement
- “1/x” velocity measurement based on signal period
- Optional interrupt on home or index signal
- Optional initialization of position on home or index signal

3.2.6 Three-Phase PWM Module

The 56F8300 PWM is unique in the industry, providing the capability to drive a broad range of motor types, well suited for power conversion systems, exceptionally high performance, and features to satisfy the most safety-critical application. The PWM module can be used very effectively with AC Induction, Brush DC, Brushless DC, Switched Reluctance, Permanent Magnet, and stepper motors. It is also optimized for performance in power conversion systems. Here are some of the features and benefits of Motorola’s PWM module:

- Each PWM module includes 6 PWM channels and a number of fault inputs
- Complementary PWM signal pairs, independent PWM signals, or a combination
  - High current sink capability on PWM pins with TTL compliance
  - Programmable PWM output polarity
  - Programmable PWM frequency and PWM pulse width cycle
  - Programmable fault protection
  - Individual software-controlled PWM output
- Features of complementary channel operation
  - Programmable dead-time insertion
  - Separate top and bottom pulse width correction (dead-time compensation via current status sensing or software)
  - Separate top and bottom polarity control
- Double-buffered PWM register
  - Reload interrupt with programmable interrupt rate
  - Integral reload rates from 1 to 16
  - 15-bit PWM pulse width register
  - 15-bit PWM period register
  - 3-bit PWM clock prescaler
- Center-aligned or edge-aligned waveforms
  - Full 0% to 100% modulation
  - 33.3ns resolution at IPBus clock = 60MHz for center-aligned mode
  - 16.7ns resolution at IPBus clock = 60MHz for edge-aligned mode
- Up to four programmable fault inputs for each PWM module
  - Programmable interrupt capability and separate interrupt vector for each input
  - Programmable fault partitioning (disables some or all PWM outputs)
  - Arbitrarily assigns the fault inputs to any of the PWM pins, which allows each pair of PWM channels to be shut down individually
  - Fault input filter prevents a false fault condition
  - Programmable automatic fault clearing or manual fault clearing
  - Operates properly even without system clock

- Capable of multiple motor control
  - 60 MIPS hybrid controller allows execution of multiple tasks
  - Separate PWM pulse width register for each PWM channel
  - Separate fault signal input for each PWM pair
  - Separate current status input for each PWM pair

Figure 1-9 illustrates a partial functional block of the PWM module.

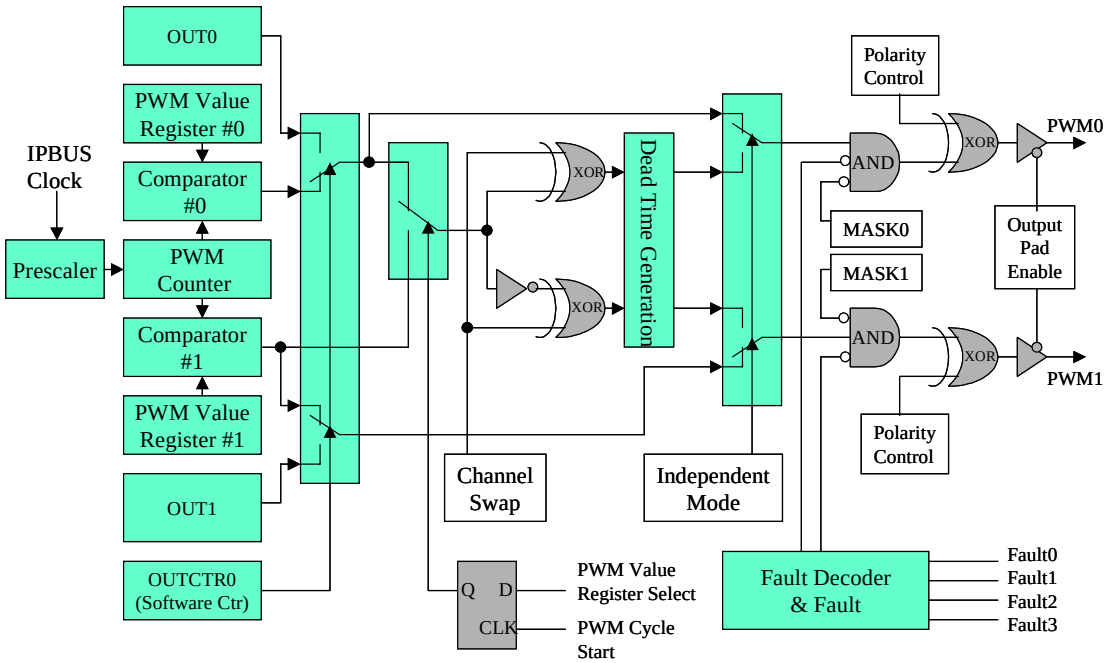
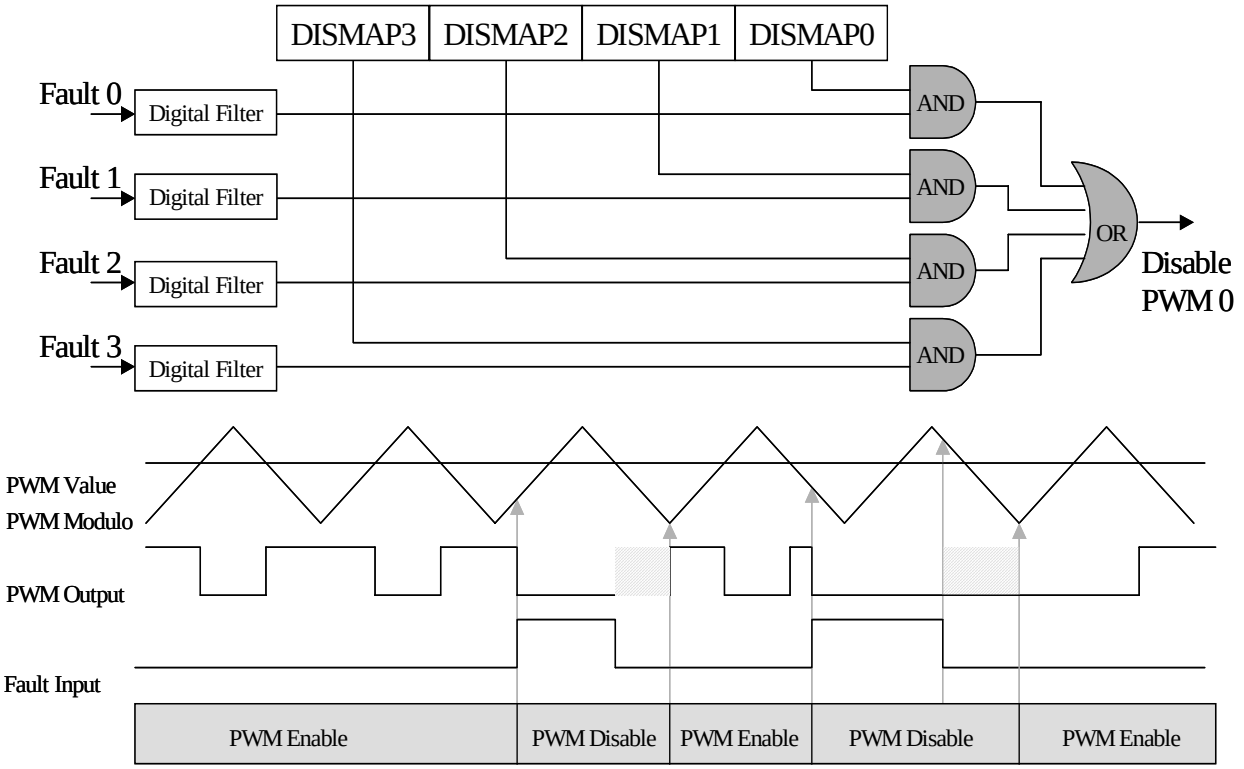


Figure 1-9. PWM Module Functional Block Diagram

The following sections offer examples using PWM features. **Figure 1-10** shows configuration of the PWM fault inputs to selectively disable a PWM complementary channel, then automatically clears the fault on the next PWM cycle. The fault generation and clearing occurs without software intervention, but the software can be notified of the event with the generation of an interrupt. This demonstrates how the PWM can be used in a safe but fault-tolerant mode.



*When Fault logic returns to logic 0, the PWM restart at beginning of the next half cycle.

Figure 1-10. PWM Fault Decode And Automatic Clearing

Figure 1-11 demonstrates how the two PWM modules present on many of the 56F8300 components can be used. In this example, it performs unity power factor correction (power flow direction control) with regeneration to mains. The second PWM could also be used to drive an independent three-phase motor.

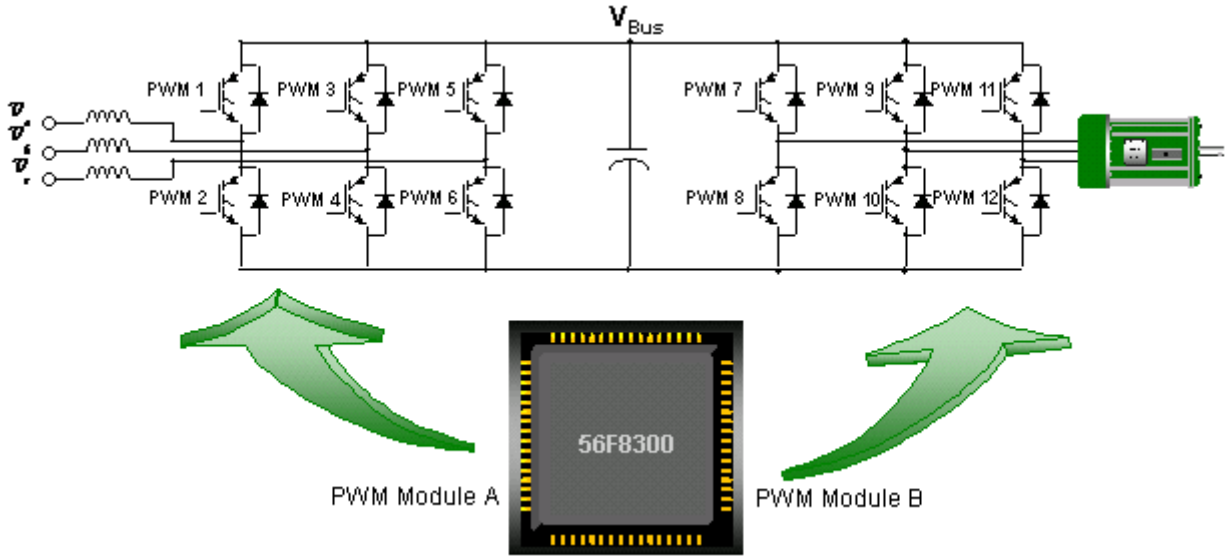


Figure 1-11. Example Using Two PWMs

Figure 1-12 shows the effect of using the PWM module 's waveform distortion correction feature. In certain operating conditions, the results can be significant. The corrected waveform results in smoother, quieter, and more efficient motor operation.

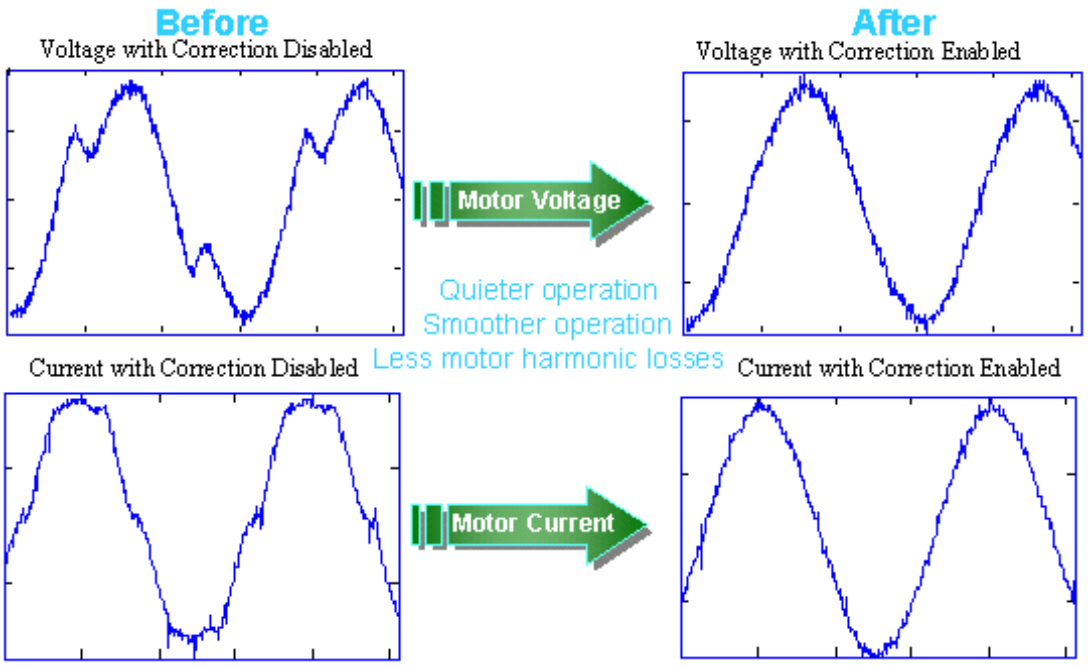


Figure 1-12. Actual Waveforms Taken on a 1/2 Horsepower Motor

The "write once" feature of certain PWM registers protects critical system configuration data from accidentally being changed. The parameters that can be covered by this protection are:

- Dead-time value
- Fault-disable mapping
- PWM output polarity bits
- Independent or complementary (tandem) PWM operation

In a typical motor control application, these parameters are constants which are not expected to change for a given system configuration. This mode is optional, in that the software developer can choose whether to make these parameters write protected after configuring them. If write protection is not enabled, then they can be modified without restriction.

3.2.7 ADC Module

The 56F8300 Analog-to-Digital (ADC) Converters are very powerful, offering high frequency operation of up to 1.2µs per conversion, and are very accurate, offering twelve bits of resolution. **Figure 1-13** shows a functional block diagram of the ADC module. As shown, it has two sample and hold circuits and two conversion units, enabling simultaneous conversions.

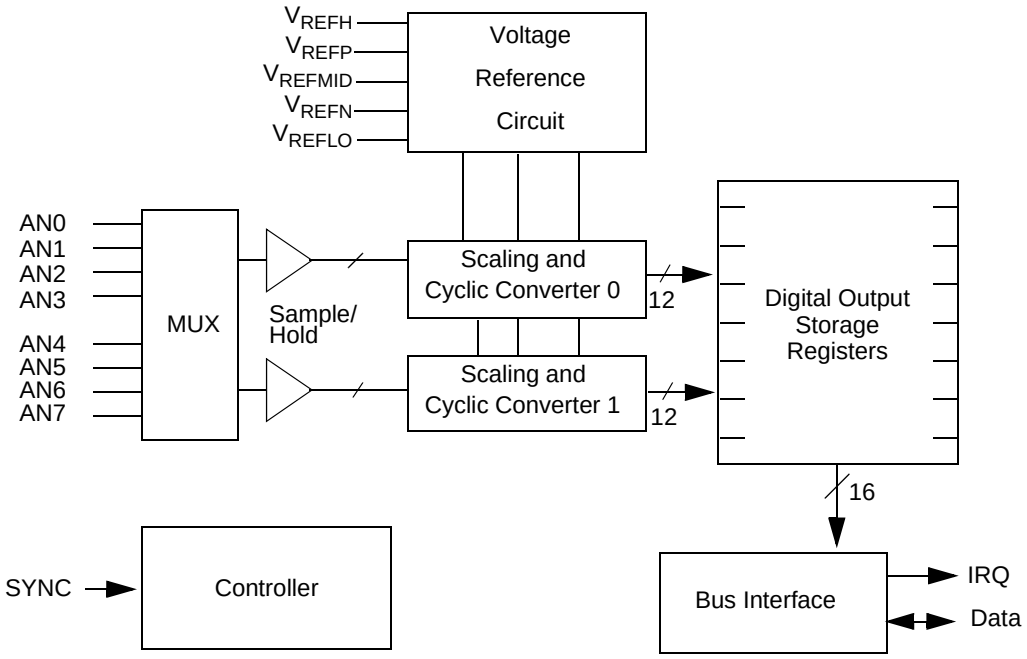


Figure 1-13. ADC Functional Block Diagram

The ADC has a sophisticated set of operating modes and capabilities. Each 56F8300 devices has either one or two of these modules. Here are some of the features and benefits of Motorola's ADC module:

- 12-bit resolution
- Two ADC conversion units per module, with up to eight analog inputs
- Sampling rate up to 1.66 million samples per second
- Single conversion in 1.2µs
- Eight conversions in 5.3µs by using simultaneous sampling mode
- Can be synchronized with Pulse Width Modulators (PWM)
- Simultaneous or sequential sampling
- Eight-word result buffer
- Sample correction via programmable offset
- Current injection protection circuitry
- Software self-calibration capability
  - Removes gain and offset errors
- Interrupt generating capabilities
  - End-of-Scan, zero crossing, high/low limit check
- Two outputs formats available
  - Two's complement
  - Unsigned
- Power-Down and Power-Saving Modes

The advanced features of the 56F8300 Series make it an excellent choice for industrial applications. **Figure 1-14** shows an ADC module used for simultaneous conversions with the PWM module's trigger source. Using the simultaneous mode, two conversions occur at the same exact time. And since the ADC inputs have a software-controlled input mux, any two ADC input lines can be simultaneously sampled.

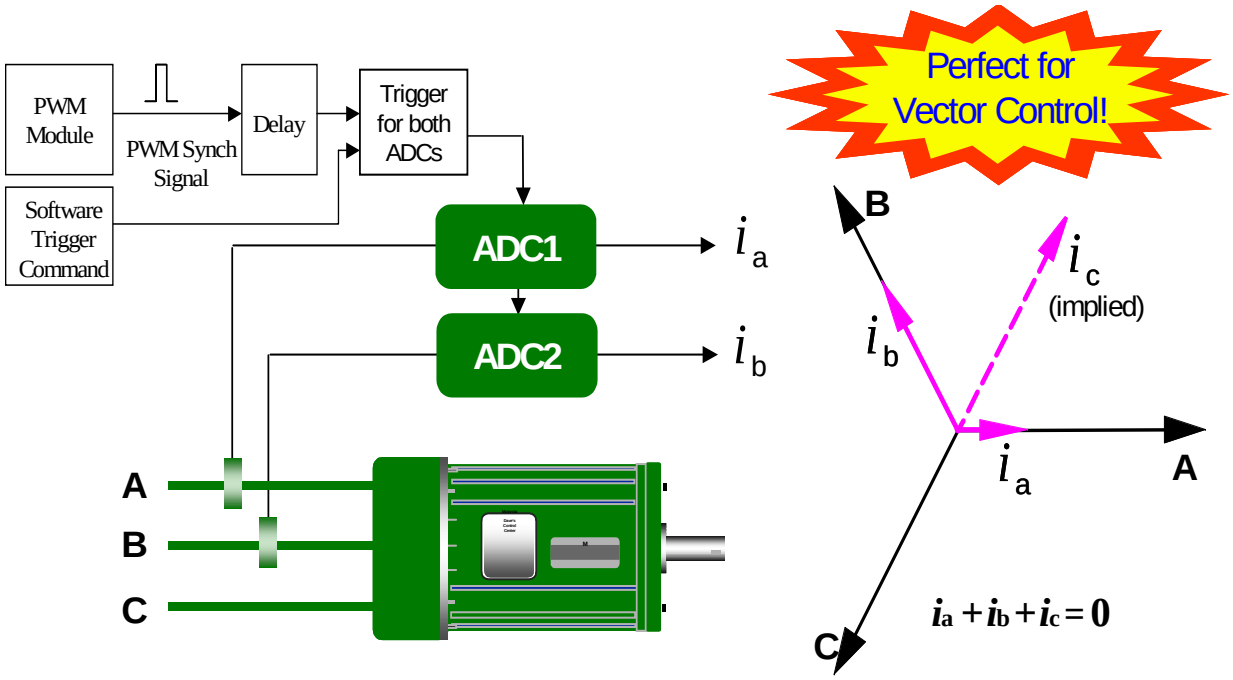


Figure 1-14. Simultaneous ADC Conversion

The triggering mechanism for the ADC is very flexible. The main sources are from the internal software or through a hardware timer. The timer can be free running, tied to an external input, or, as demonstrated, tied to the PWM. **Figure 1-15** shows how to use the hardware timer to precisely delay the conversion trigger, allowing for exact positioning of the sample where needed and providing the lowest possible jitter. This method can be used with the PWM or an external trigger signal.

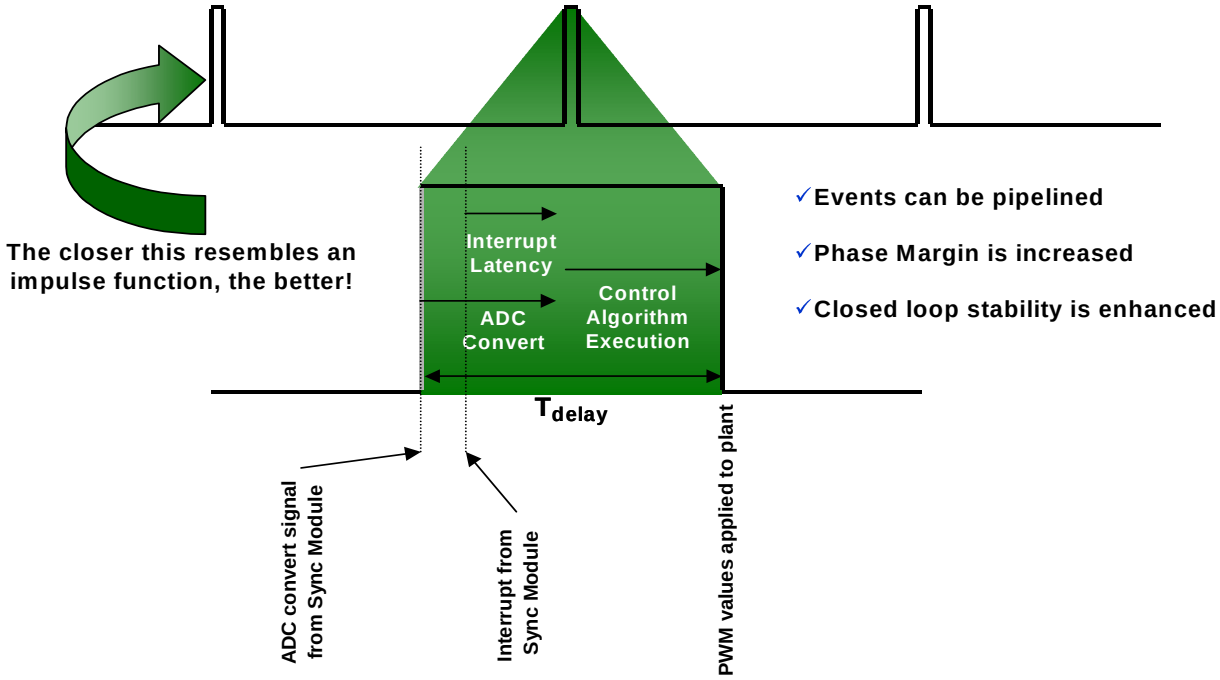


Figure 1-15. ADC Delay Triggering Mechanism

The ADC also has unique capabilities to process and extract information from ADC samples. Level and threshold detection are shown in **Figure 1-16**. The ADC can perform limit checking and zero crossing detection with no CPU intervention. Each ADC channel has its own upper, lower, and threshold comparators, allowing for completely independent channel operation and levels.

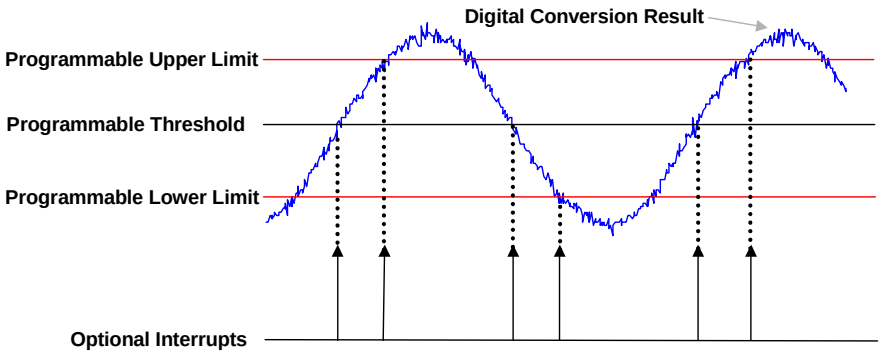


Figure 1-16. ADC Limit and Threshold Crossing

The ADC module has an internal self-calibration capability. Internal to the ADC is a highly accurate voltage reference system that can feed stable known voltages into any ADC input, allowing for software to read the conversion and adjust for any residual gain and offset errors.

The ADC also has a sophisticated set of power-down modes that still let normal conversions occur. The ADC can automatically power itself down between conversions and wake itself back up when a trigger event occurs.

3.2.8 Temperature Sensor

The 56F8300's temperature sensor is used to determine the internal operating temperature of the component and, in safety-critical applications, provides a mechanism to determine if an over temperature failure condition exists. The temperature sensor is an IPBus peripheral and temperature readings may be taken through an ADC channel.

The temperature sensor module features are:

- Operating range: -40°C to +150°C junction temperature
- Monotonic with temperature
- Resolution is better than 1°C/bit over a 10-bit range from 0 to 3.6V
- Use is optional, depending on customer's application
- Temperature Sensor has a power-down mode

Figure 1-17 shows a typical use of the temperature sensor.

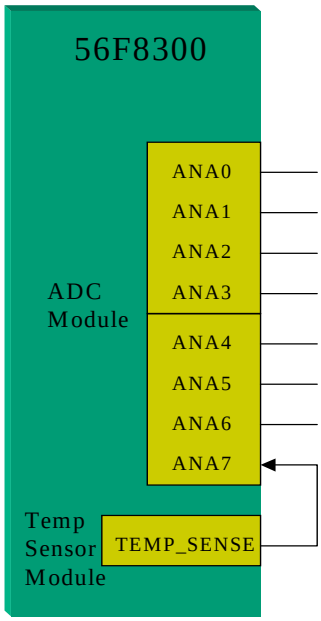


Figure 1-17. Temperature Sensor Use Model

3.2.9 FlexCAN Module

The FlexCAN module is a communication controller implementing the Controller Area Network (CAN) protocol, an asynchronous communications protocol used in automotive and industrial control systems. It is a high-speed (1Mbit/sec), short distance, priority-based protocol which can communicate using a variety of mediums (for example, fiber optic cable or an unshielded twisted pair of wires). The FlexCAN module supports both the standard and extended identifier (ID) message formats specified in the CAN protocol specification, revision 2.0, part B.

The CAN protocol was primarily, but not exclusively, designed to be used as a vehicle and industrial serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the harsh EMI environment, cost-effectiveness and required bandwidth. The CAN protocol is supported by a large variety of devices, enabling designers to easily create very cost-effective networked designs.

Here are some of the features and benefits of the FlexCAN module:

- Version 2.0-compliant
  - Standard and extended data frames
  - 0-8 bytes data length
  - Programmable bit rate up to 1 Mbps
  - Support for remote frames
- “Time Stamp”, based on a 16-bit free-running timer
  - Global network time, synchronized by a specific message
- Two serial message buffers for buffer frame
- Sixteen flexible message buffers of 0-8 bytes data length, each configurable as Receive (Rx) or Transmit (Tx); all support standard and extended messages
- Flexible, maskable identifier filter
- Programmable wake-up functionality with integrated low-pass filter
- Separate signaling and interrupt capabilities for all CAN Receive (Rx) / Transmit (Tx) error states
- Three low-power modes

3.2.10 Serial Communication Interface (SCI) Module

The SCI operates as a Universal Asynchronous Receive and Transmitter (UART) for industry standard serial communications, such as RS-232. It can also be used in many other applications requiring reliable serial asynchronous communication. The following are some of the features and benefits of the SCI module:

- Full-duplex operation provides simultaneous data transmit and receive
- Half-duplex operation allows data transmit and receive via single wire
- Separately enabled transmitter and receiver
- 13-bit baud rate selection
- Standard mark/space non-return-to-zero (NRZ) format:
  - Programmable 8-bit or 9-bit data format
- Separate receiver and transmitter CPU interrupt requests
- Programmable polarity for transmitter and receiver
- Two receiver wake-up methods:
  - Idle line
  - Address mark
- Interrupt-driven operation with eight flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

Figure 1-18 shows two examples of the SCI used as a multiprocessor communication network.

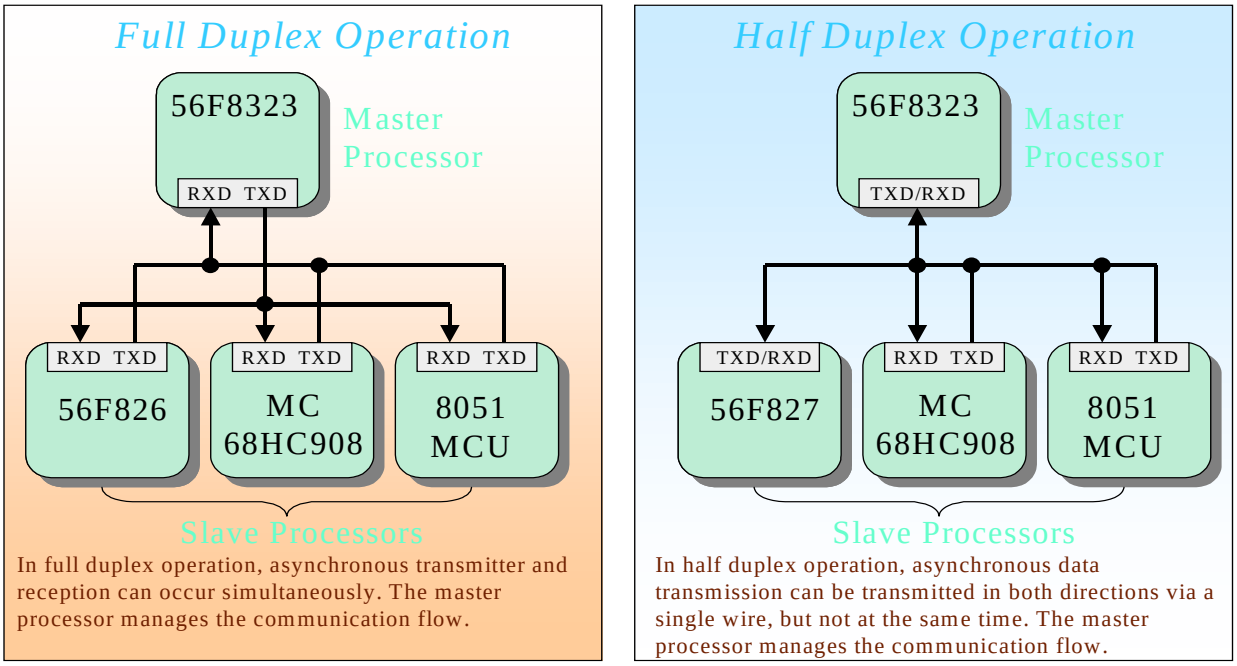


Figure 1-18. SCI: Multiprocessor Communication

3.2.11 Serial Peripheral Interface (SPI)

This synchronous serial interface is double buffered and operates in wide variety of modes, rates, and bit lengths, enabling the glueless connection to external peripherals and other processors at rates up to 30 Mbps. Some potential applications are in LCD drivers, A/D subsystems, and MCU systems. Here are some of the features and benefits of the SPI module:

- Supports interprocessor communications in a multiple master system
- Supports demand-driven master or slave devices with high data rates
- Full-duplex operation
- Double-buffered operation with separate transmit and receive registers
- Programmable length transmissions from 2 to 16 bits
- Programmable transmit and receive shift order, MSB or last bit transmitted
- Four master mode frequencies (maximum = bus frequency / 2)
- Maximum slave mode frequency = bus frequency
- Serial clock with programmable polarity and phase
- Two separately enabled interrupts:
  - Receiver Full
  - Transmitter Empty
- Mode fault and overflow error flag with device interrupt capability

3.2.12 Computer Operating Properly (COP)

The Computer Operating Properly (COP) module assists software recovery from runaway code. The COP is a free-running down counter and once enabled, is designed to generate a reset when reaching zero. Software must periodically service the COP to clear the counter and prevent a reset.

Some of the features and benefits of the COP Module:

- Free-running counter designed to generate a chip-wide reset on overflow
- The length of the time-out period is programmable
- Programmable Wait and Stop mode operation

3.2.13 General Purpose Input/Output (GPIO)

The General Purpose Input/Output (GPIO) module allows direct read or write access to pin values, or the ability to assign a pin to be used as an external interrupt. All of the digital pins for the on-board peripherals can also be individually assigned to be GPIO and individually assigned a direction. Each GPIO has programable pull-ups. The GPIO also has a push-pull mode to efficiently implement a keypad interface.

The GPIO module's features include:

- Individual control for each pin to be in either Normal or GPIO mode
- Individual direction control for each pin in GPIO mode
- Individual pull-up enable control for each pin in either Normal or GPIO mode
- Supports use with a keypad interface with push-pull I/O
- Ability to monitor pin logic values, even when GPIO are not enabled by using the GPIO_X_RAWDATA register
- Interrupt assert capability

3.2.14 JTAG/EOnCE Module

The enhanced on-board emulation module enables true full-rate emulation without the need for expensive hardware emulators. Simply attach to the processor, using the industry standard JTAG interface and you can perform powerful, non-intrusive real-time debugging. Some of features and benefits of the JTAG/EOnCE module are:

- Both are accessed through a common JTAG/EOnCE interface
- Retains debug control in target system
- System-level debugging at one of three levels:
  - Non-intrusive real-time debug
  - Minimally-intrusive real-time Debug
  - Breakpoint and Step mode; core is halted
- Nexus Level 0-compliant
- Real-time data exchange through the JTAG port
- Advanced breakpoint capability
- Change of flow buffer
- Event viewing through a terminal
- Resources accessible through JTAG or through the core

3.3 Software Development Tools and Code

The 56F8300 products are supported with an exceptional and complete set of tools, enabling developers to reach an unprecedented level of productivity. These tools include the following:

- **CodeWarrior Development Studio 56800 Hybrid Controllers** - A Windows-based visual IDE that includes an optimizing C compiler; assembler and linker; project management system; editor and code navigation system; debugger; simulator; scripting; source control and third-party plug-in interface
- **Processor Expert (PE)** - A Rapid Application Design (RAD) tool that combines the ability to create an easy-to-use component-based software application with an expert knowledge system. PE is fully integrated with CodeWarrior.
- **PC Master Software** - This tool provides customizable real time debug and control of a fully operational target. Features include Real Time Data Capture, Real Time Data Logging, Graphical data Visualization, Command and Status exchange, and Real time graphical analysis.
- **Hardware Tools**- The 56F8300 devices are supported with a complete set of evaluation modules (EVMs) and Demo kits, which supply all required items for rapid evaluation and software and hardware development. In addition, several command converter options exist for customer target system debugger/emulation connection.

These tools provide the elements required for rapid software and prototype development, testing, and field support. The following section describes these tools in greater detail.

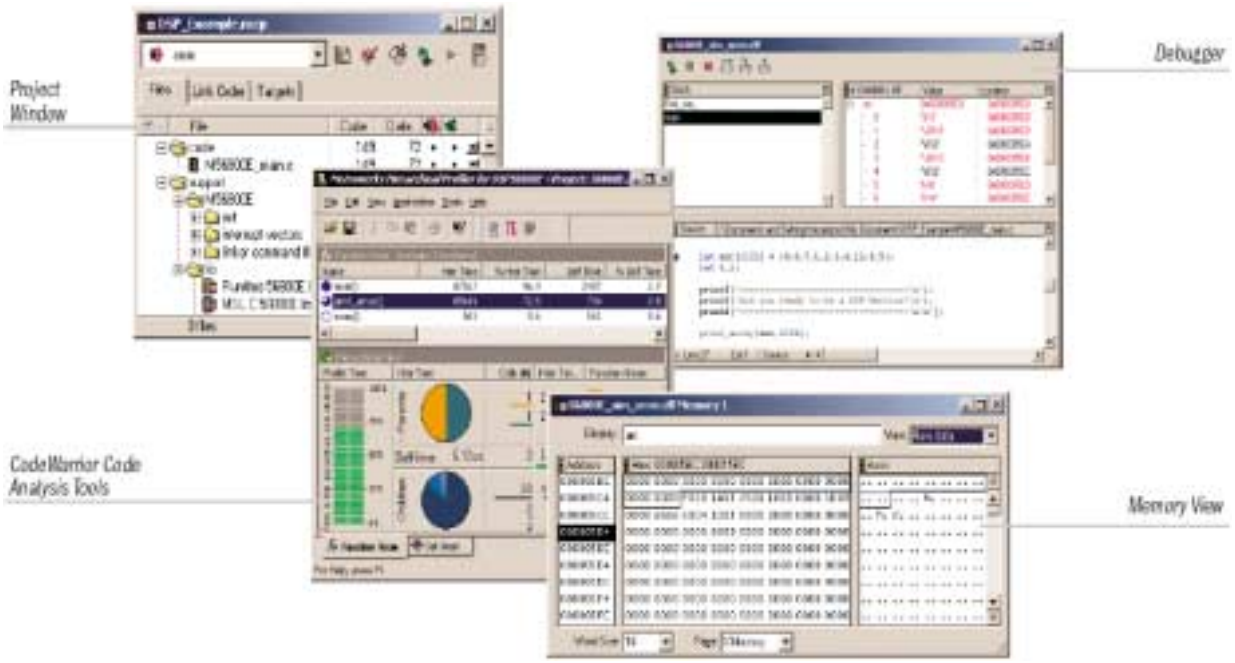


Figure 1-19. CodeWarrior IDE

Figure 1-19 shows some of the CodeWarrior IDE tools and demonstrates its graphical nature. Some of the features and benefits of the award-winning CodeWarrior IDE are:

- A development environment that seamlessly integrates the project manager, build system, editor, compiler, linker and debugger

- Support for 56F8300, 56F800, and 56850 series, including integrated EVM and Demo board support
- An advanced instruction set simulator that enables hardware/software co-design
- A highly optimized C compiler ensures the smallest code size and fastest execution time
- A graphical source-level debugging tool solves complex problems quickly and easily
- Compiler optimization takes advantage of the device's loop constructs
- Processor Expert with components for the 56F8300 on-chip peripherals and software algorithms
- Supports CodeWarrior Analysis Tools for Motorola DSP56800E, version 1.0
- Supports CodeWarrior HTI (Host Target Interface) that enables data transfers to be over 85% faster
- Supports CodeWarrior Turbo Downloader, which transfers data 50% faster than over a parallel port

The Processor Expert Rapid Application Design (RAD) tool combines the ability to create easy-to-use component-based software applications with an expert knowledge system that is entirely graphically driven. The PE environment tool:

- Supports rapid application development
- Allows component oriented programming
- Provides expert advice if necessary
- Delivers instantly functional, auto-generated code
- Provides tested, ready-to-use code

The PE system can both advise you on how to best use Motorola's components and can supply fully tested, professional-quality code ready to use in your system. The PE system delivers this support in an intuitive, graphical system. The features of the PE system are possible because the PE system:

- Has been developed by experienced programmers of embedded systems
- Contains an expert knowledge system working in the background which checks all settings
- Provides context help and access to CPU/MCU vendor documentation
- Is tested according to ISO testing procedures

Processor Expert is not only about the tool, but about the right approach. Part of this approach is providing software components at two different levels of abstraction; the two key types of abstraction are shown in **Figure 1-20**.

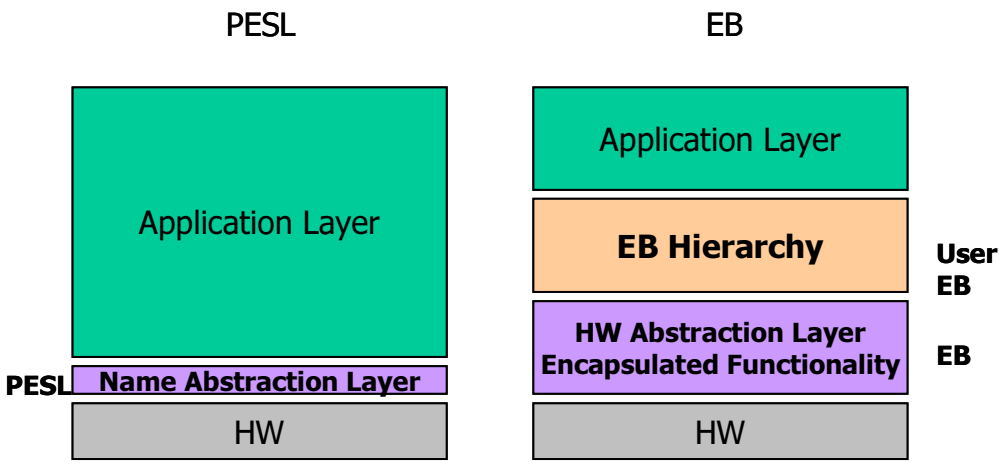


Figure 1-20. PE Software Abstraction Layers

The software that PE generates according to your graphical configuration are either at the Processor Expert System Library (PESL) level or the Embedded Bean (EB) level. The PESL level is highly efficient and simple, but it is at a low level and provides a low level of abstraction from the hardware as well as a low level of fictionalizing. Using the PESL software requires a greater degree of knowledge of the component peripherals and the application is generally less portable across platforms.

The EB level is at a higher level that provides much more functionality and a high level of abstraction. Using embedded beans doesn't require nearly as much knowledge of the underlying hardware and provides for much improved portability of code across platforms. Where the PESL level is closely tied to on-board peripherals, the EB level provides for both peripheral drivers and an extensive set of application, I/O, and signal processing libraries.

In any given application PESL, EB, or both, can be used. Motorola's Demo boards and EVM kits include reference applications using PE to further aid in the rapid development of end applications.

Figure 1-21 illustrates an example using PC Master Software to digitally probe signals internal to the software operating on the 56F8300 device. The application is run in real time and the data is exchanged in real time from the 56F8300 processor to the oscilloscope display function in the PC Master Software running on the Windows host computer. Some of the features of the PC Master Software are:

- Real time data capture
- Real time data logging
- Command and status exchange
- Real time graphical analysis
- Graphical environment
- Visual Basic Script or Java Script can be used for control of target board
- Easy-to-understand navigation
- Connection to target board is possible over a network, including the Internet
- Demo mode with password protection support
- Visualization of real-time data in Scope window

- Acquisition of fast data changes using integrated Recorder
- Value interpretation using custom-defined text messages
- Built-in support for standard variable types (integer, floating point, bit fields)
- Several built-in transformations for real type variables
- Automatic variable extraction from Metrowerks' CodeWarrior linker output files (MAP, ELF)
- Remote control of application execution

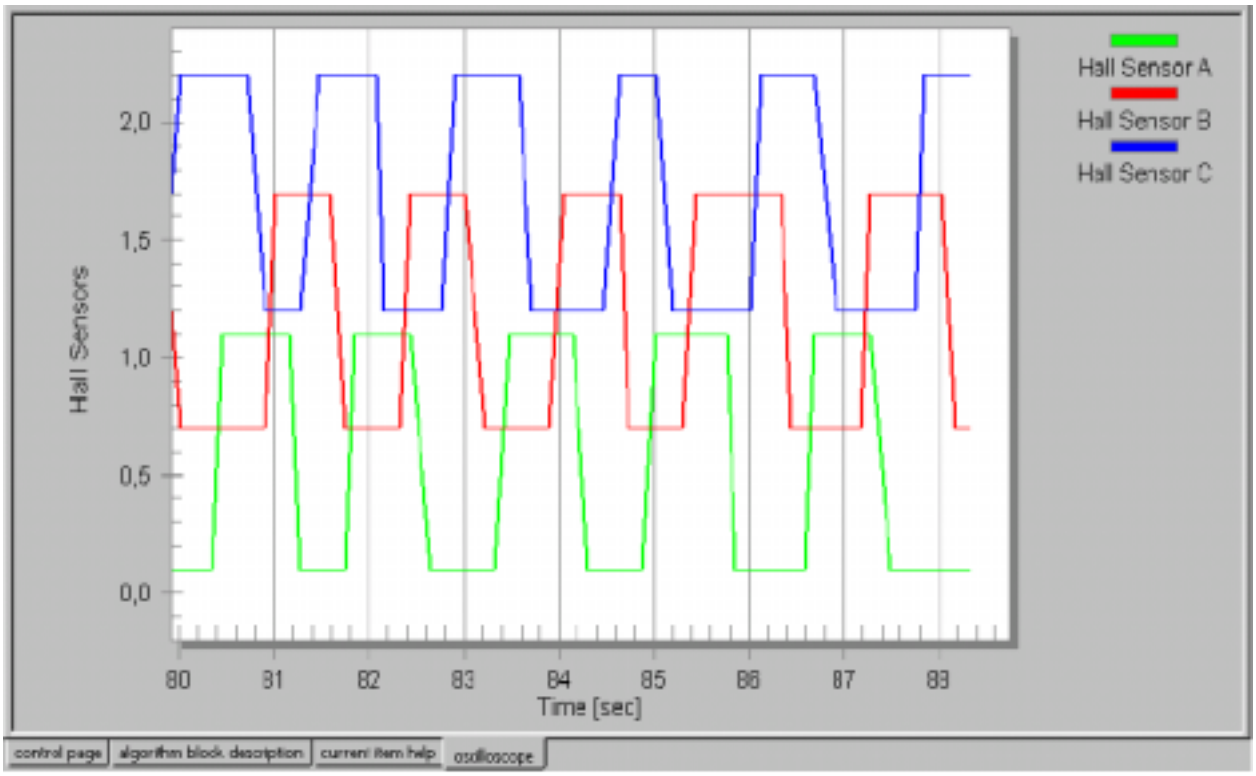


Figure 1-21. Example PC Master Software Screen

The PC Master Software tool provides an excellent capability to develop and debug an application while running in real time operation and to analyze data in a graphical form. Because the PC Master Software is web browser-based it is easily customizable by the customer. The PC Master Software can be easily used by customers to create custom graphical user interfaces for software running on a 56F8300 device. In this way the PC Master Software tool can help customers quickly develop high impact graphical user interfaces into demonstration systems to support demonstrations to their own end customers.

The EVM and Demo kits include everything required to start developing code immediately, including all documentation, required cabling, power supply, CodeWarrior IDE, Processor Expert, and a rapid development system CD. These kits are exceptional values, enabling rapid evaluation and development at a very low cost. **Figure 1-22** shows the how the EVM kit is used.

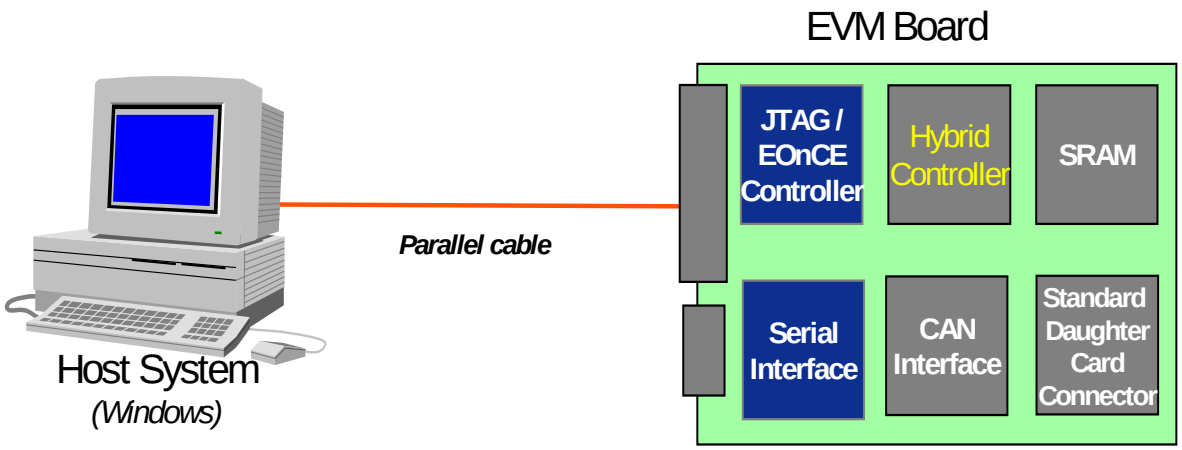


Figure 1-22. EVM Kit

Here are some of the standard features of the EVM/Demo kits:

- Parallel port connection to Host PC
- Non-intrusive debug via the EOnCE port
- JTAG connector
- RS-232 serial connector
- Expansion memory (not available on the 56F8323 or Demo kit)
- Standard daughter card connection (not available on the Demo kit)
- CAN PHY layer
- Power supply
- CodeWarrior CD
- Processor Expert
- 56F8300 Series Rapid Development System CD

In addition to the EVMs and Demo kits, a full line of low-cost command converters are available to enable connection to the JTAG/OnCE port on the user's custom hardware implementation.

4. Migration Path to Higher Performance for the Motorola Controller Continuum

The 56F8300 Series of devices complements Motorola's 56F800 embedded Flash portfolio. It is not a replacement for any of these devices, but instead provides an excellent growth path for customers requiring its enhanced performance, memory configurations, and peripherals.

The 56800E core is fully source code-compatible with the 56800 core. Customers who have developed products on a 56F80x device have a very straightforward and easy transition into the 56F8300 for applications requiring enhanced features and performance. The 56F8300 devices also share the powerful CodeWarrior IDE, EVMs, and development systems of the 56F80x product line. Like the 56800 Series of processors, the 56F8300 has broad software support, including motor control, industrial, automotive, and general purpose libraries and applications.

The 56F8300 Series also provides an excellent migration path for customers of our 8/16-bit MCU devices who require increased performance, as well as the ease of programming and excellent integration they have today. These users will see their migration to the 56F8300 eased by the availability of similar on-chip peripherals with the capabilities and interfaces they expect. The 56F8300 also has many of the same language constructs and shares a common CodeWarrior and Processor Expert tool chain with current and future 8/16-bit MCU devices.

The 56F8300 Series of devices is a natural migration path for today's customers of Motorola's 56F80x and 8/16 bit MCUs who require additional performance and capabilities.

Some of the improvements in the 56F8300 when compared to its companion 56F80x Series of components:

Table 4: 56F8300 Enhancements Compared to 56F80x

Enhancements
Increased performance, up to 60MHz
Extended Temperature Operating Range up to -40°C to 125°C
Larger internal memory sizes
Larger external memory address space
Enhanced Flash security
Enhanced Interrupt Controller with fast interrupts
Higher-performance mixed-signal capability
Improved communication performance
Lower power consumption
Improved code density
Improved 32-bit performance
Improved EMI performance and features
Addition of Temperature Sensor
Improved CAN peripheral
Improved ADC accuracy and lower power consumption
GPIO has push-pull feature for improved keypad interface
Higher speed PWM with greater resolution at higher speeds and increased dead time range

5. Conclusions

5.1 An Exciting Time

With the introduction of the 56F8300 family, Motorola has provided a new level of performance and integration to Flash-based products. The 56F8300 family provides an excellent path for our current 8/16-bit MCU and 56F8xx customers to increased performance and features. The enhanced performance, memory, and features of the 56F8300 family enable a developer to expand his horizons with new product possibilities.

Motorola's wide range of offerings in its portfolio of Flash processors makes this a great time to be a developer. Today, as never before, customers have Flash processors at their disposal to develop new and exciting products. The features and performance of the 56F8300 offer exceptional value to Motorola's customers.

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